Doctoral Thesis

A Study on the Reliability of Metal Gate–La_2O_3 Thin Film Stacked Structures

(Summary of Doctoral Thesis)

Joel Molina Reyes

March 2007

Principal Supervisor: Professor **Hiroshi Iwai**

Associate Supervisor: Visiting Professor **Nobuyuki Sugii**

Abstract

This work discusses charge trapping effects and the dielectric reliability of metal-gated La_2O_3 stacked dielectrics. It will be shown that the gate stacks suffer from severe charge trapping, which causes adverse effects on the characteristics of La_2O_3-gated MIS devices like flat band Vfb and threshold voltages Vth shifts after stress. On the other hand, the lifetime projection of La_2O_3 after time-dependent dielectric breakdown measurements (TDDB) guarantees a 10 years operation period for La_2O_3-gated MIS devices at low gate voltages before breakdown. That latter result encourages us to look for alternative ways to minimize the electrical degradation found in La_2O_3-gated MIS devices after stress, whether by modifications in the deposition process of La_2O_3 or by introducing post-deposition processes like thermal treatments before and after the metallization step. Moreover, the problem of IL formation atop the silicon substrate still is a great challenge to be solved since La_2O_3 tends to develop this lower-k IL when deposited on silicon, thus increasing the final equivalent oxide thickness (EOT) of the whole high-k/IL stacked structure. Because of this La_2O_3–IL stack formation, the deterioration of the oxide stack will depend on the nature of these layers as well as the nature of the injected species (electrons or holes) under stress.

From carrier separation measurements, substrate electron injection results in a shorter time to oxide breakdown t_{bd} as compared to gate electron injection. Nevertheless, longer t_{bd} for La_2O_3/IL as well as smaller degradation of its electrical characteristics with time were obtained after improving the deposition process and post-deposition process for this oxide. Specifically, an *in-situ* metallization for La_2O_3 minimizes the exposition of La_2O_3 surface to environment and post-metallization annealing (PMA), can help to reduce the damage introduced into La_2O_3 and its interfaces after the deposition by sputtering of the gate electrode, thus increasing the final reliability of La_2O_3-gated MOS devices. Further improvements on the physical characteristics of La_2O_3 will increase its reliability so that this dielectric material will have good chances to replace conventional gate oxides well beyond the 45 nm node since the fabrication of La_2O_3-gated MIS devices with EOT < 1 nm has been already demonstrated.

Organization of this study

This dissertation consists of seven chapters which are described schematically in fig. 1.

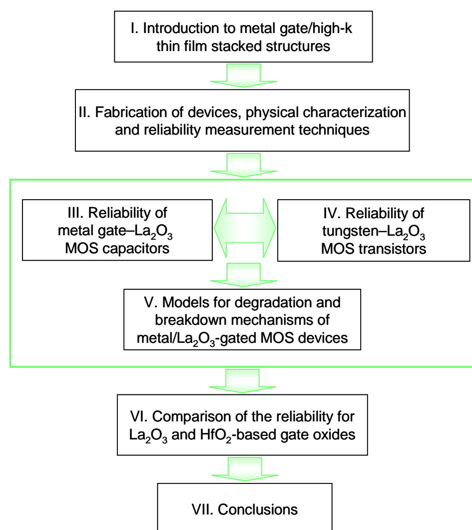


Figure 1 Outline of this dissertation.

Chapter 1

This chapter reviews and briefly discusses the long recognized necessity of replacing conventional gate oxides (SiO_2-based) with the Metal/high-k gate stack structure in order to continue the scaling down of CMOSFET devices. The requirements for metal gates and high-k materials are discussed along with a brief review of the rare-earth oxides (REO) that are being considered as potential candidates for the replacement of SiO_2. Also, the main research problems that have been found for the development of La_2O_3-based dielectrics at Iwai Lab are discussed here, see fig. 2. Next, some results obtained at Iwai Lab are presented and then, the reasons about the significance of researching the reliability properties of La_2O_3 are presented.

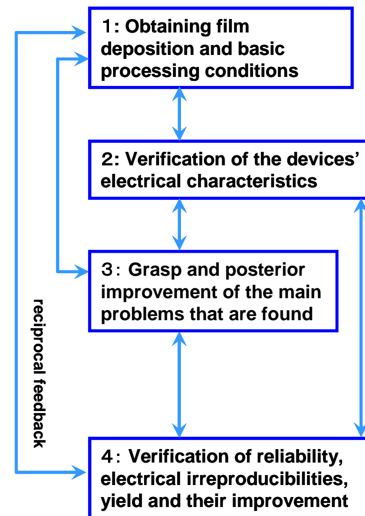


Figure 2 Main research problems to be solved.

This is followed by the introduction to La_2O_3 which is a member of the REO family, and the motivations that this material poses over other high-k dielectric materials.

Chapter 2

Here, we describe the fabrication and characterization methods used throughout this study. Detail fabrication flows of MOSCAP and MOSFET as well the basic principles behind all fabrication equipments were briefly discussed. The measurement setups and characterization methods used in this study were also mentioned, taking especial emphasis on the reliability characterization techniques (see table 1) that were applied to our fabricated

samples. The electrical stress for the La_2O_3-gated MOS devices was applied by: a ramped (TZDB) or constant voltage stress (TDDB). The measurement setup for interface-states density Dit after stress is also presented. Dit was obtained after charge-pumping measurements. The carrier separation measurement was also introduced in order to obtain a clearer vision on the phenomena of La_2O_3 degradation/breakdown since this technique is able to separate the individual contributions of tunneling electrons and holes flowing thorough the stacked oxide.

Table 1 Methods for reliability measurement of metal/La_2O_3-gated MOS devices.

Measurement	Obtained data
TZDB	Breakdown strength, SILC
TDDB	Oxide lifetime, Tbd, Qbd, SILC, Vfb and Vt shift
Charge pumping	Interface-states density Dit
Carrier separation	Ielectrons, Iholes, BKD mechanism

Depending on the intensity of the applied stress, electrically-induced degradation (SILC, Dit generation, Vth shift, etc) and/or breakdown condition (hard breakdown) can be reached within La_2O_3.

Chapter 3

This chapter presents the results obtained from reliability characterization of metal- La_2O_3 MOS capacitor devices under low and high-voltage stressing conditions. The shift in flat-band voltage Vfb for low or high-stressing conditions showed electric-field dependence after stress. By stressing La_2O_3 with TDDB, the degradation/breakdown of the dielectric will produce different effects on the final electrical characteristics of the stressed devices. First, the measurements of Vfb shift after stress for thick ad thin films were quantized and both results are shown in fig. 3.

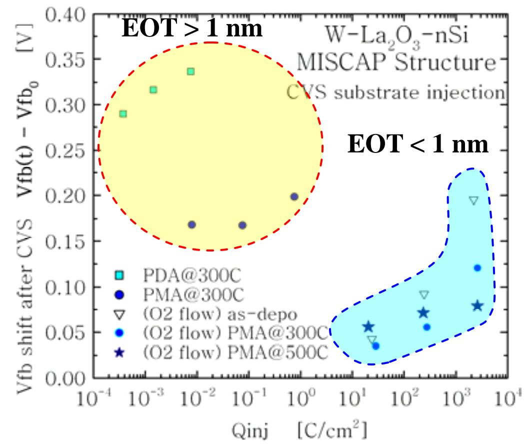


Figure 3 Vfb shift after stress for La_2O_3.

It is clearly seen that thinner films with a modified La_2O_3 deposition process shows better reliability characteristics regarding to Vfb shift after substrate injection of electrons into the oxide. This shift in Vfb can be reduced depending on the processing conditions applied for La_2O_3. The use post-metallization annealing (PMA) was of great help in order to reduce Vfb shift after stress (as compared to post-deposition annealing PDA) so that better reliability properties were obtained. We also stressed the dielectric with higher and longer stressing conditions so that HBD condition would develop in order to obtain the lifetime of La_2O_3-gated capacitors and the required density of charge for breakdown Qbd. By extrapolating the obtained lifetime data to lower operation

voltages, lifetime expectancy for La_2O_3 of 10 years was predicted by using the linear Vg model, see fig. 4. PMA increases the lifetime expectancy of La_2O_3 compared to PDA thermal treatment.

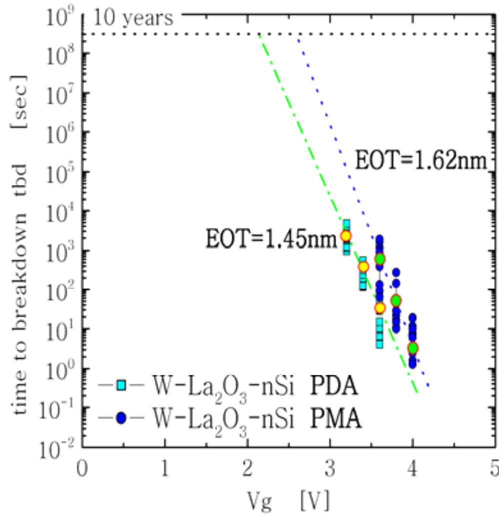


Figure 4 Lifetime projection for W-La_2O_3 gated MOSCAP after PDA/PMA annealing.

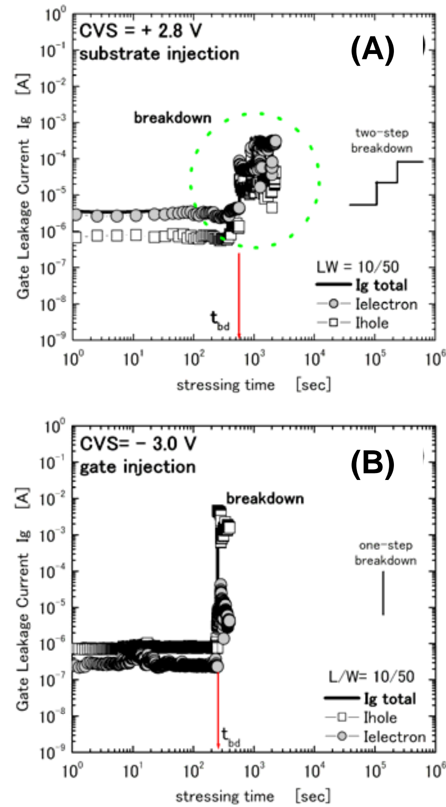


Figure 5 Evolution of gate leakage current with stressing time. (A) $I_{electron}$ is the dominant component of the total Ig during substrate injection of electrons. (B) I_{hole} is the dominant component of the total Ig during gate injection of electrons.

Chapter 4

This chapter presents the results of applying electrical stress on the gate of La_2O_3-gated MOSFET devices. In MOS transistors, it is possible to monitor not only the gate current Ig but also the substrate current I_{bulk} simultaneously. This is a well-known technique usually referred to as carrier separation that allows identifying the dominant carrier type on the gate leakage current. From carrier separation measurements it was observed that electron injection was the dominant component of total gate leakage current Ig under positive TDDB whereas hole injection was the dominant component under negative TDDB, see fig. 5 A-B.

Also, since the degradation of La_2O_3 involves both interfaces of the oxide with the metal and the silicon substrate, measurements of interface-state density Dit after stress were performed in order to correlate Vth shift with respect to Dit. The results are shown in fig. 6. Electrically-induced Dit generation after constant voltage stress (CVS) is almost zero for La_2O_3 and the use of forming gas (FG) during the PMA processing reduces the initial level of Dit, which indicates that some of the dangling bonds at the silicon surface have been passivated. The shift in Vth for nMOSFET and pMOSFET devices is shown in fig. 7 A-B.

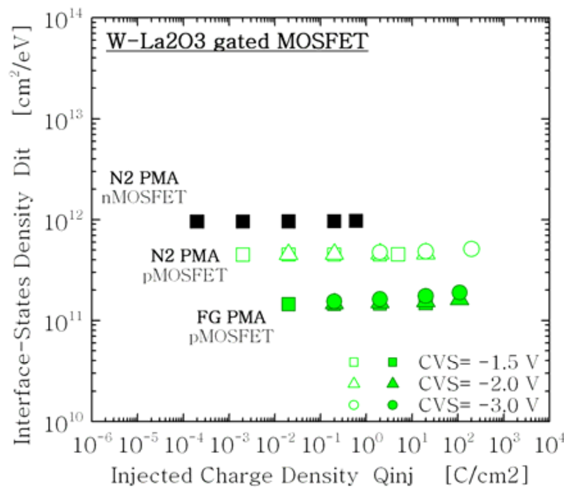


Figure 6 Interface-states Dit measurements for nMOSFETs and pMOSFETs devices after positive and negative CVS respectively.

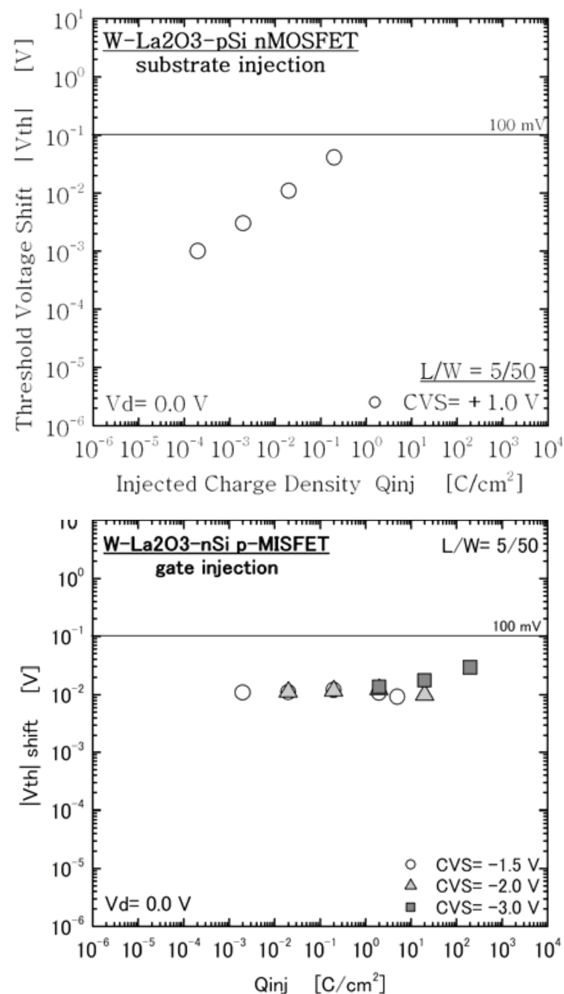


Figure 7 Evolution of Vth shift with injected charge. (A) nMOSFET devices show an exponential shift in Vth after stress. (B) pMOSFET devices show almost no change in Vth in the same way as in the Dit generation case.

From fig. 7 A-B we can see that for pMOSFET devices, the change in Vth during stressing is very small compared to the exponentially increasing shift in Vth for nMOSFETs. The shift in Vth for the nMOSFET device would come by the increase in fixed charge (Qf) instead of the almost zero Dit after stress.

Chapter 5

In this chapter, the previous results from the reliability characterization of La_2O_3-gated MOSCAP and MOSFET devices are joined in order to develop a more concise model explaining the mechanisms behind the degradation and breakdown of the La_2O_3-IL stacked layers on silicon; see fig. 8.

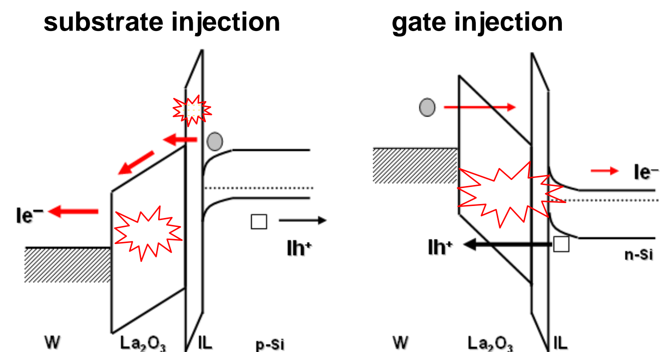


Figure 8 Proposed models for the breakdown of La_2O_3-gated MOS devices during substrate/gate injection conditions after positive/negative CVS.

At this stage, it has been concluded that during substrate injection, La_2O_3 presents IL breakdown followed by the breakdown of the La_2O_3 film. For the gate injection case, simultaneous breakdown of both the IL and the La_2O_3 film is proposed. Lastly, we briefly propose methods to improve reliability so that better projections and enhanced degradation

and lifetime characteristics of La_2O_3 after stress can be obtained.

Chapter 6

Here, a comparison of the reliability properties for Hf-based oxides and La_2O_3 is presented. In order to predict the reliability of the La_2O_3 dielectrics for use of the gate insulator, the published data for that of HfO_2-based oxides were examined and compared with that of the La_2O_3. In general, the La_2O_3 dielectrics show higher reliability than that of HfO_2-based dielectrics, although some of the reliability evaluations have not been carried out for the La_2O_3. Better SILC, Dit generation, Vth shift after stressing and time to breakdown data has been found for La_2O_3-gated MOS devices as compared to HfO_2. On the other hand, the published data in the journal and the conference predict not sufficient reliability for the Hf-based oxide to be used in commercial products. However, Intel announced Hf-based high-k gate oxide introduction into the 45 nm CMOS with sufficiently high reliability which meets the commercial production thus the reliability of the Hf-based oxides with EOT down to sub 1 nm seems to have been already established, fig. 9 below.

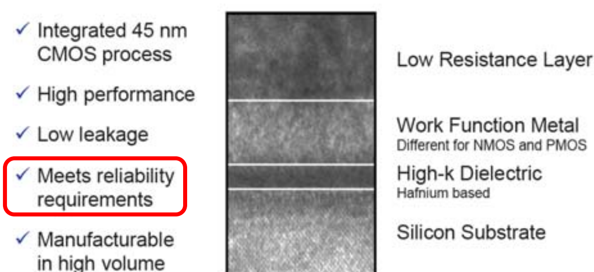


Figure 9 Metal gate/high-k (Hf-based) stacked architecture developed by Intel and which meets the reliability requirements for commercial production.

At this moment, any fundamental problems for the reliability of La_2O_3 dielectrics have not been found by this study; see table 1 below.

Table 1 Summary of the reliability results for HfO_2 and La_2O_3-gated MOS devices.

Property \ Material	La_2O_3* EOT [nm]	HfO_2-based EOT [nm]
SILC degradation	Estimated to be acceptable [1.5 nm]	To be a problem [1.5 nm]
Dit generation	Estimated to be acceptable [1.6 nm]	To be a problem [1.7 nm]
Vth shift	Estimated to be acceptable [1.6 nm]	To be a problem [1.8 nm]
t_{bd}, Q_{bd}	Estimated to be acceptable [1.5 nm]	Estimated to be acceptable [1.5 nm]
HCI	?	Very poor

* High-temperature reliability measurements are needed.

Thus, it is expected that the La_2O_3 reliability will meet the requirements for the production by the time when it is introduced into commercial devices.

Chapter 7

This chapter summarizes the findings and contributions of this study for the analysis of the reliability characteristics of La_2O_3-gated MOS devices. It was found that by using appropriate metal gate–La_2O_3 stacks in conjunction with thermal treatments, the problem of higher leakage current for low EOT could be substantially decreased. This has been achieved by avoiding the formation of an interfacial layer at the metal–La_2O_3 interface by using tungsten as the gate electrode. Because of the La_2O_3–Silicon interfacial layers formation by annealing, the deterioration of the La_2O_3 gate stack will depend on the nature of these layers as well as the nature of the injected species (electrons or holes) under the stress. In

this respect, and from carrier separation measurements, the substrate injection of electrons degrades more severely the conduction characteristics of the La_2O_3–IL stack, where the IL degrades more severely during the stress. A longer lifetime for the breakdown of La_2O_3 as well as smaller degradation of its electrical characteristics with time were obtained after improving the deposition process and post-deposition process for this oxide. An in-situ metallization for La_2O_3 enhances its reliability by minimizing the exposition of La_2O_3 surface to environment. On the other hand, by comparing the reliability properties of La_2O_3-gated MOS devices with those of HfO_2-based gate oxides both with similar EOT, very important differences were found. It was observed that during SILC degradation, less degradation in gate leakage current after stress is found for La_2O_3-gated MOSCAP at the same EOT. Similarly, even though La_2O_3 presents an initially higher density of interface-states Dit, the generation of additional Dit is lower compared to HfO_2, in which an exponential generation of Dit is observed. With La_2O_3, additional Vth shift after electron injection is minimized. By comparing TDDB lifetime extrapolation data, a 10 years operation before breakdown for both high-k materials is guaranteed even at relatively high Vg $>$ 1 V. Regarding to the breakdown models for these oxides, it was found that during substrate injection, a Hf-based system experiences high-k bulk breakdown whereas La_2O_3 shows interfacial-layer (IL) breakdown followed by the breakdown of La_2O_3 itself. During the gate injection condition, a Hf-based system mostly experiences IL breakdown whereas La_2O_3 shows complete IL + high-k breakdown simultaneously. All the former results suggest that La_2O_3-gated MOS devices have an advantage over HfO_2 since better reliability results have been demonstrated for La_2O_3–gated devices at very similar EOT levels. By using very thin high-k films with EOT $<$ 1nm we have identified a large SILC increase for La_2O_3-gated devices so that it is thought that the degradation-related reliability of very thin La_2O_3 gate oxides becomes compromised but their final lifetime before breakdown would remain within the specifications. Finally, even though the reliability results for HfO_2-based gate oxides with EOT $<$ 1nm that are found in the published literature are not good enough, the production of Hf-based MOSFET products for the 45 nm node announced by Intel make us think that the reliability issues for EOT $<$ 1nm have already been resolved.

Doctoral Thesis

A Study on the Reliability of Metal Gate–La_2O_3 Thin Film Stacked Structures

A DISSERTATION SUBMITTED TO THE
DEPARTMENT OF ADVANCED APPLIED ELECTRONICS
INTERDISCIPLINARY GRADUATE SCHOOL OF
SCIENCE AND ENGINEERING
TOKYO INSTITUTE OF TECHNOLOGY
FOR THE DEGREE OF
DOCTOR OF ENGINEERING

Joel Molina Reyes

March 2007

Principal Supervisor: Professor **Hiroshi Iwai**

Associate Supervisor: Visiting Professor **Nobuyuki Sugii**

Tokyo Institute of Technology

Contents

Contents II

List of tables VI

List of figures VII

Abstract of this doctoral thesis XIX

CHAPTER 1 INTRODUCTION TO METAL GATE/HIGH-K THIN FILM STACKED STRUCTURES 1

1.1 Brief summary of the history of semiconductor devices 2
1.2 Beyond SiO_2-based CMOS device scaling 2
1.3 Requirements for metal gates and high-k materials 6
1.4 Review of rare-earth metal oxides 9
1.5 Observations regarding the development of La_2O_3 films 11
1.6 Motivations for using La_2O_3 as high-k material 18
1.7 Objectives and organization of this study 20
References 24

CHAPTER 2 FABRICATION OF DEVICES, PHYSICAL CHARACTERIZATION AND RELIABILITY MEASUREMENT TECHNIQUES 27

2.1 Introduction 28
2.2 MOS capacitor and MOSFET fabrication 29
2.3 Fabrication process 34
2.3.1 Si surface cleaning and preparation 34
2.3.2 E-beam evaporation of La_2O_3 36
2.3.3 Low temperature annealing by rapid-thermal anneal (RTA) 37
2.3.4 Deposition of metals for gate electrodes 39
2.3.4.1 Thermal evaporation of Al gate electrode 39
2.3.4.2 E-beam evaporation of Pt gate electrode 40
2.3.4.3 RF-sputtering of Ta, Ru and W gate electrodes 41

2.3.5 Metal gate and La_2O_3 etching 42
2.3.6 Photolithography 43
2.4 La_2O_3 deposition in O_2 ambient with *in-situ* metallization 44
2.5 Physical characterization 45
2.5.1 Spectroscopic ellipsometry 45
2.5.2 Transmission electron microscopy 47
2.5.3 X-ray photoelectron spectroscopy (XPS) 49
2.6 Electrical characterization 51
2.6.1 C-V measurement 52
2.6.2 Ig-Vg measurement 53
2.6.3 Threshold voltage (Vth) determination 53
2.6.4 Charge pumping for interface-state density (Dit) measurement 54
2.7 Reliability measurement techniques 56
2.7.1 TZDB and TDDB measurements 57
2.7.2 Stress Induced Leakage Current (SILC) 59
2.7.3 Charge pumping (CP) measurement 60
2.7.4 Carrier separation (CS) measurement 62
References 64

CHAPTER 3 RELIABILITY OF METAL GATE–La_2O_3 MOS CAPACITORS .. 65

3.1 Introduction 66
3.2 Influence of post-deposition annealing (PDA) 67
3.3 Influence of post-metallization annealing (PMA) 69
3.4 Evaluation of the metal gate electrode material 72
3.5 C-V and I-V characterization 78
3.6 Breakdown and reliability of metal gate–La_2O_3 thin films after post-deposition annealing in N_2 84
3.7 Charge trapping characteristics of W-La_2O_3-nSi MOSCAP after post-metallization annealing in N_2 97
3.8 Degradation and breakdown of W-La_2O_3 stack after post metallization annealing in N_2 126
3.8.1 Observations regarding breakdown of La_2O_3 134
3.9 La_2O_3 post-breakdown I-V and I-t characteristics 138
3.9.1 Switching and noisy behavior of Ig during stress 138
3.9.2 Propagation of the breakdown event 140
3.9.3 SILC-SBD-HBD of La_2O_3-gated MOSCAP 142
3.10 Summary 143
References 146

CHAPTER 4 RELIABILITY OF TUNGSTEN–La_2O_3 MOS TRANSISTORS ... 154

4.1 Introduction ………… 155
4.2 Threshold voltage shift (ΔVth) ………… 156
4.2.1 Influence of Vth shift on drain current Id ………… 163
4.2.2 Influence of drain voltage on Vth shift ………… 167
4.3 Interface-state density (Dit) measurement after stress ………… 174
4.4 Comparison of degradation by substrate injection with that by gate injection ………… 183
4.5 Carrier separation measurements ………… 186
4.6 Carrier separation and Vth measurements of W-La_2O_3 gated MOSFET structures after electrical stress ………… 197
4.7 Summary ………… 203
References ………… 206

CHAPTER 5 MODELS FOR DEGRADATION AND BREAKDOWN MECHANISMS OF METAL/La_2O_3–GATED MOS DEVICES ………… 209

5.1 Introduction ………… 210
5.2 Carrier injection in the La_2O_3-SiO_2 system ………… 212
5.3 Trap creation and interface-state generation ………… 217
5.4 Failure modes for degradation of La_2O_3-SiO_2 stack ………… 218
5.4.1 Stress-induced leakage current SILC ………… 219
5.4.2 Charge trapping-detrapping degradation ………… 222
5.4.3 Soft-breakdown (SBD) ………… 223
5.4.4 Hard-breakdown (HBD) ………… 224
5.4.5 Progressive breakdown (PBD) ………… 225
5.5 Towards a unified vision of breakdown in La_2O_3-SiO_2 dual layers …… 231
References ………… 234

CHAPTER 6 COMPARISON OF THE RELIABILITY FOR La_2O_3 AND HfO_2-BASED GATE OXIDES ………… 237

6.1 Main reliability results for Hf-based oxides ………… 238
6.2 Comparison of reliability between La_2O_3 and Hf-based oxides …… 247
6.2.1 SILC degradation ………… 247

6.2.2 Interface-states Dit generation ………………………………….. 248
6.2.3 Threshold voltage Vth shift ………………………………….. 249
6.2.4 Time to breakdown t_{bd} …………………………………………… 249
6.2.5 Breakdown models for substrate and gate injection …………….. 250
6.3 Remaining problems for the reliability of La_2O_3 gate insulator MOSFETs ……………………… 253
6.4 Summary ………………………………………………………… 255
References ……………………………………………………………….. 256

CHAPTER 7 CONCLUSIONS …………………………………………… 259

7.1 Conclusions ………………………………………………………… 260
7.2 Recommendations for future works ………………………………….. 267

List of publications and presentations …………………………………………… 269

Acknowledgements ………………………………………………………… 272

List of tables

Table 1.1 Scaling rules for constant-field scaling.

Table 1.2 Physical properties of the metals used in this thesis.

Table 2.1 Sources and related effects of various contaminations.

Table 3.1 Obtained reliability data depending on the severity of the applied stress.

Table 6.1 Summary of the reliability results for HfO_2 and La_2O_3-gated MOS devices.

Table 6.2 Summary of the reliability results for HfO_2 and La_2O_3-gated MOS devices when EOT < 1nm.

List of figures

Chapter 1

Fig. 1.1 Cross-sectional sketch to show that the MOSFET gate capacitance Cg is made up of three capacitances in series: the oxide capacitance Cox, the capacitance due to the poly-Si depletion effect C_{pd} and a capacitance due to the finite thickness of the conducting channel C_{inv}.

Fig. 1.2 Schematic of direct tunneling through a SiO_2 layer and the more difficult tunneling through a thicker layer of high-k oxide.

Fig. 1.3 (A) Static dielectric constant versus band gap for candidate gate oxides.
(B) Band gap for the REO of the lanthanide series.

Fig. 1.4 Identification of some of the main problems to be solved for the posterior development of La_2O_3-based high-k materials within Iwai laboratory.

Fig. 1.5 Gate leakage current density versus EOT at Vg= 1 V for high-k materials. Several other high-k dielectric materials are compared to La_2O_3 results obtained at Iwai Lab.

Fig. 1.6 Effective mobility versus effective electric field for La_2O_3-gated n-channel MOSFET. Very high electron mobility along with very low interface-states density Dit was obtained.

Fig. 1.7 Normalized capacitance versus gate voltage for HfO_2 and La_2O_3-gated MOS devices on silicon. Fermi level pinning is observed only for the HfO_2-based MOS device samples.

Fig. 1.8 (A) Band offsets of several high-k candidates with silicon. Band offsets for La_2O_3 are shown in red.
(B) Gate leakage current density of La_2O_3-based oxides compared to Hf-based oxides.

Fig. 1.9 Outline and organization of this dissertation.

Chapter 2

Fig. 2.1 (A) Standard deposition of La_2O_3 for the fabrication of MOS capacitors.
(B) Use of SiO_2-based spacers for the standard and modified deposition of La_2O_3.

Fig. 2.2 (A) Top and cross-sectional views of MOS capacitors after standard deposition of La_2O_3.
(B) Top and cross-sectional views of MOS capacitors after deposition of La_2O_3 using SiO_2-based spacers in order to reduce exposure to moisture through lateral regions of gate area.

Fig. 2.3 (A) Simplified process flow for La_2O_3-gated MOS capacitors after standard deposition.
(B) Simplified process flow for La_2O_3-gated MOS capacitors after modified deposition.

Fig. 2.4 (A) La_2O_3-gated MOSFET fabrication flow (only in-situ metallization and PMA processing).
(B) Micrograph of W-La_2O_3 gated MOSFET structure (L/W = 10/50 μm).
(C) Cross-sectional view of the MOSFET structure shown in (B).

Fig. 2.5 Si wafer cleaning and surface preparation steps.

Fig. 2.6 (A) Photograph of MBE chamber 1 used for the deposition of La_2O_3 on Si.
(B) Schematic of the La_2O_3 deposition within MBE chamber with UHV.

Fig. 2.7 Schematic drawing of MILA-3000 RTA system.

Fig. 2.8 (A) Photograph of RTA system MILA-3000 used for the annealing of La_2O_3 on silicon.
(B) Photograph of RTA system QHC-P610C used for the annealing of La_2O_3 on silicon.

Fig. 2.9 Schematic drawing of bell-jar type thermal evaporator system.

Fig. 2.10 Schematic drawing of Pt-based e-beam evaporation system.

Fig. 2.11 Schematic drawing of a typical RF sputtering system.

Fig. 2.12 Photolithography process flow.

Fig. 2.13 Schematic setup of an ellipsometry experiment.

Fig. 2.14 (A) TEM of W-La_2O_3 without O_2 flow during deposition (as-depo).
(B) TEM of W-La_2O_3 with O_2 flow during deposition (as-depo).

Fig. 2.15 Basic components of a monochromatic XPS system.

Fig. 2.16 Annealing temperature dependence of Si 1s XPS spectrum of La_2O_3 deposited within oxygen flow. A La-silicate IL formation is present for all samples whereas an additional SiO_2-based IL formation appears for PMA at 500°C.

Fig. 2.17 Linear extrapolation for Vth extraction from Id-Vg curve.

Fig. 2.18 Charge pumping measurement setup for the extraction of Dit.

Fig. 2.19 (A) TZDB I-V plot. Vg increases until La_2O_3 reaches breakdown at V_{bd} the breakdown voltage.
(B) TDDB I-t plot. For a fixed Vg, Ig evolves with time until breakdown occurs at t_{bd}.

Fig. 2.20 (A-F) Device cross-sections and energy band diagrams for charge pumping measurements. The figures are explained in the text.

Fig. 2.21 (A) CS measurement for nMOSFETs in inversion (positive CVS). Both electron and hole current components are detected at the gate and substrate respectively.
(B) CS measurement for pMOSFETs in inversion (negative CVS). Even though both electrons and holes tunnel simultaneously through the gate oxide, only the hole current component is illustrated flowing through the oxide for clarity purposes. Both hole and electron current components are detected at the gate and substrate respectively.

Chapter 3

Fig. 3.1 C-V characteristics of Al-La_2O_3 gated MOSCAP after PDA in N_2 ambient at different temperatures (300°C– 800°C).

Fig. 3.2 Changes in physical thickness for La_2O_3 after several PDA temperatures.

Fig. 3.3 W-La_2O_3 gated MOSCAP before and after thermal treatment in N_2 ambient at 300°C. PDA and PMA thermal treatments are both compared to the as-depo condition.

Fig. 3.4 TEM of an aluminum-gated La_2O_3 MOSCAP after PMA in N_2 at 300°C (10 min.). The existence of a low-k Al_2O_3-based IL at the Al–La_2O_3 interface is shown.

Fig. 3.5 (A) TEM of W-La_2O_3 without O_2 flow during deposition (as-depo).
(B) TEM of W-La_2O_3 with O_2 flow during deposition (as-depo).

Fig. 3.6 TEM of W-La_2O_3 without O_2 flow during deposition (PMA).

Fig. 3.7 C-V characteristics of La_2O_3 gated with different gate metals.

Fig. 3.8 C-V characteristics of Ru-gated La_2O_3 before and after PDA at different temperatures. The large variations between samples exist even for the PDA@800°C samples.

Fig. 3.9 J-V characteristics of Ru-gated La_2O_3 before and after PDA at different temperatures. It is clearly seen that there is almost no reproducibility in Jg even for the same sample.

Fig. 3.10 J-V characteristics of Al and Ru-gated La_2O_3 after PDA in N_2 at 400°C. The use of a higher work function metal leads to a reduced density of leakage current (gate injection). The inset shows the difference in barrier height for electrons during gate injection.

Fig. 3.11 C-V characteristics of metal–La_2O_3 after PDA/PMA in N_2. Even though lower EOT can be achieved with other metals, W gets the more stable and reproducible characteristics.

Fig. 3.12 C-V and I-V characteristics of Al–La_2O_3 before and after PDA in N_2.

Fig. 3.13 (A) Variation of some physical and electrical characteristics of Al–La_2O_3 stacked structure before and after PDA in N_2.
(B) Jg-EOT plot for the same Al–La_2O_3 stacked structure.

Fig. 3.14 J-V characteristics for Al-gated La_2O_3 stacked on p and n-type silicon. La_2O_3 physical thickness ~ 4.3 nm for as-depo condition on both Si substrates.

Fig. 3.15 Jg-EOT plot for some of the Metal-La_2O_3 stacked MOS structures evaluated in this dissertation. Jg is taken at |1V|.

Fig. 3.16 (A) I-V data for Ru-La_2O_3-stacked MOSCAP showing the Ig switching characteristic during TZDB stressing conditions. The trapping-detrapping processes occur before the HBD condition is reached.
(B) I-t characteristic for W-La_2O_3 MOSCAP. Here, the trapping-detrapping processes occur after the HBD condition. The switching characteristic of Ig can be confirmed once the La_2O_3-IL stack breakdown.

Fig. 3.17 (A) I-V characteristic of La_2O_3-gated MOSCAP showing the propagation of the breakdown spot as a gradual "jump"-like increase in leakage current Ig.
(B) I-t characteristic for a different sample with the same structure in (A). The propagation of the breakdown spot is clearly visible as the tiny jumps in Ig after breakdown.

Fig. 3.18 (A) I-V characteristic of La_2O_3-gated MOSCAP. The effect of the severity of stress on gate leakage current Ig is clearly shown (in real devices lower stress fields are expected).
(B) I-t characteristic showing the effect of stress on the evolution of leakage current with time. The occurrences of SILC-SBD-HBD are highlighted both in the I-V and I-t data.

Chapter 4

Fig. 4.1 (A) ΔVth after CVS= 1V. Vth totally shifts to the left side in proportion to injected charge Qinj.
(B) ΔVth after CVS= 1.5V. Vth continues to shift to left side until a SBD event takes place.
(C) ΔVth after CVS= 2V. Vth increases to more positive values until SBD events changes this trend.

Fig. 4.2 Vth shift versus injected charge density Qinj for W-La_2O_3 gated nMOSFETs after low to high positive stressing CVS conditions.

Fig. 4.3 (A) ΔVth after CVS= -1.5V. Vth totally shifts to the left side in proportion to injected charge Qinj.
(B) ΔVth after CVS= -2.0V. Vth continues to shift to left side as expected for pMOSFETs.
(C) ΔVth after CVS= -3.0V. ΔVth gradually increases during this higher CVS condition.

Fig. 4.4 Vth shift versus injected charge density Qinj for W-La_2O_3 gated pMOSFETs after low to high negative stressing CVS conditions.

Fig. 4.5 (A) Id-Vd plot for W-La_2O_3 gated nMOSFET before and after a positive and relatively low CVS.
(B) Id-Vd plot showing the effect that a SBD event have on drain current Id.
(C) Id-Vd plot with the expected trend in Id under high-stressing conditions and the effect of SBD.

Fig. 4.6 (A) Simplified Id-Vg diagram showing the effect of negative ΔVth after stress.
(B) Simplified Id-Vg diagram showing the effect of positive ΔVth after stress.

Fig. 4.7 Schematic of nMOSFET with both Vg and Vd polarization during CVS. The total gate leakage current Ig is now reduced in proportion to Vd.

Fig. 4.8 Hot carrier generation, current components, and electron injection into the La_2O_3-IL stacked oxide structure.

Fig. 4.9 Vth shift versus injected charge density Qinj for W-La_2O_3 gated nMOSFETs after both low positive CVS and Vd stressing conditions.

Fig. 4.10 Log-log plot of the data presented in fig. 4.9.

Fig. 4.11 (A) Gate leakage current Ig versus stressing time. Ig reduces in proportion to drain voltage Vd.
(B) In order to reach the same injected charge density, more time is necessary for the sample with a decreased Ig (higher Vd). The final effect is a stronger dependence of ΔVth with Qinj.

Fig. 4.12 Drain current Id increases with Vd until saturation occurs when the channel is cut-off at Vdsat (pinch-off condition).

Fig. 4.13 Schematic of the charge pumping (CP) technique. CP is able to measure recombined charges at the substrate Isub=Icp.

Fig. 4.14 Timing chart of square pulse method for CP measurement.

Fig. 4.15 (A) Log-log plot of ΔVth versus injected charge density Qinj for nMOSFET under positive CVS. A linear relationship between ΔVth–Qinj is observed in this plot.
(B) Interface-states density Dit measured at the maximum substrate current Isub after positive stressing measurements. A log-log plot shows no correlation of ΔVth with injected charge density. The inset shows a linear-log plot of the same data for comparison.

Fig. 4.16 Same data as presented in fig. 4.4.

Fig. 4.17 Dit versus Qinj for pMOSFET after negative CVS. Independently of the CVS applied, the change in Dit after stress is almost constant. The inset shows a linear-log plot of these data for comparison purposes.

Fig. 4.18 (A) Dit-Vbase plot for W-La_2O_3 gated pMOSFET after negative CVS= -1.5 V.
(B) Dit-Vbase plot for W-La_2O_3 gated pMOSFET after negative CVS= -2.0 V.
(C) Dit-Vbase plot for W-La_2O_3 gated pMOSFET after negative CVS= -3.0 V.

Fig. 4.19 (A) Log-log plot of ΔVth versus Qinj for pMOSFET under negative CVS and FG-based PMA. As before, identical behavior for these pMOSFETs is obtained but the initial levels of Vth are slightly lower than those found in N_2-based PMA devices.
(B) A log-lo plot of Dit vs. Qinj after stress shows lower levels of Dit as

compared to those found in N_2-based PMA devices. It is thought that FG-based PMA is able to reduce the initial density of dangling bonds so that lower changes in Dit with stress are obtained.

Fig. 4.20 (A) Schematic diagram showing nMOSFETs stressed with a positive CVS. The flow of both electrons and holes currents are measured at the gate and substrate respectively.
(B) The energy band diagram shows that positive CVS implies injection of electrons directly from the substrate (via the inverted channel) into the IL-La_2O_3 stacked structure.

Fig. 4.21 (A) Schematic diagram showing nMOSFETs stressed with a positive CVS. The flow of both electrons and holes currents are measured at the gate and substrate respectively.
(B) The energy band diagram shows that positive CVS implies injection of electrons directly from the substrate (via the inverted channel) into the IL-La_2O_3 stacked structure.

Fig. 4.22 (A) CS measurement for nMOSFETs in inversion (positive CVS). Both electron and hole current components are detected at the gate and substrate respectively.
(B) CS measurement for pMOSFETs in inversion (negative CVS). Even though both electrons and holes tunnel simultaneously through the gate oxide, only the hole current component is illustrated flowing through the oxide for clarity purposes.

Fig. 4.23 (A) Ig versus Vg plot for nMOSFET before positive CVS (gate injection). After CS measurement, electrons were identified as the major contributors to gate leakage current.
(B) After positive CVS, the Ig-Vg shape remains almost unchanged. Because of the trapping of electrons at the bulk of La_2O_3, Ig gets slightly lower as compared to fresh condition.

Fig. 4.24 (A) Id versus gate voltage Vg. Same as the data presented in fig. 4.1C.
(B)(C)(D) CS measurement for gate leakage current under positive CVS= +2.0 V. The electron current is the main contributor to total leakage current with Ihole increasing with Qinj.
(E) After a SBD event occurs, the main contributor to Ig changes from electrons to holes for low electric fields and the final effect can be seen as a net increase in Ig as well.
(F) After SBD event, Ielectron is still dominant though Ihole increases well

above its fresh value.

Fig. 4.25 Ig-Vg plot for nMOSFET with higher Vg ramping stress. Several degradation steps occur before and after fatalistic HBD event appear.

Fig. 4.26 (A) Plot of CS measurement of Ig vs. Vg before and after negative CVS for pMOSFET. The injection of a smaller density of injected charge did not change the major contributor to Ig.
(B) Holes still are the major contributors to Ig before and after negative CVS. The injection of a relatively higher charge density increases Ig compared to its fresh value.
(C) Similarly, at the higher CVS condition, holes are the major components of Ig after inversion of pMOSFET and the fresh levels of Ig increases after stress indicating hole trapping in the oxide.

Fig. 4.27 (A) Evolution of gate leakage current (substrate injection) with stressing time. Ielectron is the dominant component of the total Ig. A two–step breakdown behavior is also observed.
(B) Evolution of gate leakage current (gate injection) with stressing time. Ihole is the dominant component of the total Ig. A one–step breakdown behavior is observed.

Chapter 5

Fig. 5.1 Schematic representation of the generation of failure modes with stressing time.

Fig. 5.2 Schematic representation of the thinned (IL BKD) oxide approach.

Fig. 5.3 Schematic representation of the percolation path between electrodes and formed within both La_2O_3 and IL lattices. For a dual-oxide, the polarization of applied stress is important to determine the “filling” of the first lattice trap sites by percolation traps and thus reach breakdown.

Fig. 5.4 Schematic representation of the breakdown “path” followed by the injection of electrons coming from the substrate. Once the stressing continues the whole layer breaks down.

Fig. 5.5 Schematic representation of the breakdown "path" followed by the injection of electrons coming from the gate. Once the stressing continues the whole layer breaks down.

Fig. 5.6 SILC measurement after positive CVS for thick and thin La_2O_3-IL stacks.
(A) EOT= 1.5 nm (normal La_2O_3 deposition).
(B) EOT= 0.74 nm (in-situ tungsten metallization)

Fig. 5.7 Relative change in leakage current induced by SILC (same data as in fig. 5.6 A-B).

Fig. 5.8 Left side plot shows an energy band diagram during CVS measurement (high voltage). During CVS, new energy levels of generated defects are created. Right side plot shows electrons tunneling inelastically through generated levels during SILC measurement.

Fig. 5.9 Left side plot shows the shift in Vth for La_2O_3-gated nMOSFETs stressed under low and high positive CVS. The change in direction of ΔVth with stress is clear. Right side energy band diagram models the degradation phenomena occurring within the oxide stack.

Fig. 5.10 Left side plot shows the evolution of leakage current with time under substrate injection conditions (positive CVS). At certain stressing time, the occurrence of a SBD event is detected. Right side energy band diagram models this degradation phenomenon as breakdown of the IL.

Fig. 5.11 Left side plot shows the evolution of leakage current with time under substrate injection conditions (positive CVS). At certain stressing time, the occurrence of a HBD event is detected. Right side energy band diagram models this degradation phenomenon as total breakdown of the stacked oxide.

Fig. 5.12 (A) Ig-Vg plot for La_2O_3-IL stack showing HBD characteristics and consequent propagation of the breakdown event with Vg. The post-breakdown current levels also increase in accordance to PBD.
(B) Ig-time plot for La_2O_3-IL stack showing HBD characteristics and consequent propagation of the breakdown event with time. During PBD, higher Ig is related to a larger size of the total breakdown spot.

Fig. 5.13 (A) The post-breakdown leakage current for nMOSFET in inversion shows a two-step breakdown.

(B) For pMOSFET, a single-step breakdown, along with higher levels for the post-breakdown Ig is obtained.

Fig. 5.14 (A) For substrate injection, the lateral breakdown propagation of the La_2O_3 layer (after IL breakdown) increases the post-breakdown Ig. Opening of new breakdown spots in La_2O_3 is also possible.
(B) In gate injection, higher post-breakdown Ig is related to the larger size in the breakdown spot within La_2O_3. PBD characteristics would be related to the widening/opening of same/new BKD spots.

Fig. 5.15 (A) Ig-Vg plot for W/La_2O_3-IL stacked MOSCAP before and after continuous stress under substrate injection. The effect of several degradation modes on leakage current is shown.
(B) Ig-time plot for W/La_2O_3-IL stacked MOSCAP before and after continuous stress under substrate injection. Again, the effect of the same degradation modes on leakage current is shown.

Chapter 6

Fig. 6.1 Summary of the main reliability problems found for Hf-based oxides deposited on silicon. Depending on the conditions of the stressing measurements and the advance of the electrical degradation, some reliability properties will be more compromised than others.

Fig. 6.2 SILC characteristics for several HfO_2-gated MOS devices.
(A) SILC characteristic for the Pt/HfO_2/Si system. EOT= 2.9 nm.
(B) SILC characteristic for the poly-Si/HfO_2/Si system. EOT= 1.8 nm.
(C) SILC characteristic for the poly-Si/HfO_2/Si system. EOT= 1.5 nm.
(D) SILC characteristic for the TaN/HfO_2/Si system. EOT= 0.9 nm.

Fig. 6.3 Dit-generation characteristic for HfO_2-gated MOS devices with similar EOT.
(A) Dit-generation for the poly-Si/HfO_2/Si system. EOT= 1.7 nm.
(B) Dit-generation for the TiN/HfO_2/Si system. EOT= 1.6 nm.

Fig. 6.4 Vth shift characteristic for HfSiON-gated MOS devices.
(A) Vth shift for the poly-Si/HfSiON/Si system. EOT= 1.24 nm.
(B) Vth shift for the poly-Si/HfSiON/Si system. EOT= 1.6 nm.

Fig. 6.5 Lifetime extrapolation of the time to breakdown data for HfO_2.
(A) Lifetime extrapolation for the poly-Si/HfO_2/Si system. EOT= 1.5 nm.
(B) Lifetime extrapolation for the TiN/HfO_2/Si system. EOT= 1.87 nm.

Fig. 6.6 (A) Proposed models for the degradation of HfO_2-gated MOS devices.
(B) When the degradation continues, the breakdown is modeled differently depending mainly on the polarity of the stress applied (gate and substrate injection of electrons)

Fig. 6.7 Structural features of the metal gate/high-k (Hf-based) stacks used by Intel and which is scheduled for commercial production of MOSFETs in the 45nm node during this year.

Fig. 6.8 (A) Less SILC degradation is found for La_2O_3 compared to HfO_2-gated MOS devices.
(B) SILC degradation for Hf-based oxides only. Exponential increase in Jg is clearly observed.

Fig. 6.9 Comparison of the observed Dit generation between HfO_2 and La_2O_3-gated devices during stress.

Fig. 6.10 Comparison of the observed Vth shift between HfO_2 and La_2O_3-gated devices during stress.

Fig. 6.11 Comparison of the observed time to breakdown data between HfO_2 and La_2O_3-gated devices

Fig. 6.12 (A) Comparison of the breakdown models for HfO_2 and La_2O_3 during substrate injection conditions.
(B) Comparison of the breakdown models for HfO_2 and La_2O_3 during gate injection conditions.

Abstract

This study discusses charge trapping effects and the dielectric reliability of metal-gated La_2O_3 stacked dielectrics. It will be shown that the gate stacks suffer from severe charge trapping, which causes adverse effects on the characteristics of La_2O_3-gated MOS devices like flat band Vfb and threshold voltages Vth shifts after stress. On the other hand, the lifetime projection of La_2O_3 after time-dependent dielectric breakdown measurements (TDDB) guarantees a 10 years operation period for La_2O_3-gated MIS devices at low gate voltages before breakdown. That latter result encourages us to look for alternative ways to minimize the electrical degradation found in La_2O_3-gated MIS devices after stress, whether by modifications in the deposition process of La_2O_3 or by introducing post-deposition processes like thermal treatments before and after the metallization step. Moreover, the problem of IL formation atop the silicon substrate still is a great challenge to be solved since La_2O_3 tends to develop this lower-k IL when deposited on silicon, thus increasing the final equivalent oxide thickness (EOT) of the whole high-k/IL stacked structure. Because of this La_2O_3–IL stack formation, the deterioration of the oxide stack will depend on the nature of these layers as well as the nature of the injected species (electrons or holes) under stress. From carrier separation measurements, substrate electron injection results in a shorter time to oxide breakdown t_{bd} as compared to gate electron injection. Nevertheless, longer t_{bd} for La_2O_3/IL as well as smaller degradation of its electrical characteristics with time were obtained after improving the deposition process and post-deposition process for this oxide. Specifically, an in-situ metallization for La_2O_3 minimizes the exposition of La_2O_3 surface to environment and post-metallization annealing (PMA), can help to reduce the damage introduced into La_2O_3 and its interfaces after the deposition by sputtering of the gate electrode, thus increasing the final reliability of La_2O_3-gated MOS devices. Further improvements on the physical characteristics of La_2O_3 will increase its reliability so that this dielectric material will have good chances to replace conventional gate oxides well beyond the 45 nm node since the fabrication of La_2O_3-gated MOS devices with EOT < 1 nm has been already demonstrated.

Chapter 1

Introduction to metal gate/high-k thin film stacked structures

1.1 Brief summary of the history of semiconductor devices

1.2 Beyond SiO_2-based CMOS device scaling

1.3 Requirements for metal gates and high-k materials

1.4 Review of rare-earth metal oxides

1.5 Observations regarding the development of La2O3 films

1.6 Motivations for using La_2O_3 as high-k material

1.7 Objectives and organization of this study

References

1.1 Brief summary of the history of semiconductor devices

In 1947, W. Schockley, J. Bardeen and W. H. Brattain invented the bipolar transistor [1] at Bell Laboratories, Murray Hill, New Jersey. The invention of the transistor, a solid state amplifier, resulted in great efforts in the field of semiconductor devices. The integration of semiconductor devices on a single chip was one of the consequences of these combined efforts. J. Kilby at Texas Instruments first demonstrated the concept of Integrated Circuits (IC) in 1959 [2]. This concept together with the fabrication of the first Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) by D. Kahng and M. M. Attala in 1960 [3] provided the basis for the evolution of the microelectronics industry. The principle of a surface field effect transistor was already proposed in the early 30's by Lilienfeld and Heil [4]. The experimental verification of the surface field effect, however, could not be demonstrated for more than 30 years. Since then, the MOSFET became by far the most important electronic device for very large scale integrated (VLSI) circuits such as microprocessors and semiconductor memories. The minimum device dimension has been reduced from ~10 μm in the 1960's to sub μm features in the 1990's. Currently, researches are being conducted towards integration of sub 45 nm CMOS devices by several groups all around the world. The introduction of alternative gate dielectrics with a high dielectric constant (ε), or so called *high-k* dielectrics, is a part of these research efforts.

1.2 Beyond SiO_2-based CMOS device scaling

The fundamental building blocks for all the silicon chips — transistors — have continuously kept on track with Moore's Law for over forty years [5]. This law states that the density of transistors (namely MOSFETs) that can be "crammed" into a single integrated circuit is doubled through advances in technology and design every 18 months or quadrupled every 3 years, but as with any rapidly developing field, a limit will eventually

be reached. In the early 1980's the minimum possible dimension was predicted to be approximately 0.5 μm. Ten years later, the predicted minimum dimension had decreased to about 0.1 μm and now, in the early 21st century, a frequently quoted limit is roughly 25 nm. Since its invention, MOSFETs have displaced bipolar transistors to become the most extensively used solid-state devices. MOSFETs have several advantages over bipolar transistors and it is easier to build them in dense arrays. They also typically consume less power than the bipolar integrated circuits do. Because of their simpler fabrication process, higher density, and low power consumption, MOSFETs are widely used in both memory circuits (totally displacing bipolar memories) and in logic circuits. The high-volume production of MOSFET IC has, in turn, financed enormous research programs to improve MOSFET performance; the ongoing research continues to reduce the device size, allowing more devices on a chip, and increasing the operation frequency. Dennard et al. [6] presented an influential systematic study of the impact of technology scaling (process of reducing the sizes of both active devices and passive elements in order to improve both packing density and circuit speed) on circuit performance. They proposed *constant-field* scaling rules, in which dimensions are changed in such a manner that the internal electric fields within the transistor remain (as close as possible) unchanged in the devices. A summary of the constant-field scaling rules is given in table 1.1.

Table 1.1 Scaling rules for constant-field scaling [6].

Physical parameters	Scaling factor
Surface dimensions, L	1/K
Vertical dimensions, tox, Xj	1/K
Impurity concentrations	K
Currents, voltages	1/K
Current density	K
Capacitance (per unit area)	K
Transconductance	1
Circuit delay time	1/K
Power dissipation	$1/K^2$
Power density	1
Power-delay product	$1/K^3$

Scaling rules of the type formulated by Dennard et al. are inherently of limited direct use because effects that can be neglected in larger devices become first significant, and then dominant as device dimensions continues to shrink. With the sub-micrometer dimension channel lengths that now characterize MOSFETs, device performance is completely dominated by high-electric field effects that are inconsequential in larger-dimension devices. So that instead of being strictly observed, the scaling rules have functioned more as a guide to size reduction in integrated circuits. In fact, the scaling of both passive and active devices has been influenced more by fabrication-technology limitations and device functionality than by the application of algebraic scaling factors. Reducing the gate oxide thickness t_{ox}, helps increase the desired coupling of the gate voltage to the channel charge, and every new generation of CMOS technology uses a thinner gate oxide. However, this scaling of oxide thickness is limited. When the oxide thickness becomes extremely thin, direct tunneling (DT) of electrons through it causes significant gate current to flow and reduces input impedance. The acceptable limit for gate oxide scaling appears to be about 2.5 nm without significant increase of the DT leakage current (though Intel™ announced a mere 1.2 nm that corresponds with only five atomic-layer thick for its 90 nm process). In addition to the limitation resulting from DT, the scaling of gate oxide below 2.5 nm cannot effectively increase the gate coupling because of carrier depletion in the poly-silicon gate electrode and the finite thickness of the inversion layer (channel) in the silicon, as illustrated in figure 1.1

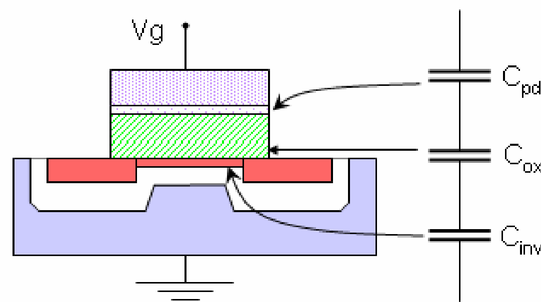


Fig. 1.1 Cross-sectional sketch to show that the MOSFET gate capacitance Cg is made up of three capacitances in series: the oxide capacitance Cox, the capacitance due to the poly-Si depletion effect Cpd and a capacitance due to the finite thickness of the conducting channel Cinv.

The combination of polysilicon depletion and inversion layer capacitance can significantly reduce the MOSFET current drive. The overall capacitance C_{tot} of capacitors in series is dominated by the layer with the lowest capacitance as shown in equation 1.1, so material interfaces must be tightly controlled in order to control gate stack capacitance.

$$Ctot_{series} = \frac{1}{\left(1/C_1 + 1/C_2 + 1/C_3 + \cdots\right)} \tag{1.1}$$

To increase gate coupling, some new approaches are being investigated. High dielectric constant (high permittivity or high-k) gate dielectrics are being actively explored, as well as gates made of metals that can eliminate the gate-depletion effect. Although these new materials and technologies have not yet become a part of production processes, their use will be necessary in future CMOS technology generations. The scaling requirements for future CMOS technologies are generally guided by the International Technology Roadmap for Semiconductors (ITRS) [7], where the introduction of alternative gate dielectrics is predicted for 2007 depending on the technology applications. The advantage for using high-k insulators is obvious. The gate oxide capacitance per unit area is given by:

$$\frac{Cg}{A} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{1.2}$$

Where ε_{ox} and t_{ox} are the relative permittivity and thickness of the oxide respectively. Increasing ε_{ox}, rather than continuing to reduce t_{ox}, avoids the problem of direct tunneling, since tunneling of leakage current through the dielectric layer exponentially increases as its thickness decreases. Nevertheless, making the dielectric ever thinner is necessary in order to meet increasing performance goals. When the gate dielectric of transistors is made thinner, its insulating quality decreases and current leaks through it. Uncontrolled, this conduction causes the transistor to stray from its purely "on" and "off" state and into an "on" and "leaky off" behavior. A schematic showing the problem of DT current flowing through thinner SiO_2 films is shown in figure 1.2. Difficulties encountered in using high-k dielectrics in the past were mainly poor uniformity of the thicknesses of the deposited films and poor quality at its interfaces. However, recent reports have shown that fairly good interfaces can be achieved [8-10].

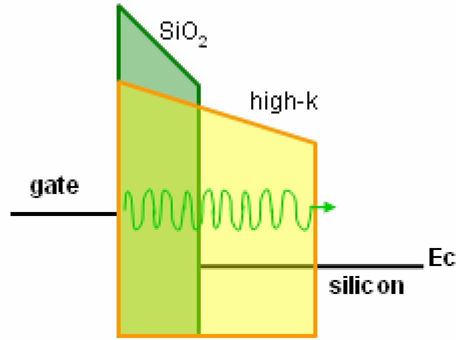


Fig. 1.2 Schematic of direct tunneling through a SiO_2 layer and the more difficult tunneling through a thicker layer of high-k oxide.

1.3 Requirements for metal gates and high-k materials

Along with the use of a high-k material to increase the gate capacitance, metallic or metal-silicide gate electrodes can be used to reduce the effect of polysilicon depletion. This additional capacitor lowers the overall capacitance of the gate stack in accordance with equation 1.1. The thickness of the depletion layer, L_d, varies inversely with the root of the carrier density as shown in equation 1.3:

$$L_d \quad \alpha \quad 1 / (N_{carriers})^2 \qquad (1.3)$$

As shown in equation 1.3, depletion width decreases with increasing dopant concentrations. This relationship is the driving force for very high doping of the polycrystalline silicon (poly-Si) gate electrode. Doping densities for poly-Si gate electrodes already reached their maximum levels. Since metals have intrinsic carrier concentrations much higher than even the most highly doped poly-Si, metal electrodes are a potential replacement for poly-Si. The solid solubility limit of many dopants in Si is about 1 atomic percent. Assuming a metal with about the same atomic density as silicon, that is, the carrier concentration in metal gates is about two orders of magnitude higher than in the poly-Si gates, Equation 1.1 shows that depletion layer widths could be reduced by a factor of 10 (at

the same bias) by replacing poly-Si with a metal (~one carrier/atom). The ITRS calls for a gate stack EOT of only 8Å by 2009, and depletion layer widths of only a few angstroms could easily limit the overall EOT of the gate stack at that time.

Meanwhile, the optimum work function for metal electrodes is believed to be ~4 eV for n-channel and ~5.1 eV for p-channel MOSFETs devices, respectively. These values match the conduction- and valance-band energies of the Si substrate. Hence, achieving proper band alignment for CMOS requires using two different metals, significantly increasing process complexity. A compromise is to use a metal having a work function close to the midgap of silicon for both types of MOSFETs at the cost of having somewhat higher threshold voltages, V_t. Also, because of the possible formation and subsequently grown of low-k IL at the metal/high-k interface after annealing even at low temperatures [11-12], the scaling of metal/high-k structures into sub 1 nm EOT regime is difficult. Therefore, the introduction of inert gate electrodes with suitable work functions for high-k gated MOSFET devices is of the outmost importance. Metals that have been investigated in this thesis include layers of Al, Ta, Ru, Pt and W. Few physical properties for these metals are summarized in table 1.2. In general, metal gate processes are not yet compatible with the conventional poly-Si-gate CMOS processes [13], so replacing poly-Si with metal for the gate electrodes will require extensive process development.

Table 1.2 Physical properties of the metals used in this thesis

Metal	Work function [eV]	Bond enthalpy to oxygen [$kJ\cdot mol^{-1}$]
Aluminum	4.06~4.20	511
Tantalum	4.12~4.25	799
Ruthenium	4.60~4.71	528
Platinum	5.32~5.50	391
Tungsten	4.10~5.20	672

Historically, the requirements for gate dielectrics are based on the unique properties of thermally grown SiO_2. Silicon dioxide has been the prototypical gate

dielectric in view of its amorphous structure, a band gap of ~ 9 eV, band-offsets relative to silicon greater than 1 eV and, most importantly, the insolubility of the oxide (SiO_2) in water. Indeed, the near ideal electrical characteristics of SiO_2 and its compatibility with silicon has been the critical element leading to the superiority of silicon over germanium, especially as the latter oxide was water soluble [14]. For integration of alternative gate dielectrics with a high-k into future CMOS technologies these stringent requirements have to be satisfied. Depending on the application, an EOT of 1 nm or less will be required. The SiO_2-equivalent oxide thickness EOT can be expressed as:

$$EOT = \left(\frac{\varepsilon_{ox}}{\varepsilon_{IL}}\right)t_{IL} + \left(\frac{\varepsilon_{ox}}{\varepsilon_{hk}}\right)t_{hk} \tag{1.4}$$

Where the index *hk* refers to the high-k layer and the index *IL* refers to a possible interfacial layer between the Si substrate and the high-k film. The formation of such IL before, during or after the deposition needs to be minimized to obtain EOT less than 1 nm. Therefore, it is of high interest to deposit the high-k material either on a hydrogen terminated Si surface as obtained after an HF clean or on a “thin” intentionally grown SiO_2 layer. The latter leaves less room for the high-k film to be reduced to a lower-k silicate film during or after its deposition. In general, the requirements for high-k dielectric materials are various and they can be revised thoroughly in an excellent report by J. Robertson [15]. These requirements are:

1. High enough k (k > 10) value to replace SiO_2 in the long term
2. Good thermodynamic stability when in contact with the silicon channel
3. Kinetically stable and compatible with CMOS process
4. Large enough (Ec, Ev > 1 eV) conduction and valence band offsets to silicon
5. Good electrical interface with silicon (low density of D_{it}, defects, etc)
6. Few bulk electrically active defects
7. Electrically, its reliability properties such match or exceed that of SiO_2.

Actually, one of the most challenging problems found in the use of high-k materials in contact with silicon is the formation of two IL at both the upper and bottom interfaces of the high-k. An interfacial layer of SiO_2 often forms between the Si channel and the high-k oxide layer. There are advantages and disadvantages to this IL, as long as its presence and thickness can be controlled. The overall EOT of a layer (*IL*) of SiO_2 and a layer (*hk*) of high-k oxide is given by equation 1.4. Thus, an extra SiO_2 layer is undesirable as it adds up directly to the overall EOT, imposing a severe limitation to scaling. The SiO_2 layer does not arise from the direct reaction of high-k with Si. It arises from the diffusion of O through the high-k layer to oxidize the Si underneath [15-17]. The SiO_2 layer usually grows during the post-deposition annealing stage, and not during the deposition itself. On the other hand, a purposely introduced SiO_2-based IL would improve the overall electrical quality of the Si-oxide interface [15]. In principle, it can be made with a very low defect concentration, by annealing. A SiO_2 layer will also space the Si channel from the high-k oxide, which can lessen carrier mobility due to remote scattering. Nonetheless, a disadvantage of an interfacial oxide is that it may not have the same quality as SiO_2 produced by thermal oxidation of Si [18-19], and it may be defective. Bersuker et al [20] have emphasized that defects in this layer contribute to decrease channel mobilities. Yet, J.A. Ng has demonstrated that by increasing the thickness of a thermally grown oxide IL, the mobilities of n-channel La_2O_3-gated MOSFETs can be improved [21]. Therefore, it is an advantage to be able to control the thickness of the interfacial SiO_2 layer and if necessary, remove it entirely.

1.4 Review of rare-earth metal oxides

"Rare earth elements" and "rare earth metals" are trivial names sometimes applied to a collection of sixteen chemical elements in the periodic table, namely scandium, yttrium, and fourteen of the fifteen lanthanides (excluding promethium), which naturally occur on the Earth. The former two are included as they tend to occur with the latter in the same ore

deposits. Some definitions additionally include the actinides. "Earth" is an obsolete term for oxide. At the time of their discovery, earths of these elements were believed to be scarce in abundance as minerals. However, the term "rare earth" is now deprecated by the International Union of Pure and Applied Chemistry (IUPAC), as these elements are in fact relatively abundant in the Earth's crust; the most abundant, cerium, at 68 parts per million, is the 25th most abundant element in the crust, more common than lead, while even the least abundant "rare" earth element, lutetium, is 200 times more abundant than gold.

The term rare-earth oxide (REO) then comprises a chemical compound containing a rare earth element and oxygen. There are several of these REO seen as potential candidates for the replacement of conventional SiO_2 at the gate of MOSFETs. Yet, a new gate dielectric can be selected in terms of its band gap and relative dielectric constant, since the product of the two can be a figure of merit to compare different dielectrics. Band gap of several candidate oxides for gate dielectric is shown in fig. 1.3, as a function of the relative dielectric constant.

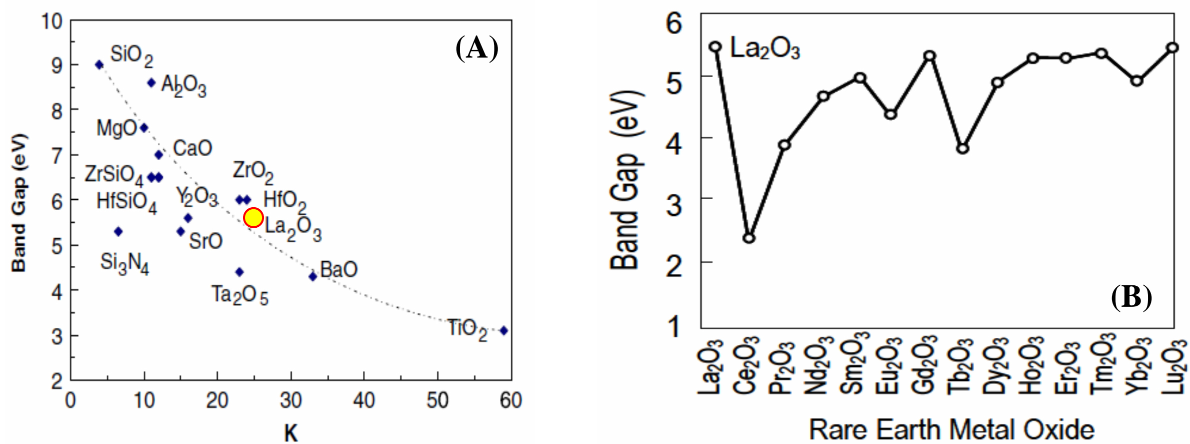


Fig. 1.3 (A) Static dielectric constant versus band gap for candidate gate oxides [22]. (B) Band gap for the REO of the lanthanide series [23-24].

1.5 Observations regarding the development of La_2O_3 films

This section presents some aspects of La_2O_3 thin films processing and characterization in order to assess their development and possible application into future CMOS technologies. Because of the highly intrinsic potential that these high-k films have regarding the replacement of conventional gate oxides, the desired development of La_2O_3-based dielectrics as gate oxides must then be introduced. To do this, the research problems that have been found during the previous developments of La_2O_3 films are summarized and the main results obtained at Iwai laboratory regarding these high-k films are presented. Finally, a brief but precise discussion regarding the significance that a reliability study has on La_2O_3-gated MOS devices will be presented.

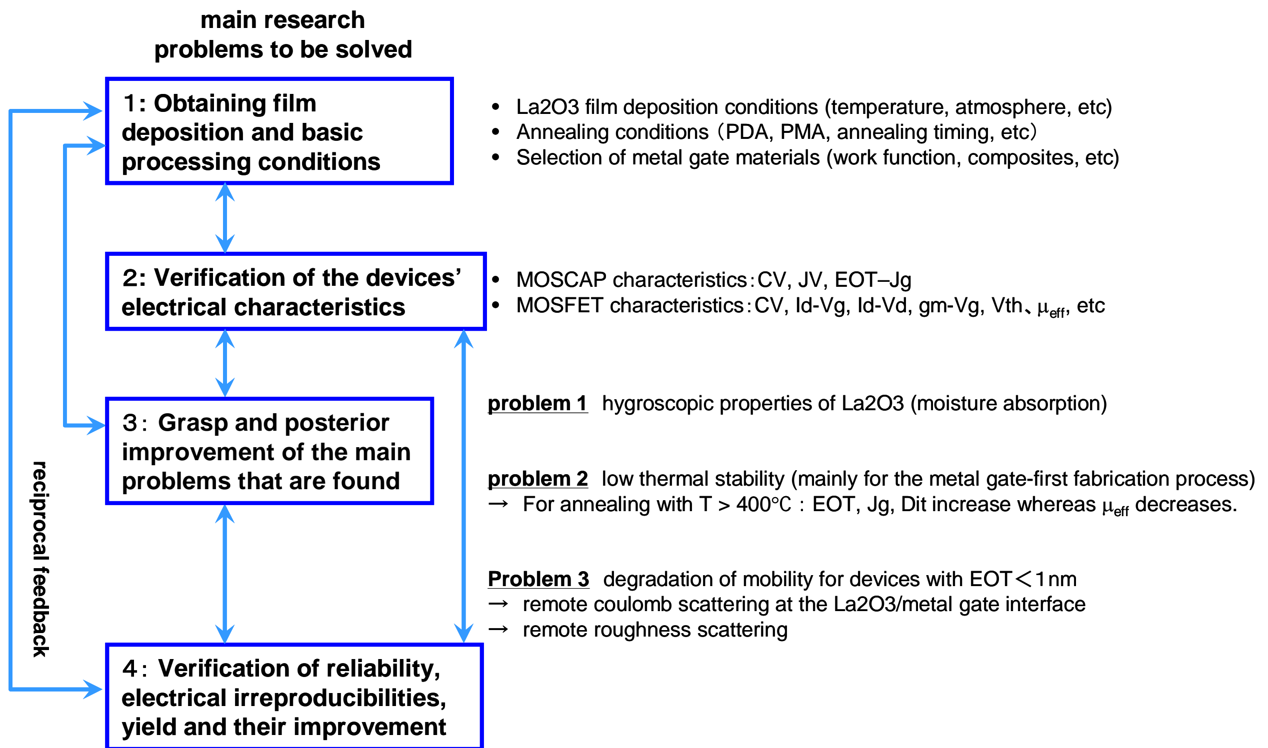


Fig. 1.4 Identification of some of the main problems to be solved for the posterior development of La_2O_3-based high-k materials within Iwai laboratory.

In fig. 1.4, identification of the research of some of the most important issues regarding the development of La_2O_3 thin films is shown. The first topic is the obtention of the basic conditions for the deposition and processing of La_2O_3 thin films, where several processing-related steps are involved. This is followed by the fabrication of MOS devices (whether capacitor or transistor structures) and the consequent verification of the correspondent devices' electrical characteristics in order to test the electrical nature and quality of the deposited La_2O_3 thin films. Since these first two topics are closely related to each-other (better electrical characteristics of devices will be obtained by improving the deposition and processing conditions of the La_2O_3 thin films), the immediate identification of the main problems related to the dielectric qualities of La_2O_3 must then be identified and some solutions must be implemented as shown in the figure. So far, some of the most important problems to be solved have been identified: 1) highly hygroscopic properties of La_2O_3 thin films, in which moisture absorption on the surface of the dielectric changes its physical, chemical and electronic properties leading to highly degraded MOS devices' characteristics, 2) low thermal stability problem, which is related to the change in the chemical and electronic structure of the whole La_2O_3 film after relatively high temperature annealing conditions (whether during the deposition of the film itself, or during PDA or PMA conditions), 3) very low carrier mobility for ultra-thin EOT (< 1 nm) La_2O_3 films, since thinner films increase the density of leakage current and therefore, the probability of trapping at the bulk and interfaces of La_2O_3 with silicon and other immediate interfaces.

In order to get a clearer vision of the high potential La_2O_3 thin films for the replacement of conventional SiO_2-based films, what follows is a very short compendium of some of its main results obtained at Iwai Laboratory. To begin with, fig. 1.5 shows a Jg-EOT plot for several high-dielectric constant materials compared to La_2O_3 results obtained at Iwai Lab. It is clearly seen that even for the smaller EOT levels (below 1 nm), the leakage current density flowing through La_2O_3-gated MOS devices is the smallest of all the compared materials. This poses a great advantage for the introduction of La_2O_3 as the gate oxide of very short channel length transistors, were the use of ultra-thin oxide films is

projected and therefore the appearance of excessive leakage currents (even when the transistor's gate is turned off) had been the major limitation towards transistor miniaturization.

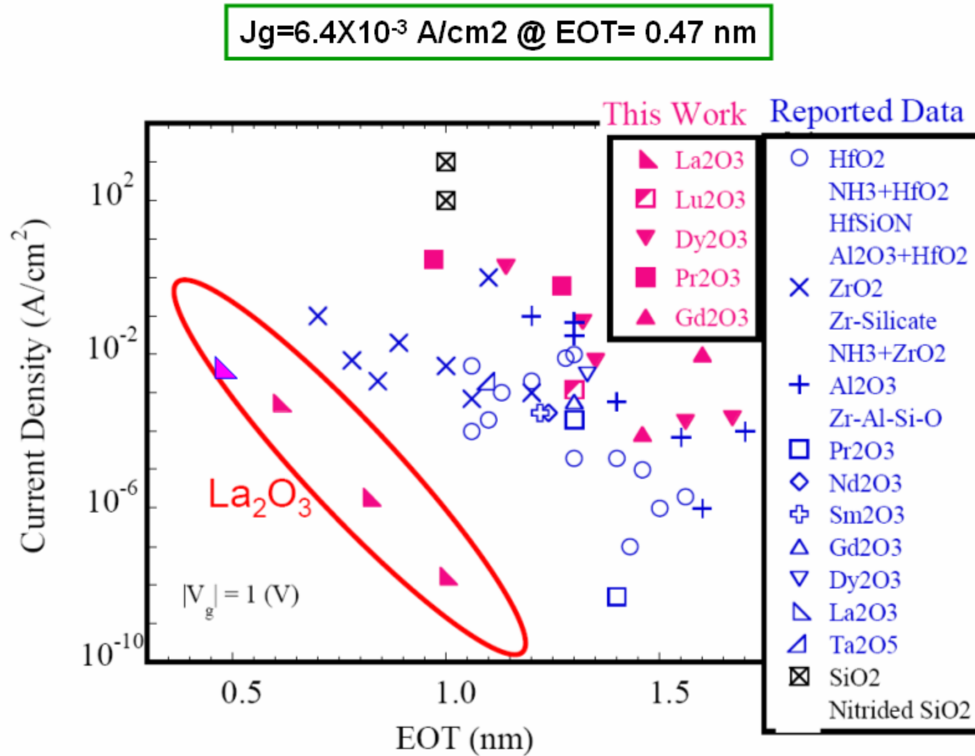


Fig. 1.5 Gate leakage current density versus EOT at Vg= 1 V for high-k materials. Several other high-k dielectric materials are compared to La_2O_3 results obtained at Iwai Lab.

Fig. 1.6 shows how La_2O_3-gated MOSFET devices very high electron mobility (high-k based) can be obtained. A very high electron mobility of μ_{eff}= 312 cm^2/Vs has been obtained along with a very low interface-state density Dit= $6x10^{10}$ cm^2/eV. Nevertheless, the relatively large EOT= 1.7 nm level obtained for this specific sample makes necessary to improve the deposition and post-deposition processing of La_2O_3 on silicon so that better electrical characteristics can be obtained. Another advantage of La_2O_3 over the very popular Hf-based high-k material is that La_2O_3 does not exhibit the Fermi-level pinning as observed for Hf-based devices, see fig. 1.7.

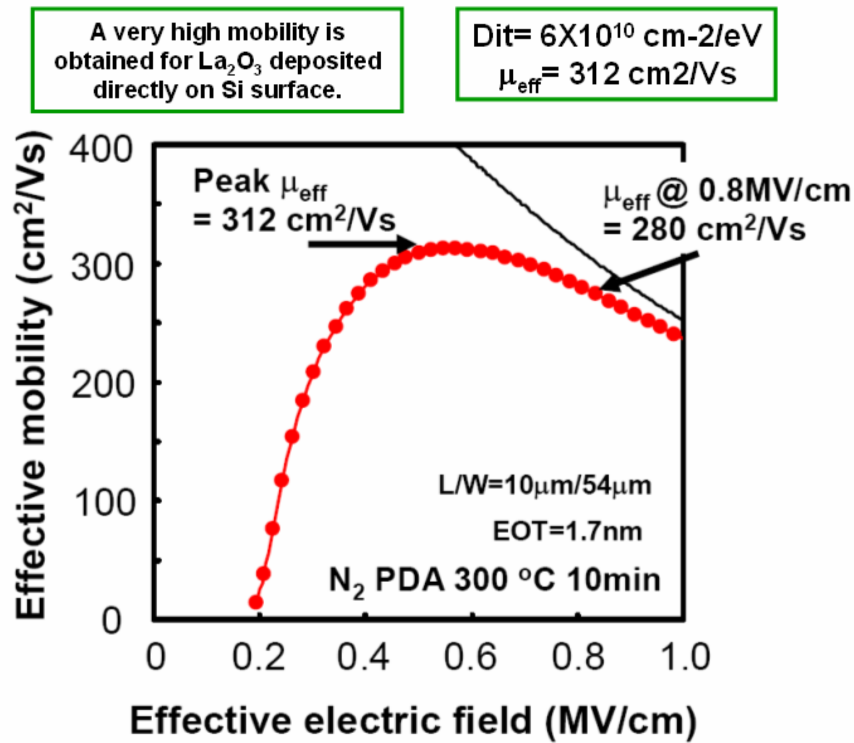


Fig. 1.6 Effective mobility versus effective electric field for La_2O_3-gated n-channel MOSFET. Very high electron mobility along with very low interface-states density Dit was obtained.

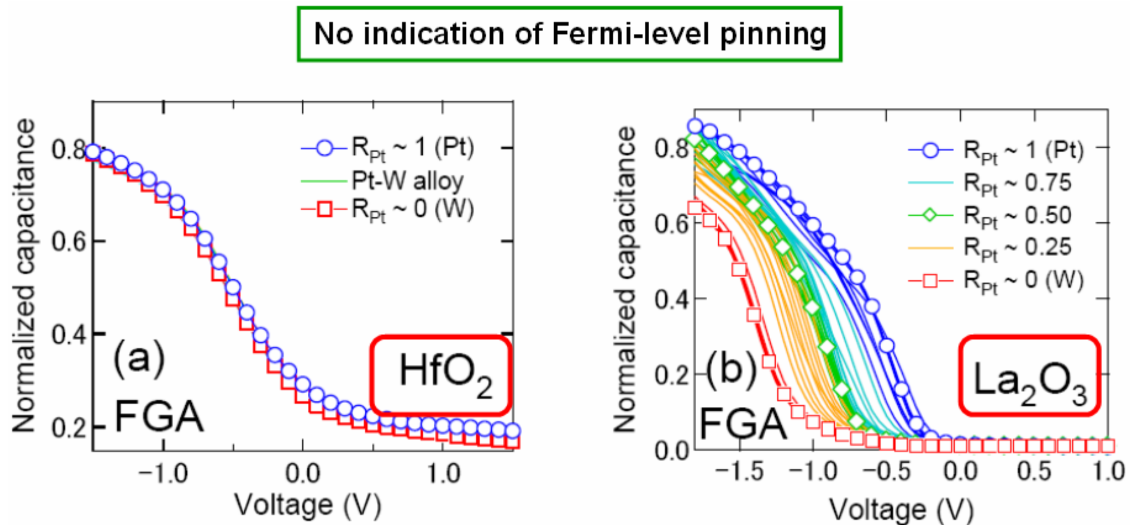


Fig. 1.7 Normalized capacitance versus gate voltage for HfO_2 and La_2O_3-gated MOS devices on silicon. Fermi level pinning is observed only for the HfO_2-based MOS device samples.

From fig. 1.7, it can be seen that by using La_2O_3 as the gate oxide, a wide controllability of the flat-band voltage Vfb can be obtained when using different compositions of the Pt-W metal electrode's system. On the other hand, HfO_2-based oxides present a "pinning" of Vfb which results in a very poor control over the threshold voltage Vth of MOSFET devices when using the same low and high metal work functions.

All these advantages of La_2O_3 over other high-k materials, along with the continuous improvement in the electrical characteristics of the MOS devices that are being fabricated (by modifying deposition and post-deposition processing conditions for La_2O_3) have resulted in the identification and most importantly, minimization of the intrinsic problems presented by these films. When all of the former approaches are put together, the research on La_2O_3-gated MOS devices must therefore advance to the next stage of electrical characterization, which is the reliability study of the fabricated devices; see level 4 of the diagram depicted in fig 1.4. A brief summary of the main problems that have been identified for La_2O_3-gated devices along with potential solutions are presented next:

Present problems for La_2O_3-based MOS devices and their respective solutions

Problem 1: Highly hygroscopic properties of La_2O_3 (moisture absorption)

Solutions:
a) In-situ deposition of both La_2O_3 and metal gate electrodes.
b) Mix La_2O_3 with other high-k materials (La_2O_3 and HfO_2, Sc_2O_3, etc)

Problem 2: Low thermal stability (TS) when using gate-first processing

Solutions:
a) Use stacked-layer structures with higher TS high-k materials (HfO_2, Sc_2O_3, Y_2O_3, etc)
b) Use alloys (La_2O_3-HfO_2, La_2O_3-Sc_2O_3, La_2O_3-Y_2O_3, etc)
c) Implement gate-last processing (reducing the final thermal budget)

Problem 3: Mobility reduction for La_2O_3-gated devices with EOT < 1nm

Solutions: a) Use appropriate deposition and annealing conditions for La_2O_3

b) Improve the quality of the La_2O_3 interface with silicon (under study)

As it can be seen, the present status of La_2O_3 still presents some serious issues before its implementation as the gate oxide for next-generation transistors. However, and because of the good results having obtained so far, La_2O_3 is being considered as a possible candidate not only for the replacement of SiO_2 but also for HfO_2-based materials since Hf-based high-k materials are surpassed by La_2O_3 in terms of ultra-low leakage current density levels for the smallest EOT ever obtained. A brief summary of the reasons behind the significance of La_2O_3-related reliability studies will be shown below.

What is the significance of La_2O_3-related reliability studies?

1. Since the Fermi-level pinning phenomenon is not present for La_2O_3-gated MOS devices, and because of the high quality of the interface between La_2O_3 and silicon substrate, the high dielectric constant of La_2O_3, the high energy band offsets for La_2O_3, etc., the expectation for the introduction of La_2O_3 for devices in the EOT < 1 nm region is growing.

2. Even though La_2O_3 still presents some problems related to its high hygroscopic properties (moisture absorption), low thermal stability, etc., the solutions to some degree of all these problems are foresighted.

3. When La_2O_3 is considered as a gate dielectric material for devices with EOT < 1nm, the importance of the role and potential that these films can be achieved has become bigger, and for that reason, it is quite important to grasp the best structure and process, that is,

using La_2O_3 as the gate oxide for gate-last or gate-first processing, single-layer La_2O_3, compositional mixtures of La_2O_3 with HfO_2, Sc_2O_3, etc., or stacked structures of La_2O_3 with Sc_2O_3, etc., the latter depending on the value of the EOT.

4. The study of the reliability evaluation for La_2O_3 films is still an undeveloped field, therefore, this study must first verify the reliability of La_2O_3 itself, must make clear what is the real nature of its dielectric degradation phenomena, and must also identify what are the main problems that need to be solved.

5. The use of La_2O_3 thin films for the EOT < 1 nm regime is the ultimate goal but since the processing for these ultra thin films is still going under continuous improvements, the present reliability study was mainly applied for films with EOT ~ 1.5 nm. In addition, the current study was focused on the use of La_2O_3 with the gate-last fabrication process, so that the highest annealing temperature during the post-deposition of the La_2O_3 films was limited to 500°C.

6. At this stage, since the fabrication of La_2O_3-gated MOS transistors with ultra-short channel length cannot be realized in this laboratory, we excluded the reliability studies of hot-carrier instabilities (HCI) for these films.

1.6 Motivations for using La_2O_3 as high-k material

La_2O_3 has the largest band gap of the rare earth oxides at Eg > 5 eV, while also having the lowest lattice energy, with very high dielectric constant, ε = 27 pF/m [25-26]. The use of La_2O_3-gated MOSFET devices will significantly reduce leakage-current density because of the larger band offset for electrons as compared to HfO_2, see fig. 1.4.

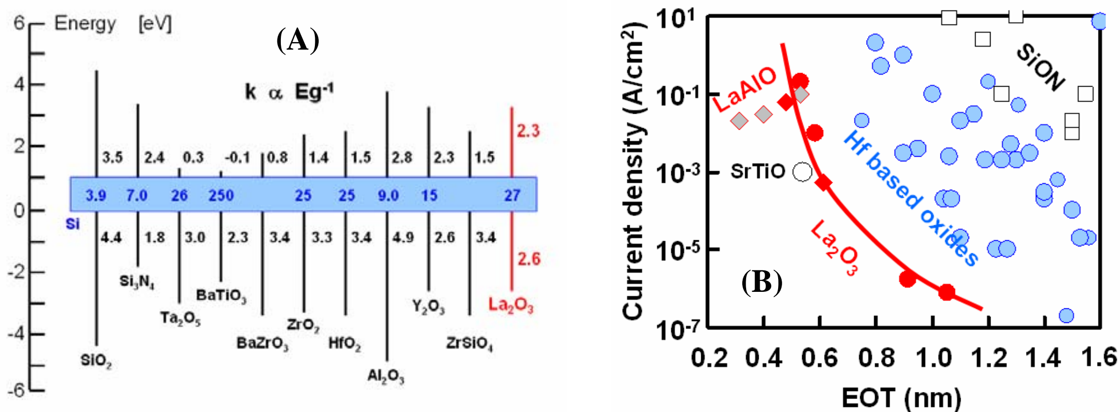


Fig. 1.8 (A) Band offsets of several high-k candidates with silicon. Band offsets for La_2O_3 are shown in red. (B) Gate leakage current density of La_2O_3-based oxides compared to Hf-based oxides [27-31].

From figure 1.4(B) it is clearly seen that La_2O_3 poses the great advantage of reduced leakage current for the same EOT when compared to other high-k materials [27-31], specifically, the Hf-based oxides family. Even for EOT below 1 nm, La_2O_3 still conserves this advantage. It is important to note that, even with good initial electrical characteristics (good J_g-EOT relationship, high electron mobility μ_n, reduced threshold voltage V_{th}, long lifetimes before breakdown, etc), after some period of time or applied stress, these good electrical characteristics might be degraded and the whole operation of the devices or circuits containing this high-k material might be compromised. In this respect, the highly reactive nature of La_2O_3 to water and CO_2 from air might pose a serious disadvantage for using such material without any protection under long periods of time

since once it is exposed to air, the hydration reaction will degrade its physical properties, thus creating defects or inducing stress concentrations of the film, even lowering its dielectric constant. A good deal of information about the chemical reactivity and stability of rare-earth and particularly La_2O_3 materials can be found in [32].

Because of the reduced densities of leakage current that can be obtained for relatively low EOT, La_2O_3 is considered a very promising candidate for the replacement of SiO_2 in future generations of CMOS devices. However, the high chemical reactivity and instabilities presented in La_2O_3 after its deposition on silicon, prevents the initially good electrical characteristics of La_2O_3-gated devices to hold with time or applied stress. Therefore, the characterization of the degradation and breakdown of La_2O_3-gated devices must be evaluated since the reliability data resulted from there will provide a consistent path towards the realistic consideration of this high-k material as a serious replacement for still SiO_2-based MOSFETs.

Finally, by limiting the reliability characterization of La_2O_3-gated MOS devices (capacitors and transistors) by excluding those samples with the higher densities of leakage current and taking only the devices with the most closely similar electrical characteristics (similar gate leakage current levels, flat-band and threshold voltages Vfb-Vth, etc), the problem of electrical irreproducibilities can be minimized and therefore, the reproducibility of the reliability data is improved. This is quite important since the degradation and breakdown of La_2O_3-gated devices must be extrapolated to very long lifetimes over 10 years and therefore, a minimized dispersion of the data must be achieved. This is also obtained by increasing the number of the stressed samples and the timing of the stressing measurements. Lately, improvements of the La_2O_3 deposition and post-deposition processing has resulted in better and more reproducible electrical characteristics of the fabricated devices so that still better reliability projections from these films can be obtained.

1.7 Objectives and organization of this study

Electrical reliability is considered to be a big challenge for La_2O_3 gate stacks. Until recently, very little was known about the reliability or long-term ability of La_2O_3-gated MOS devices to perform and maintain their functions in normal operation (low voltages and currents) conditions, as well as in high-field stressing conditions (which will be normally found in scaled down devices). In this respect, the most influential parameter than can modify the electrical behavior of La_2O_3-gated MOSFETs is the injection of carriers whether at low or high gate voltages. Under low voltage conditions, the increase in the density of gate leakage current will degrade the electrical performance of the devices whereas at high voltage conditions the injection of hot electrons and the continuous degradation of La_2O_3 will ultimately lead towards its total destruction or electrical breakdown. Because devices are often designed to operate reliably under normal operation conditions for at least 10 years, it is impractical to wait for this long period of time to verify the reliability of La_2O_3-gated devices. Instead, we need to find ways to accelerate the stress test so that we can obtain the time-to-failure t_f in a reasonable time. One technique is to carry out the stress at higher biases than are normally used during system operation; typically the gate voltage V_g is increased to accelerate the life test. In this study we used relatively high gate voltage stressing conditions to induce La_2O_3 degradation and breakdown in order to asses its lifetime and therefore extrapolate these results in order to obtain degradation and lifetime projections at normal operation conditions.

The objective of this study is to investigate the reliability characteristics of La_2O_3-gated MOS devices, and to identify what are the main issues and what are the differences from conventional SiO_2-based gate stacks. Besides, since a metal–La_2O_3–silicon stacked structure usually contains interfacial layers at both the bottom and top of the dielectric, the reliability characterization for this stacked structure must take into account this phenomenon. Especially, efforts should be made to enhance the reliability properties of La_2O_3-gated MOS devices by decreasing V_{th} shifts after stress and increasing

the lifetime before breakdown t_{bd} of this dielectric. From the current results, the initial understanding on the physical mechanisms that lead to these degradations and the ways to prevent or at least minimize them should be provided.

With this objective, the approach was to focus on the improvement in the quality of the metal–La_2O_3 stack by modifying the deposition process and after-deposition process of the stack, that is, by adequate thermal treatments and less exposure to environment contaminants so that an improvement in the reliability characteristics for La_2O_3 can be obtained. Additionally, the certainty of the reliability projections was improved by stressing a relatively high number of samples in which the reproducibility of their fresh electrical characteristics was ensured. Since the data collection would be meaningless without comparing to other high-k materials, the results were compared with the results available in the literature in order to find a more direct path towards ensuring better reliability properties for the metal–La_2O_3 stacked structures.

This dissertation consists of seven chapters which are described schematically in fig. 1.9. Following this chapter, chapter 2 describes the fabrication and characterization methods used throughout this study. Detailed fabrication flows of MOS capacitors and MOS transistors as well the basic principles of all the equipment used for the fabrication were briefly discussed. The measurement setups and characterization methods used in this study were also mentioned, taking especial emphasis on the reliability characterization techniques that were applied to the fabricated samples.

Chapter 3 presents and discusses the results obtained from reliability characterization of metal-La_2O_3 MOS capacitor (MOSCAP) devices under low and high-voltage stressing conditions. It is important to notice that by stressing La_2O_3 with an applied constant voltage, the immediate or retarded breakdown of the dielectric will produce different effects on the final electrical characteristics of the stressed devices. First, the dielectric was electrically stressed with low-electric fields so that hard-breakdown

(HBD) could be avoided during the stress and the degradation in the devices' parameters (shifts in V_{fb}, SILC, etc.) could be measured. Secondly, the dielectric films were stressed with higher-electric fields in order to force La_2O_3 to HBD condition and thus, obtain the lifetime of La_2O_3-gated MOSCAP. All these results of degradation and breakdown for this dielectric are presented.

Chapter 4 presents and discusses the effects of electrical stress for La_2O_3-gated MOSFET devices in which the dielectric was also conditioned to avoid/reach the condition of HBD. Since the MOSFET structure can give us a more detailed description of the degradation phenomena occurring during the stress, most of the results in this chapter belong to low-stressing conditions in which HBD was avoided. Additionally, in MOS transistors, it is possible to monitor not only the gate current I_g but also the substrate current I_{bulk} simultaneously. This is a well-known technique usually referred to as carrier separation that allows identifying the dominant carrier type on the gate leakage current. These measurements and the discussion of the results are presented here. Since the degradation of La_2O_3 under carrier injection conditions involves both interfaces of the oxide with the metal and principally, the silicon substrate, measurements of interface-state density D_{it} after stress were also performed and the correlation between D_{it} and the degradation of the threshold voltages of nMOSFET and pMOSFET devices was discussed.

In chapter 5, the previous results from the reliability characterization of La_2O_3-gated MOS capacitors and transistors are taken in order to develop a more concise model explaining the mechanisms behind the degradation and breakdown of the La_2O_3-IL stacked layers on silicon. It will be shown that there are many similarities as well as differences regarding the degradation of these high-k layers when compared to SiO_2. Lastly, brief proposal on methods to improve reliability was presented so that a better projection of the degradation and lifetime of La_2O_3 after stress can be obtained.

Chapter 6 presents a summary of the most important reliability results obtained for

Hf-based high dielectric constant materials along with a comparison of the reliability properties of these Hf-based oxides with those of the present La_2O_3-gated MOS devices.

Finally, chapter 7 summarizes and concludes the findings and contributions of this study and suggests recommendations for future work.

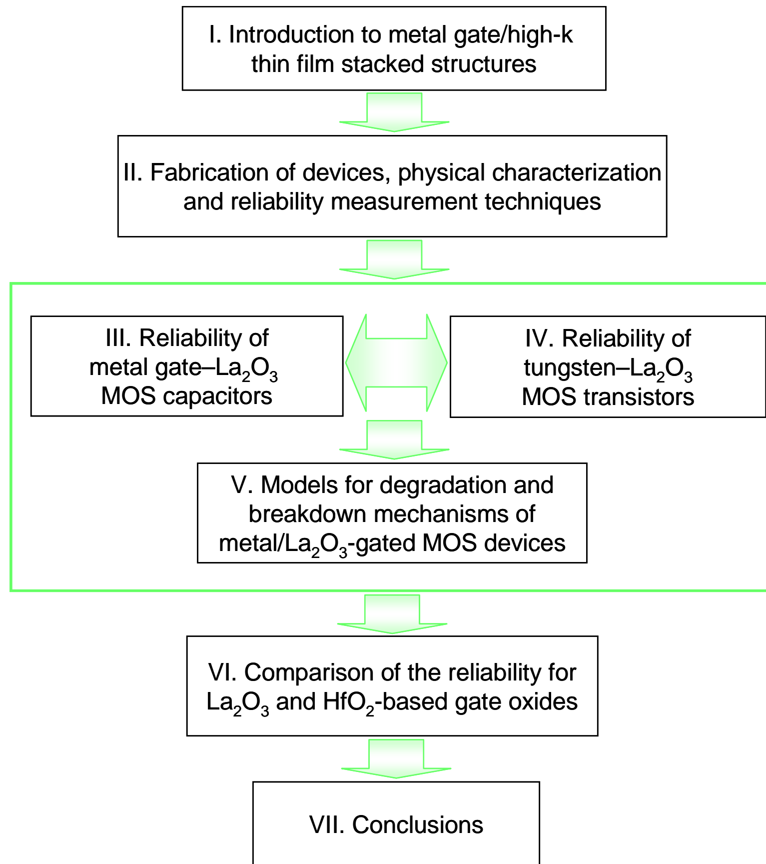


Fig. 1.9 Outline and organization of this dissertation.

References

[1] W. Shockley, "The path to the conception of the junction transistor," IEEE Trans. Electron Devices, vol. ED-23, no. 7, pp. 597-62O, July1976.
J. Bardeen, "Three-electrode circuit element utilizing semiconductive materials," U.S. Patent 2 524033. Application filed Feb. 26,1948, granted Oct. 3,1950.
J. Bardeen and W. H. Brattain, "Three-electrode circuit element utilizing semiconductive materials," U.S. Patent 2 524 035. Application filed June 17, 1948, granted Oct. 3, 1950.

[2] Jack S. Kilby, "Invention of the integrated circuit," IEEE Trans. Electron Devices, vol. ED-23, no. 7, pp. 648-654, July 1976.

[3] D. Kahng and M. M. Atalla, "Silicon-silicon dioxide field induced surface devices," presented at the IRE-AIEE Solid- State Device Research Conference at Carnegie Institute of Technology, Pittsburgh, PA, 1960.

[4] I. E. Lilienfeld, "Method and apparatus for controlling electric currents," U.S. Patent 1 745 175. Application filed Oct. 8,1926, granted Jan. 18, 1930.
0. Hei1,"lmprovements in or relatingtoelectricalamplifiers and other control arrangements and devices," British Patent 439 457, application filed Mar. 4, 1935, granted Dec. 6, 1935.

[5] G. Moore, "Cramming more components onto integrated circuits", Electronics, 38(8), pp.114-117 (1965).

[6] R.H. Dennard, F.H. Gaensslen, H.N. Yu, V.L. Rideout, E. Bassous and A.R. LeBlanc, IEEE J. Solid-State Circuits, SC-9, 256 (1974).

[7] International Technology Roadmap for Semiconductors (ITRS). *Semiconductor Industry Association*. 181 Metro Drive, Suite 450, San Jose, CA, 95510, http://public.itrs.net, 2006 updated edition

[8] Suzuki, M. Tomita, M. Yamaguchi, T., and Fukushima, N., "Ultra thin (EOT=3A) and Low Leakage Dielectrics of La-Alminate Directly on Si Substrate Fabricated by High Temperature Deposition", *Tech. Dig.,. IEEE IEDM*, pp. 433-436, 2005.

[9] Inumiya, S.; Akasaka, Y.; Matsuki, T.; Ootsuka, F.; Torii, K.; Nara, Y., "A thermally-stable sub-0.9nm EOT TaSix/HfSiON gate stack with high electron mobility, suitable for gate-first fabrication of hp45 LOP devices", *Tech. Dig.,. IEEE IEDM*, pp. 23-26, 2005.

[10] D.J. Lichtenwalner, J.S. Jur, A.I. Kingon, P.A. Melody, Y. Yang, S. Stemmer, L.V. Goncharova, T. Gustafsson and E. Garfunkel, "Lanthanum silicate gate dielectric stacks with subnanometer equivalent oxide thickness utilizing an interfacial silica consumption reaction", *J. Appl. Phys*. **98**, 024314 (2005).

[11] J.A. Ng, Y. Kuroki, N. Sugii, K. Kakushima, S. Ohmi, K. Tsutsui, T. Hattori, H. Iwai and H. Wong, "Effects of low temperature annealing on the ultrathin La_2O_3 gate dielectric; comparison of post deposition annealing and post metallization annealing", *Microelec. Eng*., **80** 206 (2005).

[12] Y. Kuroki, J. Ng, K. Kakushima, N. Sugii, K. Tsutsui and H. Iwai, "Al/ La_2O_3 Analysis of Post Metallization Annealed MISFET by XPS", *ECS Trans*. **1** (5) 239 (2006).

[13] A. Chatterjee, Chapman, R, Dixit G., Kuehne J, Hattangady, S et al., "Sub-100 nm gate length metal gate NMOS transistors fabricated by a replacement gate process", *Tech. Dig., IEEE IEDM,* pp. 821-824, 1997.

[14] H.R. Huff and John Bardeen, *Transistor Physics, Characterization and Metrology for ULSI Technology*, 2000 International Conference), 3-29 (2001), AIP Press.

[15] J. Robertson, "High dielectric constant gate oxides for metal oxide Si transistors", *Rep. Prog. Phys., Inst. Phys. Pub*. **69** 327 (2006).

[16] M.H. Hakala, A.S. Foster, J.L Gavartin, P. Havu, M.J. Puska and R.M. Nieminen, "Interfacial oxide growth at silicon/high-k oxide interfaces", *J. Appl. Phys*., **100** 43708 (2006).

[17] L. Marsella and Vincenzo Fiorentini, "Structure and stability of rare-earth and transistion-metal oxides", *Phys. Rev. B*., **69** 172103 (2004).

[18] M. Copel and M.C. Reuter, *Appl. Phys. Lett*. **83** 3398 (2003).

[19] G.D. Wilk and D.A. Muller , *Appl. Phys. Lett*. **83** 3984 (2003).

[20] Bersuker G et al., *Jap. J Appl. Phys*. **43** 7899 (2004).

[21] J.A. Ng, "A Study on Mobility of MOSFETs with La_2O_3 Gate Dielectric", Doctoral Thesis, Tokyo Institute of Technology (2006).

[22] Robertson J, *J. Vac. Sci. Technol. B* **18** 1785 (2000).

[23] G. Adachi, *Science of rare earths*, Kagakudojin Co., 1999, p.291.

[24] A. Prokofiev, A. Sheykh, and B. Melekh, “Periodicity in the band gap variation of Ln2X3 (X=O,S,Se) in the lanthanide series”, *J. Alloys and Compounds*, **242** 41 (1996).

[25] Bedoya, C. “MOCVD of Lanthanum Oxides: A Thermal and Kinetic Investigation.” *Chemical Vapor Deposition*. **12** 46 (2006).

[26] T. Hattori et al., *Microelec. Eng*. **72** 283 (2004).

[27] IEEE Elect. Dev. Letters vol. 21, no. 7, p. 341 (2000)

[28] IEDM ’02, p. 625. H. Iwai

[29] IEDM ’02, p.955. S. J. Lee

[30] J. of the Electrochem. Soc., 150 (8) G429 (2003).

[31] VLSI Tech ’05, p. 168. C. Choi.

[32] G. Adachi, N. Imanaka and Z.C Kang (Eds), *Binary Rare Earth Oxides*, Kluwer Academic Publishers., pp. 9 (2004).

Chapter 2

Fabrication of devices, physical characterization and reliability measurement techniques

2.1 Introduction

2.2 MOS capacitor and MOSFET fabrication

2.3 Fabrication process

2.4 La_2O_3 deposition in O_2 ambient with in-situ metallization

2.5 Physical characterization

2.6 Electrical characterization

2.7 Reliability measurement techniques

References

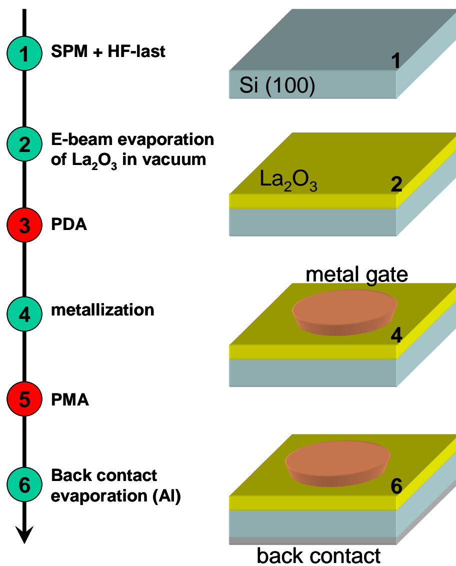
2.1 Introduction

This chapter is devoted to the discussion of the fabrication steps of La_2O_3-gated metal-oxide-semiconductor (MOS) capacitors and MOS field-effect transistors (MOSFET's) that were used in this study. The standard as well as modified deposition process of La_2O_3 on silicon is introduced and their post-deposition processes, thermal treatments before and after metallization, are explained as well. The physical and electrical characterization of the fabricated devices will be briefly presented giving especial emphasis on the techniques used for reliability characterization.

2.2 MOS capacitor and MOSFET fabrication

Figure 2-1 (A-B) schematically shows the fabrication steps for MOS capacitor (MOSCAP) structures after two different processing sequences. N- or P-type silicon (Si) substrates with (100) orientation were used as the semiconductor material.

(A) Standard deposition of La_2O_3



(B) Standard and modified deposition of La_2O_3 using SiO_2-based spacers

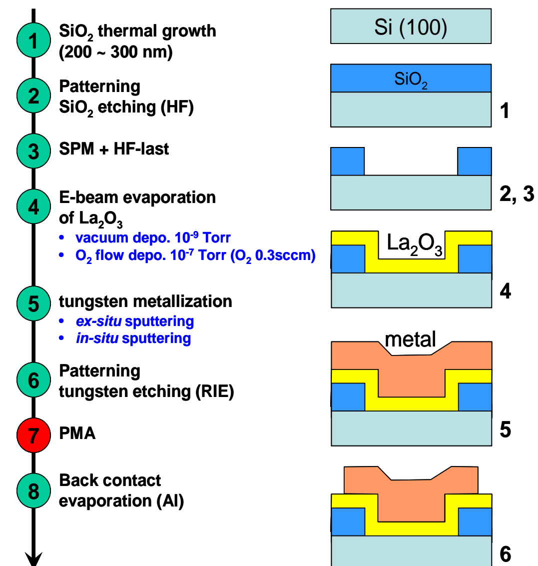


Fig. 2.1 (A) Standard deposition of La_2O_3 for the fabrication of MOS capacitors.
(B) Use of SiO_2-based spacers for the standard and modified deposition of La_2O_3.

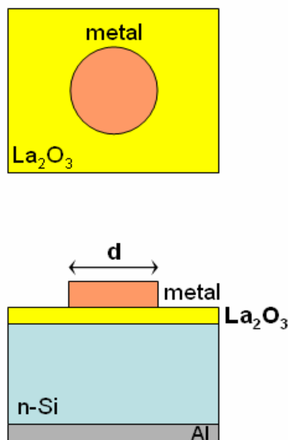
From figure 2.1 (A), the standard deposition of La_2O_3 on silicon initiates with the chemical cleaning of the silicon surface with Sulfuric acid Hydrogen Peroxide Mixture (SPM), which is a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) in ratio of 4:1. This mixture is used to chemically oxidize the Si surface. After that, the induced SiO_2 is removed by dipping it into 1 % hydrofluoric acid (HF), thus providing passivation for the Si dangling bonds with hydrogen (HF-last surface). La_2O_3 is then deposited on Si

surface at 300°C by E-beam evaporation within an ultra-high vacuum (UHV) chamber using molecular beam epitaxy (MBE) system. The chamber pressure during deposition was between 10^{-7} to 10^{-5} Pa. After removing the La_2O_3-Si substrates from the UHV chamber, ex-situ low temperature post deposition annealing (PDA) inside infrared lamp based rapid thermal annealing (RTA) was carried out. This step is done before the metal gate formation. If the low temperature heat treatment is performed after metal gate formation, it is known as post metallization annealing (PMA). The gate metallization is usually done by thermal evaporation of aluminum or RF magnetron sputtering of different metal materials. The deposition of the metal on La_2O_3 is done through a shadow mask with circular patterns of different areas which define the gate of the capacitors. For some samples, ex-situ low temperature PMA is then carried out inside RTA apparatus and finally, backside aluminum (Al) metallization is done by using bell-jar type thermal evaporator. This completes the fabrication process of MOSCAP structures.

In figure 2.1 (B), the introduction of SiO_2-based spacers (with thickness 200–300 nm) for a modified capacitor structure were used in order to minimize La_2O_3 exposition to environment's moisture through the lateral regions of the gate area. For some samples, the standard deposition of La_2O_3 on Si surface was then realized as described above. Also, a modified deposition of La_2O_3 was realized in which a continuous flow of oxygen (O_2) was introduced in order to minimize oxygen losses during the film deposition. Therefore, in an effort to minimize the formation of oxygen vacancies and to stabilize the reactivity of the metal–oxide, the deposition of La_2O_3 under process (B) can be thought as being done under PDA in O_2 ambient, so that La_2O_3 is oxidized during the deposition itself, creating a silicate layer. Although detrimental to the permittivity, the resulting structure should be more stable and less apt to contain oxygen deficiencies [1]. The deposition temperature for both processes was done at 300 °C. The metallization step in figure 2.1 (B) also played an important role in determining the final electrical characteristics of the fabricated devices. Here, tungsten was primarily used as the gate electrode and it was deposited directly on the La_2O_3 surface without shadow masks. An ex-situ deposition of tungsten means that this

material was deposited within a dedicated sputtering chamber (outside the UHV chamber) so that the vacuum obtained during the dielectric deposition was broken and La_2O_3 was briefly exposed to environment's moisture. Ex-situ tungsten deposition was done within 30 min after the deposition of La_2O_3 to reduce moisture adsorption and any other possible contamination on these films at minimum. For other samples, an in-situ deposition of tungsten was realized in a contiguous chamber (within the same MBE system) immediately after the dielectric deposition thus avoiding the breakdown of the UHV and reducing the exposure of La_2O_3 surface to the environment. Because of this, the physical thickness of La_2O_3 cannot be measured by conventional methods like ellipsometry but by transmission electron microscopy or any other imaging technique. During the in-situ deposition of the metal, an argon flow of 7 sccm at the pressure of 1.33 Pa with 150 W RF power was used and the patterning of the gate electrodes was done by reactive-ion etching (RIE) using SF_6 chemistry at 30 W power together with standard photolithography processing. Only PMA were applied and the back-side metallization by thermal evaporation of Al concludes the processing flow for these samples. Top and cross-sectional views of the fabricated devices after both processing flows (A) and (B) are shown in figure 2.2 (A-B).

(A) Standard deposition of La_2O_3 on silicon



(B) Modified deposition of La_2O_3 on silicon

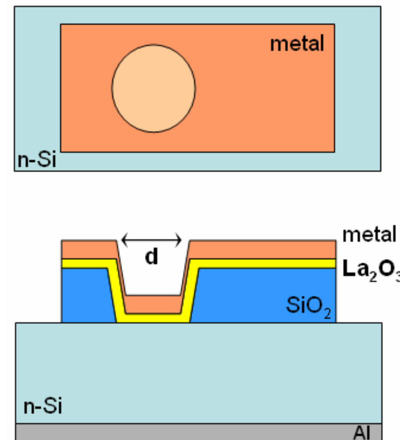


Fig. 2.2 (A) Top and cross-sectional views of MOS capacitors after standard deposition of La_2O_3.
(B) Top and cross-sectional views of MOS capacitors after deposition of La_2O_3 using SiO2-based spacers in order to reduce exposure to moisture through lateral regions of gate area.

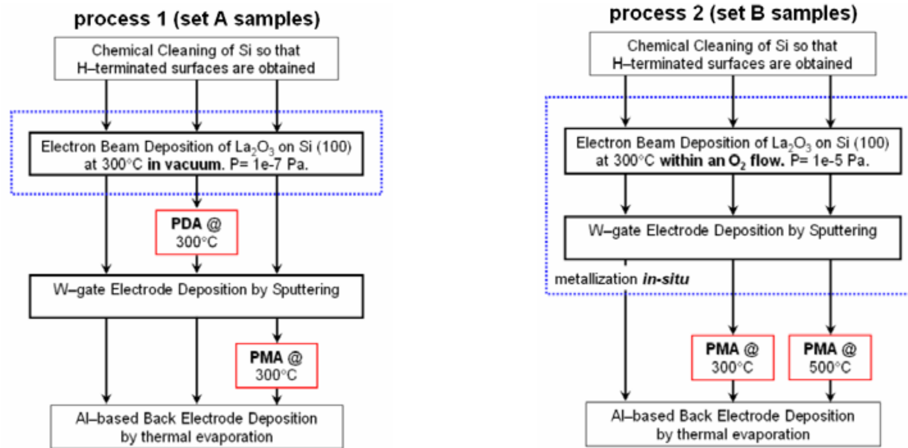
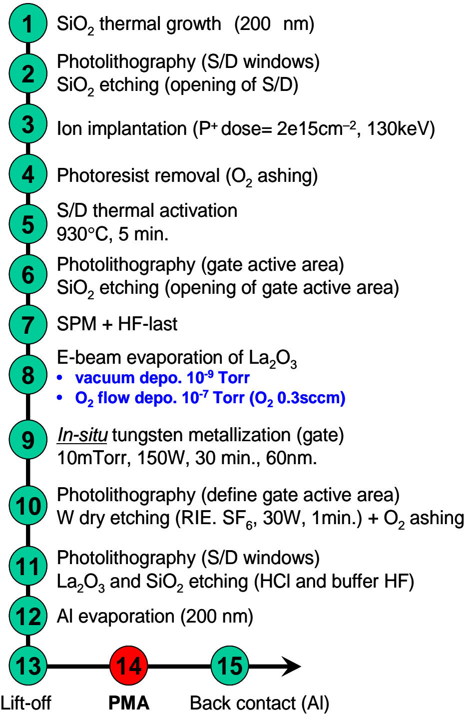
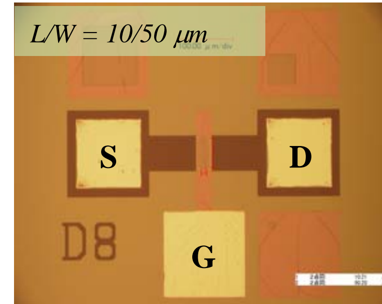


Fig. 2.3 (A) Simplified process flow for La_2O_3-gated MOS capacitors after standard deposition.
(B) Simplified process flow for La_2O_3-gated MOS capacitors after modified deposition.

A simplified MOSCAP process flow with standard and modified La_2O_3 deposition is schematically depicted in figure 2.3 (A-B). For process 1, different metals as well as different PDA and PMA temperatures were used. For process 2, samples with PMA at different temperatures were obtained. For these two processes, as-deposited (no-annealing), PDA and PMA samples were obtained.

Outline of the MOSFET fabrication processing, a micrograph of the fabricated MOSFET's along with its cross sectional view are shown in figure 2.4 (A-B-C). The gate structure is of the type W–La_2O_3–pSi (nMOSFET) for the as-depo sample. After Source/Drain (S/D) implantation and thermal activation through SiO_2-based windows, wet chemical cleaning of the gate active area is done by SPM and HF-last step as in the MOSCAP case. This is followed by deposition of La_2O_3 whether in vacuum or within an O_2 flow to reduce oxygen losses in the film. Only *in-situ* metallization of tungsten by sputtering is done in a contiguous chamber within the same MBE system immediately after the dielectric deposition in order to keep the UHV conditions during this step, thus reducing the exposure of La_2O_3 surface to environment.





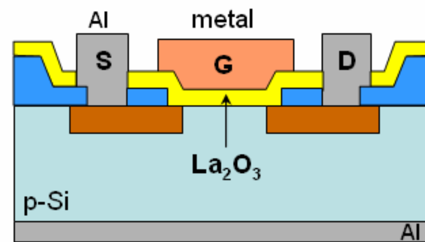


Fig. 2.4 (A) La_2O_3-gated MOSFET fabrication flow (only in-situ metallization and PMA processing). (B) Micrograph of fabricated W-La_2O_3 gated MOSFET structure (L/W = 10/50 μm). (C) Cross-sectional view of the MOSFET structure shown in (B).

The tungsten metallization step by sputtering is done at room temperature (RT). The gate area definition and the opening of windows for S/D metallization with aluminum are obtained after photolithography. Once Al is directly evaporated on the exposed surfaces of S/D areas, the remaining aluminum metal is removed by lift-off and the samples are then ready for PMA in N_2. After PMA, the back contact electrode is deposited and that finalizes the fabrication of the W-La_2O_3 gated MOSFET structures used in this study. A micrograph of the fabricated W-La_2O_3 MOSFET structure is shown in Fig. 2.4 (B).

2.3 Fabrication process

In this sub-chapter, next major fabrication steps outlined in Figs. 2.1 and 2.4 will be discussed in details (including operational theories and actual fabricating conditions):

- Si surface cleaning and preparation
- E-beam evaporation of La_2O_3
- Low temperature annealing by rapid-thermal anneal (RTA)
- Metal gate evaporation
- Metal gate and La_2O_3 etching
- Photolithography

2.3.1 Si surface cleaning and preparation

ULSI technology requires more stringent and reliable means to control the surface smoothness and to get rid of particles and contamination, such as metallic and organic residues on the silicon surface, than does VLSI technology. These basic concepts to remove contamination have not changed since they were developed. However, as the dimensions of the devices have shrunk to submicrometer scale, additional requirements have been proposed for an ultra clean wafer surface in VLSI and ULSI. The sources and the related effects of the contaminations are shown in table 2.1. Different contaminants will cause different effects on device reliability.

Table 2.1 Sources and related effects of various contaminations

Contamination	Possible source	Effects
Particles	Equipment, ambient, gas, deionized (DI) water, chemical	Low oxide breakdown (BKD). Poly-Si and metal bridging-induced low yield
Metal	Equipment, chemical, reactive ion etching (RIE), implantation, ashing	Low BKD field. Junction leakage. V_t shift
Organic	Vapor in room, residue of photoresist, storage containers, chemical	Change in oxidation rate
Microroughness	Initial wafer material, chemical	Low oxide BKD field. Low mobility of carrier
Native oxide	Ambient moisture, DI water, rinse	Degraded gate oxide. Low quality of epi-layer. High contact resistance. Poor silicide formation.

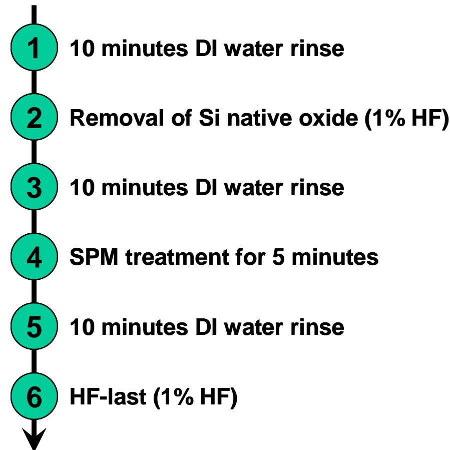


Fig. 2.5 Si wafer cleaning and surface preparation steps.

In this dissertation, the surface cleaning and preparation processes is outline in fig. 2.5. First of all, Si wafer is rinsed with running DI water for 10 minutes before removal of native oxide at the Si surface by dipping into 1 % HF. After that, the Si wafer is again rinsed with running DI for 10 minutes prior to SPM (H_2SO_4:H_2O_2 = 4:1) treatment for up to 5 minutes. SPM helps formed chemical oxide (SiO_x) layer at the Si surface and at the same time removed existence organic and metallic impurities. Prior to dipping into 1 % HF

solution, Si wafer is against rinsed with running DI water for the third times. After final step 1 % HF dip treatment, Si wafer with hydrogen terminated (or HF-last) surface is then ready to be loaded into UHV chamber for La_2O_3 deposition.

2.3.2 E-beam evaporation of La_2O_3

In this study, La_2O_3 film is deposited by the E-beam evaporation method in the ultra high vacuum chamber (deposition chamber), as shown in fig. 2.6. There are four compartments to allocate same/different solid sources at the bottom of the chamber. La_2O_3 is then bombarded and subsequently heated by the E-beam, which is located near the source and its beam being controlled by a magnetic sweep controller. The E-beam is accelerated at 5 kV prior to bombardment onto solid La_2O_3 source. Now, there are many types of pumps, but the ones used to create UHV conditions are typically one or more of the following: turbo molecular (TMP), diffusion (DP), ion or (IP), sublimation (SP) or cryopumps (CP). The base pressure inside growth chamber is maintained at 10^{-8} Pa by using IP together with liquid nitrogen (LN) trap. Then, since the chamber is maintained at the ultra high vacuum state, the La-O molecule begins to evaporate when the temperature of the source is greater than the evaporation temperature. Evaporation temperature is reported as 1820 °C at vapor pressure at 10^{-4} Pa [2]. The Si substrate is heated and its temperature is maintained at 250 °C during La_2O_3 deposition. Chamber pressure during deposition is around 10^{-7} - 10^{-6} Pa. The physical thickness of La_2O_3 thin film is controlled and monitored through crystal oscillator for better thickness controllability. To ensure better uniformity during deposition, the sample holder, which contain the Si wafer is rotated at 30 rpm.

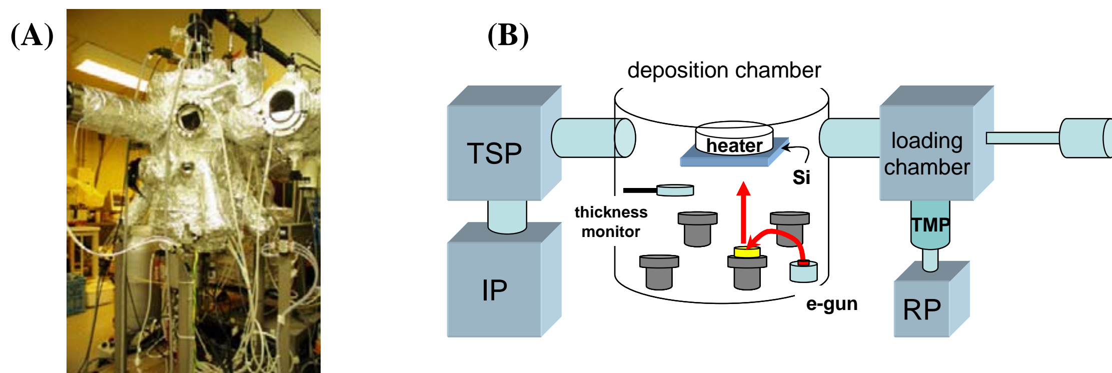


Fig. 2.6 (A) Photograph of MBE chamber 1 used for the deposition of La_2O_3 on silicon.
(B) Schematic of the La_2O_3 deposition within MBE chamber with UHV.

In general, as-deposited films (without annealing) have large atomic defects compared to the thermally grown film. This deficiency of the composition often leads to the fixed oxide charge. Since the fixed charge of the as-deposited La_2O_3 film is always positive, oxygen deficiency in the film are expected, which can function as trapping centers for electrons and consequently, affect the reliability properties of La_2O_3-gated MOS devices (shifts in flat band voltage Vfb after trapping of electrons by electrical stress).

2.3.3 Low temperature annealing by rapid-thermal anneal (RTA)

Thermal annealing processes are often used in modern semiconductor fabrication for defects recovery, lattice recovery or impurity electrical activation of doped or ion implanted wafers. In this study, low temperature (between 300°C–600°C) thermal treatments utilizing infrared lamp typed rapid thermal anneal (RTA) system were used. The MILA-3000 and QHC-P610C RTA systems from ULVAC Co., were used for oxygen (O_2), nitrogen (N_2) or forming gas (97% N_2 + 3% H_2) annealing, either for post deposition

annealing (PDA) or post metallization annealing (PMA). Fig. 2.7 illustrates the schematic drawing for MILA-3000 [3] whereas fig. 2.8 shows photographs of both RTA systems. Prior to every annealing cycle, existent gases inside the anneal chamber and gas lines were pumped and purged out to minimize any possibility of contamination of other residual gases or particles. This RTA system is heated-up by infrared lamp heating furnace and cooled-down by constant flowing of pipe water. Thus, it has an asymmetric profile of temperature ramping for heating up and cooling down. The ramp up rate of annealing temperature is set at 400 °C/min. The gas flow rate is kept at 1.2 l/min for annealing cycles. All annealed samples were removed from the chamber at 100 °C.

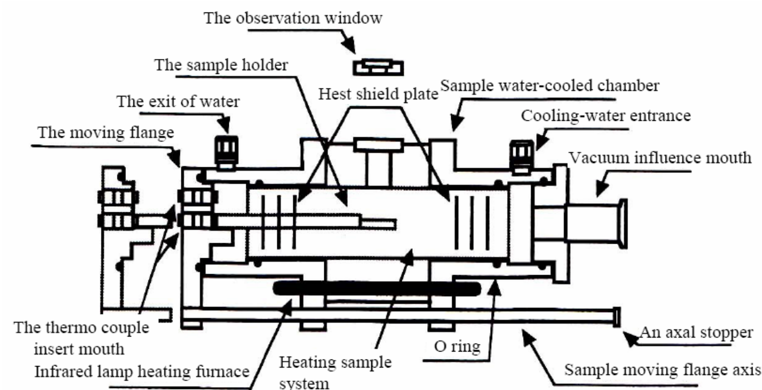


Fig. 2.7 Schematic drawing of MILA-3000 RTA system.

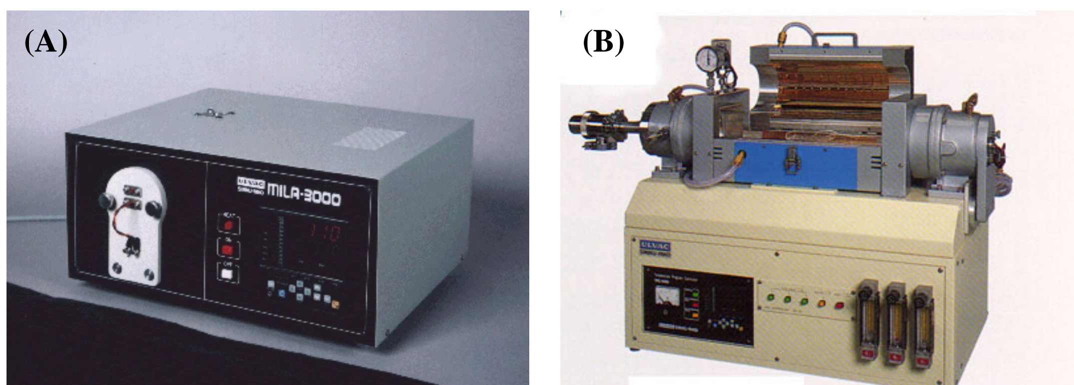


Fig. 2.8 (A) Photograph of RTA system MILA-3000 used for the annealing of La_2O_3 on silicon.
(B) Photograph of RTA system QHC-P610C used for the annealing of La_2O_3 on silicon.

2.3.4 Deposition of metals for gate electrodes

At least three different types of metal gate materials have been studied and analyzed yet tungsten (W) was used as the main gate electrode in this dissertation. Because of different melting temperatures, all these different metals, aluminum (Al), platinum (Pt), tantalum (Ta), ruthenium (Ru) and tungsten (W) were evaporated by using different techniques. The melting temperature for Al is the lowest, at around 660 °C, thus, Al can be evaporated by using thermal evaporation method. On the other hand, Pt, Ru, Ta and W have higher melting temperatures of 1768°C, 2334°C, 3017°C and 3422°C, respectively [4]. Thus, these higher melting temperature materials can be deposited on top of La_2O_3 either by E-beam evaporation or RF-sputtering. In this study, E-beam evaporation for Pt and RF sputtering for Ru, Ta and W deposition on La_2O_3 were used. Initially, metal shadow mask (15 mm X 15 mm) consisting of multiple 100 μm and 200 μm diameter round shape patterns were used to form the metal gate of La_2O_3 MOSCAP, besides, photolithography was also used for the gate electrode definition as shown in fig. 2.1B. For La_2O_3-gated MOSFET structures, only tungsten was sputtered directly on La_2O_3 and then patterned by photolithography. All MOS capacitors and MOSFETs were coated with Al as backside electrode.

2.3.4.1 Thermal evaporation of Al gate electrode

Aluminum evaporation in this study was formed by using bell-jar type thermal evaporation as illustrated in fig. 2.9. This system utilized a turbo molecular pump (TMP) to achieve background pressure up to 1.0x10-5 Pa prior to Al evaporation at 300 °C (achieved

after DC current flow through the tungsten-type filament at around 18 A). The filament used to hold Al wires is made of tungsten. The purity of both W filament and Al source is 99.999%. Methanol and acetone were used to clean the W filament and Al wires prior to every evaporation process. Chamber pressure during evaporation is $2x10^{-5}$ to $4x10^{-5}$ Pa.

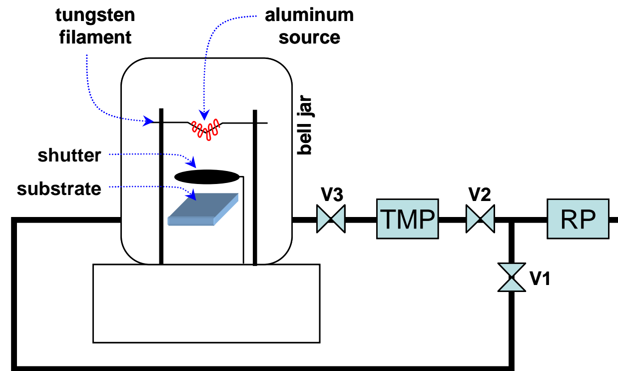


Fig. 2.9 Schematic drawing of bell-jar type thermal evaporator system.

2.3.4.2 E-beam evaporation of Pt gate electrode

The schematic cross section of Pt based e-beam evaporation system used in this study for Pt gate evaporation is shown in Fig. 2.10. E-beams were accelerated by 4 KV before bombarded onto Pt source. Base pressure during Pt evaporation is 10^{-4} Pa. Pt film thickness and evaporation rate are monitored by crystal oscillator throughout the whole evaporation process. Pt source used in this study has purity of 99.999 %.

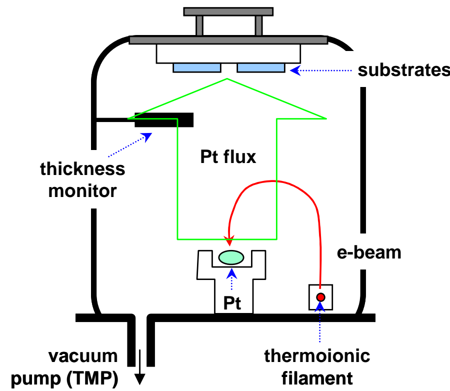


Fig. 2.10 Schematic drawing of Pt-based e-beam evaporation system.

2.3.4.3 RF-sputtering of Ta, Ru and W gate electrodes

All Ta, Ru and W thin films were deposited by RF magnetron sputtering due to their high melting temperatures. Figure 2.11 illustrates the schematic drawing for RF magnetron sputtering system. The deposition of Ta and Ru thin films is done by means of physical sputtering that occurs in a magnetically-confined RF plasma discharge within an inert argon (Ar) gas. The base pressure during sputtering process is 10^{-5} Pa. The flow rate and RF power of Ar gas is 7 sccm and 150 W, respectively. The system is equipped with auto impedance matching circuit. For the deposition of W, the sputtering of this film occurs whether outside/within the MBE deposition chamber (see process flow of fig. 2.1B) so that *ex-situ* W deposition is done within the former sputtering system (outside the MBE system) and *in-situ* W deposition is done within the same MBE system in UHV conditions where no carrier gas is available. Whether with *ex-situ* or *in-situ* tungsten deposition, the physical sputtering process for the deposition of this metal is the same.

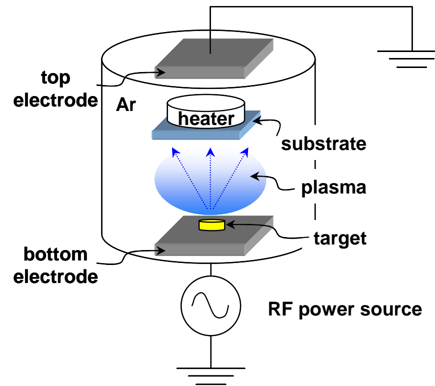


Fig. 2.11 Schematic drawing of a typical RF sputtering system.

2.3.5 Metal gate and La_2O_3 etching

The etching process of Al, Pt and W metal gates were all different between each other. Initially, Al and W metal gates were etched by using chemical solvent (wet etching process) whereas Pt metal gate electrode's pattern was defined after dry etching process. Al etching is done at 50°C by using phosphoric acid (H3PO4:H20 = 1:1) whereas W gate was formed after dipping into hydrogen peroxide (H_2O_2) at room temperature. Ar bombardment inside reactive ion etching (RIE) system was used for Pt gate electrode formation. Ar flow rate and RF power is 50 sccm and 150 W, respectively. After that, resist layer on top of Pt was removed by O_2 flashing method inside the same RIE system. Aqua regia (mixture of HNO3 and HCl) is not suitable for etching of Pt/ La_2O_3 structure due to its reaction with La_2O_3 (La_2O_3 will react with HCl even at very low HCl concentration at room temperature). For the last samples (W-only metallized MOSCAP and MOSFET), RIE was performed to define W-based patterns. W etching by RIE was done within SF6 gas at 30W by 1 min and this was followed by O_2-based ashing for resist removal.

2.3.6 Photolithography

The photolithography process flow which was used throughout this study is shown in fig. 2.12. Electrical hotplate is used for baking purposes. Spin coating consists of coating OAP (5000 rpm, 20 seconds spin) and OFPR800 (3000 rpm, 20 seconds spin) layers. The spin-coated dual-layer photoresist was aligned and exposed through tungsten coated e-beam patterned hard-mask with high-intensity ultraviolet (UV) light at 405 nm wavelength. MJB3 of Karl Suss contact-type mask aligner was used for aligning and exposition purposes. The exposure duration was set to 13 sec. After that, exposed wafers were developed using the specified developer called NMD-3 (Tokyo Ohka Co. Ltd.) by dipping them into the solvent for 1 minute. Baking at 110 °C for 5 minutes is necessity to harden the developed photoresist pattern before metal gate etching or prior to S/D metallization (lift-off method).

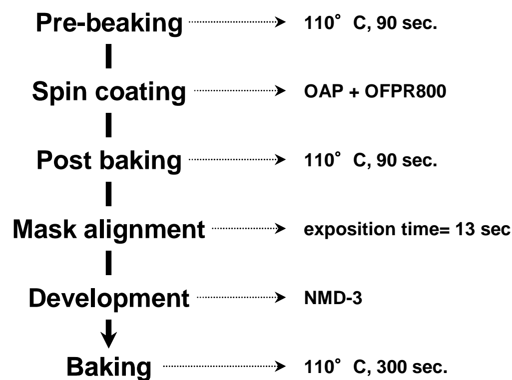


Fig. 2.12 Photolithography process flow.

2.4 La_2O_3 deposition in O_2 with *in-situ* metallization

Two different La_2O_3 deposition methods were used in order to evaluate the impact of *O_2-flow* and tungsten *in-situ* metallization for reliability characterization. The silicon substrate doping for all samples was between 1e15 to 6e15 cm^{-3}. Only dry N_2-based annealing was performed for all the samples.

Because the deposition of La_2O_3 in UHV conditions at 300°C is regarded as being done under PDA conditions, the occurrence of oxygen losses during the deposition of the La_2O_3 film would create defects for the trapping of charge that ultimately will pose serious restrictions on the final reliability of MOS devices with these films. In order to reduce any possible oxygen loss during the La_2O_3 deposition [5], La_2O_3 film for these samples was deposited at 300°C within an oxygen flow of 1x10-5 Pa. Also, in-situ sputtering of tungsten was done at 150W in a contiguous chamber (within the same MBE system) immediately after the dielectric deposition in order to reduce the exposure of La_2O_3 surface to the environment. Because of this, the physical thickness of La_2O_3 cannot be measured by conventional methods like ellipsometry but by transmission electron microscopy or any other imaging technique. During the deposition of the metal an argon flow of 1.33 Pa was used. Patterning of the gate electrodes was done by reactive-ion etching using SF6 plasma with a 30W power. There were Si O_2-based spacers (200nm in thickness) used around the gates of the devices in order to minimize La_2O_3 exposition to environment's moisture. Only PMA was done in N_2 ambient at 300°C and 500°C during 5 min. A simplified process flow

for these samples is shown in fig. 2.3B where it can be compared to the process flow of *“standard”* deposition of La_2O_3 on silicon (fig. 2.3A).

2.5 Physical characterization

The physical characterization of deposited La_2O_3 films consisted of spectroscopic ellipsometry measurements for physical thickness determination (of as-deposited samples or La_2O_3 without annealing), transmission electron microscopy (TEM) for the imaging of the structures created before and after annealing and X-ray photoelectron microscopy (XPS) measurements for the determination of the nature of the interfaces created between La_2O_3 and silicon before and after annealing.

2.5.1 Spectroscopic ellipsometry

This technique uses a polarized laser light source which is directed to the oxide-covered wafer at a specified angle. The polarized beam enters the semi-transparent oxide film and reflects off the reflective wafer surface. During its passage through the film, the angle of the beam plane is rotated. The amount of rotation of the beam is a function of the thickness and index of refraction of the film. A detector in the instrument measures the amount of rotation and an onboard computer calculates the resulting thickness and index of refraction. Ellipsometer accuracy and range is enhanced with the addition of multi-viewing angle capabilities, multiple wavelengths sources and reduction in beam spot size. The

La_2O_3 physical thickness was optically extracted by Otsuka FE-5000 ellipsometer using a Cauchy model and a single layer approximation [6]. Incident angle was fixed at 70°. Photon energy varied from 1.55 to 4.14 eV, which correspond to wavelengths from 800 to 300 nm and which were used for data fitting. Film thickness without PDA corresponds to the as-deposited (as-depo) film thickness. The schematic setup of an ellipsometry experiment for La_2O_3 thickness measurement is depicted in fig. 2.13.

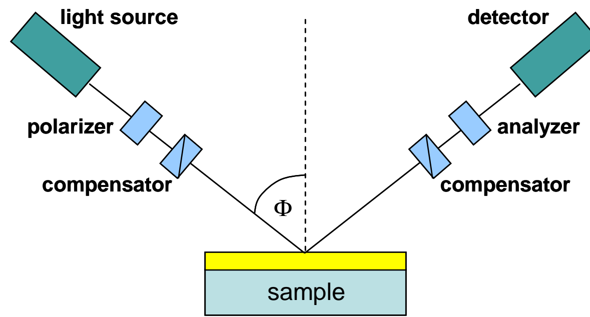


Fig. 2.13 Schematic setup of an ellipsometry experiment.

The refractive index *n* increases with decreasing wavelength in the visible range, and this is referred to as normal dispersion. One of the common empirical relations for this behavior is the Cauchy formula:

$$n = A + (B/\lambda^2) + (C/\lambda^4) \quad (2.1)$$

Here, *n* is the refractive index of a single wave length. A, B and C are all fitting constants. On the other hand, in the region of the natural frequency where resonance occurs, the index *n* decreases with the decreasing of wavelength and this is known as anomalous dispersion. Eq. 2.1 can be derived in the following way. The square of the refractive index *n*, at frequencies far from the resonant frequency, is expressed by the relation:

$$n^2 = 1 + \frac{Ne^2 / \pi m}{\nu_o - \nu} \tag{2.2}$$

Where N is the number of the atoms per unit volume, e is the electronic charge, m is the electronic mass, V_0 is the natural frequency, and finally V is the frequency of the incident radiation. If V >> V0, with the binomial series expansion, Eq. 2.2 becomes:

$$n^2 = 1 + \frac{Ne^2}{\pi m}\frac{1}{\nu_o^2}\left[1 - \left(\frac{\nu}{\nu_o}\right)^2\right]^{-1} = 1 + \frac{Ne^2}{\pi m}\frac{1}{\nu_o^2} - \frac{Ne^2}{\pi m}\frac{\nu^2}{\nu_o^4} \tag{2.3}$$

Densification of the films after PDA can be evaluated by the film density obtained from the Lorentz-Lorenz relationship, in the similar fashion of SiO_2 thin film case. From the refractive index *n*, the film density can be determined by the Clausius-Mossotti (CM) or Lorentz-Lorenz relationship [7]:

$$\rho = K\frac{n^2 - 1}{n^2 + 2} \tag{2.4}$$

Where K is a constant, which can be evaluated using the values of bulk La_2O_3.

2.5.2 Transmission electron microscopy

Cross section of the fabricated samples was observed by transmission electron microscope (TEM). The principle of TEM is similar to that of optical microscope. In TEM, observation is made in ultrahigh vacuum, where an electron beam is focused onto the sample by electromagnetic lenses. Because the electron beam's wavelength is less than that of visible spectra, resolution of TEM is higher than the conventional optical type microscope. The thickness of the sample must not be greater than 0.1 μm in order for the electron beam to transit through the structure under study. Thus, special way of sample

preparation has to be done prior to every cross section evaluation. In this study, Hitachi FB-2100 system which is a focus ion beam (FIB) system and equipped with micro-sampling module was used for sample preparation, which will be then transferred to Hitachi HD-2300 scanning transmission electron microscope (STEM) ultra-thin film evaluation system for observation and evaluation. Prior to transfer to HD-2300 system, TEM samples were treated and cleaned with ozone (O3) plasma to reduce ion density on the sample's surface. Samples preparation and observation was done in Fujita laboratory of Tokyo University. Figure 2.14 shows photographs of W (30nm) – La_2O_3 (8nm) stacked structure with and without O_2 flow during La_2O_3 deposition.

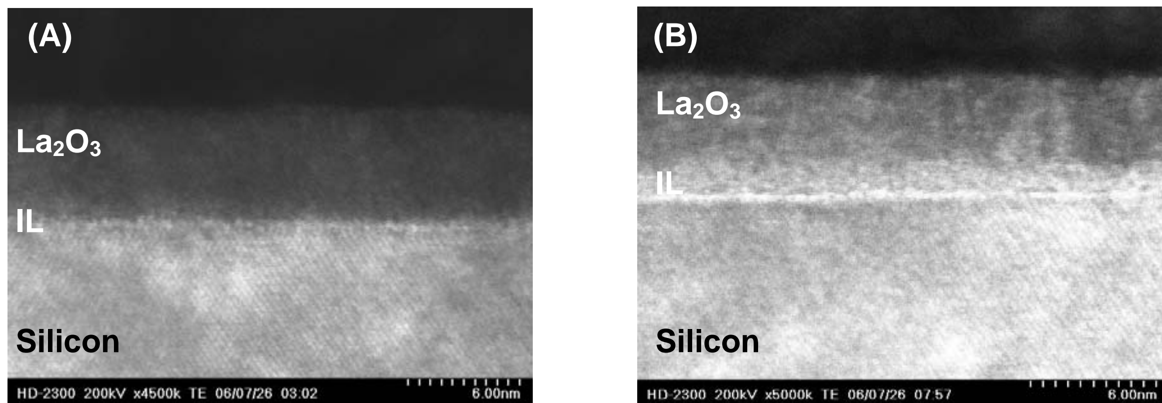


Fig. 2.14 (A) TEM of W-La_2O_3 without O_2 flow during deposition (as-depo).
(B) TEM of W-La_2O_3 **with O_2 flow** during deposition (as-depo).

The deposition of La_2O_3 within O_2 ambient is intended to minimize any oxygen losses within the oxide that could occur during the deposition of the film. This is done in order to reduce the density of oxygen vacancies-type of defects that could serve as centers for trapping of charge and thus decrease the final reliability of the La_2O_3-gated (oxygen

deficient) MOS devices. On the other hand, it is seen from fig. 2.14 that the introduction of O_2 during the deposition of the La_2O_3 film will increase the thickness of the IL so that a final lower dielectric constant for the whole stack can be expected. This imposes a serious limitation towards the fabrication of La_2O_3-gated devices with sub 1nm EOT.

2.5.3 X-ray photoelectron spectroscopy (XPS)

X-ray Photoelectron Spectroscopy (XPS) is a quantitative spectroscopic technique that measures the chemical composition and electronic state of the elements that exist within a material. XPS spectra are obtained by irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energy (KE) and number of electrons that escape from the top 1 to 10 nm of the material being analyzed. XPS requires ultra-high vacuum (UHV) conditions. Fig, 2.15 shows a typical XPS experimental setup.

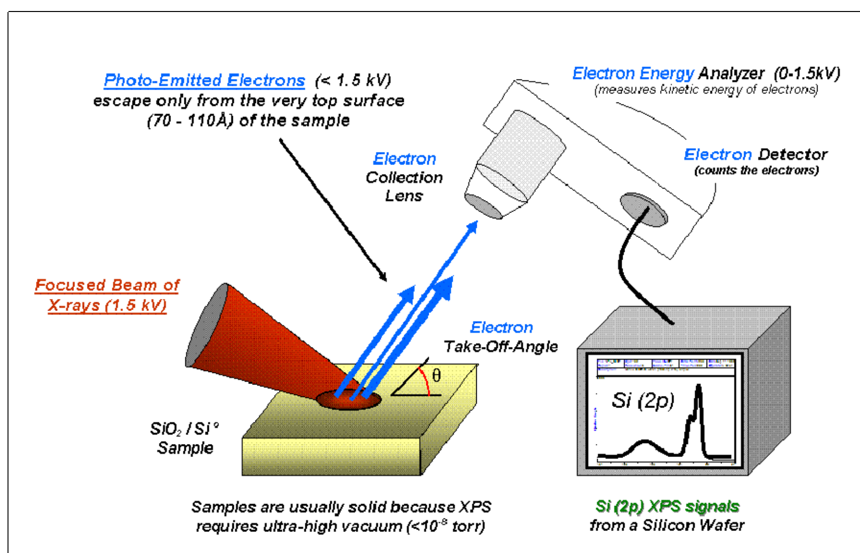


Fig. 2.15 Basic components of a monochromatic XPS system.

A typical XPS spectrum is a plot of the number of electrons detected (Y-axis, ordinate) versus the binding energy of the electrons detected (X-axis, abscissa). Each element produces a characteristic set of XPS peaks at characteristic binding energy values that directly identify each element that exist in or on the surface of the material being analyzed. These characteristic peaks correspond to the electron configuration of the electrons within the atoms, e.g., 1s, 2s, 2p, 3s, etc. The number of detected electrons in each of the characteristic peaks is directly related to the amount of element within the area (volume) irradiated. To generate atomic percentage values, each raw XPS signal must be corrected by dividing its signal intensity (number of electrons detected) by a "relative sensitivity factor" (RSF) and normalized over all of the elements detected. To count the number of electrons at each KE value, with the minimum of error, XPS must be performed under ultra-high vacuum (UHV) conditions because electron counting detectors in XPS instruments are typically one meter away from the material irradiated with X-rays. It is important to note that XPS detects only those electrons that have actually escaped into the vacuum of the instrument. The photo-emitted electrons that have escaped into the vacuum of the instrument are those that originated from within the top 10 to 12 nm of the material. All of the deeper photo-emitted electrons, which were generated as the X-rays penetrated 1–5 micrometers of the material, are either recaptured or trapped in various excited states within the material. For most applications, it is, in effect, a non-destructive technique that measures the surface chemistry of any material. Fig. 2.16 shows a typical XPS spectrum for the analysis of La_2O_3 deposited on silicon with O_2 flow. The detection of a La-silicate and SiO_2-based interfacial layers after PMA are clearly demonstrated with this technique.

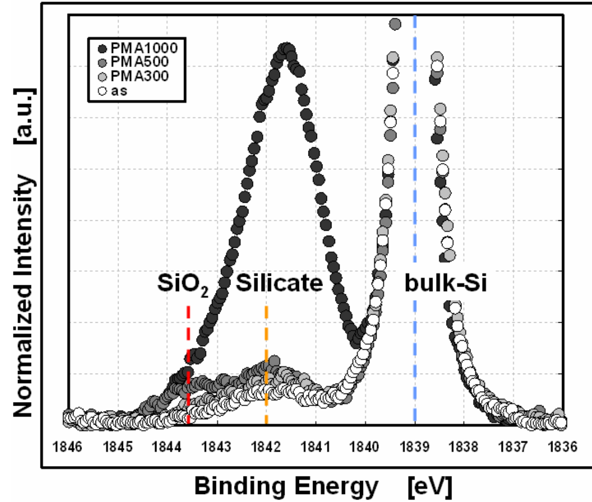


Fig. 2.16 Annealing temperature dependence of Si 1s XPS spectrum of La2O3 deposited within oxygen flow. A La-silicate IL formation is present for all samples whereas an additional SiO2-based IL formation appears for PMA at 500°C.

2.6 Electrical characterization

In this sub-chapter, electrical measurement techniques and characterization methods that were used for the analysis and evaluation of La_2O_3 MOSCAP and MOSFET structures in this study will be discussed in detail. This section is separated into two main categories, MOSCAP and MOSFET electrical characterization. The capacitance-voltage (C-V) and gate leakage current density-voltage (Jg-V) are used to evaluate the oxide's equivalent oxide thickness (EOT), hysteresis, flatband voltage (Vfb) and leakage current density of fabricated MOS capacitor and MOSFET structures. I-V plots from MOSFET are

used to evaluate the subthreshold slope (a.k.a. subthreshold swing), which is related to channel interface properties and threshold voltage (Vth) extraction. Finally, the charge pumping evaluation technique for the extraction of *interface-states density* Dit is presented.

2.6.1 C-V measurement

A detailed introduction of C-V and its basic operating principles can be found on Schroder [8]. The high frequency C-V measurement technique was used to evaluated the C-V profiles in terms of high frequency dependency (1 KHz – 1 MHz), magnitude of hysteresis, flatband voltage shift and EOT determination. Step voltage for both forward and backward sweeps was 50 mV on all C-V measurements. Magnitude of hysteresis is calculated from the biggest gap between forward and backward sweeps. Vfb shift is accurately determined by plotting $(1/C)^2$ versus Vg. The lower knee of this curve occurs at Vg=Vfb. Such a transition is sometimes difficult to determine due to distortion on the initial C-V curve. Differentiating this curve and finding the maximum slope of the left flank of this differential curve a second time results in a sharply peaked curve whose peak coincide with Vfb. For comparison purposes, CVC software (version 5) developed by North Carolina State University [9] was also used to determine the EOT taking into consideration the quantum mechanic tunneling effect. EOT calculations were based on high frequency 100 KHz C-V curve. Together with the La_2O_3 physical thickness obtained from spectroscopic ellipsometry measurement and the calculated EOT, dielectric constant of deposited La_2O_3 film can be easily determined:

$$k_{La2O3} = \frac{t_{La2O3}}{EOT} \times k_{SiO2} \tag{2.5}$$

2.6.2 Ig-Vg measurement

I-V measurements were done on HP4156A semiconductor parameter analyzer with a 25 mV voltage step and 100msec/step measurement setup for every single sample in order to ensure proper distribution on the leakage current density. Metal gate electrode with circular patterns and different diameters were used in this study when measuring the gate leakage current of MOSCAP. The measurement started at 0 V and sweep towards accumulation region until breakdown occurs. Detailed analyses on conduction mechanisms of La_2O_3 can be found on Kim [10]. For all the samples, capacitance–voltage (C-V), current–voltage (I-V) and time-dependent dielectric breakdown (TDDB) characteristics were obtained with a precision LCR meter (Agilent 4284A) and semiconductor parameter analyzer (Agilent 4156C) respectively.

2.6.3 Threshold voltage (Vth) determination

Threshold voltage (Vth) is an important MOSFET parameter. However, Vth is a parameter that is not uniquely defined. The existence of nonlinearities at the subthreshold region on the Id-Vg plot makes it difficult to have a universal definition. One of the most common threshold-voltage determination techniques is the “linear extrapolation method”. Here, the drain current Id is measured as a function of gate voltage at a low drain voltage of 100 mV to ensure operation in the linear MOSFET region. The threshold voltage is not zero below threshold and approaches zero only asymptotically. Hence the Id versus Vg curve is extrapolated to Id = 0, and the threshold voltage is determined from the extrapolation or

intercept gate voltage Vg by:

$$Vth = VG_{Si} - \frac{Vd}{2} \tag{2.6}$$

Where VG_{Si} is the intercepted Vg value at Id = 0 and Vd is the drain voltage used during the measurement (100 mV in this study). The Id–Vg curve deviates from the straight line at low gate voltage below threshold voltage due to subthreshold currents and above threshold voltage due to series resistance and mobility degradation effects. Thus, in order to determine the threshold voltage accurately, it is a common practice to find the point of maximum slope on the Id–Vg curve by maximum in the transconductance, then fit a straight line to the Id–Vg curve from this point and extrapolate to Id = 0, see fig. 2.17.

Fig. 2.17 Linear extrapolation for Vth extraction from Id-Vg curve.

2.6.4 Charge pumping for interface-state density (Dit) measurement

In this study, measurement of interface state density based on charge pumping technique on fabricated La_2O_3 MOSFET is used for evaluation and characterization

purposes. The measurement of Dit is done before and after a positive constant voltage stress under which a fixed density of charge is trapped inside La_2O_3 and at its interfaces. Then we correlate the change in Dit after TDDB stress with respect to the resulted changes in Vt in order to establish/eliminate a relationship between Vt instability and Dit increase after stress. Charge pumping method, originally proposed in 1969 by Burgler and Jespers [11], allows probing of interface state density of actual small geometry MOSEFT instead of large diameter MOS capacitor. Thus, eliminating the need of a separate test device and extrapolate the electrical characterizations between MOS capacitor and MOSFET. The measurement setup of charge pumping is shown in Fig. 2.18.

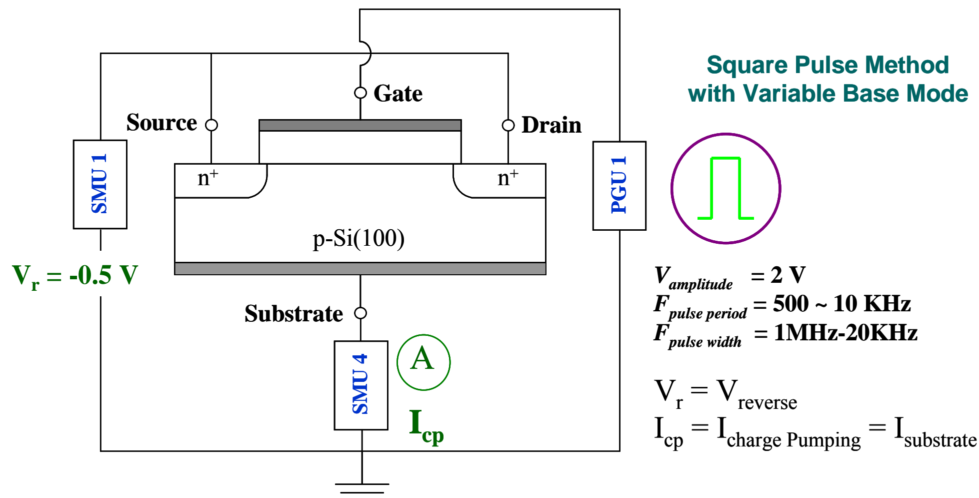


Fig. 2.18 Charge pumping measurement setup for the extraction of Dit.

The MOSFET's source and drain are both interconnected and slightly reverse biased with Vr = -0.5 V. The time varying gate voltage (pulse unit) is 2 V, sufficient enough for the Si surface under the gate to be driven into inversion and accumulation. Square type

pulse train with 100 KHz pulse width was used throughout the Dit evaluation. The charge pumping current (Icp) is then measured at the substrate. The charge pumping action proceeds in the following manner. When the pulse is on (transits from accumulation to inversion), electrons flow to the surface from the source and the drain. The interface states capture the inversion electrons and become negatively charged. When the pulse is off (transit from inversion to accumulation), the inversion electrons immediately flow back to the source and the drain while the captured electrons are still retained by the interface states. However, the surface is accumulated now and the holes are captured by the negatively charged interface states resulting in recombination. The holes, needed in this recombination, flow through the substrate. Thus, by measuring the charge pumping current at the substrate, the interface state density can be obtained by following equation:

$$Dit = \frac{I_{cp}}{f \times q \times Ag} \tag{2.7}$$

Where Icp is the measured charge pumping current (measured at the substrate), f is the pulse frequency used in the measurement, q is the magnitude of electron charge and Ag MOSFET's gate area. The transit time from pulse's off to on and vice versa is 10 MHz.

2.7 Reliability measurement techniques

This section introduces the measurement principles behind the reliability characterization used on La_2O_3-IL stacked oxides thorough this study. Reliability can be defined as the probability of operating a product for a given time under specified conditions

without failure. Failure can be defined as the cease in the operational functions of the measured device or as device parameter degradation, i.e. if the MOSFET threshold voltage drifts from its specified value, the drain current changes and the circuit may not operate within its specification. Since the gate oxide of an MOS device is one of the most important MOS device parameters, it is very sensitive to damage and can be easily degraded. Although the oxide resistivity is on the order of 10^{15} $\Omega\cdot$cm (for SiO_2), it is not infinite. Hence, gate currents flow through a gate oxide for any gate voltage and with the reduction in the oxide thickness they growth exponentially with applied voltage. To characterize the lifetime and integrity of gate oxides, voltages higher than operating voltages or temperatures higher than operating temperatures are used with appreciable current flow through the oxide.

2.7.1 TZDB and TDDB measurements

Oxide integrity is determined by time to zero and time dependent dielectric breakdown measurements (TZDB and TDDB respectively). TZDB measurement method is simply an Ig-Vg MOS device measurement with increasing gate voltage until the oxide breaks down, see fig. 2.19A. The breakdown voltage is gate-voltage ramp–rate dependent. This dependence is related to the damage created in the oxide during the measurement. For low ramp rates, more time is available to create damage resulting in lower breakdown voltage than for higher ramp rates. For TZDB measurements of La_2O_3-gated MOS devices, we used a ramp rate of 100 mV/sec in all cases.

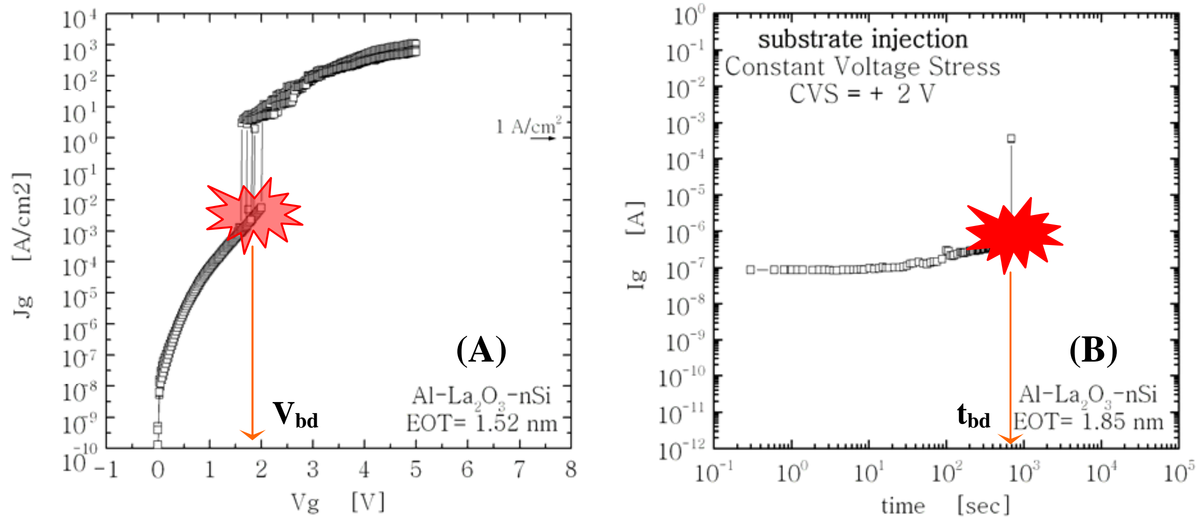


Fig. 2.19 (A) TZDB I-V plot. Vg increases until La2O3 reaches breakdown at Vbd the breakdown voltage. (B) TDDB I-t plot. For a fixed Vg, Ig evolves with time until breakdown occurs at tbd.

The time-dependent measurements are the constant gate voltage and constant gate current methods. We make use only of constant gate voltage stressing (CVS) conditions for the degradation and breakdown of La_2O_3-gated MOS devices, see fig. 2.19B. In the CVS-TDDB method, a gate voltage near the breakdown voltage Vbd (illustrated in the Ig-Vg plot) is applied and the gate leakage current is measured as a function of time. The evolution of gate leakage current with time during the CVS conditions, will increase or decrease with respect to its fresh condition or initial value (at t= 0 sec) depending on the density and polarity of the charge trapped into La_2O_3 and at its interfaces. When a sudden jump in leakage current occurs, the time of this event is defined as the time to breakdown t_{bd} point. Time to breakdown is a very important parameter since stressing of multiple samples with different magnitudes of gate voltage will result in a broad range of tbd data

and by extrapolating all these tbd data with respect to applied gate voltages, the lifetime projection of La_2O_3 to operational voltages can be obtained. When the oxide is driven into breakdown, one defines a charge to breakdown Qbd as:

$$Qbd = \int_0^{tbd} J_g \, dt \tag{2.8}$$

Where t_{bd} is the time to breakdown and Qbd is defined as the charge density flowing through the oxide necessary to break it down and it depends mainly on the gate oxide thickness, magnitude, polarity as well as frequency of the CVS. In fig. 2.19B, Qbd is the area under the curve so that even with samples presenting different levels of gate leakage current during TDDB measurements (which produce a broad range of tbd points), the use of Qbd as a comparison parameter helps greatly to reduce dispersion of the resulting data and thus, more accurate predictions of oxide lifetime can be realized.

2.7.2 Stress Induced Leakage Current (SILC)

An effect frequently observed in thin electric field-stressed oxides is a gate oxide current increase, referred to as SILC. It is defined as the increase of oxide leakage current after high-field stress compared to before stress (fresh condition). It is typically observed at low to moderate oxide electric fields and increases markedly as oxide thickness decrease. However, SILC decreases for oxides thinner than about 5 nm (where direct tunneling DT currents take over Fowler-Nordheim FN currents), believed to be due to reduced trap generation rates in thin oxides. Different models have been proposed to explain SILC: interface-state generation, bulk-oxide electron-trap generation, non-uniformities or weak

spot formation into the oxide films, trapped holes injected from the anode. SILC can be best explained by the generation of neutral electron traps in the oxide, allowing more current to flow through the oxide layer by these traps acting as “stepping stones” for tunneling carriers, know as trap-assisted tunneling. The generation of these neutral sites is caused mainly by the “trap creation” phenomenon related to hydrogen release by hot electrons. SILC is obtained by first measuring the Ig-Vg fresh condition characteristics of MOS devices, stressing the oxide with CVS-TDDB measurements and measuring the Ig-Vg characteristics again, this IV-TDDB-IV-TDDB-IV… cycle is repeated over and over again until the required conditions (certain amount of stressing time, injected charge, etc) are reached.

2.7.3 Charge pumping (CP) measurement

In the charge pumping (CP) method, a MOSFET is used as the test structure. We explain the technique with reference to fig. 2.20. The MOSFET source and drain are tied together and slightly reverse biased with V_R. The time varying gate voltage is of sufficient amplitude for the surface under the gate to be driven into inversion and accumulation. The pulse train can be square, triangular, trapezoidal, sinusoidal or tri level. The CP current is measured at the substrate, at the S/D tied together, or at the source and drain separately. Let us begin by considering the MOSFET in inversion, fig. 2.20(A). The corresponding semiconductor band diagram – from the Si surface in to the substrate – is shown in (C). For clarity we show only the semiconductor substrate on this energy band diagram. The interface traps, continuously distributed through the band gap, are represented by the small

horizontal lines at the semiconductor surface with the filled circles representing electrons occupying interface traps.

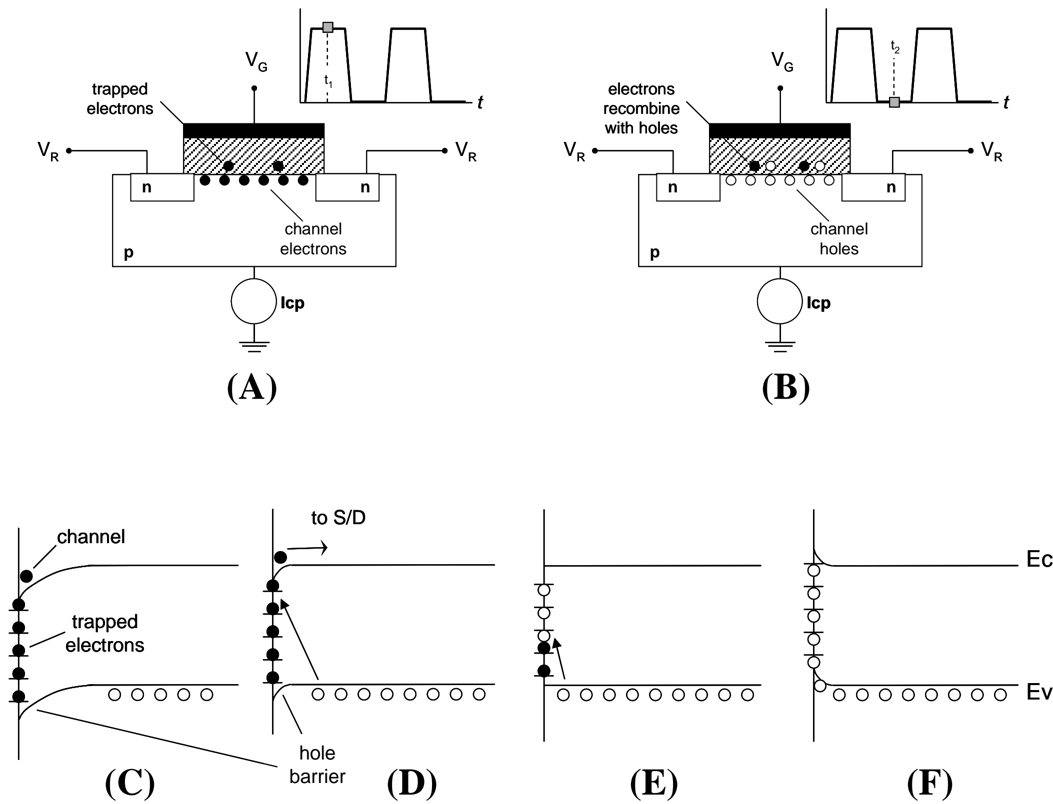


Fig. 2.20 (A-F) Device cross-sections and energy band diagrams for charge pumping measurements. The figures are explained in the text.

When the gate voltage changes from positive to negative potential, the surface changes from inversion to accumulation and ends up as in (B) and (F). However, the important processes take place during the transition from inversion to accumulation and from accumulation to inversion. When the gate pulse falls from its high to its low value during its finite transition time, most electrons in the inversion layer drift to source and

drain and electrons on those interface traps near the conduction band are thermally emitted into the conduction band (D) and also drift to source and drain. Those electrons on interface traps deeper within the band gap do not have sufficient time to be emitted and will remain on interface traps. Once the hole barrier is reduced (E), holes flow to the surface where some are captured by those interface traps still occupied by electrons. Holes are indicated by the open circles on the band diagrams. Finally, most traps are filled with holes as shown in (F). Then, when the gate returns to its positive voltage, the inverse process begins and electrons flow into the interface to be captured. Eight holes flow into the device in (B). Two are captured by interface traps. When the device is driven into inversion, six holes leave. Hence, eight holes in, six out result in a net charge pumping current Icp, that is proportional to Dit.

2.7.4 Carrier separation (CS) measurement

In MOS transistors, it is possible to monitor not only the gate current but also the substrate current simultaneously. This is a well-known technique usually referred to as carrier separation that allows identifying the dominant carrier type on the gate leakage current [12]. The identification of the major carrier contributor to leakage current can also help us to identity the major carrier contributor to the damage and consequent electrical degradation of the MOSFET characteristics with applied stress. A simplified carrier separation measurement methodology along with the contributions of electrons and holes to total gate leakage current Ig is illustrated in fig. 2.21 A-B for nMOSFET and pMOSFET devices respectively.

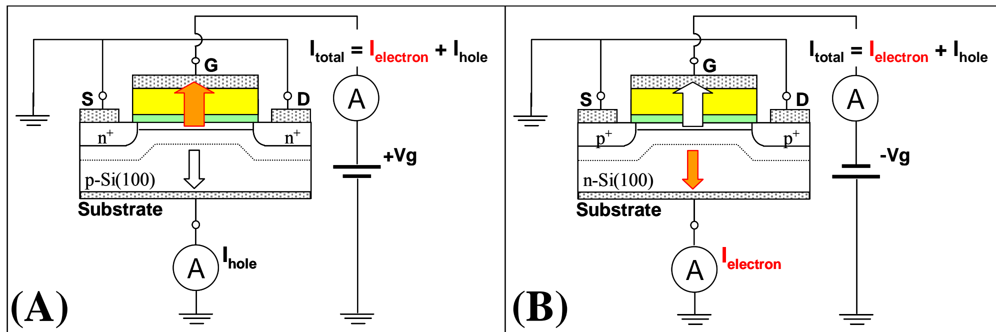


Fig. 2.21 (A) CS measurement for nMOSFETs in inversion (positive CVS). Both electron and hole current components are detected at the gate and substrate respectively.
(B) CS measurement for pMOSFETs in inversion (negative CVS). Even though both electrons and holes tunnel simultaneously through the gate oxide, only the hole current component is illustrated flowing through the oxide for clarity purposes. Both hole and electron current components are detected at the gate and substrate respectively.

References

[1] M. Copel at al., “Formation of a stratified lanthanum silicate dielectric by reaction with Si (001)”, Applied Physics Letters, **78** (11), 1607 (2001).

[2] H. Hughes and J. Benedetto, “Radiation effects and hardening of MOS technology: devices and circuits”, IEEE Trans Nuclear Science 2003;50(3):500-21.

[3] http://www.ulvac-riko.co.jp/MILA3000_E.htm

[4] http://www.webelements.com

[5] J.P. Maria, D. Wicaksana, A. I. Kingon, B. Busch, H. Schulte, E. Garfunkel, and T. Gustafsson, J. Appl. Phys. 90 (7), 3476 (2001).

[6] W. Kingery, H. Bowen, and D. Uhlmann, “Introduction to ceramics”, John Willey & Son, 2nd Edition, pp.664 (1976).

[7] A. Hippel, “Dielectrics and waves”, John Willey & Son, 1954.

[8] D.K. Schroder, “Semiconductor material and device characterization”, John Willey & Son, 2nd Edition, (1998).

[9] “NCSU CVC Analysis, Version 5.0”, North Carolina State University, (2000).

[10] Y. Kim, “Analysis of electrical conduction in rare earth gate dielectrics”, PhD thesis, Tokyo Institute of Technology (2005).

[11] J.S. Brugler and P.G.A. Jespers, “Charge pumping in MOS devices”, IEEE Trans. Electron. Dev., ED-16, pp.297-302 (1969).

[12] Chen I, Holland S, Young K, Chang C, Hu C, Appl Phys Lett 1986; 49:669–71.

Chapter 3

Reliability of metal gate–La_2O_3 MOS capacitors

3.1 Introduction

3.2 Influence of post-deposition annealing (PDA)

3.3 Influence of post-metallization annealing (PMA)

3.4 Evaluation of the metal gate electrode material

3.5 C-V and I-V characterization

3.6 Breakdown and reliability of metal gate–La_2O_3 thin films after post-deposition annealing in N_2

3.7 Charge trapping characteristics of W-La_2O_3-nSi MOS capacitors after post-metallization annealing in N_2

3.8 Degradation and breakdown of W-La_2O_3 stack after post metallization annealing in N_2

3.9 La_2O_3 post-breakdown I-V and I-t characteristics

3.10 Summary

References

3.1 Introduction

The reliability results of La_2O_3-gated MOS capacitors after low and high voltage stressing conditions are presented and discussed in this chapter. During low-stressing conditions for La_2O_3 (avoiding hard-breakdown, HBD) the degradation in the MOSCAP devices' parameters (shifts in Vfb, hysteresis, stress-induced leakage current SILC, etc.) could be measured and quantified. We also stressed the dielectric under higher electric-field strengths or longer stressing times so that HBD would eventually appear in order to obtain the lifetime of La_2O_3-gated capacitors. All these conditions are summarized in table 3.1 as follows:

Table 3.1 Obtained reliability data depending on the severity of the applied stress.

Severity of electrical stress	MOSCAP measurements	MOSFET measurements
Fresh condition (low voltages and low currents without stress)	Ig-Vg, Cg-Vg, Jg-EOT, Vfb, hysteresis, etc.	Ig-Vg, Id-Vg, Id-Vd, Vth, subthreshold slope Ss, transconductance gm, interface-states density Dit, etc.
Degradation	Vfb shit, hysteresis, stress-induced leakage current SILC,	Vth shift, negative and positive bias-temperature instabilities NBTI/PBTI, Ss shift, gm shift, carrier separation during stress, Dit shift, etc.
Breakdown	Time to zero dielectric breakdown TZDB, time-dependent dielectric breakdown TDDB, lifetime projection, time to breakdown tbd, charge to breakdown Qbd, soft, hard and progressive breakdown SBD, HBD, PBD.	TZDB, TDDB, lifetime projection, tbd, Qbd, SBD, HBD, PBD, carrier separation until breakdown, mechanism of breakdown, etc.

3.2 Influence of post-deposition annealing (PDA)

By annealing the as-deposited La_2O_3 within a relatively low temperature and N_2-based atmosphere, the electrical characteristics of the dielectric can be enhanced as shown in fig. 3.1. In this figure, the use of aluminum as the gate electrode for a La_2O_3-gated MOS capacitor is evaluated by obtaining the MOSCAP C-V electrical characteristics before and after PDA treatment.

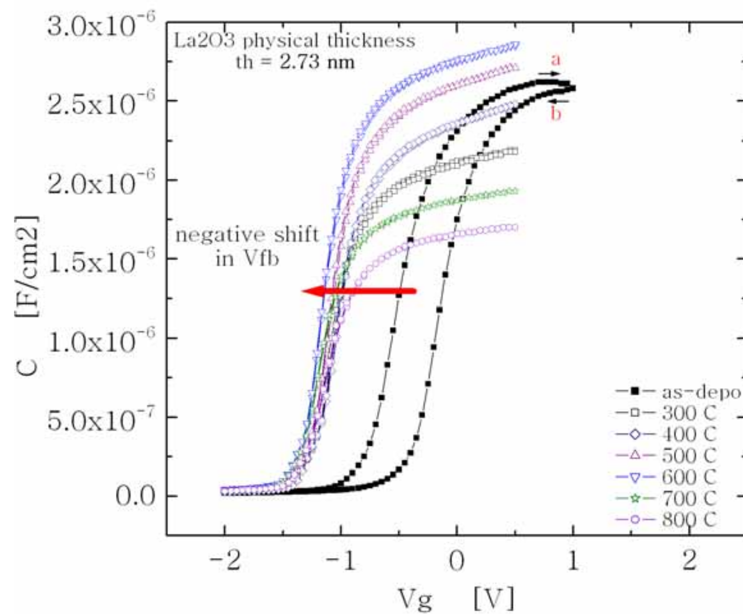


Fig. 3.1 C-V characteristics of Al-La_2O_3 gated MOSCAP after PDA in N_2 ambient at different temperatures (300°C– 800°C).

Fig. 3.1 shows capacitance-voltage (C-V) results for La_2O_3 capacitors before (as-depo condition) and after PDA treatment at several temperatures. The metal gate used was aluminum. The as-depo condition shows a huge hysteresis after a double-sweeping capacitance measurement. La_2O_3 after PDA shows a negative shift in

Vfb for all temperatures and a reduction in hysteresis. Thus, reduction in hysteresis is the main advantage of annealing as-deposited La_2O_3. On the other hand, the shift in Vfb (ΔVfb) and the reduction in accumulation capacitance Cacc at higher temperatures (T>600°C) after PDA are some issues that need to be solved since the controllability of these parameters are extremely important to predict the final electrical characteristics of La_2O_3-gated MOS devices. From fig. 3.1 we can see that after PDA with T > 600°C, the final Cacc is reduced compared to the Cacc of the as-depo condition. It is thought that changes in the physical thickness of La_2O_3 through a densification process after PDA are the main factor for changing Cacc, see fig. 3.2.

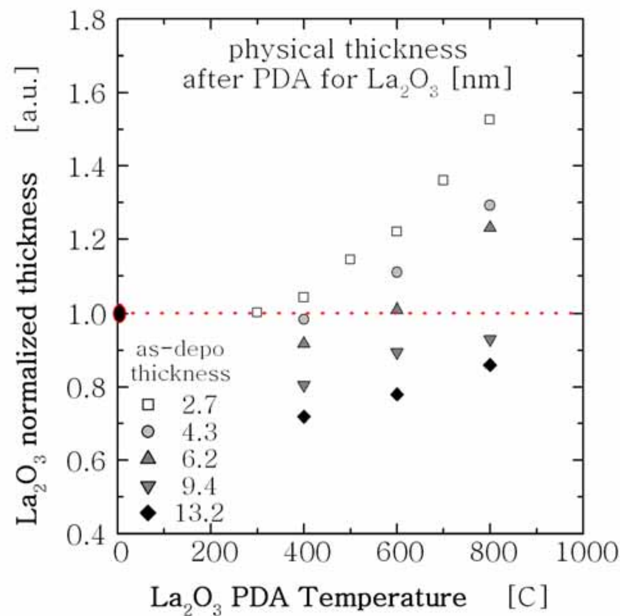


Fig. 3.2 Changes in physical thickness for La_2O_3 after several PDA temperatures.

From fig. 3.2 we can see that the physical thickness for thinner La_2O_3 films after higher PDA temperatures tends to increase as compared to thicker La_2O_3 films. A 6.2 nm thick La_2O_3 film shows both decrease and increase in its physical thickness and

this change occurs at a temperature of 600°C. It is thought that a densification process takes place in order to decrease the final thickness of the dielectric whereas an increase in a lower-k interfacial layer (IL) occurs simultaneously and it is enhanced at higher PDA temperatures thus explaining the monotonous increase in thickness. From the literature it is well known that PDA leads to densification [1-3], decrease in leakage current [4-5], density of midgap states [6], and charge trapping [7-8]. Also, during PDA, an interfacial layer is easy to be formed at between the high-k oxide film and Si substrate in general, resulting in Equivalent Oxide Thickness (EOT) increment. To suppress the interfacial layer growth, in-situ vacuum PDA of the Lanthana films was proposed [9]. However, vacuum PDA could trigger oxygen loss in Lanthana film via oxygen desorption and reduction of La in the Lanthana-layer [10]. Since PDA treatment can dramatically alter the final electrical characteristics of as-deposited La_2O_3, we also compared the results of post-metallization annealing (PMA) treated La_2O_3, where the thermal treatment is done after the metallization step.

3.3 Influence of post-metallization annealing (PMA)

The introduction of thermal treatment after the deposition of the metal gate electrode is able to recover the Vfb shift generated during PDA treatment as illustrated in fig. 3.3. The sample for this figure is a W- La_2O_3 gated MOSCAP. Here we can see that PMA sample can recover Vfb shift to positive side as compared to PDA treatment, where Vfb is shifted to the opposite side with respect to the as-depo La_2O_3. The shift in Vfb after PDA or PMA can be related to the creation and compensation of opposite

fixed charge inside the dielectric or at its interfaces, development of both top and bottom interfacial layers with respect to La_2O_3, increase of oxygen losses during the annealing, etc. All these issues will be discussed in detail further in this chapter.

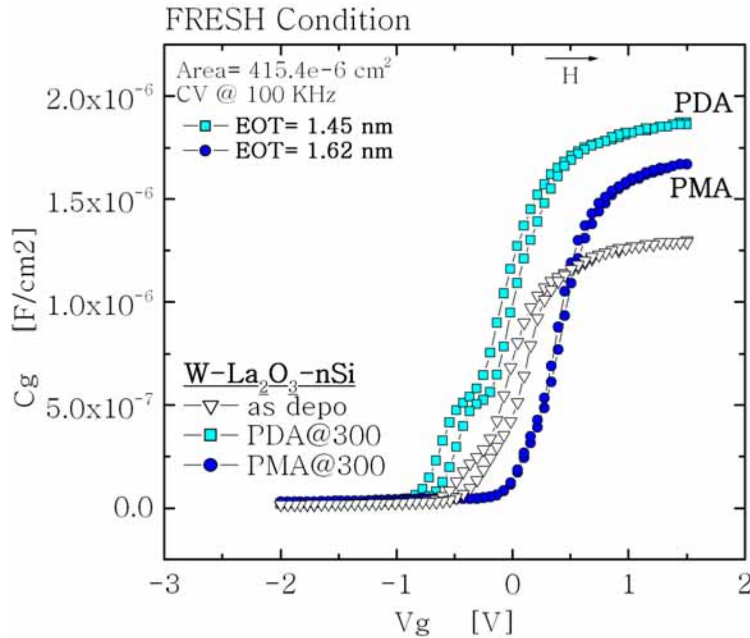


Fig. 3.3 W-La_2O_3 gated MOSCAP before and after thermal treatment in N_2 ambient at 300°C. PDA and PMA thermal treatments are both compared to the as-depo condition.

It is important to note that an aluminum-gated La_2O_3 MOSCAP will develop an alumina-based interfacial layer after PMA, and this IL is located at the interface between La_2O_3 and Al. Because of this lower-k IL development, the scaling of EOT towards sub 1nm is quite limited with this Al- La_2O_3 stacked material. The evidence for this lowest-k IL is shown after imaging the gate section of a MOSCAP with this Al-La_2O_3 stack by transmission electron microscopy, see fig. 3.4 [11]. Because of the Al_2O_3-based IL developed after PMA, the reduction in Cacc after even low-temperature PMA treatments will prevent this stacked structure to be used for scaled down devices below EOT < 1 nm.

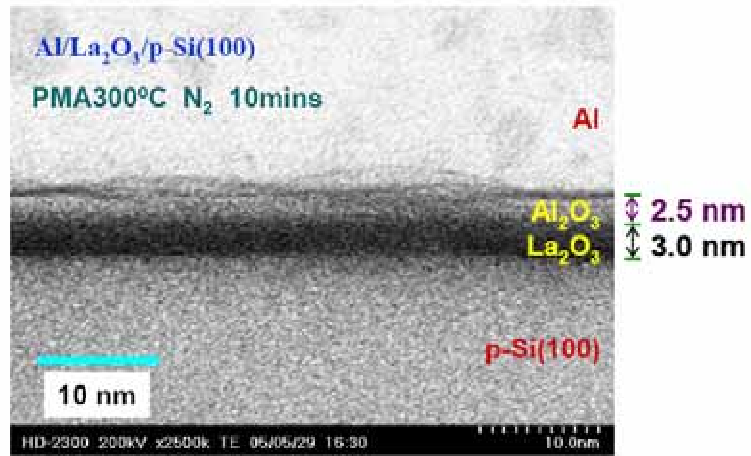


Fig. 3.4 TEM of an aluminum-gated La_2O_3 MOSCAP after PMA in N_2 at 300°C (10 min.). The existence of a low-k Al_2O_3-based IL at the Al–La_2O_3 interface is shown, after Ng [11].

This is why the use of metal gate materials with a less reactive nature to La_2O_3 during PMA is necessary in order to minimize the development of lower-k IL during the annealing. TEM images of W-gated La_2O_3 before and after PMA treatment are shown in figs. 3.5-3.6 for comparison. .

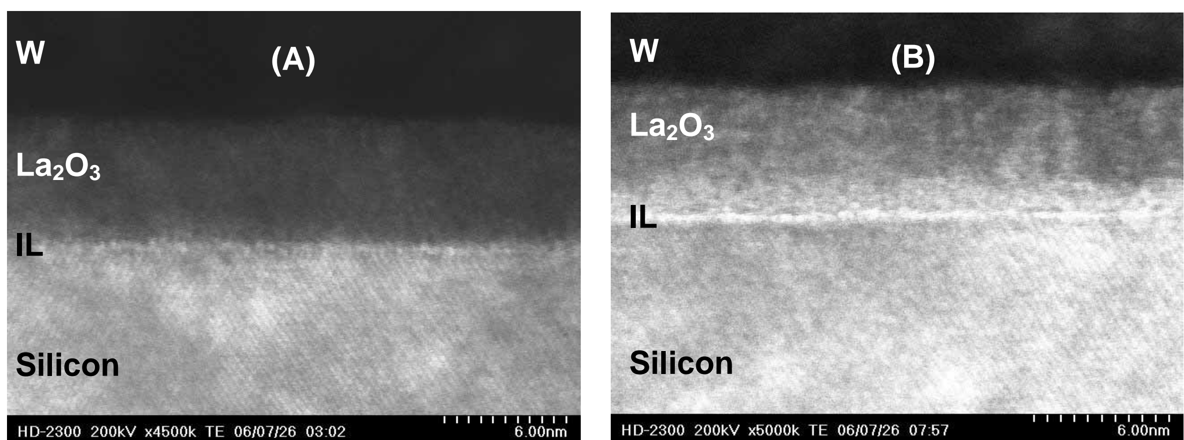


Fig. 3.5 (A) TEM of W-La_2O_3 without O_2 flow during deposition (as-depo).
(B) TEM of W-La_2O_3 **with O_2 flow** during deposition (as-depo).

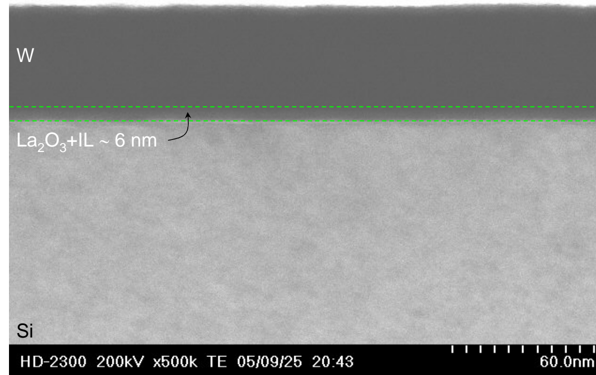


Fig. 3.6 TEM of W-La_2O_3 without O_2 flow during deposition (PMA).

As seen in fig. 3.3, the use of tungsten as the gate electrode not only prevents the reduction in Cacc after PMA, but also compensates the shift in Vfb and decreases the hysteresis generated during the PDA treatment.

3.4 Evaluation of the metal gate electrode material

Fig. 3.7 shows the C-V characteristics of La_2O_3 (different physical thicknesses) with different metals used as gate electrodes. The annealing conditions for all of these samples are described in the left side of fig. 3.7. We can see that ruthenium (Ru) is able to produce the biggest increase in Cacc after annealing, which consequently results in a very low EOT<1 nm. However, Ru-gated La_2O_3 MOSCAP showed a lot of variations in their electrical characteristics as shown in fig. 3.8 and 3.9.

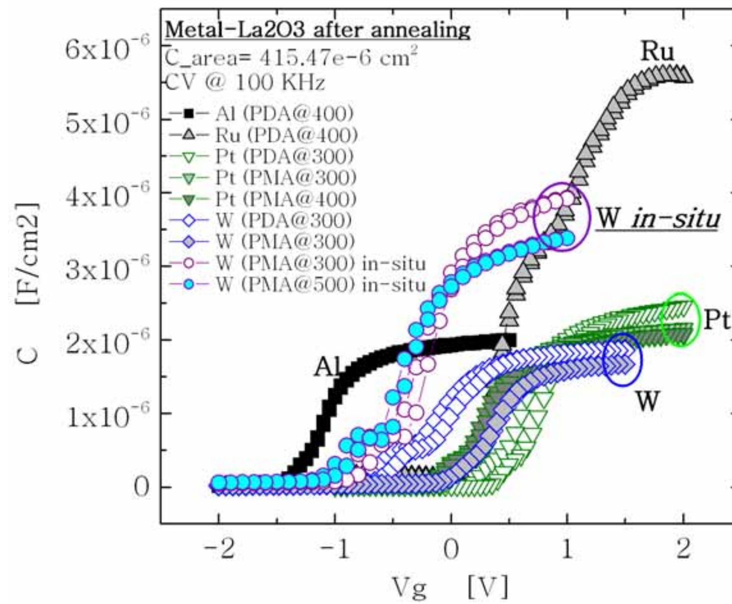


Fig. 3.7 C-V characteristics of La_2O_3 gated with different gate metals.

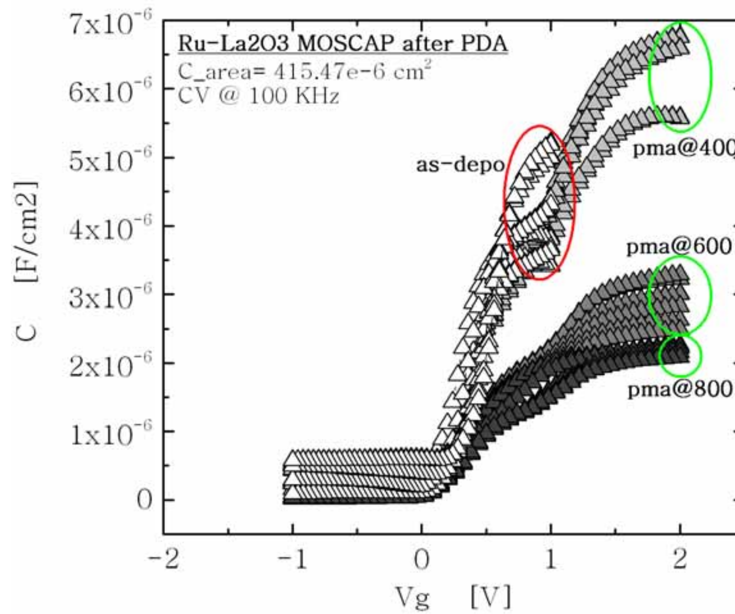


Fig. 3.8 C-V characteristics of Ru-gated La_2O_3 before and after PDA at different temperatures. The large variations between samples exist even for the PDA@800°C samples.

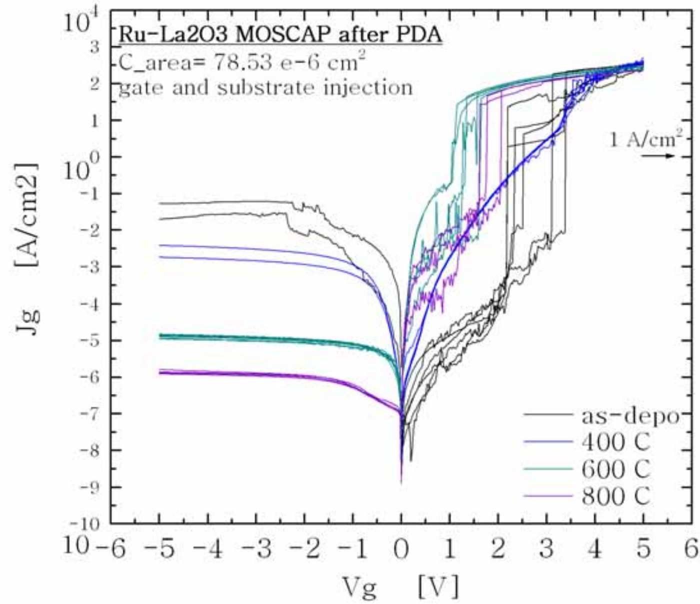


Fig. 3.9 J-V characteristics of Ru-gated La_2O_3 before and after PDA at different temperatures. It is clearly seen that there is almost no reproducibility in Jg even for the same sample.

By using Ru as the metal gate electrode, La_2O_3-gated MOSCAP showed a lot of variations in Cacc and Vfb values as well. Even after PDA, these irreproducibilities could not be minimized as shown by the variations on Vfb for the sample annealed with the highest PDA temperature. Fig. 3.9 shows the J-V characteristics of Ru-gated La_2O_3 before and after PDA treatment. The large variations and lack of reproducibility in gate leakage current density Jg for these samples avoid the implementation of Ru as the metal gate electrode for La_2O_3. Besides, because of the deposition technique used for this metal (rf sputtering at room temperature), it is expected that La_2O_3 will present large amounts of plasma damage-induced traps which could only be minimized after PMA treatment.

The use of platinum (Pt) electrode above La_2O_3 also showed large variations in Vfb and Cacc before and after PDA as well (not shown here), so that its implementation as the gate electrode for La_2O_3 could not be carried out at this stage. We also investigated Ta as the gate electrode for La_2O_3 and this metal was directly deposited on the oxide by rf sputtering at room temperature. We found, however, that by depositing this metal directly on La_2O_3 at room temperature, the thickness uniformity of the deposited TaN film was not directly controlled by the time or any condition of the sputtering process (rf power, pressure). Since Ta was deposited at room temperature (with fixed rf power and pressure), there were many variations in thickness along the MOSCAP area so that non-reproducible electrical characteristics were always obtained. It is interesting to observe that by increasing the temperature used during the sputtering process of the metal under evaluation, we could improve the thickness uniformity of the whole stack. Nonetheless, this increase in temperature during the sputtering of the metal (time where the La_2O_3 surface is directly exposed to the ambient within the sputtering deposition chamber) would lead to an undesirable PDA annealing of the stack and thus, variations in the final electrical characteristics of the devices.

On the other hand, being Ru a metal with a higher work function compared to Al, it is expected that a reduction in leakage current will be obtained at least during gate injection conditions because of the higher barrier for electrons, see fig. 3.10. From fig. 3.10 and for the same La_2O_3 film thickness, we can observe the reduction in leakage current density Jg (gate injection) just by changing the metal electrode from low to a high work function metal material.

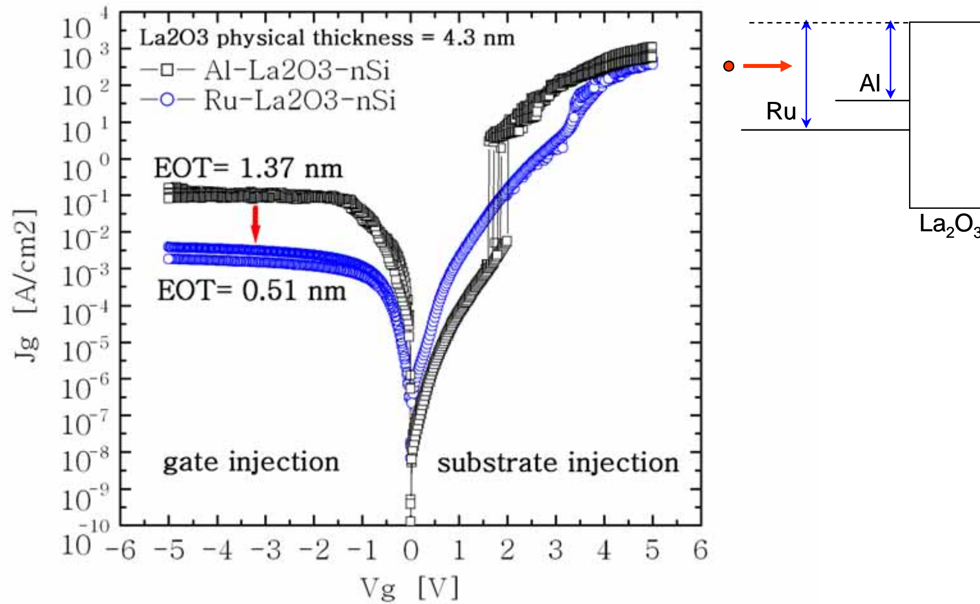


Fig. 3.10 J-V characteristics of Al and Ru-gated La_2O_3 after PDA in N_2 at 400°C. The use of a higher work function metal leads to a reduced density of leakage current (gate injection). The inset shows the difference in barrier height for electrons during gate injection.

Besides, compared to Al, Ru has a higher enthalpy for chemical bond formation with oxygen (see table 1.2). This is a great advantage since the formation of a lower-k IL at the interface between La_2O_3 and the metal would make more difficult to use this high-k material for devices purposed to be scaled down to EOT < 1 nm. The use of inert metal electrodes for the gate of high-k MOS devices has a great potential to further scale down the EOT of these devices. In fig. 3.10 and for the same La_2O_3 physical thickness (measured by spectroscopic ellipsometry during the as-depo condition), EOT > 1nm is obtained by using Al whereas EOT < 1 nm is obtained by using Ru as the gate electrodes. Fig. 3.11 shows other potential metal gate electrode candidates in conjunction with the ones we already presented. Here, La_2O_3 with

different physical thicknesses were used for these samples so that the C-V data is presented only for comparison purposes.

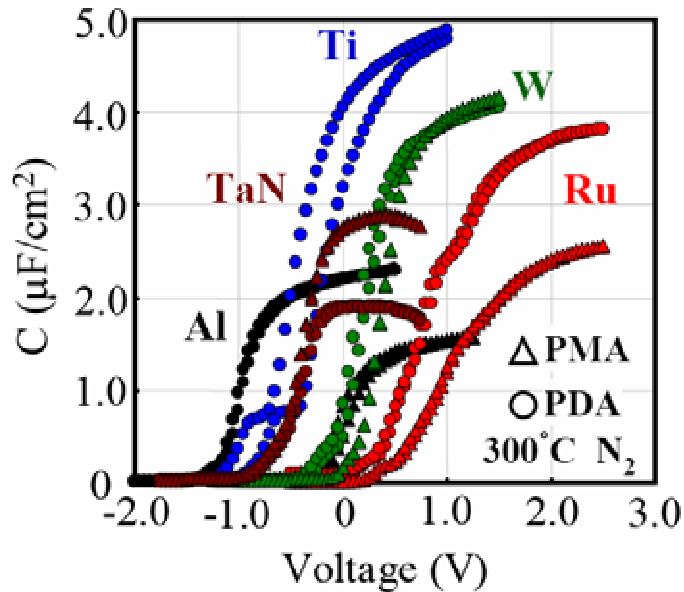


Fig. 3.11 C-V characteristics of metal–La_2O_3 after PDA/PMA in N_2. Even though lower EOT can be achieved with other metals, W gets the more stable and reproducible characteristics.

From fig. 3.11 we can observe a wide variation in the final electrical characteristics of La_2O_3 when gated with a specific metal gate electrode. One of the most important parameters obtained when gating La_2O_3 with a specific metal is the flat-band voltage Vfb. Because different metals (with different work functions) are expected to be used for both n and p-channel MOSFETs, the search for a metal able to produce a low threshold voltage Vth for both types of MOSFETs is desirable. In literature [12], extensive simulations have shown that the optimal gate work functions for the sub-50 nm channel lengths should be 0.2 eV below (above) the conduction (valence) band edge of silicon for n-type MOSFETs (p-type MOSFETs). In this respect,

W is considered as a mid-gap-metal gate electrode able to produce normally-off n and p-channel MOSFETs with low enough threshold voltages. Nevertheless, a dual-metal gate electrode technology is needed to further reduce the Vth for these surface-channel MOSFETs. On the other hand, the hysteresis and variations in Vfb after the first stressing measurements are quite important to determine the reliability characteristics of metal-gated La_2O_3. These reliability results for La_2O_3-gated MOSFETs will be presented in chapter 4. Now, from the viewpoint of process integration, the use of inert materials as the gate electrode for high-k gated devices imposes a big challenge related to the etching of this metal for the definition of the gate area patterns. This analysis, however, is beyond the scope of this dissertation but it is a research topic that needs to be further investigated.

3.5 C-V and I-V characterization

In this section, we will present the C-V and I-V electrical results before any electrical stress was applied to La_2O_3-gated MOSCAP. This condition is defined as the "fresh condition". Fig. 3.12 shows the electrical characterization of Al-gated La_2O_3 before and after PDA annealing in N_2 at different temperatures. From both figures we can see that La_2O_3 without annealing will present too bad electrical characteristics which make it unable for use in MOS devices. From the C-V data, La_2O_3 without annealing presents a large degree of hysteresis and poor insulation properties are observed from the J-V characteristics for this sample. After PDA, the hysteresis is minimized and better insulation characteristics are obtained as observed by the

reduction in gate leakage current for the annealed samples.

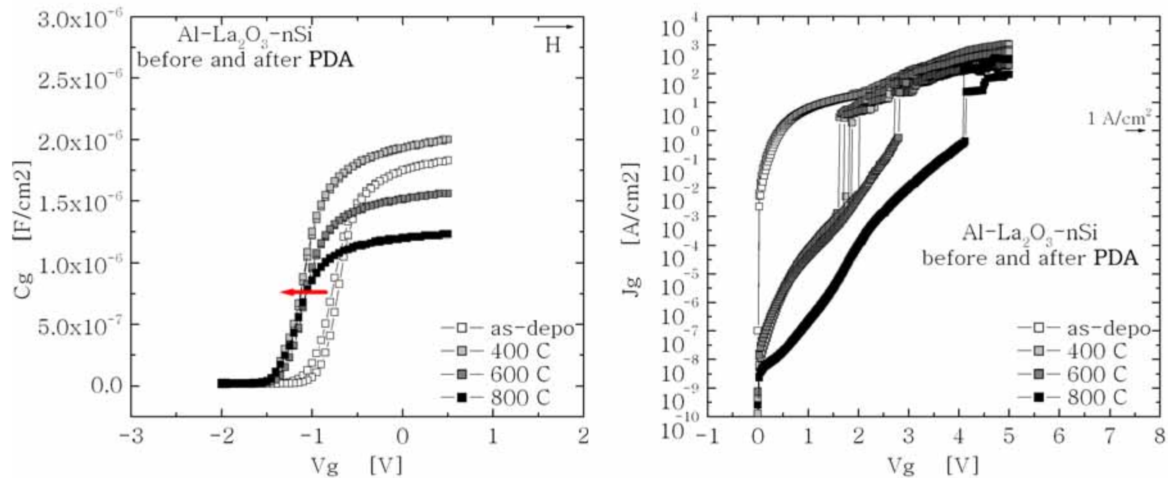


Fig. 3.12 C-V and I-V characteristics of Al–La_2O_3 before and after PDA in N_2.

The highly conductive nature of La_2O_3 without annealing is quite characteristic of an oxide with extrinsic breakdown features (the highly conductive state caused by extrinsic bulk and interfacial defects rather than to intrinsic properties of La_2O_3). Fig. 3.13A shows the variation in some of the parameters for this Al-gated La_2O_3 MOSCAP and fig. 3.13B plots the leakage current density Jg versus EOT for these samples as well. From fig. 3.13A it is clearly seen that the increase in EOT after PDA is directly correlated to the increase in the physical thickness of the stack. This is related to the development and continuous increase in the physical thickness of a lower-k interfacial layer IL (at the interface between La_2O_3 and silicon) and which worsens at higher PDA temperatures. Since the use of Al as the gate electrode makes it difficult to obtain devices with EOT < 1 nm, even by using relatively thin La_2O_3 films (4.3 nm for the present sample) the final EOT after PDA was always greater than 1 nm.

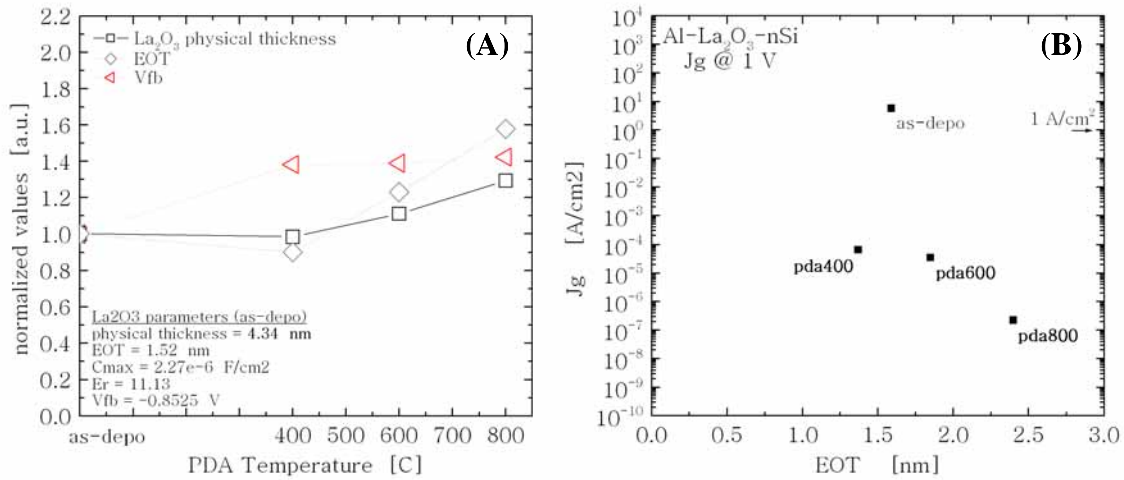


Fig. 3.13 (A) Variation of some physical and electrical characteristics of Al–La_2O_3 stacked structure before and after PDA in N_2.
(B) Jg-EOT plot for the same Al–La_2O_3 stacked structure.

The use of n and p-type silicon substrates for the evaluation of both substrate and gate injection of carriers respectively, was carried out and these results are shown next.

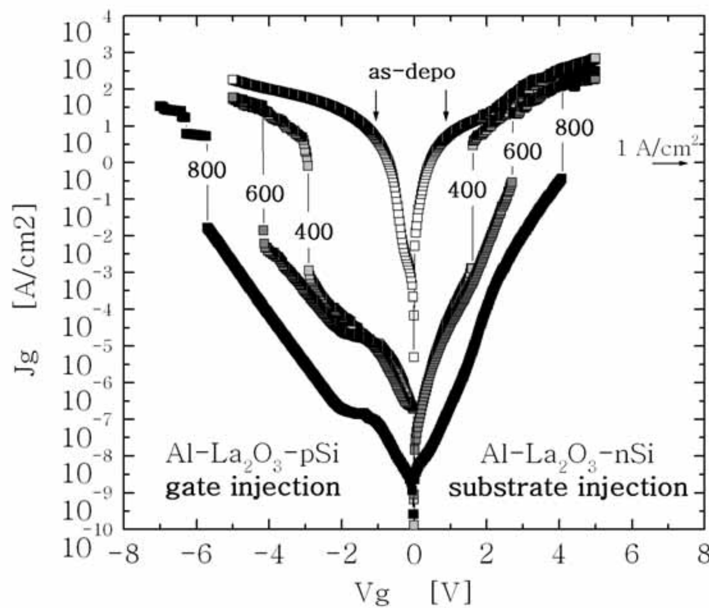


Fig. 3.14 J-V characteristics for Al-gated La_2O_3 stacked on p and n-type silicon. La_2O_3 physical thickness ~ 4.3 nm for as-depo condition on both Si substrates.

From fig. 3.14, the gate leakage current levels and the distribution of the breakdown voltages for La_2O_3 deposited on p and n type silicon substrates shows an asymmetry in their respective values. When several samples with the same PDA condition were stressed, a more smooth distribution of the TZDB voltages was found for La_2O_3 deposited on n-Si substrate (only one sample for each PDA condition is shown) so that the voltage at which breakdown was reached (Vbd), was closely distributed at almost the same gate voltage. Interestingly, the asymmetry in the gate current density levels with respect to the injection polarity can be partially explained by the difference in barrier heights of the different silicon substrates and Al. For Al-La_2O_3 stacked on n-type Si substrates, higher levels of leakage current as well as lower TZDB voltages are found, so that by increasing the quality of La_2O_3 films deposited on n-type silicon substrates (reducing Jg and increasing breakdown voltages) it is expected that the quality of the metal- La_2O_3 stacked on p-type silicon substrates will increase as well.

By resuming and comparing the C-V and I-V electrical characteristics of most of the fabricated samples we can obtain the leakage current density Jg versus Equivalent Oxide Thickness EOT or so called Jg vs. EOT plot as shown in fig. 3.15. The leakage current density shown for all the samples was taken at the gate voltage of + 1 V for La_2O_3 on n-type silicon and – 1 V for La_2O_3 on p-type silicon substrates respectively. The EOT values were obtained after simulation of the C-V data by using the CVC NCSU Software [13], which takes into account the quantum mechanical correction for very thin La_2O_3 films.

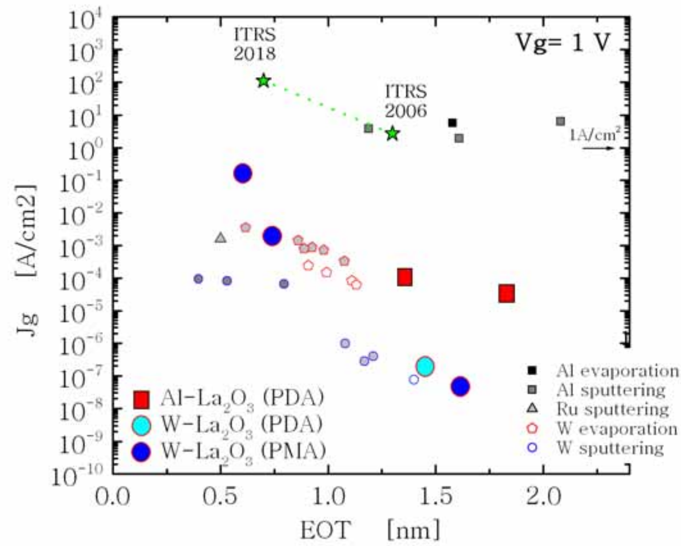


Fig. 3.15 Jg-EOT plot for some of the Metal-La_2O_3 stacked MOS structures evaluated in this dissertation. Jg is taken at |1V|.

From fig. 3.15 it is seen that depending on the metal used as the gate electrode, La_2O_3 will present variations in the final level of leakage current density Jg even for the same EOT. For instance, at EOT ~ 1.5 nm, Al-gated La_2O_3 produces a higher Jg by almost 3 orders of magnitude compared to a W-gated La_2O_3. Since an Al-gated La_2O_3 will develop a lower-k IL at the Al-La_2O_3 interface, the use of this metal with even thinner La_2O_3 films imposes a limitation towards obtaining La_2O_3-gated devices with EOT < 1nm. By using tungsten, which is a material highly valued because of its highly inert properties (resistance to oxidation even during high temperature conditions), obtaining MOS devices with EOT < 1nm can be guaranteed. The limit imposed by ITRS on the Jg and EOT parameters for MOS devices is seen as the two topmost data points of the graph. Because of the La_2O_3 high dielectric constant, devices gated with relatively thick La_2O_3 films can produce low EOT levels together with low Jg and which lie below the limits imposed by ITRS (Low Operation Logic LOP) thus

demonstrating the high potential of La_2O_3 as a candidate to replace conventional SiO_2 as the gate oxide for future generation devices.

The next section will present and discuss the reliability characteristics of Metal- La_2O_3 stacked MOSCAP devices as submitted to their respective journals. In the first paper, entitled *"Breakdown and Reliability of Metal Gate– La_2O_3 Thin Films after Post-Deposition Annealing in N_2"*, the reliability characteristics of Al and W-gated La_2O_3 before and after PDA annealing are presented. The second paper, *"Charge Trapping Characteristics of W-La_2O_3-nSi MIS Capacitors After Post Metallization Annealing in N_2"*, presents the results of only W-gated La_2O_3 MOSCAP after PMA for thick and thin La_2O_3 films (EOT>1nm and EOT<1nm respectively). Finally a third paper, *"Degradation and breakdown of W-La_2O_3 stack after post metallization annealing in N_2"* reviews the degradation mechanism for La_2O_3 with respect to the severity of the applied stress and proposes a very simple degradation mechanism able to explain the results shown in there. The figures' numeration for the following subchapters 3.6–3.8 will be shown as presented during the submission of these papers to their respective journals.

3.6 Breakdown and reliability of metal gate–La_2O_3 thin films after post-deposition annealing in N_2

With the continuous scaling down of the CMOS technology, the research of ultra thin gate oxide films with higher dielectric constant has been greatly advanced. The main motivation behind the use of high dielectric constant materials for the gate of MOS transistors is the lower gate leakage current density levels that can be obtained by using thicker oxide films without compromising their final EOT values. However, the list of viable candidates for the long-term replacement of SiO_2 shrinks when the k value and the bandgap energy of these materials are both considered. Figure 1 shows that there is an inversely proportional relationship between the dielectric constant and the bandgap energy for some of the most important high-k gate oxides under research (2-4). From figure 1, we can see for instance that materials like ZrO_2 and HfO_2 have a large k = 25 but they also have small band offsets for electrons and holes when these materials came into contact with silicon. A material like Al_2O_3 has larger band offsets for both carriers but its small value of k = 9.0 make it unable to replace SiO_2 in the long term. In the case of La_2O_3, the band offsets for electron and holes are large enough so that low levels of leakage currents by both carriers can be expected. Besides, the k value of La_2O_3 is big enough so that lower EOT levels can be guaranteed for relatively thick films. On the other hand, the gate poly-depletion effect represents a serious concern that can lower the final capacitance of the gate stack; this can be overcome by using metal-based gate electrodes. For all these reasons, metal/high-k gate stacks are now becoming important issues to be addressed. In this paper, we

evaluate the reliability characteristics of metal/high-k gate stacks in order to determine their electrical evolution before breakdown and their integrity during electrical stress conditions.

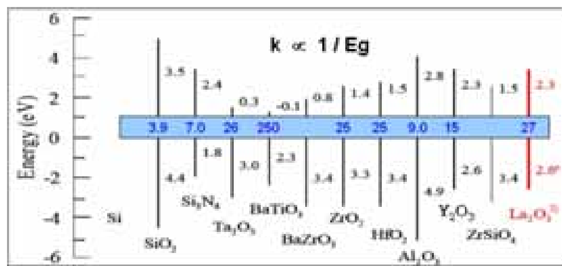


Fig. 1 Permittivity and band offset values for SiO_2 and different high-k materials on silicon (2-4).

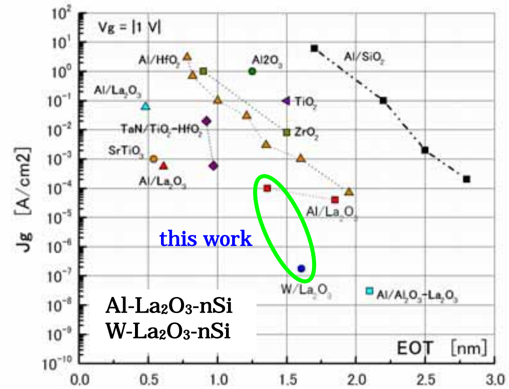


Fig. 2 Jg-EOT for metal/high-k materials (5-9).

Thin films of La_2O_3 with physical thickness= 4.3 nm and 9.1 nm (after PDA) were deposited on H-terminated n-type silicon substrates by electron-beam evaporation using MBE system (ANELVA I) at 250°C. The pressure in the chamber during the deposition was around 1x10-9 Torr with rate of 0.5nm/min. PDA thermal treatments were carried out in N_2 ambient at 400°C and 300°C for 5min by Rapid Thermal Annealing (ULVAC-MILA 3000) system for the 4.3nm and 9.1nm La_2O_3 films respectively. Shortly after the La_2O_3 deposition and PDA treatment, the metal gate electrodes were immediately deposited by using a metal shadow mask. 2 different metals for the gate were used. Al=150nm and W=50nm metal thin films were deposited by thermal evaporation and RF magnetron sputtering respectively. The experimental procedure is all resumed in figure 3. C-V, I-V and Time Dependent Dielectric Breakdown (TDDB) electrical characteristics were obtained using a

precision LCR meter (HP 4284A) and SPA (HP 4156C) respectively.

Figure 2 shows the Jg-EOT characteristics of several metal/high-k gate stacks (5-9). We can observe that for an EOT ～ 1.5 nm, the level of gate current density Jg decreases for almost 3 orders of magnitude by using W-gated La_2O_3 instead of aluminum as the gate electrode. Here, we must state that the physical thickness of La_2O_3 below the tungsten electrode is almost twice the thickness of La_2O_3 below the aluminum electrode (La_2O_3 th_{phys}= 4.3nm, 9.1nm for Al and W-based gate electrodes respectively). In this way, the Jg level can be greatly reduced in the W-La_2O_3 stack thanks to a thicker oxide film with the added advantage of keeping a low EOT. From C-V measurements for both Al-La_2O_3-nSi and W-La_2O_3-nSi systems, EOT = 1.4nm and 1.6nm were respectively estimated, see figure 4. This figure shows that even when the physical thickness of La_2O_3 below the aluminum electrode is almost 2 times thinner than the physical thickness used for the W-gated capacitor, the capacitance in accumulation for the later structure is higher. Two different values of k for La_2O_3 were found from these C-V curves after taking into account the quantum mechanical correction (10).

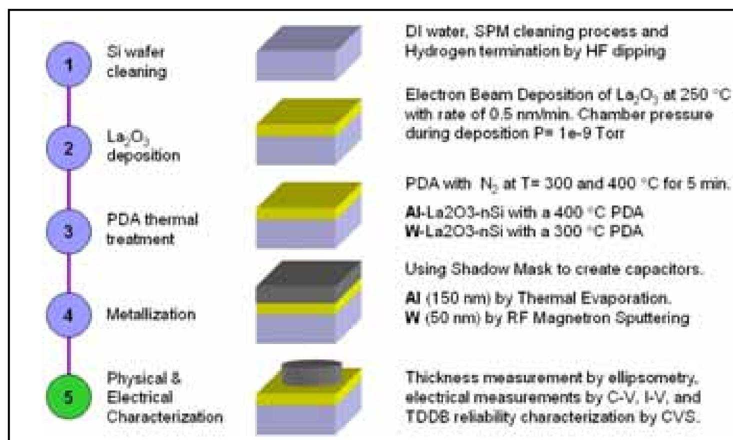


Fig. 3 Process flow for La_2O_3-based MIS structures.

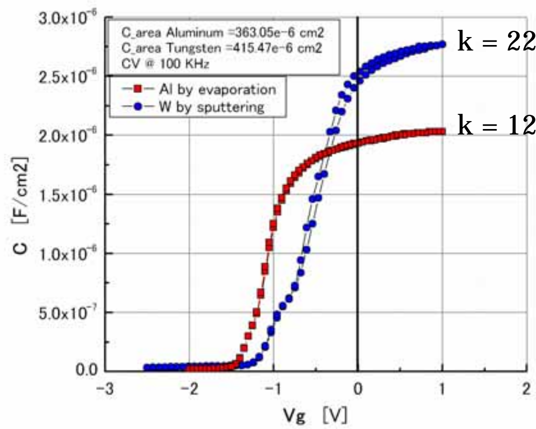


Fig. 4 C-V characteristics of Al-La_2O_3-nSi and W-La_2O_3-nSi gate stack structures.

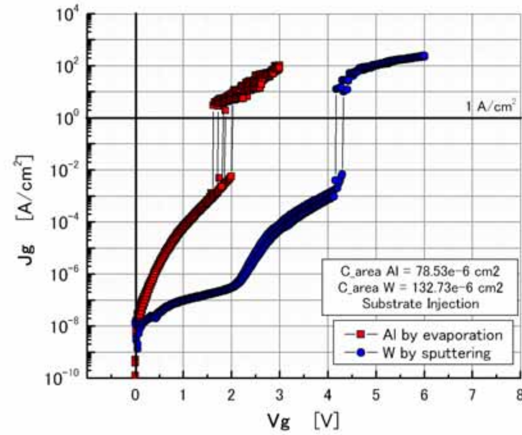


Fig. 5 J-V characteristics of Al-La_2O_3-nSi and W-La_2O_3-nSi gate stack structures.

A relatively low k = 12 was found for the Al-gated La_2O_3 capacitor, whereas a larger k = 22 was found by using W as the gate electrode. These differences in the k value were attributed to the presence of an extra interfacial layer formed between the aluminum electrode and the La_2O_3 film. It is well known the easy with which aluminum oxidizes when in contact to any source of oxygen (11). The oxidation of Al by oxygen taken directly from the La_2O_3 film could be enhanced by temperature during the thermal evaporation of this metal so that a relatively low k interfacial oxide is created. This undesired effect is able to increase the devices' EOT and it gets worse after post-metallization annealing of the Al-La_2O_3 stack (12). Then, by having this Al_2O_3-based interfacial layer in addition to the unavoidable SiO_2-based interfacial layer, the final k of the oxide stack lowers dramatically. In the case of a W-gated La_2O_3 stack, the final EOT obtained is very close to that of 27 reported for La_2O_3 (13). We can also observe a difference in the flat band voltage Vfb for both systems due to different work functions WF for the gate electrodes, being WF = 4.1 and 4.7 eV for Al and W respectively (14). This is why the Vfb for the W-La_2O_3 system gets closer to 0 V.

Ideally, the Vfb of Al-oxide-nSi stack should be close to 0 V but when a high density of positive charge is present in the oxide (a likely situation for our C-V curve in figure 4), the Vfb then shifts to more negative values as a consequence of large amounts of oxygen vacancies or the presence of hydroxyl group $(OH)^{-1}$ ions in $(O_2)^{-2}$ sites (15). Now, because the deposition of the tungsten electrode was done by RF magnetron sputtering method, plasma-related damage caused during the sputtering of this metal was induced in the MOS capacitor and this can be observed in the distortion caused to its C-V curve at the lowest part of the depletion regime. In resume, we have a lower k value for the Al-La_2O_3 stack caused by the probable oxidation of aluminum at the interface and on the other hand, higher k values for W-La2O3 stack at the expense of higher levels of damage by the sputtering of the metal (which can increase the density of traps in the oxide). With all this in mind, the reliability characteristics of both systems, especially the degradation of their electrical characteristics during conditions of electrical stress must be asserted. Figure 5 shows the J-V characteristics for Al-La_2O_3 and W-La_2O_3 stacks in which the gate voltage increases until the oxide breaks down. As expected, the gate current density before breakdown was larger for the thinner film because of a large contribution of Direct-Tunneling leakage current. For the thicker film, at least two different carrier conduction mechanisms can be directly observed. Also, the breakdown strength Ebd of La_2O_3 is obtained from this “time to zero breakdown” measurement. An Ebd = 4.3 MV/cm was found for both Al and W-gated La_2O_3, which is in agreement with the value reported for La_2O_3 in the literature (16). The conduction mechanism just before breakdown was also investigated and in the case of both films, Fowler-Nordheim (F-N) conduction mechanism was detected after plotting the same data of figure 5 by using an F-N plot, see figures 6-7.

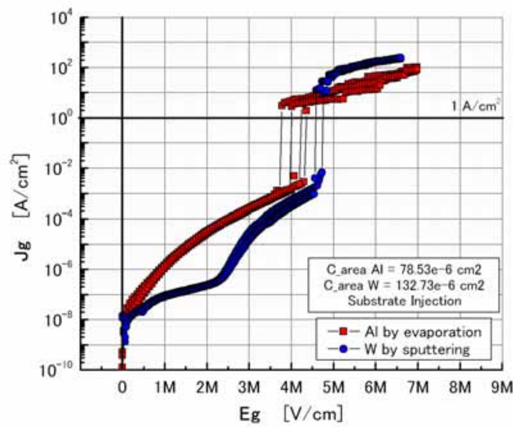


Fig 6 J-E characteristics of Al-La_2O_3-nSi and W-La_2O_3-nSi gate stack structures.

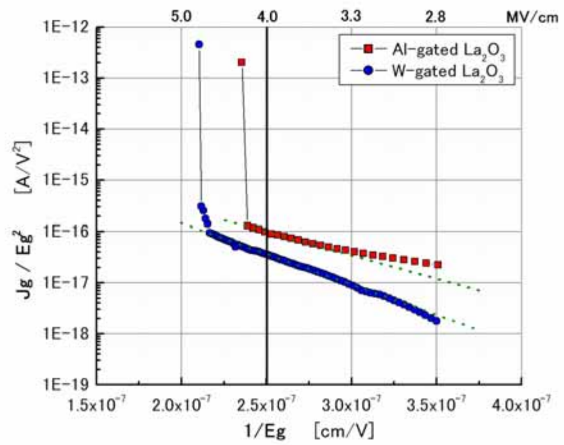


Fig 7 F-N plot of Metal-gated La_2O_3 on Si.

The breakdown strength of La_2O_3 is shown in Figure 6 for both gate electrodes. Figure 7 shows the F-N plot of the former J-V data for a limited interval of the electric field. We can see that the Al-gated La_2O_3 stack shows F-N conduction just before breakdown and this is only for the higher range of the electric field applied. We also observed a deviation from the F-N conduction regime at lower electric fields, which can be thought as a larger contribution to the leakage current coming from the Direct-Tunneling (D-T) regime for thinner films. The thicker La_2O_3 film (which is gated with tungsten) shows purely F-N conduction for the whole range of electric field shown in figure 7. In any case, the high electric field applied to the MOS capacitors triggers the trapping of charge that comes from F-N conduction until the oxides reach breakdown. Figure 8 indicates that a SiO_2-based interfacial layer IL at the La_2O_3-nSi interface is present because of nonzero intercept. The physical thickness for this IL is about th= 0.3 nm. With this information, we can now depict a clearer image of the gate stack for both Al-La_2O_3-nSi and W- La_2O_3-nSi systems, see figure 9.

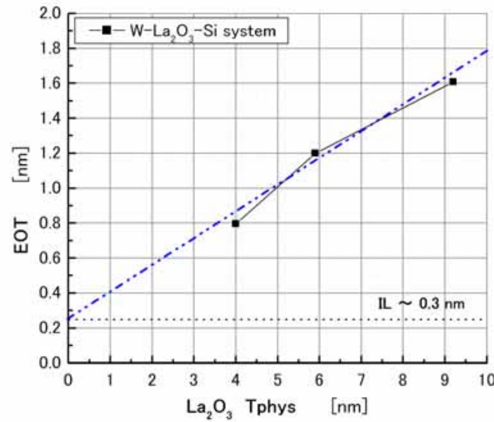


Fig 8 SiO_2-based IL estimation after PDA.

One important difference for these proposed stacks is that for the Al-gated capacitor, there must be an extra IL which comes after the oxidation of aluminum during its deposition on La_2O_3 (reaction that could possibly be triggered or enhanced during the thermal evaporation of this gate electrode). Tungsten has a larger bond enthalpy to oxygen compared to aluminum. Due to this higher resistance of W to form or break bonds with oxygen, and because of the deposition method used for this metal (sputtering on La_2O_3 at room temperature) we have then omitted an IL at the W-La_2O_3 interface. This does not means that the real physical structure for both systems is exactly like the presented below, but it should be close to it, and more importantly, it helps to explain the observed electrical characteristics after CVS measurements. TEM imaging, XPS analysis or any other technique able to visualize these structures could solve this question.

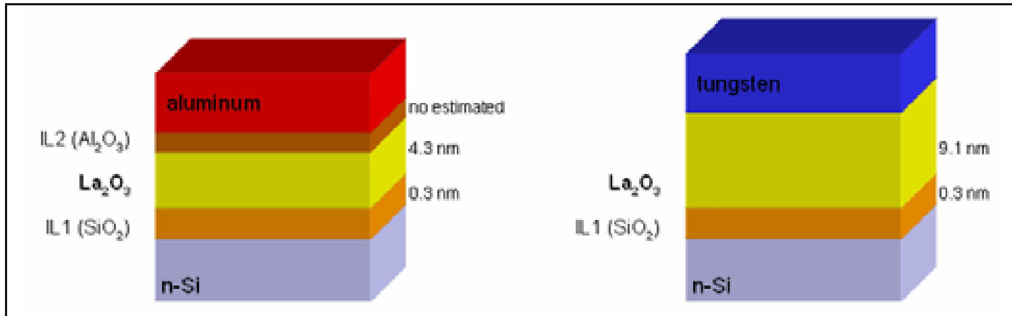


Fig 9 Schematic drawings of the proposed structural model for the Al-La_2O_3-nSi and

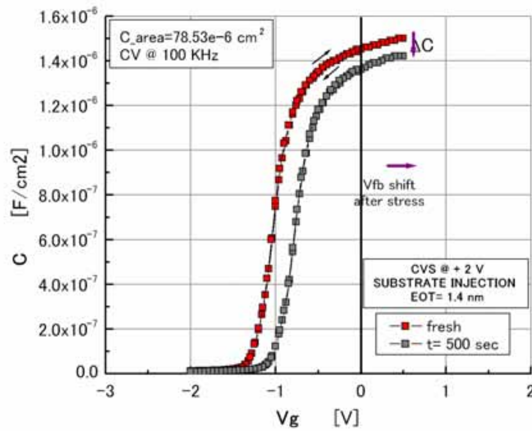


Fig 10 C-V for Al-La_2O_3-nSi stack before and after stress under substrate injection condition.

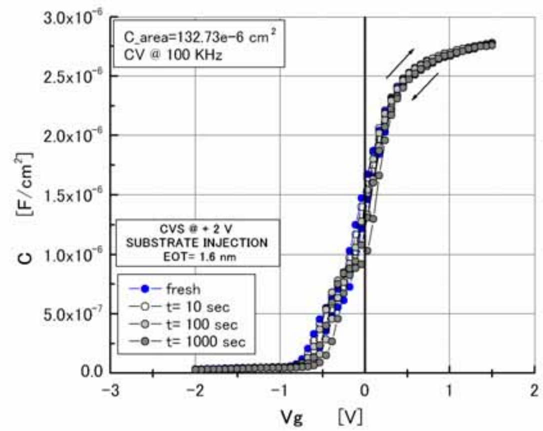


Fig 11 C-V for W-La_2O_3-nSi stack before and after stress under substrate injection condition.

Figures 10-11 show the C-V characteristics of the stack structures depicted in figure 9 before and after a CVS in the substrate injection condition. After a stress of 2V, the Al-La_2O_3-nSi stack shows a large positive flat band voltage shift ΔVfb and its capacitance in the accumulation regime Cacu decreases. The W-La_2O_3-nSi stack however, shows only a very slight change in its Vfb and almost no change in its Cacu after the same stress was applied for even longer times. By using a modified Reaction–Diffusion model (17), these changes in the CV characteristics of the Al-gated La_2O_3 system can

be explained. To better illustrate how this model works, refer to figure 12.

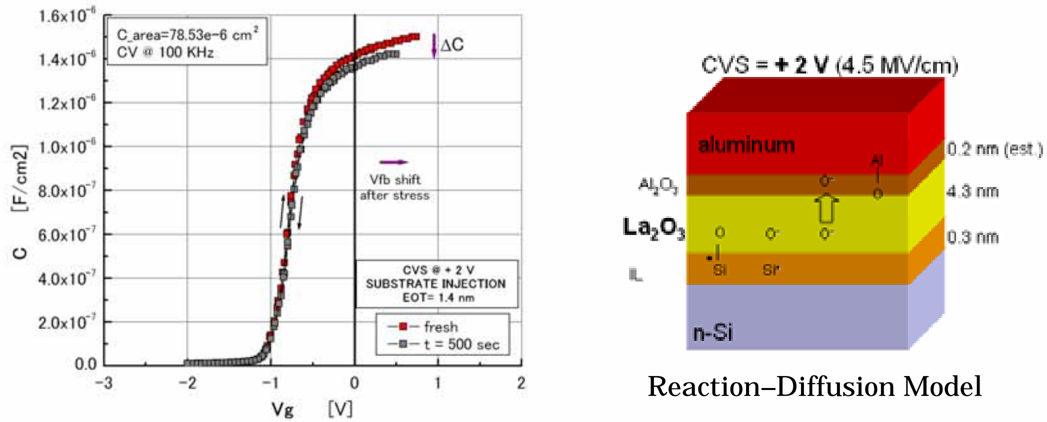


Fig 12 Shifted C-V data of figure 10 and schematic of the Reaction–Diffusion Model mechanism.

The C-V curve in figure 12 shows the same data as in figure 10 but here, the data of the fresh condition is purposely shifted towards the right side of the plot to illustrate the real reduction in Cacu after the stress. A schematic of the R-D model is also presented. The R-D model makes use of the Electric Stress–Induced Defect Generation ESIDG mechanism to explain the degradation of SiO_2 dielectrics (17). During conditions of high-electrical stress, some of the electrons coming from the silicon substrate are injected and trapped into localized states of the SiO_2–based IL (which can be generated by irregularities in the bonding network and other defects in SiO_2 like oxygen vacancies). In there, some of the trapped electrons are attached to Si–O bonds so that their binding energy weakens. The weakened Si–O bonds are easily broken into Si+ and O- species and separated under the electric field. The Si+ would accumulate in the IL layer and the O- species then diffuse/drift towards the aluminum electrode across the bulk of the La_2O_3 dielectric. The diffusion/drift of O- species

through La_2O_3 would have two important consequences: contribution to a more positive Vfb shift after stress by the filling up of some oxygen vacancies, the other would be the possible reaction occurring at the aluminum electrode which could create extra Al–O bonds so that a very thin layer of alumina–based dielectric is created. This Al_2O_3 IL formation/modification could be the reason for the final lowering of Cacu in the stack as seen in figure 12 and also could contribute to a more positive Vfb shift by the creation of some Al–O dangling bonds after the stress (18-19). In the end, the greatest contribution for this large positive Vfb shift would be the trapping of electrons within trap sites of La_2O_3 after the high electric field stress applied. Figure 13 shows the evolution with time of the gate leakage current after different CVS stresses on the substrate injection condition for Al-gated and W-gated La_2O_3 stacks.

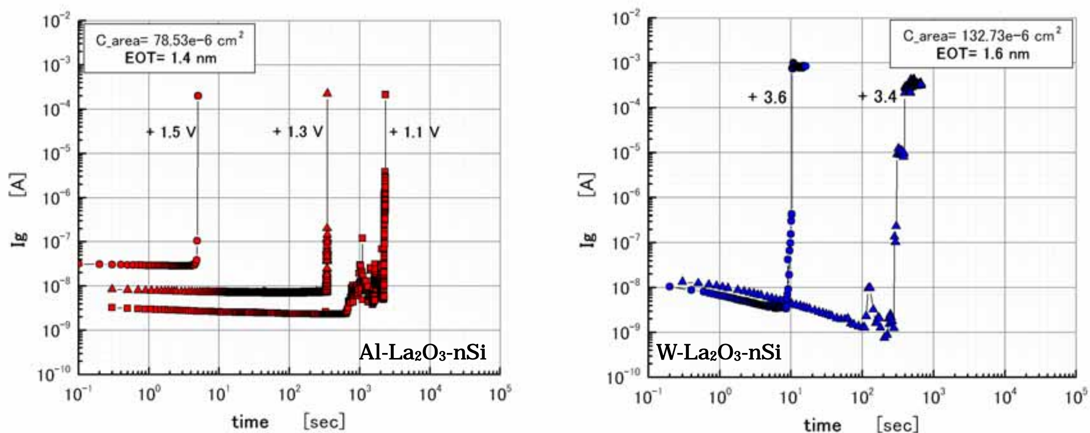


Fig 13 Gate current evolution with time after different CVS for Al-gated and W-gated La_2O_3.

From figure 13 we can see at least two important characteristics coming out from these TDDB measurements. First, both stacks show that their initial levels of gate

leakage current are proportional to the CVS applied and so is the time required for these samples to reach breakdown. For instance, the Al-gated La_2O_3 structure shows that for the lowest stress applied, a lower initial gate leakage current level is obtained so that a longer time to breakdown develops. By applying a higher CVS, the leakage current increases and the time to breakdown shortens as expected. On the other hand, the initial levels of leakage current for the Al-La_2O_3-nSi stack are kept almost without change until the samples reach breakdown. There is a significant difference with respect to the W-gated La_2O_3 structure, in which the initial levels of gate current decrease almost immediately after applying the CVS for a few seconds. This fast decrease in the gate current with time could be attributed to the fact whether to a lower temperature used during the PDA treatment or to plasma damage introduced during the sputtering of the metal so that a large amount of charge traps are generated. Figure 14 shows the lifetime projection for both structures after TDDB–CVS measurements and by taking into account a 63% mean time to failure.

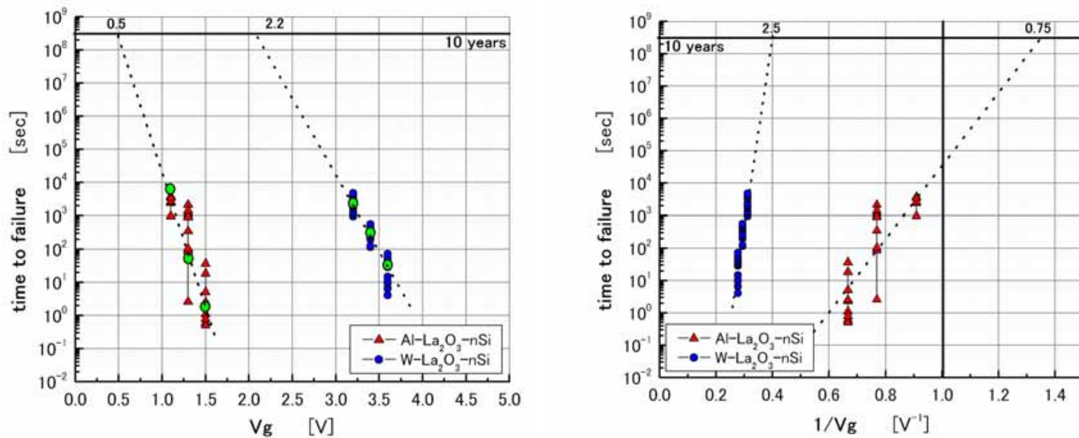


Fig 14 Linear and Reciprocal Vg models for the lifetime projection of Al-gated and W-gated La_2O_3.

In figure 14, we found that the gate voltage necessary for both stacks to last at least 10 years before breakdown occurs is around 0.6V and 2.3V for Al-gated and W-gated La_2O_3, respectively. Of course, this prediction is only a rough approximation because once the exponential law of voltage dependence reaches voltages as low as use conditions; the linear model will tend to approach a more power-law based model (20-21). In any case, a 10 years operation is guaranteed by using the very simple linear Vg or reciprocal 1/Vg models because of the high electric fields applied during the stressing of these samples. At high electric fields, the linear and reciprocal models converge and that is why both models can be used here to project at least roughly, the lifetime of La_2O_3. In the end, none of these simple extrapolation laws are exact when considering more real voltage operation conditions, i.e., by applying very low voltages for comparing long-term stress data, so that a larger set of samples would be needed for a more accurate prediction. Finally, we can see that the advantages of a W-gated La_2O_3 stack resided on the ability to produce higher k oxides and longer lifetimes before breakdown while keeping almost the same EOT value. Nonetheless, the introduction of plasma-related damage during the sputtering of this metal into La_2O_3 should be taken into consideration for the reliable operation of MOS devices and the expected improvement on the electrical characteristics of W-gated La_2O_3 stacks by introducing a post-metallization annealing PMA treatment is also necessary.

Summarizing this section, the reliability characterization of Metal-La_2O_3 thin films on silicon after the high-k Post-Deposition Annealing in N_2 was carried out. A modified Reaction-Diffusion mechanism was used to explain the small change in the CV characteristics of Al-based samples before and after stress. Diffusion/drift of

oxygen ion species within the bulk of La_2O_3 and their posterior reaction with aluminum are discussed. No change was detected for W- La_2O_3-nSi system. Because of the high electric fields applied during TDDB tests, a 10 years lifetime is guaranteed for La_2O_3 by using the linear or reciprocal model. In conclusion, for an EOT ～ 1.5 nm, a W-La_2O_3-nSi system shows better electrical characteristics and longer lifetimes before breakdown when compared to Al-La_2O_3-nSi capacitors. We need to compare Al and W-gated La_2O_3 under the same processing conditions such as PDA temperature, and we need damage removal by annealing after W electrode sputtering for the fair comparison of the lifetime. However, we can expect that W-gated La_2O_3 can produce higher lifetimes than Al at the same EOT.

3.7 Charge trapping characteristics of W-La_2O_3-nSi MOSCAP after post-metallization annealing in N_2

The main motivation behind the use of high dielectric constant materials for the gate of MOS transistors is the lower gate leakage current density levels that can be obtained by using thicker oxide films without compromising their final EOT values. In this respect, Hafnium (Hf) based family of high-k materials has received a lot of interest and has been intensively studied during the past years and it is expected to be used in production in year 2008. The immediate question then arises as to which material can be considered to replace Hf-based oxides in the future? According to the International Technology Roadmap for Semiconductors (ITRS), lanthanum oxide (La_2O_3), which is a member of rare earth-based oxides, was classified into the next group of potential candidates to succeed Hf-based oxides. Besides, the selection of the metal electrode material also plays an important role in the final electrical characteristics of the devices with high-k dielectrics since poly-Si based electrodes will not work below 1 nm EOT regime due to the gate poly-depletion effect so that introduction of suitable metal gate will be needed. Furthermore, because of the possible formation and subsequently growth of low-k interfacial layer at the metal–La_2O_3 interface after PMA even at low annealing temperature, the scaling of metal–La_2O_3 stacked structures into sub 1 nm regime is limited. Therefore, the introduction of inert gate electrodes with suitable work functions for La_2O_3-gated MOSFET devices is of the outmost importance. Tungsten-gated La_2O_3 films results in lower EOT as compared to aluminum-gated La_2O_3 so that the introduction of this metal

atop of high-k La_2O_3 film (already providing an advantage into sub 1 nm scaling) needs to be evaluated for reliability purposes. A critical parameter for gate stacks is the injection barrier which is the offset between the conduction band edges of the silicon substrate and the oxide. Fig. 1 shows a roughly inversely proportional relationship between the dielectric constant and the bandgap energy for some of the most important high-k gate oxides under research (1-3).

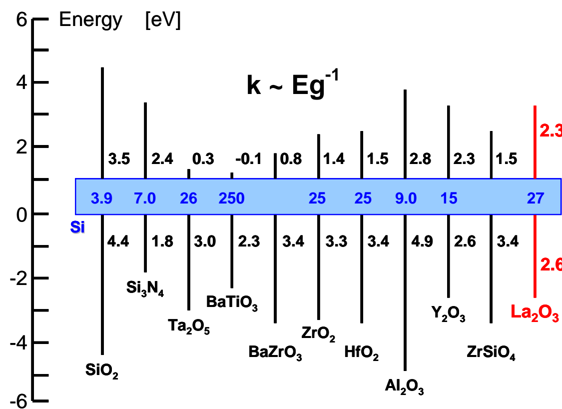


Fig 1 Permittivity and band offset values for SiO_2 and different high-k materials on silicon (1-3). The injection barrier for electrons is higher in La_2O_3 as compared to HfO_2 while both dielectrics have almost the same dielectric constant 25.

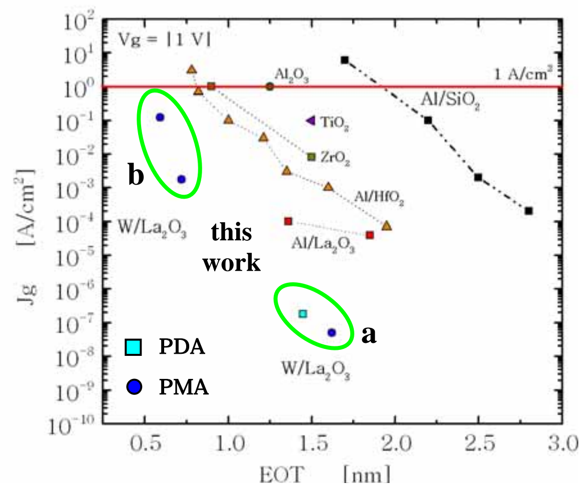


Fig 2 Jg–EOT plot for metal/high-k stacks (4-8). Set A contains PDA and PMA samples for the same La_2O_3 film whereas set B contains only PMA samples for a thinner La_2O_3 film. From set A, the timing of annealing after La_2O_3 deposition can significantly change the EOT versus Jg characteristics.

From fig. 1, we can see for instance that materials like ZrO_2 and HfO_2 have a large k=25 but they also have small band offsets for electrons and holes when these materials came into contact with silicon. A material like Al_2O_3 has larger band offsets for both carriers but its small value of k=9 makes it unable to replace SiO_2 in the long term. In the case of La_2O_3, the band offsets for electron and holes are both large

enough so that low levels of leakage current by both carriers can be expected. Besides, the k value of La_2O_3 is big enough so that lower EOT levels can be guaranteed for relatively thick films. Fig. 2 shows gate leakage current Jg versus EOT characteristics for some metal/high-k gate stacks (4-8) including the results of PDA and PMA thermal treatments from W-La_2O_3 gated stacks. From these Jg–EOT data, we can observe that there exists a significant difference in La_2O_3 after PDA or PMA thermal treatment. While PMA will produce the lowest Jg levels, its EOT value gets slightly compromised, yet the final effect of both annealing procedures on the reliability characteristics of La_2O_3 gated devices has not been totally clarified. In a previous report (9), the reliability characteristics of Al and W-gated La_2O_3 MOS capacitors were evaluated after annealing the deposited dielectric in what is called Post-Deposition Annealing (PDA). This PDA thermal treatment consists in annealing the dielectric film immediately after its deposition on the silicon wafer. After PDA, it is expected to improve the La_2O_3-silicon interface quality in order to reduce the density of defects and/or interfacial trapped charge thus improving its electrical characteristics like mobility from La_2O_3-gated MOS transistors (10). Obviously, the nature of the silicon–high-k interface is of paramount importance regarding to the successful operation of MOSFET devices because after modifying the electronic structure of this interface, technological requirements can be meet (11). The La_2O_3 film after PDA will modify its bulk and interface properties with silicon by going through some physical and chemical changes during the thermal treatment. Here, one of the most important side effects of PDA on La_2O_3 is that oxygen losses can occur during the thermal treatment or even during the deposition of La_2O_3 itself thus increasing the density of oxide traps inside the dielectric and consequently, degrading its electrical

characteristics (12-13). On the other hand, the effect of PMA for La_2O_3 films has been that a more positive Vfb can be obtained (from Capacitance–Voltage CV measurements) as compared to PDA for the same gate metal, thus leading to think that the occurrence of oxygen loss during annealing is less probable after the metallization step (14). Moreover, PMA involves the improvement on the physical quality of both silicon–high-k and metal–high-k interfaces so that more reliable characteristics of MOS devices after PMA can be expected. In the present report, we evaluate the effect of PMA thermal treatment on the reliability characteristics of W- La_2O_3 gated MOS capacitors after positive constant stress.

Two different deposition methods and annealing sequences for La_2O_3 were used in order to evaluate the impact of the annealing timing within the process flow and also, the influence of in-situ metallization for reliability characterization. The silicon substrate doping for all samples was between 1e15 to 6e15 cm^{-3}. Only dry N_2-based annealing was performed for all samples and they are schematically depicted in fig. 3.

(a) La_2O_3 Deposition in vacuum with ex-situ Tungsten Deposition

Thin films of La_2O_3 with physical thickness = 9.7nm were deposited on HF-last or Hydrogen-terminated n-type silicon substrates by electron-beam evaporation using Molecular Beam Epitaxy MBE system (ANELVA I) at 300°C. The base vacuum in the chamber during the deposition was around 1x10-7 Pa with a constant rate of

0.5nm/min, which is much smaller than one single atomic layer so that the thickness of the films grown by this method can be easily controlled. Following the La_2O_3 deposition, PDA and PMA thermal treatments were carried out in N_2 ambient at 300°C during 5min by Rapid Thermal Annealing (ULVAC-MILA 3000) system. Tungsten was used as the metal gate electrode for both PDA and PMA–annealed samples and it was sputter-deposited within 30min after the deposition of La_2O_3 to reduce moisture absorption and any possible contamination on these films at minimum. Tungsten deposition with a thickness of W= 50nm was carried out by using a metal shadow mask with circular patterns for the gate definition of MOS capacitors. Tungsten was deposited by RF magnetron sputtering at room temperature. C-V, I-V and Time-Dependent Dielectric Breakdown (TDDB) electrical characteristics were obtained using a precision LCR meter (HP 4284A) and Semiconductor Parameter Analyzer (HP 4156C) respectively.

(b) La_2O_3 Deposition within O_2-Flow with in-situ Tungsten Deposition

In order to reduce any possible oxygen loss during the La_2O_3 deposition (13), which is carried out at 300°C, La_2O_3 for these samples was deposited within an oxygen flow of 1x10-5 Pa. Also, in-situ sputtering of tungsten was done at 150W in a contiguous chamber (within the same MBE system) immediately after the dielectric deposition in order to reduce the exposition of La_2O_3 surface to the environment. Because of this, the physical thickness of La_2O_3 can not be extracted by conventional methods like ellipsometry but by Transmission Electron Microscopy TEM or any other imaging

technique. However, it is estimated that the physical thickness for this film was about 4 nm (more than half the physical thickness used for the first samples). During the deposition of the metal an argon flow of 1.33 Pa was used. Patterning of the gate electrodes was done by Reactive-Ion Etching RIE within SF6 plasma radical specie and with a 30W DC power. There were SiO_2-based spacers (200nm in thickness) used around the gates of the devices in order to minimize La_2O_3 exposition to environment's moisture. Finally, PMA thermal treatments in N_2 ambient at 300°C and 500°C during 5 min were carried out. Same as with the first samples, the C-V, I-V and TDDB electrical characteristics were also obtained using a precision LCR meter (HP 4284A) and Semiconductor Parameter Analyzer (HP 4156C) respectively. The experimental procedures for both samples are all resumed in Fig. 3.

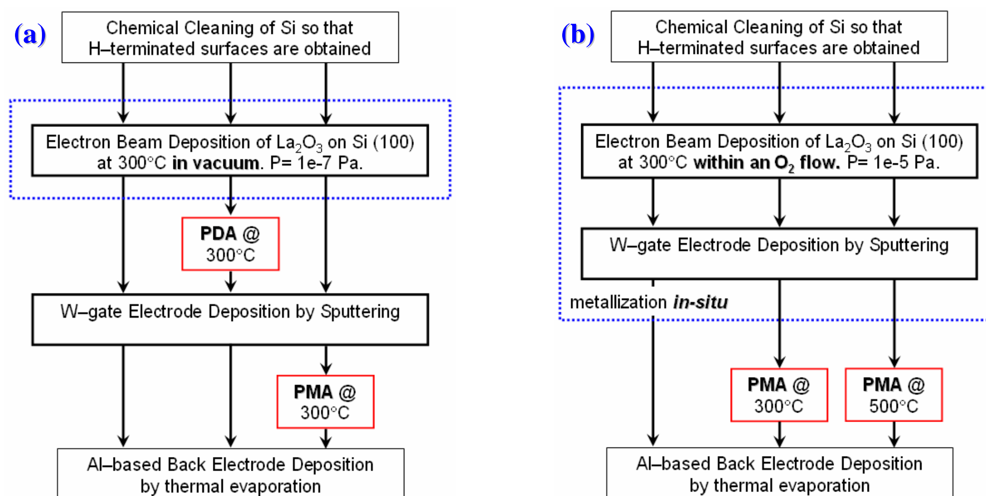


Fig 3 Process flow for the samples used in this work. Two different processing methods were used to evaluate the impact of *in-situ* metallization on W–La_2O_3 reliability. In the first deposition of La_2O_3, 3 different samples were obtained: as-deposited (no-annealing), PDA and PMA both at 300°C. In the second (and modified) deposition of La_2O_3, a thinner dielectric film was deposited and 3 different samples were also obtained: as-deposited, PMA at 300°C and PMA at 500°C.

(a) Vfb shift and lifetime projection for W-La_2O_3 gated MOSCAP with EOT > 1 nm

Fig. 2 shows gate leakage current Jg versus EOT for some metal/high-k gate stacks [4-8]. The Jg results for W-gated La_2O_3 stacks used in this section are also shown. From these Jg–EOT data, we found a significant difference in the resulting characteristics of La_2O_3 after PDA or PMA (PDA means that La_2O_3 was annealed right after its deposition on Si and before metallization). From the set A samples, La_2O_3 after PMA produces the lowest Jg level but its EOT gets slightly increased, so that the sensitivity of La_2O_3 electrical characteristics with respect to the annealing timing and conditions within the process flow can lead to further improvements in its final reliability. This difference in the EOT-Jg characteristic for La_2O_3 after PDA and PMA samples comes after considering that a stronger densification of the La_2O_3 film during PDA results in a stronger reduction of La_2O_3 thickness thus decreasing the final EOT for this particular sample. Besides, it is thought that PMA improves the physical quality of both silicon/high-k and metal/high-k interfaces simultaneously so that more reliable characteristics of MOS devices after PMA can be expected. In the present report, we evaluate the PMA effect on the reliability characteristics of MOS capacitors with W-gated La_2O_3 dielectric after constant positive voltage stressing.

From figure 2 we can observe that for an EOT around 1.5nm, Jg decrease for almost three orders of magnitude by using W-gated La_2O_3 instead of aluminum as its gate electrode. Here, the Al-gated La_2O_3 MOSCAP made use of a much thinner dielectric film (La_2O_3 thickness= 4.3nm) compared to W-gated La_2O_3 (La_2O_3 thickness= 9.7nm) thus its Jg levels are higher as expected. The main disadvantage of Al-gated La_2O_3 is that a low-k Al_2O_3-based interfacial layer is developed at the Al–La_2O_3 interface that

ultimately increases EOT and this effect worsens after PMA (15). Therefore, a less reactive interface between gate metal and La_2O_3 is desired. Tungsten, having a higher resistance to form or break bonds with oxygen compared to aluminum (because of its larger bond enthalpy to oxygen) is therefore ideal. On the other hand, depending on the annealing conditions of the W-La_2O_3-nSi system, this EOT level can be further altered after PDA or PMA thermal processing. For the same La_2O_3 physical thickness, it is clear that a W–La_2O_3 stack after PDA will produce the lowest EOT while keeping a slightly higher Jg as compared to its PMA-annealed sample. In order to explain these EOT and Jg differences, measurements of the physical thickness of La_2O_3 after PDA were obtained but before presenting these results we would like to first focus on the C-V measurements done to all samples. Fig. 4 shows the C-V characteristics of the samples fabricated after the process flow A of fig.3 before and after a positive Constant Voltage Stress (CVS). From fig. 4a, EOT=1.45 and 1.62nm were estimated for PDA and PMA samples respectively, and two different values for the dielectric constant k of La_2O_3 were found from these C-V curves after taking into account the quantum mechanical correction (16). The C-V characteristics in Fig. 4a show that the W-La_2O_3-nSi stack without annealing (known as the as-deposited or as-depo condition) present large amounts of hysteresis compared to PDA and PMA samples. An important difference between thermally grown SiO_2 and La_2O_3 is that the later is deposited directly on Si substrates, so that a high density of interface traps Dit would be expected because of a high roughness and density of defects present at the La_2O_3-nSi interface. In Fig. 4a, the clockwise hysteresis loops suggest that hysteresis is caused by negative charge trapping which would occur during the C-V transition from depletion to accumulation regimes. By annealing the stack with a PDA thermal treatment, an

increase in the accumulation capacitance Cacu and a slight shift of Vfb towards the negative side occur.

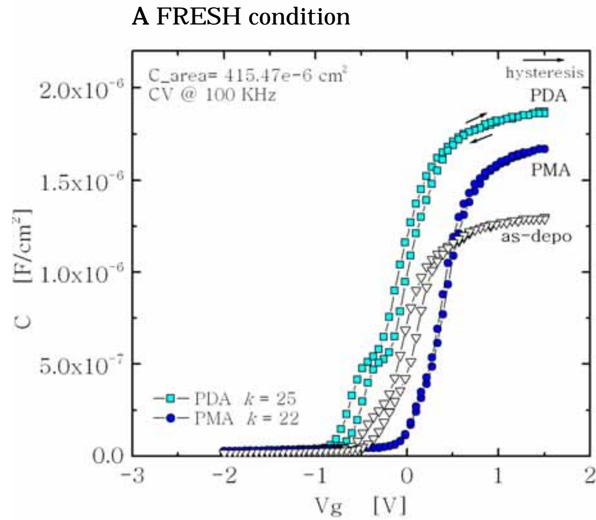
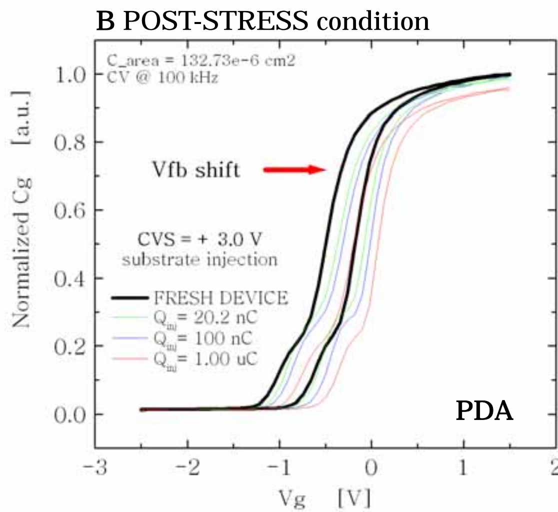


Fig 4a, b, c C–V characteristics of W–La_2O_3 gated MIS capacitors after PDA and PMA thermal treatments. After annealing, lower hysteresis and decrease in EOT are obtained as compared to non-annealed sample.



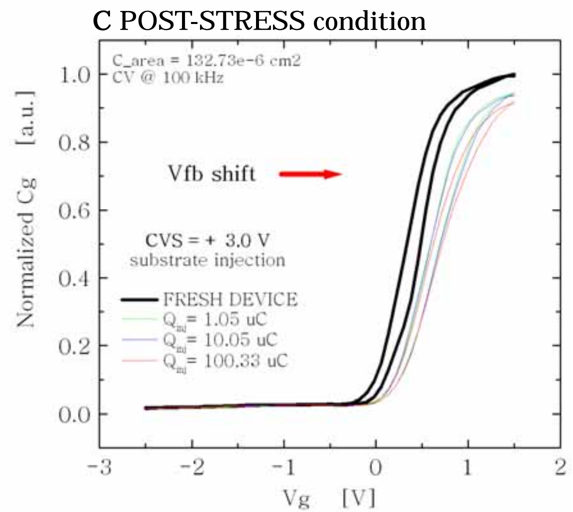


Fig 4b, c C-V characteristics of fig. 4a before and after positive constant voltage stress CVS. PMA samples will produce the lower shift in flat-band voltage Vfb after CVS for even higher densities of injected charge Qinj.

The increase in Cacu after PDA seems to be related to the densification of the lanthana film which would result in a reduction of the initial thickness of La_2O_3, see fig. 5. The reduction of the total amorphous dielectric physical thickness from its initial value for

the as-deposited stack to thinner values after PDA and PMA (from 9.7 nm for the as-depo sample to 9.1 nm after PDA) indicates that annealing results in film densification. Some reports also indicate that part of oxygen in lanthana is consumed to form a silicate-based IL (13). As a result, La_2O_3 film becomes oxygen-deficient especially near/at the IL and has a more negative Vfb, since oxygen deficiency in the oxide film results in negative Vfb shift (17-18). Now, given that the physical thickness of La_2O_3 for those particular samples was relatively high (about 10nm) and that the temperature used during the PDA and PMA treatments was relatively low (300°C for 5min for both samples), it is thought that the observed increase in Cacc shown in figure 4a, comes mainly by the densification process of bulk La_2O_3 whereas the silicate formation only affects the lower portion of the La_2O_3. This is to say, a very thin silicate IL layer would form between the La_2O_3 and silicon and not all of the La_2O_3 would turn into silicate. This is evidenced by the increase in Cacc after annealing in figure 4a, since complete reduction of La_2O_3 into silicate would increase EOT as compared to non-annealed La_2O_3 film. Of course, a more complete physical characterization of La_2O_3 after annealing is needed to verify IL formation. Nonetheless, there are reports in which the reduction of full La_2O_3 into silicate for even thicker films can be expected if the annealing temperature is increased to levels (900°–1050°C) well above the temperatures we used in this report. Additionally, La_2O_3 is known to be readily affected by moisture absorption so that the presence of $(OH)^{-1}$ ions replacing O^{-2} sites could become another factor for the Vfb shift toward negative side (14). Finally, the PDA sample still presents a slight degree of hysteresis formed during the C-V measurement. This can be thought as a consequence of the rough interface present now at the metal-oxide interface. Since the W-gate was deposited directly on La_2O_3 at room

temperature by sputtering, it is expected that a high degree of charge traps are present now at the W-La_2O_3 interface and also within La_2O_3 itself after the damage introduced by this plasma-related processing technique. It is highly likely that after PMA, some of this plasma-related damage will be annealed-out and hence, La_2O_3 with better reliability characteristics will be expected as compared to PDA samples. This difference in the reliability properties after annealing will be demonstrated later on this paper.

On the other hand, the C-V characteristic of the PMA sample in fig. 4a shows a Vfb recovery towards positive side and a slight decrease of Cacu when compared to its PDA counterpart. The decrease in Cacu comes after considering that the physical thickness of La_2O_3 is not efficiently reduced after PMA because the dielectric is already covered with the metal electrode. Nevertheless, it is recognizable that a significant La_2O_3 densification after PMA has occurred just as in the PDA case when both samples are compared to the as-depo curve. Fig. 4a also shows that a slight positive shift in Vfb for the PMA sample has occurred and this effect can be explained whether by the reduction in the oxygen-loss after PMA because the La_2O_3 film is already covered by the metal electrode during the annealing (in the PDA case, La_2O_3 is totally exposed to the environment and thus higher oxygen-losses could take place leading to huge negative Vfb shifts) or by the chemical reactions taking place in the W-La_2O_3 and/or La_2O_3-silicon interfaces during the annealing itself. A plausible explanation for the positive shift of Vfb after low-temperature PMA comes after considering that formation of a silicate layer generating negative charge in the dielectric film could result in this Vfb shift towards the positive side (14). Another

explanation for positive Vfb shift is the formation of chemical bonds at the interface between the metal electrode and the dielectric during PMA (19-20). In any case, the net effect is a positive shift on the Vfb characteristics of PMA samples. Therefore, the thermal processing following the deposition of La_2O_3 plays a key role to control the threshold voltage of W-gated La_2O_3 MOSFETs. Fig. 4b and 4c show the C-V characteristics of PDA and PMA samples before and after a positive Constant Voltage Stress CVS was applied. For both samples, a positive Vfb shift proportional to the charge injected Qinj during CVS stress was observed. In the case of PMA, less hysteresis and less Vfb shift was observed as compared to PDA sample which suggests that some of the damage introduced into La_2O_3 and its interface by sputtered-deposited W was annealed-out. Moreover, the PMA sample shifts Vfb only after a larger Qinj was introduced during the CVS stress as compared to PDA. For both samples, the reduction in Cacu after stress is a sign of the loss of La_2O_3 insulating properties thus allowing a large density of gate leakage current flow through it. Besides, a positive Vfb shift after CVS for both samples shows that a net negative charge is trapped whether inside the bulk of La_2O_3 trap sites or at the interface the dielectric forms with silicon substrate. Fig. 6 shows the gate leakage current Ig evolution with time during a short CVS stress. The purpose of the data in fig. 6 is to show that by applying higher CVS, the Ig evolution with time is smoother for PMA samples when compared to PDA. For instance, at a CVS > 2.0V, Ig for La_2O_3 after PDA evolves with a more noisy behavior (which can be thought as a high occurrence of trapping-detrapping events during the stress) instead of the smoother but monotonous decreasing behavior of Ig for La_2O_3 after PMA. The general tendency of Ig to decrease during CVS is explained by the trapping of negative charge which would increase the electric field near to these traps

sites thus distorting the energy band of La_2O_3.

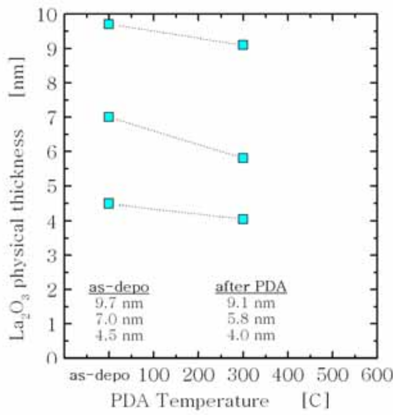


Fig 5 La_2O_3 physical thickness after PDA annealing.

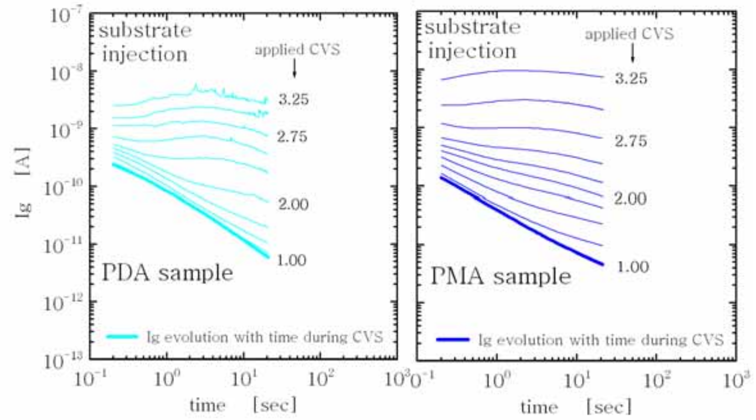


Fig 6 Ig evolution with time of W-La_2O_3 samples after several positive CVS tests.

Fig. 7a shows the J-V characteristics of W-La_2O_3 after PDA and PMA in which the gate voltage Vg increases until the oxide breaks down. Compared to the as-depo sample (which have the largest density of gate leakage current), La_2O_3 after annealing shows better electrical characteristics. For both PDA and PMA samples, at least two different carrier conduction mechanisms can be directly observed at low and high-electric field regimes. The conduction mechanism just before breakdown was also investigated and in the case of both films, Fowler-Nordheim (FN) conduction mechanism was detected. The breakdown strength Ebd of La_2O_3 is obtained from this "time to zero breakdown" measurement. An Ebd= 4.6MV/cm was found for W-gated La_2O_3, which is in agreement with the value reported for La_2O_3 in the literature (21). Figures 7 b-c show the evolution with time of gate leakage current Ig during a time-dependent dielectric breakdown (TDDB) measurement with a positive CVS stress. We can see at least two important characteristics coming out from these TDDB

measurements. First, both PDA and PMA annealed stacks show that their initial levels of gate leakage current are proportional to the CVS applied and so is the time required for these samples to reach breakdown.

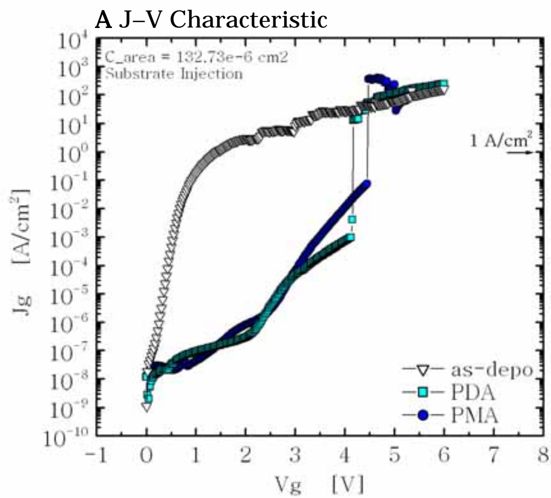
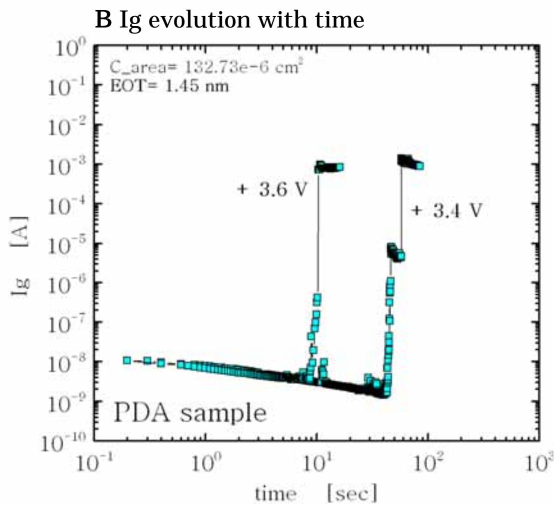


Fig 7a J–V characteristics of W–La_2O_3 gated MIS capacitors after PDA and PMA. The as-depo sample shows extrinsic breakdown characteristic as compared to annealed W-La_2O_3 stacks.



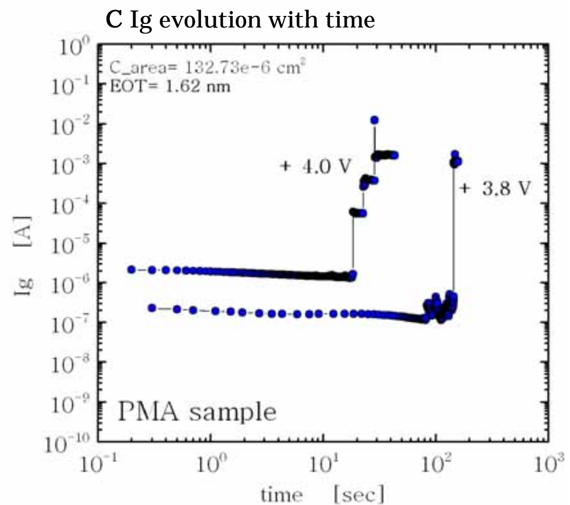


Fig 7b, c Evolution of gate leakage current Ig with time during CVS for La_2O_3 (PDA and PMA samples). PMA samples reach breakdown at longer times even for higher stressing voltages.

For instance, La_2O_3 after PMA shows that for the lowest Vg stress applied, a lower initial gate leakage current level is obtained so that a longer time to breakdown develops. By applying a higher CVS in the same sample, the leakage current increases and the time to breakdown shortens as expected. On the other hand, the initial levels of leakage current for the PMA sample are kept almost without change during the CVS measurement until the samples reach breakdown. This is a significant difference with respect to a PDA-annealed La_2O_3, in which the initial levels of Ig decrease almost immediately after applying the CVS for a few seconds. This fast decrease in the gate current with time is attributed whether to a large density of oxygen vacancies (created after oxygen-losses during PDA) that in turn, generate a large density of trap sites for electrons or to plasma damage introduced during the sputtering of the metal so that a large amount of charge traps are generated within La_2O_3. Because La_2O_3 after PMA can anneal-out some of this plasma-related damage, the density of traps for electrons within La_2O_3 is reduced and thus the evolution or degradation of Ig with time during CVS is more constant like the curve of fig. 7c. In brief, PDA samples show a higher density of traps within the oxide that are electron–filled during the stress and this effect can dramatically shift the Vfb of the MOS capacitors as shown in fig. 4b. Fig. 8 shows the dependence of Vfb shift on injected charge density Qinj for La_2O_3 after CVS for both PDA and PMA samples. From this graph it is straightforward to see that La_2O_3 after PMA produces lower amount of Vfb shift even for greater densities of Qinj. These data is taken from the C-V characteristics shown in figures 4b and 4c. Fig 8b shows the same data as in fig 8 but here we included the results of positive CVS with a lower stressing condition (+1 V compared to +3 V).

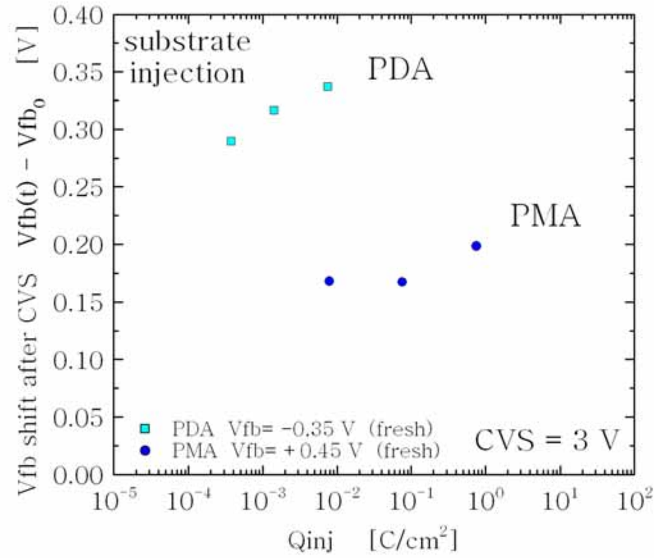


Fig 8 Vfb shift after CVS for La_2O_3 (PDA and PMA). The lowest Vfb shift is obtained for the PMA sample. It is thought that PMA La_2O_3 enhances the electrical characteristics (less charge trapping during stress) of both top and bottom interfaces.

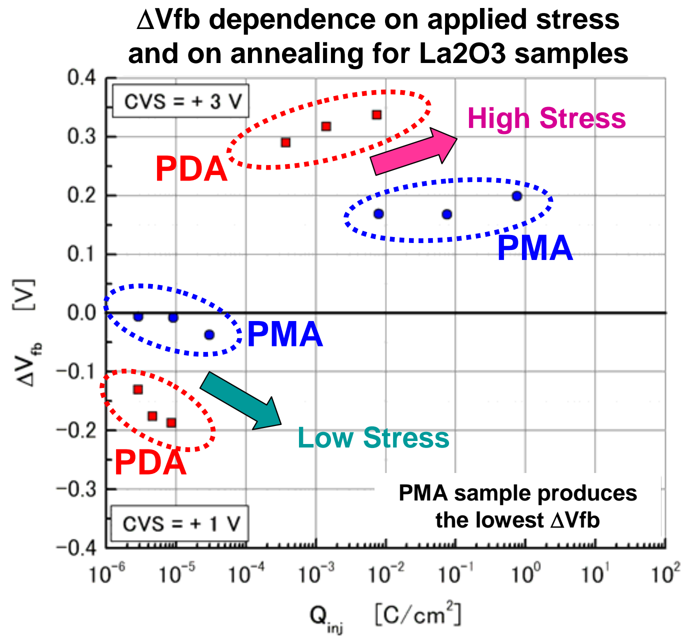


Fig 8b Same data as in fig 8 including Vfb shift at lower stressing conditions. The lowest Vfb shift is obtained for the PMA sample in both low and high-stressing conditions.

We notice that ΔVfb seems to be dependent on electric field. This is to say, at higher applied Vg stress, ΔVfb changes from negative to positive shift after stress. We thought that the change in the direction of the Vfb shift at low/high stressing conditions is related to the trapping-detrapping processes during stress. This model will be explained later in chapter 5. No matter what the direction of Vfb takes after stress, the lower shift in Vfb is obtained for the sample annealed after PMA as compared to PDA La_2O_3. Here we would like to point out that La_2O_3-gated MOSFETs stressed under the same low and high-stressing conditions showed the same direction dependence of Vth shift so that the physical origin for this change of direction in Vfb must have a common origin. These results will be shown later on chapter 4. Fig. 8c shows the C-V results of W- La_2O_3 stack before and after PDA/PMA and biased under low stress conditions (CVS= +1 V). In contrast to the results shown in figs. 4b, c, the Vfb shifts to the negative direction after stress, and the lowest shift in Vfb is produced for the PMA sample even at higher densities of injected charge.

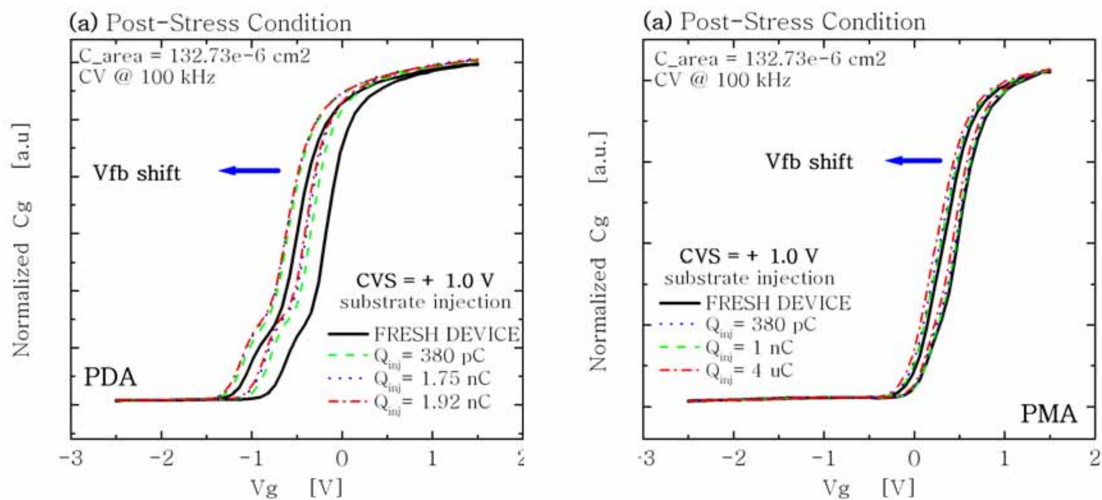


Fig 8c C-V characteristics of fig. 8b before and after lower CVS conditions. PMA samples will produce the lower shift in flat-band voltage Vfb after CVS for even higher densities of injected charge Qinj.

Figures 9 and 10 show the lifetime projection and charge to breakdown density Qbd respectively for W-La_2O_3 stack after PDA or PMA thermal treatments. The lifetime projection and charge to breakdown Qbd data is taken after TDDB with CVS measurements by taking into account a 63% mean time to failure. In figure 9, we can clearly see that compared to PDA, a W-La_2O_3 stack after PMA shows longer times to failure even for the same applied gate voltage Vg. Once this time to failure data for La_2O_3 after PDA and PMA is linearly extrapolated, we found that the gate voltage necessary for both samples to last at least 10 years before breakdown lies around 2.1V and 2.3V for PDA and PMA-annealed La_2O_3 respectively. Thus, even by applying relatively higher Vg to the gate of W-La_2O_3 gated MOS devices, PMA will provide more reliable devices because its lower Vfb shift after stress and its longer lifetime before breakdown. As a reference, the lifetime projection for an Al-La_2O_3 gated capacitor is also shown.

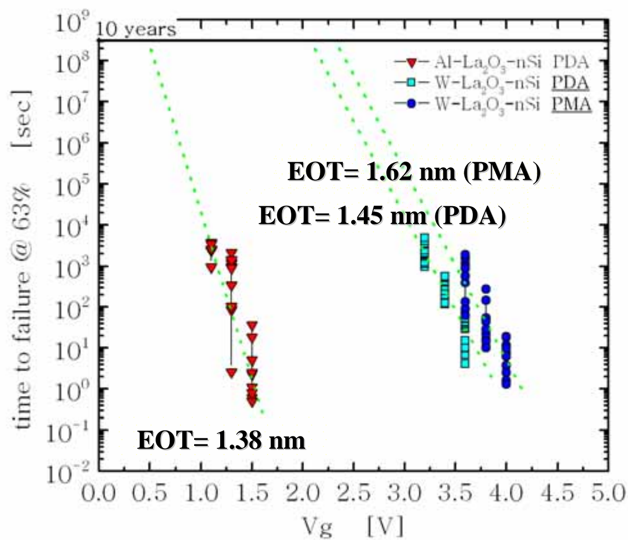


Fig 9 Lifetime projection for W-La_2O_3 gated MISCAP after PDA and PMA. By extrapolating time to breakdown to lower Vg with a linear model, both PDA and PMA samples are projected to survive 10 years of continuous operation if Vg<2V.

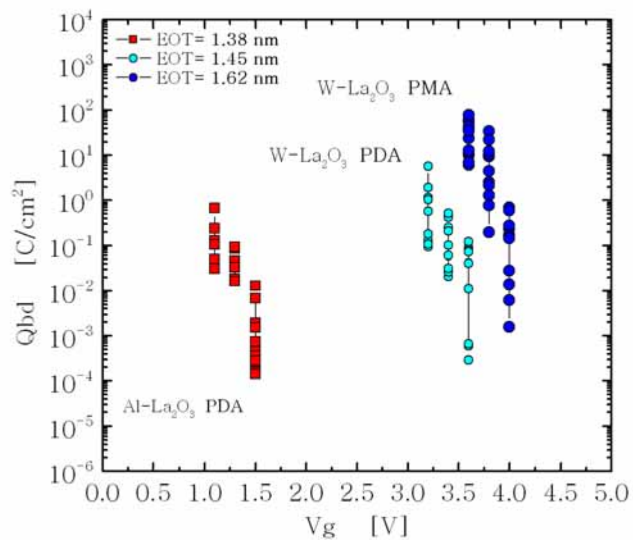


Fig 10 Density of charge to breakdown Qbd for W-La_2O_3 stack after PDA and PMA. Because of the higher charge to breakdown for PMA samples, longer lifetimes are obtained for PMA samples even at higher Vg.

By using Al as the gate electrode, the breakdown event during a CVS measurement is not so easy to interpret because of the presence of an Al_2O_3 interfacial layer between Al and La_2O_3. The breakdown of a very thin Al_2O_3 interfacial layer instead of the bulk La_2O_3 film would explain the very low operative gate voltages that are found after extrapolating its time to failure data. Furthermore, we would like to point out that all these lifetime predictions are only a rough approximation to reality because once the exponential law of voltage dependence reaches very low voltages (compared to those used during operation conditions), the linear model will tend to approach a more power-law based model (22-23). In any case, a 10 years operation is guaranteed by using the very simple linear Vg or reciprocal 1/Vg models because of the high electric fields applied during the stressing of these samples. At high electric fields, the linear and reciprocal models converge and that is why both models can be used here to project at least roughly, the lifetime of La_2O_3. Fig. 10 shows that for W-La_2O_3 after PMA, higher densities of injected charge are required to reach breakdown as expected. At a same gate voltage of Vg= 3.5V, Qbd density for La_2O_3 after PMA is almost 3 orders of magnitude bigger than La_2O_3 after PDA so that longer lifetimes are ensured for La_2O_3 after PMA.

(b) Vfb shift for W-La_2O_3 gated MOSCAP with EOT < 1 nm

In this section we will present some reliability results of a very-thin and high-quality La_2O_3 film (after reducing O_2 deficiency in the dielectric by depositing it within an O_2 flow). We will focus on the results of charge trapping after stress on W-La_2O_3 with PMA in which the metallization step was done in-situ (see the process flow of fig. 3B) so that less exposure of La_2O_3 to the environment was desired in order to reduce any

possible contamination or degradation on its electrical properties (24). Because of the in-situ metallization, it was not possible to measure the physical thickness of La_2O_3 after its deposition. From C-V and J-V data however, we could obtain the EOT and gate leakage current density levels respectively for these samples (see the highlighted data points in the upper left corner of fig. 2). EOT= 0.58nm and 0.74nm were obtained for W-La_2O_3 stack after PMA at 300°C and 500°C respectively. Figure 11 shows the C-V characteristics of these PMA samples together with the as-depo condition for La_2O_3. It can be observed that there is no significant difference between as-deposited La_2O_3 and PMA-annealed La_2O_3. More importantly is that the Vfb shift after PMA was suppressed. The decrease in Cacu for the W-La_2O_3 stack after PMA at 500°C is result of a SiOx-based interfacial layer developed at the La_2O_3-silicon interface and which presence was detected only for this sample after XPS measurements; see fig. 15 (25). It is thought that better interface trap properties (improvement in the quality of the interface immediately above the silicon substrate or reduced interface-state density Dit compared to as-depo sample) between La_2O_3 and silicon can be achieved because of this IL formation; however, Dit after PMA still needs to be evaluated because of the low quality (i.e. high defect density) of the SiO_2-based IL formation. Besides, forming gas annealing the samples would be necessary to passivate the defects at this newly formed Si-SiO_2 interface. Now, because of the very thin La_2O_3 thickness deposited, a high gate leakage current density was always present in these samples so that the time to failure data necessary to project the lifetime of this ultra-thin La_2O_3 film can not be so easily extracted. A conventional TDDB measurement under constant voltage stress for thicker oxide films provides good reproducibility when considering lower dispersion of the time to breakdown data.

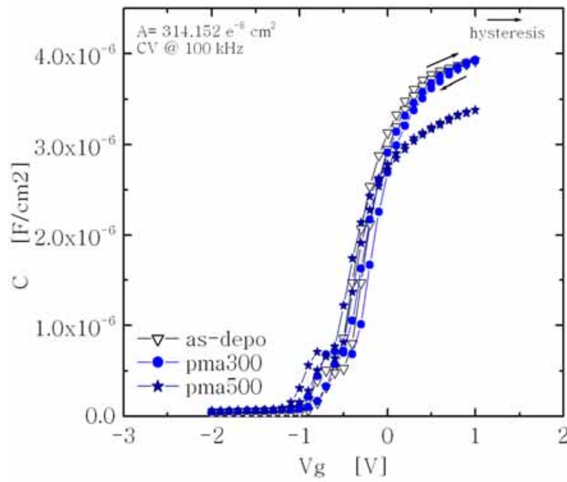
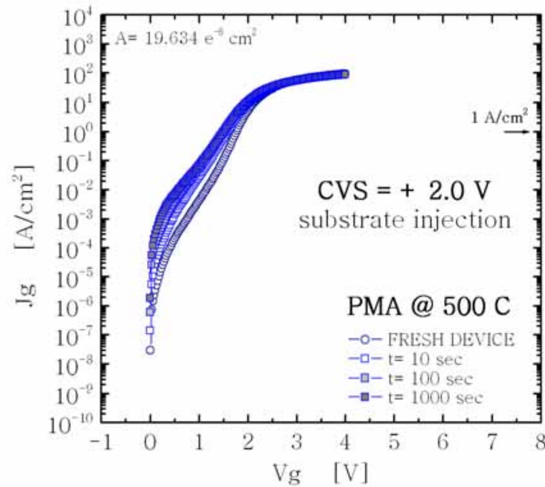


Fig 11 C-V curves for W-La_2O_3 stacks after La_2O_3 deposition within an O_2 flow and in-situ W metallization. PMA samples are also shown. A more stable Vfb for all samples is obtained.



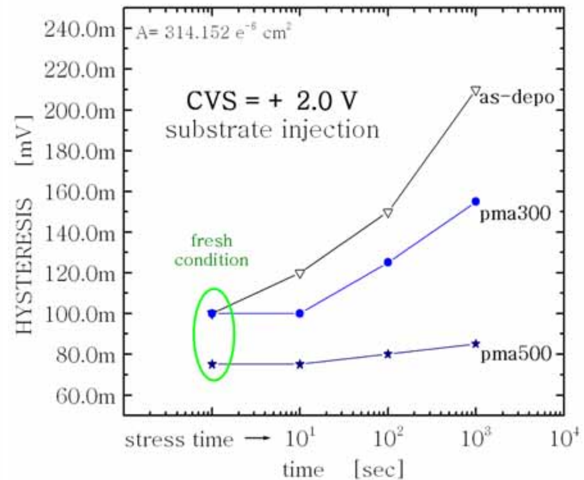


Fig 12 Jg-Vg plot for W-La_2O_3 (PMA@500°C) before and after CVS stress. The huge increase in SILC (which is related to Dit) after stress poses a serious limit for the use of very thin La_2O_3 films.

Fig 13 Increase in C-V hysteresis H after stress for W-La_2O_3. Almost no increase in H is observed for La_2O_3 after PMA at 500°C.

For ultra-thin oxides however, it is very difficult to extract time to breakdown data since the detection of hard-breakdown is no longer straightforward because of the many current fluctuations that appear during the stress. Unlike hard breakdown, where an abrupt increase in gate current or as sudden collapse in the gate voltage can be observed, soft breakdown is observed only as a slight change in voltage or current,

usually accompanied by noise or signal fluctuations. Therefore, the soft breakdown mechanism becomes the dominant effect behind ultra-thin oxide degradation (26-28). One method to detect the oxide degradation on the electrical characteristics of these ultra-thin oxides is by measuring changes in the Stress-Induced Leakage Current SILC, which corresponds with anomalous increases on the gate leakage current that are proportional to the stressing time. Fig. 12 shows that for low electric fields, an anomalous increase of the SILC for W-La_2O_3 stack occurs while at high fields the Fowler-Nordheim current remains unchanged. For ultra thin oxides and low-bias stressing, SILC and Soft-Breakdown (SBD) mechanisms will play a fundamental role in the degradation of the devices. It is important to note that even after plasma-related damage removal by PMA for this very thin La_2O_3 film, this sample still shows a high density of traps that are electron-filled during a CVS and which final effect is a relatively higher increment in SILC. Even though the La_2O_3 film does not reach total breakdown, oxide degradation through a soft-breakdown mechanism is apparently more severe for these thinner films. Fig. 13 shows how the initial hysteresis from fresh C-V curves for W-La_2O_3 devices increases proportionally to stressing time (hysteresis was measured at flat band voltage Vfb from double-sweeping the capacitance firstly from the inversion to accumulation regimes and vice versa). The as-depo and PMA@300°C samples show the largest hysteresis increase for the W-La_2O_3 stack. On the other hand, La_2O_3 after PMA at 500°C shows the lower hysteresis change with stress and this trend is kept almost constant around 80mV even after a stressing time up to 1000 sec. Higher gate leakage current densities and consequently, larger increases in the density of oxide trapped charge Qox during stress are thought to be the main reason behind the huge hysteresis change of the as-depo and PMA@300°C samples. A PMA

at 500°C reduces the density of gate leakage current (see fig. 16) and at the same time, enhances the quality of the La_2O_3-silicon interface by developing a SiOx-based IL there (see fig. 15), so that less hysteresis and Vfb shift after stress could be obtained. Also, it is thought that after higher PMA temperature, a more densified (thinner La_2O_3-IL stack) oxide structure is obtained and in this respect, the reason for the lower hysteresis could be precisely attributed to this physically thinner stack, which has a lower number of defects (assuming a uniform density cm^{-3}; as it has a lower volume, the number of defects in the film will reduce), and consequently there is less charge trapped. Of course, the main disadvantage will be a slight reduction in the final EOT of W-La_2O_3 after a higher PMA temperature.

On the other hand, a higher PMA temperature will further reduce any possible plasma-related damage after the tungsten electrode deposition. All of these effects combined would suggest a decrease in the density of trapped charge at both the La_2O_3-silicon interface and the bulk of La_2O_3. Nonetheless, a higher reliability for this W-La_2O_3 stack will come along with an increase in EOT after PMA at higher temperatures. By suppressing the IL formation, reduced EOT's can be obtained but their reliability can be degraded so that an important issue to be solved for La_2O_3 with high temperature annealing will be to engineer EOT versus IL formation for better reliability.

Fig. 14 shows the change on the C-V characteristics of W-La_2O_3 before and after a CVS in the substrate injection condition. Same as with thicker La_2O_3, a positive Vfb shift proportional to the stressing time is also observed for all these samples. By

annealing La_2O_3 with a higher PMA temperature, less Vfb shift after stress is observed.

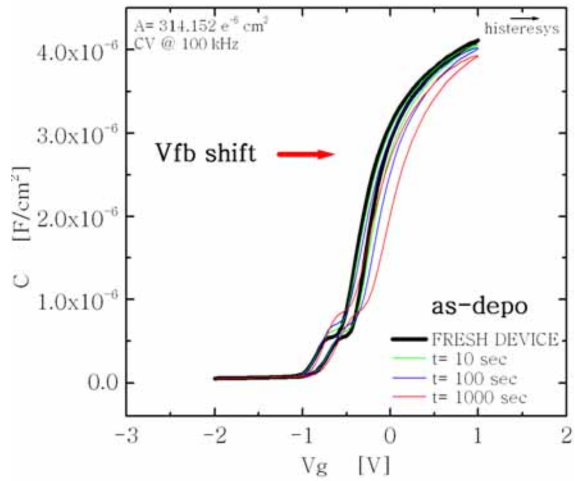
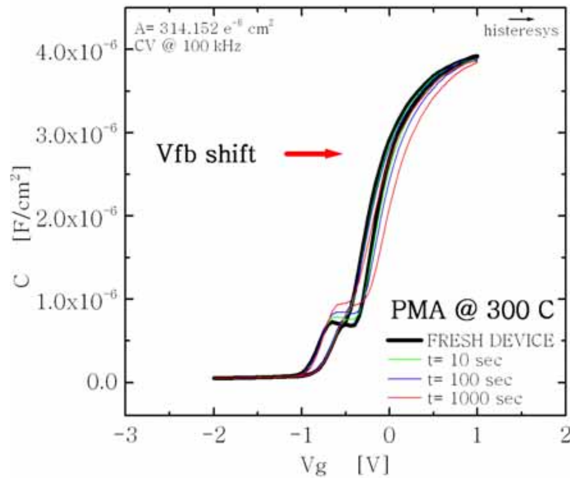


Fig 14a C-V characteristics of W-La_2O_3-nSi stacks (EOT<1nm) before and after CVS. The shifts in Vfb for the as-depo sample are shown.



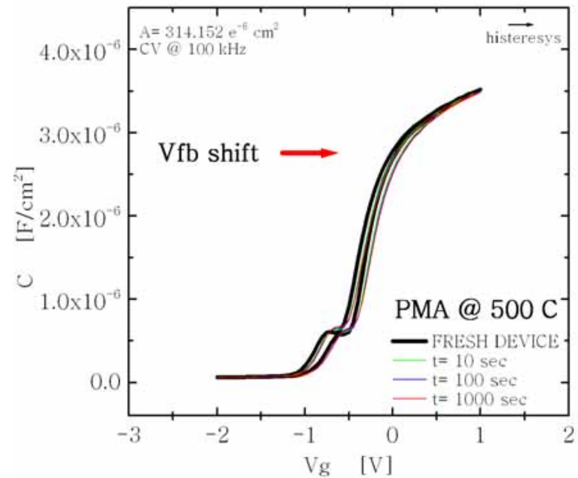


Fig 14b, c C-V characteristics of W-La_2O_3-nSi stacks (EOT<1nm) before and after CVS. The shifts in Vfb for the PMA@300°C and PMA@500°C samples are shown. Even though a relatively high Dit is still present (lowest bump in the CV curve), the lowest shift in Vfb after stress is obtained for the PMA@500°C sample.

One important difference between these C-V curves and those presented in fig. 4 is that less Vfb shift, less hysteresis and thus, a more reliable La_2O_3 is achieved by depositing the W gate electrode in-situ immediately after the oxide deposition. It is important to

note that a high Dit (which is presumably present in all these samples by looking at the lowest bump in the CV curves) makes difficult to calculate the real Vfb of the devices. For that reason we also obtained (and compared to calculated values) Vfb by double differentiating [1/(C/Cacc)] 2 versus Vg curve from the experimental data in which a sharply peaked curve was obtained. The position of the peak was then considered as the experimental Vfb. Nonetheless, irrespective of the real value of Vfb before and after stress, the general trend for all the stressed samples was to shift their Vfb to more positive side as a consequence of electron trapping (being Vfb shift more severe for samples annealed at lower PMA temperature). This allows us to get a general perspective of the highly potential that PDA/PMA treatments have on the trapping characteristics of the devices under evaluation. On the other hand, the chemical analysis of the interfacial layer IL that develops after PMA treatment was done by X-ray photoelectron spectroscopy (XPS). The results are shown in fig. 15.

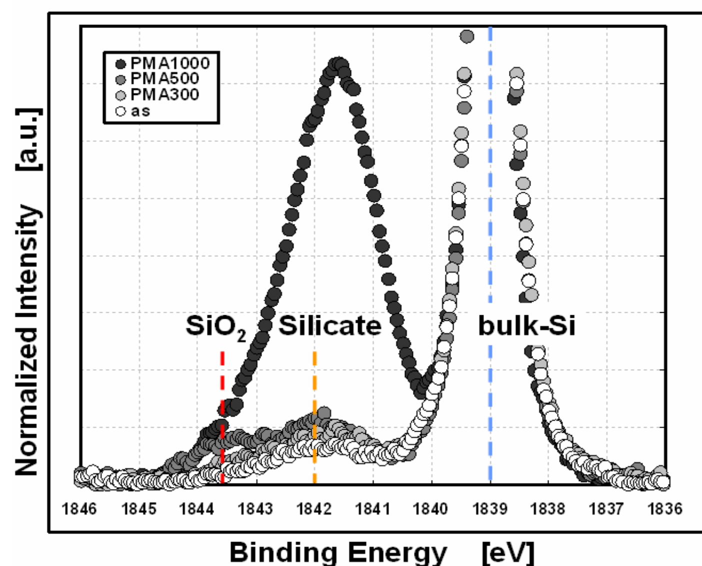


Fig 15 Annealing temperature dependence of Si 1s XPS spectrum of La_2O_3 deposited within oxygen flow. A La-silicate IL formation is present for all samples whereas an additional SiO_2-based IL formation appears for PMA at 500°C.

From XPS results, as-deposited La_2O_3 was reduced to a La-based silicate immediately during the oxide deposition (non-annealed sample). The PMA@300°C sample showed a relatively higher same silicate peak thus confirming that before and after PMA@300°C the chemical composition of La_2O_3 is identical for both samples. This is a consistent result since during the deposition of La_2O_3 (which was done within an O_2 flow), the same temperature was used. For the PMA@500°C sample, the development of a SiOx-based IL together with a La-silicate was detected and this extra IL can have some influence on the several improvements in charge trapping characteristics now so far obtained. The stacked structure obtained after PMA at 500°C is then of the LaSixOy-SiO_2 type.

Fig. 16 shows that after annealing La_2O_3 with a higher PMA temperature, the gate leakage current for this sample will decrease after formation of a SiOx-based interfacial layer at the La_2O_3-silicon interface. As stated earlier, in-situ deposition of tungsten aims to reduce the La_2O_3 exposure to the environment at minimum, thus avoiding undesired contamination. Also, it is thought that because of the interfacial layer formation, a better interface between La_2O_3 and silicon is achieved. Besides, a higher annealing temperature will further reduce any possible plasma-related damage after the tungsten electrode deposition. All of these effects will combine in order to decrease the density of trapped charge at both the La_2O_3-silicon interface and the bulk of La_2O_3. The final effect will be that a more reliable W-La_2O_3 stack will be obtained as shown in Fig. 17, where the Vfb shift after stress is plotted against the density of injected charge Qinj for these samples.

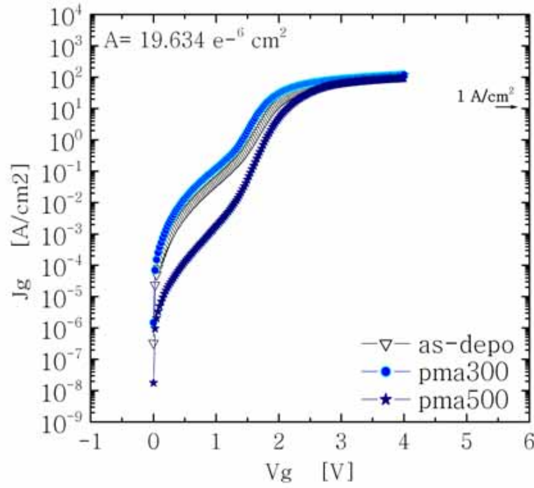


Fig 16 J-V characteristics (fresh condition) for W-La_2O_3 (EOT<1nm) after *in-situ* metallization. Higher PMA temperature will reduce Jg.

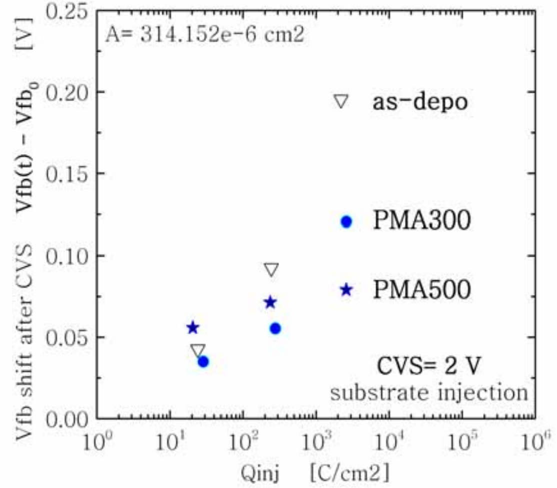


Fig 17 Vfb shift after CVS for W-La_2O_3 with EOT < 1nm. The lowest Vfb shift is obtained for the sample with LaSixOy–SiO_2 stacked structure which is formed after PMA at 500°C.

Fig. 17 shows the dependence of Vfb shift on injected charge density (Qinj) for La_2O_3 films with EOT < 1 nm after positive CVS. The La_2O_3 films after PMA at 500°C presents the lowest Vfb shift after stress. These data are taken from the C-V characteristics shown in figures 14a, b and c. Compared to fig. 8, a higher reduction in Vfb shift after CVS for the thinner La_2O_3 film is obtained and this is related in part to the high-quality of both the film itself, its interface with silicon substrate and also to the very-thin physical thickness of the film as well. A reduction in the density of oxygen vacancies in the film should decrease the density of trap sites in La_2O_3 and because of a SiO_2-based interfacial layer formation, trapping of charge at the interface with silicon substrate is thought to decrease as well. Moreover, a very thin La_2O_3 film will increase the contribution of direct tunneling (DT) leakage current so that the density of trapped charge within La_2O_3 is decreased because DT through very thin

oxide layers can be a much less destructive transport mechanism than FN injection for thicker oxides (29-30). In order to compare the shift in Vfb after stress for samples with different thicknesses, Vfb shift data must be plotted against density of injected charge Qinj instead of stressing time. The results are shown in fig. 18. We can evaluate that from all the samples analyzed, the thinner LaxSiOy-SiO_2 stacked layer (developed after PMA@500°C) the more reliable since a lower Vfb shift was obtained for even higher densities of Qinj.

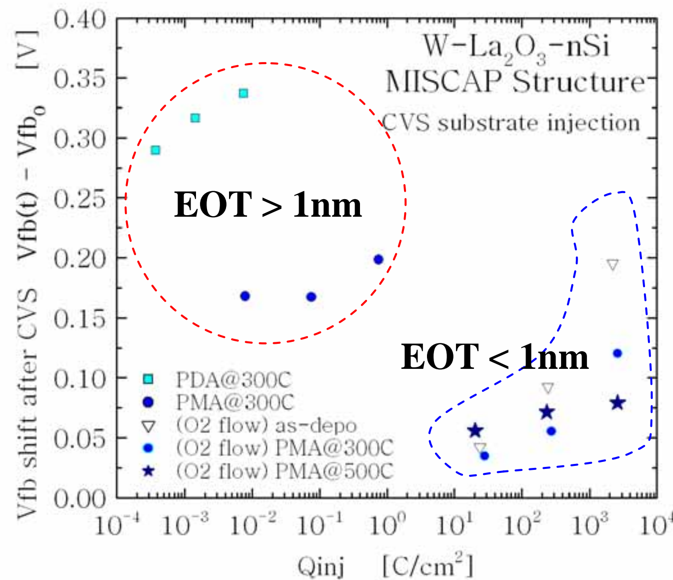


Fig 8 Vfb shift after CVS for thick and thin La_2O_3 film (PDA and PMA). The lowest Vfb shift is obtained for the LaxSiOy-SiO_2 stacked structure developed after PMA@500°C.

Summarizing this section, the electrical and reliability characterization of W-La_2O_3-nSi stacks with EOT= 1.5 nm and less than 1 nm after annealing was carried out. Compared to PDA samples, PMA samples show better reliability characteristics so that important parameters like higher endurance to Vfb shift, longer lifetimes and higher charge densities to breakdown can be obtained. Because of the high voltages

applied during stressing, a 10 years lifetime projection for the W-La_2O_3-nSi system is guaranteed by using the very simple Vg linear model. It is thought that La_2O_3 deposition within an oxygen flow can reduce oxygen deficiency in the dielectric film and in-situ deposition of tungsten on La_2O_3 would reduce exposure of the La_2O_3 surface to environment contamination, so that an improved interface between La_2O_3 and silicon can be obtained. In an effort to minimize the formation of oxygen vacancies and to stabilize the reactivity of the metal–oxide, the deposition of La_2O_3 under process B (figure 3) can be thought as being done under PDA in O_2 ambient, so that La_2O_3 is oxidized during the deposition itself, creating a silicate layer. Although detrimental to the permittivity, the resulting structure should be more stable and less apt to contain oxygen deficiencies [31]. A higher PMA temperature for La_2O_3 enhances the formation of a SiO_2-based interfacial layer, and this higher annealing temperature will further reduce possible plasma-related damage during the tungsten electrode deposition at the same time. All these procedures combined with a very-thin physical thickness for La_2O_3 will result in a more reliable W-La_2O_3 stack. It is thought that the formation of a very thin SiO_2-based interfacial layer could help to improve the reliability characteristics of metal-high-k stacked devices. However, the increase in EOT by lower-k interfacial layer formation is an issue that must be addressed since small EOT less than 1 nm requires very thin dielectrics and thus the controllability and quality of this interfacial layer becomes crucial. Finally, the lowest Vfb shift after stress corresponds for the LaSixOy-SiO_2 stack structure formed after PMA at 500°C.

3.8 Degradation and breakdown of W-La_2O_3 stack after post metallization annealing in N_2

High dielectric constant materials for the gate of MOS transistors can reduce the gate leakage current (Ig) by using thicker oxide films while maintaining the same electrically equivalent oxide thickness (EOT). Lanthanum oxide (La_2O_3), which is a member of rare earth-based oxides, was classified into the next group of potential candidates to succeed conventional oxides [1]. On the other hand, the introduction of metal gates for high-k materials has been focused on choosing the right metal material for good electrical performance and best compatibility with standard CMOS processing. However, metal gate integration and its impact on high-k reliability are not well understood. It is vitally important to understand the impact of metal gates on reliability issues such as defect density, electrical stability, and failure rate since many factors in metal gate integration (deposition, annealing, etching, etc) can potentially affect the reliability of a high-k gated CMOS device. In this work, W-gated La_2O_3 stacked structures were fabricated and the effects of high voltage stressing on their reliability characteristics were evaluated.

MOS capacitors were fabricated on n-type (100) oriented silicon wafers with resistivity of 1–5 ohm·cm. Thin films of La_2O_3 were deposited on HF-last or hydrogen-terminated n-type silicon substrates by electron-beam evaporation using molecular beam epitaxy MBE system (ANELVA I) at 300°C. The pressure in the chamber during the deposition was around $1x10^{-7}$ Pa. Also, in-situ sputtering of

tungsten was done at 150W rf power in a contiguous chamber immediately after the dielectric deposition in order to avoid exposure of La_2O_3 surface to the environment. Because of this, the physical thickness of La_2O_3 cannot be measured by ellipsometry but by transmission electron microscopy. During the deposition of the metal an argon flow of 1.33 Pa was used. Patterning of the gate electrodes was done by reactive-ion etching using SF6 gas with a 30W power. Finally, post-metallization annealing (PMA) was done in dry N_2 ambient at 500°C for 5 min.

The results are presented as follows: first, fig. 1 shows C-V and I-V characteristics of the fabricated samples. From C-V data in fig.1 (A), the as-depo sample presents higher hysteresis compared to PMA sample. Also, the hysteresis loops show that hysteresis is caused by negative charge trapping which occurs during the transition from depletion to accumulation regimes. The increase in EOT after PMA is considered to be due to the reaction of La_2O_3 with silicon into silicate that caused to form a lower-k interfacial layer (IL) between La_2O_3 and silicon [2-4]. In fig.1 (B), the as-depo sample shows a continuous increase in gate leakage current until the oxide reaches breakdown for Vg > 2V, this is followed by a progressive-breakdown (PBD) characteristic, where the breakdown spots would gradually progress with time and stress and they are considered to be associated with the increase of the oxide conductivity which has associated an increase of the total size of the percolation path created during the breakdown event [5-7]. It is thought that for the non-annealed La_2O_3, a higher and random density of bulk/interfacial defects would make easier for these defects to be electrically "connected" during stress so that the size of the total leakage path during breakdown increases. On the other hand, a PMA–La_2O_3 sample suddenly

breaks down for Vg > 4 V, which suggests both reduction and densification of defects within La_2O_3, and thus, a breakdown event with a more discrete nature.

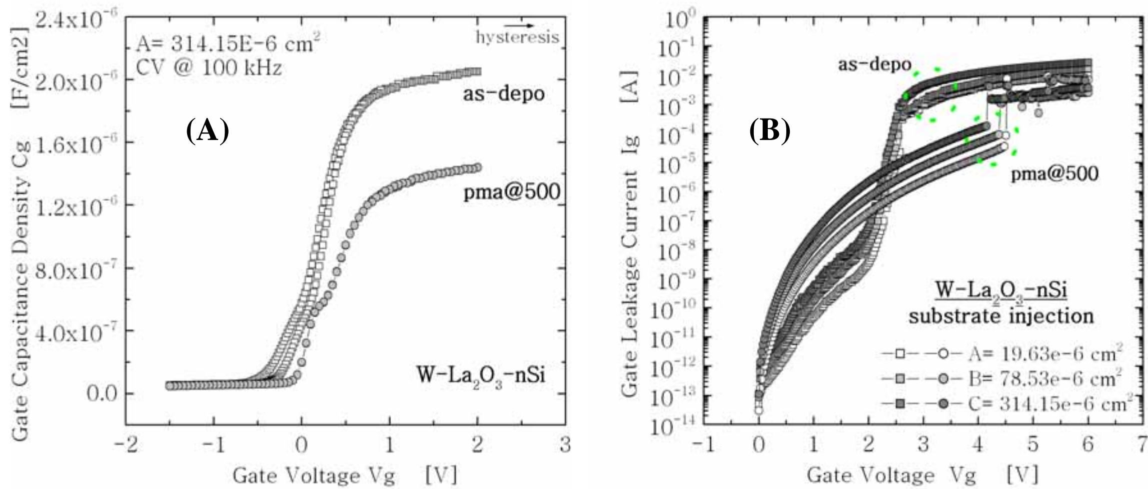


Fig. 1. (A) C-V curves for W-La_2O_3 capacitors before and after PMA at 500°C. EOT= 1.3 and 1.8 nm are obtained for as-depo and PMA samples respectively.
(B) From I-V data, the densification of the films after PMA increases Ig and the time-to-zero breakdown point.

In fig.2 (A), the evolution of Ig with stressing time clearly shows that for identical stress conditions, smaller area devices exhibit larger time to breakdown tbd where more severe breakdown events take place. Different tbd distributions are associated with the average density of generated defects during stress [8], so that samples with larger area would find more sites for defect generation during the stress. Also, the post-breakdown characteristic of Ig for all samples does not show a clear relationship with device area, this suggests a highly localized nature for Ig flow through the leakage spot after breakdown [9]. Despite the disagreement about the defect generation model, there is a general consensus in considering that a critical density of bulk defects generated at random places eventually leads to the formation of a localized leakage

path across the oxide layer [10]. After this, the current runaway and the energy dissipation dynamics through the damaged zone would determine the severity of the event and consequently the magnitude of the leakage current. It is thought that a higher post-breakdown Ig is linked to a greater conductivity and size of the total damaged spot area after stress.

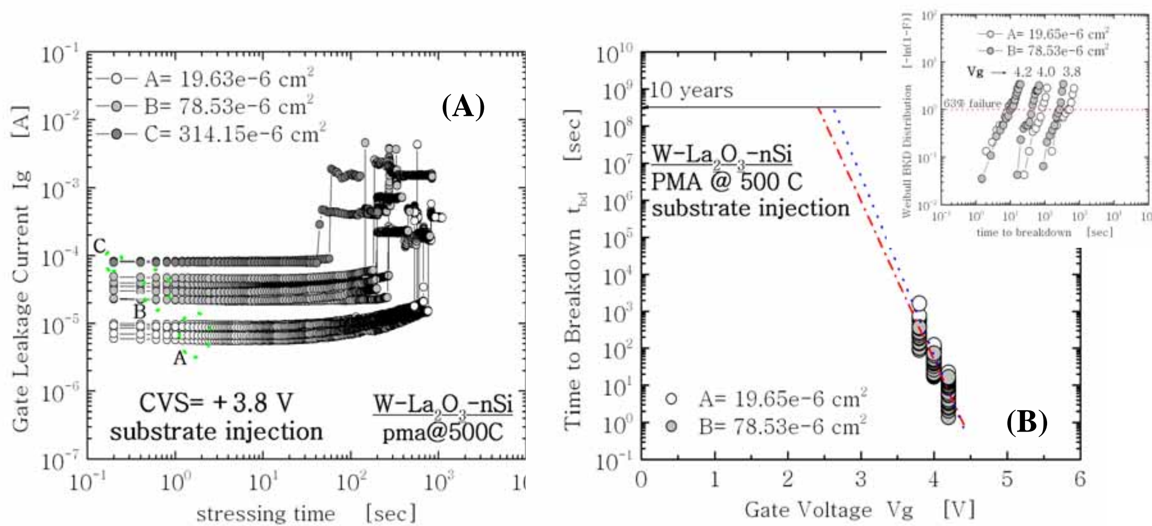


Fig. 2. (A) I-t curves of W-La_2O_3 capacitors. At the same stressing conditions, longer times for breakdown are observed for devices with smaller areas.
(B) Lifetime projection for W-La_2O_3. Smaller area devices present slightly longer lifetimes to breakdown.

In fig.2 (B), the lifetime projection for the W-La_2O_3 stack is plotted based on time-dependent dielectric breakdown (TDDB) measurements with constant voltage stress (CVS) by taking into account a 63% mean time to failure. It is shown that smaller area devices will require longer times to reach breakdown even if the same applied CVS are used. The inset in fig.2 (B) shows the breakdown distributions for two different devices' areas stressed at 3.8, 4.0 and 4.2 V. The stress voltages were applied on the gate with substrate grounded at room temperature. From that figure, it is not

clear whether or not the distribution slopes depend on the area of the test structures. In addition, it cannot be concluded what is the statistical nature of these distributions [11]. By linearly extrapolating tbd data up to 10 years, we found that the maximum gate voltage necessary for W-La_2O_3 stack to reach breakdown is about 2.5 V for both samples. Again, it is important to notice that these lifetime predictions are only a rough approximation because once the exponential law of voltage dependence for breakdown reaches very low voltages (compared to those used during operation conditions), the linear model will tend to approach a more power-law based model [12-13]. In any case, a 10 years operation is guaranteed by using the very simple linear Vg or reciprocal 1/Vg models because of the high electric fields used during the stressing of these samples. At high electric field, the linear and reciprocal models converge and that is why both models can be used here to project the lifetime of La_2O_3. Fig. 3 (A) shows the increase in SILC after positive CVS. Gate voltage Vg was 3.5 V during all the time of stressing measurements. At the same points during the degradation by stressing, which are shown as t1, t2, … , t5 in fig. 3 (B), SILC was measured for all samples by applying a ramped voltage measurement with Vg less than CVS in order to avoid extra induction of defect generation. The normalized SILC values are shown in fig. 3 (C). Interestingly, higher increases in SILC after stress are observed for samples with smaller area during all the range of the gate leakage current evolution with time, shown in fig. 3 (B). During stress, the injection of electrons into La_2O_3 is caused by the same conduction mechanism independently of the area of the device, so that we can assume that the same degradation rate is occurring through all the devices. It is thought that an increased density of new defects generated during stress adds-up to an initially uniform density of intrinsic defects so that smaller area devices under the same stress

conditions will end up with a higher final density of defects which in turn increases SILC, see fig. 3 (D). The newly generated defects can be located at the interfaces of La_2O_3 with silicon, interfacial layer and tungsten or at the bulk of the La_2O_3 itself.

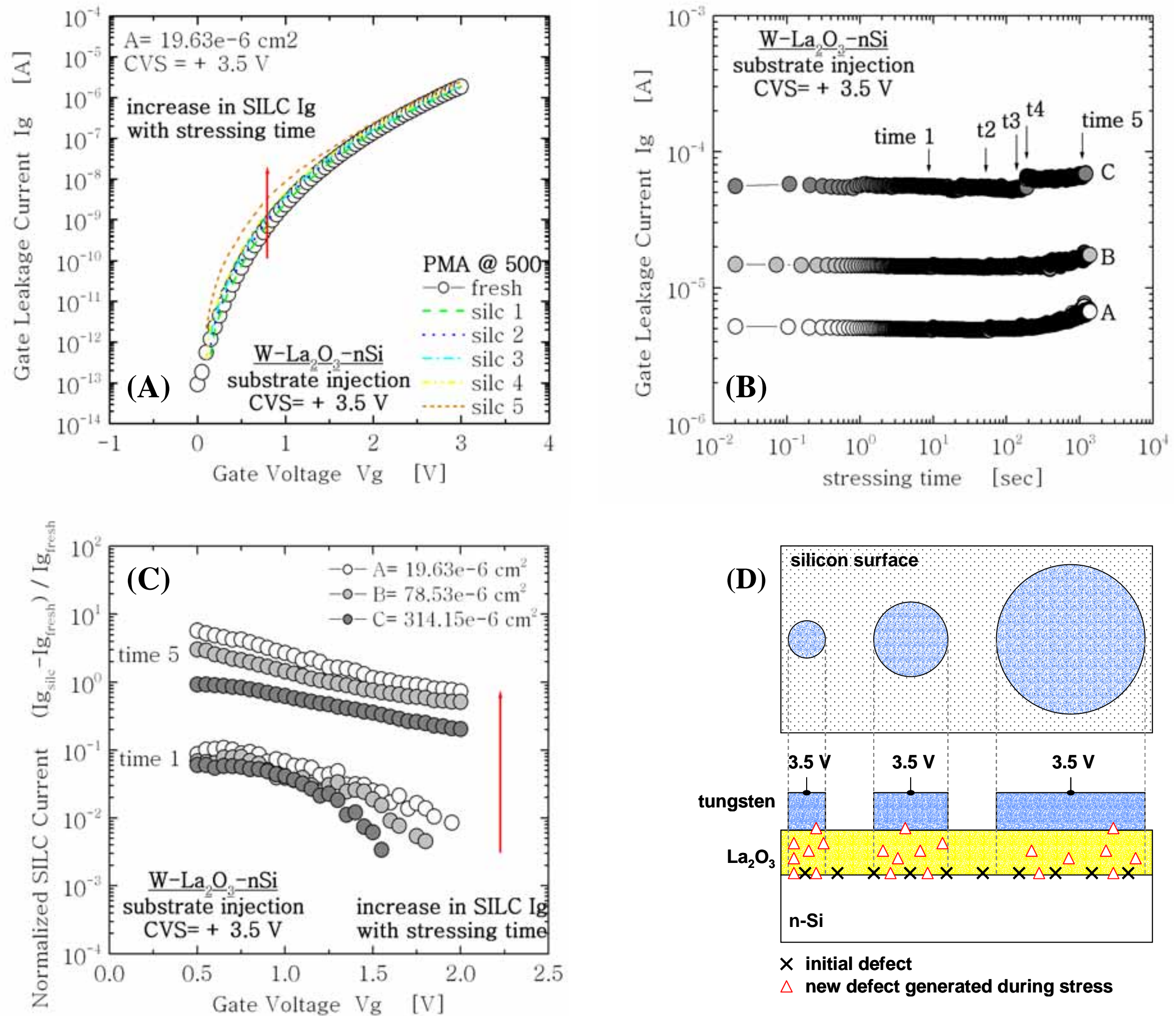


Fig. 3. (A) I-V characteristic of W-La_2O_3 before and after positive CVS. The increase in SILC after stressing time is shown for the device with smaller area.
(B) Evolution of gate leakage current with stressing time. SILC measurement was performed at the same points t1 … t5 for all areas A, B and C.
(C) Normalized SILC Ig current as a function of gate voltage and stressing time. Higher SILC-induced degradation is obtained for smaller area devices.
(D) Schematic model representing the generation of new defects during CVS measurements. Smaller devices get a crowded defect density after stress.

In fig. 3 (D), a very simplified model is drawn to represent this effect. It is seen that smaller area devices will produce a crowd of new and initial defects during CVS as compared to devices with bigger areas. These sites would allow more SILC to flow through the oxide layer by acting as "stepping stones" for tunneling carriers. This phenomenon is often referred to as trap-assisted tunneling. This is important because even though smaller area devices produce longer lifetimes to breakdown during higher-voltage stressing conditions (see figs. 2A-B), the stressing of W-La_2O_3 stacks during lower CVS (as compared to the CVS used for lifetime projection) does not break down the oxide but the damage induced in the dielectric results in an inversely proportional dependence of SILC increase with respect to gate area. This implies that even with long-lasting lifetimes for oxides with smaller areas, their electrical degradation before breakdown will ultimately impose a serious limit towards their use for smaller-area devices.

Summarizing this section, the degradation and breakdown characteristics of W-La_2O_3-nSi gate stacks with EOT= 1.3 and 1.8 nm (after PMA) were investigated. The introduction of PMA at 500°C improved the electrical characteristics of the oxide by reducing hysteresis in the C-V data and increasing the time-to-zero breakdown voltage during a ramped-voltage measurement. By extrapolating time to breakdown results after positive CVS measurements, the lifetime projection for the oxide was obtained. A 10-year operation for W-La_2O_3 is predicted if $Vg < 2.3$ V by using the very simple linear Vg model. The dependence of device's area on the electrical degradation and breakdown of W-La_2O_3 was also investigated. It is found that the post-breakdown characteristic of Ig for all samples does not show a direct relationship with area, which

suggests a highly localized nature the breakdown spot. Finally, even though smaller area devices produce longer lifetimes to breakdown during higher-voltage stressing conditions, the stressing with lower CVS does not break down the oxides but the damage induced in the dielectrics results in an inversely proportional dependence of SILC increase with respect to gate area.

3.8.1 Observations regarding breakdown of La_2O_3

(A) About the increase in damaged area after stress

Although the exact nature of the electron transport mechanism in the stressed La_2O_3 is still unknown and needs to be further investigated, the identification of its post-breakdown I-V characteristics is quite important to determine the origin of the breakdown events. During a progressive breakdown (PBD) event (shown in fig. 1B for the as-depo sample at Vg>2V), we can consider 1) the spreading of a single breakdown spot, which is interpreted as the local accumulation of many leakage sites, or 2) the creation of micro-breakdowns randomly scattered over the device area, corresponding to the onset of many leakage sites in various positions. Nevertheless, the lateral propagation of the breakdown event has been investigated many times by means of combined light emission microscopy and electrical experiments [1-2]. A clear correlation between the size of the damaged area and the leakage current level has been established which has also been confirmed by conductive atomic force microscope measurements [3].

We propose that the gradual increment of the post-breakdown gate current registered during standard electrical tests for this highly defective La_2O_3 film (non-annealed sample) is a consequence of the progressive increase of the oxide conductivity (at the location where breakdown is initially triggered), which has associated an increase of the size of the percolation path created during the breakdown event. However, there is not yet direct experimental evidence on the origin of the current increase after the breakdown event, basically because this phenomenon occurs in areas much smaller

(~10^{-12} cm2) [4] than those that can be characterized with the standard characterization techniques (which normally analyze areas of 10^{-8}–10^{-3} cm2). Therefore, these tests can only provide spatially averaged information of the electrical properties of the broken down region, and no detailed information can be gained since the averaging effect can mask this very specific degradation and breakdown related phenomena. In our present report, the lack of enough data to validate the progressive increase in Ig after breakdown (fig. 1B, as-depo sample) with respect to the increasing size of a single or numerous breakdown spots make us take both cases into consideration. For now, we will refer to the size of the damaged area as the total size of the percolation site generated during breakdown.

(B) About the localized nature of leakage current Ig after breakdown

We considered that the breakdown event (whether as the spreading of a single breakdown spot or the creation of micro-breakdowns randomly scattered over the device area) is localized since the post-breakdown I-t characteristics no longer showed a direct correspondence of gate leakage current level to device area. This is to say, after the triggering of breakdown, a localized and highly conductive percolation path would cause the majority of the leakage current to flow trough it without considering the undamaged area of the device which has itself a lower conductivity. In the present report, the localized nature of the gate leakage current after breakdown was meant to represent the highly conductive and localized breakdown spot trough which the leakage current will flow at higher densities. Besides, the post-breakdown I-t characteristics of some of the analyzed samples show more breakdown events, in which the current presents tiny jumps (the first and highest jump representing the

occurrence of the first hard-breakdown event) during the rest of the stressing time. These extra-jumps are thought to come after the development of different breakdown spots through the initially undamaged area of the device.

(C) About the SILC/HBD dependence on gate area

It was determined that for all La_2O_3 samples stressed by a CVS= 3.5V, the F-N conduction mechanism during this stress regime was obtained. During stress, the injection of electrons in La_2O_3 is caused by the same conduction mechanism independently of the area of the device, so that we can assume that the same degradation rate is occurring trough all the devices.

On the other hand, some researchers have proposed that SILC is caused by interface-state Dit generation, bulk-oxide electron-trap generation and to non uniformities or weak spot formation in the oxide. Since we lack of multiple samples for a more systematic analysis on all these issues, we can only propose at this stage a more idealistic and simple model which is able to explain the dependence of SILC variation with gate area: we propose that an increased density of new defects generated during stress adds-up to an initially uniform density of intrinsic defects so that smaller area devices under the same stress conditions will end up with a higher final density of defects which in turn increases SILC. The newly generated defects can be located at the interfaces of La_2O_3 with the silicon, interfacial layer and tungsten or at the bulk of the La_2O_3 itself. The draw in fig. 3D graphically depicts this model. In fig. 3D, it is seen that smaller area devices will produce a crowd of new and initial defects during CVS as compared to devices with bigger areas. These sites would allow more SILC to

flow through the oxide layer by acting as "stepping stones" for tunneling carriers. This phenomenon is often referred to as trap-assisted tunneling. It is thought that the effect of stress-induced new defects can be partially measured as an increase in Dit (defects generated at the silicon–La_2O_3 interface) so that Dit measurements before and after CVS must be done and correlated to the gate area of the devices. These measurements are currently underway and will be soon published.

When the oxide stress continues, a very highly conducting path is created that triggers breakdown. The important questions that remain are whether these newly stress-induced defects or traps for electrons are generated 1) at specific locations at the bulk/interfaces of La_2O_3, for instance, sites where the accumulation of defects can growth and be "connected", or 2) they are randomly distributed all thorough the oxide until a certain density is reached and breakdown is then triggered. Finally, it is important to determine whether the final breakdown event is triggered by the accumulation of newly induced traps/defects or by the initial density of intrinsic traps/defects readily available before the stress measurement, or by the combination of both.

[1] F. Monsieur et al., "A thorough investigation of progressive breakdown in ultra-thin oxides", Proc. Int. Rel. Phys, Symp., pp. 45-54, 2002.
[2] C. Leroux et al., "Light emission microscopy for thin oxide reliability analysis", Microelectron. Eng., vol. 36, pp. 297-300, 1997.
[3] M. Porti at al., "Propagation of the SiO_2 breakdown event on MOS structures observed with conductive atomic force microscopy", Microelectron. Rel., vol. 59, pp. 265-269, 2001.
[4] J. Sune et al., "The physics and chemistry of SiO_2 and the Si-SiO_2 interface–4" vol. 2000-2. The Electrochemical Society., p. 333, 2000.

3.9 La_2O_3 post-breakdown I-V and I-t characteristics

Up to this point, we have observed that the triggering of breakdown for La_2O_3-gated devices is strongly accelerated mainly by electric field, less by device gate area and though not shown here, it is also highly influenced by temperature. Now this section shows the switching and sometimes noisy behavior of the post breakdown gate leakage current Ig characteristics, and the lateral propagation of the damaged area in very thin La_2O_3 films when subjected to electrical stress.

3.9.1 Switching and noisy behavior of Ig during stress

Most of the electrical characteristics of stressed La_2O_3-IL stacked structures resemble those of very thin SiO_2-based oxide films. Since the application of a positive CVS during the stressing of the samples produces trapping of electrons (coming from the n-type silicon substrate) directly into a SiO_2-based IL before reaching a thicker La_2O_3 film, most of the following theory purposed to explain the switching behavior and propagation breakdown mechanism is then closely linked to that of conventional oxides. For SiO_2-based devices, both HBD and SBD currents have been shown to exhibit discrete switchings at high and low applied voltages, respectively. The switching behavior in thick oxides has often been explained invoking a band-to-band impact ionization mechanism and positive charge trapping near the injecting electrode. However, in present technologies (thinner oxides), it is commonly attributed to the highly localized nature of the current flow through the leakage spot. Although no definitive picture of the phenomenon exists yet, the partial reversibility of HBD in ultra-thin oxides has been addressed to switchings between different oxide conduction

states, to changes in the charge state of percolating sites and to defects' migration caused by the electron wind force effect. On the other hand, the switching behavior after SBD has received much more attention. As before, the phenomenon can be observed both in ramped-voltage measurements and during constant-stress tests. The same results also appear for La_2O_3 (or La-silicate) based devices as shown in fig. 3.16a, b, which illustrate the switching phenomenon in either case.

The most widely invoked mechanism to explain the SBD current fluctuations is the charge trapping–detrapping process, and the underlying idea is that the capture of a single electron within the insulator can cause a perturbation in the local injection field. The mean capture and emission times as well as the fluctuations' relative amplitudes have been related to the energetic and geometric location of the trap inside the insulator band gap. Alternatively, the switchings have been ascribed to the fluctuation of the effective thickness representing the locally damaged region and to on–off modulations of the breakdown paths. So far, no consensus has been reached about this issue whether for SiO_2 or for higher-k based oxides during stress. Fig. 3.16a, b shows the switching characteristic of Ig during stress before and after the HBD condition has been reached. For the I-t curve, a greater size of the gate area was evaluated and this also influences the final behavior of Ig after breakdown.

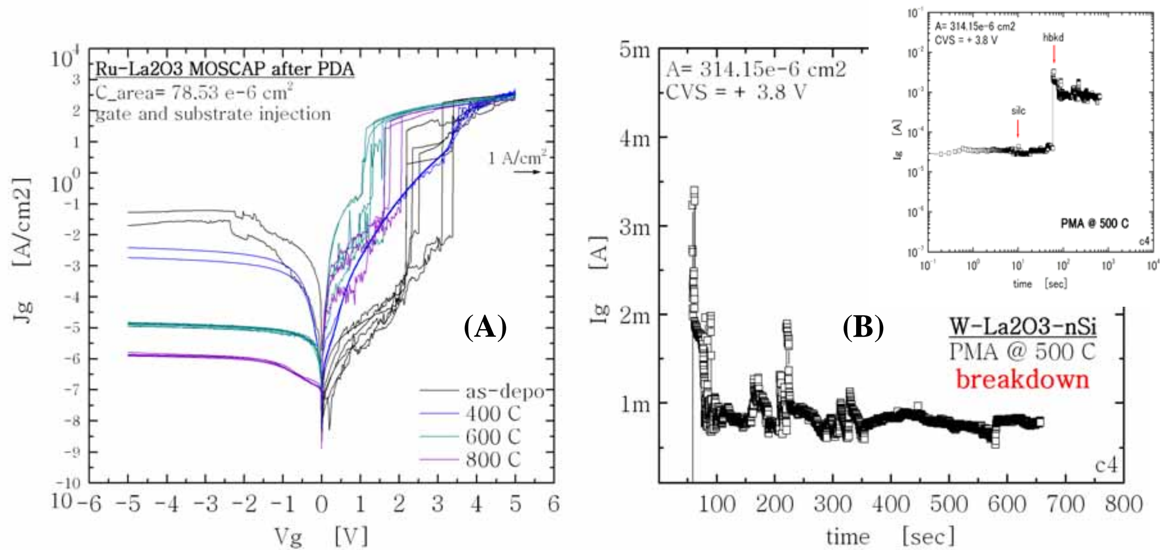


Fig 3.16 (A) I-V data for Ru-La_2O_3-stacked MOSCAP showing the Ig switching characteristic during TZDB stressing conditions. The trapping-detrapping processes occur *before the HBD condition* is reached.
(B) I-t characteristic for W-La_2O_3 MOSCAP. Here, the trapping-detrapping processes occur *after the HBD condition.* The switching characteristic of Ig can be confirmed once the La_2O_3-IL stack breakdown.

3.9.2 Propagation of the breakdown event

The lateral propagation of the damaged area as the result of a constant electrical stress has also been matter of research. Within this evolutionary process, two clearly distinguishable timescales must be considered for the study of the breakdown dynamics. First, there is a timescale related to the formation of the initial leakage spot, which is in the order of nanoseconds [14] and secondly, a timescale related to the subsequent spread of the damage, which is in the order of seconds or more [15]. In this regard, breakdown event has been related to the instantaneous switching of an SBD spot into an HBD spot. Lombardo et al. [14] have suggested that HBD arises as a consequence of the repetition of multiple SBD events occurring in close weak spots induced by local perturbations in the electron distribution at the cathode interface. At

variance with this propagation model, it has been claimed many times that SBD and HBD occur on different locations over the device area, so whether HBD is the consequence of one or more previous SBD events is still a debatable question. However, the fact that for identical stress conditions, larger times-to-breakdown are associated with more severe breakdown events further supports the idea that large average densities of generated defects favored the lateral propagation of the damage.

In a second stage, after their appearance, the breakdown spots can gradually progress with time, be it SBD or HBD. This process has been referred to as progressive breakdown (PBD) and is a major issue for the current CMOS technologies because it might change the way in which oxide reliability criteria must be assessed. Because of this gradual evolution, the time-to breakdown (or charge-to-breakdown) would no longer be the characteristic reliability variable but the time to a given current level (delay@if in [15]). PBD has only been observed in ultrathin oxides and, as revealed by optical studies, it is directly associated with the increase of the damaged area. The degradation and breakdown of ultra-thin SiO_2 films at a local level has also been investigated by means of atomic force microscopy, and it has been found that, although the degradation takes place in areas of few hundreds of nm2, the breakdown event laterally propagates to neighbor spots, eventually affecting areas of thousands of nm2. Using this alternative technique, it has been confirmed that the size of the damaged area is related to the severity of the breakdown event [16]. Following figures 3.17a, b we show the occurrence and posterior propagation of the breakdown spot during electrical stress for a W-La_2O_3-IL stacked MOSCAP structure.

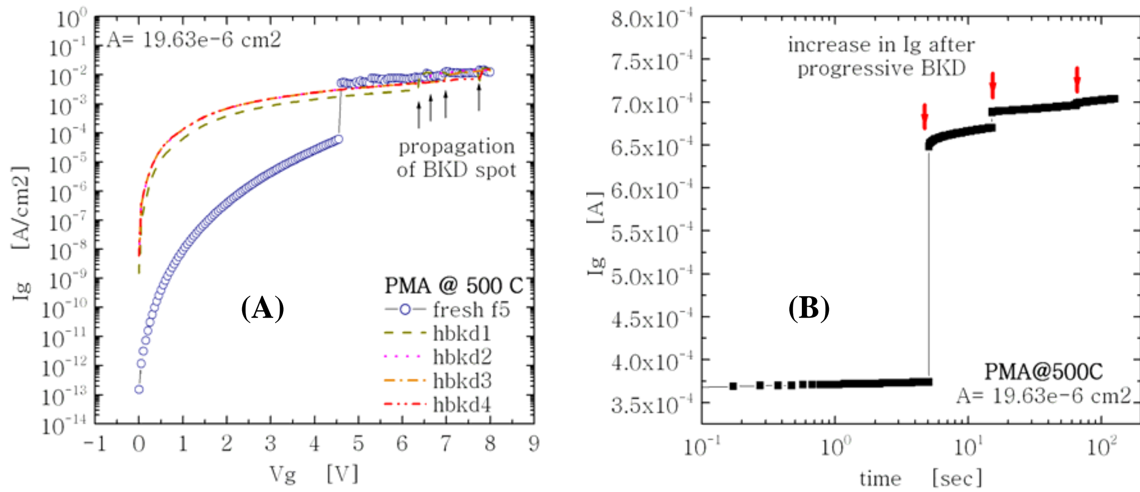


Fig 3.17 (A) I-V characteristic of La_2O_3-gated MOSCAP showing the propagation of the breakdown spot as a gradual "jump"-like increase in gate leakage current Ig.
(B) I-t characteristic for a different sample with the same stacked structure in (A). The propagation of the breakdown spot is clearly visible as the tiny jumps in Ig after breakdown.

3.9.3 SILC-SBD-HBD of La_2O_3-gated MOSCAP

Finally, the I-V electrical characteristics of La_2O_3 before stress (fresh condition), after soft-breakdown (SBD) and hard-breakdown (HBD) events have been obtained and compared to illustrate the effect of positive CVS. The results are shown in fig. 3.18a, b. From fig. 3.18a, we can see that under moderate stressing conditions, the SILC conduction mode does not severely degrade the La_2O_3 insulation properties during stress as compared to SBD and HBD so that operation of La_2O_3-gated MOS devices operated at lower biases (of 1 V or less for future generation devices with a physical gate length of 45nm) is guaranteed. Even after HBD has occurred, the propagation of the breakdown event could continue, thus the final reliability parameter used to quantize the electrical endurance of La_2O_3 to degradation should be taken into a new perspective as was previously discussed.

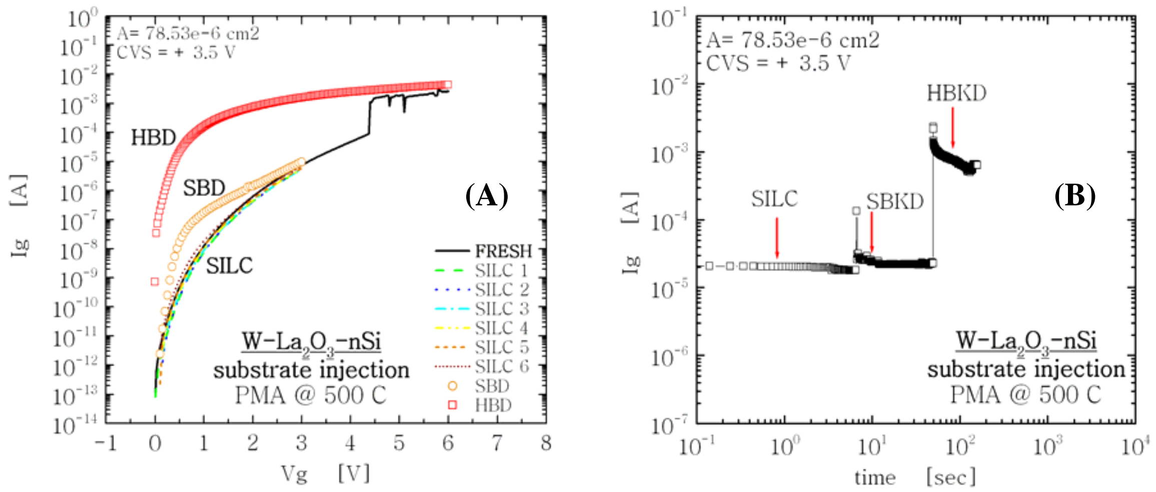


Fig 3.18 (A) I-V characteristic of La_2O_3-gated MOSCAP. The effect of the severity of stress on gate leakage current Ig is clearly shown (in real devices lower stress fields are expected).
(B) I-t characteristic showing the effect of stress on the evolution of leakage current with time. The occurrences of SILC-SBD-HBD are highlighted both in the I-V and I-t data.

Fig. 3.18b shows the occurrences of SILC-SBD-HBD degradation during the evolution of Ig with time and they are both compared to the I-V data in order to better illustrate the real effect that this specific stressing condition would have in the final and more conventional electrical characteristics of La2O3-gated MOSCAP.

3.10 Summary

The I-V, C-V and I-t characteristics before and after time-dependent dielectric breakdown (TDDB) stress of La_2O_3-gated MOSCAP were obtained and compared to the metal gate, the thermal treatment and the severity of the applied stress.

From the obtained results, a higher-k gate oxide stack was achieved with tungsten-based electrodes. This was attributed to the less reactive interface formed between this metal and the La_2O_3 underneath. The aluminum-based system showed a lower k value in La_2O_3, which indicates the formation of a lower-k Al_2O_3 interfacial layer. From TDDB data, and because of the high electric fields applied during stress, a 10 years lifetime is guaranteed for La_2O_3 by using the linear or reciprocal model.

We also evaluated the electrical and reliability characteristics of W- La_2O_3-nSi stacks for relatively thick and thin La_2O_3 film (EOT>1.5nm and EOT<1nm) after annealing. Compared to PDA samples, PMA samples showed better reliability characteristics so that important parameters like higher endurance to Vfb shift, longer lifetimes and higher charge densities to breakdown can be obtained. Same as before, a 10 years lifetime projection for the W-La_2O_3-nSi system is guaranteed by using the very simple Vg linear model. We also deposited La_2O_3 under UHV and O_2 flow (in an effort to minimize oxygen deficiency during the oxide deposition) and also, an *in-situ* deposition of tungsten on La_2O_3 was realized in order to reduce exposure of the La_2O_3 surface to environment contamination. All these were carried out in order to obtain an improved interface between La_2O_3 and silicon. After PMA treatment done on these samples, a higher PMA temperature for La_2O_3 enhanced the formation of a SiO_2-based interfacial layer. All these procedures combined with a very-thin physical thickness for La_2O_3 resulted in a more reliable W-La_2O_3 stack. It is thought that the formation of a very thin SiO_2-based interfacial layer could help to improve the reliability characteristics of metal-high-k stacked devices. However, the increase in EOT by lower-k interfacial layer formation is an issue that must be addressed since small EOT

less than 1 nm requires very thin dielectrics and thus the controllability and quality of this interfacial layer becomes crucial. The lowest Vfb shift after stress corresponded to that of the LaSixOy-SiO_2 stack structure formed after PMA at 500°C.

On the other hand, the dependence of device's area on the electrical degradation and breakdown of W-La_2O_3 was also investigated. It was found that the post-breakdown characteristic of Ig for all samples does not show a direct relationship with area, which suggests a highly localized nature the breakdown spot. Besides, even though smaller area devices produce longer lifetimes to breakdown during higher-voltage stressing conditions, the stressing with lower CVS does not break down the oxides but the damage induced in the dielectrics results in an inversely proportional dependence of SILC increase with respect to gate area. Finally, the post-breakdown I-V and I-t characteristics of La_2O_3 were evaluated in order to get a picture of the switching and noisy characteristic of gate leakage current before and after fatalistic hard-breakdown. The occurrence of a progressive breakdown (PBD) phenomenon for La_2O_3 after HBD was related to the increase in the lateral propagation of the damaged area (increase in the total size of the breakdown spot) as a result of constant electrical stress.

Even though thinner La_2O_3 with EOT < 1nm showed highly degraded SILC characteristics, the expected operation voltages for future generation devices are so low that the reliable operation of La_2O_3-gated MOS devices before HBD can be expected.

References

[1] E. EerNisse, C. Norris, Introduction rates and annealing of defects in ion-implanted SiO_2 layers on Si, J. Appl. Phys. 45 (12) (1974) 5196–5205.

[2] W. Choi, C. Choo, K. Han, J. Chen, F. Loh, K. Tan, Densification of radio frequency sputtered silicon oxide films by rapid thermal annealing, J. Appl. Phys. 83 (4) (1998) 2308–2314.

[3] J. Conley, Y. Ono, W. Zhuang, D. Tweet, W. Gao, S. Mohammed, R. Solanki, Atomic layer deposition of Hafnium oxide using anhydrous hafnium nitrate, Electrochem. Solid-State Lett. 5 (5) (2002) C57–C59.

[4] B. Lee, L. Kang, R. Nieh, W. Qi, J. Lee, Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing, Appl. Phys. Lett. 76 (14) (2000) 1926–1928.

[5] M. Mansouri, Y. Chiou, Y. Ono, S. Hus, Effect of post annealing on the electrical properties of ZrO_2 and ZrAlOx, Proc. Electrochem. Soc.: Phys. Technol. High-k Gate Dielect. I 2002–28 (2002) 135–140.

[6] S. Miyazaki, Characterization of high-k gate dielectric/silicon interfaces, Appl. Surf. Sci. 190 (2002) 66–74.

[7] Z. Weinberg, D. Young, J. Calise, S. Cohen, J. DeLuca, V. Deline, Reduction of electron and hole trapping in SiO_2 by rapid thermal annealing, Appl. Phys. Lett. 45 (11) (1984) 1204–1206.

[8] K. Kakuno, D. Ito, N. Fujimura, T. Matsui, T. Ito, Growth process and interfacial structure of epitaxial Y_2O_3/Si thin film deposited by pulsed laser deposition, J. Cryst. Growth 237–239 (2002) 487–491.

[9] Yongshik Kim, Kunihiro Miyauchi, Shun-ichiro Ohmi, Kazuo Tsutsui, Hiroshi Iwai, "Electrical properties of vacuum annealed La_2O_3 thin films grown by E-beam evaporation", Microelectronics Journal 36 (2005) 41–49.

[10] T. Yoshida, T. Shiraishi, H. Nohira, S. Ohmi, Y. Kobayashi, N. Aun, H. Iwai, W. Sakai, K. Nakajima, M. Suzuki, K. Kimura, T. Hattori, Effect of post-deposition annealing of composition and chemical structures of La_2O_3 film/Si(100) interfacial transition layers, International Workshop on Dielectric Thin Films for Future ULSI Devices, 2004.

[11] J.A. Ng, "A study on mobility of MOSFETs with La_2O_3 gate dielectric", Doctoral Thesis, Tokyo Institute of Technology (2006).

[12] B. Cheng, M. Cao, R. Rao, A. Inani, P. Vande Voorde, WM Greene, JMC Stork, Y. Zhiping, PM Zeitzoff, JCS Woo, "The impact of high-κ gate dielectrics and metal gate electrodes on sub-100 nm MOSFETs", IEEE Trans. on Elec. Dev., 46 (7), pp. 1537-1544 (1999).

[13] "NCSU CVC Analysis, Version 5.0", North Carolina State University, (2000).

[14] Lombardo S, La Magna A, Spinella C, Gerardi C, Crupi F. "Degradation and hard breakdown transient of thin gate oxides in metal–SiO_2–Si capacitors: dependence on oxide thickness", J Appl Phys 1999; 86: 6382–91.

[15] Monsieur F, Vincent E, Roy D, Bruyere S, Vildeuil J, Pananakakis G, et al. "A thorough investigation of progressive breakdown in ultra-thin oxides. Physical understanding and application for industrial reliability assessment", In: Proc IEEE IRPS'02, 2002. p. 50–60.

[16] Porti M, Nafrıa M, Blum M, Aymerich X, Sadewasser S. "Breakdown-induced negative charge in ultrathin SiO_2 films measured by atomic force microscopy", Appl Phys Lett 2003; 81: 3615–7.

References from section 3.6

[1] N. Sa, et al., IEEE Elec. Dev. Lett. 26 no. 9, p. 610 (2005)

[2] J. Robertson, MRS Bulletin p. 217 (2002)

[3] T. Hattori et al., Microelec. Eng. 72 p. 283 (2004)

[4] J. S. Suehle et al., 2001 6th Symp. On PPID, AVS p. 90 (2001)

[5] IEEE Elect. Dev. Lett. 21 no. 7, p. 341 (2000)

[6] Hirotoshi Yamada et al., J. Electrochem. Soc. 150 no. 8 p. 429 (2003)

[7] IEDM ’02, p. 955. S. J. Lee (2002)

[8] VLSI Tech ’05, p. 168. C. Choi (2005)

[9] IEDM ’02, p. 625. H. Iwai (2002)

[10] J. Hauser, CVC NCSU Software, Version 3.0. Raleigh, NC: North Carolina State Univ., (1996)

[11] Chang, C., J. Electrochem. Soc. 125 no. 5, p. 787 (1978)

[12] J. A. Ng et al., Microelec. Eng. 80 p. 206 (2005)

[13] VLSI Tech ’00, p. 16. A. Chin (2000)

[14] F. Palumbo et al., Microelec. Eng. 72 p. 45 (2004)

[15] S. Guha et al., Appl. Phys. Lett. 77 p. 2710 (2000)

[16] Joe W. McPherson et al., IEEE Trans. On Elec. Dev. 50 no. 8, p. 1771 (2003)

[17] A. A. Korkin et al., Comput. Mater. Sci. 24 p. 223 (2002)

[18] IEDM ’00, p. 645. J. H. Lee et al., (2000)

[19] C. G. Ahn et al., Jap. J. of App. Phys., 37 p. 1316 (1998)

[20] J. H. Stathis IBM J. Res. & Dev. 46 no. 2/3 p.265 (2002)

[21] E. Y. Wu et al., IBM J. Res. & Dev. 46 no. 2/3 p.287 (2002)

References from section 3.7

[1] J. Robertson, MRS Bulletin p.217 (2002).

[2] T. Hattori et al., “Composition, Chemical Structure, and Electronic Band Structure of Rare Earth Oxide / Si(100) Interfacial Transition Layer”, Microelec. Eng. 72, pp.283 (2004).

[3] J. S. Suehle et al., 6th Symp. On PPID, AVS p.90 (2001).

[4] Y. Wu et al., “Electrical characteristics of high quality La_2O_3 gate dielectric with equivalent oxide thickness of 5 Å”, IEEE Elect. Dev. Lett. 21 (7), pp.341 (2000).

[5] H. Yamada et al., “MOCVD of High-Dielectric-Constant Lanthanum Oxide Thin Films”, J. Electrochem. Soc. 150 (8) pp.429 (2003).

[6] IEDM ’02, p.955. S. J. Lee et al. (2002).

[7] VLSI Tech ’05, p.168. C. Choi et al. (2005).

[8] IEDM ’02, p.625. H. Iwai et al. (2002).

[9] J. Molina et al., “Electrical Breakdown and Reliability of Metal Gate-La_2O_3 Thin Films after Post Deposition Annealing in N_2”, ECS Trans. 1, (5) pp. 757 (2006).

[10] J. Ng et al., “Effective Mobility and Interface-State Density of La_2O_3 nMISFETs after Post Deposition Annealing”, IEICE Elec. Exp. 3, (13) pp. 316 (2006).

[11] Clemens J. Forst et al., “The Interface between Silicon and a High-k Oxide”, Nature 47, pp. 53 (2004).

[12] Y. Kim et al., "Electrical Properties of Vacuum Annealed La_2O_3 Thin Films Grown by e-Beam Evaporation", Microelec. J. 36, pp. 41 (2005).

[13] J. Maria et al., "High Temperature Stability in Lanthanum and Zirconia-based Gate Dielectrics", J. Appl. Phys. 90, (7) pp. 3476 (2001).

[14] A. Kuriyama et al., "Effect of Post-Metallization Annealing on Electrical Characteristics of La_2O_3 Gate Thin Films", Jap. J. App. Phys. 44, pp.1045 (2005).

[15] Y. Kuroki et al., "Al/La_2O_3 Analysis of Post Metallization Annealed MISFET by XPS", ECS Trans. 1, (5) pp. 239 (2006).

[16] J. Hauser, CVC NCSU Software, Version 3.0. NCSU (1996).

[17] B. Deal et al., J. Electrochem. Soc. 114 no. 3 p.266 (1967)

[18] S. Ohmi et al., "Characterization of La_2O_3 and Yb2O3 Thin Films for High-k Gate Insulator Application", J. Electrochem. Soc. 150 (7) pp.134 (2003).

[19] M. Kadoshima et al., "Flat-band Voltage Shift of MOS Capacitors with Tantalum Nitride Gate Electrodes Induced by Post Metallization Annealing", Mat. Res. Soc. Symp. Proc. 786, pp. (2004).

[20] D. A. Buchanan et al., in Tech. Dig. Int. Electron Device Meeting, Washington DC, USA, Dec. 11-13, pp. 223 (2000).

[21] Joe W. McPherson et al., "Trends in the ultimate breakdown strength of high dielectric-constant materials", IEEE Trans. On Elec. Dev. 50 (8) pp. 1771 (2003).

[22] J. H. Stathis IBM J. Res. & Dev. 46 no. 2/3 p.265 (2002)

[23] E. Y. Wu et al., IBM J. Res. & Dev. 46 no. 2/3 p.287 (2002)

[24] T. Gougousi et al., “Properties of La-silicate high-K dielectric films formed by oxidation of La on silicon”, J. Appl. Phys. 93, 1691 (2003).

[25] K. Tachi et al., “Effect of Oxygen for Ultra-Thin La_2O_3 Film Deposition”, presented at the 210th ECS Meeting at Cancun, Mexico (2006).

[26] Depas M., et al., “Soft Breakdown of Ultra-Thin Gate Oxide Layers”, IEEE Trans. On Elec. Dev. 43 (9) pp. 1499 (1996).

[27] E. Miranda et al., “Soft Breakdown Conduction in Ultrathin (3-5 nm) Gate Dielectrics”, IEEE Trans. On Elec. Dev. 47 (1) pp. 82 (2000).

[28] J. S. Suehle et al., “Ultrathin Gate Oxide Reliability: Physical Models, Statistics, and Characterization”, IEEE Trans. On Elec. Dev. 49 (6) pp. 958 (2002).

[29] I. V. Grekhov et al., “Degradation of Tunnel-Thin Silicon Dioxide Films”, IEEE Trans. On Elec. Dev. 44 (12) pp. 2307 (1997).

[30] Sasaki H. et al., “1.5 nm Direct-Tunneling Gate Oxide Si MOSFET's”, IEEE Trans. On Elec. Dev. 43 (8) pp. 1233 (1996).

[31] M. Copel, E. Cartier and F.M Ross, Appl. Phys. Lett., 78 (11), 1607 (2001).

References from section 3.8

[1] G. D. Wilk, R. M. Wallace and J. M. Anthony, “High-k gate dielectrics: current status and materials properties considerations”, J. Appl. Phys., vol. 89, no. 10, pp. 5243-5275, May 2001.

[2] K.Tachi, K.Kakushima, T.Hattori, N.Sugii, K.Tsutsui, P.Ahmet and H.Iwai, “Effect of oxygen for ultra-thin La_2O_3 film deposition”, ECS Trans., vol. 3, no. 3, pp. 425-434, Oct. 2006.

[3] H. Nohira, T. Yoshida, H. Okamoto, W. Sakai, K. Nakajima, M. Suzuki, K. Kimura, J. Ng, Y. Kobayashi, S. Ohmi, H. Iwai, E. Ikenaga, K. Kobayashi, Y. Takata and T. Hattori, "Thermal stability of lanthanum oxide/Si(100) interfacial transition layer", ECS Trans., vol. 1, no. 1, pp. 87-96, Oct. 2005.

[4] T. Gougousi, M.J. Kelly, D.B. Terry and G.N. Parsons, "Properties of La-silicate high-k dielectric films formed by oxidation of La on silicon", J. Appl. Phys., vol. 93, no. 3, pp. 1691-1696, Feb. 2003.

[5] F. Monsieur, E. Vincent, D. Roy, S. Bruyere, J.C. Vildeuil, G. Pananakakis and G. Ghibaudo, "A thorough investigation of progressive breakdown in ultra-thin oxides. Physical understanding and application for industrial reliability assessment", Proc. IEEE IRPS., pp.45-54, April 2002.

[6] T. Hosoi, P. LoRe, Y. Kamakura and K. Taniguchi, "A new model of time evolution of gate leakage current after soft breakdown in ultra-thin gate oxides", Proc. IEEE IEDM, pp. 155-158, Dec. 2002.

[7] E. Miranda, A. Cester and A. Paccagnella, "Logistic model for leakage current in electrical stressed ultra-thin gate oxides", Electron Lett., vol. 39, no. 9, pp. 749-750, May 2003.

[8] S. Lombardo, A. LaMagna, C. Spinella, C. Gerardi and F. Crupi, "Degradation and hard breakdown transient of thin gate oxides in metal–SiO_2–Si capacitors: dependence on oxide thickness", J. Appl. Phys., vol. 86 , no. 11, pp. 6382-6391, Dec. 1999.

[9] E. Miranda and J. Sune, "Electron transport through broken down ultra-thin SiO_2 layers in MOS devices", Microelectron. Rel., vol. 44, no. 1, pp. 1-23, Jan. 2004.

[10] B. Kaczer, R. Degraeve, A. Keersgieter, K Van de Mieroop, V. Simons and G. Groeseneken, "Consistent model for short-channel nMOSFET after hard gate oxide breakdown", IEEE Trans. On Elec. Dev., vol.49, no. 3, pp. 507-513, March 2002.

[11] E.Y. Wu, W.W. Abadeer, L.K. Han, S.H. Lo and G.R. Hueckel, “Challenges for accurate reliability projections in the ultra-thin oxide regime”, Proc. IEEE IRPS., pp.57-65, March 1999.

[12] J. H. Stathis, “Reliability limits for the gate insulator in CMOS technology”, IBM J. Res. & Dev., vol. 46, no. 2/3, pp. 265-286, March/May 2002.

[13] E. Y. Wu, E. J. Nowak, A. Vayshenker, W. L. Lai, and D. L. Harmon, “CMOS scaling beyond the 100-nm node with silicon-dioxide-based gate dielectrics”, IBM J. Res. & Dev., vol. 46, no. 2/3, pp. 287-298, March/May 2002.

Chapter 4

Reliability of tungsten–La_2O_3 MOS transistors

4.1 Introduction

4.2 Threshold voltage shift (ΔVth)

4.3 Interface-state density (Dit) measurement after stress

4.4 Comparison of degradation by substrate injection with that by gate injection

4.5 Carrier separation measurements

4.6 Carrier separation and Vth shift measurements of W-La_2O_3 gate MOSFET structures after electrical stress

4.7 Summary

References

4.1 Introduction

Fowler-Nordheim (F-N) tunneling has been widely used for programming and erasing memory cells in EEPROMs and may cause significant number of electrons to pass through the thin gate oxides over the lifetime of an aggressively scaled MOSFET. It has been found that these tunneling currents can lead to oxide charge trapping and interface traps generation, which cause long-term drift in threshold voltage and degradation of transconductance and has been identified as one of the major limitation to MOSFET scaling. Since the use of non-conventional gate oxides is expected for future generation MOSFET devices with physical gate lengths of 45 nm or less, we then concentrated part of this dissertation on the analysis of the dependence of La_2O_3-gated-MOSFET electrical characteristics with stress. The La_2O_3 film used for this purpose was covered with tungsten as a gate electrode and was subjected to a PMA in N_2 ambient for 5 minutes, since these conditions were proved to enhance the reliability of MOSCAP and they are expected to increase the intrinsic reliability properties of the W-La_2O_3-IL stacked MOSFETs as well.

This study focused on the characterization of Vth instabilities for La_2O_3-gated MOSFET devices due to low and high-stressing and we correlate these with the degradation of MOSFET characteristics. The stressing of both n- and p-channel MOSFET was mainly focused on three sets of **stress and parameter degradation measurements**: on the first place, the *dependence of Vth shift on the stressing conditions* was evaluated; another very important characteristic was the identification of the polarity of the majority carrier flowing as leakage current and its corresponding

breakdown characteristics using the *carrier separation* technique. The latter measurements are done by using the MOSFET-type structure that is possible to separate both electron and hole carrier contributions to gate leakage current and they are important since can give us a lot of information on the precise breakdown mechanism during stress. Finally, measurements of the *interface-state density (Dit)* before and after stress were done in order to investigate a relationship between ΔDit and ΔVfb. Moreover, the effect of substrate and gate injection of electrons on the electrical characteristics of La_2O_3-IL stacked structure was investigated.

4.2 Threshold voltage shift (ΔVth)

In this section we will present results regarding the time-dependent threshold voltage increase caused by the application of a positive (negative) constant voltage stressing on the gate of an nMOSFET (pMOSFET) device at room temperature.

As was discussed in chapter 3, the V_{fb} of La_2O_3-gated MOSCAP shifted in the positive or negative direction depending on the magnitude of the applied stressing voltage (low or high gate voltages). This electric field-dependent Vfb shift was also observed on the Vth shift of W-La_2O_3 gated nMOSFET and pMOSFET devices. Figure 4.1 shows the drain current Id versus gate voltage Vg plot (Id-Vg) for W-La_2O_3 gated *nMOSFET before and after a positive CVS* (1V, 1.5V, 2V). Drain voltages of V_d = 0 V and 100 mV were used for all samples during the stressing and Vth measurements respectively. The very simple polarization scheme during CVS is shown as the inset in

fig. 4.1A. We can see that at the lowest CVS= 1 V, the Vth shifts towards negative direction proportional to the duration of stress (labeled in the plot as injection charge density Qinj, ranging from 200μC/cm^2 to 800 mC/cm^2). When a CVS= 1.5 V is applied (fig 4.1B) to the gate of the transistor, the shift in Vth continues to increase in the negative direction but is not as pronounced as in the former case.

Interestingly, when a soft-breakdown (SBD or SBKD) event occurs during the stressing of the device, the Vth shifts to the opposite direction and the final Vth of the device increases drastically. The evidence for the occurrence of SBD events can be seen as tiny jumps in gate leakage currents (without fatalistic HBD) during CVS measurements. You can refer to figure 3.18B in chapter 3 to differentiate a SBD from a HBD event.

When a higher voltage of 2 V is applied during a CVS, the V_{th} shifts to the expected direction, that is, to more positive values since during a positive CVS, the trapping of electrons into La_2O_3 (and its top and bottom interfaces) are expected to induce a positive increase in Vth. This is shown in fig. 4.1C. The general trend for all these V_{th} shifts is in good agreement with the results obtained for W-La_2O_3 gated MOSCAP, where a similar electric-field dependency on Vfb shift was detected as well. It should be noted that the subthreshold slope Ss of all Id-Vg curves did not change before or after stress for any voltage condition, thus suggesting a constant Ss.

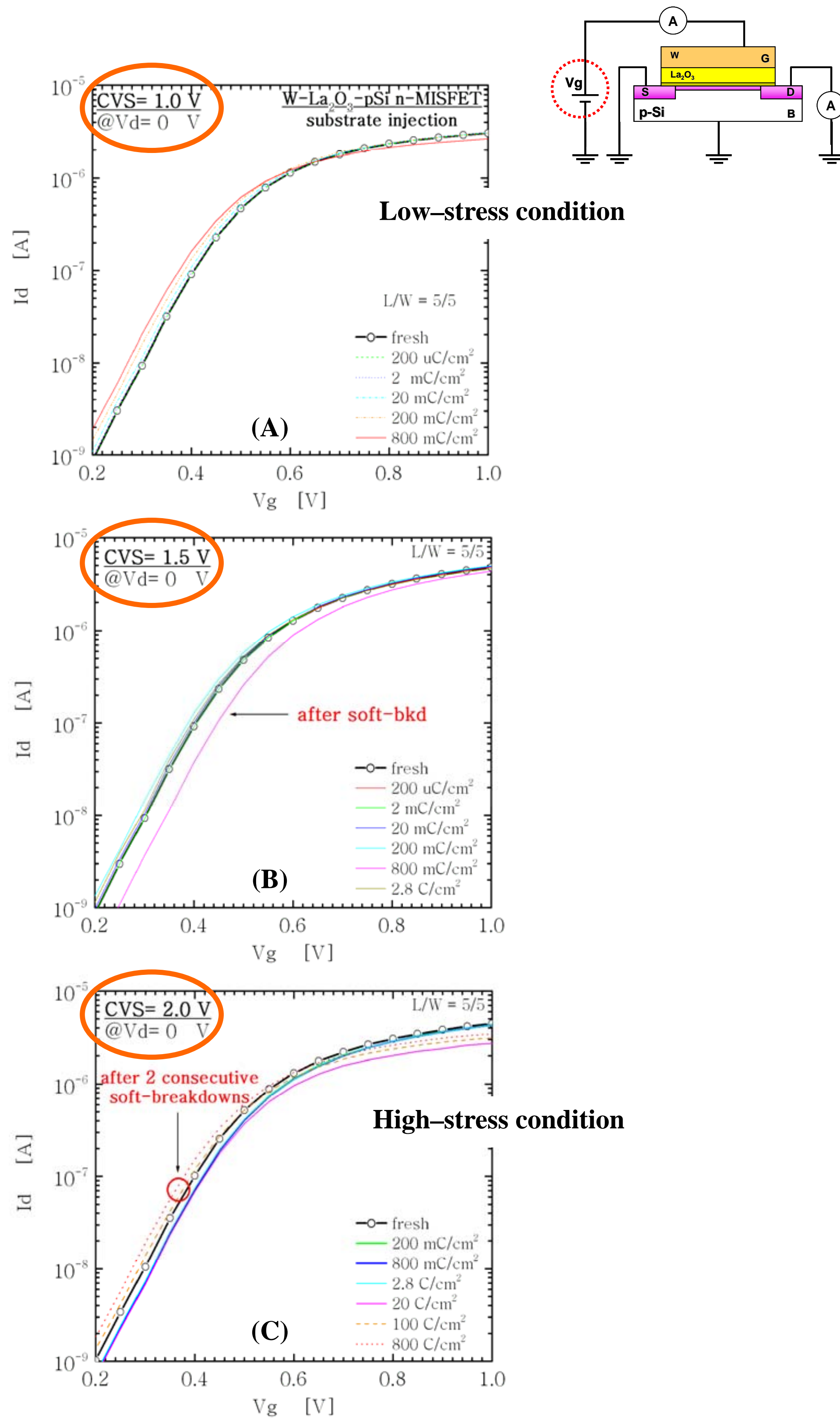


Fig 4.1 (A) ΔVth after CVS= 1V. Vth totally shifts to the left side in proportion to injected charge Qinj.
(B) ΔVth after CVS= 1.5V. Vth continues to shift to left side until a SBD event takes place.
(C) ΔVth after CVS= 2V. Vth increases to more positive values until SBD events changes this trend.

The former results shown in fig. 4.1 are now plotted again in a more standard form without showing the effect of SBD events on Vth for the sake of simplicity. The following plot represents the trend that Vth follows as the voltage intensity of CVS increases from low to higher stress conditions.

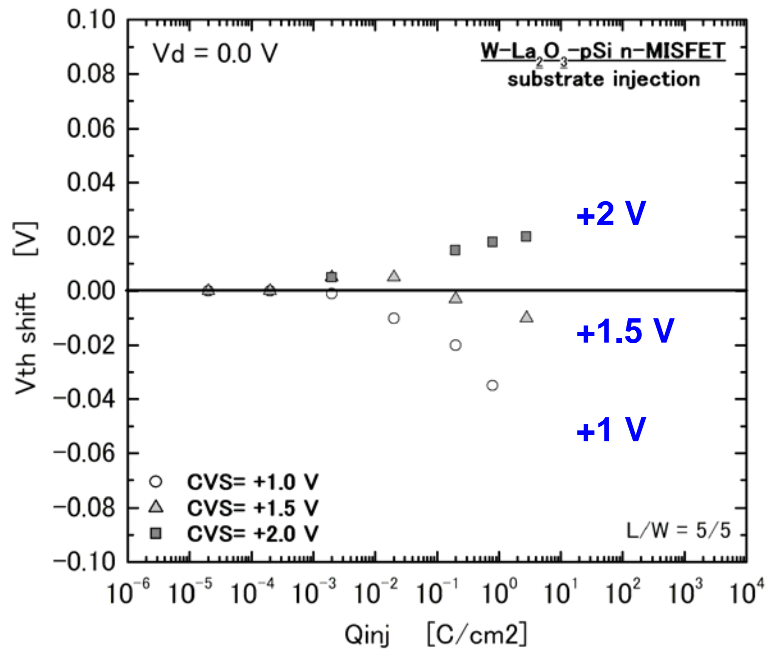


Fig. 4.2 Vth shift versus injected charge density (Qinj) for W-La_2O_3 gated *nMOSFETs* after various positive stressing CVS conditions.

For W-La_2O_3 gated pMOSFETs, the ΔVth after negative CVS became more negative than the initial state in both low and high-stressing conditions, see fig. 4.3. A positive/negative CVS is applied to the gate of nMOSFETs/pMOSFETs in order to induce strong inversion and therefore, the channel in both types of transistors. Figure 4.3 shows the Id-Vg plot for W-La_2O_3 gated ***pMOSFET before and after a negative CVS*** (-1.5V, -2.0V, -3.0V). Drain voltages of V_d = 0 V and -100 mV were used for all samples during the stressing and Vth measurements, respectively.

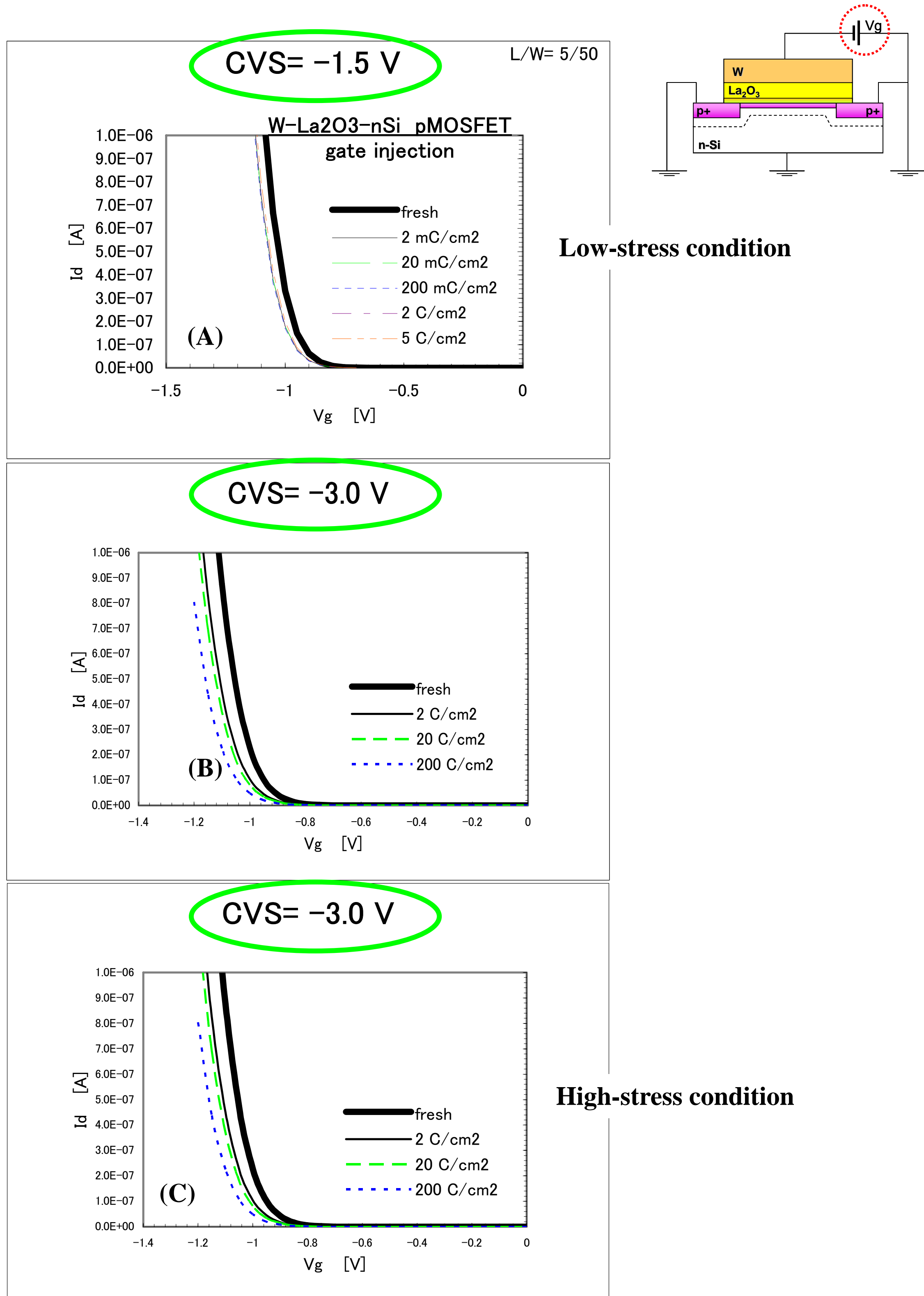


Fig 4.3 (A) ΔVth after CVS= -1.5V. Vth totally shifts to the left side in proportion to injected charge Qinj.
(B) ΔVth after CVS= -2.0V. Vth continues to shift to left side as expected for pMOSFETs.
(C) ΔVth after CVS= -3.0V. ΔVth gradually increases during this higher CVS condition.

Again, a very simple polarization scheme during CVS is shown in the inset of fig. 4.3A. At the lowest CVS= -1.5 V, Vth shifts towards negative direction proportionally to the duration of stress or injected charge density. Since the application of a highly negative gate voltage to the gate of this PMOSFET induces a p-type channel and most of the trapped carriers at the La_2O_3 and its interfaces are holes (which are detected as the majority carriers within the total gate leakage current), this trend of Vth shift after stress is then expected.

When a CVS= -2.0 V is applied (fig 4.3B) to the gate of the transistor, the shift in Vth still occurs in the negative direction thus increasing the magnitude of Vth with stress. This stressing condition produces almost the same electrical results as in the lowest-stressing conditions formerly discussed. Even though higher amountss of charge (Qinj) are injected into La_2O_3 compared to the former case, the shift in Vth seems to be at almost the same rate. For the case of CVS= -3.0 V, higher amouints of Qinj are injected into La_2O_3 because a higher density of leakage current is flowing through the oxide. Because of this higher stressing condition, the shift in Vth is more severe as seen by the more pronounced Id-Vg curve's moving to the left direction in the graph. In conclusion, we observed that a monotonous increase in Vth is proportional to injected charge density (Qinj) and which is obtained as a result of negative CVS. Interestingly, no observation of any SBD event was detected during the CVS measurement for pMOSFETs, so that the change in the direction of ΔVth after a SBD event could not be demonstrated as in the case of nMOSFETs stressed with a positive CVS.

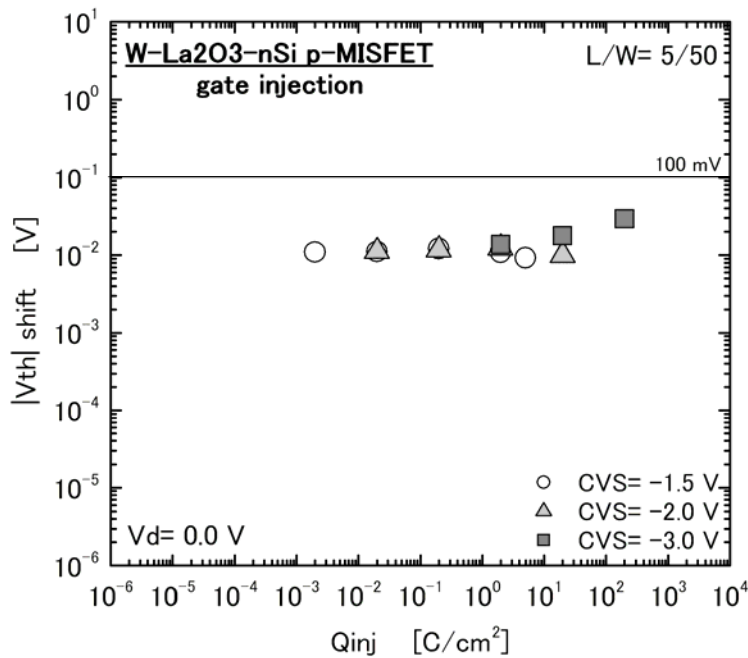


Fig. 4.4 Vth shift versus injected charge density Qinj for W-La_2O_3 gated *pMOSFETs* after low to high negative stressing CVS conditions.

Figure 4.4 shows a log-log plot of the data presented in fig. 4.3 by introducing the absolute value of the calculated Vth's. We can see that independently of the magnitude of CVS, all measured samples immediately produced a large shift in Vth even after the first injection of charge, and all subsequent shifts were always into the negative direction. The initially large ΔVth ~ 10 mV was kept almost constant for the samples stressed with low CVS (even after higher densities of Qinj) and gradually increased with injected charge for the sample stressed with higher CVS. It is important to notice that even with larger CVS, which are able to produce significant shifts in Vth, the final Vth measured after the largest injection of charge was kept always below ΔVth =100 mV. This is a very important result since these La_2O_3 films are intended to be applied for devices with gate voltage polarizations of 1 V or less, so that even lower

shifts in Vth can be expected.

4.2.1 Influence of Vth shift on drain current Id

In the previous parts of the dissertation, we have only presented Id-Vg and ΔVth results for n- and p-channel MOSFETs with a stacked W-La_2O_3 gate structure. In this section, we will present the effect that ΔVth has on the drain current of the MOSFET devices under evaluation. In order to get a clearer picture of degradation with stress for the W-La_2O_3 stack and its influence on MOSFET electrical characteristics, all 3 Id-Vg plots in figure 4.1A, B and C, where the same stressing conditions were applied, are reviewed. Figure 4.5A shows Id-Vd plot for W-La_2O_3 gated nMOSFET before and after a positive CVS under low CVS= 1V. We can see that for all densities of injected charge (Qinj), the drain current in saturation (Idsat) increases well above the value in its fresh state and this effect is more visible when greater gate voltages (Vg) are applied. Remember that CVS is the constant gate voltage applied during the stressing of the device and it can be sustained for as long (as much damage) as you want to induce into the device. The increase in Idsat after stress comes by recognizing that once Vth has been shifted to positive direction or less Vth values for nMOSFETs, then the amount of Id for a same range of Vg increases proportionally. This is schematically depicted in figure 4.6. Because of the logarithmic dependence of Id on Vg, even the slightest shift in the Id-Vg curve (caused by electrical stress) will cause ΔId greatly to increase or decrease (in accordance with the direction of ΔVth) in the same range of gate voltage ΔVg evaluated.

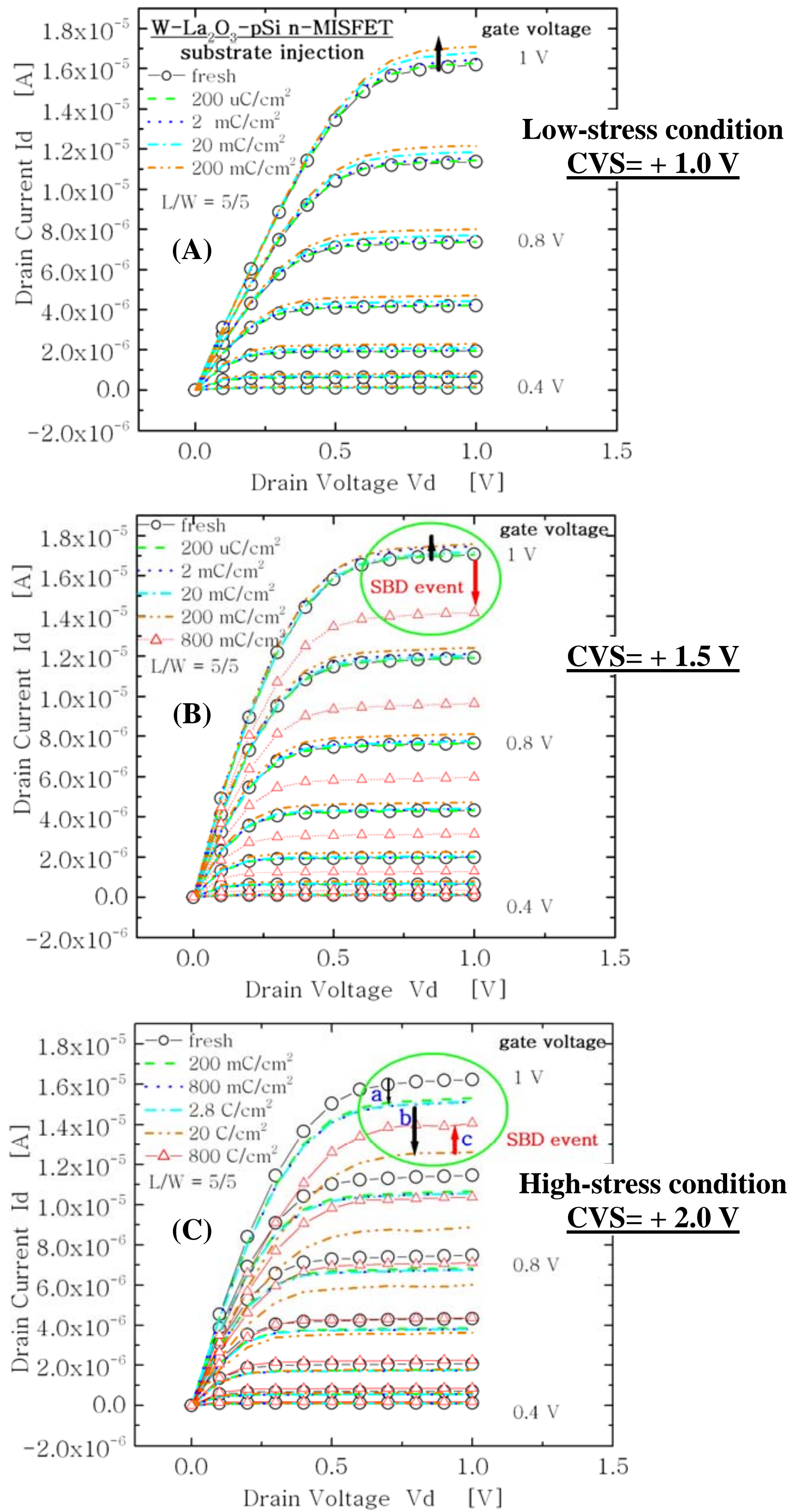


Fig 4.5 (A) Id-Vd plot for W-La_2O_3 gated nMOSFET before and after a positive and relatively low CVS.
(B) Id-Vd plot showing the effect that a SBD event have on the drain current Id.
(C) Id-Vd plot with the expected trend in Id under high-stressing conditions and the effect of SBD.

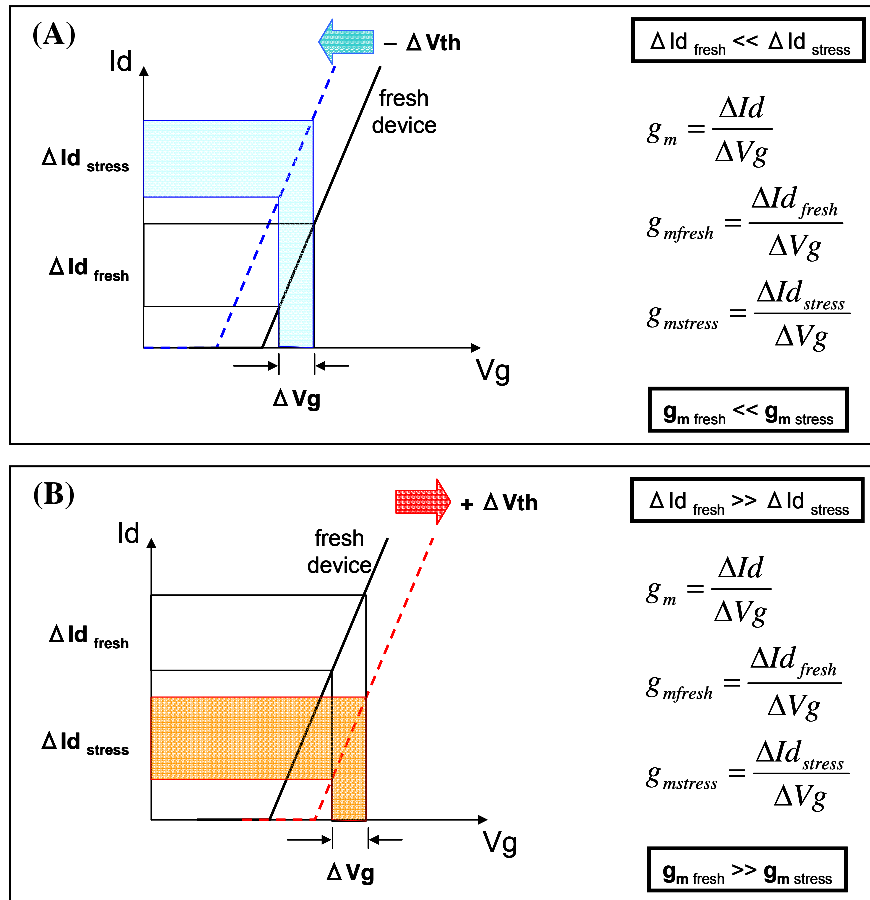


Fig 4.6 (A) Simplified Id-Vg diagram showing the effect of negative ΔVth after stress.
(B) Simplified Id-Vg diagram showing the effect of positive ΔVth after stress.

Figure 4.5B shows the result of stressing La_2O_3 with a slightly higher CVS. Here it must be noted that Idsat increases at the initial stage of stressing with the smaller densities of injected charge. For a higher Qinj= 800 mC/cm^2, however, a SBD event was detected during the stressing of the oxide (which is seen as a tiny jump in gate leakage current on an I-t curve) and the corresponding effect was initially detected as a change in the direction of ΔVth (see fig. 4.1B), from negative to positive direction. From fig. 4.6B, a positive shift in Vth after stress will cause decrease in Id of the stressed device and this is exactly what is clearly observed for the Idsat once the SBD

event appears. All stages initial increase and latter reduction in Idsat (after SBD) during the injection of charge are indicated by a circle shown in fig. 4.5B and they were taken for the highest Vg condition during the Id-Vd plot.

The above case is quite interesting that represents the highest stressing condition used for these samples CVS= + 2.0 V, and this means that a higher density of injected charge (higher damage since a higher density of leakage current is flowing through the oxide) will cause La_2O_3 to present faster changes in its electrical characteristics, which are difficult to visualize when stressing with lower CVS. All stages of Idsat variations with injected charge are indicated by a circle in fig. 4.5C and there we have three different Idsat behaviors which were labeled as a, b and c. In the first stage (a), the reduction in Idsat comes by the positive shift in Vth once the first and low densities of charge are injected. In the (b) stage, Idsat further decreases as a result of a larger injection of charge and this effect will cause a severe reduction in the transconductance. Interestingly, an even larger density of charge (a longer time for the flow of leakage current) injected into the gate oxide will cause a SBD event which, as was explained before, changes the direction of ΔVth to the opposite side (from positive to negative direction) and consequently, a change in the previous trend for Idsat. The Idsat then reverses its original tendency to decrease with stress and increases significantly as it is shown in the (c) stage. This stress-induced recovery of Idsat to its original value would increase gm but other different electrical characteristics like mobility and interface-state density are thought to get worse once a higher density of charge has been injected into the gate oxide. This is a topic that needs further investigation since the reduction of subthreshold drain currents is very important for

the design and implementation of ultra-low power devices. If a MOSFET is biased at or even slightly below Vth, the drain current Id is not zero. The subthreshold current Idsub may add significantly to power dissipation in a large-scale integrated circuit in which millions of MOSFETs are used. The circuit design must include the appropriate Idsub or ensure that the MOSFET is biased sufficiently below the Vth in the "off" state. However, and since we now are able to detect the changes in drain current which are promoted by positive or negative ΔVth (and both of them as a consequence of injected charge density), the decrease or increase in Idsub by electrical stress must be further investigated in order to predict its changes with time or charge and then include appropriate models for more accurate CAD representation of devices containing La_2O_3-based oxides.

4.2.2 Influence of drain voltage on Vth shift

This section presents the results of stressing W-La_2O_3 gated nMOSFETs with both a positive CVS at the gate of transistors and also a drain voltage Vd during the stressing measurement simultaneously. The electrical polarization for this condition is schematically pictured as follows.

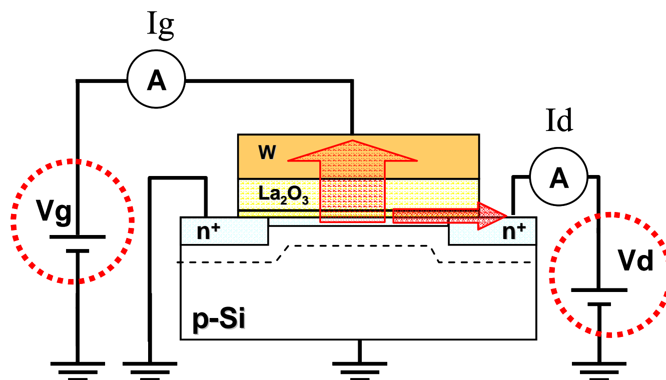


Fig 4.7 Schematic of nMOSFET with both Vg and Vd polarization during CVS. The total gate leakage current Ig is now reduced in proportion to Vd.

The main difference of this stressing condition with respect to those presented in previous sections is the presence of an additional source for oxide degradation by applying drain voltage (Vd). Since the total gate-leakage current (Ig) flowing through the oxide is now reduced in proportion to the magnitude of Vd, we would think that the damage induced into La_2O_3-IL is also reduced. However, even though the bulk damage into La_2O_3 could be reduced by this reduction in Ig, the flow of electrons through the surface of the channel towards the drain now induces additional damage by increasing the density of interface-state and thus, the creation of more sites for the trapping of carriers with stress. This phenomenon could be quite similar to that produced by hot electrons in what is so called "hot-carrier injection" effect [1] if the magnitude of Vd is high enough.

As the drain-to-source voltage (Vds) increases, the electric field in the space charge region at the drain increases. At high electric field, electron-hole pairs can be generated in the space charge region by impact ionization. The generated electrons tend to be swept to the drain and generated holes swept into the substrate for the nMOSFET device. Some of the electrons generated in the space charge region are attracted to the La_2O_3-IL stack due to the electric field induced by a positive Vg; this effect is shown in fig. 4.8. These generated electrons have energies far greater than the thermal-equilibrium value and are called hot electrons. If the electrons have energies on the order of 1.5 eV, they may be able to tunnel into the oxide stack. A fraction of the electrons traveling through the oxide may be trapped, producing negative charge in the oxide and thus a positive shift in Vth (as was previously observed for W- La_2O_3-IL gated nMOSFET stressed with the highest positive CVS). The probability of electron

trapping is usually less than that of hole trapping; but a hot-electron induced gate current may exist over a long period of time, therefore the negative charging effect may build up. The negative oxide charge trapping will cause a local positive shift in Vth.

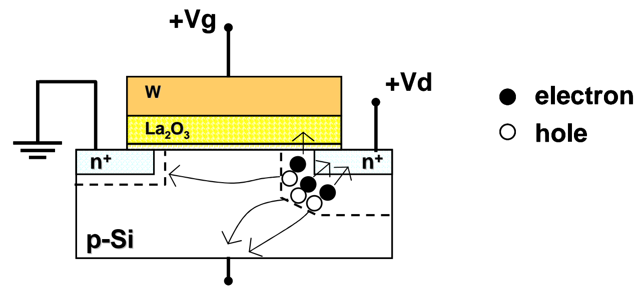


Fig 4.8 Hot carrier generation, current components, and electron injection into the La_2O_3-IL stacked oxide structure.

The energetic electrons, as they cross the Si-IL first interface (the next interface been that formed between La_2O_3-IL), can generate additional interface states. The probable cause of interface state generation is the breaking of silicon-hydrogen bonds (a dangling silicon bond is produced, which acts as an interface state). The charge trapping in interface states causes a shift in Vth, additional surface scattering, and reduced mobility. The hot electron charging effects are continuous processes, so the device degrades over a period of time. This degradation is obviously an undesirable effect and may tend to limit or reduce the useful lifetime of the device. On the other hand, the charge trapping in the second interface could lead to the breakdown of the IL, additional shift in Vth, additional surface scattering and reduction in mobility and thus, a still lower operational lifetime of the device.

Figure 4.9 presents the result of stressing W-La_2O_3 stacked nMOSFET with both Vg and Vd during positive CVS. Because of the low gate voltage used to stress the devices (CVS= + 1.0 V), Vth shifts in the negative direction for all samples.

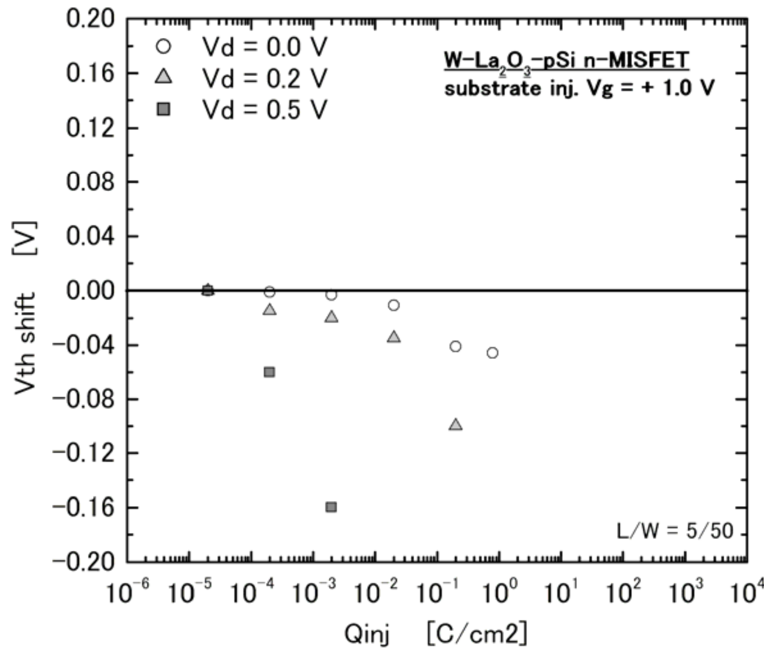


Fig. 4.9 Vth shift versus injected charge density Qinj for W-La_2O_3 gated *nMOSFETs* after both low positive CVS and Vd stressing conditions.

From fig. 4.9 and for Vd= 0 V (only a positive gate CVS is applied), the usual shift in Vth is observed. A gradual and proportional shift in Vth with injected charge density and which resembles that in fig. 4.2. Once Vd is applied during the stressing of the devices, the total gate leakage current is then reduced. Even though the damage induced in the bulk of the La_2O_3-IL stacked oxide by the direct flow of Ig is reduced, the additional damage induced by Vd increases the shift in Vth. Applying Vd at +0.5 V creates the largest shift in Vth even for the smallest densities of injected charge (this charge results by the integration of total gate leakage current with time). Fig. 4.10

shows the log-log plot of fig. 4.9 by using the absolute value of ΔVth.

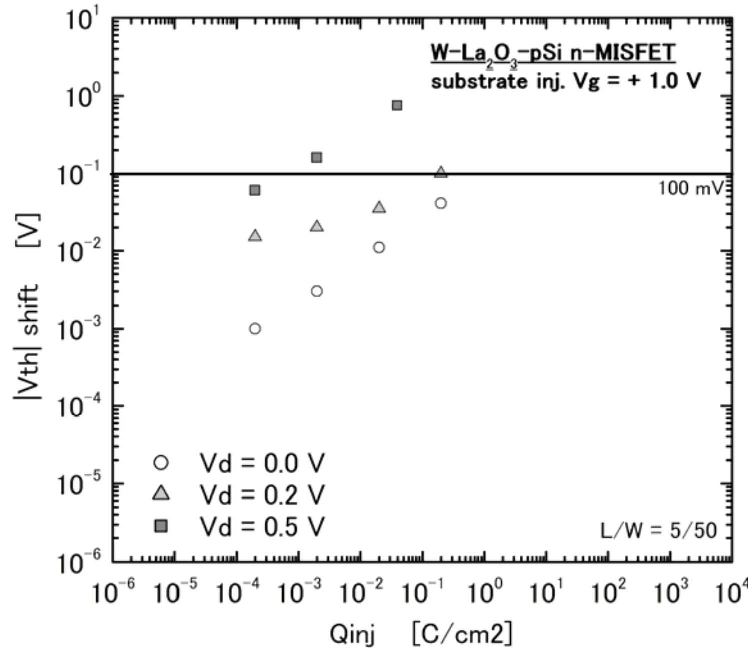


Fig. 4.10 Log-log plot of the data presented in fig. 4.9.

Even though Ig is reduced with increasing Vd (see fig. 4.11A), the damage induced by Vd greatly influences the final Vth of the stressed devices. It is interesting to observe that in literature, where too many reports exist indicating the reliability characteristics of SiO_2 and high-k based oxides during CVS measurements, the analysis and stressing of MOSFET devices under real operation conditions (V_{gate}, V_{drain}, V_{bulk}, frequency and temperature) is almost non-existent. Since the beginning, very popular and simple stressing conditions were used to obtain the reliability characteristics of conventional oxides. Negative/Positive Bias-Temperature Instabilities (NBTI/PBTI) for instance, stresses the gate oxides with both gate voltage and temperature, and the evaluated parameter (change in Vth) is always correlated to the

amount of stressing time or injected charge. Since the additional damage created by the inclusion of only Vd can worse the final electrical characteristics of La_2O_3-gated MOSFETs, it is quite important to include as much degradation-factors as possible when stressing these devices in order to get a more realistic projection of their operational lifetimes. Once all factors that contribute to electrical degradation are determined, they can be used to obtain more reliable models for lifetime projections and even propose enhancement techniques in order to increase reliability.

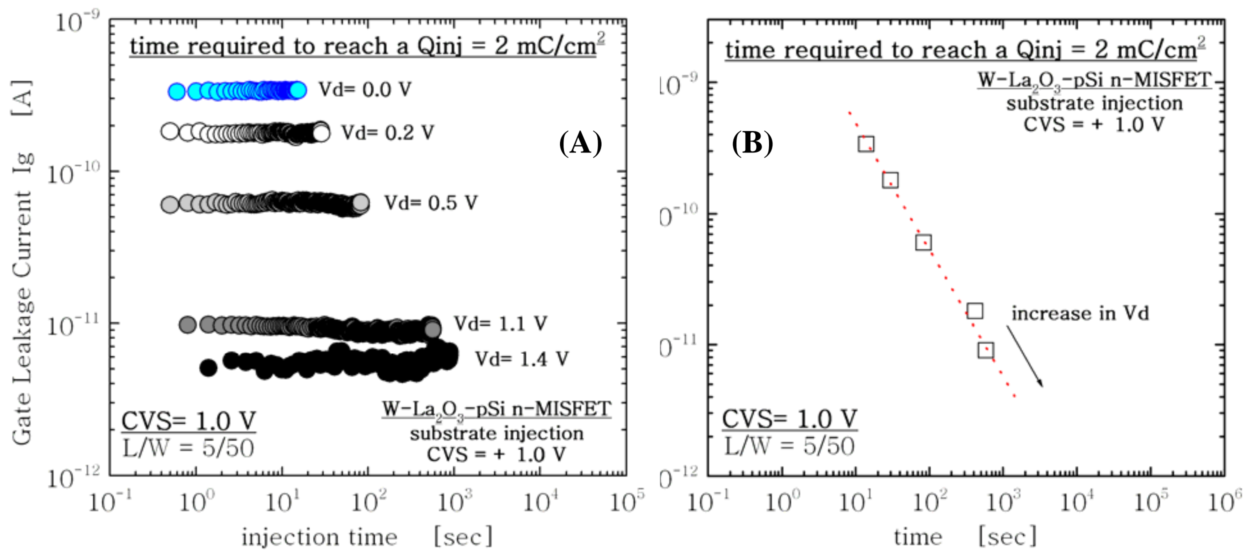


Fig. 4.11 (A) Gate leakage current Ig versus stressing time. Ig reduces in proportion to drain voltage Vd. (B) In order to reach the same injected charge density, more time is necessary for the sample with a decreased Ig (higher Vd). The final effect is a stronger dependence of ΔVth with Qinj.

Fig. 4.11A shows the decrease in gate leakage current Ig with respect to Vd. Since the shift in Vth is determined with respect to the density of injected charge (Qinj) at the gate of MOSFETs, fig. 4.11B shows that in order to obtain the same Qinj, more stressing time is needed when the applied Vd increases.

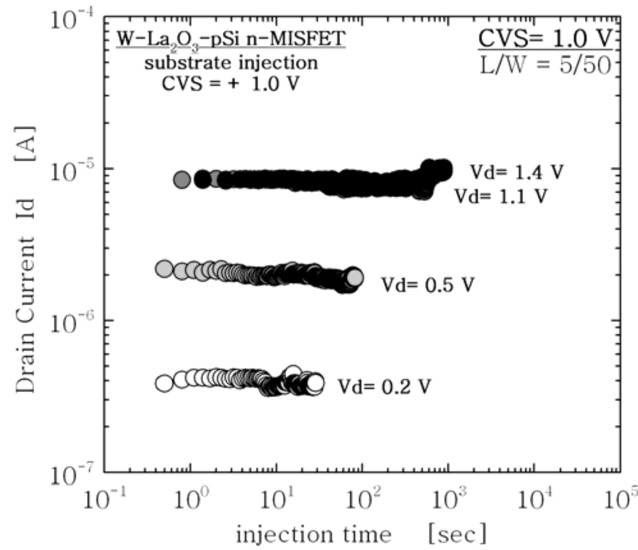


Fig. 4.12 Drain current Id increases with Vd until saturation occurs when the channel is cut-off at Vdsat (pinch-off condition).

We have chosen to correlate Vth shift with respect to Qinj instead of stressing time for a very important reason. Even with similar MOSCAP/MOSFET devices (which have undergone the same fabrication processing and which belong to the same die area); there exist several magnitudes for the density of leakage current when several devices are compared. This lack of reproducibility in the electrical characteristics of some of the devices makes necessary to stress several dozens of them until a relatively enough population of devices with similar fresh-electrical characteristics (densities of leakage current, Vth, Id-Vg, Id-Vd, etc) can be gathered for stressing measurements. Even with more closely similar characteristics for the resulted devices, the slight variation in, for instance, their gate leakage currents, results in larger variations in their final time to breakdown. We have detected that higher Ig leads to shorter tbd and vice versa. By using injected charge instead of stressing time as the parameter under which the device's characteristic can be correlated, these variations in

the leakage current can be minimized since the injection of charge results by the integration of leakage current with stressing time. This helps us to obtain more reliable data for more accurate lifetime projections.

4.3 Interface-state density (Dit) measurement after stress

In the previous section, we have presented the effect of electrical stress on the MOSFET Vth characteristics. Thanks to the MOSFET structure, we can measure interface trap densities using the charge pumping technique discussed in chapter 2. Charge pumping (CP) is a convenient tool to study defects produced into the gate oxide of MOSFETs under electrical stress [2]. Because of the MOSFET structure, we can measure interface-state densities (Dit) on small geometry MOSFETs instead of large-diameter MOSCAPs where the density of extrinsic defects could overcome the density of intrinsic defects and thus, screening the initial density and growth of stress-related defects. A very simple schematic of the CP technique is shown in fig. 4.13.

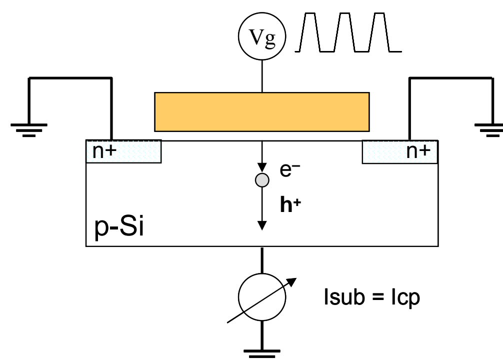


Fig. 4.13 Schematic of the charge pumping (CP) technique. CP is able to measure interface trapped charge by sweeping out through the substrate as Isub=Icp.

Fig. 4.13 shows the measurement circuit diagram of a CP test. The gate electrode of a MOSFET device is connected to a pulse generator, and then a reverse bias is applied to the source and the drain (Vds, not shown in the figure), while the substrate current Isub is measured. This current is caused by the repetitive recombination of minority carriers with majority carriers at the interface traps when the gate pulses the channel between inversion and accumulation. The method we used to measure Dit in our samples is called “Square Pulse Method”. The Square Pulse Method (SPM) extracts Dit by an iteration loop in which Isub=Icp is constantly measured for different pulse’s base and peak voltages. In SPM, a square pulse is applied to the gate, and the substrate leakage current is measured at the pulse’s peak voltages as shown in fig. 4.14.

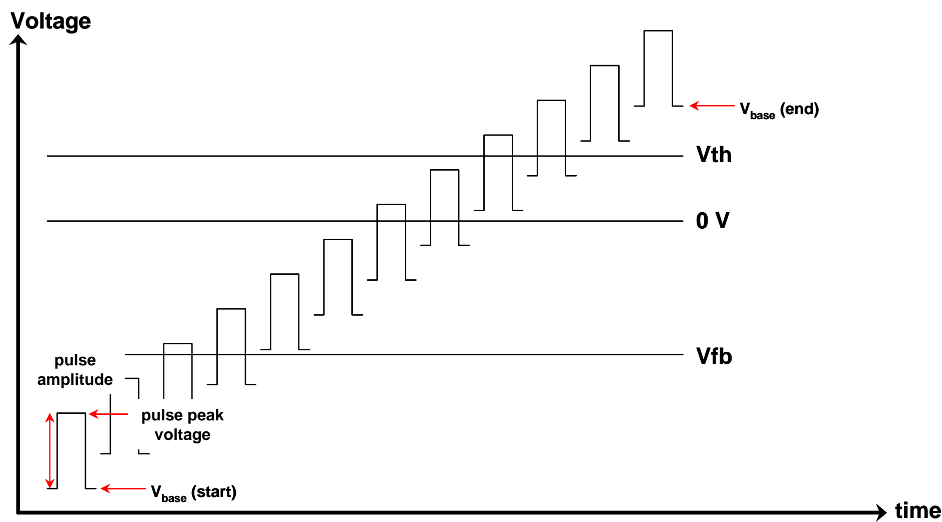


Fig. 4.14 Timing chart of square pulse method for CP measurement.

The amplitude of the square pulse is not changed, and the pulse base voltage (Vbase) is varied from well-below to well-above the threshold voltage (Vth) of the

measured MOSFET. The substrate leakage current is measured for each pulse base voltage. For every sampling measurement, the maximum substrate current is defined as the charge pumping current, Icp. The pulse base voltage is then increased with each iteration of the measurement loop. Then the charge pumping current Icp versus pulse base voltage Vbase curve is drawn. Dit is extracted from the Icp versus Vbase curve. The interface-states density Dit is extracted from the equation shown below.

$$\overline{Dit} = \frac{Icp}{f \times q \times Ag} \qquad (4.1)$$

where:

$\overline{Dit}$: mean interface-state density, averaged over the energy levels swept through by the Fermi level [$cm^{-2}\ eV^{-1}$]

Icp : charge pumping current [A]

f : pulse frequency

q : electron charge

Ag : channel area of the transistor

In this study, we used f = 100 kHz, Vds = -0.5 V and times of rise and fall of the pulse $tr = tf$ = 10 MHz. Fig. 4.15A shows the trend on Vth shift with respect to Qinj during a positive CVS measurement for ***<u>nMOSFETs</u>***. The log-log plot shows a linear relationship between these two parameters, indicating that Vth shifts in proportion to injected charge. On the other hand, the measurement of Dit after each CVS measurement results in almost no change for this parameter if the same log-log plot is used to present this data, see fig. 4.15B. It is thought that the origin of ΔVth for these nMOSFET devices is related to La_2O_3–bulk or to stacked La_2O_3-IL defect processes generated during stress since Dit showed almost no direct correlation to changes in Vth for the same densities of Qinj.

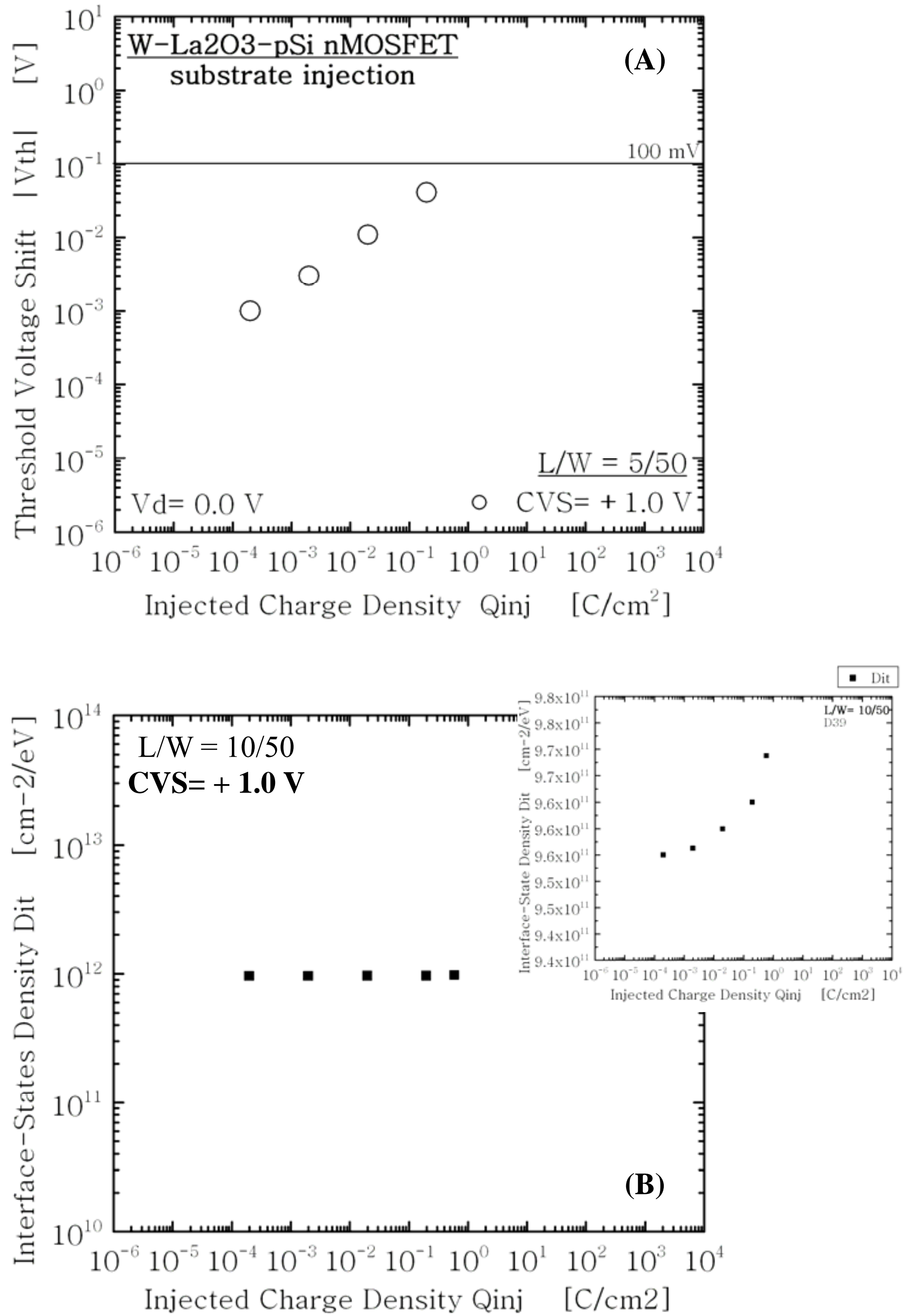


Fig. 4.15 (A) Log-log plot of ΔVth versus injected charge density Qinj for nMOSFET under positive CVS. A linear relationship between ΔVth–Qinj is observed in this plot.
(B) Interface-states density Dit measured at the maximum substrate current Isub after positive stressing measurements. A log-log plot shows no correlation of ΔVth with injected charge density. The inset shows a linear-log plot of the same data for comparison.

Another reason for the change in Vth could be directly related to the generation of positive fixed charge within the oxide stack since Vth shifts in the negative direction during low-stressing CVS conditions (see fig. 4.1A). The origin of the negative shift in Vth for low CVS conditions in nMOSFETs must be clarified but at this point, it is thought that Dit plays a minor role in this degradation phenomenon.

For the case of ***pMOSFETs*** we have a different scenario as shown below. The ΔVth vs. Qinj data previously presented in fig. 4.4 is again shown in fig. 4.16 together with the Dit results taken after each density of injected charge. Going back to the previous data (fig. 4.3), we note that since the shift in Vth for pMOSFETs was always in the negative direction irrespective of the magnitude of the CVS applied, we concluded that the injection of charge into the oxide stack was always positive. The origin of this positive charge is holes coming from the channel that connected to S/D and then flowing directly through the oxide into the gate by means of the electric field developed by the negative CVS. Since holes are heavier than electrons, they have a greater probability to get trapped in available trapping sites within the oxide or at its interfaces. Since a W-La_2O_3 stack tends to develop into a W/La-silicate/IL stacked structure after PMA at 500°C (being the SiO_2-based IL a new source of electrical defects for trapping of carriers), the trapping of heavy holes directly injected into the IL-Si interface could lead to higher Dit value. By looking into figs. 4.16–4.17, it is found that the same trend of ΔVth is followed by that in ΔDit after the same densities of injected charge. While both Vth and Dit are kept constant after low stressing conditions, higher CVS conditions slightly increases both Vth and Dit.

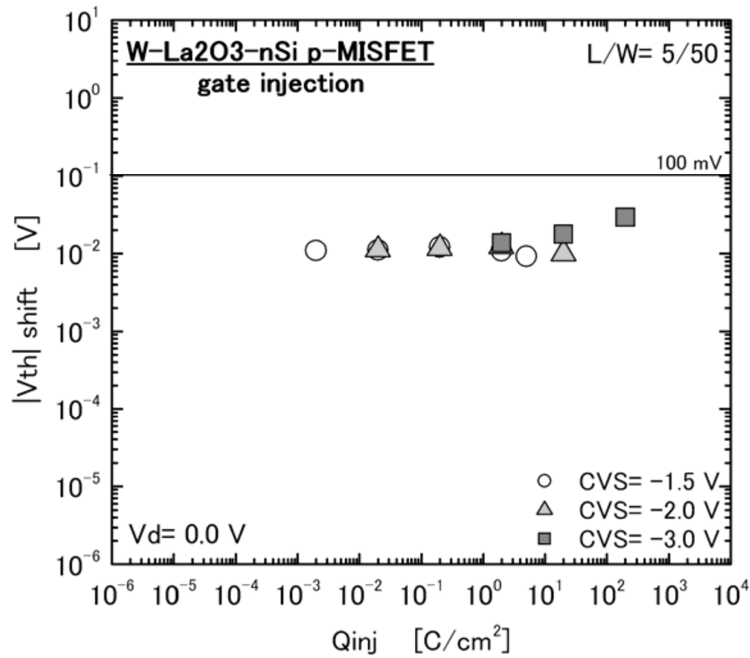


Fig. 4.16 Same data as presented in fig. 4.4.

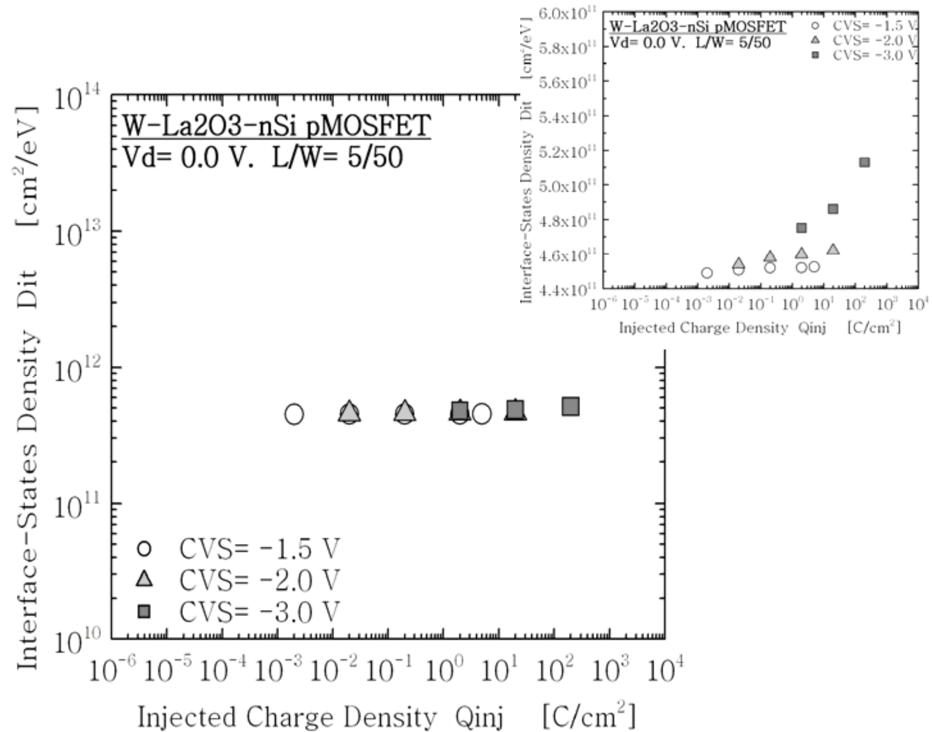


Fig. 4.17 Dit versus Qinj for pMOSFET after negative CVS. Independently of the CVS applied, the change in Dit after stress is almost constant. The inset shows a linear-log plot of these data for comparison purposes.

These results seem to indicate that after the injection and trapping of holes into the La_2O_3-IL stacked oxide, the shift of Vth with stress is somewhat related to the damage produced by the injection of these holes directly into the IL-Si interface, which in turn, increases the density of interface-states Dit. Fig. 4.18 shows the Dit vs. Vbase characteristic curve for the data presented in fig. 4.17 before and after negative CVS. For a same CVS applied, the increase in Dit with injected charge indicates that interfacial defects are produced under electrical stress, being the defect creation largely increased by a higher CVS.

In conclusion, for pMOSFETs, ΔVth seems to be related to increases in Dit after negative CVS. Nonetheless, after the first injection of charge, consequent ΔVth are lower at even higher Qinj as compared to nMOSFET stressed devices. It is thought that the physical origin for the increase in interface-state density (Dit) with electrical stress is related to the breaking of silicon-hydrogen bonds. On the other hand, it should be noted that PMA is important for the enhancement of reliability as well as the electrical characteristics of La_2O_3-gated MOS devices. Up to now, the PMA we have been using to do this has been done by using a dry-N_2 atmosphere. In order to further enhance the reliability characteristics of La_2O_3-gated devices, a forming gas (FG= 97% N_2, 3% H_2) PMA was carried out after the La_2O_3 deposition and tungsten metallization so that the initial density of dangling bonds at the IL-Silicon interface can be minimized. FG annealed pMOSFET devices were stressed with negative CVS and the changes in Vth as well as Dit with stress were measured. The results are shown in fig. 4.19.

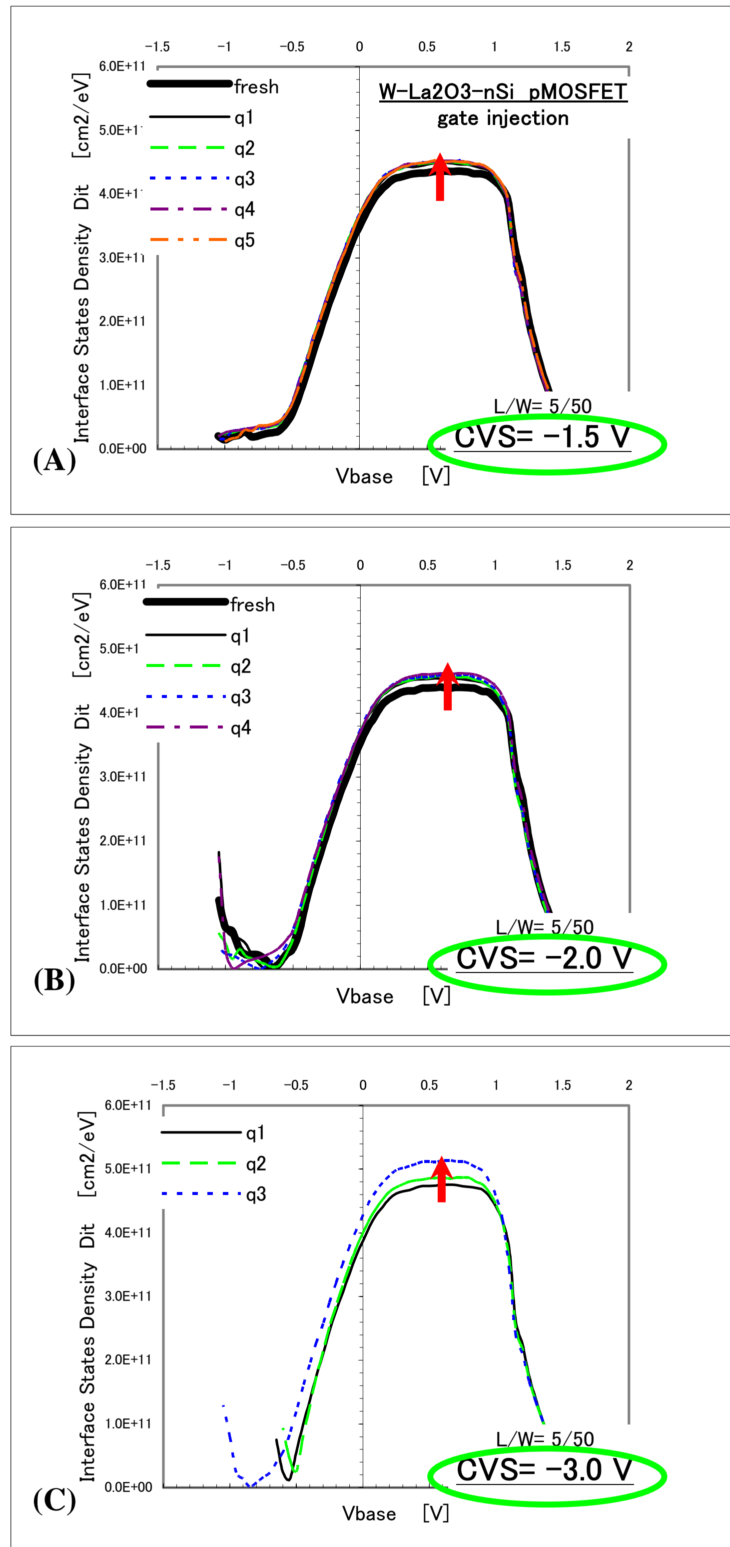


Fig. 4.18 (A) Dit versus Vbase plot for W-La_2O_3 gated pMOSFET after negative CVS= -1.5 V.
(B) Dit versus Vbase plot for W-La_2O_3 gated pMOSFET after negative CVS= -2.0 V.
(C) Dit versus Vbase plot for W-La_2O_3 gated pMOSFET after negative CVS= -3.0 V.

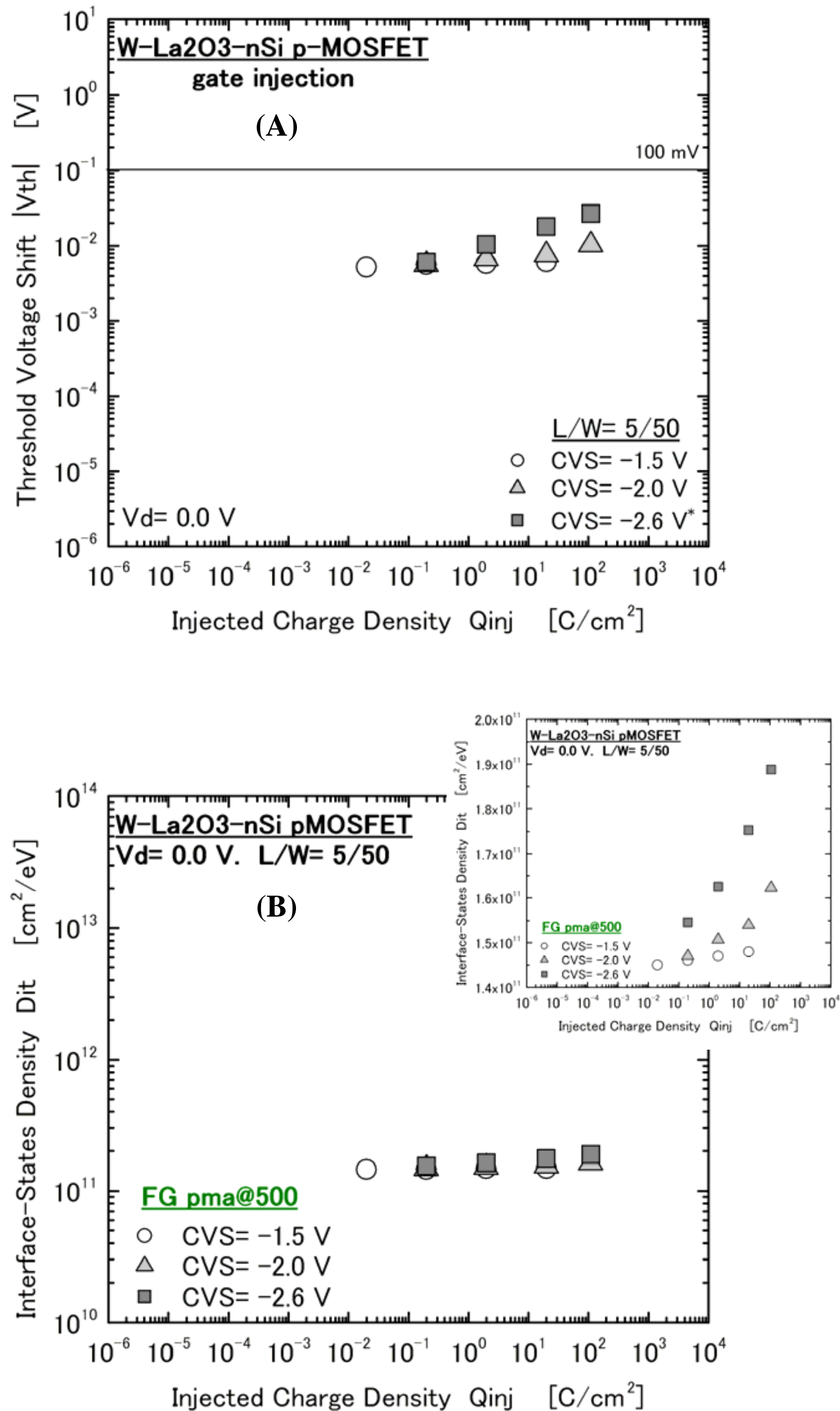


Fig. 4.19 (A) Log-log plot of ΔVth versus Qinj for pMOSFET under negative CVS and FG-based PMA. As before, identical behavior for these pMOSFETs is obtained but the initial levels of Vth are slightly lower than those found in N_2-based PMA devices.
(B) A log-log plot of Dit vs. Qinj after stress shows lower levels of Dit as compared to those found in N_2-based PMA devices. It is thought that FG-based PMA is able to reduce the initial density of dangling bonds so that lower changes in Dit with stress are obtained.

Fig. 4.19A shows ΔVth versus Qinj for FG-based PMA pMOSFET devices. Lower ΔVth and ΔDit before and after negative CVS are obtained by FG-based PMA at the same temperature. As before, an identical trend in Vth shift after negative CVS has been found but the initial levels of Vth are slightly lower than those found in N_2-based PMA devices. On the other hand, Dit is kept almost constant but here, lower levels of Dit are found as those compared to N_2-based PMA devices. It is thought that FG-based PMA is able to reduce the initial density of dangling bonds so that lower changes in Dit with stress are obtained. Interestingly, improvements in the reliability of deuterium (D_2) annealed MOS devices have been lately reported. Compared with oxide stacks annealed in a forming gas containing hydrogen (H_2), the stack dielectrics annealed in D_2 ambient exhibit various advantages such as less charge trapping, less generation of interface state density (Dit), a larger charge-to-breakdown (Qbd), and longer time-dependent dielectric-breakdown characteristics under conditions of electrical stress [3]. The improved reliability can be attributed to the strength of the deuterium bond. This deuterium based PMA of high-k/IL stacked gate dielectrics has considerable potential for future use in ultra large-scale-integration devices so that it must be considered to further improve the reliability characteristics of Metal/ La_2O_3-based MOS devices.

4.4 Substrate injection versus gate injection degradation

Up to now, we have been using both types of gate voltage polarity for the stressing of La_2O_3-gated MOS devices. In the case of nMOSFETs and pMOSFETs, we

have made use of positive and negative CVS respectively in order to induce the inversion channel and thus separate the contribution of electrons and holes to leakage current. The measurement of both components is known as carrier separation measurement [4]. On the other hand, the importance of positive or negative CVS is more apparent when the energy band diagrams of the stressed stacks are analyzed.

Fig. 4.20 shows the electrical and energy-band diagrams for ***nMOSFETs stressed by positive CVS***. Since the use of tungsten as the gate electrode avoids the injection of holes directly into La_2O_3 from this metallic gate, only electrons are injected into the La_2O_3-IL stack and they are detected as gate leakage current Ig (with electrons being the major contributor to Ig). The origin of these electrons is the S/D regions that are connected by the channel when the inversion condition is reached, and this condition is called ***substrate injection*** since electrons are injected directly from the silicon substrate.

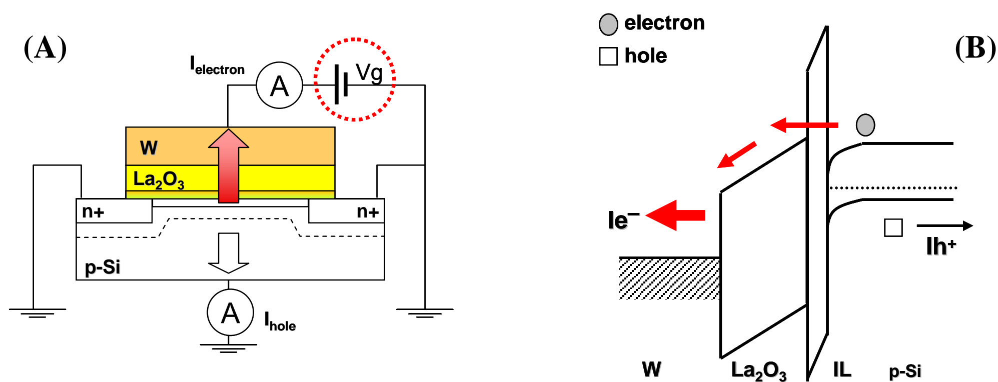


Fig. 4.20 (A) Schematic diagram showing nMOSFETs stressed with a positive CVS. The flow of both electrons and holes currents are measured at the gate and substrate respectively.
(B) The energy band diagram shows that positive CVS implies injection of electrons directly from the substrate (via the inverted channel) into the IL-La_2O_3 stacked structure.

Some of the injected electrons will tunnel through the stacked oxide and others will be trapped there thus degrading the nMOSFET characteristics in proportion to the intensity or timing of the stress. Because substrate injection conditions injects only electrons into the stacked oxide, this is then a very convenient stressing condition since the effect of only one carrier on the degradation and breakdown characteristics of La_2O_3 can be obtained. Therefore, substrate injection conditions or positive CVS on n-type silicon based MOSCAPs were extensively used in order to obtain the degradation and lifetime characteristics of La_2O_3, see chapter 3. From ΔVth versus Dit measurements, substrate injection of electrons resulted in both higher ΔVth and Dit (for the same densities on injected charge) compared to gate injection, compare figs. 4.15–4.16–4.17.

On the other hand, fig. 4.21 shows the electrical and energy-band diagrams for ***pMOSFETs stressed by negative CVS***. This stressing condition is quite different from the former in that electrons and holes are both injected simultaneously into the gate oxide. Because of the negative CVS, electrons are injected directly from the metallic gate into the oxide and this condition is called ***gate injection***. From carrier separation measurements, it will later be shown that the major contributor to leakage current under gate injection condition is the injection of holes via the inverted channel. From fig. 4.21, the simultaneous injection of both carriers into the La_2O_3-IL stack is observed. The origin of electrons is the gate voltage source while that of injected holes is the inverted channel after a sufficiently negative CVS is applied to the gate of these pMOSFET devices. Since substrate injection of electrons can severely degrade the MOSFET characteristics as compared to gate injections, the enhancement of devices

stressed under positive CVS has therefore a priority importance over those with negative CVS.

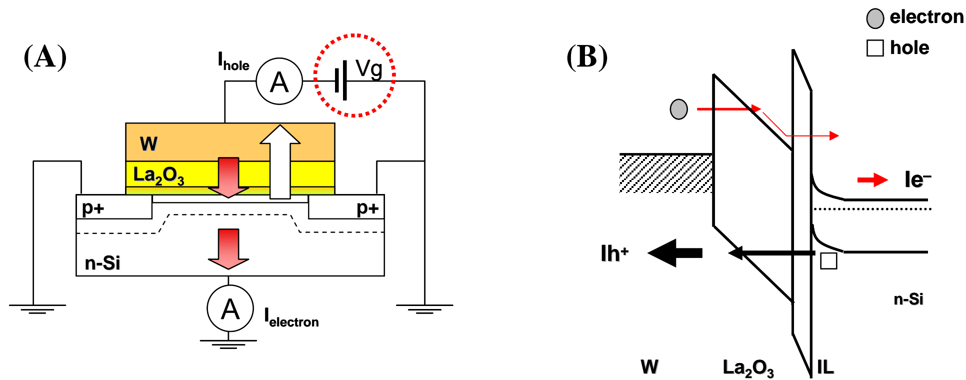


Fig. 4.21 (A) Schematic diagram showing nMOSFETs stressed with a positive CVS. The flow of both electrons and holes currents are measured at the gate and substrate respectively. (B) The energy band diagram shows that positive CVS implies injection of electrons directly from the substrate (via the inverted channel) into the IL-La_2O_3 stacked structure.

4.5 Carrier separation measurements

This section will show the effect of gate and substrate injection of electrons on the degradation characteristics of W-La_2O_3 gated MOSFET devices after PMA in N_2. Because of the MOSFET structure, the total gate leakage current flowing through the gate oxide can be separated into its two components: electron current and hole current. The identification of the major carrier contributor to leakage current can also help us to identity the major carrier contributor to the damage and consequent electrical degradation of the MOSFET characteristics with applied stress. A simplified carrier separation measurement methodology along with the contributions of electrons and

holes to Ig is again illustrated in fig. 4.22 for both nMOSFET and pMOSFET.

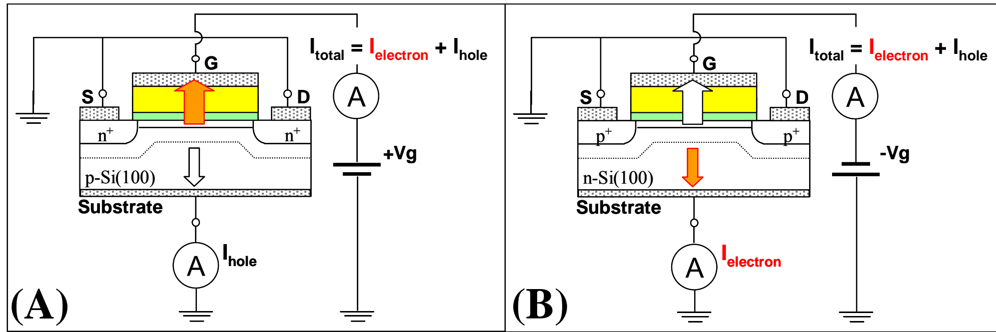


Fig. 4.22 (A) CS measurement for nMOSFETs in inversion (positive CVS). Both electron and hole current components are detected at the gate and substrate respectively.
(B) CS measurement for pMOSFETs in inversion (negative CVS). Even though both electrons and holes tunnel simultaneously through the gate oxide, only the hole current component is illustrated flowing through the oxide for clarity purposes.

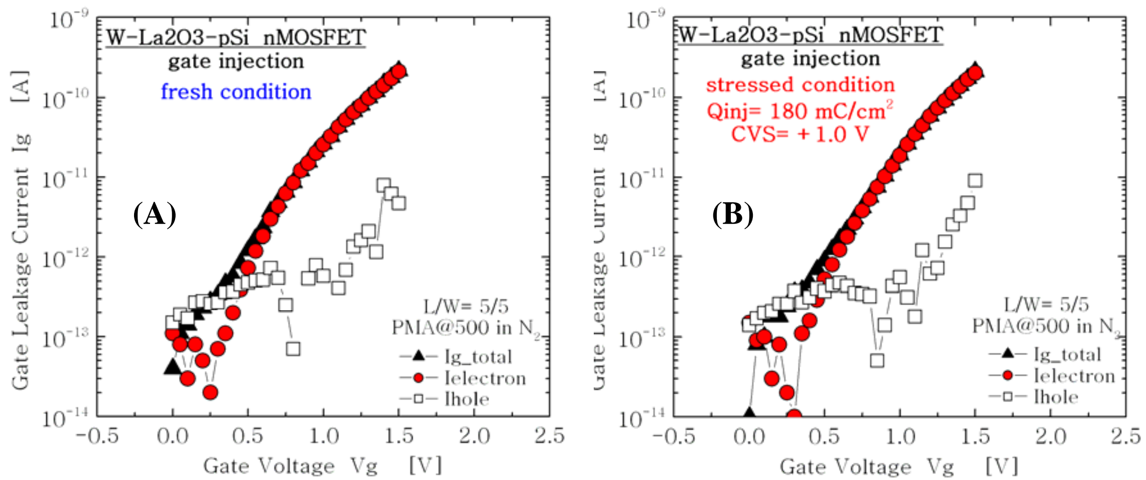


Fig. 4.23 (A) Ig versus Vg plot for nMOSFET before positive CVS (gate injection). After CS measurement, electrons were identified as the major contributors to gate leakage current.
(B) After positive CVS, the Ig-Vg shape remains almost unchanged. Because of the trapping of electrons at the bulk of La_2O_3, Ig gets slightly lower as compared to fresh condition.

Fig. 4.23A shows the result of ***CS measurements on nMOSFET*** before positive CVS. It is clearly seen that electrons are the major carrier contributors to leakage current where Vg > Vth. Once the same sample has been stressed with Qinj=180mC/cm^2, the contribution of electrons to Ig does not change and the resulting shape of the Ig-Vg is kept unchanged as in the fresh condition case. Note that the level of Ig for all currents was slightly lower than that compared before CVS. Since the use of higher ramping gate voltages (Vg= 0 to 1.5 V compared to CVS= 1.0 V) can create defects into the oxide for trapping of electrons, the trap of a single electron would increase the energy barrier at the trap site (within the energy band of La_2O_3 far from the interface IL or silicon) and thus, a reduction in Ig would be obtained.

When higher positive CVS is used, the probability of breakdown event (SBD or even fatalistic HBD) increases. By looking back at the data presented in fig. 4.1C, the initially positive trend in ΔVth changes to the opposite direction after a SBD event that is observed during the stressing measurement. From CS measurements shown in fig. 4.24-B-C-D, electrons are identified as the main component to Ig and thus, they are also the main contributor to degradation and trapping within the La_2O_3 and its interfaces. Since the trapping of electrons would shift Vth to positive direction, the trend of ΔVth for low Qinj (see fig. 4.24A) is now well correlated along with the CS data. Once a SBD event occurs during the stressing measurement, an increase in Ig is detected at the Ig-Vg plot seen in fig. 4.24E. More importantly, the occurrence of a SBD event inverts the polarity of the main contributor to Ig.

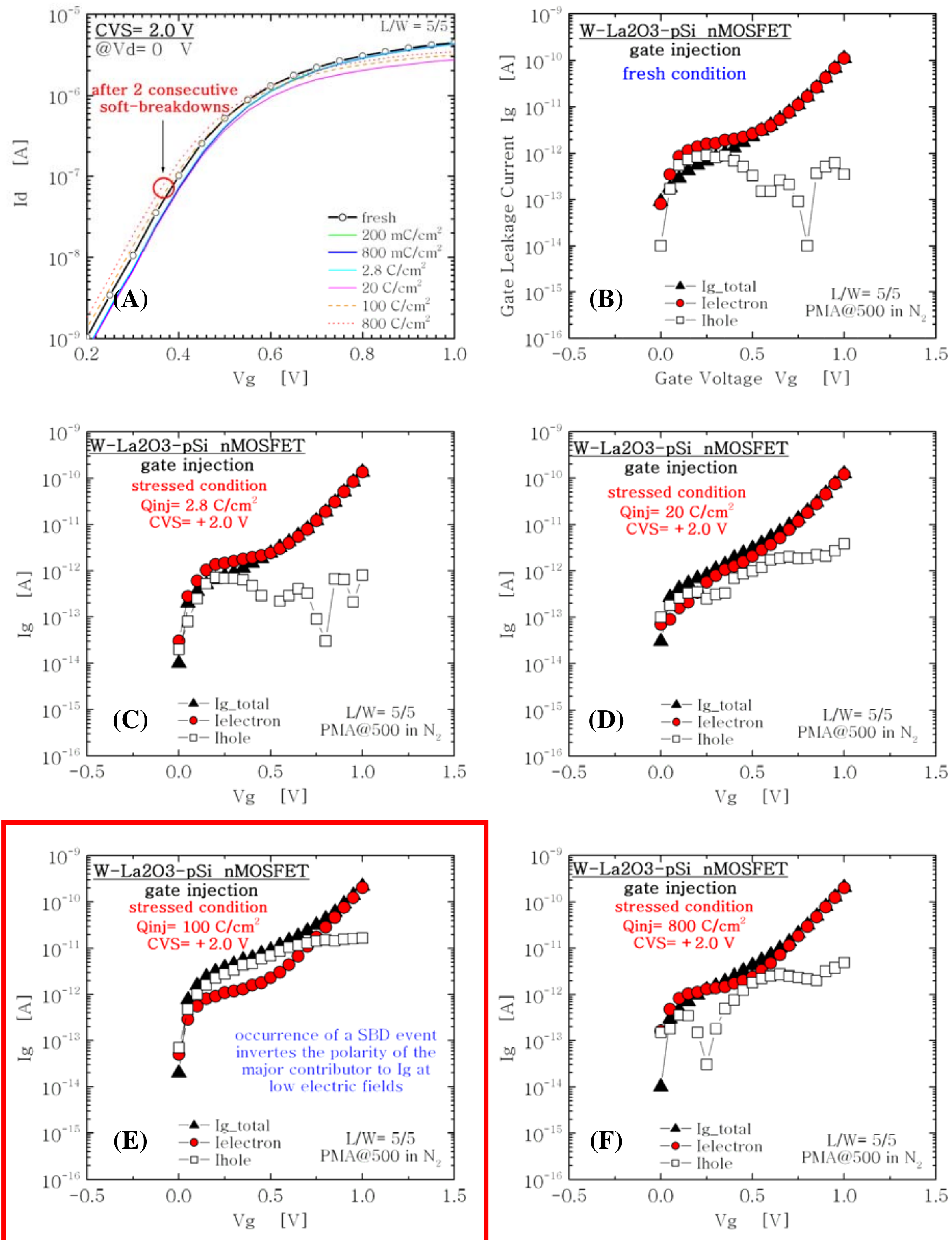


Fig. 4.24 (A) Drain current Id versus gate voltage Vg. Same as the data presented in fig. 4.1C.
(B)(C)(D) CS measurement for gate leakage current under positive CVS= +2.0 V. The electron current is the main contributor to total leakage current with Ihole increasing with Qinj.
(E) After a SBD event occurs, the main contributor to Ig changes from electrons to holes for low electric fields and the final effect can be seen as a net increase in Ig as well.
(F) After SBD event, Ielectron is still dominant though Ihole increases well above its fresh value.

Fig. 4.24E shows that after SBD, holes are now the main source for charge trapping within the La_2O_3-IL stacked oxide. From the Id-Vg plot, SBD event will ultimately change the direction of ΔVth because of the trapping of holes at low electric fields during the Ig-Vg plot. Finally, fig. 4.24F shows that after SBD, the electron component of Ig is switched back to the dominant position while the hole contribution has now significantly increased with respect to its fresh initial value.

On the other hand, since substrate injection of electrons can severely degrade the MOSFET characteristics as compared to gate injection, higher positive ramping gate voltages, until the oxide reach hard-breakdown (HBD) condition in an Ig-Vg plot, results in the development of several degradation steps within the La_2O_3-IL stack before and after this HBD event, see fig. 4.25. Initially, the higher contribution to Ig after inversion (from **a** point onwards) comes by the electron current component. Once the ramping voltage increases, degradation in the hole-current component occurs after **b** point. Just before HBD in **c**, the electron-current component also experiences a similar degradation characteristic observed for the hole current. This initial degradation then leads to HBD and all the currents (Itotal, Ielectron, Ihole) suddenly jump about three orders of magnitude above its pre-BKD values. Once HBD appears at the point indicated by the circle (**d**) shows the switching behavior or trapping-detrapping characteristics of the leakage current with ramping stress. Here, Itotal, Ielectron and Ihole components try to switch back to pre-BKD condition by dramatically showing a reduction in their current values compared to those obtained immediately after HBD. This trapping-detrapping process after breakdown could be related to the capture of a single electron within the insulator that causes a perturbation in the local injection field.

The leakage current continues to increase with Vg until a progressive breakdown (PBD) event is now detected at point e. The additional increase in post-breakdown gate-leakage current could be related to the increase in the total spot area of the leakage site that develops after breakdown. This concept was also analyzed in MOSCAP devices in chapter 3.

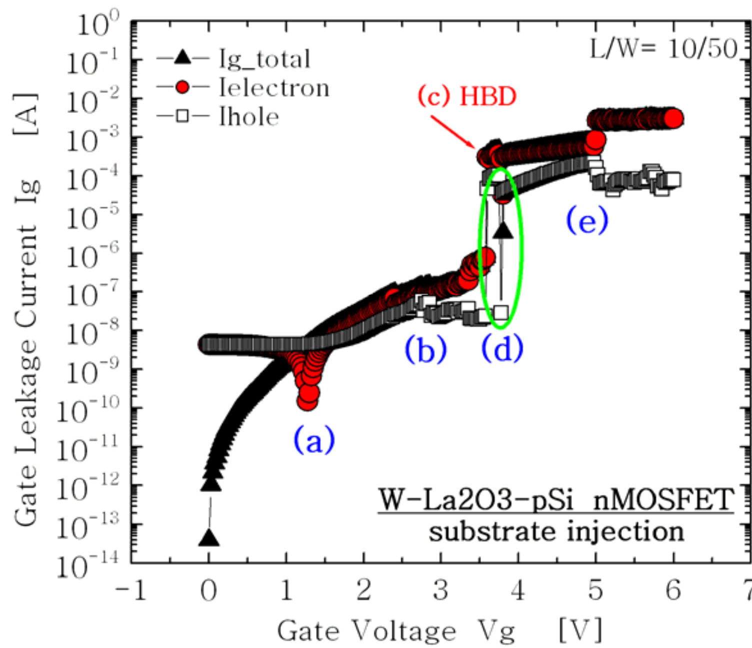


Fig. 4.25 Ig-Vg plot for nMOSFET with higher Vg ramping stress. Several degradation steps occur before and after fatalistic HBD event appear.

For pMOSFETs, the application of negative CVS (high enough to invert the silicon surface and create the channel) induces a leakage current that consists of both electrons and holes injected simultaneously into the oxide. Since the degradation and consequent breakdown of La_2O_3-IL structure is thought to be highly dependent on the polarity of the applied stress, *CS measurements on pMOSFET* before and after negative

CVS were also performed.

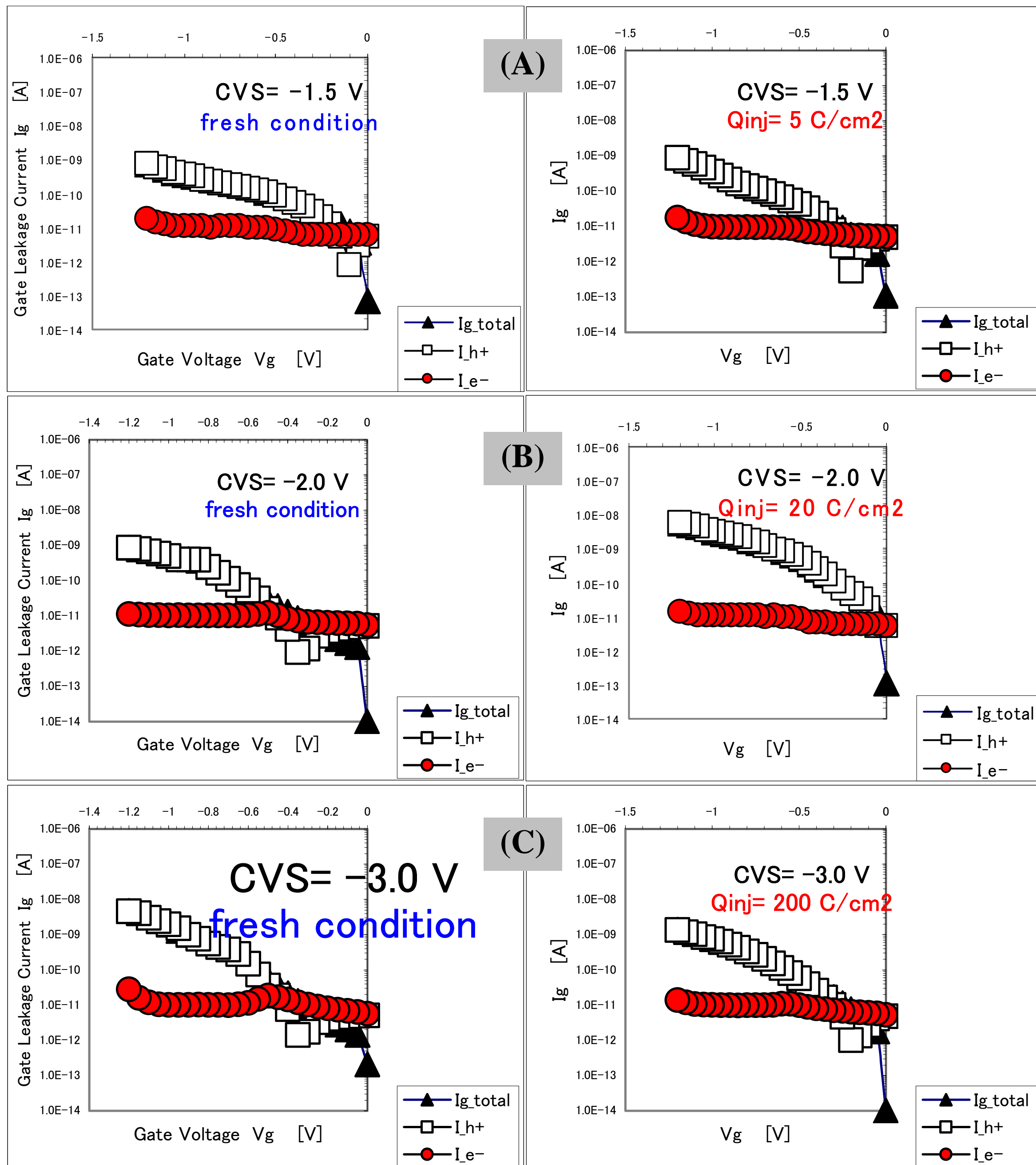


Fig. 4.26 (A) Plot of CS measurement of Ig vs. Vg before and after negative CVS for pMOSFET. The injection of a smaller density of injected charge did not change the major contributor to Ig.
(B) Holes still are the major contributors to Ig before and after negative CVS. The injection of a relatively higher charge density increases Ig compared to its fresh value.
(C) Similarly, at the higher CVS condition, holes are the major components of Ig after inversion of pMOSFET and the fresh levels of Ig increases after stress indicating hole trapping in the oxide.

Fig. 4.26A shows Ig-Vg plot before and after a negative CVS with low density of Qinj. The major contributor to leakage current is the hole-current component in a inversion state for all stressing conditions. Fresh and stressed Ig-Vg characteristics under low CVS conditions showed no significant change. When higher CVS is applied to the gate, see figs. 4.26 B-C, a higher density of leakage current flows and thus, a higher density of charge is injected into the oxide. Nevertheless, hole current is still the dominant component for oxide degradation under high stressing conditions.

Up to this point, the CS measurement technique has been used to determine the major carrier contributor to Ig in an Ig-Vg plot, where a ramping gate voltage is applied until the sample reaches certain degradation specifications or breakdown. Next, the results of CS measurements on the evolution of leakage current with time (I-t) after a constant voltage stress (quite common when TDDB measurements were performed to determine the lifetime of La_2O_3) are presented; see fig. 4.27 A-B. Fig. 4.27 A-B shows the evolution of both electron and hole current components with respect to stressing time under substrate and gate injection conditions for nMOSFET and pMOSFET structures, respectively. From this figure, we can see that the dominant carrier for gate leakage current changes from electrons for substrate injection to holes for gate injection condition. Also, it is clearly seen that depending on the polarization of the stress gate voltage, two different oxide-breakdown mechanisms will emerge. A W/La_2O_3-IL stack stressed under the substrate-injection condition will likely produce a two-step breakdown behavior as compared to the single step breakdown found under gate injection.

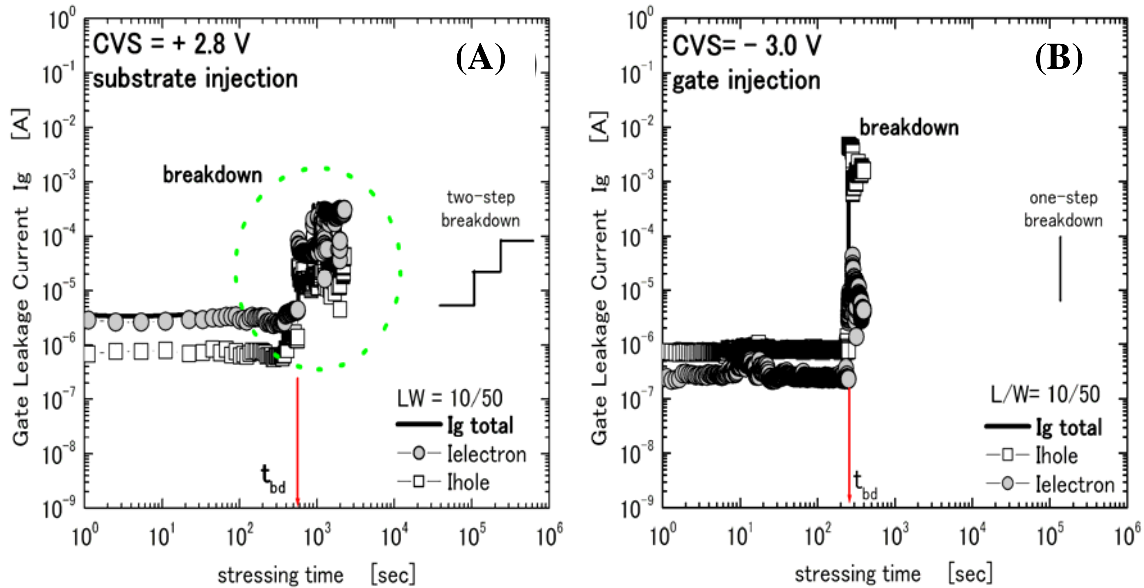


Fig. 4.27 (A) Evolution of gate leakage current (substrate injection) with stressing time. Ielectron is the dominant component of the total Ig. A two–step breakdown behavior is also observed.
(B) Evolution of gate leakage current (gate injection) with stressing time. Ihole is the dominant component of the total Ig. A one–step breakdown behavior is observed.

This difference in the breakdown characteristic for substrate and gate injection conditions is thought to be related to the different dominant carrier for gate leakage current found during the stress. The electrical nature of the dominant carrier would also have some influence with respect to the required time for breakdown tbd. A slightly longer tbd is found for substrate-injection condition as compared to tbd for gate injection. This result suggests that the injection of electrons into the oxide will likely produce relatively longer lifetime before the breakdown of this La_2O_3-IL stack as compared to gate injection where most of the trapped carriers are holes. Nevertheless, dozens of MOSFETs stressed under the same conditions must be analyzed in order to obtain reproducibility and also quantify the occurrence of two-step and single breakdown behavior under both polarities.

In order to get a clearer picture of the breakdown mechanisms involved, simplified energyband diagrams for both substrate and gate injection conditions can be looked at in figs. 4.20B and 4.21B, respectively.

During ***substrate injection (nMOSFET)***, a positive voltage is applied to the gate and both Ie and Ih are detected as shown in fig. 4.27A. The origin of Ie comes from the tunneling of electrons through the La_2O_3-IL stack. The source for these electrons is the S/D regions that are connected once the channel is formed at sufficiently positive gate voltages. Determining the origin of the hole current Ih however, is not so straightforward. Because of the metallic W gate, the possibility of cold or hot-hole injection from the gate is eliminated. The possible mechanisms that could explain the origin of Ih are: 1) Anode-hole injection (AHI), 2) electron-hole (e-h) pair generation in the oxides' bulk/interface via trap levels (TL), 3) tunneling of valence-band electrons from the substrate (leaving holes behind) into the La_2O_3 conduction band directly or via TL and, 4) generation–recombination currents after impact ionization of electrons. It is thought that hole creation via 1) AHI [5] (injected electrons from the substrate generate holes at the anode that can tunnel back into La_2O_3) and, consequently, 2) e-h pair generation via TL within the bulk/interfaces of La_2O_3 are the more plausible mechanisms for the origin of Ih since this oxide tends to develop a high density of TL because of its highly defective nature after deposition [6]. With the application of a continuous electrical stress, more traps or defects within the insulator are created [7]. The two-step nature of the breakdown event during stress is interpreted as initial breakdown of the IL, followed by the breakdown of the La_2O_3 layer itself.

In the case of *gate injection (pMOSFET)*, the single breakdown event takes place at a slightly shorter tbd. A shorter tbd would come by considering a heavier mass for holes that consequently would make more easy for these carriers to be trapped into the oxide during the stress. The sudden current jumps for both electrons and holes occur simultaneously at tbd, see fig. 4.27B, and the breakdown process is considered to start with the simultaneous breakdown of both La_2O_3 and the IL layers. It is thought that the "direction" for the propagation of breakdown is strongly dependent on the polarity of the applied stress. The breakdown propagation would be from cathode towards the anode direction, in other words, dielectric breakdown would occur along the electron current direction for both injection conditions. Interestingly, the post-breakdown current levels for substrate injection are smaller as compared to gate injection; compare both figs. 4.27 A-B. This is explained by considering different sizes for the leakage spots after breakdown. It is thought that the area size of the breakdown spot in gate injection is larger than that after substrate injection.

The next section will present and discuss the reliability characteristics of W/ La_2O_3-IL stacked MOSFET devices after PMA in N_2.

4.6 Carrier separation and Vth shift measurements of W-La_2O_3 gated MOSFET structures after electrical stress

With gate oxides (SiO_2) thinner than 2 nm, the stand-by power consumption due to the gate leakage current (Ig) becomes a critical issue in advanced CMOS devices. In order to reduce Ig, the dielectric film with a higher dielectric constant "k" and a relevant value of the barrier height is needed. Compared to other high-k materials, La_2O_3 has been considered a potential candidate for the long-term replacement of SiO_2 because of its relatively high dielectric constant and band offsets to silicon [1-2]. Moreover, since La_2O_3-gated transistors have presented good initial electrical characteristics [3-4], the research on this material should advance to the next stage where reliability data can be collected and the understanding of the mechanisms for dielectric degradation and breakdown can be identified in order to minimize the sources that lead to failure. In this report, we studied the impact of stress polarity on the breakdown and electrical degradation mechanisms of W-La_2O_3 gated MOSFET structures.

MOS transistors were fabricated on p-type and n-type (100) oriented silicon wafers following the gate last fabrication process [5] in order to avoid the high temperatures used during the thermal activation of source/drain (S/D) regions. After S/D definition, thin films of La_2O_3 were deposited on HF-last or hydrogen-terminated n-type silicon substrates by electron-beam evaporation using molecular beam epitaxy

MBE system (ANELVA I) at 300°C. The pressure in the chamber during the deposition was around 1x10-7 Pa. This is followed by in-situ sputtering of tungsten (60 nm) at 150 W rf power in a contiguous chamber immediately after the dielectric deposition in order to avoid exposure of La_2O_3 surface to the environment. Because of this, the physical thickness of La_2O_3 cannot be measured by ellipsometry but by transmission electron microscopy. During the deposition of the metal an argon flow of 1.33 Pa was used. Patterning of the gate electrodes was done by reactive-ion etching using SF6 gas with a 30 W power. Finally, PMA was done in N_2 ambient at 500°C for 5 min for both n and p-channel MOSFETs.

When La_2O_3 is deposited on silicon, IL formation is almost present at the La_2O_3/Si interface [6]. Thus, it is essential to consider a two-layer oxide stacked structure for the analysis and characterization of its reliability. By using a MOSFET structure, the total Ig can be separated into its electron and hole components (Ie and Ih respectively) using the carrier separation method [7]. A schematic illustration of the carrier separation measurement is shown in fig. 1 (A-B) for nMOSFET and pMOSFET structures respectively. Fig. 1 (C-D) shows the evolution of both Ie and Ih components with respect to stressing time under substrate and gate injection conditions for nMOSFET and pMOSFET structures. From this figure, we can see that the dominant carrier for gate-leakage current changes from electrons for substrate injection to holes for gate injection condition. Also, it is clearly seen that depending on the polarization of the stress gate voltage (Vg), two different oxide breakdown mechanisms will emerge. W/ La_2O_3-IL stack stressed under substrate injection will produce a two-step breakdown behavior as compared to the single-step breakdown found under gate

injection. This difference in the breakdown characteristic for substrate and gate injection conditions is thought to be related to the different dominant carrier for gate-leakage current during the stressing. The electrical nature of the dominant carrier would also have some influence with respect to the required time for breakdown, tbd. A slightly longer tbd is found for substrate injection condition as compared to tbd for gate injection. This result suggests that injection of electrons into the oxide will produce relatively longer lifetime before the breakdown of this La_2O_3-IL stack as compared to gate injection where most of the trapped carriers are holes.

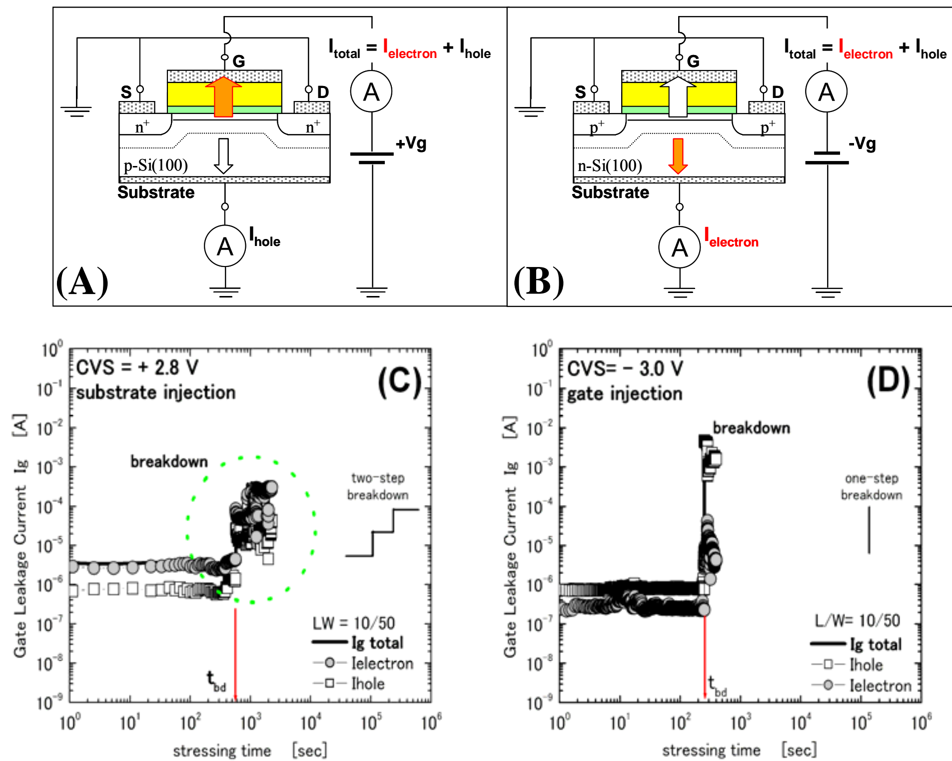


Fig. 1. (A) A schematic illustration of the carrier separation experiment for a W/La_2O_3-IL nMOSFET. $I_{electron}$ and I_{hole} indicate the currents coming from S/D and substrate regions respectively.
(B) A schematic illustration of the carrier separation experiment for a W/La_2O_3-IL pMOSFET. $I_{electron}$ and I_{hole} indicate the currents coming from substrate and S/D regions respectively.
(C) Evolution of gate leakage current (substrate injection) with stressing time. $I_{electron}$ is the dominant component of the total Ig. A two–step breakdown behavior is also observed.
(D) Evolution of gate leakage current (gate injection) with stressing time. I_{hole} is the dominant component of the total Ig. A one–step breakdown behavior is observed.

In order to get a clearer picture of the breakdown mechanisms, simplified energy band diagrams for both substrate and gate injection conditions are shown in fig. 2 (A-B).

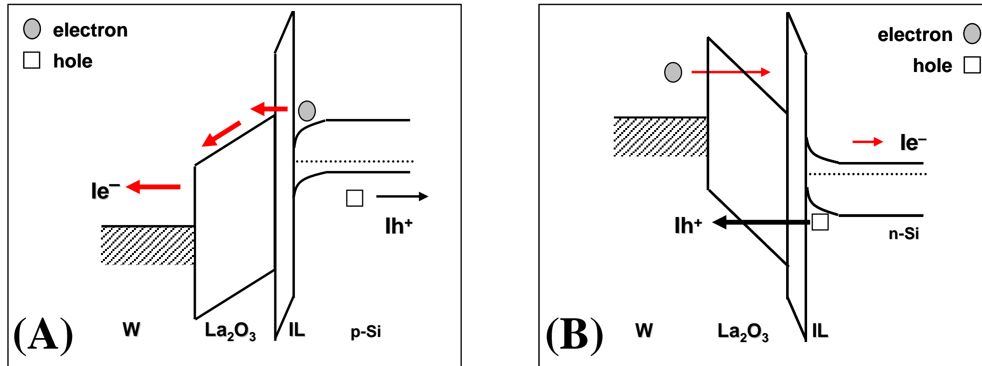


Fig. 2. (A) Energy band diagram for W-La_2O_3 gated nMOSFET under substrate injection stress.
(B) Energy band diagram for W-La_2O_3 gated pMOSFET under gate injection stress.

During the *substrate injection (nMOSFET)*, a positive voltage is applied to the gate and both Ie and Ih are detected as shown in fig. 1 (C). The origin of Ie comes from the tunneling of electrons through the La_2O_3-IL stack. The source for these electrons is the S/D regions that are connected once the channel is formed at sufficiently positive gate voltages. Determining the origin of the hole current Ih, however, is not so straightforward. Because of the metallic W gate, the possibility of cold or hot-hole injection from the gate is eliminated. The possible mechanisms that could explain the origin of Ih are now: 1) Anode-hole injection (AHI), 2) electron-hole (e-h) pair generation in the oxides' bulk/interface via trap levels (TL), 3) tunneling of valence-band electrons from the substrate (leaving holes behind) into the La_2O_3 conduction band directly or via TL and, 4) generation– recombination currents after impact ionization of electrons. It is thought that hole creation via 1) AHI [8] (injected

electrons from the substrate generate holes at the anode that can tunnel back into La_2O_3) and consequent 2) e-h par generation via TL within the bulk/interfaces of La_2O_3 are the more plausible mechanisms for the origin of Ih since this oxide tends to develop a high density of TL because of its highly defective nature after deposition [9]. With the application of a continuous electrical stress, more traps or defects within the insulator are created [10]. The two-step nature of the breakdown event during stress is interpreted as breakdown of the IL first, followed by the breakdown of the La_2O_3 layer itself.

In the case of *gate injection (pMOSFET)*, the first and only breakdown event takes place at a slightly shorter tbd. A shorter tbd would come by considering a heavier mass for holes that consequently would make more easy for these carriers to be trapped into the oxide during the stress. The sudden current jumps for both electrons and holes occur simultaneously at tbd, see fig. 1 (D), and the breakdown process is considered to start with the simultaneous breakdown of both La_2O_3 and the IL layers. It is thought that the "direction" for the propagation of breakdown is strongly dependent on the polarity of the stress applied. The breakdown propagation would be from cathode towards the anode direction, in other words, dielectric breakdown would occur along the electron current direction for both injection conditions. Interestingly, the post-breakdown current levels for substrate injection are smaller as compared to gate injection; see fig. 1 (C-D). This is explained by considering different sizes for the leakage spots after breakdown. It is thought that the area size of the breakdown spot in gate injection is larger than that after substrate injection.

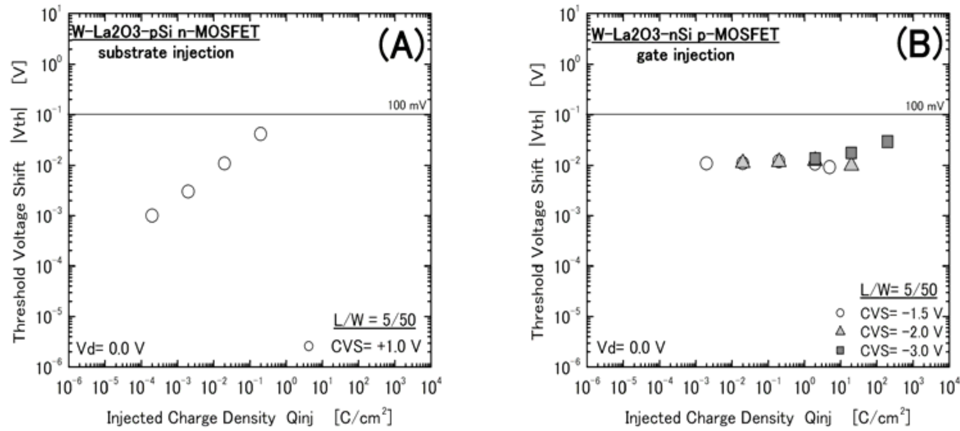


Fig. 3. (A) Vth shift for a W/La_2O_3-IL stacked nMOSFET structure after substrate injection stress.
(B) Vth shift for a W/La_2O_3-IL stacked pMOSFET structure after gate injection stress.

Finally, the influence of substrate and gate injection stress conditions on the electrical characteristics of n and p-channel MOSFET structures is shown in fig. 3 (A-B). Here, the shift in threshold voltage Vth is plotted against the density of injected charge Qinj. Substrate injection conditions will produce a monotonous increase in Vth shift after stress whereas gate injection will produce a more stable Vth shift at the same density of injected charge. Nonetheless, gate injection produces a huge shift in Vth (tenths of millivolt) after the first stressing measurement which is in contrast to the smaller but progressive Vth shifts (few millivolts) produced by substrate injection. Because holes are the major carrier contributors to leakage current during gate injection and since they have a heavier mass than electrons during conduction, it is thought that the density of available sites for the trapping of holes during stress is rapidly filled and saturated after the first injected charges are trapped.

Resuming this section, the effect of electron and hole currents on the breakdown and electrical degradation of the La_2O_3-IL stacked oxide layers was

determined after carrier separation and Vth shift measurements on n and p-channel MOSFET structures. The dominant carrier for the leakage current is strongly dependent on the polarity of the applied stress and this has profound effects on the breakdown characteristics of the oxide layers. Under substrate injection, electrons from the channel are the main contributors to Ig and a two-step breakdown behavior is observed. For gate injection, holes become the main contributors to Ig and a one-step breakdown behavior is now observed. After comparing the Ig post-breakdown characteristics for both substrate and gate injection conditions, it is thought that the area size of the breakdown spot after gate injection is larger than that after substrate injection, thus suggesting that the stress-induced damage is also strongly polarity dependent. Finally, the Vth shift dependence on Qinj is also polarity dependent, with gate injection producing the larger shifts in Vth even after a small density of initially injected charge.

4.7 Summary

By using the MOSFET structure, important measurements have been carried out in order to determine the effect that a positive or negative CVS has on the reliability properties of La_2O_3-gated transistors. By injecting different densities of charge into the oxide structure, the shift in Vth and the respective increases in interface-states density (Dit) were evaluated and compared between nMOSFET and pMOSFET devices. For nMOSFET devices we obtained an electric field-dependent shift in Vth similar to the electric field-dependent shift in Vfb for MOSCAP on n-type

silicon substrates. For low-stressing conditions a negative shift in Vth is produced but the direction of ΔVth changes when the applied CVS increases. Therefore, ΔVth is dependent on the magnitude of the applied stress and injected charge density. In some cases, the occurrence of soft-breakdown SBD events for higher CVS conditions lead to a change in the direction of Vth and Idsat as well. On the other hand, stress-induced changes in Ioff (promoted by positive or negative ΔVth with stress) must be investigated since higher Ioff may add significantly to power dissipation in ULSI circuits and most importantly, the prediction of these changes with time or charge must be worked out in order to develop appropriate models for CAD of La_2O_3-gated devices and circuits. By including a constant drain voltage together with the positive CVS at the gate of nMOSFETs, a higher degradation on Vth is found. Since the additional damage created by Vd worsens the final characteristics of La_2O_3-gated MOSFETs, it is quite important to include as much degradation-factors as possible when stressing these devices in order to get a more realistic projection of their operational lifetimes. In the case of pMOSFETs stressed with negative CVS, only negative ΔVth are observed for all stressing conditions, being Vth dependent on the density of injected charge only. This negative change in ΔVth is related to the trapping of positive charge within the La_2O_3 and its interfaces. Additionally, Dit measurements were obtained after stress. Dit correlated to ΔVth for the case of pMOSFET stressed devices while for nMOSFETs there appears to be no correlation between Dit and ΔVth after stress.

The effect of substrate and gate injection on the degradation and breakdown of La_2O_3-IL stacked MOSFETs were obtained after CS measurements. It was shown that the major contributor to leakage current under gate (substrate) injection comes by the

injection of holes (electrons) via the inverted channel. Also, substrate injection of electrons degraded more severely the MOSFET characteristics as compared to gate injection since the likely occurrence of SBD events during CVS can lead to alternate switches in the direction of the final Vth.

Finally, the effect of electron and hole currents on the breakdown and electrical degradation of the La_2O_3-IL stacked oxide layers was determined after CS measurements on n- and p-channel MOSFET structures. The dominant carrier for the leakage current is strongly dependent on the polarity of the applied stress and this has profound effects on the breakdown characteristics of the oxide layers. Under substrate injection, electrons from the channel are the main contributors to Ig and a two-step breakdown behavior is observed. For gate injection, holes become the main contributors to Ig and a one-step breakdown behavior is now observed. After comparing the post-breakdown Ig characteristics for both substrate and gate injection conditions, it is thought that the area size of the breakdown spot after gate injection is larger than that after substrate injection, it thus suggests that the stress-induced damage is also polarity dependent. Finally, the Vth-shift dependence on Qinj is also polarity dependent, with gate injection producing the larger shifts in Vth even after a small density of initially injected charge.

References

[1] AS Oates, "Reliability issues for high-k gate dielectrics", IEDM, pp. 3821-3824 (2003).

[2] P. Heremans, J. Witters, G. Groeseneken and HE Maes, "Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation", IEEE Trans. on Elec. Dev., 36 (7), pp. 1318-1335 (1989).

[3] H. Park, MS Rahman, M. Chang, BB Lee, M. Gardner, CD Young and H. Hwang, "Effect of high pressure deuterium annealing on electrical and reliability characteristics of MOSFETs with high-k gate dielectric", Proc. IRPS, pp. 646-647 (2005).

[4] WY Loh, BJ Cho, MS Joo, MF Li, DSH Chan, S. Mathew and DL Kwong, "Analysis of charge trapping and breakdown mechanism in high-k dielectrics with metal gate electrode using carrier separation", IEDM, pp. 3831-3834 (2003).

[5] K.F. Schuegraf and C. Hu, "Metal-oxide-semiconductor field-effect-transistor substrate current during Fowler–Nordheim tunneling stress and silicon dioxide reliability", J. Appl. Phys., vol. 75, no. 6, pp. 3695-3700, Sept. 1994.

[6] Y.N. Sang, E. Dail, S.H. Cheol and J.K. Hyeong, "Properties of lanthanum oxide thin films deposited by cyclic chemical vapor deposition using tris(isopropyl–cyclopentadienyl) La precursor", J. Appl. Phys., vol. 100, pp. 24111, July 2006.

[7] E. Miranda. J. Molina, Y. Kim and H. Iwai, "Tunneling in sub-5 nm La_2O_3 films deposited by E-beam evaporation", J. Non. Crystal. Solids, vol. 352, no. 1, pp. 92-97, Jan. 2006.

References from section 4.6

[1] T. Hattori , T. Yoshida , T. Shiraishi , K. Takahashi , H. Nohira , S. Joumori , K. Nakajima , M. Suzuki , K. Kimura , I. Kashiwagi, C. Ohshima d, S. Ohmi, and H. Iwai, "Composition, chemical structure, and electronic band structure of rare earth oxide / Si(100) interfacial transition layer", Mic. Engineering, Volume 72, Issues 1-4, April 2004, Pages 283-287.

[2] G. D. Wilk, R. M. Wallace and J. M. Anthony, "High-k gate dielectrics: current status and materials properties considerations", J. Appl. Phys., vol. 89, no. 10, pp. 5243-5275, May 2001.

[3] J.A. Ng, N. Sugii, K. Kakushima, P. Ahmet, K. Tsutsui, , T. Hattori and H. Iwai, "Effective mobility and interface-state density of La_2O_3 nMISFETs after post deposition annealing", IEICE Electron Express, vol. 3, no. 13, pp. 316-321, June (2006).

[4] J.A. Ng, Y. Kuroki, N. Sugii, K. Kakushima, S. Ohmi, K. Tsutsui, T. Hattori, H. Iwai and H. Wong, "Effects of low temperature annealing on the ultrathin La_2O_3 gate dielectric; comparison of post deposition annealing and post metallization annealing", Microelectron. Eng., vol. 80, no. 17, pp. 206-209, June (2005).

[5] W. Tsai, L.A. Ragnarsson, T. Schram, S. Degendt, M. Heyns, M.C. Ozturk, L.J. Chen, P.J. Timans, F. Roozeboom, E.P. Gusev, D.L. Kwong and G. Miner, "Challenges in integration of metal gate high-K dielectrics gate stacks", Proc., Electrochem. Soc., Advanced short-time thermal processing for Si-based CMOS devices II, San Antonio, TX, USA. vol. 1, pp. 321-327, May 2004.

[6] H. Nohira, T. Yoshida, H. Okamoto, W. Sakai, K. Nakajima, M. Suzuki, K. Kimura, J. Ng, Y. Kobayashi, S. Ohmi, H. Iwai, E. Ikenaga, K. Kobayashi, Y. Takata and T. Hattori, "Thermal stability of lanthanum oxide/Si(100) interfacial transition layer", ECS Trans., vol. 1, no. 1, pp. 87-96, Oct. 2005.

[7] C. Chang, C. Hu and R.W. Brodersen, "Quantum yield of electron impact ionization in silicon", J. Appl. Phys., vol. 57, no. 2, pp. 302-309, Jan. 1985.

[8] K.F. Schuegraf and C. Hu, “Metal-oxide-semiconductor field-effect-transistor substrate current during Fowler–Nordheim tunneling stress and silicon dioxide reliability”, J. Appl. Phys., vol. 75, no. 6, pp. 3695-3700, Sept. 1994.

[9] Y.N. Sang, E. Dail, S.H. Cheol and J.K. Hyeong, “Properties of lanthanum oxide thin films deposited by cyclic chemical vapor deposition using tris(isopropyl–cyclopentadienyl) La precursor”, J. Appl. Phys., vol. 100, pp. 24111, July 2006.

[10] E. Miranda. J. Molina, Y. Kim and H. Iwai, “Tunneling in sub-5 nm La_2O_3 films deposited by E-beam evaporation”, J. Non. Crystal. Solids, vol. 352, no. 1, pp. 92-97, Jan. 2006.

Chapter 5

Models for degradation and breakdown mechanisms of Metal/La_2O_3-gated MOS devices

5.1 Introduction

5.2 Carrier injection in the La_2O_3-SiO_2 system

5.3 Trap creation and interface-state generation

5.4 Failure modes for degradation of La_2O_3-SiO_2 stack

5.5 Towards a unified vision of BKD in La_2O_3-SiO_2 dual layers

References

5.1 Introduction

This chapter presents the physical models that are proposed in order to explain the degradation and breakdown characteristics of La_2O_3-gated MOS devices under stressing conditions. It should be pointed out that, since the degradation phenomena of high-k based oxides is not so easy to analyze as in conventional oxides, and because establishing more accurate model for reliability prediction requires thousands of samples, the proposed models and mechanisms for breakdown are mere attempts to explain the electrical results we have obtained so far.

Because of the unavoidable reaction of La_2O_3 into silicates or even formation of additional SiO_2-based interfacial layers between La_2O_3 and silicon at higher PMA temperatures, the presence of a lower-k IL must be taken into account when modeling the physical degradation of La_2O_3-gated oxides is done. From the observations in this study, depending on the intensity of the applied stress or density of the injected charge, the degradation of La_2O_3 can result in the following failure modes:

1) Stress-induced leakage current (SILC) degradation

2) Charge trapping-detrapping ($\Delta Vfb/\Delta Vth$) degradation

3) Soft-breakdown (SBD) degradation

4) Hard-breakdown (HBD) degradation

5) Progressive-breakdown (PBD) degradation

The occurrence of one or several of these degradation events are closely related to the density of Qinj and magnitude of applied stress. In the case of lifetime prediction of La_2O_3, the inclusion of the IL and the very simple linear Vg model is introduced. Besides, since higher densities of injected charge are possible by whether higher densities of injected current or longer times of stressing, the identification of the major carrier contributor to leakage current is necessary. This separation of the total gate-leakage current into both electron- and hole-current components was already introduced in the previous chapter and will be extended here in order to develop a model able to explain the obtained results.

The polarization used during the stressing measurement also plays a significant role in the degradation of Metal/La_2O_3-gated devices. From the previous results, we have been able to identify a higher degradation rate for substrate injection compared to gate injection conditions on La_2O_3-gated MOSFET devices. From the carrier separation measurements, it is concluded that, compared to gate injection (where both electrons and holes are simultaneously injected), substrate injection only tunnel and trap electrons into the La_2O_3-IL stacked structure and this current is detected at the gate of the transistors. The injection of a single or both types of carriers must be taken into account for a more precise modeling of the degradation phenomena. In general, it is thought that depending on the duration of the same applied stress, all types of electrical degradation (failure modes) can take place for the flow of current to produce the required damage by the creation of new defects, charge trapping (within the bulk of La_2O_3 and/or at its interfaces), consequent formation of localized conduction paths and ultimately, growth of the leakage spots

(progressive breakdown) once hard breakdown condition has been reached. This scenario is graphically depicted in fig. 5.1, where all failure modes are represented.

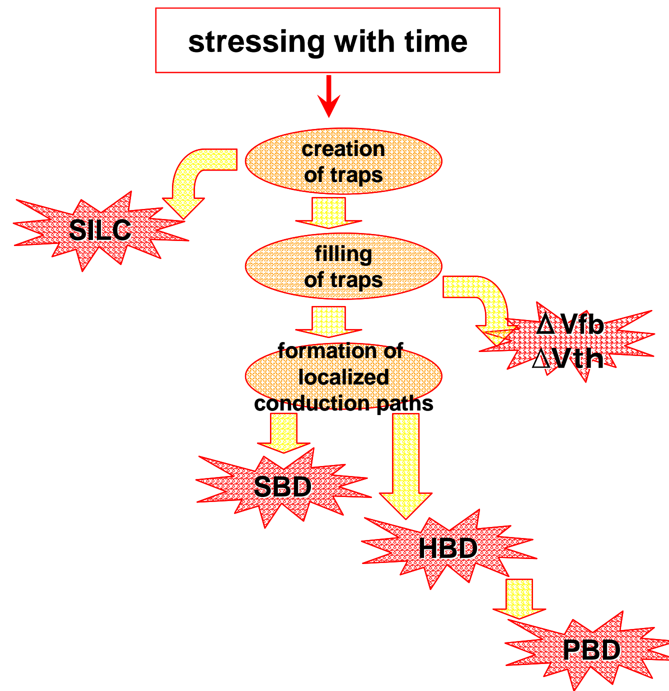


Fig. 5.1 Schematic representation of the generation of failure modes with stressing time.

5.2 Carrier injection in the La_2O_3-SiO_2 system

It has been claimed that the SBD current flowing through conventional oxides could be explained by means of a direct tunneling (DT) process [1]. This conduction mechanism corresponds to tunneling through a trapezoidal-type potential barrier, i.e. when the energy of the passing electrons is below the top of the barrier all the way across its thickness. They proposed that SBD arises as a consequence of the progressive degradation

of a localized region close to the anode interface. According to this picture, the ballistic impact of the injected electrons on the silicon surface would cause a physical damage that could be thought of as a *reduction of the effective oxide thickness*. For a La_2O_3-based device, however, the presence of a very thin IL between La_2O_3 and silicon substrate would make the reduction of the effective oxide thickness appears as breakdown of the IL followed by an undamaged La_2O_3 region (this is schematically depicted in fig. 5.2).

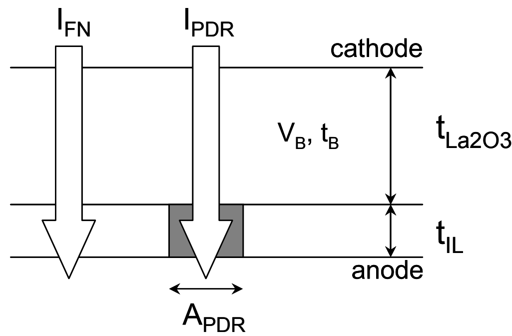


Fig. 5.2 Schematic representation of the thinned (IL BKD) oxide approach.

Within this framework, the physical damaged region (PDR) is associated with a purely resistive region of resistivity ρ and the remaining barrier thickness is the undamaged thick La_2O_3. The total gate current Ig is therefore modeled as the superposition of the FN current through the undamaged device area I_{FN} (tunneling through both La_2O_3-IL stack) and the DT current through the PDR I_{PDR}:

$$I_T = (1 - A_{ratio})I_{FN} + A_{ratio}I_{PDR} \tag{5.1}$$

Where $A_{ratio}= A_{PDR} / A_{cap}$, A_{PDR} and A_{cap} being the area of the spot and the total capacitor area, respectively. From fig. 5.1, the oxide voltage drop Vox (from cathode to anode) can be

written as: $V_{OX} = V_B + I_{PDR}\rho(t_{OX} - t_B)$. Where t_B is the thickness of the DT barrier and V_B the potential drop across this barrier. I_{PDR} can be calculated by means of a numerical iteration process. The importance of this model comes by representing the increase in leakage current (during FN conditions) as a thinning of the total oxide barrier which in case of La_2O_3-based oxides would be the breakdown of the IL developed underneath. The modeling of Ig increase during FN condition is important because this can lead to understanding of the mechanisms behind the physical processes occurring into the oxide stack before total breakdown occurs.

For the degradation of oxides, it has also been proposed a SBD model based on the *percolation theory of non-linear conductor networks* with a distribution of percolation thresholds [2-3]. According to this model, during degradation, traps randomly occupy the sites of the SiO_2 lattice eventually forming a backbone that spans between the electrodes. It is assumed that the current i between two neighboring traps is proportional to the square of the voltage-drop value between sites v, that is $i = \sigma v^2$, where σ is the bond conductivity. The origin of this quadratic-law was ascribed to the product of the trapped charge density in the capacitor and the electron drift mobility. For a La_2O_3-IL stacked structure, this percolation model should take into account the generation of traps at different oxide lattices (see fig. 5.3). Therefore, the polarization of the applied stress would play an important role in determining the initial creation of traps within the first lattice and thus, the probability for this lattice to reach breakdown. In a dual-oxide structure, it is thought that the polarization of the applied stress is important to trigger the initial breakdown of the lattice whose trap

sites become to be filled by the percolation paths. For nMOSFETs stressed in inversion, the injection of electrons (via the inverted channel from the substrate) severely degrades the characteristics of the devices (shifting Vth in accordance to the magnitude of the applied voltage and proportionally to Qinj). Even the appearance of SBD events could change the direction in ΔVth, so that the application of the percolation model for degradation analysis [4] should be applied to the IL which is quite likely to breakdown during substrate injection conditions.

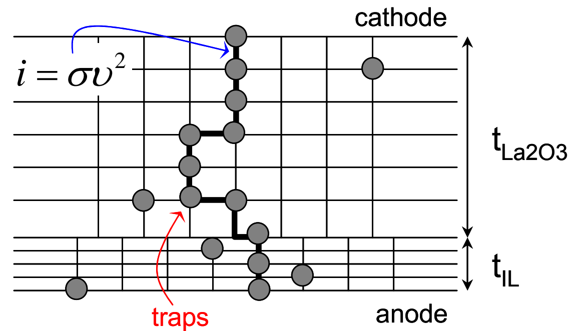


Fig. 5.3 Schematic representation of the percolation path between electrodes and formed within both La_2O_3 and IL lattices. For a dual-oxide, the polarization of applied stress is important to determine the "filling" of the first lattice trap sites by percolation traps and thus reach breakdown.

Once the breakdown of IL occurs during the substrate injection stressing, the breakdown paths formed in the IL by the connection of percolation sites should be followed by the breakdown of the La_2O_3 and therefore, the entire layer breaks down. This is schematically depicted in fig. 5.4.

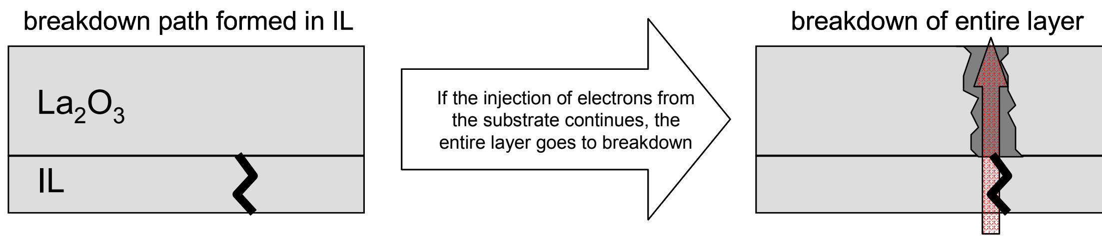


Fig. 5.4 Schematic representation of the breakdown "path" followed by the injection of electrons coming from the substrate. Once the stressing continues the whole layer breaks down.

From the model proposed for the substrate injection in fig. 5.4, we can see that since a denser lattice in SiO_2-based IL creates a thinner percolation path for conduction of electrons, the following percolation path created in the broader La_2O_3 lattice would tend to limit its size to that of the thinner and broken lattice region found underneath. Therefore, the total size of the leakage spot after total breakdown would be smaller to that found in gate injection and this simple model explains the results shown in fig. 4.27A, where the post-breakdown current levels of W/La_2O_3-IL stacked MOSFET after substrate injection are smaller compared to those found after gate injection conditions. For comparison purposes, the breakdown path proposed during gate injection is also depicted in fig. 5.5.

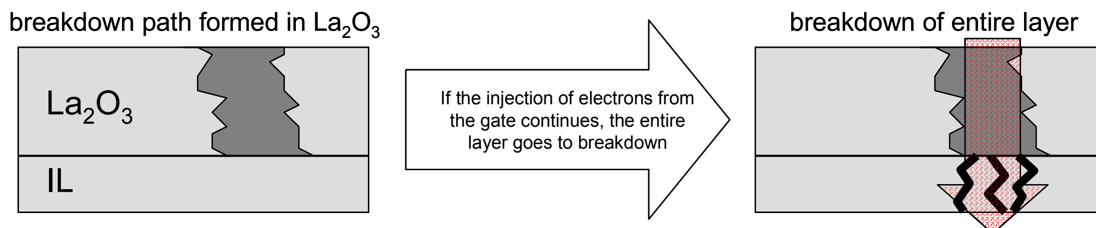


Fig. 5.5 Schematic representation of the breakdown "path" followed by the injection of electrons coming from the gate. Once the stressing continues the whole layer breaks down.

In the proposed model, the injection of electrons coming from the gate creates a broad percolation path since the lattice for La_2O_3 is bigger. A bigger lattice implies that the connection of electrical defects (percolation sites) covers a bigger area so that once all the defects are connected, the total size of the leakage spot is increased. Once the La_2O_3 reaches breakdown, the IL follows immediately by developing multiple percolation sites towards the substrate so that the final density of post-breakdown leakage current increases compared to substrate injection.

5.3 Trap creation and interface-state generation

There are several kinds of traps in which electrons or holes can be trapped during stress. They can be classified into two general groups: bulk and interfacial traps. Since La_2O_3 easily changes its chemical composition after PMA (La_2O_3 tends to transform to La-silicate with silicon), the generation of additional traps (mainly by the creation of oxygen vacancies during annealing) could limit the final reliability of La_2O_3-gated devices. However, the recovering of initial traps after PMA is also a process that counterbalances the final density of available sites for trapping of charge. It has been shown that the reliability characteristics of PMA-La_2O_3 devices are far superior to those without annealing, thus supporting the idea that whatever density of new traps generated during PMA, they are overwhelmed by the recovering or passivation of the traps' initial density. On the other hand, once electrical stress is applied, new kinds of defects or traps are created and they are

generated by the tunneling of electron/hole currents within the oxide stack.

Prior to catastrophic breakdown, the tunneling electrons, directly or indirectly, also cause several other physical processes to take place, with the net effect of “softening” the oxide stack before final breakdown. These include trap generation, which enhances the trapping of electrons and holes, and interface-state generation, which is a sign that some of the electron bonds in the oxide, at least those near the IL-silicon interface, are “weakened”. The physics of trap generation and interface-state generation is very complex but their effects can be quantitatively measured as shown by the Dit measurements of La_2O_3-gated MOSFETs already shown in chapter 4.

5.4 Failure modes for degradation of La_2O_3-SiO_2 stack

As stated earlier, depending on the intensity of the applied stress, the degradation of La_2O_3 is thought to proceed as follows:

1) Stress-induced leakage current (SILC) degradation

2) Charge trapping-detrapping ($\Delta Vfb/\Delta Vth$) degradation

3) Soft-breakdown (SBD) degradation

4) Hard-breakdown (HBD) degradation

5) Progressive-breakdown (PBD) degradation

The occurrence of one or several of these degradation events are closely related to the density of Qinj and magnitude of applied stress and they will be presented next.

5.4.1 Stress-induced leakage current SILC

The first reports of SILC on low-field gate leakage current following high-field stressing of thin SiO_2-based MOS capacitors appeared almost two decades ago [5-6]. These leakage currents increased with decreasing oxide thickness and were identified as a scaling limitation for nonvolatile memory tunnel oxide [6]. Additional studies of the stress-induced leakage current have since been performed and it is now generally agreed upon that this current is caused by the trap-assisted tunneling [7-10]. However, there are certain aspects of SILC that had yet to be satisfactorily explained, including its dependence on the oxide thickness and the effect of the IL when a high-k oxide is used. In this section, a simple model is proposed to explain the SILC results in the current study.

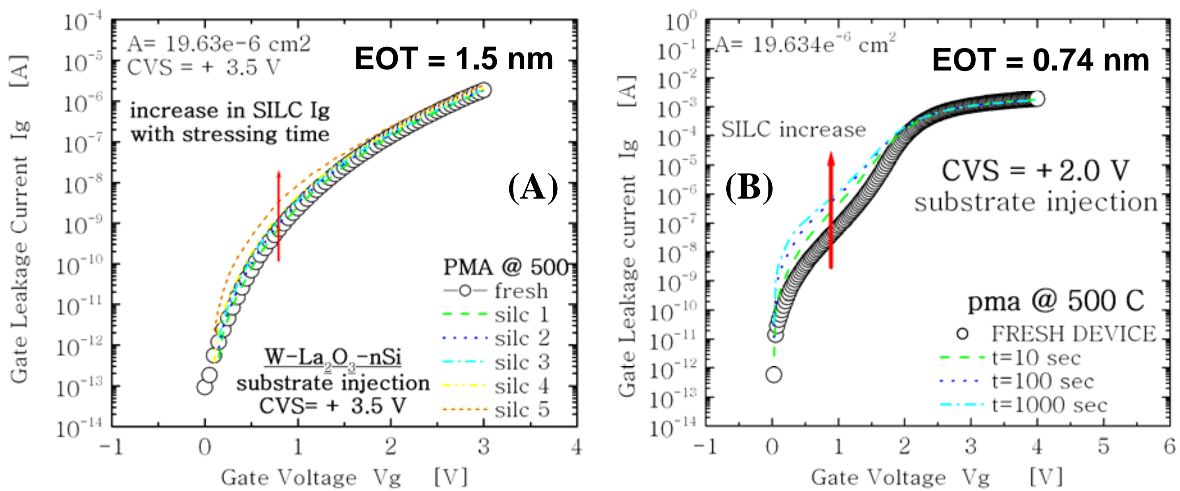


Fig. 5.6 SILC measurement after positive CVS (gate injection) for thick and thin La_2O_3-IL stacks. (A) EOT= 1.5 nm (normal La_2O_3 deposition). (B) EOT= 0.74 nm (in-situ tungsten metallization).

Fig. 5.6 A-B shows the increment in SILC after positive stress for thick and thin La_2O_3-IL stacked oxide films. Because it is not clear whether higher SILC results from thick or thin La_2O_3, the same results were plotted in fig. 5.7 by normalizing the relative change in SILC to the respective fresh condition of both samples.

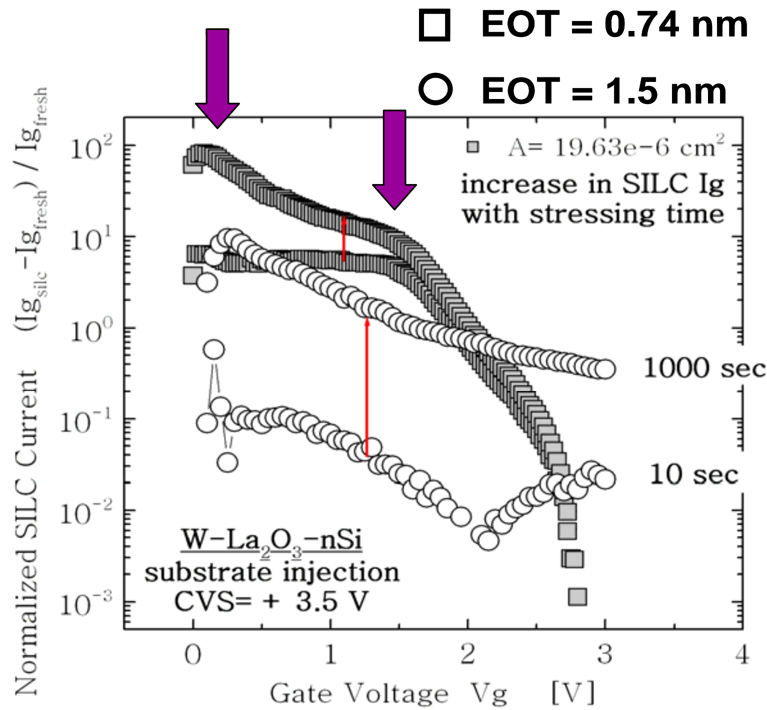


Fig. 5.7 Relative change in leakage current induced by SILC (same data as in fig. 5.6 A-B).

From fig. 5.7, the relative increment in SILC for both thick and thin La_2O_3-IL stacked films shows a higher increase in gate leakage current for the thinner film at low gate voltages. SILC increases as the oxide thickness is reduced. The generally accepted model for SILC in MOS capacitors is an electron tunneling between the gate and substrate conduction bands via a stress-induced trap in the oxide. To date, this process has been

represented as a resonant or elastic tunneling process; however, more recent studies have demonstrated that the difference between the SILC characteristics for thick or thin oxides is related to a single-trap assisted inelastic tunneling process [11]. Because replacing SiO_2-based oxides with the highly defective La_2O_3 film could lead to multiple-trap assisted inelastic tunneling, this process is proposed in order to explain the different SILC characteristics for thick and thin La_2O_3-IL films. Besides, the appearance of two visible "kinks" for the SILC variation in the Vg dependences could be related to the energy distribution of defects within La_2O_3 that are generated during the stressing measurement.

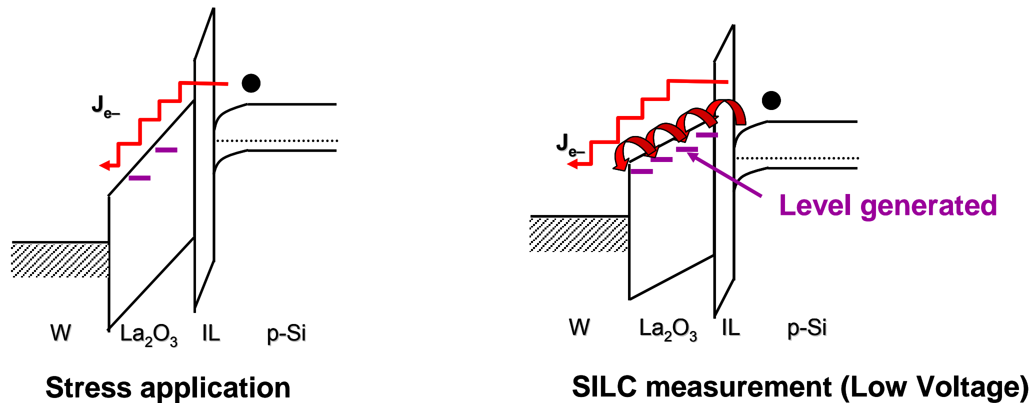


Fig. 5.8 Left side plot shows an energy band diagram during CVS measurement (high voltage). During CVS, new energy levels of generated defects are created. Right side plot shows electrons tunneling inelastically through generated levels during SILC measurement.

Once new defects are generated during CVS (high-voltage), they serve as "stepping-stones" for electrons tunneling inelastically through them and towards the gate. In short, SILC is the flow of carriers through pre-existent traps within La_2O_3 and the density of these sites for carrier conduction increases with stress, so that SILC for longer stress voltages/time will accordingly increase.

5.4.2 Charge trapping-detrapping (ΔVfb/ΔVth) degradation

When analyzing the effect of electrical stress on the reliability properties of La_2O_3-gated MOS devices, we have found that there is an electric-field dependency of the resulting flat-band and threshold-voltages Vfb/Vth shifts with stress under the substrate injection. Under low-stressing conditions, negative shifts in Vfb/Vth (presuming trapping of positive charge) take place whereas under higher stressing conditions the expected positive shifts in Vfb/Vth occur. This change in the direction of the Vfb/Vth shift is explained in terms of electron trapping-detrapping processes within the La_2O_3-IL stack, see fig. 5.9. Under the substrate injection (positive CVS), the trapping of electrons is expected since electrons are identified as the major contributors to leakage current from carrier separation measurements. However, at low positive CVS, negative ΔVfb/ΔVth take place indicating that whether trapping of positive charge or detrapping of negative charge occurs within the oxide stack. Once the positive CVS is increased, the change in the direction of Vfb/Vth to positive values takes place and this indicates the occurrence of electron trapping or detrapping of holes within the oxide stack. Since electrons are the only carriers injected in the oxide during substrate injection stressing conditions (see fig. 4.20) the detrapping of electrons during low-field stressing, generation of new trap levels and consequent trapping of electrons during high-field stressing is the more plausible physical mechanism for the data presented in fig. 5.9. The energy-band diagram showed the models explaining the effect of electron trapping-detrapping along with the generation of new trap levels with stress. In summary, this simple degradation model implies the trapping-detrapping of

electrons at different spatial locations of the La_2O_3-IL stack and which are dependent on stress polarity.

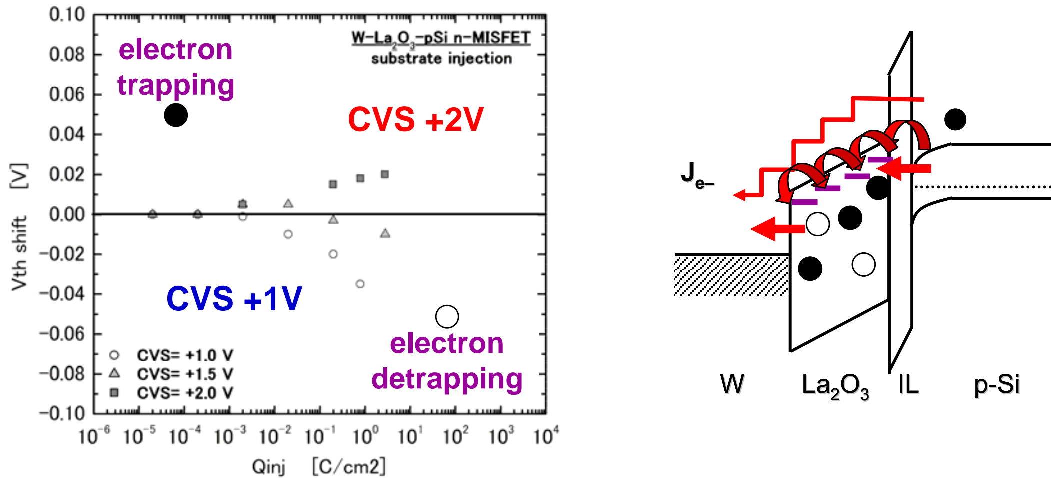


Fig. 5.9 Left side plot shows the shift in Vth for La_2O_3-gated nMOSFETs stressed under low and high positive CVS. The change in direction of ΔVth with stress is clear. Right side energy band diagram models the degradation phenomena occurring within the oxide stack.

5.4.3 Soft-breakdown (SBD) degradation

During the stressing of La_2O_3-gated nMOSFET devices with positive CVS, the occurrence of soft breakdown (SBD) event is detected as a sudden jump in an I-t plot. The effect of this SBD event on the nMOSFET, however, changes the direction of the trend originally followed by ΔVth, see fig. 4.1. The SBD degradation is modeled as the breakdown of the interfacial layer (IL) so that the resulting Vth depends on the charge trapped at the bulk of La_2O_3. The model is shown in fig. 5.10.

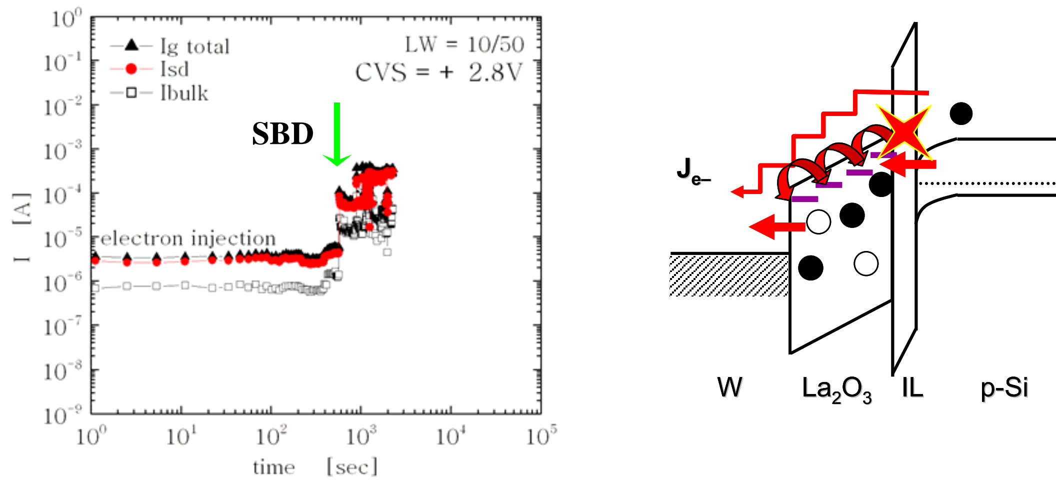


Fig. 5.10 Left side plot shows the evolution of leakage current with time under substrate injection conditions (positive CVS). At certain stressing time, the occurrence of a SBD event is detected. Right side energy band diagram models this degradation phenomenon as breakdown of the IL.

Once the stress continues under substrate injection, the generation of new traps as well as electron detrapping-trapping processes both takes place until the interfacial layer breaks down. This is seen as a sudden jump in the leakage current in an I-t plot and as a change in the direction of ΔVth during the Id-Vd MOSFET measurements. It is important to emphasize that even with the breakdown of a single-oxide layer (La_2O_3 or IL), a dual-oxide MOSFET device is still operative if the location of the breakdown spot along the channel does not compromise the operational characteristics of the device.

5.4.4 Hard-breakdown (HBD) degradation

Hard breakdown is a kind of fatalistic failure mode in which both oxide layers broke down. This mode lead to the continuous conduction of huge amounts of leakage current through a conductive leakage spot connecting both a gate electrode and a silicon

substrate and eliminating the electric field to control the charge in the inverted channel. HBD can be seen as an immediate consequence of applying high-stressing conditions on the stressed device and its effect can be seen as a sudden jump in the leakage current on Ig-Vg or Ig-time plots. It is thought that the breakdown occurs by the accumulative gathering of previous degradation events (SILC, trapping-detrapping processes, SBD), so that the hard or total breakdown of the oxide stack would come after gathering a certain density of intrinsic and stress-generated defects and satisfying conditions for the connection of these defects.

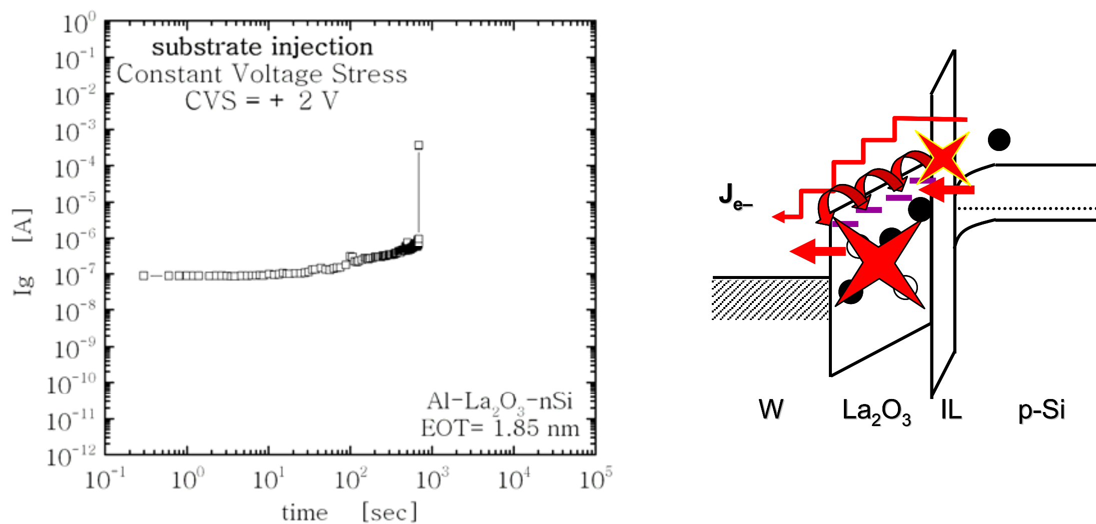


Fig. 5.11 Left side plot shows the evolution of leakage current with time under substrate injection conditions (positive CVS). At certain stressing time, the occurrence of a HBD event is detected. Right side energy band diagram models this degradation phenomenon as total breakdown of the stacked oxide.

5.4.5 Progressive-breakdown (PBD) degradation

The lateral propagation of the damaged area as the result of a constant electrical stress is now introduced. It has been concluded that two clearly distinguishable timescales

must be considered for the study of the breakdown dynamics [12-13]. First, there is a timescale related to the formation of the initial leakage spot, which is in the order of nanoseconds, and secondly, a timescale related to the subsequent spread of the damage, which is in the order of seconds or more. After their appearance, the breakdown spots can gradually progress with time, be it SBD or HBD and this process has been referred to as progressive breakdown (PBD). The degradation and breakdown of ultra-thin SiO_2 films at a local level has also been investigated by means of atomic force microscopy [14-15], and it has been found that, although the degradation takes place in areas of few hundreds of nm^2, the breakdown event laterally propagates to neighboring spots, eventually affecting areas of thousands of nm^2. Using this alternative technique, it has been confirmed that the size of the damaged area is related to the severity of the breakdown event [16]. For metal/high-k gated nMOSFET devices, the area size of the breakdown spots in accumulation (gate injection) is larger than that in inversion (substrate injection) [17-18]. Interestingly, for our La_2O_3-IL stacked nMOSFET and pMOSFET devices, we also have found a similar behavior. The post-breakdown current levels for nMOSFETs after positive CVS (substrate injection) are smaller as compared to pMOSFETs after negative CVS (gate injection). This is explained by considering different sizes for the leakage spots after breakdown. It is thought that *the area size of the breakdown spot in gate injection is larger than that after substrate injection*. These results are all shown in fig. 5.12 and 5.13. Fig. 5.12 A-B shows that after HBD is reached in La_2O_3-IL gated MOSCAP, the occurrence and propagation of the breakdown spot during electrical stress presents similar behavior in both Ig-Vg and Ig-time plots. The propagation of the breakdown spot is seen as a sudden “jump” in gate

leakage current.

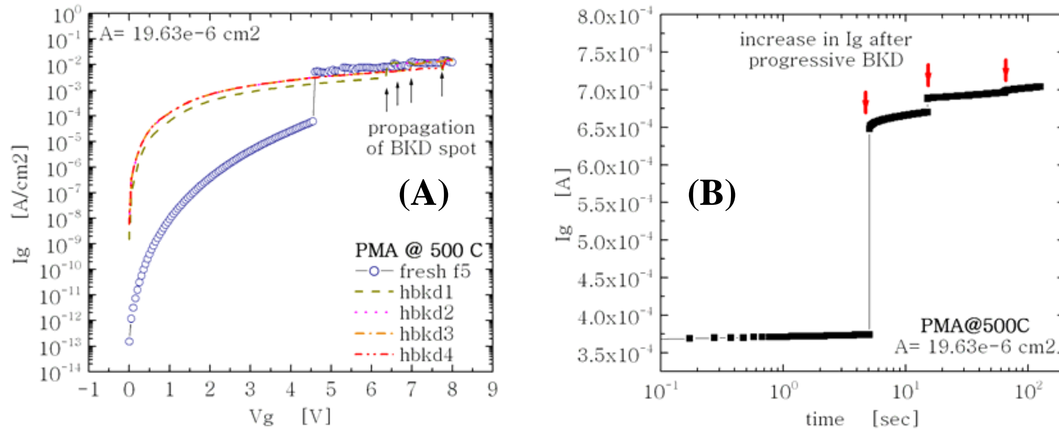


Fig. 5.12 (A) Ig-Vg plot for La_2O_3-IL stack showing HBD characteristics and consequent propagation of the breakdown event with Vg. The post-breakdown current levels also increase in accordance to PBD. (B) Ig-time plot for La_2O_3-IL stack showing HBD characteristics and consequent propagation of the breakdown event with time. During PBD, higher Ig is related to a larger size of the total breakdown spot.

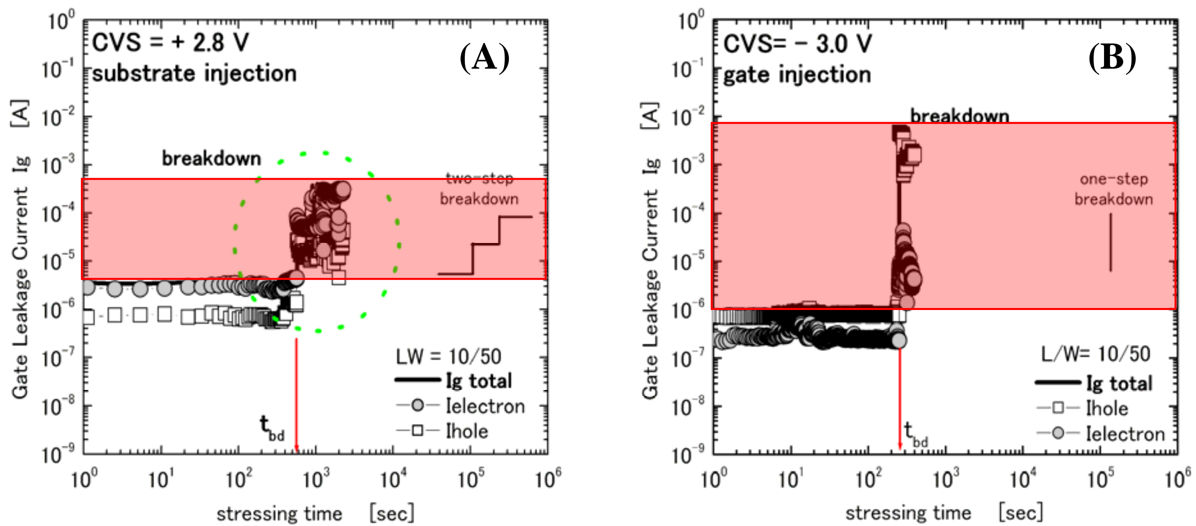


Fig. 5.13 (A) The post-breakdown leakage current for nMOSFET in inversion shows a two-step breakdown. (B) For pMOSFET, a single-step breakdown, along with higher levels for the post-breakdown Ig is obtained.

On the other hand, for La_2O_3-IL gated MOSFET devices, the evolution of Ig until the oxide stack breaks down results in higher densities of post-breakdown Ig for pMOSFETs as compared to nMOSFET (highlighted zones), both in inversion state (fig. 5.13). It is thought that the total area size of the breakdown spots in gate injection (pMOSFET in inversion) is larger than that after substrate injection (nMOSFET in inversion). The proposed model that explains the former results is schematically depicted in fig. 5.14 presented next. Here, the PBD characteristics for substrate and gate injection conditions are shown.

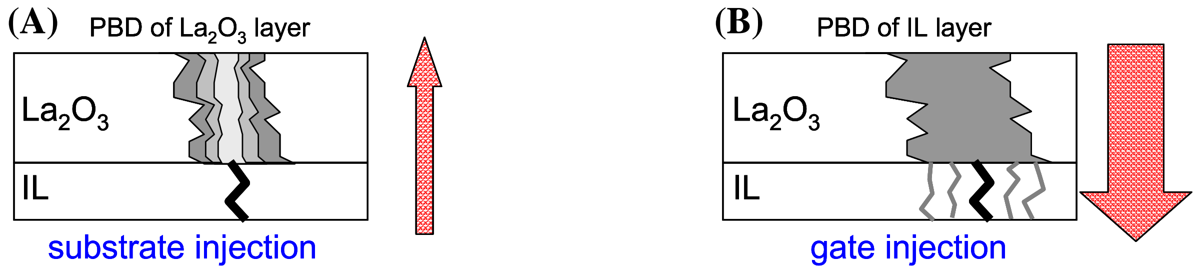


Fig. 5.14 (A) For substrate injection, the lateral breakdown propagation of the La_2O_3 layer (after IL breakdown) increases the post-breakdown Ig. Opening of new breakdown spots in La_2O_3 is also possible.
(B) In gate injection, higher post-breakdown Ig is related to the larger size in the breakdown spot within La_2O_3. PBD characteristics would be related to the widening/opening of same/new BKD spots.

It is noteworthy that a more severe breakdown characteristic is found for La_2O_3-IL stack after gate injection (fig. 5.12B) and this could be directly related to the formation of a wide percolation path created by the breakdown of the La_2O_3 layer. The formation of this wide percolation path is probably assisted by grain boundaries within the La_2O_3 layer. A higher post-breakdown Ig could therefore be linked to high conductivity and the total

damaged spot area after stress. The inclusion of only one damaged spot that increases in size (fig. 5.14A), does not restrict the creation of other breakdown spots at different locations within La_2O_3 or even within the IL (fig. 5.14B). Nevertheless, the lateral propagation of the breakdown event, whether by a single spot increasing in size or the generation of multiple spots at different spatial locations, has been correlated to the magnitude of Ig after breakdown [19-20].

Even though it is beyond the scope of this work, how the different breakdown modes affect the fundamental reliability of MOSFET devices and circuits is a very important topic that must be addressed. Even though there is nowadays a growing consensus that SBD would be the prevailing breakdown mode for low-voltage operation, its final consequences upon the device behavior are rather complex and seem to depend on various factors such as the location of the breakdown spot along the device channel and the dimensions of the damaged area compared to those of the device under test. Briefly, it has been found that a breakdown event near the source/drain regions produce more severe consequences than a breakdown in the channel region. In other words, gate-to-substrate leakage paths exhibit higher resistances than those occurring in the source/drain regions. Cester et al. [21] have shown that the MOSFET characteristics after SBD are strongly dependent on the aspect ratio W/L. According to this report, the drain saturation current and transconductance collapses after SBD, and these are linked to the formation of an oxide defective region around the breakdown spot, whose effective area is much larger than the conductive path itself. This is somewhat similar to the present results for La_2O_3-gated

MOSFETs where Vth and Idsat presented serious instabilities after the occurrence of SBD events during the stressing of the devices. The effects of the gate-oxide breakdown in MOSFETs operating in the RF range, the implications for the drain current low-frequency noise as well as the effects on SRAM cells must also be investigated. On the other hand, a fundamental problem that arises with this context is whether a transistor remains functional or not after the occurrence of a gate oxide breakdown. Even if the device is able to survive after SBD, there may still be some impact of subsequent stress on the already broken-down sample. Particularly noteworthy is the fact that even though it has been long considered that HBD straightforwardly leads to a total loss of the transistor effect, it is now understood that the device functionality criterion must be assessed in close connection with the role it plays within a particular circuit structure and its intended purpose. In this regard, as demonstrated by Kaczer et al. [22], many HBD events can occur in a digital CMOS circuit without affecting its logical functionality. This means that depending on the particular application, current reliability criteria may be, in some extent, relaxed. Finally, the physical models for the post-breakdown conduction characteristics (which are rather ambiguous even for explaining post-breakdown currents in conventional SiO_2-based oxides) are strongly dependent of the stressing conditions that led to breakdown. An excellent review in this issue can be found in [23].

5.5 Towards a unified vision of breakdown in La_2O_3-SiO_2 dual layers

In the previous part, it is presented that ***SILC conduction mode*** does not severely degrade the La_2O_3 insulation properties during stress as compared to SBD and HBD so that operation of La_2O_3-gated MOS devices operated at low biases can be guaranteed even with the SILC related increases in leakage current. Moreover, one of main issues for high-k gate stack is the charge trapping characteristics during reliability test. Initial observation of instability was studied through capacitance-voltage (C-V) characteristics in flat-band voltage change and current-voltage (I-V) characteristics in threshold voltage (Vth) change. Since electrons can be trapped and detrapped (***trapping-detrapping processes***) in the high-k/IL dielectrics with a minimal residual damage to its atomic structure [24], a Vth instability associated with electron trapping/detrapping in high-k layer can significantly affect the transistor parameters and complicate the evaluation of the effects of stress-induced defect generation phenomenon on the high-k gate stacks, which typically is not an issue in the case of SiO_2 dielectrics. Additionally, when ***soft-breakdown (SBD)*** events take place, the I-V or Vth instability characteristics of high-k gated MOS devices becomes difficult to analyze since the original tendency of Vth shifting towards a specified direction switches back to the opposite direction irrespective of the applied stress. Once the device reaches ***hard-breakdown (HBD)*** degradation, the operational lifetime of that device in particular expires leaving now space to the consecutive ***progressive breakdown (PBD)*** with stress that increases the levels of post-breakdown leakage currents. By putting all these

degradation modes together, the following data would result, fig. 5.15 A-B.

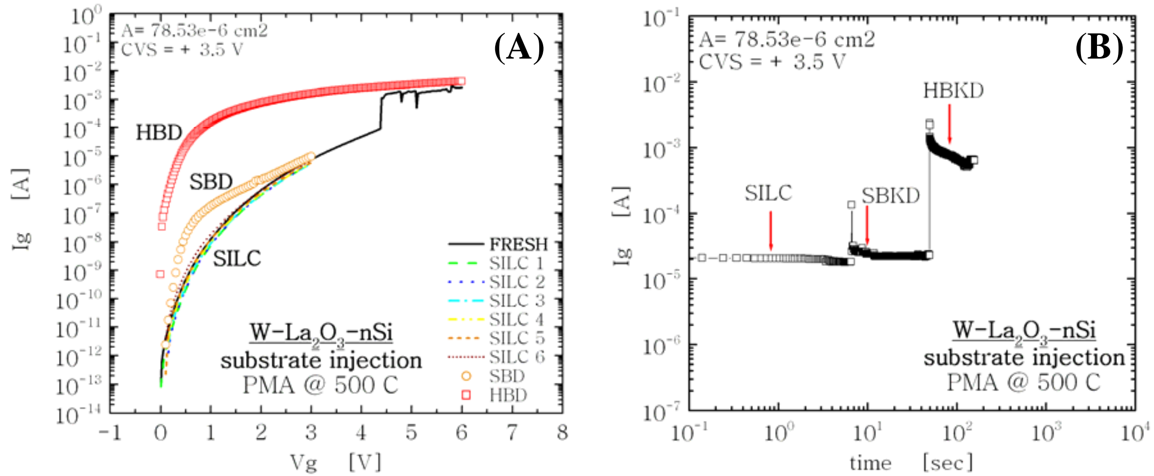


Fig. 5.15 (A) Ig-Vg plot for W/La_2O_3-IL stacked MOSCAP before and after continuous stress under substrate injection. The effect of several degradation modes on leakage current is shown. (B) Ig-time plot for W/La_2O_3-IL stacked MOSCAP before and after continuous stress under substrate injection. Again, the effect of the same degradation modes on leakage current is shown.

Under substrate injection (positive CVS), several degradation modes for La_2O_3-gated MOSCAP were found. From Ig-Vg measurements before and after stress (fig. 5.15A), it is found that even though SILC-mode degradation slightly increases the fresh levels of gate-leakage current, the continuous operation of La_2O_3-gated MOS devices can be guaranteed if only SILC conduction develops. When a SBD event takes place (seen as tiny jump in leakage current from the Ig-time plot), the occurrence of IL breakdown will change the direction of Vth shift and therefore the levels of Idsat as well. But the most noticeable event will be a higher increase in leakage current compared to SILC. Once the La_2O_3-IL stacked oxide reaches catastrophic or total breakdown (HBD), the insulating characteristics of the stacked oxide are lost and the consequent lateral propagation of the damaged area begin to take place if the stressing continues.

During the stressing of La_2O_3-IL gated MOS devices, it is highly possible that the occurrence of a single failure mode, a combination of them or the sequential development of all of them in the same oxide, will develop in accordance with the polarity, magnitude and duration of the stress itself. Since additional degradation-factors like temperature, cycle or frequency of the applied stress, drain voltage, etc., would further change the estimated projections for the lifetime of La_2O_3, the reliability analyses of La_2O_3 including as much of those factors as possible are necessary in order to develop more accurate physical models that is able to explain the obtained degradation phenomena.

References

[1] Lee S, Cho B, Kim J, Choi S. Quasibreakdown of ultrathin gate oxide under high field stress. In: Proc IEEE IEDM'94, 1994. p. 605–8.

[2] Houssa M, Nigam T, Mertens P, Heyns M. Model for the current–voltage characteristics of ultrathin gate oxides after soft breakdown. J Appl Phys 1998;84:4351–5.

[3] Houssa M, Nigam T, Mertens P, Heyns M. Soft breakdown in ultrathin gate oxides: correlation with the percolation theory of nonlinear conductors. Appl Phys Lett 1998;73:514–6.

[4] J.H Stathis, "Percolation models for gate oxide breakdown", J. Appl. Phys., 86 (10), pp. 5757-5766 (1999).

[5] T. Nguyen, P. Olivo, and B. Ricco, "A new failure mode of very thin (<50 A°) thermal SiO_2 films," in Proc. Int. Reliability Phys. Symp., 1987, p. 66.

[6] K. Naruke, S. Taguchi, and M. Wada, "Stress-induced leakage current limiting to scale down EEPROM tunnel oxide thickness," in IEDM Tech. Dig. 1988, p. 424.

[7] R. Moazzami and C. Hu, "Stress-induced current in thin silicon dioxide films," in IEDM Tech. Dig., 1992, p. 139.

[8] M. Kimura and H. Koyama, "Stress-induced low-level leakage mechanism in ultrathin silicon dioxide films caused by neutral oxide trap generation," in Proc. Int. Reliability Phys. Symp., 1994, p. 167.

[9] M. Hao, K. Lai, W. Chen, and J. Lee, "Reliability characteristics and surface preparation technique for ultra-thin (33 A° –87 A°) oxides and oxynitrides," in IEDM Tech. Dig., 1994, p. 601.

[10] D. DiMaria and E. Cartier, "Mechanism for stress-induced leakage currents in thin silicon dioxide films," J. Appl. Phys., vol. 78, no. 6, p. 3883, 1995.

[11] E. Rosenbaum and LF Register, "Mechanism of Stress-Induced Leakage Current in MOS Capacitors", IEEE Trans. on Elec. Dev., 44 (2), pp. 317-323 (1997).

[12] Lombardo S, La Magna A, Spinella C, Gerardi C, Crupi F. Degradation and hard breakdown transient of thin gate oxides in metal–SiO_2–Si capacitors: dependence on oxide thickness. J Appl Phys 1999;86:6382–91.

[13] Monsieur F, Vincent E, Roy D, Bruy┐ ere S, Vildeuil J, Pananakakis G, et al. A thorough investigation of progressive breakdown in ultra-thin oxides. Physical understanding and application for industrial reliability assessment. In: Proc IEEE IRPS'02, 2002. p. 50–60.

[14] Porti M, Nafria M, Aymerich X, Olbrich A, Ebersberger B. Propagation of the SiO_2 breakdown event on MOS structures observed with conductive atomic force microscopy. Microelectron Eng 2001;59:265–9.

[15] Porti M, Nafria M, Aymerich X, Olbrich A, Ebersberger B. Electrical characterization of stressed and broken down SiO_2 films at a nanometer scale using a conductive atomic force microscope. J Appl Phys 2002;91: 2071–9.

[16] Porti M, Nafria M, Blum M, Aymerich X, Sadewasser S. Breakdown-induced negative charge in ultrathin SiO_2 films measured by atomic force microscopy. Appl Phys Lett 2003;81:3615–7.

[17] M. Sato, I. Hirano, T. Aoyama, et al., "Impact of polarity and Hf concentrations on breakdown of HfSiON/SiO_2 gate dielectrics", Tech. Dig. Symp. On VLSI Tech., 2006.

[18] Ranjan, R.; Pey, K.L.; Tung, C.H.; Tang, L.J.; Groeseneken, G.; Bera, L.K.; De Gendt, S, "A comprehensive model for breakdown mechanism in HfO/sub 2/ high-k gate stacks", IEDM Tech. Dig., pp. 725-728 (2004).

[19] F. Monsieur et al., “A thorough investigation of progressive breakdown in ultra-thin oxides”, Proc. Int. Rel. Phys, Symp., pp. 45-54, 2002.

[20] C. Leroux et al., “Light emission microscopy for thin oxide reliability analysis”, Microelectron. Eng., vol. 36, pp. 297-300, 1997.

[21] Cester A, Cimino S, Paccagnella A, Ghidini G, Guegan G., “Collapse of MOSFET drain current after soft breakdown and its dependence on the transistor aspect ratio W=L”, In: Proc IRPS’03, 2003.

[22] Kaczer B, Degraeve R, Rasras M, Van de Mieroop K, Roussel P, Groeseneken G. Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability. IEEE Trans Electron Dev 2002;49:500–6.

[23] E. Miranda, J. Sune, “Electron transport through broken down ultra-thin SiO_2 layers in MOS devices”, Microelec. Rel., 44, pp. 1-23 (2004).

[24] E. P. Gusev and C. P. D’Emic, “Charge detrapping in HfO_2 high- gate dielectric stacks”, Appl. Phys. Lett. 83 (25) 5223 (2003).

Chapter 6

Comparison of the reliability for La_2O_3 and HfO_2-based gate oxides

6.1 Main reliability results for Hf-based oxides

6.2 Comparison of reliability between La_2O_3 and Hf-based oxides

6.3 Remaining problems for the reliability of La_2O_3 gate insulator MOSFETs

6.4 Summary

References

6.1 Main reliability results for Hf-based oxides

In the last years, the research of high-k materials has been mainly focused on the very specific Hf-based oxides because of their high thermal stability when deposited on silicon substrates, their high values of relative dielectric constant and conduction/valence band offsets to silicon, etc., which resulted in very good performance (low leakage current for low EOT, high carrier channel mobility, low Vth, etc) of the transistors fabricated with these dielectric materials. Nonetheless, the reliability evaluation of Hf-based oxides (mainly HfO_2, HfSiN, HfSiON) has produced a wide span of reliability results that although consistent, have demonstrated that these dielectrics present serious reliability issues related to their degradation when subjected to electrical stress. In the best of the cases, a broad look into some of the main important reliability results for Hf-based oxides has served to identify what are the main weak and strong points related to the degradation and breakdown of these dielectric materials and most importantly, we have been able to compare those results with the obtained by La_2O_3-gated devices.

The main reliability problems presented by these oxides include defects in the material which can lead to undesired transport through the dielectrics and trapping-inducing instabilities. Furthermore, the asymmetric gate band structure induces polarity effects on the leakage and thus, reliability.

A brief summary of the main reliability problems found for Hf-based gate oxides when subjected to a continuous electrical stress [1-10] are shown next.

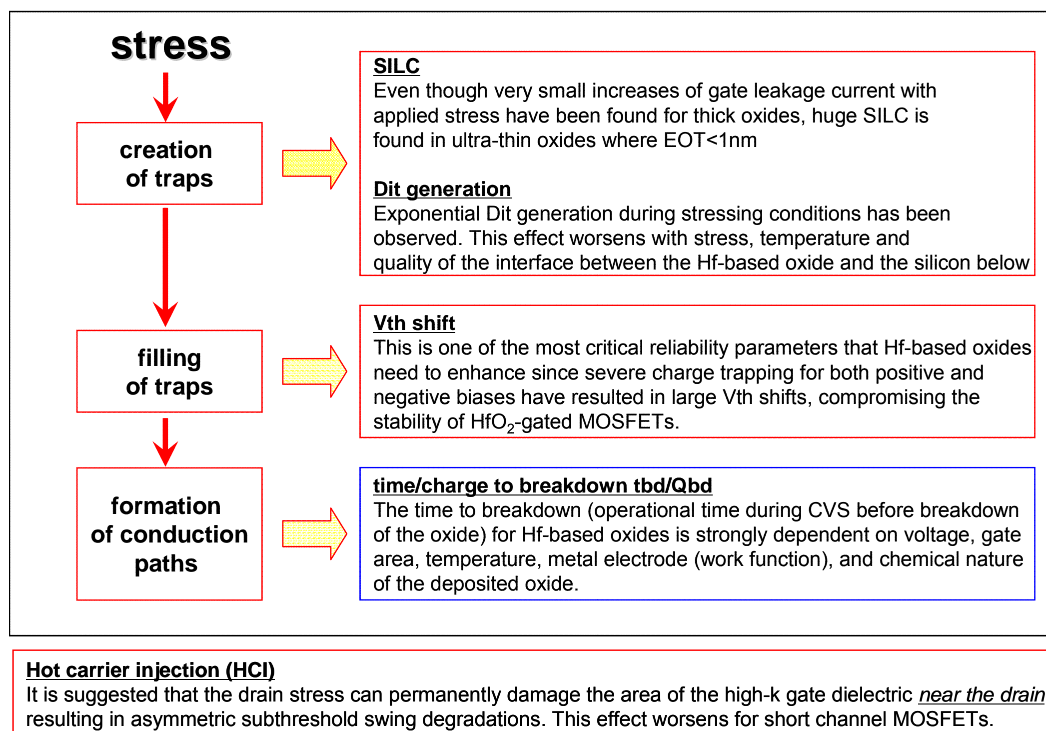


Fig. 6.1 Summary of the main reliability problems found for Hf-based oxides deposited on silicon [1-10]. Depending on the conditions of the stressing measurements and the advance of the electrical degradation, some reliability properties will be more compromised than others.

As shown in fig. 6.1, the duration and severity of stress will induce several mechanisms for the creation of defects within the bulk of HfO_2 and its interfaces with the interfacial layer, the silicon substrate and the metal gate. Even though the determination of the first degradation event and its relation to the affected reliability parameter (SILC, Dit generation, Vth shift, etc) is rather ambiguous and rather complex, there is strong evidence supporting the "staircase"-like degradation proposed in fig. 6.1. Initially, the creation of

traps induced by stress results in severe degraded SILC and Dit generation characteristics, once these traps are being filled by the injection of carriers, the Vth is shifted in accordance to the electrical nature of the trapped carrier (holes or electrons). Nevertheless, by making improvements in the deposition and post-deposition processing of Hf-based oxides, good results have been obtained especially for the later HfSiON oxides, where a compositional profiling of the material along with a combination of the suitable metal gates, has led to further minimization on Vth shifts. Once the duration (or intensity) of the stressing increases, the formation and consequent interconnection of internal conductive paths lead to the final hard breakdown of the oxides. In this respect, very promising results have been obtained demonstrating that Hf-based oxides can withstand long-term operational conditions before the final breakdown occurs. On the other hand, by stressing the oxides with both gate and drain electric fields simultaneously, the injection of hot carriers near the drain side of the HfO_2-gated short-channel MOSFET devices will present the more serious case of charge trapping and thus, Vth instability. Since the hot-carrier instability is permanent (it has been demonstrated that Vth shift by gate field-only stressing can be partially recovered), the degradation presented under these conditions is still a major issue for the processing and device development in order to increase the reliability of Hf-based gate oxide materials.

The following section presents one-by-one, the reliability results of Hf-based oxides. First, the *SILC degradation* is shown in fig. 6.2. As we can see, even though very small increases of gate leakage current with applied stress have been found for thick oxides,

huge SILC is found in ultra-thin oxides where EOT < 1 nm.

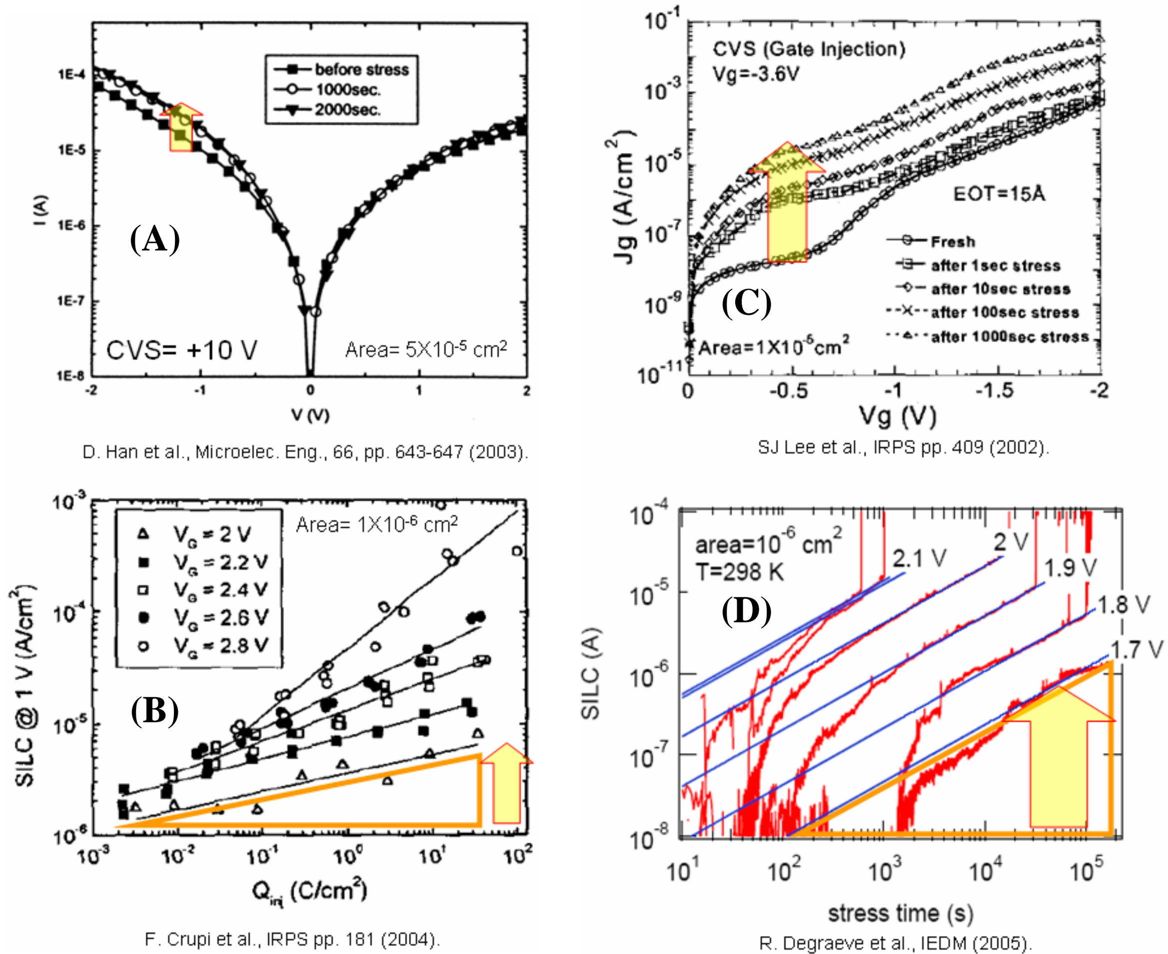


Fig. 6.2 SILC characteristics for several HfO_2-gated MOS devices [11-14].
(A) SILC characteristic for the Pt/HfO_2/Si system. EOT= 2.9 nm.
(B) SILC characteristic for the poly-Si/HfO_2/Si system. EOT= 1.8 nm.
(C) SILC characteristic for the poly-Si/HfO_2/Si system. EOT= 1.5 nm.
(D) SILC characteristic for the TaN/HfO_2/Si system. EOT= 0.9 nm.

From figures 6.2 B and D, it is clearly seen that exponential dependence of SILC with injected charge or stressing time develops. This effect is worse for the HfO_2 film with EOT < 1 nm, which presents more pronounced slope. Fig. 6.3 A–B shows the results of

interface-states (Dit) generation for HfO_2 whereas fig. 6.4 A–B shows the corresponding *Vth instability* characteristics during several electrical stressing conditions.

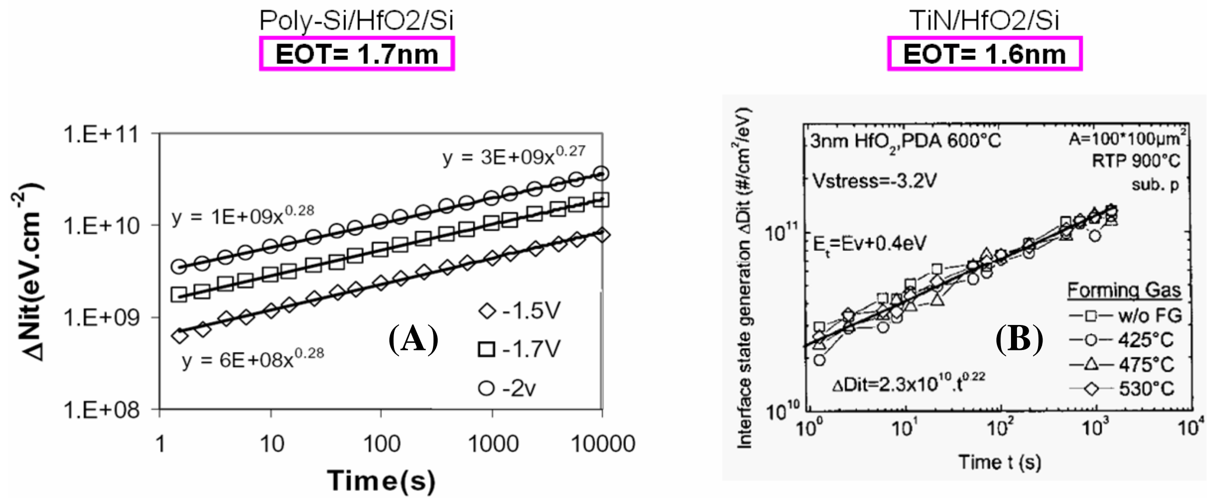


Fig. 6.3 Dit-generation characteristic for HfO_2-gated MOS devices with similar EOT [15-16].
(A) Interface-state Dit increase with stress time for the poly-Si/HfO_2/Si system. EOT= 1.7 nm.
(B) Interface-state Dit increase with stress time for the TiN/HfO_2/Si system. EOT= 1.6 nm.

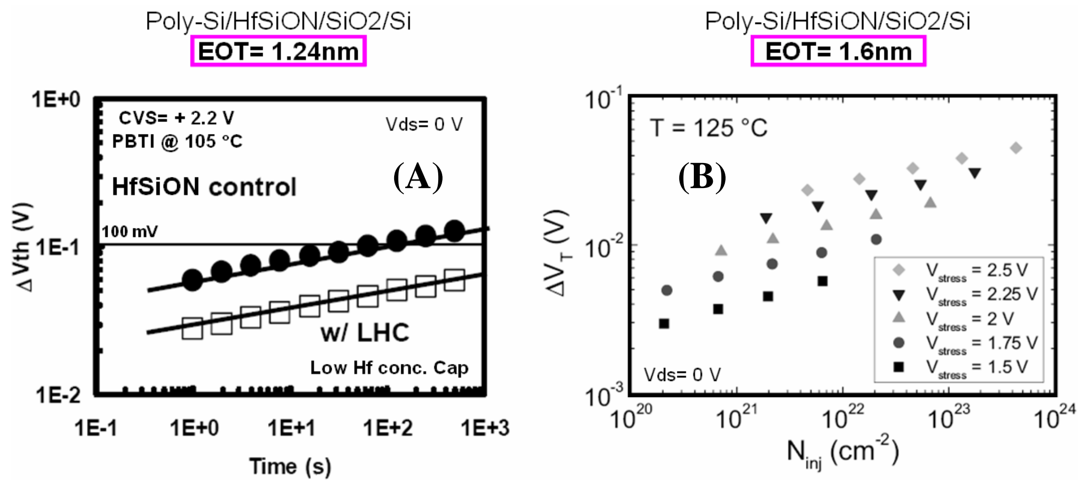


Fig. 6.4 Vth shift characteristic for HfSiON-gated MOS devices [17-18].
(A) Vth shift versus stressing time for the poly-Si/HfSiON/Si system. EOT= 1.24 nm.
(B) Vth shift versus injected charge density for the poly-Si/HfSiON/Si system. EOT= 1.6 nm.

We can see that there is both exponential Dit generation and exponential Vth shift during the stressing of Hf-based oxides on silicon. Both of these degradation effects are worsened (higher Dit generation and Vth shift is observed) with stress, temperature and quality of the interface between the Hf-based oxide and the silicon below. Especially, the highly severe charge trapping during both positive and negative biases results in large Vth shifts, thus compromising the stability of these MOSFETs devices.

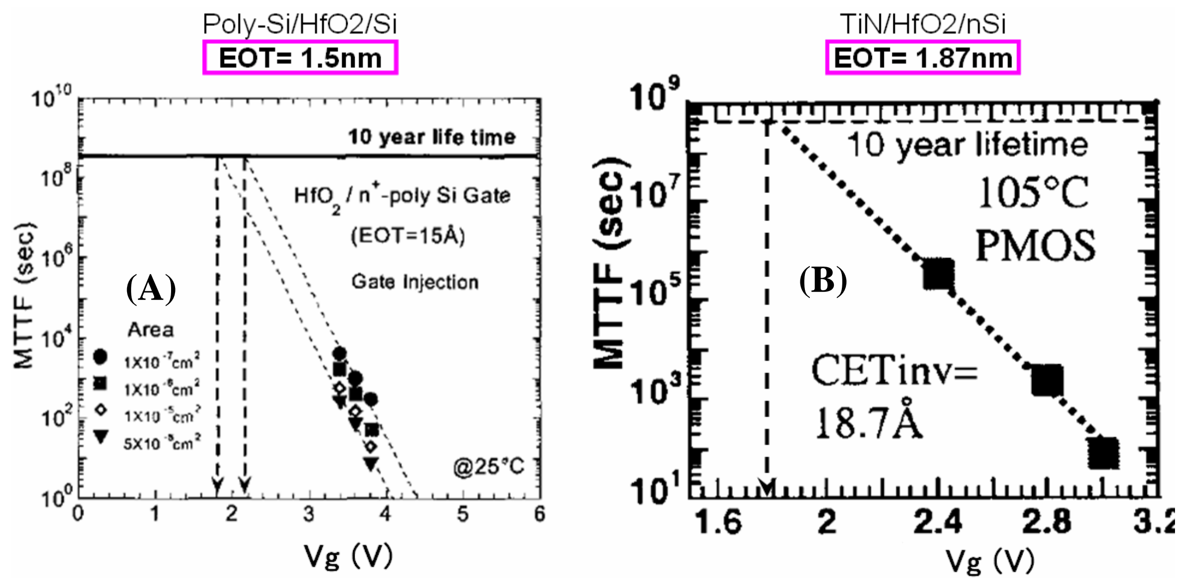


Fig. 6.5 Lifetime projection based on the time to breakdown data for HfO_2-gated MOS devices [19-20]. (A) A 10-years continuous operation is guaranteed for the poly-Si/HfO_2/Si system. EOT= 1.5 nm. (B) A 10-years continuous operation is also guaranteed for the TiN/HfO_2/Si system. EOT= 1.87 nm.

Fig. 6.5 A–B shows that by extrapolating the *time to breakdown* data of HfO_2 -gated MOS capacitors and small area pMOSFET devices (the MOSFET with higher temperature stressing conditions), the continuous operation of both samples is guaranteed before the complete breakdown of the high-k stack. It is interesting to note that by stressing

very small area devices (like those presented by the pMOSFET) with higher temperature conditions, the lifetime is not severely shortened since fewer number of defects is expected when smaller area sizes are used.

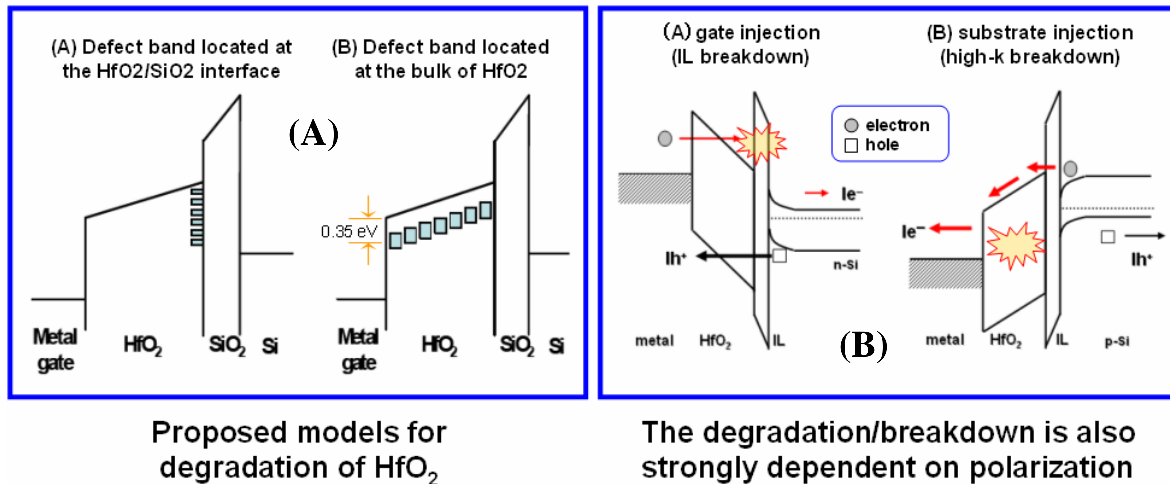


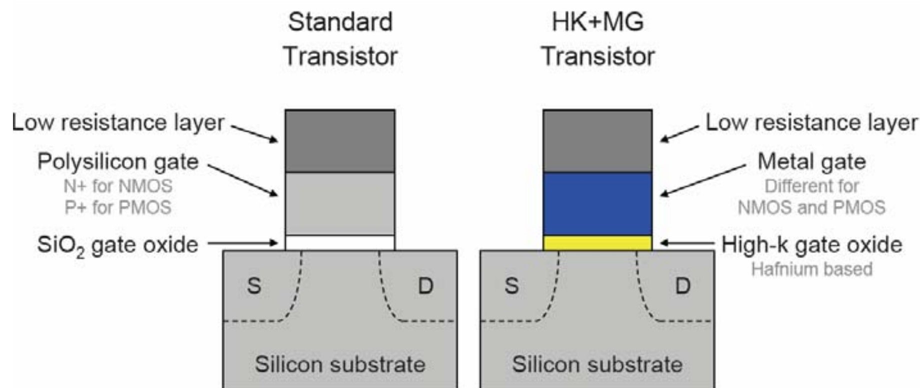
Fig. 6.6 (A) Proposed models for the degradation of HfO_2-gated MOS devices [3, 15, 21-24]. (B) When the degradation continues, the breakdown is modeled differently depending mainly on the polarity of the stress applied (gate and substrate injection of electrons)

Fig. 6.6 A shows the *proposed models* found in the literatures [3, 15, 21-24] regarding the degradation of HfO_2-based oxides. The degradation of these oxides is influenced by numerous parameters namely bias, temperature, time and stack structure (presence and/or chemical composition of the IL) among others. The magnitude of Vth instability in SiO_2/HfO_2 dual-layer gate dielectrics is shown to depend strongly on experimental conditions too. Taking into account this polarity and time dependence, a simple model has been proposed utilizing a defect-band in the HfO_2 layer located at the energy level the silicon and hafnia conduction band (fig. 6.6 A-a). This model has some

advantages since it explains qualitatively, both for negative and positive gate bias, the charging and discharging of defects by tunneling through the interfacial SiO_2 layer. At the same time, studying the mobility degradation in high-k MOS devices, Morioka et al. [24] proposed that hysteresis traps are located at the HfSiO/SiO_2 interface as shown in Fig. 6.6 A-b. Thus, two types of models are proposed in the literature. The physical and chemical nature of the electron traps in the HfO_2/SiO_2 structure remains unclear because the performance of high-k gate dielectrics is likely to be affected by various defects. Among these defects, ***interstitial oxygen atoms and positively charged oxygen vacancies*** are suspected to play a significant role in the observed instability since they can trap electrons from the bottom of the hafnia conduction band and from silicon.

Moreover, the breakdown of HfO_2-based oxides is mainly discussed in terms of the polarity of the applied stress [25-30], see fig. 6.6 B (a-b). For gate injection conditions, it has been proposed that the IL is mainly broken down whereas the high-k layer itself is broken down for substrate injection conditions, though further research is required. In all likelihood, the layer responsible of the breakdown event seems to be the high-k layer. Accurate statistical analyses, with both IL and high-k thickness layer dependences, remain crucial in order to understand the breakdown during this stressing regimes. Lastly, it should be noted that the above information is only provided by the published literatures. In January 2007, Intel just announced the production of Hf-based high-k gate insulator microprocessors with 45 nm technology. In the announcement there, it was projected that Hf-based high-k gate oxide with reliability requirements as shown in fig. 6.7 (for more details see Intel's web page at

www.intel.com/technology/silicon/high-k.htm). From the transistor performance written in the announcements as shown in fig. 6.7, the EOT value is estimated to be at least less than one nanometer. Thus, reliability problem for HfO_2-based gate oxide are estimated to have been already solved for the commercial products, although academic papers published by research groups demonstrate many reliability problems.



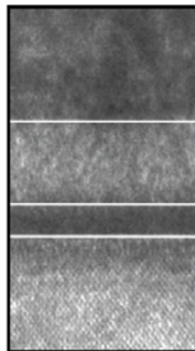
✓ Integrated 45 nm CMOS process

✓ High performance

✓ Low leakage

✓ Meets reliability requirements

✓ Manufacturable in high volume



Low Resistance Layer

Work Function Metal
Different for NMOS and PMOS

High-k Dielectric
Hafnium based

Silicon Substrate

Process Name:	P1262	P1264	P1266	P1268	P1270
Lithography:	90 nm	65 nm	45 nm	32 nm	22 nm
1st Production:	2003	2005	2007	2009	2011

Advantage of Intel's 45 nm technology (compared to its 65 nm technology)

- 2X improvement in transistor density
- 30% reduction in transistor switching power
- 20% improvement in transistor switching speed
- 10X reduction in gate oxide leakage power

Fig. 6.7 Structural features of the metal gate/high-k (Hf-based) stacks used by Intel and which is scheduled for commercial production of MOSFETs in the 45nm node during this year.

6.2 Reliability comparison between La_2O_3 and HfO_2

6.2.1 SILC degradation

This section compares the main reliability results obtained for La_2O_3-gated devices with those of Hf-based oxides. First, the ***SILC degradation*** is compared [31-33].

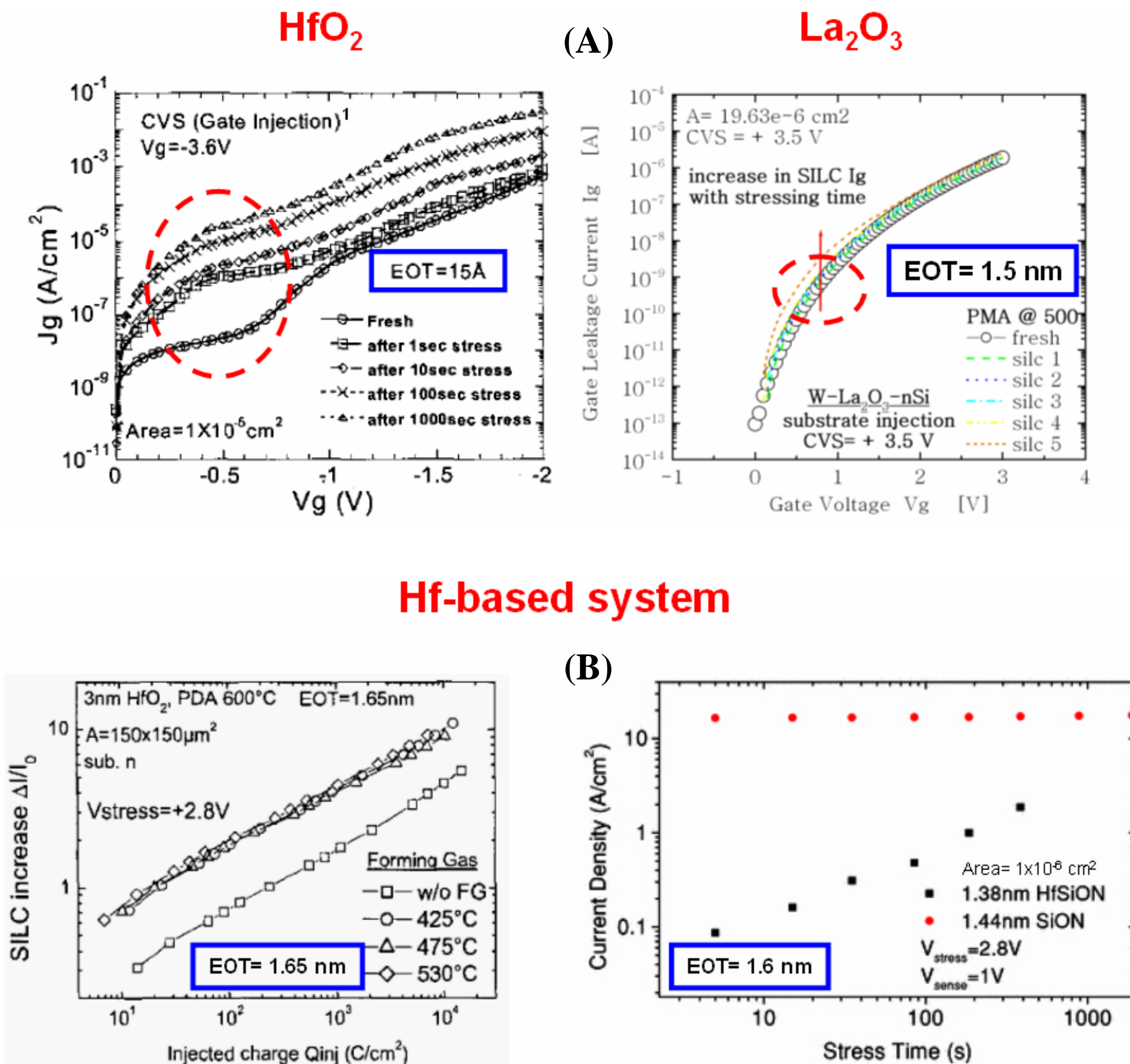


Fig. 6.7 (A) Less SILC degradation is found for La_2O_3 compared to HfO_2-gated MOS devices [31].
(B) SILC degradation for Hf-based oxides only. Exponential increase in Jg is clearly observed [32-33].

By comparing SILC of MOS devices with similar EOT, less degradation in gate leakage current after stress is found for La_2O_3-gated MOSCAP compared to HfO_2 (see fig. 6.7 A) and this effect gets worse for thinner films (especially for EOT < 1nm). By considering other results in the literature with closely similar EOT for HfO_2-gated devices, the exponential increase in SILC degradation is then clearly observed (see fig. 6.7 B).

6.2.2 Interface-states Dit generation

Very similar are the results for the ***Dit generation*** during stressing measurements of HfO_2-gated devices, see fig. 6.8. Here, the exponential increase in Dit during stress is clearly observed even for samples annealed after relatively high forming gas PMA temperatures [32]. Even though La_2O_3 presents an initially higher density of interface –states, Dit, generation of additional Dit during stress is lower compared to HfO_2.

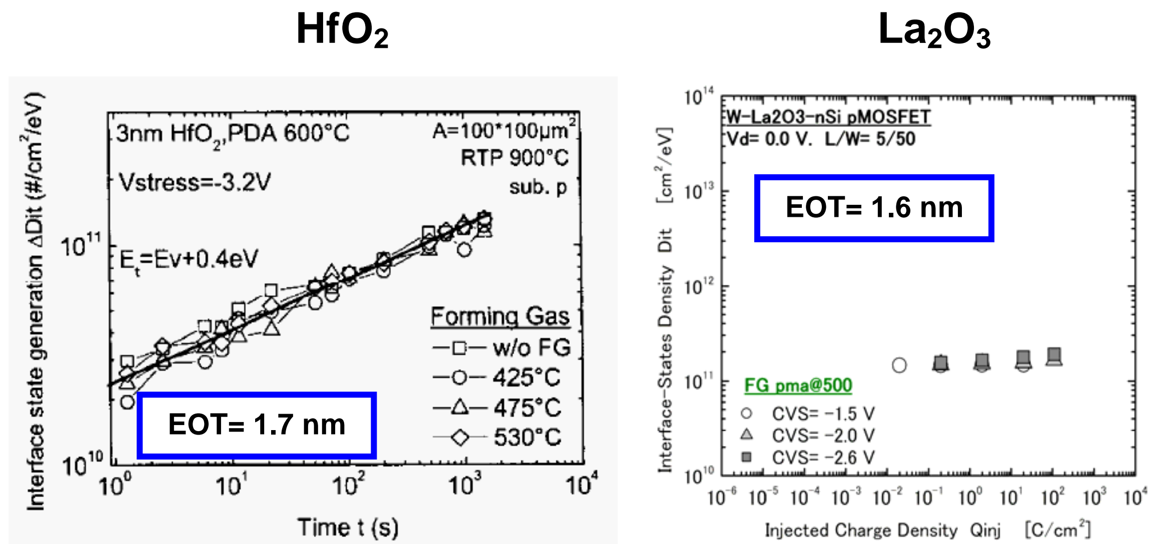


Fig. 6.8 Comparison of the observed Dit generation between HfO_2 and La_2O_3-gated devices during stress [32].

6.2.3 Threshold voltage Vth shift

For La_2O_3, additional ΔVth after electron injection is minimized, which is in contrast to the exponentially dependence of Vth shift with stress for HfO_2 [34], see fig. 6.9.

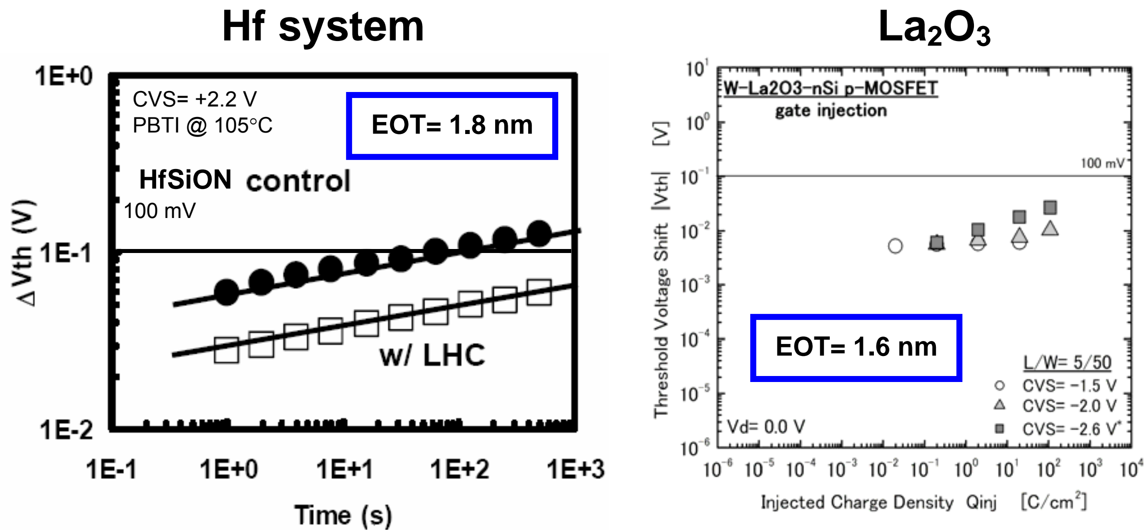


Fig. 6.9 Comparison of the observed Vth shift between HfO_2 and La_2O_3-gated devices during stress [34].

6.2.4 Time to breakdown tbd

On the other hand, a 10-year extrapolation of the time to breakdown data for both dielectrics ensures the operation of MOSFETs gated with both dielectrics even in the voltages applied to their gates exceed more than 1 V. In the case of La_2O_3, slightly higher gate voltages (compared to those found for HfO_2 with same EOT [35]) can be applied before the final breakdown of the dielectric film.

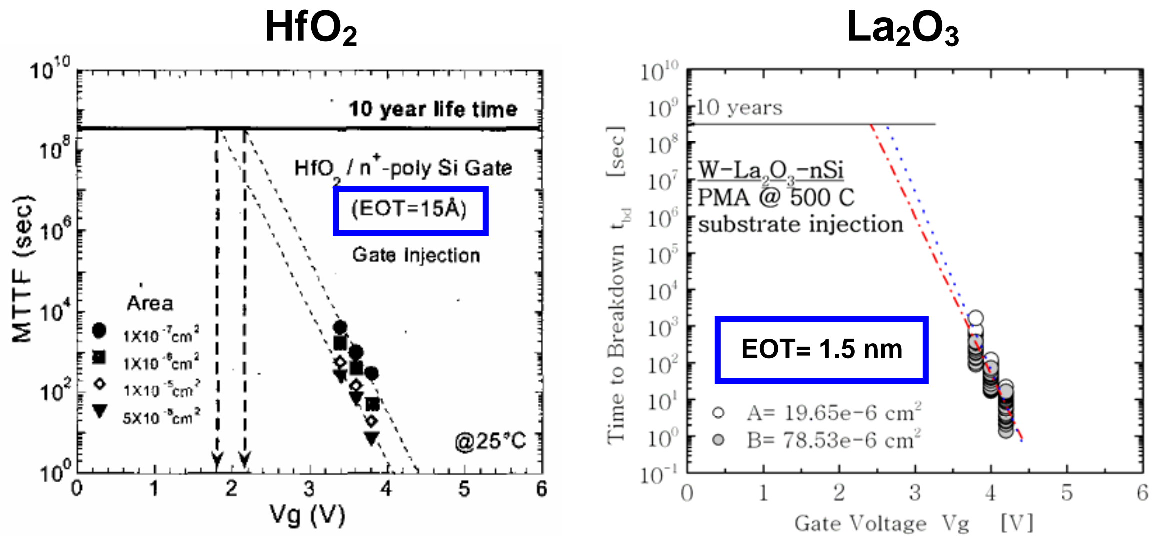


Fig. 6.10 Comparison of the observed time to breakdown data between HfO_2 and La_2O_3-gated devices [35].

6.2.5 Breakdown models for substrate and gate injection

The proposed models for the breakdown of La_2O_3 and HfO_2 are both strongly dependent on the polarity of the applied stress [36-37]. During substrate injection, a Hf-based system experiences high-k bulk breakdown whereas La_2O_3 initially shows IL breakdown followed by La_2O_3 bulk breakdown. During gate injection, an Hf-based system mostly experiences IL breakdown whereas La_2O_3 shows complete IL plus bulk La_2O_3 breakdown simultaneously, see fig. 6.11 A-B.

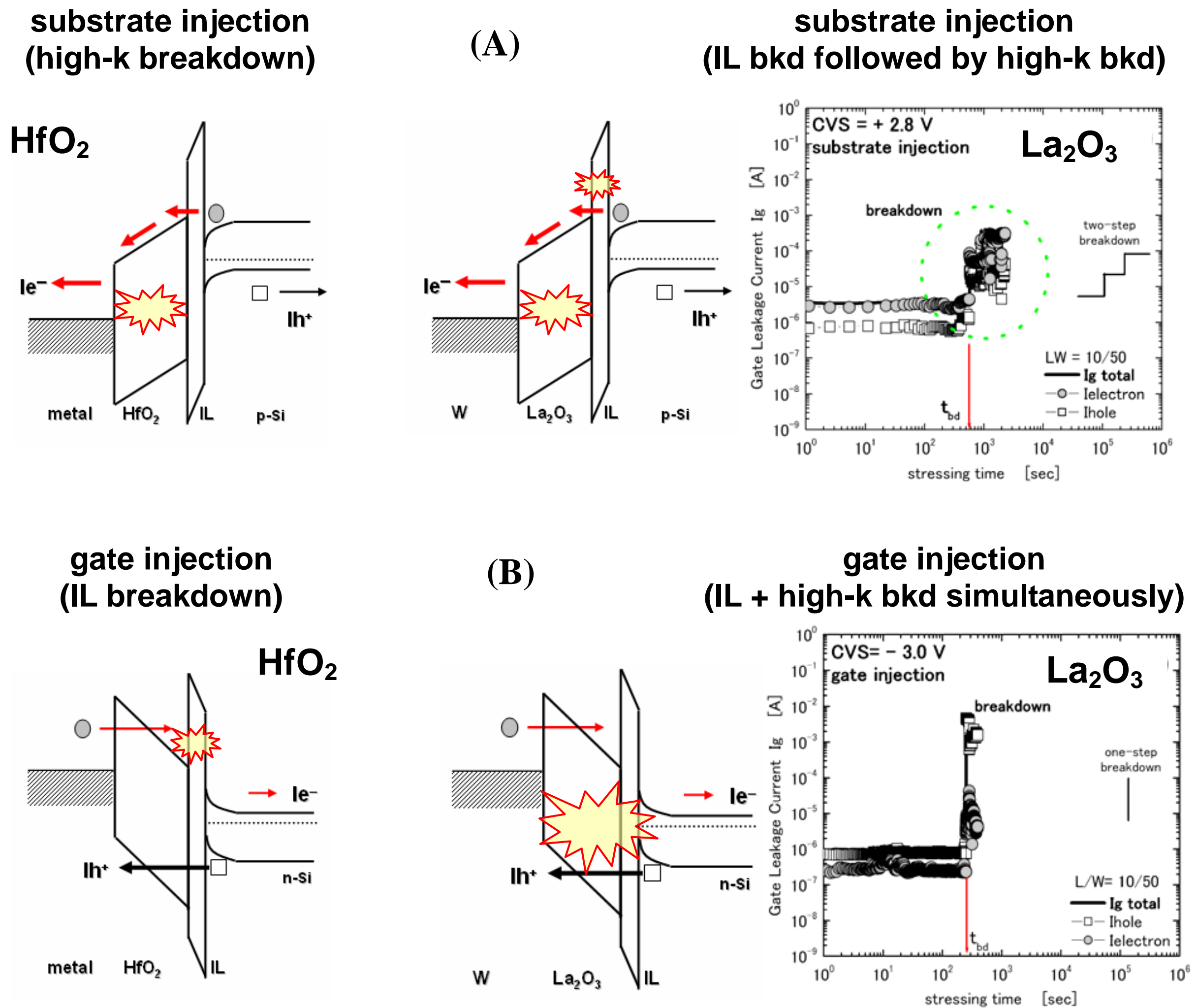


Fig. 6.11 (A) Comparison of the breakdown models for HfO_2 and La_2O_3during substrate injection conditions. (B) Comparison of the breakdown models for HfO_2 and La_2O_3 during gate injection conditions.

In summary, the comparison of the typical reliability results for both dielectric films are summarized as follows. Table 6.1 shows the comparison of the reliability for HfO_2-based and La_2O_3 with the EOT value of 1.5 nm. In general, La_2O_3 shows better reliability than Hf-based oxide. Thus, La_2O_3 dielectrics do not seem to have a fundamental reliability problem to be used as a gate insulator.

Even though La_2O_3 presents better reliability properties compared to those for HfO_2-based devices, the reliability characterization for La_2O_3 has been done only at room temperature. Therefore, as already described, the reliability test with small gate length MOSFETs were not carried out in this study. Thus, there are no results of the hot-carrier injection reliability for MOSFETs thus there are no data for La_2O_3 hot-carrier reliability.

Table 6.1 Summary of the reliability results for HfO_2 and La_2O_3-gated MOS devices.

Material / Property	La_2O_3* EOT [nm]	HfO_2-based EOT [nm]
SILC degradation	Estimated to be acceptable [1.5 nm]	To be a problem [1.5 nm]
Dit generation	Estimated to be acceptable [1.6 nm]	To be a problem [1.7 nm]
Vth shift	Estimated to be acceptable [1.6 nm]	To be a problem [1.8 nm]
t_{bd}, Q_{bd}	Estimated to be acceptable [1.5 nm]	Estimated to be acceptable [1.5 nm]
HCI	?	Very poor

* Higher temperatures during reliability evaluation are needed.

Regarding the comparison of the reliability of the HfO_2-based and La_2O_3 gate oxides with the EOT value of less than 1 nm, the reliability of HfO_2-based oxide seems to be much worse than that of La_2O_3 as shown in table 6.2. However, as described in section 6.1, Intel's Hf-based gate oxides are estimated to establish the sufficiently high reliability with the EOT of less than 1 nm. Thus, the HfO_2-based oxides reliability problems can be basically solved even though the published papers described those problems. Probably, the reliability of La_2O_3 gate insulator will be solved by the time when the La_2O_3 is introduced

into the commercial devices, as the case of Hf-based oxides.

Table 6.2 Summary of the reliability results for HfO_2 and La_2O_3-gated MOS devices when EOT < 1 nm.

Reliability characteristics at EOT < 1nm regime	HfO_2	La_2O_3
SILC degradation	Very poor	To be a problem
Dit generation	Very poor	?
Vfb, Vth shift	Very poor ～ To be a problem	To be a problem ～ Estimated to be acceptable
tbd, Qbd	Estimated to be acceptable	Estimated to be acceptable

Reliability tests at different temperature conditions are necessary. In another words, negative-bias temperature instability (NBTI) and positive-bias temperature instability (PBTI) were not measured in this study and those measurements are necessary to confirm the reliability of La_2O_3.

6.3 Remaining problems for the reliability of La_2O_3 gate insulator MOSFETs

Finally, this chapter closes with a brief summary of the remaining problems found for La_2O_3 with respect to its reliability characteristics. Even though the following list may not be complete, it is quite valuable in which provides a good look at the fundamental

reliability problems of La_2O_3 and also, provides an insight into the expected solutions in order to increase the reliability properties of La_2O_3-gated MOS devices.

1. Reliability tests in different temperatures. Only room temperature test were done. NBTI, PBTI tests were not done.

2. More evaluations of reliability for samples with EOT < 1nm, and clarification of problems at EOT < 1nm. At this moment, only SILC was found to be the problem.

3. Reliability tests for smaller size capacitors. The smallest capacitors used for the reliability tests were that with a 100 μm diameter.

4. Reliability tests for small gate length (Lg < 50nm) MOSFETs. Especially, hot carrier instability testing is needed.

5. More studies for degradation mechanism.

6. More studies for the optimization of processing conditions for enhanced reliability. At this moment, it was found that higher annealing temperatures, in-situ gate metallization and La_2O_3 deposition in oxygen ambient improve the reliability. Also it was found that W gate electrode is better than that of Al for reliability.

6.4 Summary

In order to predict the reliability of the La_2O_3 dielectrics for use of the gate insulator, the published data for that of HfO_2-based oxides were examined and compared with that of the La_2O_3.

In general, the La_2O_3 dielectrics show higher reliability than that of HfO_2-based dielectrics, although some of the reliability evaluations have not been carried out for the La_2O_3. The published data in the journal and the conference predict not sufficient reliability for the Hf-based oxide to be used in commercial products. However, Intel announced Hf-based high-k gate oxide introduction into the 45 nm CMOS with sufficiently high reliability which meets the commercial production thus the reliability of the Hf-based oxides with EOT down to sub 1 nm seems to have been already established.

At this moment, any fundamental problems for the reliability of La_2O_3 dielectrics have not been found by this study. Thus, it is expected that the La_2O_3 reliability will meet the requirements for the production by the time when it is introduced into commercial devices.

References

[1] John Robertson, *Rep. Prog. Phys*. **69** 327–396 (2006).

[2] M Houssa et al., *Mat. Sci. and Eng*., **51** (4-6) pp.37-85 (2006).

[3] G Ribes et al, *Trans. on Dev. and Mat. Rel*., **5** (1) pp. 5-19 (2005).

[4] Critical Reliability Challenges for the ITRS. SEMATECH (2004).

[5] S Jakshick et al., *Int. Integ. Rel. Workshop* pp. 125-128 (2006).

[6] JYC Yang et al., *Int. Integ. Rel. Workshop* pp. 179-181 (2006).

[7] J Liu et al., *IEEE EDL* **28** (1) pp. 11-13 (2007).

[8] PK Hurley et al., *Electrochem. Sol. St. Lett*. **8** (2) pp. G44-G46 (2005).

[9] M Terai et al., *Trans. on Elec. Dev*., **54** (3) pp. 483-491 (2007).

[10] JH Sim et al., *IEEE Trans. on Dev. Mat. and Rel*., **5** (2), pp. 177-182 (2005).

[11] D. Han et al., *Microelec. Eng*., **66**, pp. 643-647 (2003).

[12] F. Crupi et al., *IRPS* pp. 181 (2004).

[13] K Iwamoto et al., *Sol. Stat. Electron*., **50** (6) pp. 999-1003 (2006).

[14] R. Degraeve et al., *IEDM* (2005).

[15] G. Ribes et al., *ESSDERC* pp. 435 (2005).

[16] X. Garros et al., *IRPS* pp. 55 (2005).

[17] M Sato et al., *IEDM* (2006).

[18] F Crupi et al., *Microelec. Eng*., **80** pp. 130 (2005).

[19] SJ Lee et al., *IRPS* pp. 409 (2002).

[20] SB Samavedam et al., *Int. Symp. On VLSI Tech*., pp. 24 (2002).

[21] E Wu et al., pp. 36, *IRPS* (2006).

[22] M Sato et al., *SSDM* A26 (2005).

[23] A Kerber et al., *IEEE Electron Dev. Lett*., **24** (2). (2003).

[24] A Morioka et al., *VLSI Symp*., (2003).

[25] X Garros et al., *IRPS* pp. 176-180 (2004).

[26] G Ribes et al., *WODIM* (2004).

[27] R Degraeve et al., *IEDM* (2003).

[28] T Kauerauf et al., *IEDM* pp. 521-524 (2002).

[29] Y Harada et al., *VLSI* (2002).

[30] DJ DiMaria et al., *APL* **70** pp. 2708-2710 (1997).

[31] SJ Lee et al., Time-dependent Dielectric Breakdown in poly-Si CVD Hf02 Gate Stack, pp. 409. *IRPS* (2002). The University of Texas, Austin.

[32] X Garros et al., Interface states in HfO_2 stacks with metal gate, pp. 55 *IRPS* (2005). CEA-LETI.

[33] R O'Connor et al., Low Voltage SILC in SiON and HfSiON gate dielectric layers, *Semicond. Sci. and Technol*. **20** No 8, pp. 668-672 (2005). IMEC.

[34] M Sato et al., "Impact of Very Low Hf Concentration (Hf=6%) Cap Layer on Performance and Reliability Improvement of HfSiON -CMOSFET with EOT Scalable to 1nm", *IEDM* (2006). Toshiba, NEC and SONY.

[35] SJ Lee et al., Time-dependent Dielectric Breakdown in poly-Si CVD Hf02 Gate Stack, pp. 409. *IRPS* (2002). The University of Texas, Austin.

[36] R Degraeve et al., Effect of bulk trap density on HfO_2 reliability and yield, pp.3851. *IEDM* (2003). IMEC.

[37] T Kauerauf et al., Towards understanding degradation and breakdown of SiO_2/high-k stacks. pp. 521-524. *IEDM* (2002). IMEC.

Chapter 7

Conclusions

7.1. Conclusions

7.2. Recommendations for future works

7.1 Conclusions

In this work, the reliability characteristics of Metal/ La_2O_3-IL stacked structures on silicon were investigated. It was demonstrated that La_2O_3 suffer from high charge trapping characteristics: 1) if the La_2O_3 deposition process is not optimized, 2) if the as-deposited oxide is not properly annealed, 3) if the suitable metal material is not used as the gate electrode and 4) if reproducibility during stressing measurements is not ensured. Besides, since the deposition of La_2O_3 directly on silicon surfaces lead to unavoidable lower-k interfacial layer IL formation, the consideration of a dual-oxide stacked structure for charge trapping analysis is necessary in order to model the degradation and breakdown phenomena occurring during the stressing of the samples.

The primary aim of introducing high-k materials into CMOS technologies is to reduce the gate leakage current. The magnitude of the leakage reduction depends on the material properties, gate-stack structure, and process conditions (IL thickness, dielectric constant of resulting stack after annealing, band-gap, band-alignment, post-deposition treatment, gate electrode, etc.).

From ***La_2O_3-gated-MOSCAP results***, a higher-k gate oxide stack could be fabricated by using tungsten-based electrodes. This was attributed to the less reactive interface formed between this metal and the La_2O_3 underneath. The aluminum-based system showed a lower-k value in La_2O_3, which indicates the formation of a lower-k Al_2O_3 interfacial layer, especially by PMA. From the TDDB data, a 10-year lifetime for La_2O_3 is guaranteed both by using the linear and reciprocal model. Additionally, the

evaluation was done for the electrical and reliability characteristics of W- La_2O_3-nSi stacks with relatively thick and thin La_2O_3 film (EOT>1.5nm and EOT<1nm) after annealing. Compared to PDA samples, PMA samples showed better reliability characteristics so that important parameters like higher endurance to Vfb shift, longer lifetimes and higher charge to breakdown were obtained. A very interesting result was that the shift in Vfb after positive stress (substrate injection) for La_2O_3-gated MOS devices: changes from negative to positive direction when the magnitude of the constant voltage stress CVS is increased or when a soft-breakdown event occurs during the stressing measurement. This phenomenon is also present for the shifts in Vth of nMOSFETs devices after positive stressing.

The deposition of La_2O_3 under UHV and O_2 flow (in an effort to minimize oxygen deficiency during the deposition) along with *in-situ* deposition of tungsten on La_2O_3 was performed in order to reduce exposure of the La_2O_3 surface to environment contamination. All these were carried out in order to obtain an improved interface between La_2O_3 and silicon. After the PMA treatment done on these samples, a higher PMA temperature for La_2O_3 enhanced the formation of a SiO_2-based interfacial layer. All these procedures combined while remaining a very-thin physical thickness of La_2O_3 resulted in a more reliable W- La_2O_3 stack. It is thought that the formation of a very thin SiO_2-based interfacial layer could help to improve the reliability characteristics of metal/high-k stacked devices. However, the increase in EOT by lower-k interfacial layer formation is an issue that must be addressed since small EOT less than 1 nm requires very thin dielectrics and thus the controllability and quality of this interfacial layer becomes crucial. The lowest Vfb shift after stress was achieved for the

W/LaSixOy-SiO_2 stacked structure which formed after PMA at 500°C in N_2.

The dependence of device's area on the electrical degradation and breakdown of W-La_2O_3 was investigated. It was found that the post-breakdown characteristic of Ig for all samples does not show a direct relationship with area, which suggests a highly localized nature of the breakdown-spot distribution. Besides, even though smaller area devices produce longer lifetimes to breakdown during higher-voltage stressing conditions, the stressing with lower CVS does not break down the oxides but the damage induced in the dielectrics results in an inversely proportional dependence of SILC increase with respect to gate area. Also, the occurrence of a progressive breakdown (PBD) phenomenon for La_2O_3 after HBD was related to the increase in the lateral propagation of the damaged area (increase in the total size of the breakdown spot) as a result of the constant electrical stress. Even though thinner La_2O_3 with EOT $<$ 1nm showed highly degraded SILC characteristics under high CVS conditions, the expected operation voltages for future generation devices are so low that the reliable operation of La_2O_3-gated MOS devices before HBD can be expected.

By using ***La_2O_3-gated MOSFET*** structures, useful information has been provided in order to determine the effect that a positive or negative CVS has on the reliability properties of La_2O_3-gated transistors. By injecting different densities of charge into the oxide structure, the shift in Vth and the respective increases in interface-state density Dit were evaluated and compared between nMOSFET and pMOSFET devices. For nMOSFET devices, we obtained an electric field-dependent shift in Vth similar to the electric field-dependent shift in Vfb for MOSCAP on n-type

silicon substrates. In some cases, the occurrence of soft-breakdown (SBD) events for higher CVS conditions lead to a change in the direction of Vth and Idsat as well. By including a constant drain voltage together with the positive CVS, a higher degradation on Vth is found. In the case of pMOSFETs stressed with negative CVS, only negative ΔVth are observed for all stressing conditions, being Vth dependent on the density of injected charge only. This negative change in ΔVth is related to the trapping of positive charge within the La_2O_3 and its interfaces. Additionally, Dit measurements were performed after stress. Strong correlation between Dit and ΔVth was found for the case of pMOSFETs, while for nMOSFETs there appears to be no correlation after stress.

The effect of substrate and gate injection on the degradation and breakdown of La_2O_3-IL stacked MOSFETs was investigated by using carrier separation (CS) measurements. It was shown that the major contributor to leakage current under gate (substrate) injection comes by the injection of holes (electrons) via the inverted channel. Under the substrate injection, electrons from the channel were the main contributors to Ig and a two-step breakdown behavior was observed. For the gate injection, holes were the main contributors to Ig and a one-step breakdown behavior was observed. By comparing the Ig post-breakdown characteristics for both substrate and gate injection conditions, it is thought that the area size of the breakdown spot after gate injection is larger than that after substrate injection, thus suggesting that the stress-induced damage is also strongly polarity dependent.

Under the substrate injection, several ***degradation modes for La_2O_3-gated MOSCAP*** were found. It is found that even though SILC-mode degradation slightly

increases the fresh levels of gate leakage current, the continuous operation of La_2O_3-gated MOS devices can be guaranteed if only SILC conduction develops during stressing. When a SBD event takes place, the occurrence of IL breakdown changes the direction of Vth shift and therefore the levels of Idsat as well. But the most influencial event will be a significant increase in gate leakage current not by SILC. Once the La_2O_3-IL stacked oxide reaches catastrophic or total breakdown HBD, the insulating characteristics of the stacked oxide are lost and the consequent lateral propagation of the damaged area begin to take place if the stressing condition is not stopped. During the stressing of La_2O_3-IL gated MOS devices, it is likely that the occurrence of a single failure mode, a combination of them or the sequential development of all of them in the same oxide, will develop in accordance with the polarity, magnitude and duration of the stress itself. Since additional degradation-factors like temperature, cycle or frequency of the applied stress, drain voltage, etc., would further change the estimated projections for the lifetime of La_2O_3, the reliability analyses of La_2O_3 including as much of those factors as possible are necessary in order to establish more accurate physical models that is able to explain the obtained degradation phenomena.

By comparing the reliability properties of La_2O_3-gated MOS devices with those of HfO_2-based gate oxides both with similar EOT, very important differences were found. It was observed that during ***SILC degradation***, less degradation in gate leakage current after stress is found for La_2O_3-gated MOSCAP at the same EOT. Other Hf-based oxides with similar EOT to our La_2O_3-gated MOS samples, still observe the same exponential increase in SILC degradation during the stressing measurements. Similarly, even though La_2O_3 presents an initially higher ***density of interface-states Dit***, the

generation of additional Dit is lower compared to HfO_2, in which an exponential generation of Dit is observed. The ***shift in Vth*** after stress for HfO_2 resulted in the same exponential behavior thus suggesting that during the stressing of HfO_2-based gate oxides, the generation and accumulation of defects at the bulk and interfaces of Hf-based oxides follows is of an exponential nature. With La_2O_3, additional Vth shift after electron injection is minimized. By comparing ***TDDB lifetime*** extrapolation data, a 10 years operation before breakdown for both high-k materials is guaranteed even at relatively high Vg > 1 V. Regarding to the ***breakdown models*** for these oxides, it was found that during substrate injection, a Hf-based system experiences high-k bulk breakdown whereas La_2O_3 shows interfacial-layer (IL) breakdown followed by the breakdown of La_2O_3 itself. During the gate injection condition, a Hf-based system mostly experiences IL breakdown whereas La_2O_3 shows complete IL + high-k breakdown simultaneously.

All the former results suggest that La_2O_3-gated MOS devices have an advantage over HfO_2 since better reliability results have been demonstrated for La_2O_3 -gated devices at very similar EOT levels. By using very thin high-k films with EOT < 1nm we have identified a large SILC increase for La_2O_3-gated devices so that it is thought that the degradation-related reliability of very thin La_2O_3 gate oxides becomes compromised but their final lifetime before breakdown would remain within the specifications.

In general, the La_2O_3 dielectrics show higher reliability than that of HfO_2-based dielectrics, although some of the reliability evaluations have not been carried out for the La_2O_3. The published data in the journal and the conference predict not sufficient reliability for the Hf-based oxide to be used in commercial products. However, Intel announced Hf-based high-k gate oxide introduction into the 45 nm CMOS with sufficiently high reliability which meets the commercial production thus the reliability of the Hf-based oxides with EOT down to sub 1 nm seems to have been already established.

At this moment, any fundamental problems for the reliability of La_2O_3 dielectrics have not been found by this study. Thus, it is expected that the La_2O_3 reliability will meet the requirements for the production by the time when it is introduced into commercial devices.

7.2 Recommendations for future works

In order to successfully integrate La_2O_3 into forthcoming generations of CMOS technologies, the improvement in the reliability characteristics of La_2O_3-gated MOS devices must be obtained as well as a deeper characterization and modeling of the charge trapping phenomena when several other degradation factors are taken into account. In this respect, there are some research topics regarding the reliability characterization of Metal/high-k stacked structures that need to be addressed as follows.

To establish a method to predict lifetime and degradation of La_2O_3 under as low operating stress conditions as possible. Besides, for ultra thin oxides and low stressing biases, SILC and SBD mechanisms will play a fundamental role in the degradation of the devices, so that the adequate extraction of degradation parameters with these ultra thin gate oxides under low stress conditions should therefore be investigated. Also, the failure modes might change with scaling. Therefore, how the different breakdown modes affect scaled down Metal-La_2O_3 MOSFET devices is also a research topic that must be investigated.

Some degradation modes such as NBTI or PBTI are strongly temperature dependent. Therefore, more detailed studies regarding the degradation of La_2O_3 under elevated temperatures must be done. In this study, only room temperature reliability measurements were done. Also, it is necessary to investigate the effects of dynamical electrical stress (and several other additional degradation factors) for the analysis of the degradation and breakdown of thin Metal-La_2O_3 stacked structures.

More reliability evaluation for La_2O_3-gated samples with EOT < 1 nm devices, and clarification of problems at this regime. At this moment, only SILC was found to be the problem. Also, reliability tests for smaller capacitors since the smallest capacitors' size we used was limited to a 100 μm diameter. Moreover, since the hot-carrier injection (HCI) instability can only be measured by using very short-channel MOSFET structures, HCI measurements for very small gate length (Lg < 50 nm) MOSFETs must be performed.

Finally, more studies for the optimization of processing conditions for enhanced reliability must be done. At this moment, it was found that higher annealing temperatures, in-situ gate metallization and La_2O_3 deposition in oxygen ambient improved the reliability. Also it was found that the reliability characteristics of devices using tungsten as a gate electrode are better than that of Al.

List of publications and presentations

Publications

1. J. Molina, K. Kakushima,, P. Ahmet, N. Sugii, K. Tsutsui, and H. Iwai, "**Breakdown and Reliability of Metal Gate–La_2O_3 Thin Films After Post-Deposition Annealing in N_2**", *ECS Transactions*, vol. 1, no. 5, pp. 757-765 (2005).

2. J. Molina, K. Tachi, K. Kakushima,, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, "**Charge Trapping Characteristics of W–La_2O_3–nSi MIS Capacitors After Post-Metallization Annealing PMA in N_2**", *ECS Transactions*, vol. 3, no. 3, pp. 233-244 (2006).

3. J. Molina, K. Tachi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, "**Effects of N_2-Based Annealing on the Reliability Characteristics of Tungsten/La_2O_3/Silicon Capacitors**", *J. Electrochem. Soc.*, vol. 154, no. 5, pp. G110–G116 (2007).

4. J. Molina, K. Kakushima, P. Ahmet, N. Sugii, K. Tsutsui, Takeo Hattori and H. Iwai, "**Carrier Separation and Vth Measurements of W-La_2O_3 Gated MOSFET Structures After Electrical Stress**", *IEICE Electronics Express*, vol. 4, no. 6, pp. 185-191 (2007).

5. E. Miranda, J. Molina, Y. Kim and H. Iwai, "**Degradation of High–k La_2O_3 Gate Dielectrics Using Progressive Electrical Stress**", Microelectronics Reliability, 45, 1365-1369 (2005).

6. E. Miranda, J. Molina, Y. Kim and H. Iwai, "**Tunneling in sub-5nm La_2O_3 Deposited by E-beam Evaporation**", Journal of Non-Crystalline Solids, vol. 352, pp. 92-97 (2006).

International presentations

1. J. Molina, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori and H. Iwai, "**Electrical Breakdown and Reliability of Metal Gate–La_2O_3 Thin Films after Post Deposition Annealing in N_2**", 208th Meeting of the Electrochemical Society, 16–21 Oct. (2005). Los Angeles, CA, USA.

2. J. Molina, K. Tachi, K. Kakushima,, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, "**Charge Trapping Characteristics of W–La_2O_3–nSi MIS Capacitors After Post-Metallization Annealing PMA in N_2**", 210th Meeting of the Electrochemical Society, Oct. 29 – Nov. 3 (2006), Cancun, Mexico.

3. B. Sen, H. Wong, J. Molina, C.K. Sarkar, J. Ng and H. Iwai, "**Effects of Ambient Temperature on the Electrical Characteristics of Thin La_2O_3 Film Grown by E-Beam Evaporation**", Electron Devices and Solid-State Circuits, 2005 IEEE Conference on, 173–176, 19-21 December (2005).

4. K. Kakushima, P. Ahmet, J. Ng, J. Molina, H. Sauddin, Y. Kuroki, K. Nakagawa, A. Fukuyama, K. Tachi, Y. Shiino, J. Song, K. Tsutsui, N. Sugii, T. Hattori and H. Iwai "**Study of La_2O_3 Gate Dielectric Suitability for Future MIM and MOSFETs**" 2006 IEEE Si Nanoelectronics Workshop, June 12, Honolulu Hawaii (2006).

Domestic presentations

1. J. Molina, A. Kuriyama, K. Tsutsui and H. Iwai, “希土類酸化物薄膜におけるポストメタルアニールに関する検討”、第 65 回応用物理学会学術講演会、仙台市、p.685 (2004 年 9 月) 。In Japanese.

2. J. Molina, N. Sugii and H. Iwai, “**Electrical Breakdown and Reliability of Metal Gate-La_2O_3 Thin Film Structures**”, 21 世紀COEプログラム「フォトニックスナノデバイス集積工学」シンポジウム、虎ノ門パストラル、P-39、(2005 年 12 月)。In Japanese.

3. J. Molina, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori and H. Iwai, “**Reliability Characteristics of W−La_2O_3 Thin Film Structures on Silicon**”, 21 世紀COEプログラム「フォトニックスナノデバイス集積工学」最終結果報告シンポジウム、虎ノ門パストラル、P-61、(2006 年 12 月)。In Japanese.

Acknowledgements

It is a pleasure to thank the many people who made this thesis possible.

First and foremost, I would like to express my deep and sincere gratitude to Professor Hiroshi Iwai, who not only offered me the opportunity to do research at his lab but also guided me throughout several stages of my academic and personal life. For his patient help and kind assistance during my stay in Japan I am truly grateful.

It is difficult to overstate my gratitude to my associate supervisor, Professor Sugii Nobuyuki of Hitachi's Central Research Laboratory, who is currently the visiting professor at Department of Electronics and Applied Physics of Tokyo Institute of Technology. I am deeply thankful for his guidance, advices and kind recommendations received throughout the development of my research. I would have been lost without him.

I would like to thank the many people who always helped me with the direction of my research: Associate Professor Kazuo Tsutsui for their comments and advices, particularly on fundamentals as well as technical scopes of my experiments. Professor Takeo Hattori for sharing his experience and advices just when I needed the most. I will never forget Assistance Professors Kuniyuki Kakushima and Parhat Ahmet, they both were the source for continuous encouragement and enlightenment when I was in total darkness. Thanks to their technical help, I could rapidly get the devices I needed and my

usually long-lasting measurements started to run more smoothly because of them. I think they have far exceeded his professional obligations in helping me. Also, I am deeply grateful for have shared the stimulating environment and for have taking advantage from the experience of the many visitor professors to Iwai Lab. I am especially grateful to Professor Enrique Miranda for his genuine encouragement to focus my research on the reliability properties of lanthanum oxide. Thank you. Professors Henryk M. Przewlocki, Hei Wong and Sarkar have all my sincere gratitude for sharing their experience with me during their short-term stay in Iwai Laboratory.

My special thanks to all the past and present secretaries of Iwai Laboratory for their helps, motivations, understandings and patience. During my stay at Tokyo Institute of Technology, they assisted me in so many ways that without them, I could not have move around all the academic paperwork. I am also indebted to the many past and present students of Iwai laboratory for providing a stimulating and fun environment in which to learn and grow. I am especially grateful to Atsushi Kuriyama, Ng Jin Aun, Henderianshah Sauddin, Koji Nagahiro and all actual members of Iwai Lab for their understanding, help, patience and for sharing those sunny days of futsal.

I would like to thank the Ministry of Education, Culture, Sport, Science and Technology, Government of Japan for economically supporting me through the Monbukagakusho scholarship during the past four years.

I wish to thank all my friends from Japan. They were always there to give me support, friendship and company when I needed it the most. During those first days I

will never forget the kindly help of my friends at the university dormitories. My friends are so many that I am afraid to forget somebody, but they know I carry their friendships in the bottom of my heart. Thanks a lot to all of you for being there.

I want to thank the love and support my girlfriend gave me during all those days of solitude and desperation I had. She just not taught me the many beautiful sightseeing spots within Japan but reassured within me the very important Japanese values of honesty, human emotion, endurance, compassion and very importantly, 和 the notion of individual and group harmony. I will always love you.

All my friends in Mexico deserve mention since they also showed me that life is worthless without friendship. Special thanks to my friends from INAOE, first of all, thanks to the professors for first introducing me to the study of semiconductor devices and for the many highly-academic discussions within INAOE and within Tonita's place. Thanks also to my student friends from all departments, to all my friends, receive my most sincere gratitude.

Last but not least, I would like to thank my family, all my love for them. My parents, Adelina Reyes Ochoa and Joel Molina Sebastian receive my special gratitude. They gave me birth, raised me, supported me, taught me, and most importantly, I know they love me no matter what or where they are. To my brothers and sisters, Juana Nancy and her husband Javier Hernandez, Eduardo, Viridiana and her husband Carlos Rodriguez, to their children and families, to all of them I dedicate this thesis.

Thanks God for always being near me when I need you.

秋に一葉の初めて枯れ落ちる姿も鋭い詩人の心には詩になるのである。