Doctorial Thesis

Analysis of Electrical Conduction in Rare Earth Gate Dielectrics

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To my mother and father

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Chapter 1. Introduction

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1.1 Scaling of MOSFET: Motivation for alternative dielectrics

Since the invention of MOSFET (Metal Oxide Field Effect Transistor) [1,2], the scaling down of the device is inevitable for the reason of high performance, device reliability, and cost-down of MOSFET. In 1965, G. Moore observed an exponential growth in the number of transistors per integrated circuit and predicted that this trend would continue [3]. The press called it "Moore's law". The law states that density is double every 18 months. In other words, density is quadrupled every 3 years. This relationship can be expressed by the equation:

$$\log_{10}\left(\frac{y}{y_0}\right) = \frac{(x - x_0)}{3}\log_{10}(4) \qquad \text{Eq. 1.1}$$

Here, y and y_0 correspond to the device density at a certain year x and the base year x_0. Fig. 1.1 shows the scaling down of bits in DRAM [4] and transistors in CPU [5]. The solid line called Moore line corresponds to Eq. 1.1. It can be seen that the Moore line fits well the number of bits or transistors at each year.

As the MOSFET is scaled down, the gate length and the gate oxide should be scaled down to keep the equal electric field, as shown in Fig. 1.2 [6]. It is well known that the invention and the continuous scaling-down of MOSFET are attributed at the superiority of the silicon dioxide as a gate dielectric, compared to other dielectrics. However, state-of-the-art technology focuses on the alternative dielectric with high dielectric constant k compared to silicon dioxide. This is because the gate oxide approaches the direct tunneling regime. It has been reported that the direct tunneling

occurs when the oxide is as thin as 3 nm [7]. If the direct tunneling current is appreciable to the channel current, transistor is unworkable.

The channel current, i.e., drain-to-source current I_{ds} can be expressed as a function of the inversion charge density Q_i with the gradual channel approximation (GCA) [8]:

$$I_{ds} = \mu_{eff} \frac{W}{L} \int_0^{V_{ds}} -Q_i(V)dV \qquad \text{Eq. 1.2}$$

Here, μ_{eff} is the carrier mobility. W and L are width and length of the gate. V_{ds} is drain-to-source voltage. Q_i can be expressed by the following with the charge-sheet approximation:

$$Q_i = -C_{ox}\left(V_g - V_{fb} - 2\psi_B - V\right) - Q_d \qquad \text{Eq. 1.3}$$

where C_{ox} is the gate oxide capacitance, V_g the gate voltage, V_{fb} flat band voltage, ψ_B the bulk potential, Q_d the bulk depletion charge density. Q_i is proportional to C_{ox} and so does I_{ds}. On the other hand, the direct tunneling current is principally determined by the gate oxide thickness T_{ox}. It can be seen by the approximated form of the direct tunneling current I_{DT}:

$$I_{DT} \sim \exp\left(-\frac{1}{|E_{ox}|}\right) \qquad \text{Eq. 1.4}$$

Here, E_{ox} is the electric field across the oxide. Thus, by increasing the dielectric constant and by decreasing the film thickness of the gate oxide, it is possible to maintain the drain-to-source current of the MOSFET and direct tunneling current of gate oxide of the MOSFET.

The requirement for high-k dielectric as a gate oxide can be easily understood in the following manner. Substituting Eq. 1.3 into Eq. 1.2 and Taylor series expansion

for large V_{ds}, one can get the saturation current expression in the linear region

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} \left[(V_g - V_t) V_{ds} - \frac{m}{2} V_{ds}^2 \right] \quad \text{Eq. 1.5}$$

where

$$m = 1 + \frac{C_{dm}}{C_{ox}} \quad \text{Eq. 1.6}$$

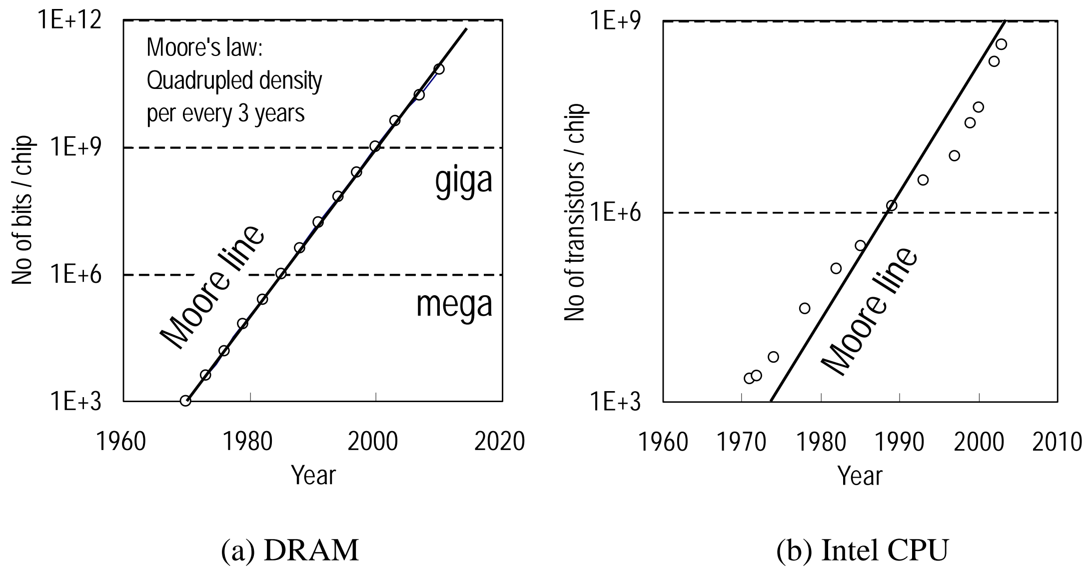
Here m typically lies between 1.1 and 1.4 and is related to body effect [8]. Since the tunneling current of gate oxide is important in the linear region, rather than in the saturation region, dividing I_{DT} by I_{ds}, one can obtain the simple current ratio describing gate tunneling current portion with respect to the drain current of the MOSFET:

$$\frac{I_{DT}}{I_{ds}} \sim \frac{\exp(-1/|E_{ox}|)}{C_{ox}} = \frac{1-1/|E_{ox}|}{\varepsilon_{ox} V_{ox}} \sim \frac{T_{ox}}{\varepsilon_{ox}} \quad \text{Eq. 1.7}$$

This equation simply tells that higher dielectric constant of the gate oxide leads to the small portion of the tunneling current, at the same gate oxide thickness. This concept is also introduced elsewhere [9]. When the gate oxide is leaky, more precise derivation results in that $I_{ds}=I_{ds0}+I_g/2$ [10], where I_{ds0} is the drain current without gate leakage current. However, the prediction from Eq. 1.7 does not change. This point is illustrated in Fig. 1.3. Like in the same fashion of MOSFET, the capacitor for memory bit cell and analog circuit requires thicker dielectric keeping the same charges at the both ends of the capacitor. Thus, high-k dielectric application is not only for the logic transistor but also memory or analog capacitor.

The scaling of lateral device dimensions of silicon field effect transistors to less than 50 nm requires replacement of thermally grown SiO_2 by deposited dielectrics

which have higher dielectric constants than SiO_2. The principal motivation for this replacement is to reduce tunneling currents at the same equivalent oxide thickness by increasing the physical thickness of the film with higher dielectric constant. According to ITRS2003 [6], SiO_2 or SiON is widely used as the gate oxide of MOSFET in the industry these days. For the next generation, a considerable number of studies have been conducted on Hf or Zr based oxide. However, Hf or Zr based oxide does not seem to meet the requirement of the whole generation of the gate oxide. For this reason, for the next generation of Hf or Zr based oxide, another alternative dielectrics, for instance, rate earth metal oxides (REOs) are being focused.



(a) DRAM (b) Intel CPU

Fig. 1.1. Scaling down of (a) the number of bit in DRAM [4] and (b) the number of transistors in CPU [5].

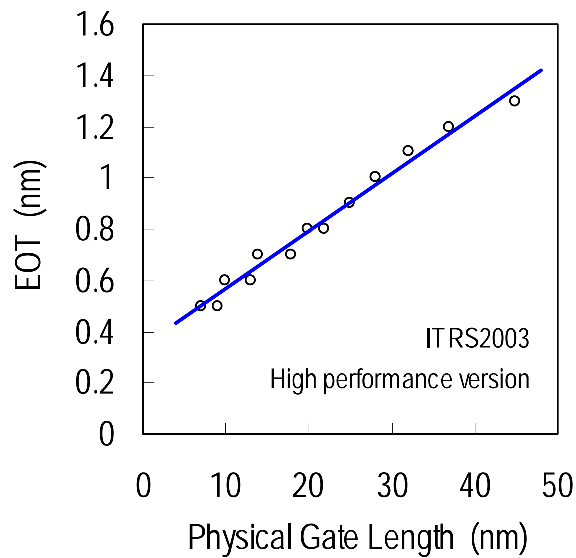
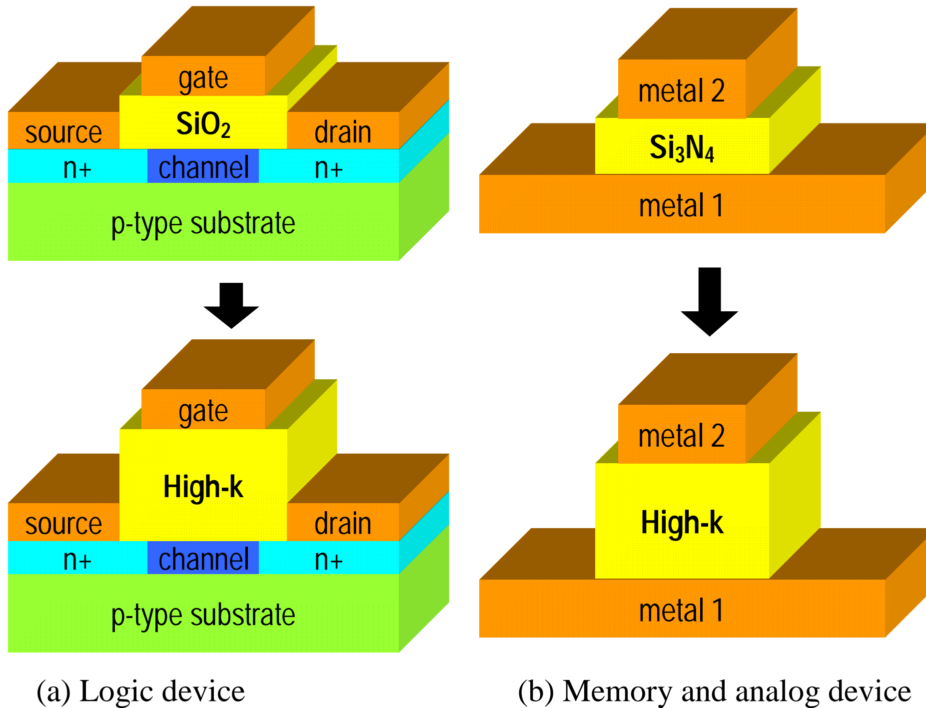


Fig. 1.2. EOT (Equivalent Oxide Thickness) versus physical gate length of MOSFET [6].



(a) Logic device (b) Memory and analog device

Fig. 1.3. Illustration of high-k gate dielectric keeping the same charge density at both ends of the dielectric, for (a) logic transistor and (b) memory bit cell or analog circuit.

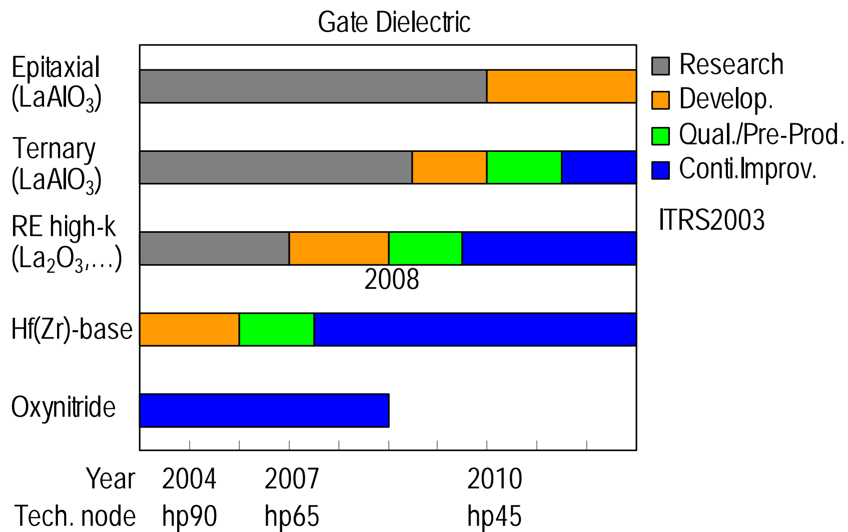
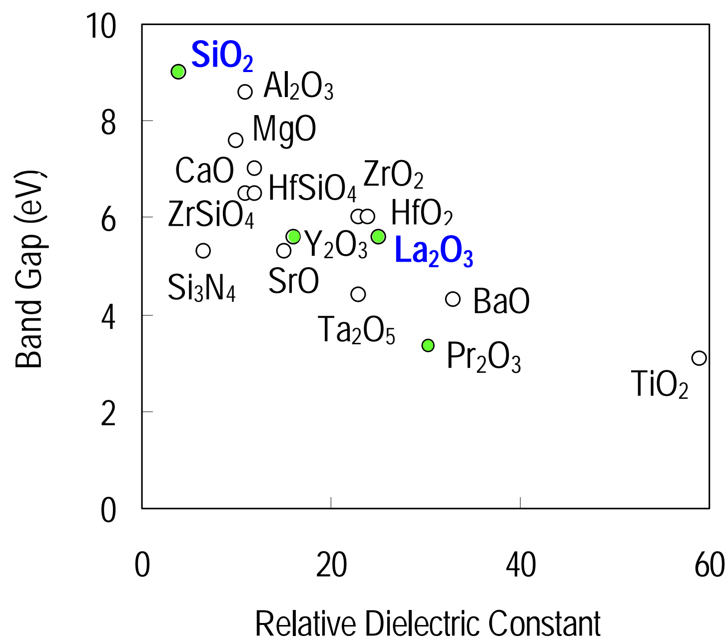


Fig. 1.4. Roadmap of gate dielectric for high performance version of MOSFET according to ITRS2003 [6].

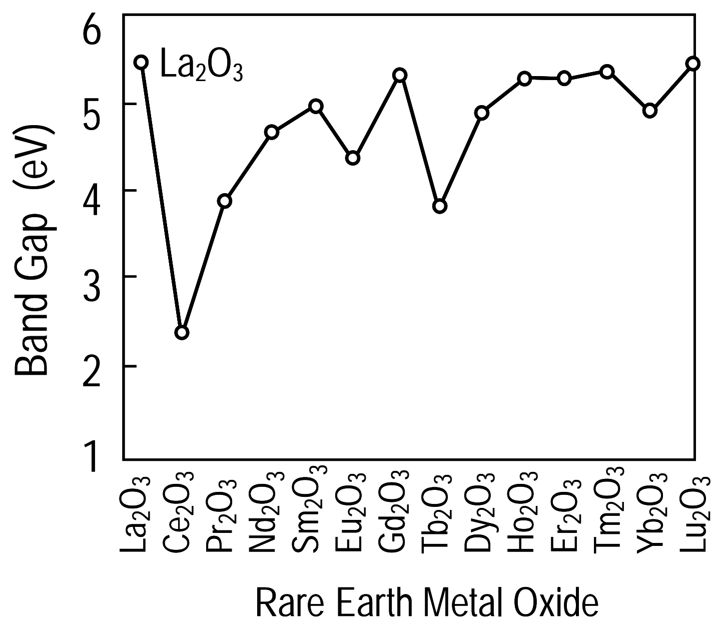
1.2 Review of Rare Earth Metal Oxides

A new gate dielectric can be selected in terms of band gap and relative dielectric constant. The product of the two can be a figure of merit to compare the dielectrics. Band gap of several candidate oxides for gate dielectric is shown in Fig. 1.5, as a function of the relative dielectric constant [11,12,13,14]. One can find the most promising dielectric in terms of the figure of merit given by the product of the band gap and the relative dielectric constant. They are Al_2O_3, ZrO_2, HfO_2, La_2O_3, BaO, and TiO_2. Compared to other REOs, Lanthana (La_2O_3) is electrically hopeful for the gate oxide of the MOSFET. In fact, band offset to silicon is relatively high as shown in Fig. 1.6 [11,15,16]. To suppress the interfacial layer growth, nitridation of the silicon surface before/after the deposition of high-k dielectric is often used, but the valence band offset is reduced by less than 1 eV [16].

In addition, it has been reported that Lanthana film has an extremely low gate leakage current [16], even better than the Al_2O_3 and HfO_2 films have, as depicted in Fig. 1.7 [17].



(a)



(b)

Fig. 1.5. Dielectric constant vs. band gap for (a) candidate gate oxides [11,12] and (b) rare earth metal oxides [13,14].

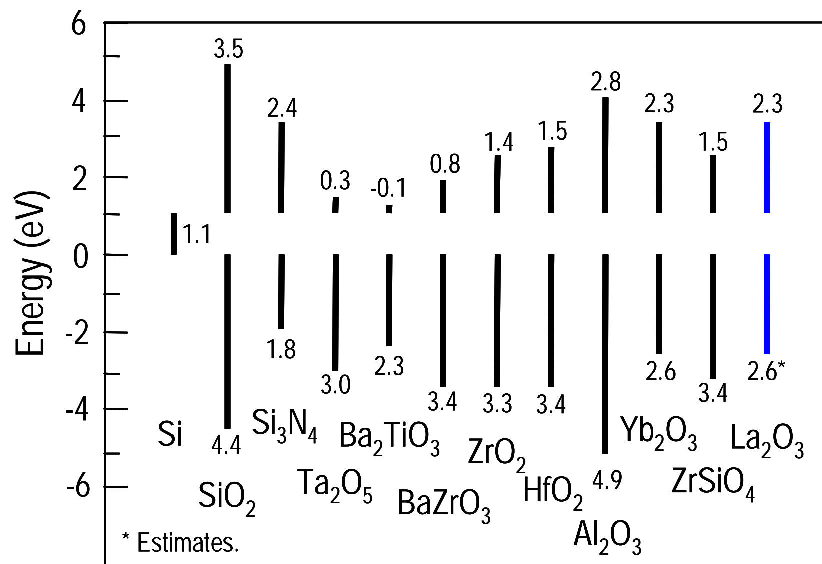


Fig. 1.6. Band offsets for high-k dielectrics on silicon [11,15,16].

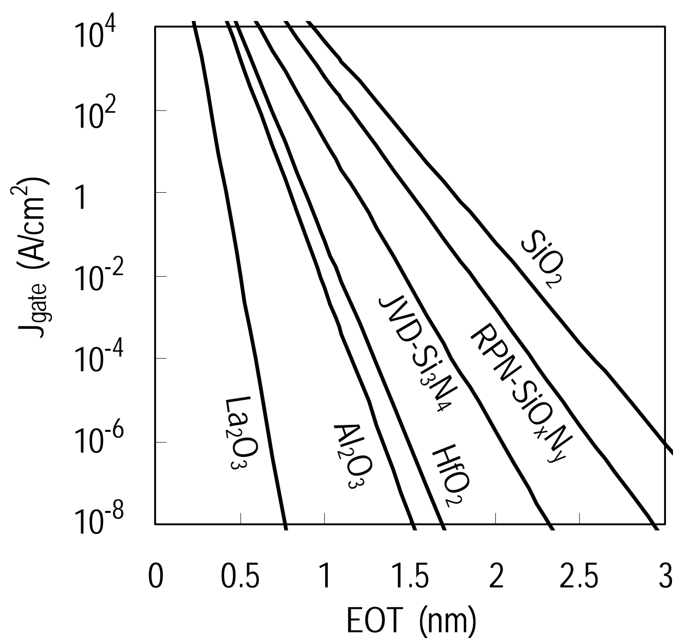


Fig. 1.7. Gate current density at a fixed inversion gate bias (1V) as a function of the equivalent oxide thickness for five different gate dielectrics. Solid lines are from the model [17].

1.2.1 Atomic defects

Atomic disorder in metal oxides can be classified in terms of stoichiometry [18]. In case of stoichiometric oxides, there are Schottky and Frenkel disorder, whereas, in case of nonstoichiometric oxides, there are oxygen-deficient and metal-deficient. Schottky disorder has involves the simultaneous of both cation and anion vacancies while Frenkel disorder has equal concentrations of vacant lattice sites and interstitial atoms.[19,20] In addition, when there are impurities in the dielectrics, two types of structural imperfections are believed to occur in the dielectrics: substitutional solid solution and interstitial solid solution [20].

Defects can be generated in a solid by (1) thermodynamic equilibrium (Schottky, Frenkel), (2) chemical substitution, (3) oxidation or reduction, and (4) energetic radiation [19]. Table 1.1 lists Korger-Vink nomenclature for the different types of ionic defects [19].

Table 1.1. Kroger-Vink nomenclature for ionic-type defects [19]

Symbol	Definition
M_M	Cation on regular lattice site
X_X	Anion on regular lattice site
V_M	Cation vacancy
V''_M	Effective charge on cation vacancy
M_i	Cation on interstitial site
$M^{\cdot\cdot}_i$	Effective charge on interstitial cation
X_i	Anion on interstitial site
X''_i	Effective charge on interstitial anion
V_X	Anion vacany
$V^{\cdot\cdot}_X$	Effective charge on anion vacany

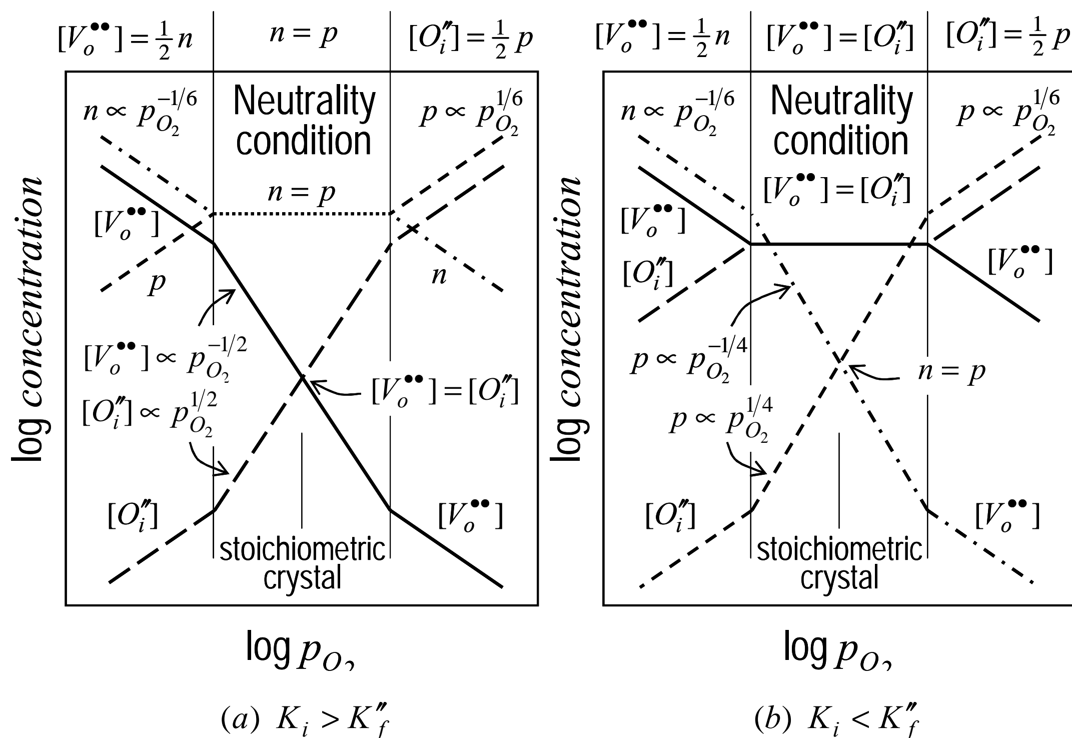


Fig. 1.8. Schematic representation (Brouwer diagrams) of concentration of oxygen point defects and electronics defects as a function of oxygen pressure in an oxide. In $(a)\ K_i > K''_f$; in $(b)\ K_i < K''_f$ [20].

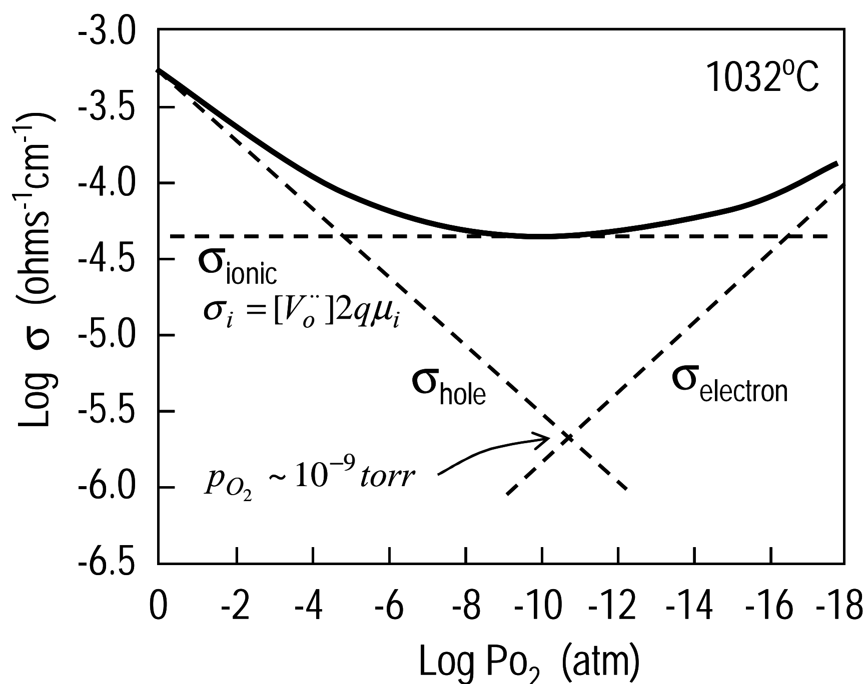


Fig. 1.9. Total and partial conductivities of La_2O_3 at 1032°C [22].

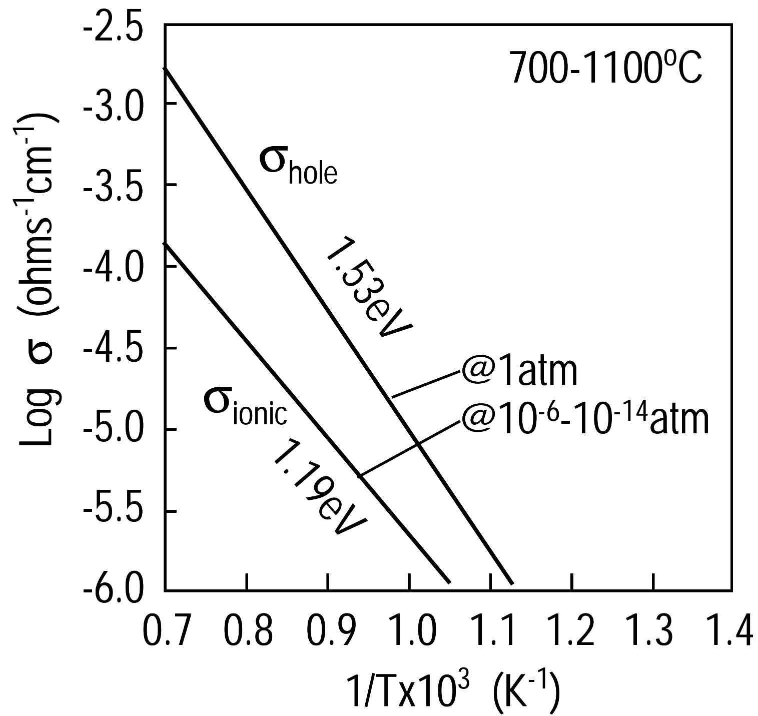


Fig. 1.10. DC conductivities of hole and ion as a function of inverse temperature [22].

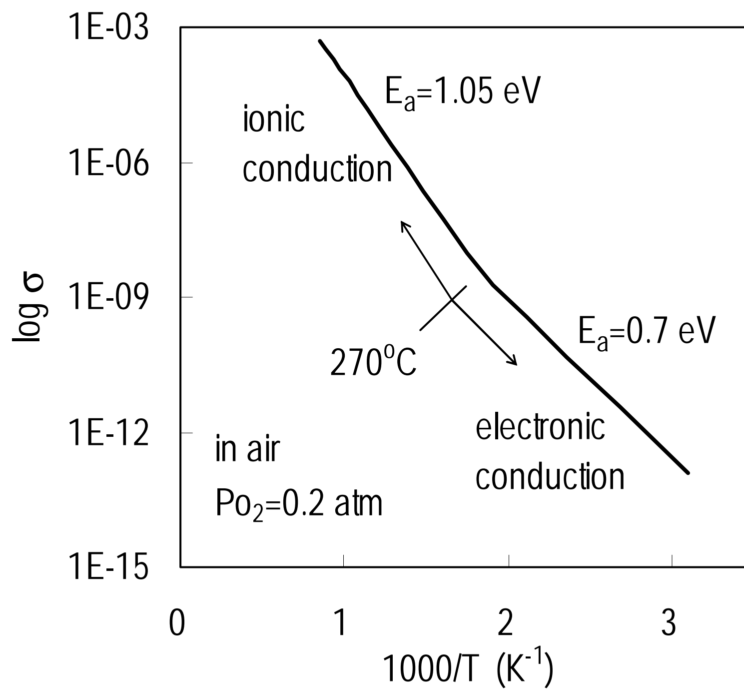


Fig. 1.11. Electrical conductivity ($\Omega^{-1}cm^{-1}$) against the reciprocal of absolute temperature [23].

Among the four types, Lanthana film is reported to have an anion Frenkel disorder [21], provided Lanthana film is stoichiometry. Due to the anion Frenkel disorder, Ionized oxygen ions O^{2-} and holes are easy to exist in nature as reported in Ilett et al. [21]. This oxygen Frenkel disorder is similar to Y_2O_3 which is one of the REOs [20].

With the defect chemistry and the assumptions of oxygen Frenkel defects, variation of the oxygen content over a range of stoichiometry, and appreciable electron-hole concentration, defect equations by Kroger-Vink notation can be given by [20]:

$$O_o = O_i'' + V_o^{\bullet\bullet} \qquad [O_i''][V_o^{\bullet\bullet}] = K_F''$$

$$O_o = \frac{1}{2}O_2(g) + V_o^{\bullet\bullet} + 2e' \qquad [V_o^{\bullet\bullet}][e']^2 P_{O_2}^{1/2} = K_1$$

$$null = e' + h^{\bullet} \qquad [e'][h^{\bullet}] = K_i$$

$$\frac{1}{2}O_2(g) = O_i'' + 2h^{\bullet} \qquad \frac{[O''][h^{\bullet}]^2}{P_{O_2}^{1/2}} = K_2$$

$$K_1 K_2 = K_i^2 K_F'' \qquad \text{Eq. 1.8}$$

Neutrality equation is

$$2[O_i''] + [e'] = 2[V_o^{\bullet\bullet}] + [h^{\bullet}] \qquad \text{Eq. 1.9}$$

At a sufficiently high oxygen pressure, the neutrality condition can be approximated by

$$[V_o''] = p/2 \qquad \text{Eq. 1.10}$$

On the other hand, at a sufficiently low oxygen pressure, the neutrality condition can be approximated by

$$[V_o^{\bullet\bullet}] = n/2 \qquad \text{Eq. 1.11}$$

When the concentration of Frenkel defects is substantially greater than the concentration of intrinsic electronic defects, that is, $\Delta g''_F < E_g$, or $[V^{\cdot\cdot}_o]=[O''_i]$, Brouwer diagram illustrating above defect equations of oxygen Frenkel disorder is show in Fig. 1.8, from which it is seen that electron is dominant in low oxygen partial pressure and hole is dominant in high oxygen partial pressure. Electron and hole conductions with oxygen partial pressure can be also seen in Fig. 1.9 [22]. Activation energy of hole conduction is compared to that of ionic conduction, in Fig. 1.10. Activation energy of electronic conduction is compared with that of ionic conduction, in Fig. 1.11 [23]. One can see the change in activation energy at 270°C, which indicates the possibility that electron conduction can govern the leakage current, at temperatures less than 270°C and in the low oxygen partial pressure. Additionally, most of the sesquioxidies in REOs are reported to show the similar change in activation energy at round 550-600°C, although La_2O_3, Pr_2O_3, and Tb_2O_3 show it at lower temperatures, around 300°C [23].

Oxide films that have Frenkel defects have sufficient oxygen atoms to oxidize other materials contacted to the films. This is not the case for films with oxygen Schottky defects. In fact, due to the low activation energy for O^{2-} vacancy migration, Lanthana is also used as a catalyst for oxidation in the chemistry [21,24,25]. Oxygen diffusion constant D0 in Lanthana is found to be 9.83×10^{-15} cm^2/s [24]. It has been also reported that oxygen diffusion plays an role in oxidation of silicon substrate [26].

In addition to the oxygen Frenkel disorder of Lanthana film, oxygen deficient disorder has been reported in several articles [27,28,29,30,31,32]. Such oxygen deficiencies can behave as donor centers for bulk-limited conduction processes, such P-F and SCLC.

To put it briefly, Lanthana film may have oxygen defects represented by anion Frenkel order and anion deficient order, which can lead to the oxidation of other

materials in touch with Lanthana, like a catalyst.

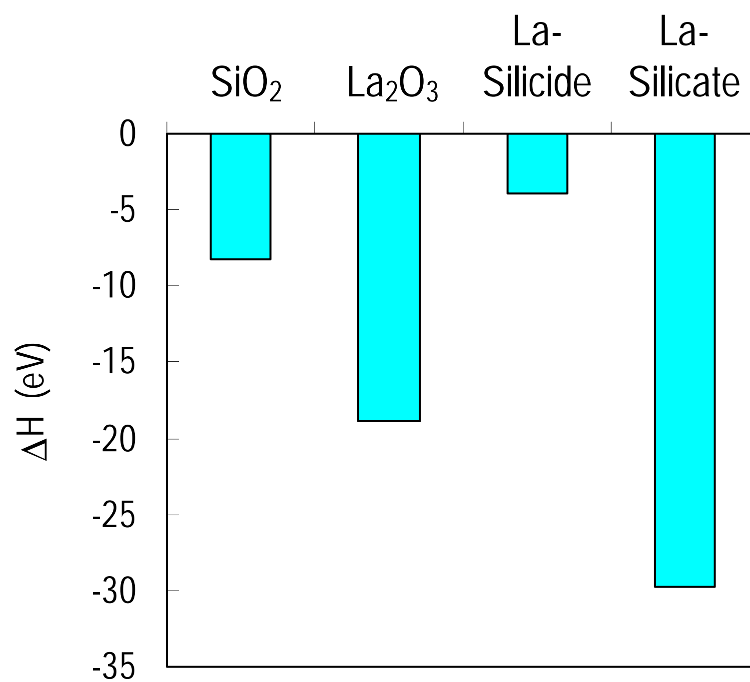


Fig. 1.12. Formation enthalpies of La system, with amorphous SiO_2 for comparison. A material with lower ΔH is more stable: La-silicate is stable against decomposition into La, La_2O_3, and SiO_2.

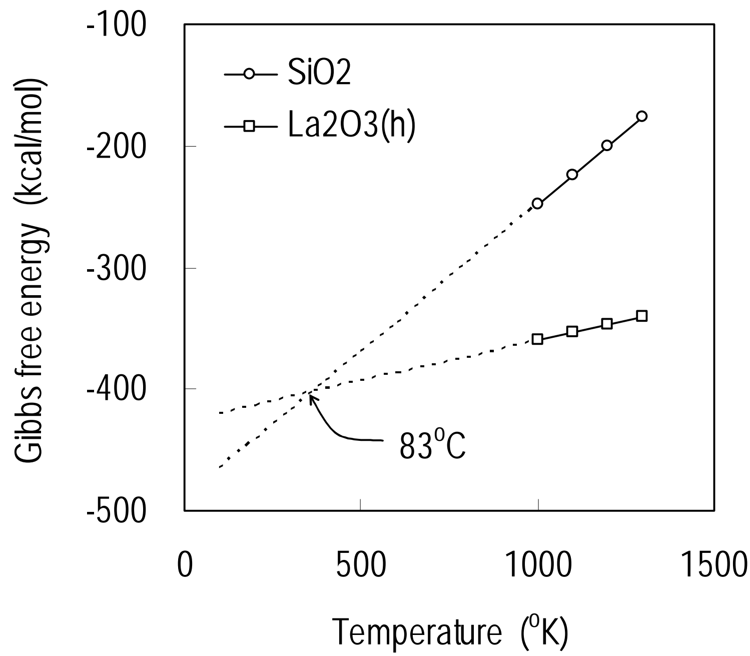


Fig. 1.13. Gibbs free energy of SiO_2 and La_2O_3 (hexagonal). Larger negative Gibbs free energy implies higher affinity with oxygen.

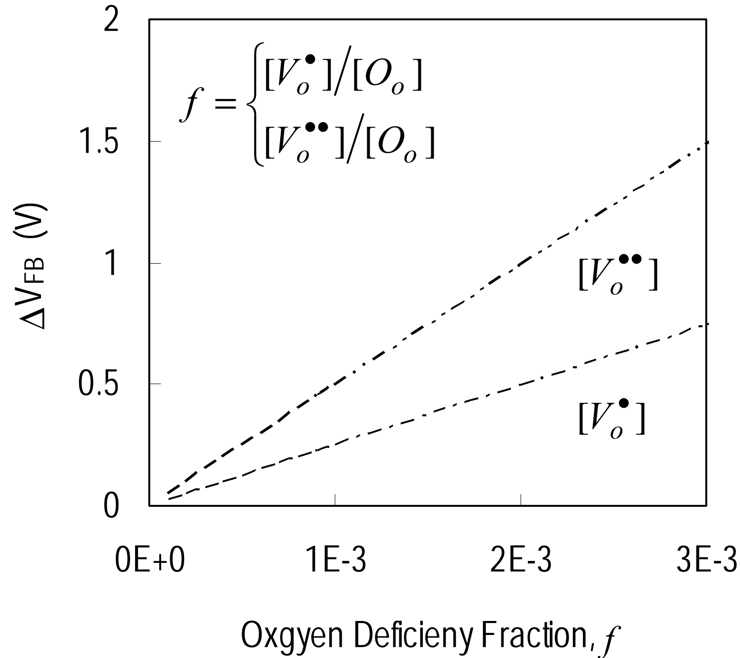


Fig. 1.14 Flat-band voltage shift ΔV_{FB} as a function of the ratio of deficient oxygen concentration to stoichiometric oxygen concentration in La_2O_3. Parameters assumed are film thickness 5 nm, relative dielectric constant 20, and c-type volume 9.16e-23 cm^3.

1.2.2 Interfacial layer (IL)

IL at the interface between high-k gate dielectrics and silicon substrate is introduced intentionally or in an unwanted way. In terms of material phase, the IL exists in two ways: immiscibility and solid-solution. The former means phase-separation of high-k material from SiO_2 and the latter means blended one.
It has been reported that the minimum thickness of SiO_2 maintaining band offsets is found to be 7 A [33,34]. Since the silicate layer barrier height would be lower than the SiO_2 layer, it can be expected that SiO_2 layer less than 7 A looses its effectiveness for reducing the tunneling current, in other words, becomes transparent. In fact, IL can play an important role on the conduction mechanism when the IL is thick, i.e., 1.7 nm [35] On the contrary, if thin, it can be transparent for tunneling [36]. What is more, gate dielectric reliability can be principally determined by thick IL, in Ta_2O_5/SiO_2 gate dielectric stack [37].

Frequently surface treatment of the silicon substrate with H_2O_2 is used to create thin SiO_2 layer called chemical oxide [38,39,40,41]. Regarding the role of chemical oxide ILs, it is reported that the chemical oxide layer can depress the gate leakage current, maintaining the same capacitance [42], and can also be an oxygen source for the growth of metal oxide in the initial several monolayers during deposition [43].

In the case of Lanthana film, IL is found to be silicate without a phase separation of La_2O_3 and SiO_2 [28,44,45,46,47,48]. This is clearly different from the phase separation of Y_2O_3 among the REOs [28,49,50].

High-k gate dielectric with IL can be regarded as stacked layers and the oxide field of two-layers, A and B, is described as following:

$$V_{applied} = t_A E_B + t_A E_B$$ Eq. 1.12 [51]

$$E_A = \frac{V_{applied}}{(\varepsilon_A / \varepsilon_B) t_B + d_A} \quad and \quad E_2 = \frac{V_{applied}}{(\varepsilon_B / \varepsilon_A) t_A + d_B}$$ Eq. 1.13 [52]

Here, t_A and t_B correspond film thicknesses of layer A and B, respectively.

The above equation assumes that no charge is accumulated at the A/B interface. In addition, the effective dielectric constant of the two-layers is expressed as following [53]:

$$\varepsilon_{eff} = \frac{(t_A + t_B)\varepsilon_A \varepsilon_B}{t_A \varepsilon_B + t_B \varepsilon_A}$$ Eq. 1.14

The dielectric constant of the silicate layer can be described by the general empirical relationship called the logarithmic mixture-rule [54,55]. This rule gives a value intermediate between the two extremes: one is when layers are parallel to the capacitor plates and the other is when layers are arranged normal to the capacitor plates. The logarithmic mixture-rule is expressed as following:

$$\log(\varepsilon) = \sum_i v_i \log(\varepsilon_i)$$ Eq. 1.15

Here, v_i is the volume fraction of each phase, equal to the relative plate thickness, and ε_i is the dielectric constant of each phase. For two elements, the above equation can be simplified as following:

$$\varepsilon = 10^{v_{ox} \log(\varepsilon_{ox}) + v_{IL} \log(\varepsilon_{IL})}$$ Eq. 1.16

The dielectric constant of IL could be greater than 3.9 of pure silicon dioxide and less than 27 of Lanthana film. If we simply assume the composition of IL as an equal

volume fraction of Lanthana and SiO_2 and the dielectric constant of the pure Lanthana film as 28, the dielectric constant of the IL is 10.5 from the logarithmic mixture rule. Since the maximum thickness of IL is 0.25 um from TEM micrograph and the film thickness is 7.7 nm from the ellipsometry, the effective dielectric constant of the two layers is 26.6. Although this is a rough approximation, it should be noted that the IL can be insignificant. Additionally, a more accurate calculation will give a higher dielectric constant of Lanthana film itself than 27. In fact, dielectric constant of La-silicate is reported as around 17 [26,56].

1.2.3 Crystallization

In general, crystallization of the gate dielectric film is avoided since large grain boundary can provide trap sites for charge trapping, fixed charges, and local path for conduction. Moreover, it is extremely difficult to achieve the uniform crystal film on the large silicon surface, on condition of following thermal processes after gate dielectric formation. In fact, many studies have been made on the leakage current comparison with amorphous and crystal films of Ta_2O_5 [57,58,59], Gd_2O_3 [60], and Y_2O_3 [60]. On the other hand, as regard to dielectric constant, it is not clear which is better. For example, dielectric constant, 20, of amorphous $(Ba,Sr)TiO_3$ is increased to 60-200 of crystalline one [61], whereas 21.1 of amorphous ZrO_2 is decreased to 15.5 due to crystallization [62].

There seems to be no consensus on crystallization temperature of Lanthana film, but some articles have reported that crystallization is not observed at annealing temperature 900°C [31] but observed at much lower temperature about 400°C [45].

Since the former film is prepared by MOCVD (Metal Organic Chemical Vapor Deposition) and the latter film is done by evaporation, the crystallization temperature may depend on deposition method.

Likewise in hafnia- and zirconia-based oxides [63], crystallization temperature of Lanthana film is reported to be higher with higher content of SiO_2 in bulk amorphous silicates [45]. So, crystallization temperature can be increased with a slight loss of gate capacitance.

Fig. 1.15 shows schematic of conductions between grains, as can be seen in ZnO (Zinc Oxide) varistors [64]. Grain corresponds to crystalline phase in the bulk of gate dielectric film. Path 2 plays a role in conduction in parallel, as well as path 1. Since the path 1 is associated with Schottky conduction and since the path 2 is correlated with hopping conduction in atomically disordered phase, current-voltage characteristic is composed of temperature-insensitive region at low voltage and temperature-sensitive region at high voltage. This is because Schottky conduction has a higher activation energy, i.e., barrier height than the hopping conduction has.

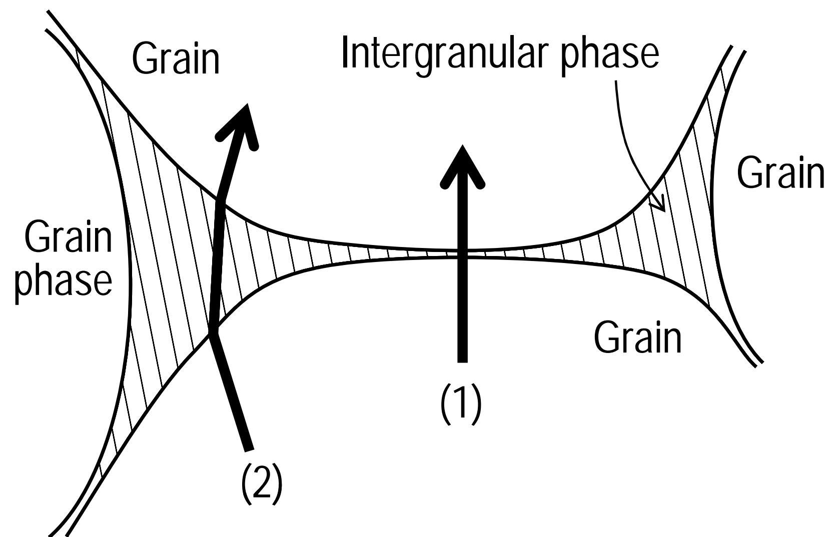


Fig. 1.15 Intergrain conduction paths between grains [64]. Path 1 is in the region of closet grain-grain contact over the Schottky barrier. Path 2 is through bulk intergranular material at grain corners. Path 1 is temperature sensitive with a Schottky barrier height. In contrast, path 2 is temperature insensitive, probably due to a low activation energy of hopping conduction in atomically disordered materials systems.

1.2.4 Contamination

It has been reported that La-based high-k dielectrics are easy to form carbonate during post-deposition exposure to air and the absorbed CO may act as a source of oxygen for interface oxidation [65]

1.3 MOS Capacitor Models

The insulator capacitor C_i is given by [66]

$$C_i = \frac{1}{\int_0^{t_{ox}} \frac{dx}{\varepsilon(x)}} \qquad \text{Eq. 1.17}$$

The electrical polarizabilities of the atoms are correlated with the dielectric constant, according to Clausius-Mosotti equation [67]:

$$\frac{\kappa_e - 1}{\kappa_e + 2} = \frac{1}{3\varepsilon_0} \sum_i n_i \alpha_i \qquad \text{Eq. 1.18}$$

Here, $\kappa_e = \varepsilon/\varepsilon_0$, n_i the number of i atoms having polarizabilities α_i. From the Clausius-Mosotti equation, the dielectric constant of a material, placed in a static electric field, can be expressed as a sum of the contributions from the electronic polarizability, the ionic polarizability, and the dipolar polarizability [67].

$$\frac{\kappa_e - 1}{\kappa_e + 2} = \frac{1}{3\varepsilon_0} \left(N_e \alpha_e + N_i \alpha_i + N_d \alpha_d \right) \qquad \text{Eq. 1.19}$$

Here, subscript e, i, and d stand for electronic, ionic, and dipolar, respectively.

The dielectric constant at the static electric field or nearly static (low frequency alternating) electric field is called static dielectric constant. In the visible spectrum (~10^{15}/sec), in which case electron contribution is only dominant and the dielectric constant equals the square of the refractive index n of the material. For this reason, it is called the high-frequency dielectric constant (or optical dielectric constant), $\kappa_f = n_i^2$.

1.4 MOS Diode Models

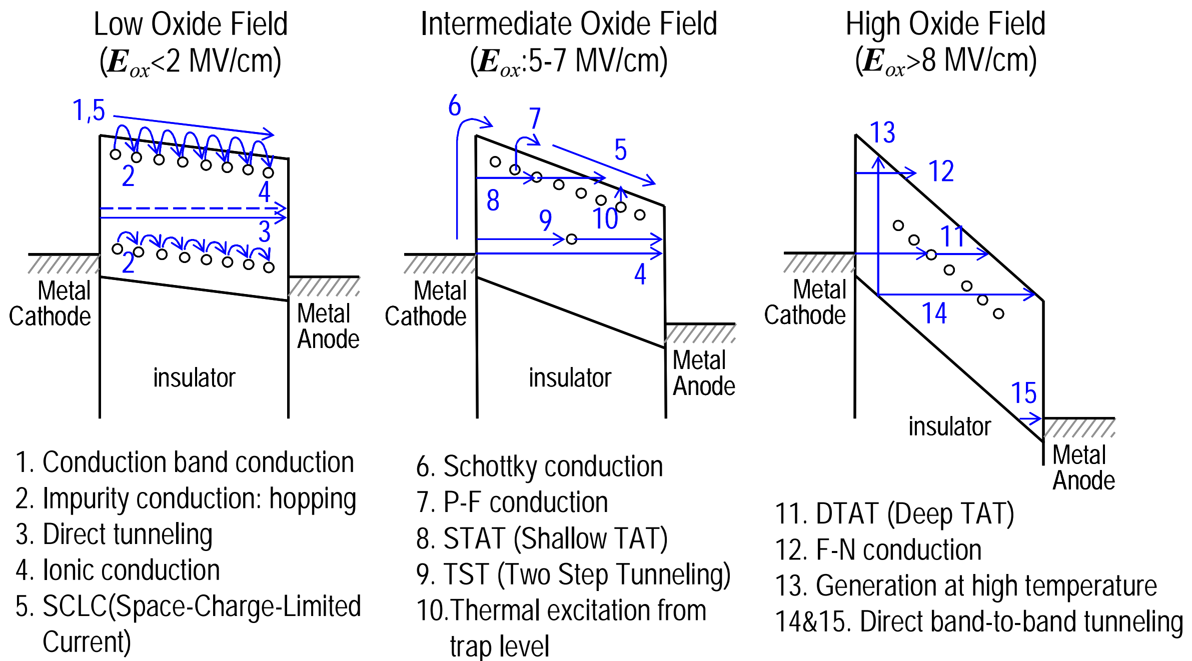


Fig. 1.16. Conduction mechanisms in thin oxide film [68].

Fig. 1.16 is the schematic view of the various conduction mechanisms with three oxide field regions. From the thermochemical model of the breakdown [68,69,70], the ultimate breakdown strength E_{bd} of the high-k dielectric can be predicted and E_{bd} of Lanthana is estimated to be 3.3 to 5.6 MV/cm with dielectric constant 30. Thus, among the conduction models illustrated in Fig. 1.16, low and intermediate oxide field models are important to explain the *J-V* characteristic of Lanthana film.

Conduction band conduction indicates the ohmic conduction determined by the carrier concentration in the conduction band. There are many ways in which electrons can be raised into the band: thermally from the valence band if it has a small enough forbidden bandwidth and the temperature is high enough (process 13 in Fig. 1.16), and by thermal excitation into the conduction band from trapping levels in the dielectric

(process 7 in Fig. 1.16).

In impurity conduction, electrons move from one trap to another without going up into the conduction band. An amorphous material has structural traps and hopping can occur between these trap sites. The hopping electrons have very low mobility, and thus any effect of them is likely to be masked if there are many electrons in the conduction band [68]. Frequently, gate currents of a film obeying ohm's law at low gate voltages are explained in terms of hopping conduction in the literature.

If the actual impurities or defects in the film migrate, ionic conduction occurs. However, this conduction seems to be difficult at near room temperatures. In fact, the ionic conduction of Lanthana has been reported at 677°C [22]. At that temperature, in addition to the ionic conduction, electronic conduction was also observed near the minima of the conductivity. The electronic conductivity was p-type at near-atmospheric pressures and n-type below the minima. From these results, it can be speculated that conduction of Lanthana film is partially contributed by the electron concentration due to oxygen Frenkel defect and oxygen vacancy.

Direct tunneling and SCLC conductions will be introduced after the following section in detail.

1.4.1 Bulk-limited and electrode-limited conductions

Analogous to thermal conductivity, the amount of conduction is a function of the amount of energy present (electric field), the number of carriers, and the amount of dissipation [71]. Ceramic materials can be classified in terms of electron conduction: metal-like, semiconductor, and insulator [71]. Like metals, some transition metal

oxides, such as ReO_3, CrO_2, VO, TiO, and ReO_2, conduct by electrons. Some metal oxides, such as CoO, NiO, Cu_2O, and Fe_2O_3, have an energy gap between the filled and empty electron bands such that conduction can occur when external energy is supplied to bridge the gap, likewise in semiconductors. Semiconducting properties can be achieved in many ceramics by doping or by forming lattice vacancies through nonstoichiometry. Examples are TiO_2, ZnO, Cds, $BaTiO_3$, Cr_2O_3, Al_2O_3, and SiC. For insulators, SiO_2, Al_2O_3, Si_3N_4, and MgO are famous due to high resistivity greater than 10^{14} Ωcm.

There are two types of electrons in an insulator: intrinsic and extrinsic [72]. Intrinsic electrons belong to the insulator and extrinsic electrons are injected from nearby electrodes. For the case of intrinsic electrons, the carrier density is low and conduction is of the ohmic type with a large resistivity. For the case of extrinsic electrons, two cases are possible. First, the electrodes behave as unlimited electron sources. This means that the current is only limited by the bulk of the insulator. Second, the electrodes limit carrier injection. The electrons once introduced travel free inside the insulator. From the view point of this, conductions illustrated in Fig. 1.16 can be classified into bulk-limited and electrode-limited ones. Bulk-limited and bulk-free conductions are listed in Table 5.1.

Due to the requirement for bulk-limited conduction [73,74], the J-V characteristics should initially be ohmic (J~V) at low applied voltage, with the help of ohmic contact (Mott-Gurney contact) at the injecting electrode. Here, the term ohmic contact is used to mean that the electrode can readily supply carriers to the insulator as needed. Schematics of ohmic and blocking contacts are shown in Fig. 1.17 [75]. In order to achieve an ohmic contact at a metal-insulator interface, it is necessary that the electrode work function be smaller than the insulator work function [75]. Although it is usually

difficult to determine the Fermi level of the insulator, the metal-insulator contact type can be estimated by measuring the normalized conduction and activation energy at low voltage where other conductions except ohmic are less dominant. The normalized conductance is given by:

$$G = \frac{d \ln I}{d \ln V} = \frac{VdI}{IdV} \qquad \text{Eq. 1.20}$$

When the normalized conductance is equal to 1 and the activation energy obtained has a physical meaning, current is ohmic and then the contact at the injecting electrode is ohmic. Thus, ohmic contact can be evaluated simply by investigating the two parameters at low voltage: normalized conductance and thermal activation energy. In addition to ohmic contact, conduction can be electrode-free, owing to carrier injection at low voltage region, such as Schottky conduction [76,77] and thermal injection into the tail of trap level states[78,79].

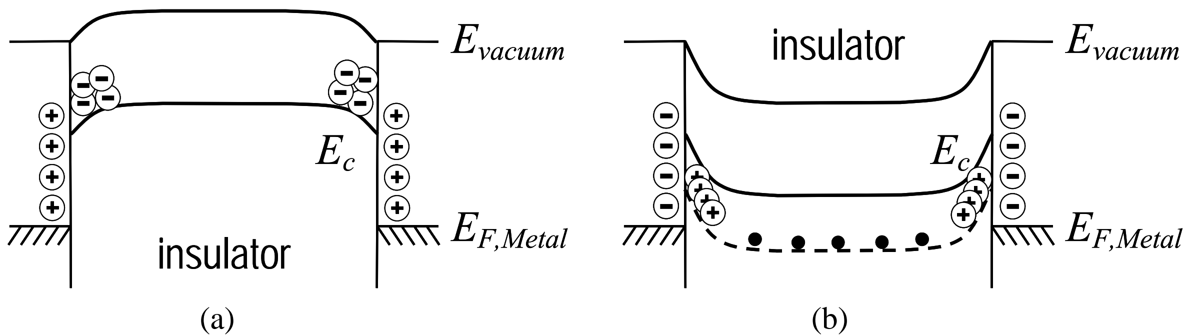


Fig. 1.17. Energy diagrams of two metal contacts on insulator, for (a) ohmic and (b) blocking contacts [75].

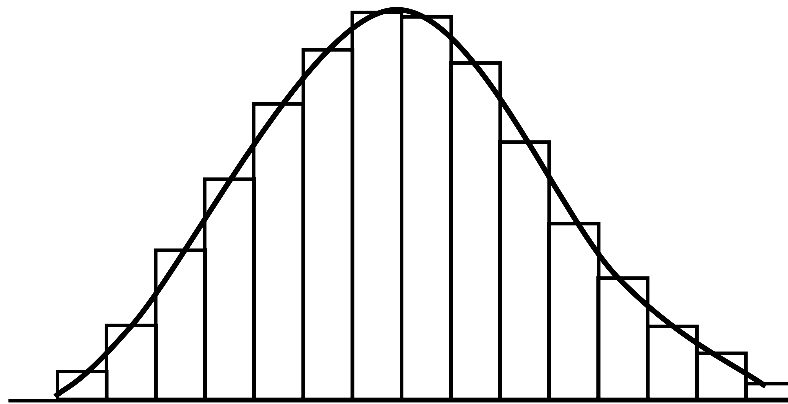


Fig. 1.18 Approximation of smooth barrier by a juxtaposition of square potential barriers [81].

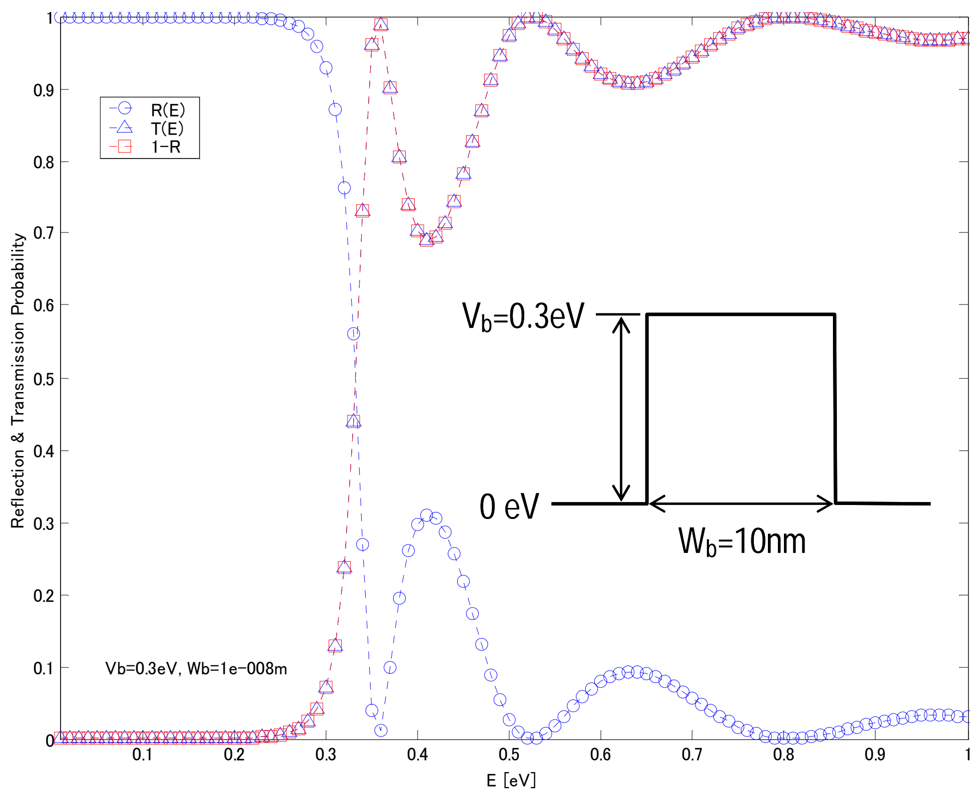
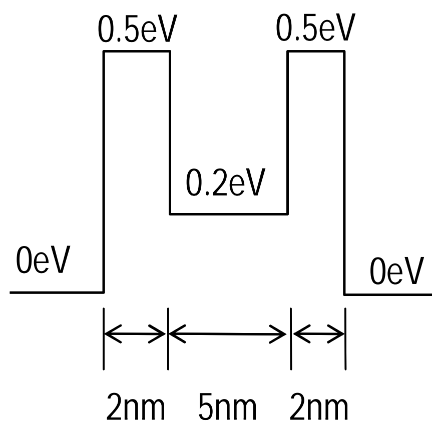
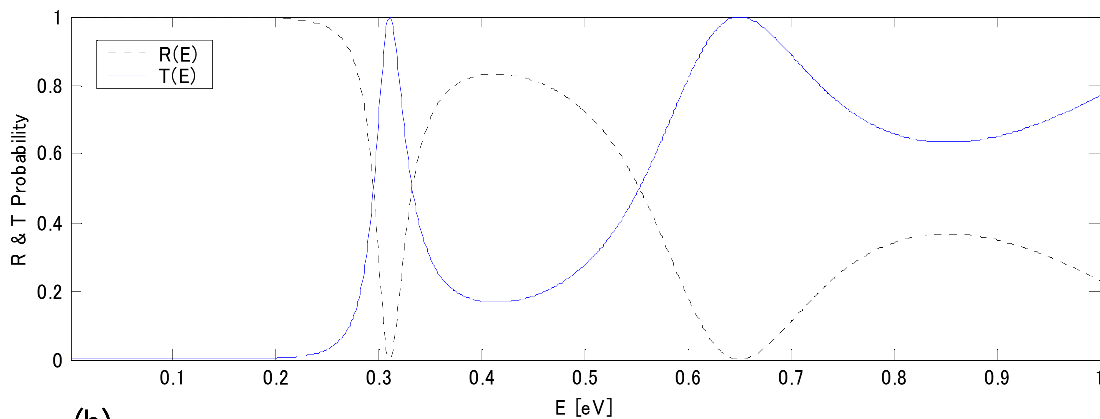


Fig. 1.19 Reflection (R) and tunneling (T) probability for single square potential barrier. Inset shows barrier dimensions: 10 nm width and 0.3 eV height.





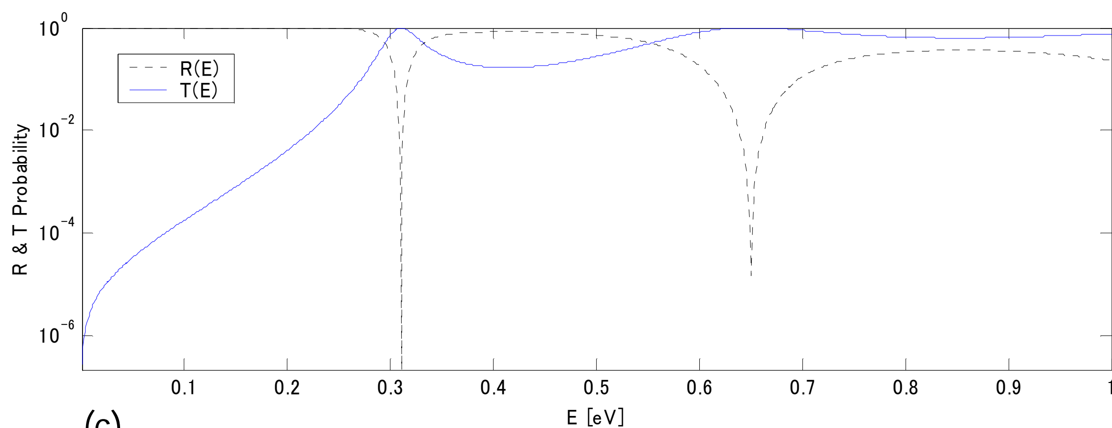


Fig. 1.20 Reflection (R) and tunneling (T) probability for double square potential barrier in (a). (b) is redrawn in (b) in logarithmic scale.

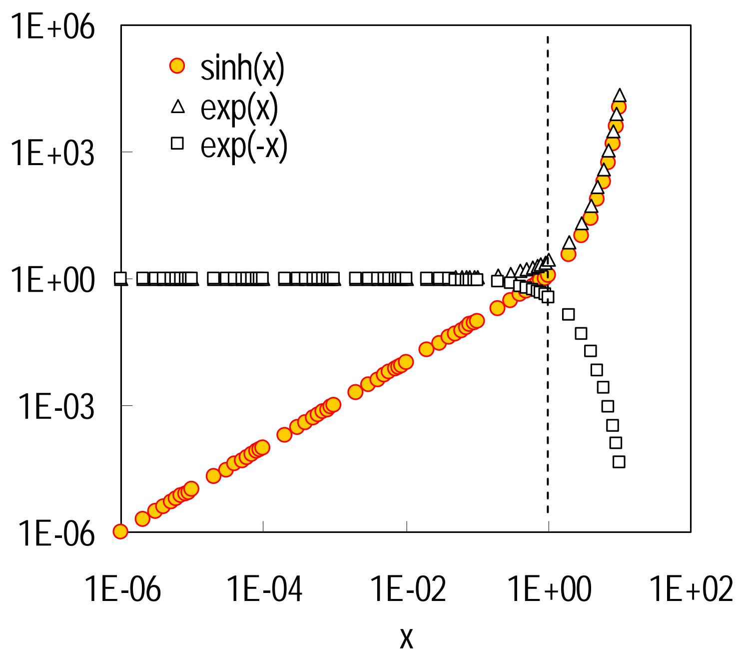


Fig. 1.21 Approximation of hyper sine (sinh(x)) function.

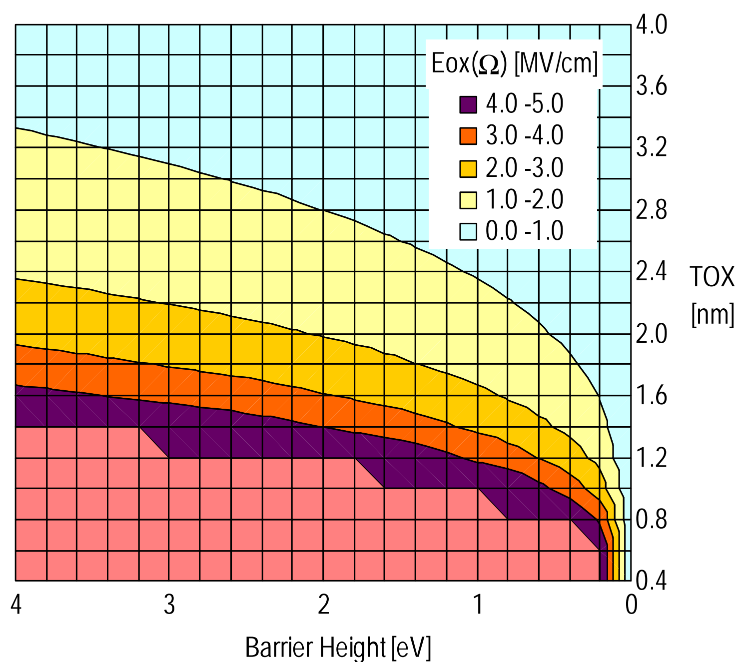


Fig. 1.22 Oxide electric field at which direct tunneling current behaves as ohmic conduction. Effective mass ratio 0.5 is assumed.

1.4.2 Direct tunneling current

If the energy of an electron is less than the interfacial potential barrier, classical physics predicts certain reflection of the electron at the interface. Quantum theory, however, contradicts this thesis. Due to the quantum mechanical wave nature of particles, there is a certain probability to penetrate an energy barrier without having enough energy to overcome the barrier. This is called tunneling. From the tunneling of the carriers, it is possible for carriers to travel the insulator without the aid of any defects in the oxide band gap. Direct tunneling current becomes prominent at the film thickness less than 30 A [7,80].

Direct tunneling current can be obtained in two ways: analytically and numerically. Numerical evaluation starts with the calculation of tunneling probability for arbitrary potential barrier, which can be approximated as illustrated in Fig. 1.18 [81]. The square barrier which consists of the arbitrary potential approximation can be solved numerically to get reflection and transmission probability, as shown in Fig. 1.19 and Fig. 1.20 for single and double square barriers, respectively.

For the case of MIM (Metal-Insulator-Metal) structure, direct tunneling current is given by [72]:

$$J = \frac{q^2}{\pi h}\frac{\phi_O}{s^2}\exp\left(-\alpha^* s\phi_O^{1/2}\right)\sinh\left(\frac{\alpha^* sV}{4\phi_O^{1/2}}\right) \qquad \text{Eq. 1.21}$$

Here, q is electronic charge, h Planck's constant (6.62×10^{-34}Js), ϕ_0 metal-insulator barrier height, α^* constant defined by Eq. 1.22, s insulator thickness, V applied voltage.

$$\alpha^* = \frac{2(2m_O q)^{1/2}}{\hbar}\left(\frac{m^*}{m_O}\right)^{1/2} = 1.25\times10^8\left(\frac{m^*}{m_O}\right)^{1/2} [=] \frac{1}{cm\sqrt{eV}}$$ Eq. 1.22

Here, $\hbar$ is reduced Planck's constant ($=h/2\pi$), m^* electron effective mass, m_0 electron mass at rest. Eq. 1.21 can be expanded as following:

$$J = \frac{q^2}{\pi h}\frac{\phi_O}{s^2}\exp\left(-\alpha^* s \phi_O^{1/2}\right)\frac{\exp\left(\frac{\alpha^* sV}{4\phi_O^{1/2}}\right)-\exp\left(-\frac{\alpha^* sV}{4\phi_O^{1/2}}\right)}{2}$$ Eq. 1.23

The first and second terms of the fraction in Eq. 1.23 describe forward electron flux and reverse electron flux, respectively. The reverse electron flux can be ignored when applied voltage is large. Eq. 1.23 can be approximated in terms of $\alpha^* sV / 4\phi_O^{1/2}$.

$$J \sim \begin{cases} V \;\; if \;\; \frac{\alpha^* sV}{4\phi_O^{1/2}} << 1 \\ e^V \;\; if \;\; \frac{\alpha^* sV}{4\phi_O^{1/2}} >> 1 \end{cases}$$ Eq. 1.24

Simplification of Eq. 1.23 is attributed to the following simple mathematical relations:

$$sinh(x) \cong \begin{cases} x \;\; when \; x << 1 \\ exp(x) \;\; when \; x >> 1 \end{cases}$$ Eq. 1.25

This relation is schematically illustrated in Fig. 1.21. It is worth mentioning here that, when applied voltage V is small, the direct tunneling current J can be thought of as being an ohmic conduction. Oxide electric field representing ohmic conduction is plotted as a function of film thickness and barrier height, in Fig. 1.22. For instance, when oxide film with 2 eV barrier height, 0.5 effective mass ratio, and 2 nm thickness, maximum oxide field to function as ohmic conduction can be obtained as:

$$E << \frac{4\cdot(\phi_0)^{1/2}}{\alpha\left(m^*/m_0\right)^{1/2}(s)^2} = \frac{4\cdot(2)^{1/2}}{\left(1.025\times10^8\right)(0.5)^{1/2}\left(2\times10^{-7}\right)^2} = 1.95\,MV/cm \qquad \text{Eq. 1.26}$$

This point is also seen in Fig. 1.22.

Analytical equation of direct tunneling current in case of MOS (Metal-Oxide Semiconductor) structure can be approximated by the following form [82,83,84]:

$$I = AV_{ox}^2 \exp\left\{-\frac{B}{V_{ox}}\left[1-\left(1-\frac{qV_{ox}}{\Phi}\right)^{3/2}\right]\right\} \qquad \text{Eq. 1.27}$$

Here, A and B are the constant, V_{ox} voltage drop across the oxide, Φ barrier height. It is interesting to note that this equation is no longer valid when $(1-q\,V_{ox}/\Phi)$ or $qVox>\Phi$ is negative. This situation is the voltage across the oxide is greater than the barrier height, which means that current is in the mode of F-N tunneling conduction [85]. For the F-N tunneling conduction, there should be a high electric field across the insulator, so that charges can tunnel though the trapezoidal part of the barrier.

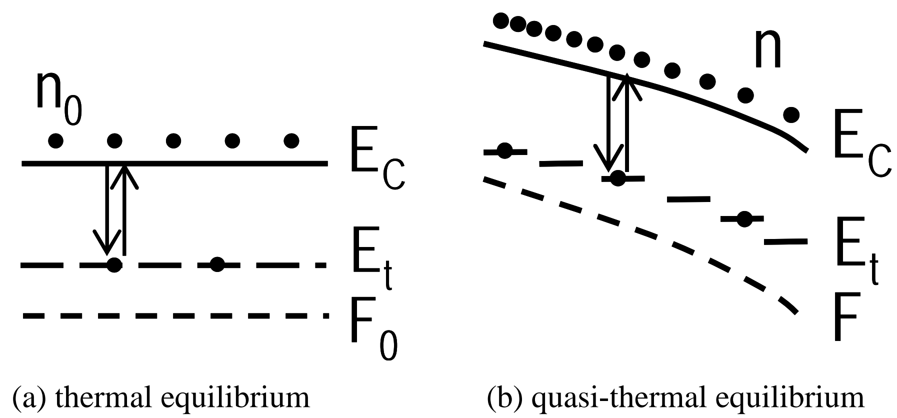


Fig. 1.23. Thermal and quasi-thermal equilibrium (steady-state) of electrons in conduction band E_c and trap levels E_t. F denotes quasi-Fermi level and the subscript 0 means the thermal equilibrium [87]. The equilibrium states can be achieved by low injection and low internal emission.

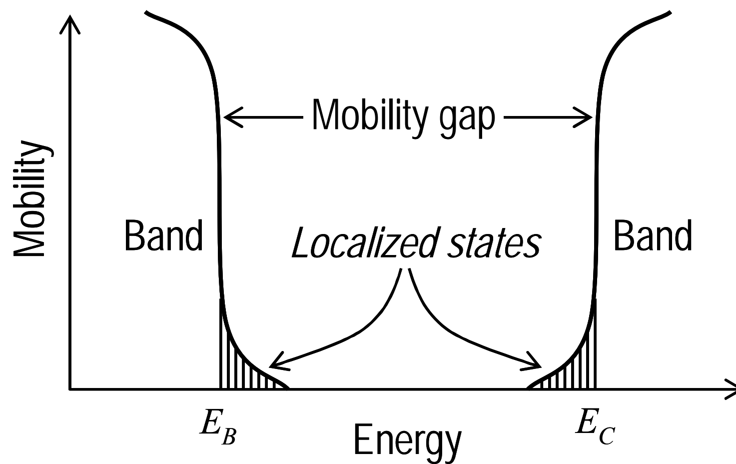


Fig. 1.24. Mobility of electrons as a function of energy showing mobility gap (amorphous state) [89,90,91].

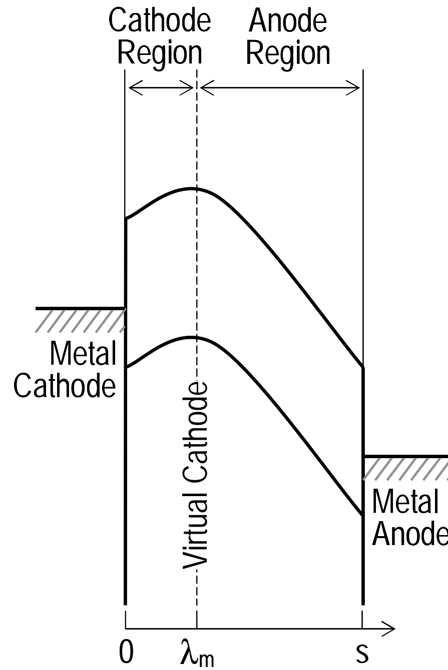


Fig. 1.25. Energy diagram illustrating virtual cathode, cathode region, and anode region under space-charge-limited condition [75,86]. λ_m denotes the position of virtual cathode in the insulator. The insulator is assumed to be free of surface states and ohmic contacts.

1.4.3 Space-charge-limited current (SCLC)

Fig. 1.23 shows thermal equilibrium and quasi-thermal equilibrium (i.e., steady-state) of electrons in the conduction band and the trap levels of the dielectric film [87]. Electron carrier concentrations for both cases are related to electrons in the trap levels. If the leakage current through the dielectric is bulk-limited, the magnitude of the current is determined by the electrons in the conduction band. The thermal and quasi-thermal equilibrium concentrations of electron carriers in the conduction band are strongly affected by trap level density, trap levels, and injected electrons to the trap levels. This implies that, with the help of equilibrium approximation, the leakage

current can be described by electrons in energy and space, causing accumulation of charges due to injected electrons, called space-charges.

The space-charge-limited current flow is efficient on the electrical properties of insulators at room temperature and below, because they normally have a low density of free carriers and charge unbalance can be easily produced by an applied voltage. The character and magnitude of space-charge-limited effects are determined largely by the presence of localized states which can trap and store charge in equilibrium with the free charge. In the case where charge is injected very effectively into the conduction (or valence) band of an insulator, the net transport is limited by the actual transport, that is drift and diffusion, of charge in the bend of the insulator [88]. Regarding electron injection into the oxide film, it seems to be difficult for electrons to jump into the conduction band by thermal transition or tunneling. However, if the oxide has a large trap density or DOS (density of states) tail near the cathode as shown in Fig. 1.24 [89,90,91], electrons are able to excite into the conduction band with small activation energy.

Fig. 1.25 shows oxide band structure distorted by the injected electrons. In order to satisfy thermal equilibrium, electrons are injected from the cathode into the insulator, resulting in a negative space-charge density adjacent to the cathode. An equal amount of positive charge remains on the cathode. Thus, the charge distribution consists of a positive charge sheet near a region of negative space charge. The same is true on the anode side. As the voltage bias increases, the net positive charge on the cathode increases and that on the cathode decreases. Total charge Q in the insulator can be expressed by the sum of cathode positive charge Q_1 and anode positive charge Q_2 [75,82]:

$$Q = Q_1 + Q_2 = \int_0^s \rho(x)dx = \int_0^{\lambda_m} \rho(x)dx + \int_{\lambda_m}^s \rho(x)dx \qquad \text{Eq. 1.28}$$

The positive charge on either contact is neutralized by an equal amount of negative charge contained between the contact and the plane at $x=\lambda_m$. Since the field due to Q_1 and Q_2 is zero at $x=\lambda_m$, the net filed there must be zero. For this reason the place at $x=\lambda_m$ is termed the virtual cathode. Eventually, when $Q_1=0$, the virtual cathode coincides with the physical cathode-insulator interface. Under this condition, the anode region extends throughout the whole of the insulator, and an ohmic contact no longer exists at the cathode-insulator interface. Thus, for further increasing voltage bias, the conduction process is no longer space-charge-limited, but rather it is emission-limited.

Space-charges have an effect to distort the oxide band shape. For electron carrier case, tunneling distance and barrier height are thought to be increased by accumulated space-charge, so that tunneling current is depressed [92]. Space-charge-limited flow is known to be effective at room temperature or below, since low density of free carriers causes charge unbalance easily [92]. This is also valid at high temperature with a considerable charge trap density, such as high-k materials.

Regarding the film thickness where SCLC can be valid, it has been reported that SCLC conduction governs the gate current of thin Si_3N_4/SiO_2 stacked film with 4.14 nm thick [93].

Fig. 1.26 shows the typical J-V behavior obeying the SCLC theory with combination of exponential and localized trap level distributions. In the logarithmic scale of J-V as shown in Fig. 1.26(a), one can find easily linear relationship according to the SCLC theory. On the other hand, in the semi-logarithmic scale as shown in Fig. 1.26(b) is difficult to realize the exact J-V relationship.

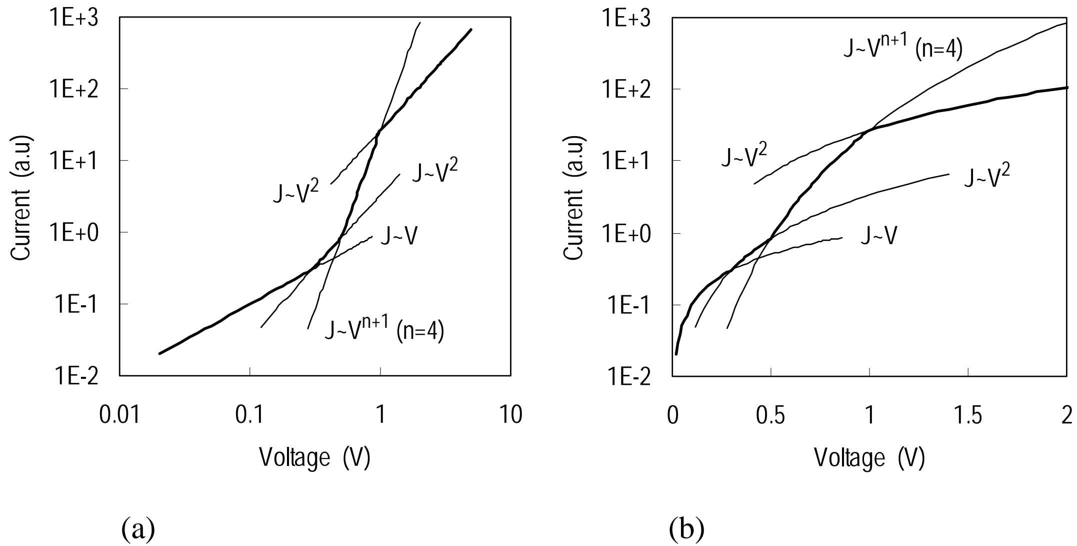
Space-charge-limited current with localized trap levels in the oxide band is given by:

$$J = \frac{9}{8}\varepsilon_0 \varepsilon_{ox} \mu \frac{V^2}{L^3} \qquad \text{Eq. 1.29}$$

Here, ε_0 and ε_{ox} are dielectric constants of vacuum and oxide film. μ is carrier mobility. V is applied voltage. L is film thickness. The mobility m is often found to be strongly field dependent, particularly at high fields [94]. Space-charge-limited current with exponential trap levels is given by:

$$J = N_c \mu \; q^{(1-l)} \left[\frac{\varepsilon \; l}{N_t (1+l)} \right]^l \left(\frac{2l+1}{l+1} \right)^{(l+l)} \frac{V^{(l+l)}}{L^{(2l+1)}} \qquad \text{Eq. 1.30}$$

Here, N_c is density of states of conduction band, q electronic charge, N_t total trap density. $l = T_t / T$ where T_t describes trap level distribution and T is absolute temperature.



(a) (b)

Fig. 1.26. Typical gate current by SCLC in (a) logarithmic scale and (b) semi-logarithmic scale. Scales are arbitrary.

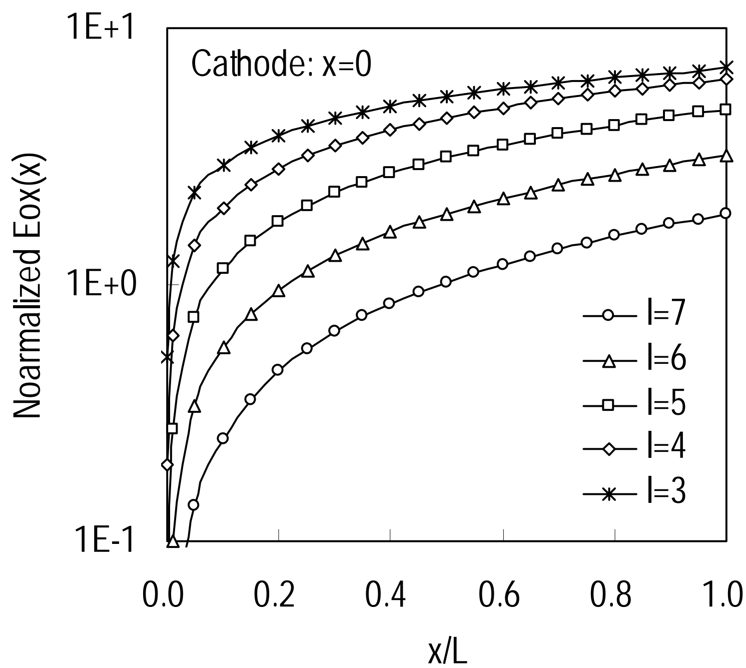


Fig. 1.27 Normalized electric field in oxide film owing to accumulated space-charge on traps with exponential trap level distribution. Normalization is carried out with respect to ohmic field (V/L).

As seen in Fig. 1.25, accumulation of electron charge near to the cathode leads to virtual cathode in the oxide film. This means that carrier transport is principally caused by the drift field between the virtual cathode and anode, with a continuous supply of charge from the charge accumulation region between the virtual cathode and the real cathode. So, one can expect that electric field near the cathode is small and that in the drift current flow region is large. This point can be realized by the oxide electric field as a function of position, which is given by,

$$E(x) = \left(\frac{2l+1}{l+1}\right)\left(\frac{x}{L}\right)^{\left(\frac{l}{l+1}\right)}\frac{V}{L}. \qquad \text{Eq. 1.31}$$

Normalized oxide field is seen in Fig. 1.27, based on Eq. 1.31. One can see that effective field in oxide film is nearly zero near the cathode and higher effective field near the anode than the applied field. This higher electric field may result in the larger current than can be expected from the external applied field, especially in the thin film.

Fig. 1.28 shows typical trap levels with exponential energy distribution and with maximum-trap-density-at-both-sides distribution. As regard to the spatial distribution of trap levels, uniform or non-uniform type of distribution does not alter the results of J-V relation. This is because the spatial trap distribution affects only the film thickness as suggested by Sworakowski [95,96]. In addition, the energetic trap distribution in the oxide band gap determines the J-V relation, such as $J \sim V$, $J \sim V^2$, or $J \sim V^{(n+1)}$. The film thickness in SCLC with a uniform trap distribution is equal to the physical film thickness (d), while the film thickness with spatially distributed traps is effective film thickness (d_{eff}). The effective film thickness describes the trap distribution inside the film. The J-V relation remains unchanged independent of how the trap is distributed

spatially.

Fig. 1.29 illustrates the relationship between the gate current and the trap density of the oxide film. Fig. 1.29 is not exactly true, but conceptually worth to read the idea that, if the gate current is explained by the SCLC theory, gate current can be reduced by increasing the oxide trap density. This interesting feature of SCLC provides a sharp contrast to other conduction mechanisms, which can give us a clue to the optimization of the film.

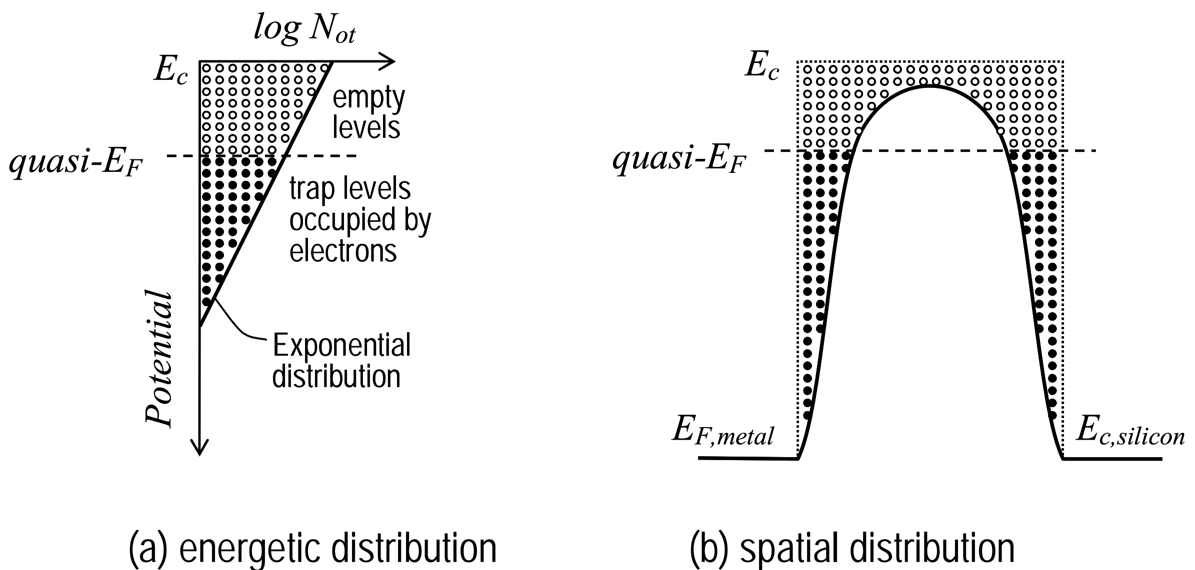


Fig. 1.28 Schematic trap level distribution at 0^oK,in the oxide (a) energetically and (b) spatially. Exponential trap distribution is assumed in (a). Trap levels filled with electrons are apparently separated from the unfilled trap levels on account of zero Kelvin degree consideration. Solid and hollow circles correspond to the trap sites with electrons and without electrons, respectively.

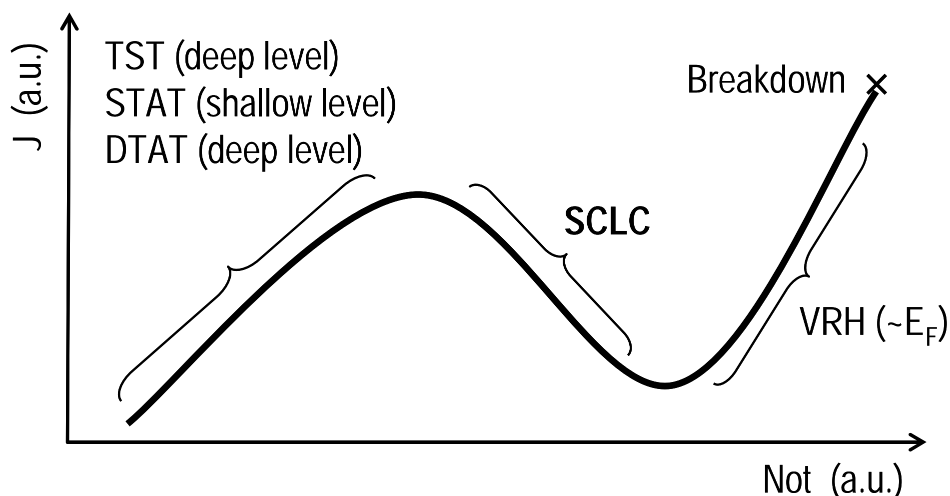


Fig. 1.29. Gate current as a function of oxide trap density N_{ot} in arbitrary scale.

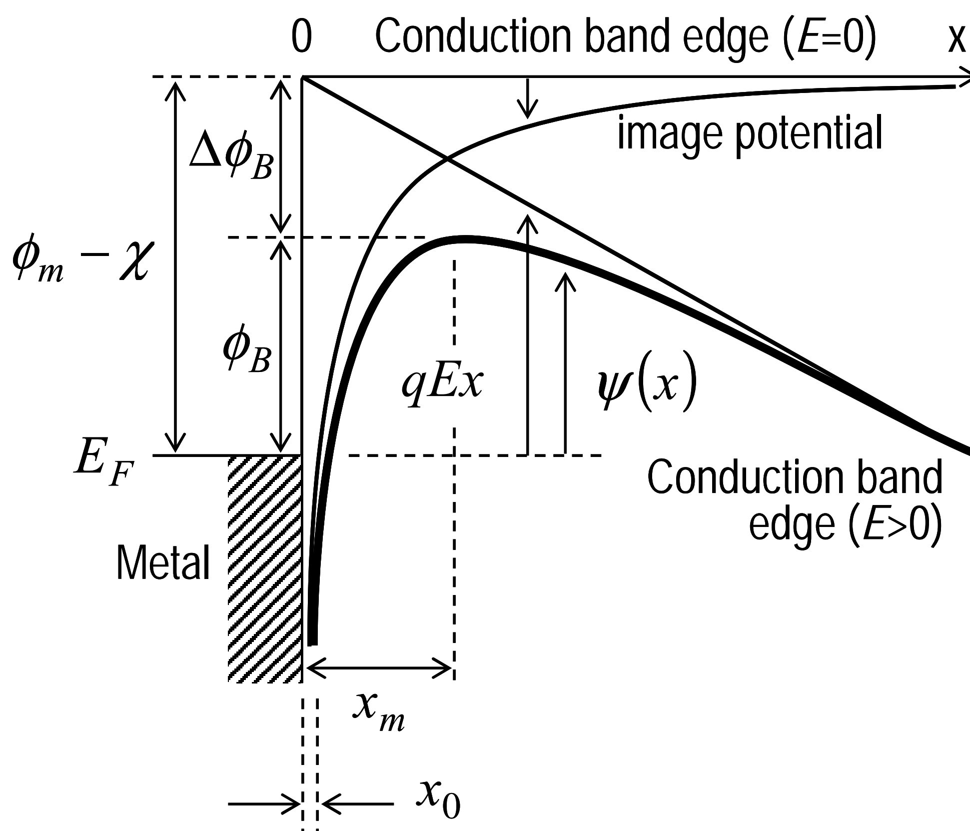


Fig. 1.30. Energy-band diagram between a metal surface and a vacuum. Conduction band edge means the vacuum energy level which is zero in electron energy. x_0 is introduced due to the singular point of image potential at x=0.

1.4.4 Schottky Conduction

The Schottky effect is the image-force-induced barrier lowering for charge carrier emission with an applied field [97]. Fig. 1.30 shows potential barrier at the metal-vacuum interface. Maximum barrier height is reduced to image-force effect when an electric field is applied. This can help the emission of thermally activated carriers from the metal electrode, which is called Schottky emission. This type of carrier emission is completely analogous to thermionic emission except that the applied field lowers the barrier height. Metal-vacuum system seen in Fig. 1.30 is also equivalent to metal-insulator system as well as semiconductor-insulator system, except for the dielectric constant of the vacuum part.

The main feature of Schottky emission is Schottky barrier lowering (or image force lowering) [97]:

$$\Delta\phi_B = q\sqrt{\frac{qE}{4\pi\varepsilon}} \qquad \text{Eq. 1.32}$$

Permittivity ε should be replaced by an appropriate permittivity characterizing the medium.

Tunneling current is written by [72,98,99,100]

$$J = \frac{4\pi m^* q}{h^3}\int_{E_m}^{\infty}\left[f_n(E) - f_n(E+V)\right]\left[\int_{E_m}^{E} D(E_x)dE_x\right]dE \qquad \text{Eq. 1.33}$$

Here, h is Planck constant, f Fermi distribution function, D tunneling probability, E_m barrier height ($\phi_0=\phi_m-\chi$), V applied voltage. Since carrier emission occurs at much higher energy levels than Fermi level of the injecting electrode, tunneling probability

can be regarded as 1. Then, integration yields

$$J = \frac{4\pi m^* q}{h^3}(k_B T)^2 \exp\left(-\frac{E_m - E_F}{k_B T}\right)\left[1 - \exp\left(-\frac{V}{k_B T}\right)\right] \qquad \text{Eq. 1.34}$$

Since the Schottky barrier lowering is given by Eq. 1.32,

$$E_m - E_F = \phi_0 - \left(\frac{qE}{4\pi\varepsilon_0\varepsilon_i}\right)^{1/2}. \qquad \text{Eq. 1.35}$$

On condition of $V >> k_B T$, then Eq. 1.34 becomes

$$J = \frac{4\pi m^* q}{h^3} k_B^2 T^2 \exp\left(-\frac{\phi_0}{k_B T}\right)\exp\left(\frac{\beta_S}{k_B T} E^{1/2}\right) \qquad \text{Eq. 1.36}$$

This is also called Richardson-Schottky equation [72]. Here, β_s is

$$\beta_S = \left(\frac{q}{4\pi\varepsilon_0\varepsilon_i}\right)^{1/2}. \qquad \text{Eq. 1.37}$$

As expected, the Schottky current is thermally activated process and the activation energy is characterized by Eq. 1.35. The activation energy is modulated by applied bias with Schottky barrier height lowering effect. This is seen in Fig. 1.31. One notices that the barrier deformation decreases as the dielectric constant increases, indicating that, in high-k oxide films, Schottky emission seems to be less probable than in conventional SiO_2 film.

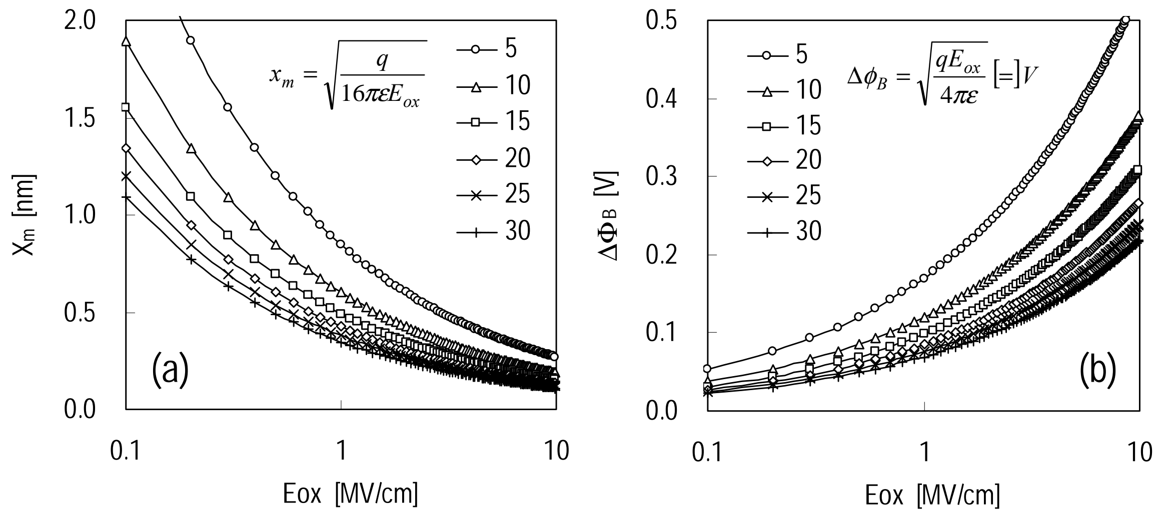


Fig. 1.31 Schottky barrier height lowering at X_m and by $\Delta\phi_B$, as a function of oxide field for different dielectric constants of the oxide film.

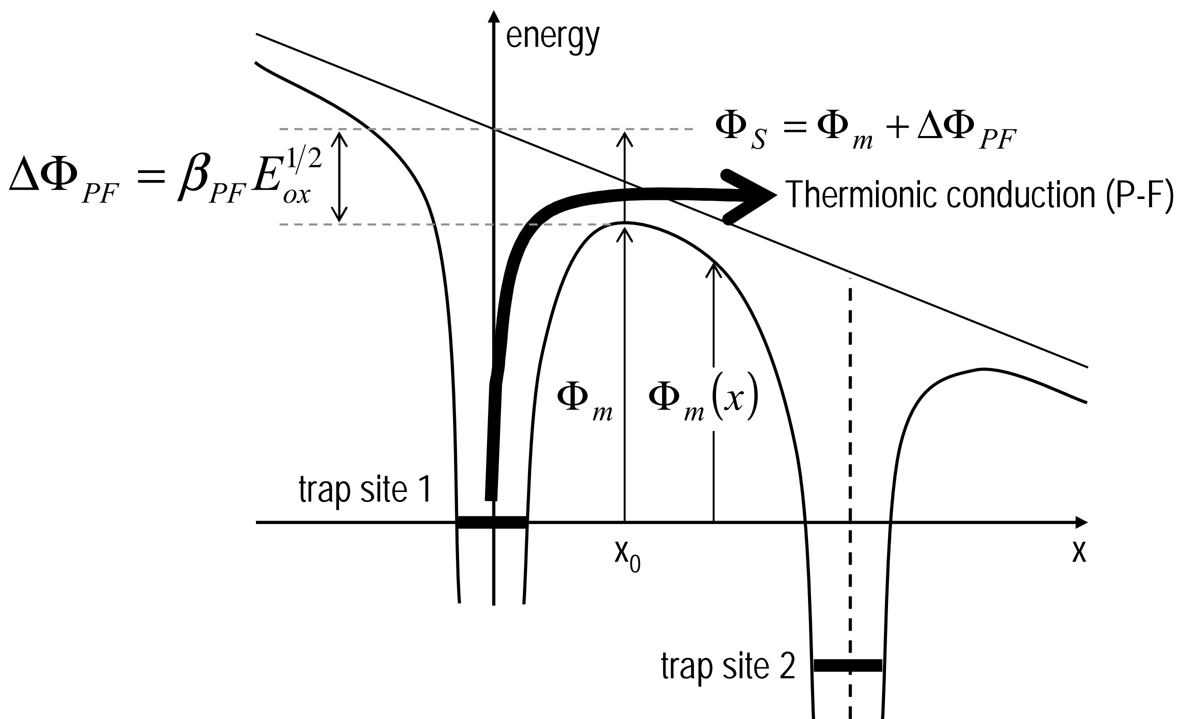
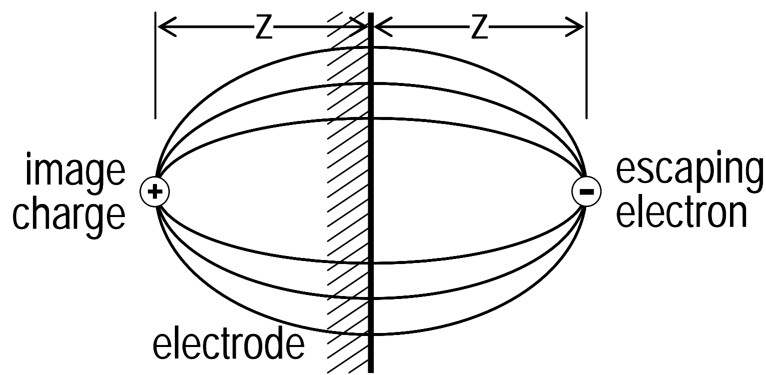


Fig. 1.32. Thermionic conduction (Poole-Frenkel conduction)



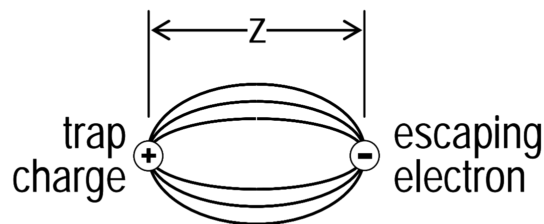


Fig. 1.33. Restoring force on escaping electron. (a) The Schottky effect. (b) The Poole-Frenkel effect [101].

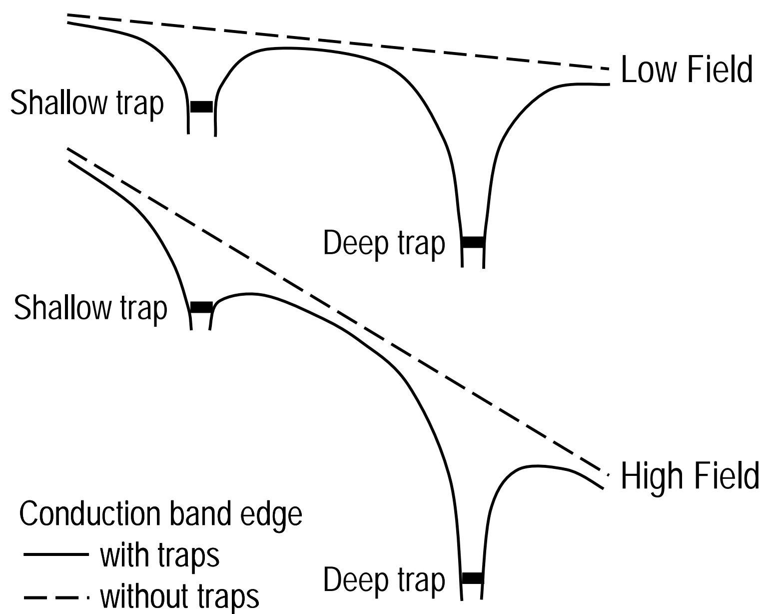


Fig. 1.34. Conduction band edge with and without trap levels at low and high oxide fields, showing barrier lowering of trap energy wells. Electrons trapped at deep trap energy levels can be emitted at high oxide field regime.

1.4.5 Poole-Frenkel (PF) Conduction

In MIS (Metal-Insulator-Semiconductor) structure, the PF and Schottky emission result from the lowering of a Coulombic potential barrier by an applied field. The Schottky emission is associated with the insulator barrier near to the injecting electrode, whereas the PF effect is associated with barrier at the trap well in the bulk of insulator film. Thus, neutral donor traps, that is neutral when filled and positive when empty, do not experience the PF effect owing to the absence of the Coulomb potential.

Fig. 1.32 shows thermionic emission of trapped carriers in the bulk of the film, which occurs at the trap site. Internal thermionic emission is called PF emission, while external one is Schottky emission. Another way for emission of electron is hopping process, which is a kind of tunneling process in a short range.

Table 1.2. Schottky-emission and Poole-Frenkel-emission

Item	Schottky Emission	Poole-Frenkel Emission
Conduction	Bulk-free	Bulk-limited
J-E_{film} on T_{film}	Uncorrelated	Correlated
Location	Interface	Bulk
Origin	Image force	Coulomb interaction
J-V polarity	Asymmetric	Symmetric

Difference between the Schottky-emission and PF-emission are summarized in Table 1.2. It should be notified here that PF conduction by PF emission is closely related to the oxide film thickness while Schottky conduction by Schottky emission is not related to that, as far as the equal oxide field is concerned.

Fig. 1.33 illustrates the restoring force in both Schottky and PF effects, which comes from Coulomb interaction between the escaping electron and a positive charge [101]. The restoring force is due to electrostatic potential that make electron move back to its equilibrium position. Although the restoring force is same for the both, they differ in that the positive image charge is fixed for PF barriers but mobile with Schottky emission. This results in a barrier lowering twice as great for the PF effect.

$$\Delta\phi_{PF} = \left(\frac{q^3 E}{\pi\varepsilon\varepsilon_0}\right)^{1/2} = \beta_{PF} E^{1/2} \qquad \text{Eq. 1.38}$$

$$\Delta\phi_{S} = \left(\frac{q^3 E}{4\pi\varepsilon\varepsilon_0}\right)^{1/2} = \beta_{S} E^{1/2} \qquad \text{Eq. 1.39}$$

In that the electrons have enough energy to go over the energy barrier and travel in the conduction band with a mobility μ which is dependent on the scattering with the lattice, the general expression of the bulk current is expressed by [72]

$$J = qn(x)\mu E \qquad \text{Eq. 1.40}$$

The concentration of free carriers in the insulator is

$$n = N_c \exp\left[-\frac{q}{kT}(E_c - E_F)\right] \qquad \text{Eq. 1.41}$$

Since E_c-E_F is equal to effective trap barrier height including barrier lowering effect

described by Eq. 1.38, the effective barrier height and current governed by the PF emission is written by:

$$E_c - E_F = \phi_s - \Delta\phi_{PF} = \phi_s - \beta_{PF} E^{1/2} \qquad \text{Eq. 1.42}$$

$$J = qN_c \exp\left(-\frac{\phi_s}{kT}\right)\exp\left(\frac{q}{kT}\beta_{PF} E^{1/2}\right)\mu E \qquad \text{Eq. 1.43}$$

On the other hand, PF emission, as well as Poole emission, loses its barrier height at oxide fields higher than the critical field [102]:

$$E_{crit.}^{PF} = \left(\frac{\Phi_i}{\beta_{PF}}\right)^2, \qquad \text{Eq. 1.44}$$

where ϕ_i is the trap barrier height at zero oxide field. At electric field higher than $E_{crit.}$, the emission process, instead of bulk-process, begins to play a dominant role.

1.4.5 Transient current

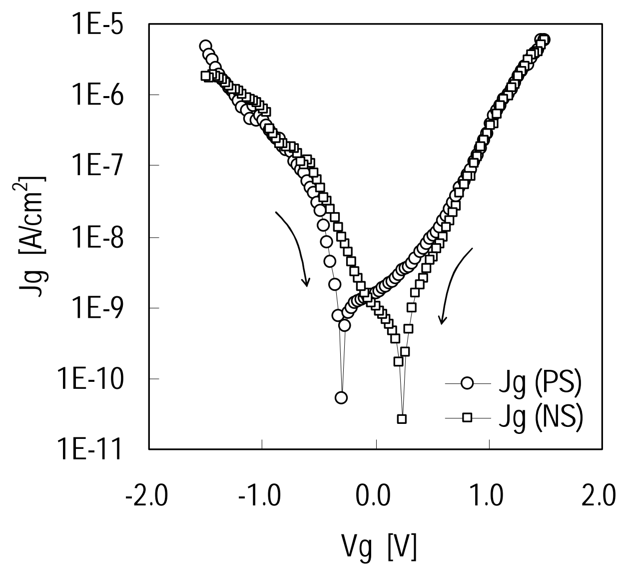


Fig. 1.35. Transient current in Lanthana film deposited by e-beam evaporation. Film thickness is 7.7 nm and annealed at 300°C in oxygen ambient for 5 min before gate electrode deposition.

If the gate oxide has a large interface state density or oxide trap density especially adjacent to the silicon substrate, gate current can be transient. Several studies have been conducted on the transient current of the gate oxide [93,103,104,105,106,107,108].

Fig. 1.35 shows the transient conduction of the Lanthana film. One can see that the gate current depends on the path of gate bias. This could be due to the trapping and detrapping the carries near the silicon substrate.

1.4.6 Image force effect

The abrupt changes in potential at the metal-insulator or insulator-semiconductor interface are physically unrealistic, since abrupt changes in potential imply infinite electric fields. The potential changes gradually as a result of the image force [16]. When an electron is at a distance x from the metal, a positive charge will be induced on the metal surface, which is called image charge. The force of attraction between the electron and the image charge is equivalent to the force that would exist between the electron and an equal positive charge located at –x. This attractive force is called the image force and given by [97].

$$F = \frac{-q^2}{16\pi\varepsilon x^2} \qquad \text{Eq. 1.45}$$

Here, q is electronic charge and ε_0 is the permittivity of the insulator. From the Eq. 1.45, one can realize that attractive force is inversely proportional to the dielectric constant of the film, so that in the high-k film, the effect of the image force will be small. It is worth commenting that the dielectric constant in the image force equation is the high-frequency constant for the electrode-limited conduction case, since electrons spend only an extremely short time in the immediate vicinity of the surface in the course of carrier emission [16].

1.5 MOSFET Models

1.5.1 Split-CV method

In order to characterize the effective channel mobility of the MOSFET, the well-known split C-V method is used [109,110].

Fig. 1.36 illustrates the schematic data handling process used in this study. Effective mobility and channel field is obtained in the following equations.

$$\mu_{eff} = \frac{L_{eff}}{W_{eff}} \frac{I_D}{V_{DS} Q_n}$$
$$F_{eff} = \frac{Q_{dep}(V_{gs}) + \eta \cdot Q_{inv}(V_{gs})}{\varepsilon_{si}} \quad \text{Eq. 1.46}$$

Here, η is 1/2 in the Newtonian mechanics and 11/36 in the Quantum theory, while 1/2 for NMOSFET and 1/3 for PMOSFET are practically used.

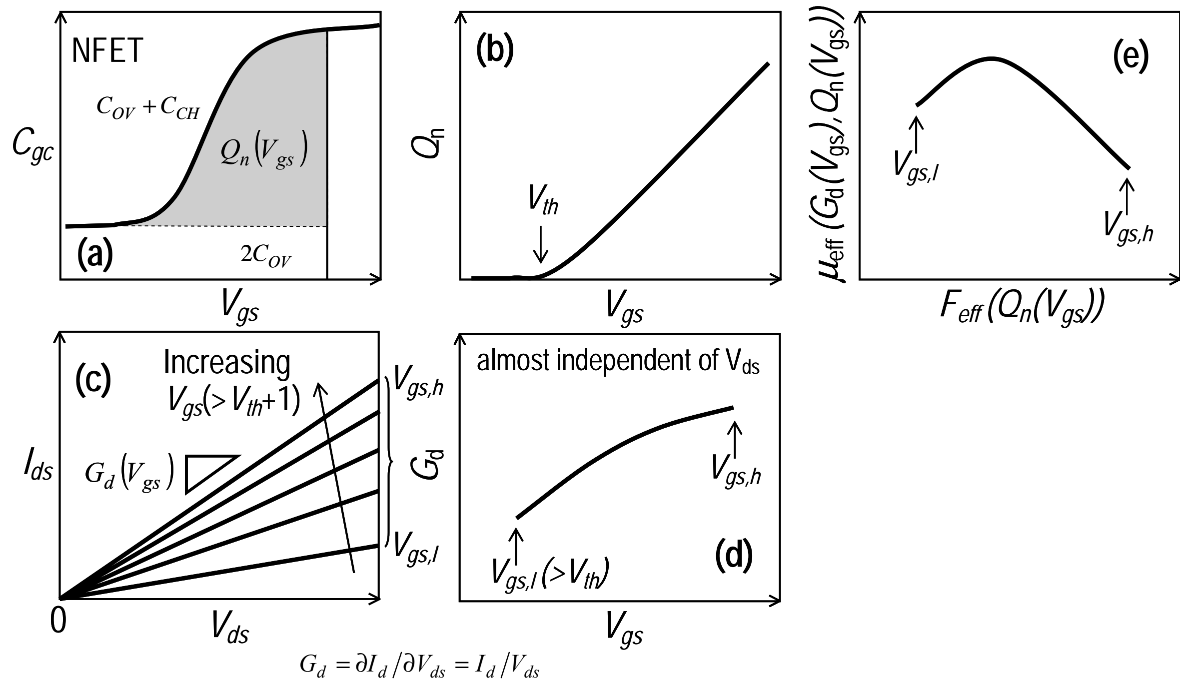


Fig. 1.36. Schematic flow of split C-V method.

1.5.2 Flicker noise

There are three types in noise: thermal, shot, and generation-recombination [111,112,113]. The thermal noise of a resistor is caused by the random motion of the current carriers. It can be dealt with diffusion noise, velocity fluctuation noise, and quantum correction. Shot noise occurs when carriers cross barriers independently and at random.

The number fluctuation model of 1/f nose is suggested by McWhorter [114]:

$$\frac{S_{ID}}{I_D^2} = \left(\frac{g_m}{I_D}\right)^2 S_{VG} \qquad \text{Eq. 1.47}$$

Voltage noise spectral density is related to the oxide trap [115]:

$$S_{VG} = \frac{q^2 kT\lambda N_{ot}}{8WLC_{ox}^2 f} \qquad \text{Eq. 1.48}$$

1.6 Purpose and organization of the study

So far, motivation for alternative gate dielectric, general property of the rare earth metal oxides, and device models have been discussed.

The objective of this study is to investigate the conduction mechanism of the Lanthana gate dielectric, to suggest how to maintain the low leakage current based on the detailed conduction mechanisms, and to make the base for the reliability study. To ensure the reliability of the dielectric film, the proper conduction mechanism should be clarified in advance. This is mandatory because the soft, hard, and progressive breakdown behavior occur by a certain carrier conduction mechanism and can be principally explained according to it.

The thesis composed of nine chapters, as illustrated in Fig. 1.37. Following this chapter, chapter 2 describes the common features of fabrication and characterization methods for Lanthana MOS and MOSFET. The first part of chapter 2 is devoted to the film deposition method and the following three parts are dedicated to the optical and electrical characterization methods for the film. From the C-V analysis, the precise oxide field can be achieved and applied to investigating for the various conduction mechanisms of the J-V. Due to the non-linearity of the gate capacitance and current on the gate voltage, all the analysis to figure out the detailed model was carried out numerically with a home-made code. Chapter 3 describes MOS capacitor geometry effect on the gate leakage current. Investigating gate leakage currents of the different gate electrode areas and structures is a key process to allow greater understanding of conduction mechanisms related to the currents. Chapter 4 describes the analysis for the conduction mechanisms for the Lanthana films annealed at ultra high vacuum state.

From the analysis, it could be found that SCLC conduction plays an important role in the gate current. To characterize the physical property of the SCLC conduction, temperature sensitivity and insensitivity equations for J-V-T relation were proposed and explained well the J-V-T behavior of the Lanthana film. Different behavior of J-V for two films was also explained well in terms of SCLC theory. In addition to J-V analysis, flat-band voltage shift of MOS capacitor with annealing condition was analyzed and led to the conclusion that interfacial layer growth leads to the positive fixed oxide charges near the interface between Lanthana and silicon substrate. Chapter 5 describes the analysis for the conduction mechanisms for the Lanthana films annealed at low-temperature in dry-nitrogen ambient. Various bulk-limited and electrode-limited conduction mechanisms were summarized and proposed the models describing J-V. Also, reasons for ruling out the conduction mechanisms were discussed. Chapter 6 describes variation in the gate leakage current of Lanthana MOS capacitor. MOS capacitors on the same wafer fabricated at the same time showed often variation in the magnitude of the gate current, although its J-V behavior was almost same. From the C-V and J-V analyses, possibility of non-uniformity in the film thickness could be eliminated. Variation at the low gate voltage was explained in terms of SCLC theory. Based on the theory, trap energy level distribution in the oxide band gap were suggested. From the suggested trap level distribution, high and low leakage currents were explained well. Chapter 7 describes the C-V and J-V results of Lanthana MIM capacitors. From the C-V characteristic and TEM(Transmission Electron Microscopy)/EDX(Electron Dispersive X-ray) analysis, it was found that Al reacts with Lanthana causing positive fixed oxide charges near the interface and less capacitance. Four types of J-V behavior were observed and found to be essentially same as those of MOS capacitors. The physical meaning of the similarity for both

MOS and MIM capacitors was discussed. Chapter 8 describes the MOSFET with Lanthana gate dielectric. The excellent I_d-V_g and I_d-V_{ds} behavior of MOSFET were obtained. From the split C-V method, effective channel mobility with various PDA conditions was investigated and the maximum mobility 290 cm^2/V-s was obtained. To get the oxide trap density and to compare with the effective channel mobility, 1/f noise characteristic was measured for both HF-last and CO-last (chemical oxide last) Lanthana films. From the relationship between the channel mobility and the oxide trap density, it was found that the mobility is proportional to the oxide trap density and the oxide trap density was high in the CO-last film, rather than in the HF-last film. It is also discussed that the high oxide trap density of the CO-last film could explain the previous reported result that the CO-last Lanthana film has a smaller gate leakage current of the MOS capacitor than the HF-last. Finally, chapter 9 summarizes the findings of the research and suggests possible areas for further investigation.

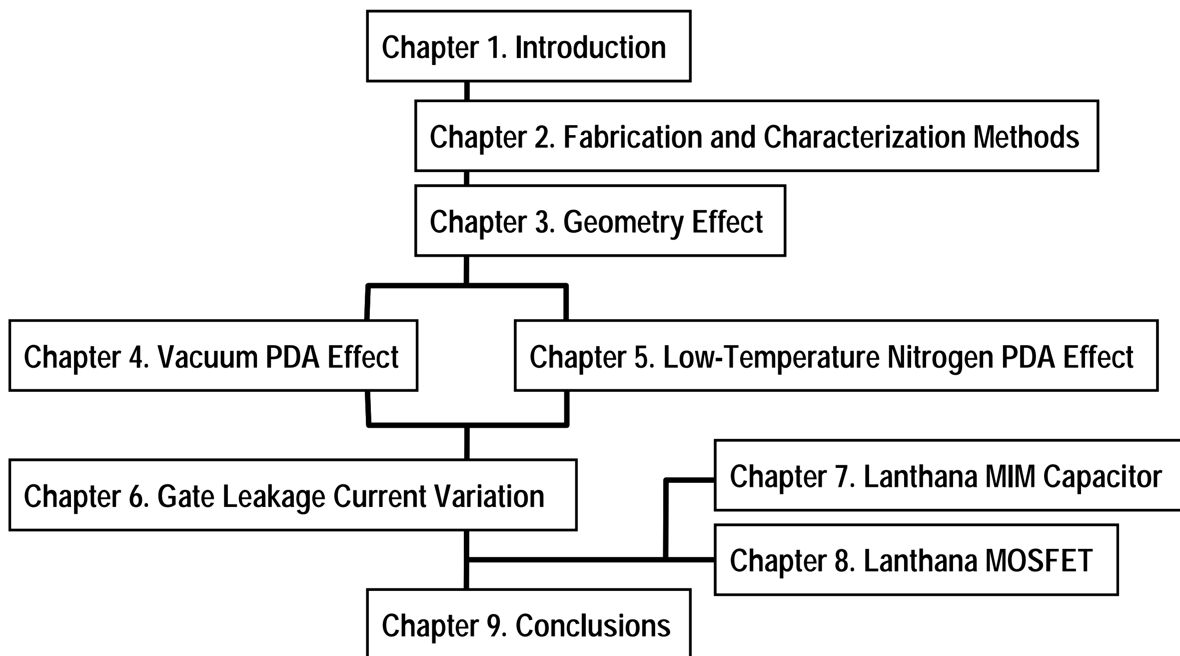


Fig. 1.37. Outline of this thesis

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Chapter 2. Fabrication and Characterization Methods

2.1 E-beam evaporation

2.2 Spectroscopic ellipsometry

2.3 C-V characteristic

2.4 J-V characteristic

Reference

2.1 E-beam evaporation

As discussed by Lucovsky [1], the high-k gate dielectric film must be deposited. Lanthana film is deposited by the e-beam evaporation method in the ultra high vacuum chamber, as shown in Fig. 2.1. There are four types of oxide sources in the bottom side of the chamber. One of the sources is La_2O_3 and heated by the e-beam near the source. Then, since the chamber is maintained at the ultra high vacuum state, the Lanthana molecule begins to evaporated when the temperature of the source is greater than the evaporation temperature. Evaporation temperature is reported as 3620°C [2]. Figure 2-2 shows the equilibrium vapor pressure of La and La_2O_3 with some materials as a function of temperature. From the equilibrium vapor pressure with temperature, SiO_2 is evaporated at 900°C at around 10^{-9} torr. This can be used to clean the surface of the silicon substrate to remove the natural oxide, and this method is referred to as thermal-flash.

In general, deposited films have large atomic defects compared to the thermally grown film [4]. This deficiency of the composition often leads to the fixed oxide charge. Since the fixed charge of the as-deposited Lanthana film is always positive, oxygen deficient sites in the film are expected, which can function as an electron trapping center.

2.2 Spectroscopic ellipsometry

The physical film thickness was optically extracted by Otsuka FE-5000 ellipsometer using a Cauchy model [5] and a single layer approximation. Incident angle was fixed to 70°. Photon energy varied from 1.55 to 4.14 eV for data fitting. 1.55 and 4.14 eV correspond to wavelength 800 and 300 nm, respectively. Film thickness without PDA corresponds to the as-deposited film thickness.

The index increase with decreasing wavelength in the visible range, and this is referred to as normal dispersion [5]. One of the common empirical relations for this behavior is the Cauchy formula:

$$n = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4} \qquad \text{(Eq. 2.1)}$$

Here, n is refractive index, l wave length, A, B, and C are fitting constants. On the other hand, in the region of the natural frequency where resonance occurs, the index decrease with decreasing wavelength, and this is called anomalous dispersion. Eq. 2-1 can be derived by the following way [5]. The square of the refractive index n, at frequencies far from the resonant frequency, is expressed by the relation:

$$n^2 = 1 + \frac{Ne^2/\pi m}{{\nu_0}^2 - \nu} \qquad \text{(Eq. 2.2)}$$

where N is the number of the atoms per unit volume, e is the electronic charge, m is the electronic mass, ν_0 is the natural frequency, and ν is the frequency of the incident radiation. If $\nu >> \nu_0$, with the binomial series expansion, Eq. 2-2 becomes

$$n^2 = 1 + \frac{Ne^2}{\pi m}\frac{1}{\nu_0^2}\left[1-\left(\frac{\nu}{\nu_0}\right)^2\right]^{-1} = 1 + \frac{Ne^2}{\pi m}\frac{1}{\nu_0^2} - \frac{Ne^2}{\pi m}\frac{\nu^2}{\nu_0^4} \qquad \text{(Eq. 2.3)}$$

It is worth to introduce that densification of the films with PDA temperatures can be evaluated by the film density obtained from the Lorentz-Lorenz relationship, in the similar fashion of SiO_2 thin film case [6]. From the refractive index n, the film density can be determined by the Clausius-Mossotti (CM) or Lorentz-Lorenz relationship [7, 8].

$$\rho = K\frac{n^2-1}{n^2+2} \qquad \text{(Eq. 2.4)}$$

where K is a constant, which can be evaluated using the values of bulk Lanthana. For Lanthana, n=2.08 and ρ=6.5g/cm^3 [9], then K=12.8. Including the ionic component of the dielectric polarizability, K=20.8 [10]. Since the refractive index ranging from 300 to 800 nm is in the optical region, the dielectric constant arises essentially from the electronic polarizability [11]. So, K=12.8 is reasonable, rather than 20.8. Recently, several studies have been made on the details of the dielectric polarizability [12,13,14].

2.3 C-V characteristic

C-V of Lanthana film was measured with various frequencies (1K~1MHz). To remove the frequency dispersion on C-V caused by leakage current of oxide, we used two-frequency model to achieve single corrected C-V [15,16]. By using of nonlinear regression method [18], the corrected C-V was compared to the calculated C-V, and then oxide field was obtained. EOT (Equivalent Oxide Thickness) was calculated from the corrected C-V with taking quantum effect into account. From EOT and

physical thickness, oxide field in Lanthana film was calculated. This theoretical oxide field was used to check conduction mechanisms for leakage current density. Lanthana film oxide field has a relation to SiO_2 equivalent oxide field:

$$E_{La_2O_3} = \frac{\varepsilon_{SiO_2}}{\varepsilon_{La_2O_3}} E_{SiO_2} = \frac{EOT}{T_{phy}} E_{SiO_2} \quad \text{(Eq. 2.5)}$$

2.4 J-V characteristic

Measured J-V data is first fitted in a small data span, for instance, 5 points, to the various conduction mechanisms numerically. Then, an identified conduction mechanism checks over the wider span of data to evaluate the maximum range of the J-V. Not only the numerical fitting is carrier out, but also the physical meaning from the fitted conduction mechanism is checked its validity. The latter is important because a good fit to the experiment with poor physical parameters is common in real work.

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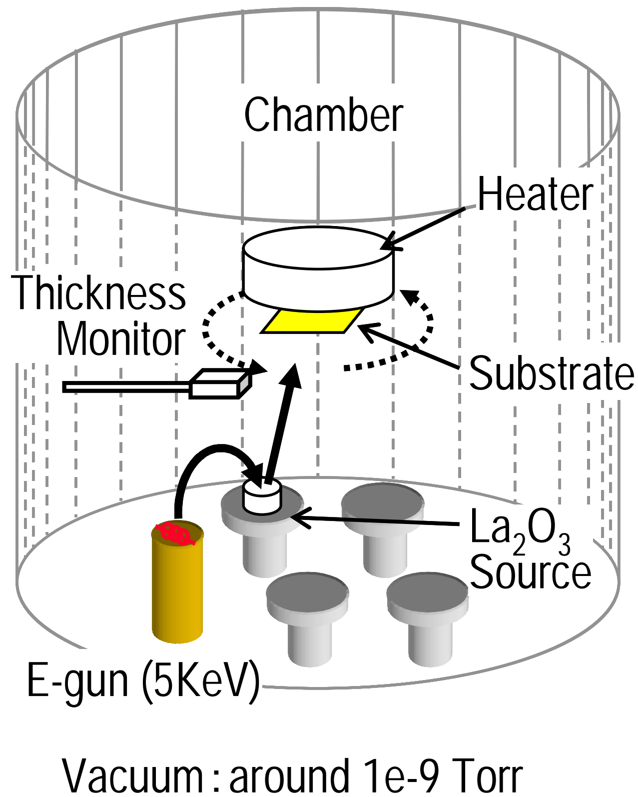

Fig. 2.1. Schematic of the chamber for Lanthana film deposition.

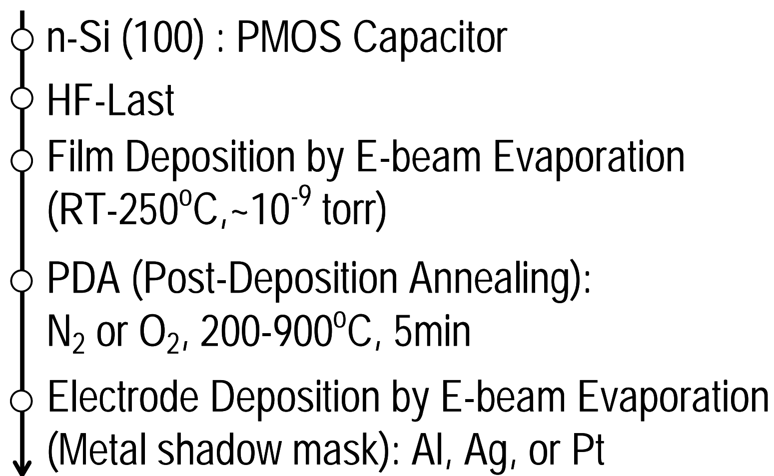

Fig. 2.2. Process steps and experimental ranges for Lanthana gate PMOS capacitor.

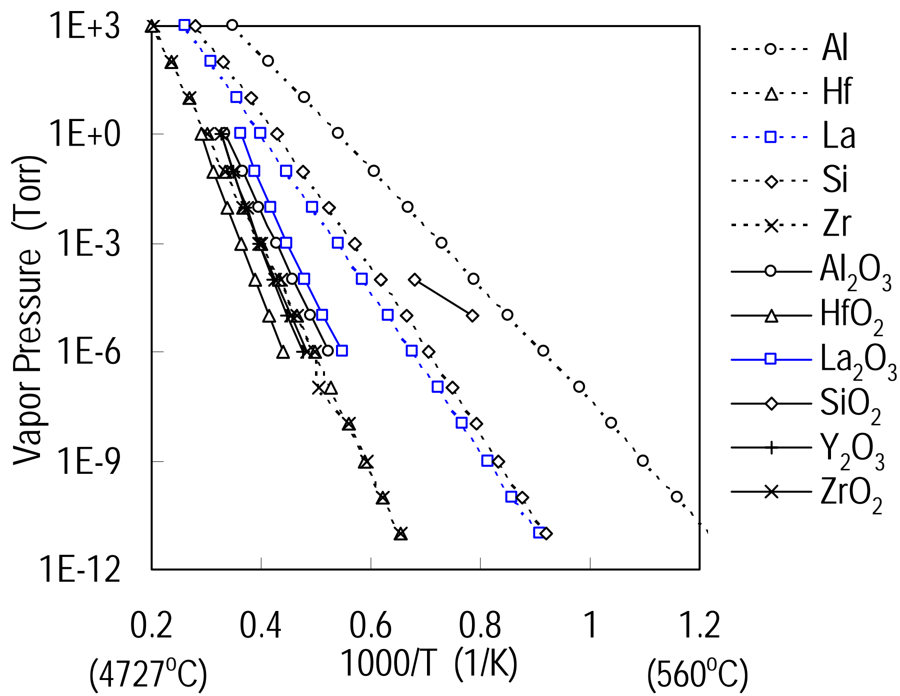

Fig. 2.3. Equilibrium vapor pressure of La and La_2O_3 compared to some materials, as a function of temperature [3].

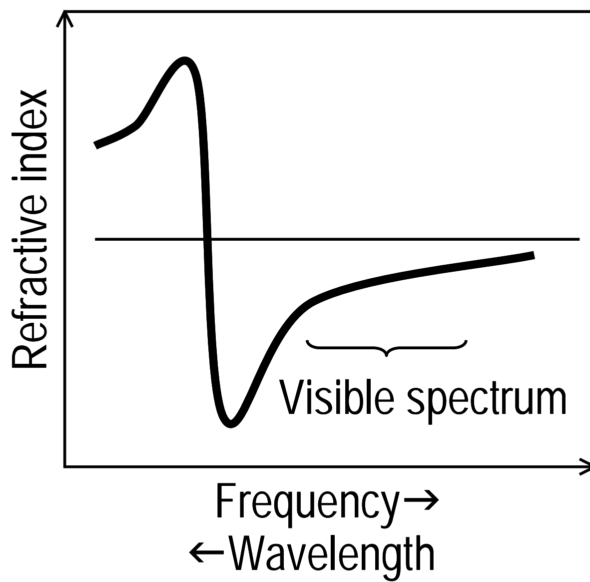

Fig. 2.4. Normal and anomalous dispersion of the refractive index [5].

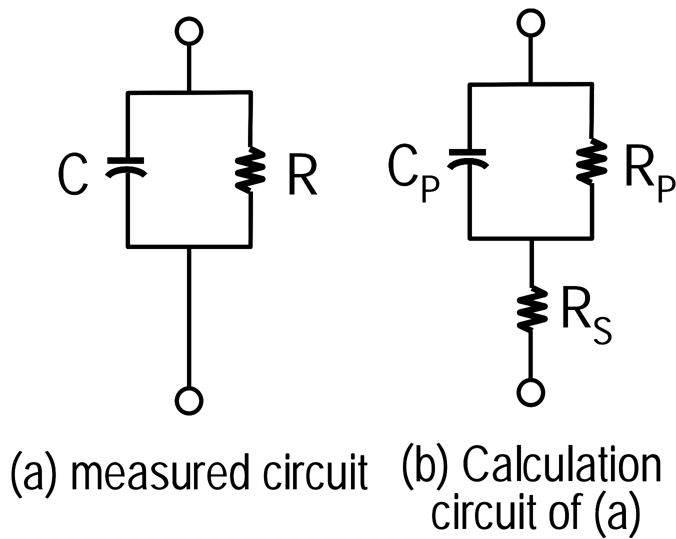

Fig. 2.5. Equivalent impedance model for MOS capacitor.

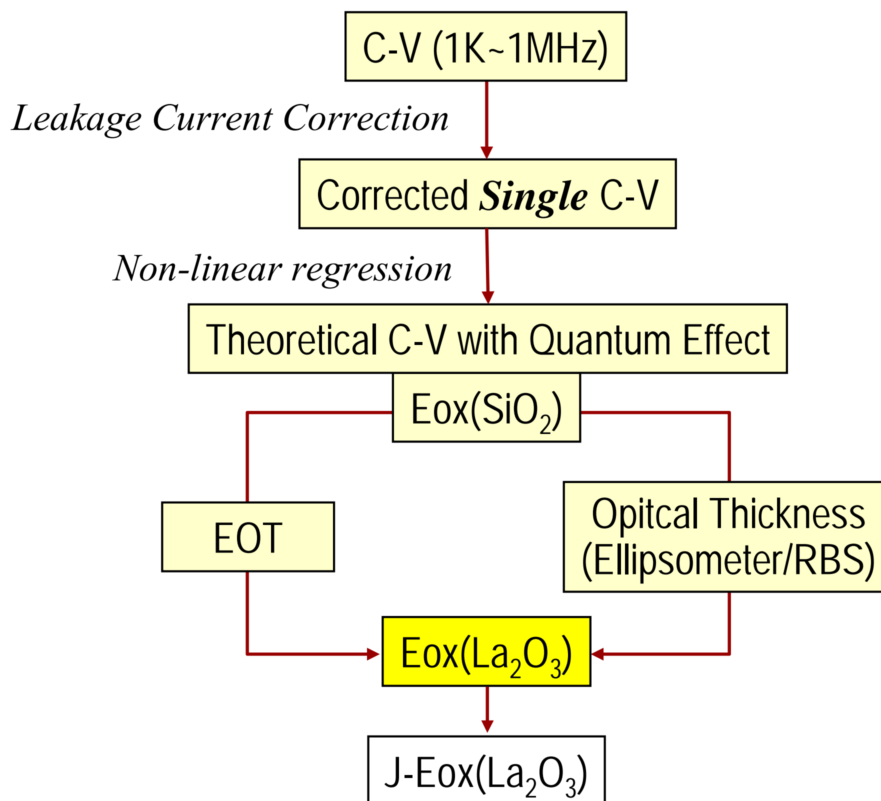

Fig. 2.6. Calculation flow for evaluating oxide field from the measured C-V at multi-frequencies.

Chapter 3. Geometry Effect on Lanthana MOS Capacitor

3.1 Introduction

3.2 Experiment

3.3 Gate leakage current with different gate areas

3.4 Gate leakage current of open and confined structures

3.5 Conclusion

Reference

3.1 Introduction

Gate leakage current of the MOS capacitor can be originated from the gate perimeter and inside of the gate electrode. Especially in the Lanthana film, the film is reported to be degraded easily by absorbing the water from the air [1]. Also, by evaluating the gate leakage current density, one can distinguish the origin of the gate current from the local defect of the film.

In this chapter, gate leakage currents with different areas and structures have been reported. It will give us a close look at the causes for the gate leakage currents.

3.2 Experiment

Fabrications steps fro silicon wafer cleaning, Lanthana film deposition, PDA, top-/bottom-gate electrode depositions, and measurements are same as described in chapter 2. To evaluate the area and perimeter dependence of the gate current, four different areas of the gate dot were used, which are shown in Fig. 3.1. All the gate dots shown in Fig. 3.1 have the exposed area along the gate perimeter. Although the measurement of the gate leakage current is completed within a week and the sample is kept in the vacuumed desiccators, it is worth to compare the leakage current of a completely sealed structure of the Lanthana film by surrounded LOCOS and deposited gate metal, as depicted in Fig. 3.2(b).

3.3 Gate leakage current with different gate areas

Figure 3-3 shows gate leakage current as a function of the square of gate dot radius and gate dot radius. As shown in Fig. 3.3(a), the gate current is proportional to the square of the gate dot radius, i.e., the gate area, while the current is not proportional to the gate dot radius. This indicates that the gate current is principally dominated by the inside of the gate dot, not by the gate edge. This also implies that the gate current is neither due to local oxide thinning, nor to surface roughness, because, in theses cases, the current is closely related to the area of the local current path. Since the gate leakage current is proportional to the gate area, the current can be ascribed to some intrinsic property of the Lanthana film. Now, the gate current is mainly associated with the inside of the gate electrode, so one can evaluate the area and perimeter component of the gate current by using following simple equation:

$$I = P \cdot 2\pi(r) + A \cdot \pi(r)^2 \quad \text{(Eq. 3.1)}$$

Here, I corresponds to the gate current. P and A are the constant describing the correlation to perimeter and area, respectively. r is the radius of the gate electrode. With Eq. 3-1, one can fit the gate current as a function of the gate dot radius to the experiment depicted in Fig. 3.1. Then, area and perimeter component of the gat current is easily obtained as shown in Fig. 3.4. Area component of the gate current is two order higher than the perimeter component.

3.4 Gate leakage current of open and confined structures

Figure 3-5 shows gate leakage currents of open and confined structure MOS capacitors. Although the gate oxide thickness is different, one can see that the gate currents for two structures of the MOS capacitor with gate voltage is quite similar each other. This implies that the gate leakage current is mainly caused by the inside of the gate electrode, for both open and confined structure types of the MOS capacitor. This is in consistent with the conclusion from the area dependence of the gate current as discussed in the previous section.

3.5 Conclusion

Area and structure dependences of the gate leakage current of the Lanthana MOS capacitor have been introduced. From the linear relationship between the gate electrode are and the gate leakage current, it has been found that the current is mainly associated with the inside of the gate electrode, not with the gate edge, and the current is spatially uniform over the gate electrode.

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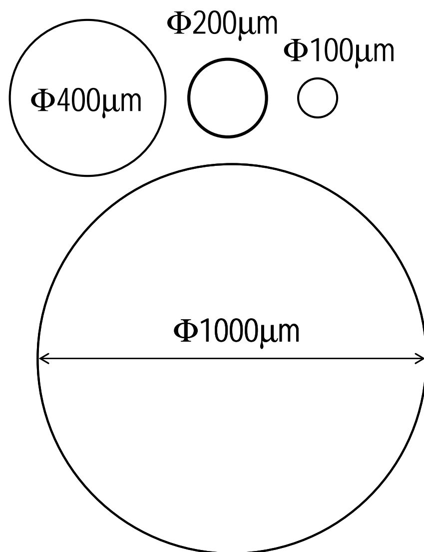

Fig. 3.1. Various gate electrode areas of gate dot

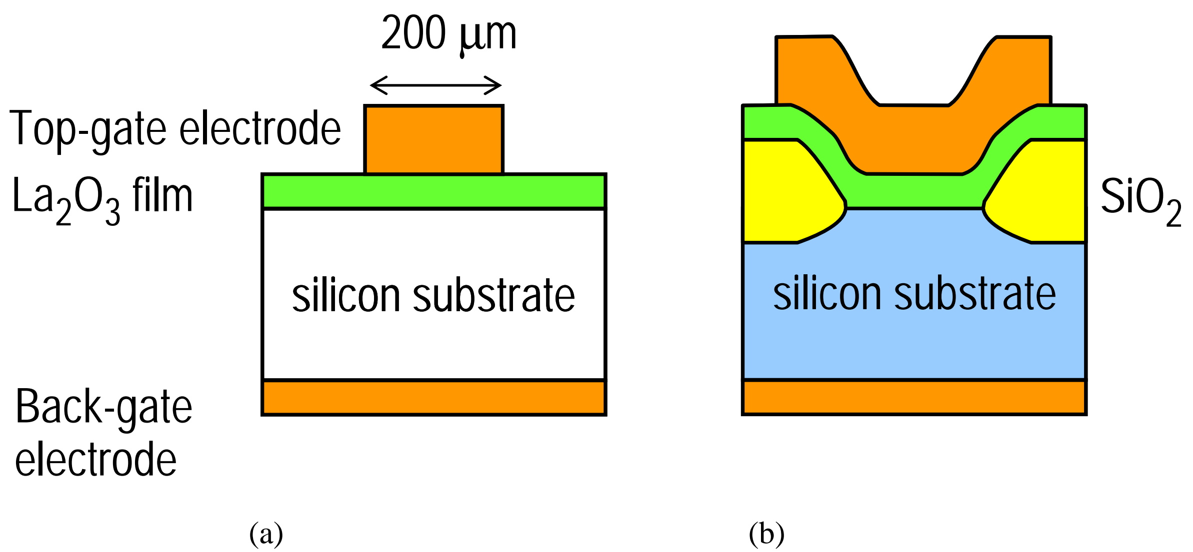

Fig. 3.2. Open (a) and confined (b) structures of MOS capacitor. Open structure has an exposed area to the air along the edge of the gate dot. Confined structure is the MOS capacitor structure whose gate oxide is completely sealed with LOCOS and gate electrode.

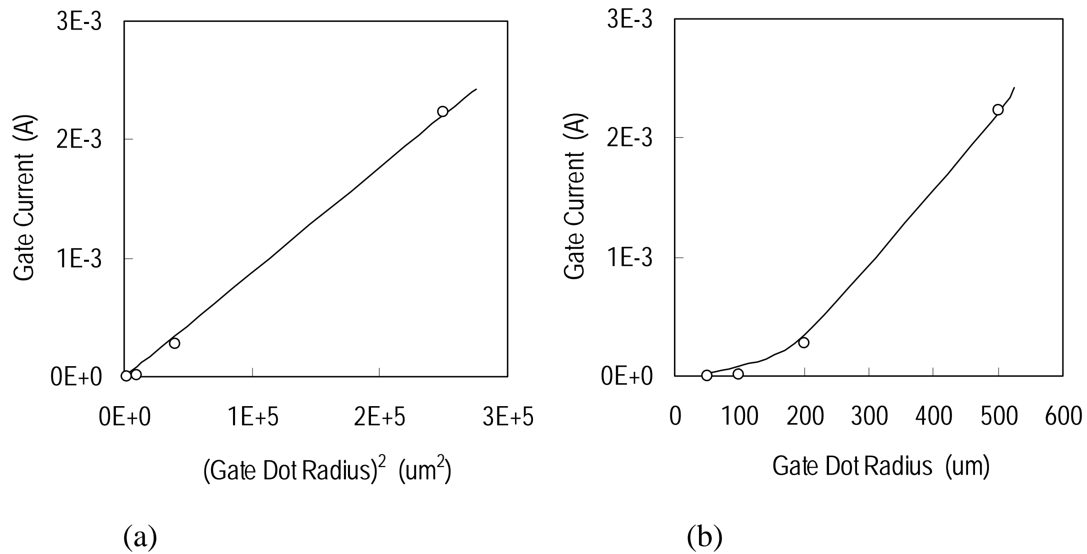

Fig. 3.3. Gate leakage current as a function of (a) the square of gate dot radius, (b) gate dot radius.

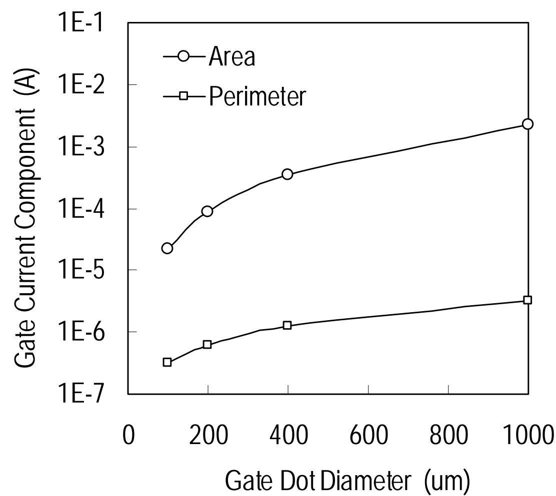

Fig. 3.4. Area and perimeter component of gate leakage current as a function of gate electrode diameter

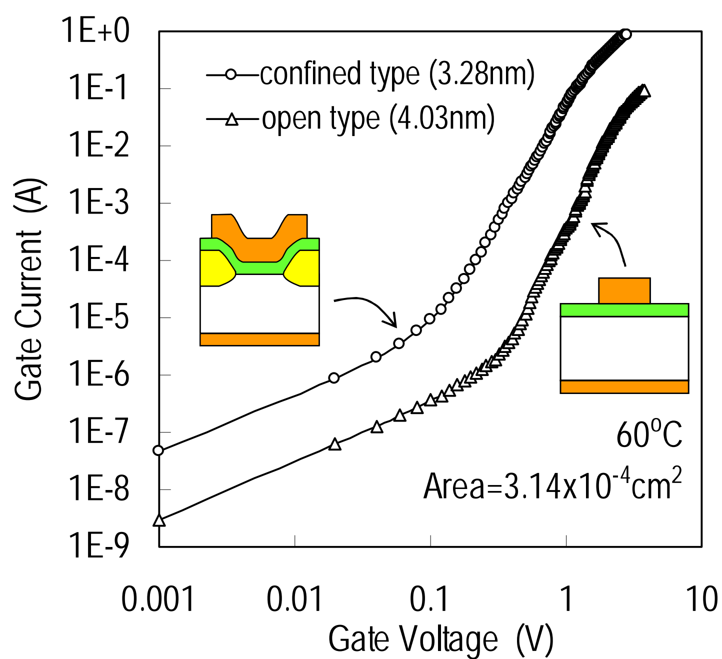

Fig. 3.5. Gate leakage currents of open and confined structures.

Chapter 4. Vacuum PDA Effect on Lanthana MOS Capacitor[a]

4.1 Introduction

4.2 Experiment

4.3 Spectroscopic ellipsometry results

4.4 Flat-band voltage (V_{FB}) characteristic

4.5 Gate electrode material dependence

4.6 Vacuum PDA temperature dependence

4.7 Scaling law based on SCLC theory

4.8 Conclusion

Reference

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[a] This chapter is based on the published paper: Yongshik Kim, Kunihiro Miyauchi, Shun-ichiro Ohmi, Kazuo Tsutsui, and Hiroshi Iwai, "Electrical Properties of Vacuum Annealed La_2O_3 Thin Films grown by E-Beam Evaporation," Microelectronics Journal, 36(1), pp 41-49 (2005).

4.1 Introduction

High-k dielectrics have been studied extensively as an alternative to silicon dioxide in the next generation of MOSFETs [1]. HfO_2, ZrO_2, and Al_2O_3 have attracted much attention because of high dielectric constant, high thermal stability, and high energy barriers at the interface in Si. On the other hand, rare earth oxides (REO), especially Lanthana (La_2O_3) and Y_2O_3, are expected to be applied for the gate oxide thickness of less than 1 nm [2]. In fact, there have been several reports that Lanthana has superior electrical properties [3,4,5]. However, similar to other high-k oxides, Lanthana have larger densities of charge traps than those of SiO_2, causing more significant trap-related conductions.

Large number of positive fixed charge for electron traps have been found in various deposited oxide films [6], also in Lanthana [7]. In the application of high-k gate oxide, operation voltage will be less than 1 V [2], which is comparable to V_{FB} due to fixed charge. This indicates that current conduction can be affected by the value of V_{FB}. Thus, it is important to understand mechanism of leakage current with taking account of flat-band voltage (V_{FB}).

In order to minimize flat-band voltage shift (ΔV_{FB}) of oxide films, post-deposition anneal (PDA) is frequently used, which leads to densification [8,9,10], and decrease in leakage current [11,12], density of states of the band gap [13], and charge trapping [14,15,16]. However, during PDA, an interfacial layer is easy to be formed at between the high-k oxide film and Si substrate in general, resulting in EOT (Equivalent Oxide

Thickness) increment.

To suppress the interfacial layer growth, *in-situ* vacuum PDA of the Lanthana films was proposed [17]. However, vacuum PDA could trigger oxygen loss in Lanthana film via oxygen vaporization and La reduction of Lanthana-layer [18]. It has been also reported that ultra-high vacuum annealing increases the trap density of oxide film due to oxygen deficiency and then enhances the leakage current density as for the case of thermal SiO_2 [19,20]. In the contrary, decrease in the leakage current with high oxide trap density has been reported [21,22], which can be explained well according to SCLC (Space-Charge-Limited Current) theory. This behavior of SCLC theory is an interesting contrast to other trap-related conductions such as Poole [23], P-F (Poole-Frenkel) [24], TAT (Trap-Assisted Tunneling) [25], Junction- like [26], and VRH (Variable Range Hopping) [27].

SCLC model has been developed and used continuously over four decades. Until recently, numerous attempts have been reported to interpret the current behavior of thin films within the frame of SCLC. Such films were deposited (not-thermally grown) SiO_2 [21,28], defective SiO_2 [22], TiO_2 [29], organic materials [30], porous silicon [31,32], nitride [33], SiO_2/nitride [34], $SrTiO_3$ [35], Ta_2O_5 [36,37], and REO [38].

As stated above, higher trap density leads to lower leakage current density if the conduction is associated with SCLC. This is because high trap density retards the movement of quasi-Fermi level in the band gap of the insulator, according to the carrier injection. If an electron is injected to a trap-free insulator, electrons will travel into the conduction band of the insulator and form a space-charge analogous to that of a vacuum

diode [39]. In this case, electron concentration in the conduction band is characterized by the quasi-Fermi level of the insulator. When the insulator has large trap sites at concentrated energy levels in the energy band gap, some of injected electrons are captured and then the position of the quasi-Fermi level remains practically constant at the concentrated energy levels until all the traps at each levels are filled. This is because, at steady-state injection, quasi-Fermi level of the insulator is determined by trap density, trap levels, and trapped carriers [40]. As a result, the nearly constant quasi-Fermi level holds the carrier concentration unchanged and in turn the leakage current density, despite increasing the carrier injection as increasing applied voltage, unless all the localized trap levels are filled. In SCLC model, shallow and deep trap levels are defined by the quasi-Fermi level [39]. When trap level is above the quasi-Fermi level, trap levels are called shallow, and when below, the trap levels are called deep. Moreover, this definition depends on the carrier injection level. As the injection increases, the quasi-Fermi level moves up and a shallow level becomes deep loosing effectiveness in reducing the current. These two types of SCLC are important when charge build-up occurs at the vicinity of cathode. Thus, SCLC conduction is affected by a distribution of trap energy levels as well as an amount of those. From SCLC theory, trap density distribution in the oxide band gap is generally described by one of the following ways: 1) discrete level [41], 2) exponential distribution [42], 3) Gaussian distribution [43], and 4) uniform distribution [40]. Diffused Gaussian trap density distribution, discrete trap level with tails, or pseudo-uniform distribution can be described by the exponential distribution [44]. Thus, since the trap density distribution is often spread out in nature, current-voltage relation of exponential distribution can be useful as first evaluation method. Exponentially distributed traps are characterized by two parameters, namely trap density N_t and a characteristic constant of the distribution

T_c, through the expression [40],

$$N(E) = \frac{N_t}{kT_c} \exp\left(\frac{E - E_c}{kT_c} \right) \qquad \text{(Eq.4.1)}$$

where N(E) is the trap concentration per unit energy range at an energy E below the conduction band edge, k Boltzman's constant, E the energy, and E_c energy level of conduction band edge. Eq. (4-1) is valid when $E<E_c$. N_t/kT_c is the trap density per unit energy range at the conduction band edge. Integrating Eq. (4-1) from the conduction band edge to infinity, 63% of traps lie within kT_c from the conduction band edge [45]

In this chapter, reported are the results of spectroscopic ellipsometry and C-V measurements, and explain detailed analysis in the conduction mechanism of E-beam evaporated Lanthana films with ultra-high vacuum annealing.

In this article, the conduction mechanisms of metal-oxide-semiconductor with vacuum annealed Lanthana (La_2O_3) oxide film are investigated. Lanthana films with thicknesses of 3.5, 4.7, and 11 nm were deposited by E-beam evaporation on n-Si (100), and annealed at various temperatures (300-500°C) in ultra-high vacuum (10^{-10}-10^{-9} Torr) for 90 min. From the measurement of spectroscopic ellipsometry, it is found that film thickness is increased with annealing temperature, which would be cause of flat-band voltage shift (ΔV_{FB}) due to the growth of interfacial layer. From the capacitance measurement, it is found that ΔV_{FB} of the film is reduced by post-deposition anneal (PDA) compared to that of as-deposited film, but increase again at high temperature annealing, especially in the case of thin film (3.5 nm). From the applied voltage and

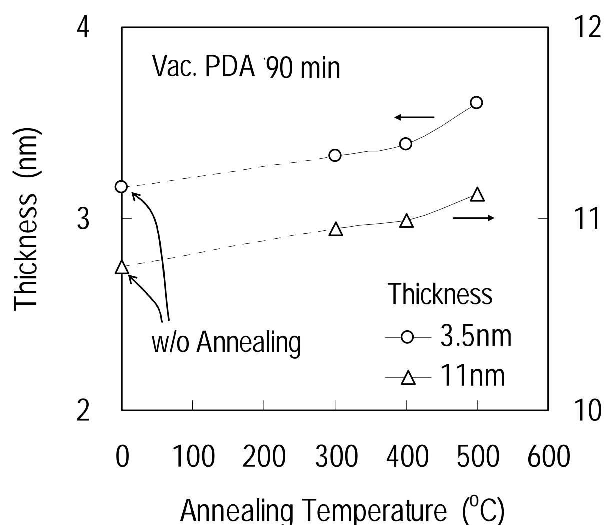
temperature dependence of the leakage current of the film, with different gate electrode materials (Ag, Al, and Pt), it is shown that the leakage currents are associated with ohmic and P-F (Poole-Frenkel) conductions when flat-band voltage (V_{FB}) is less than zero, and ohmic and SCLC (Space-Charge-Limited Current) conductions when V_{FB} is greater than zero. The dielectric constants obtained from P-F conduction for Al gate electrode case is found to be 11.6, which is consistent with the C-V result 11.9. Barrier height of trap potential well is found to be 0.24 eV from P-F conduction. Based on SCLC theory, leakage currents of 3.5 and 11 nm films with different PDA temperatures are explained in terms of oxide trap density.

4.2 Experiment

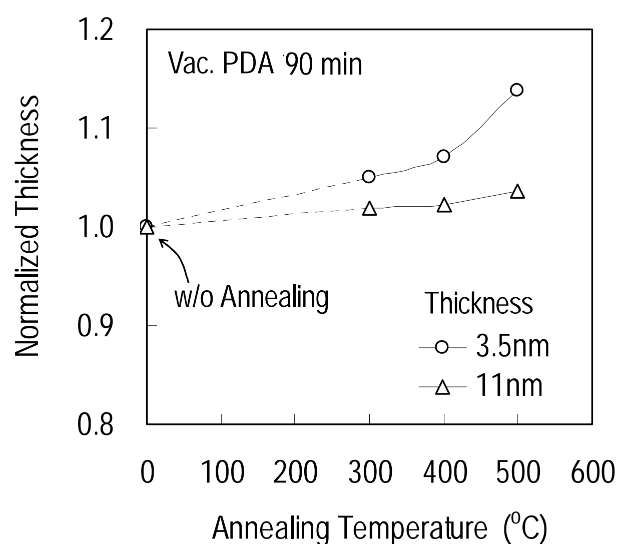
Lanthana thin films were deposited on HF dipped n-Si (100) substrate (HF-last) by E-beam evaporation at 250°C using MBE equipment. The pressure in the chamber before and during depositions was about 10^{-9} Torr. Then, wafers were annealed in the chamber with vacuum pressure of 10^{-10}-10^{-9} Torr. Annealing was carried out *in-situ* or *ex-situ* for 90 min at 300, 400, 500°C. In order to investigate different V_{FB} effect on leakage current, Al, Ag, or Pt electrode was formed by metal evaporation with a metal shadow mask using bell-jar type evaporator at 10^{-5} Torr. An exposure time to the air before gate metal deposition was kept less than 1 hour. Capacitance versus applied voltage (C-V) and leakage current density versus applied voltage (J-V) measurements were performed using a HP4284A multi-frequency LCR meter and a HP4156C Semiconductor Parameter Analyzer. The ramp-up speed of gate voltage in J-V test was about 0.1 V/s to achieve steady-state of the oxide leakage current to probe trapping

effects since occupied trap level with electron have a release time depending on trap level [40]. The film thickness was confirmed by Otsuka FE-5000 ellipsometer.

C-V of Lanthana film was measured with various frequencies (1K~1MHz). To remove the frequency dispersion on C-V caused by leakage current of oxide, we used two-frequency model to achieve single corrected C-V [46,47]. By using of nonlinear regression method [48], the corrected C-V was compared to the calculated C-V, and then oxide field was obtained. EOT (Equivalent Oxide Thickness) was calculated from the corrected C-V with taking quantum effect into account. From EOT and physical thickness, oxide field in Lanthana film was calculated. This theoretical oxide field was used to check conduction mechanisms for leakage current density.



(a) physical film thickness, T_{phy}



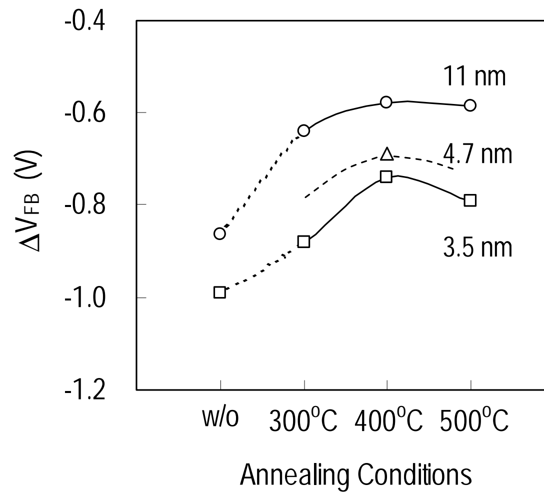
(b) normalized film thickness (=T_{phy} (PDA)/T_{phy}(non-PDA))

Fig. 4.1. Physical thickness variation of films as a function of *ex-situ* vacuum annealing temperature, compared to that without annealing. (a) corresponds to the thickness measured by spectroscopic ellipsometry and (b) corresponds to normalized film thickness for comparison. Normalization was carried out with respect to the physical thickness of the film without PDA. Film thickness of zero annealing temperature corresponds to that without vacuum anneal.

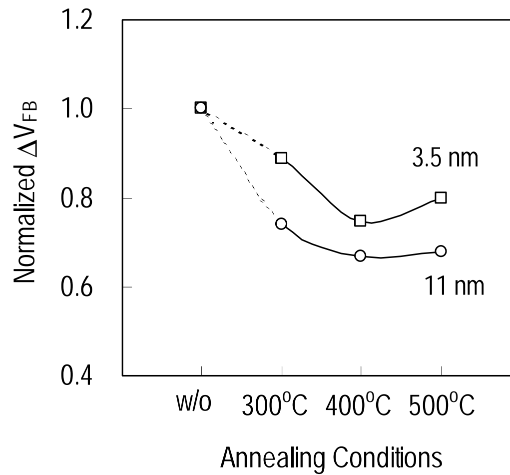
4.3 Spectroscopic ellipsometry results

Fig. 4.1 shows physical thickness variation measured by ellipsometry with ultra-high vacuum PDA conditions. Increase in PDA temperature led to increase in the film thickness by the same amount at both 3.5 and 11 nm films, as shown in Fig. 4.1(a). This means that relative increase in the case of thin film (3.5 nm) is more severe than the thick film case, as shown in Fig. 4.1(b). It is believed that the increase in film thickness as increase in PDA temperature is due to the growth of the interfacial layer between the Lanthana film and the silicon substrate, although vacuum PDA is effective to suppress the growth. It is worth noting that the growth of interfacial layer in Lanthana film with nitrogen PDA, which is also known to be effective to minimize the interfacial layer, was observed and the layer was reported as La-silicate [18,49]. In addition, under oxygen PDA, the interfacial layer of Lanthana was found to be as La-silicate [50,51]. This indicates that part of oxygen in Lanthana is consumed to form the silicate interfacial layer [18]. As a result, Lanthana film becomes oxygen-deficient especially near/at the interfacial layer and has a negative V_{FB}, since oxygen deficiency in the oxide film results in negative ΔV_{FB} [52,53,54]. This phenomenon of La reduction process can be expected in the case of vacuum PDA because oxygen is rarely supported to the interfacial layer growth of the film, similar to the nitrogen PDA case. Since an amount of oxide charges caused by oxygen-deficiency near/at the interfacial layer is thought to be nearly same for both thin and thick films, ΔV_{FB} of the thick film is expected to be more negative than that of the thin film. This is because ΔV_{FB} is proportional to the amount of charge and the distance between the fixed charge and the gate electrode [55]. However, the

experimental results from C-V characteristic are contrary to this expectation. It is clear that the positive charge from the interfacial layer growth makes ΔV_{FB} negative, however, which is not enough to explain the fact that $|\Delta V_{FB}|$ of the thin film is greater than that of the thick film, under the assumption that oxide charges due to the interfacial layer growth are same for both thin and thick films. This point will be further discussed in the section of V_{FB} characteristic.



(a) ΔV_{FB}



(b) normalized ΔV_{FB} (=ΔV_{FB}(PDA)/ΔV_{FB}(non-PDA))

Fig. 4.2. Variation in flat-band voltage shift ΔV_{FB} (a) and normalized ΔV_{FB} (b) with different film thicknesses as a function of vacuum anneal temperature for 90 min. Normalization was carried out with respect to ΔV_{FB} of the film without PDA. Gate electrode for 3.5 and 11 nm films was Pt. Gate electrode for 4.7 nm film was Ag. Vacuum PDA was carried out *ex-situ* for 3.5 and 11 nm films and *in-situ* for 4.7 nm film.

4.4 Flat-band voltage (V_{FB}) characteristic

Vacuum PDA effect on the oxide film is three-fold: interfacial layer growth due to high temperature, film densification due to high temperature, and oxygen vaporization due to ultra-low pressure. The first is discussed in the section of spectroscopic ellipsometry characteristic. The interfacial layer growth causes negative ΔV_{FB} of the film. The second is related with the atomic rearrangement into its equilibrium position with the help of thermal activation, which results in decrease of $|\Delta V_{FB}|$. The third is the thermodynamic process to hold equilibrium vapor pressure, easy to occur at the film surface. Several studies have been made on this oxygen vaporization effect for the case of thermally-grown SiO_2 [19,56], laser-deposited Y_2O_3 [16], and Lanthana deposited by evaporation [18]. Equilibrium partial pressure of oxygen between atmosphere and Lanthana film increases with annealing temperature [57], so that ΔV_{FB} increases in the negative direction with increase in PDA temperature. These three effects, which are the interfacial layer growth, the film densification, and the vaporization effects, cause a different behavior of ΔV_{FB} depending on the film thickness and the PDA temperature, as shown in Fig. 4.2.

ΔV_{FB} of Lanthana films with 3.5, 4.7, and 11 nm for different PDA conditions is shown in Fig. 4.2. ΔV_{FB} of all the conditions were negative, which means the existence of positive oxide charge which is effective for electron trapping.

For the case of non-PDA conditions, as the film thickness increases, $|\Delta V_{FB}|$ decreases, as depicted in Fig. 4.2(a). This could be attributed to the difference in the

deposition time since deposition rate for all the films was kept constant as about 1 nm/min. The more time for deposition is required for the thicker film. This longer time for the thicker film could result in the film densification and the interfacial layer growth, rather than the film vaporization. This could be because vaporization is less effective due to a continuous supply of Lanthana molecules during deposition. As discussed before, if $|\Delta V_{FB}|$ is mainly determined by the fixed charges near/at the interfacial layer, $|\Delta V_{FB}|$ of thick film should be greater than that of thin film. This is opposite to the experimental results. Thus, it could be suggested that the thick film (11 nm) is less defective in terms of long deposition time which also functions as annealing, than the thin film (3.5 nm). This leads to small $|\Delta V_{FB}|$ of 11 nm film compared to that of 3.5 nm film.

For the comparison of vacuum PDA temperature effect, ΔV_{FB} of two different thickness films (3.5 and 11 nm films) is normalized with respect to that of the non-PDA, which is shown in Fig. 4.2(b). For the case of 300°C and 400°C PDAs, normalized ΔV_{FB} is minimized compared to that without PDA, especially more for 400°C PDA temperature. The amount of change in normalized ΔV_{FB} by PDA for thin film (3.5 nm) is less than that for thick film (11 nm). This indicates that densification by PDA occurs throughout the film and near the interface between the Lanthana film and the substrate, since reduction of fixed oxide charges near the gate electrode has less effect on ΔV_{FB}. This also explains that $|\Delta V_{FB}|$ of the thicker film becomes smaller than that of the thinner film for the case of 400°C PDA as shown in Fig. 4.2(a). For the case of 500°C PDA case, normalized ΔV_{FB} of the thin film (3.5 nm) was slightly increased again, while that of the thick film (11 nm) remained constant. For the same temperature and duration time of PDA, an amount of the film densification and the

interfacial layer growth is thought to be almost same for the both films. However, since the oxygen vaporization is expected to first occur at the exposed surface of the film and then spreads throughout the film, positive charges caused by oxygen vaporization could exist over a limited depth from the surface for the thick film case, while could exist throughout the film for the thin film case. This indicates that the oxygen vaporization of the thin film case is greater than that of the thick film case because the vaporization is expected to occur more uniformly and within a shallower depth in the case of thin film than in the case of thick film. As a result, in the thin film case, the more oxygen vaporization results in the more positive charges than in the thick film case. This explains well the experimental results of 500°C PDA that $|\Delta V_{FB}|$ and normalized ΔV_{FB} of the thick film (11 nm) are less than those of the thin film (3.5 nm) as shown in Figs. 4-2(a) and 4-2(b), respectively.

Therefore, it is reasonable to consider that positive charges for electron-trapping exist less and non-uniformly at both ends of the thick film, and exist more and relatively uniformly throughout the thin film, with higher vacuum PDA temperature. This point will be confirmed again by the analysis of the conduction mechanisms.

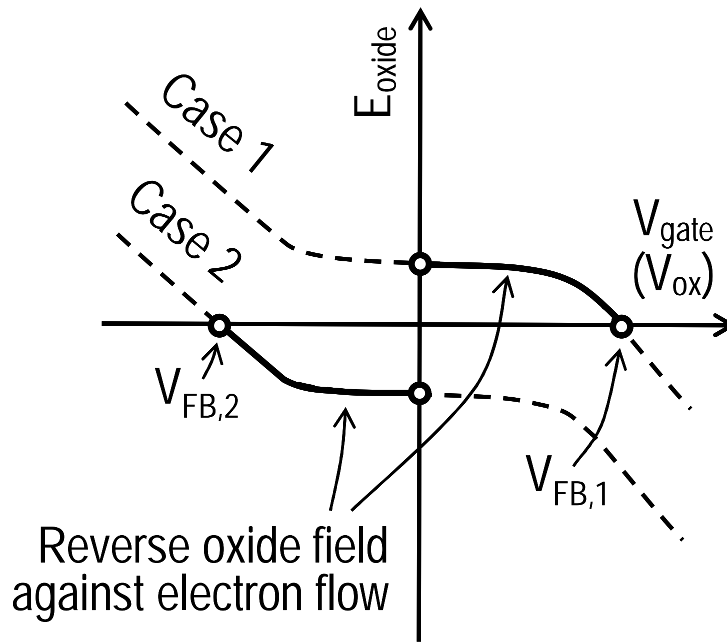


Fig. 4.3. Typical relations between gate voltage, equivalent to metal-silicon Fermi level difference, versus oxide field: $V_{FB}>0$ at case 1 and $V_{FB}<0$ at case 2. Horizontal and vertical axes are in arbitrary scale. Solid lines represent reverse oxide field region against electron flow. Broken lines represent relation between oxide field and gate voltage.

4.5 Gate electrode material dependence

As the MOSFET is scaled down, operation voltage becomes comparable to the V_{FB} caused by the work function difference between the gate electrode and silicon substrate, and the fixed charge in the oxide film. A positive or negative V_{FB} leads to change in the oxide conduction band slope. In order to investigate the effect of oxide conduction band slope on the leakage current, we compared oxide leakage currents between two different gate electrode materials: Al and Ag. Two general cases of relation between oxide field and gate voltage applied to oxide film when V_{FB} is non-zero are shown in Fig. 4.3. Case 1 is when $V_{FB}<0$ and Case 2 is when $V_{FB}>0$.

When gate voltage is between 0V and V_{FB}, oxide field is opposite to the carrier flow direction determined by the gate voltage. In this reverse oxide field region, the oxide field is practically constant and becomes less effective than when gate voltage is less than 0 V or greater than V_{FB}. This implies that leakage current is rarely correlated with conduction band slope of the oxide. This suggests that trapped charges can be released mostly due to thermal activation not by field-assisted emission, and the conduction band slope is susceptible to the trapped charges. The reverse oxide field region is significant especially in the case of high-k films, since higher dielectric constant leads to smaller oxide field and high-k films generally have large non-zero V_{FB}.

Fig. 4.4 shows the leakage current versus the gate voltage for the case of Al electrode. V_{FB} is found to be less than zero, corresponding to case 2 shown in Fig. 4.3. Ohmic conduction matches well in low gate voltage region: $-0.7<V_g<0.2$ V. P-F conduction corresponds to gate voltage greater than 0.2 V. This P-F conduction occurred at the oxide electric field above -1.65 MV/cm even while gate voltage was still low. P-F conduction at high electric field region is reasonable, since high electric field in the same direction with carrier flow could sweep away the trapped carriers almost immediately so that carriers at traps exist in a short time and then distortion in energy band diagram of oxide becomes negligible. In the inversion region ($V_g<V_{FB}$), silicon surface is subjected to generate minority carrier to support leakage current. This generation is limited by the temperature and light, which leads to the saturation in the current density [58]. This explains the saturation in leakage current for the negative gate voltage region in Fig. 4.4.

Fig. 4.5 shows P-F plot. The calculation results were well fitted to the

experimental results. Relative dielectric constant value of 11.9 was obtained at three different temperatures, which is in good agreement with the value of 11.6, which was obtained from the C-V curve. In Fig. 4.6, intercepts of y-axis in Fig. 4.5 are plotted as a function of inverse temperature. Trap barrier height of coulombic center was found to be 0.24 eV, which is similar to other high-k oxides showing P-F conduction, such as Eu_2O_3 [59] and Ta_2O_5 [60].

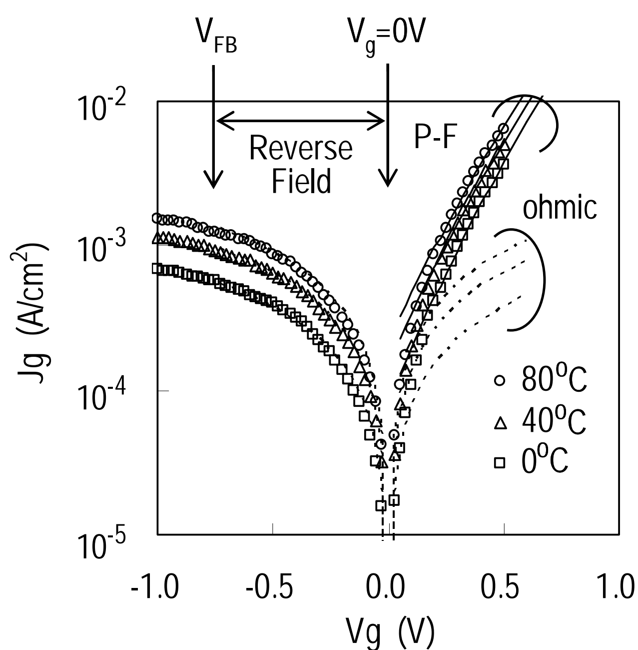


Fig. 4.4. Leakage current density for films of Al gate electrode case as a function of the gate voltage. Symbols correspond to experimental results. Solid and dotted lines correspond to the best fits to experimental results obeying P-F and ohmic conductions, respectively. The films were annealed *in-situ* vacuum PDA. Relative dielectric constant was 11.9. EOT (Equivalent OXide Thickness), with a consideration of quantum effect, and physical thickness measured by spectroscopic ellipsometry were 1.54 and 4.7 nm, respectively. Reverse field means reverse oxide field against carrier flow direction.

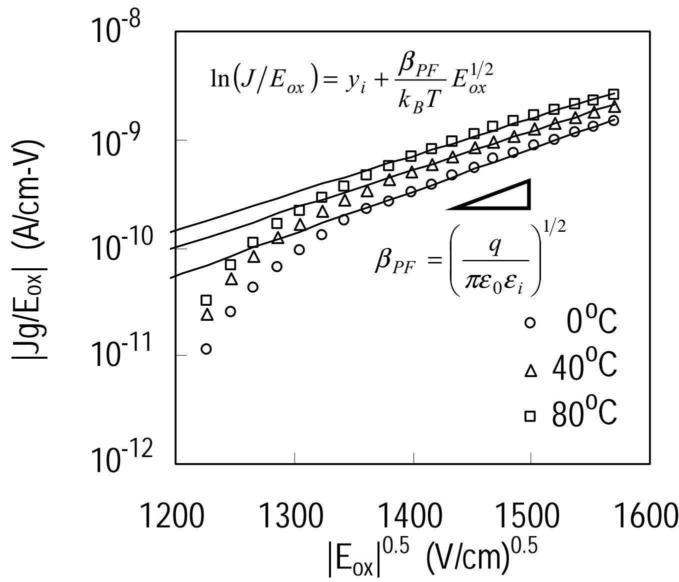


Fig. 4.5. P-F plot for Al gate electrode case: $\log(J_g/E_{ox})$ versus square root of oxide field E_{ox}. Symbols correspond to experimental results: 0°C(circle), 40°C(triangle), and 80°C(square). Solid lines correspond to the best fits to experimental results following P-F model with permittivity of 11.6. Inserted equations express the solid lines, where k_B is Boltzman constant, and T, q, and ε_0, and ε_i correspond to those of Eq. (4-2).

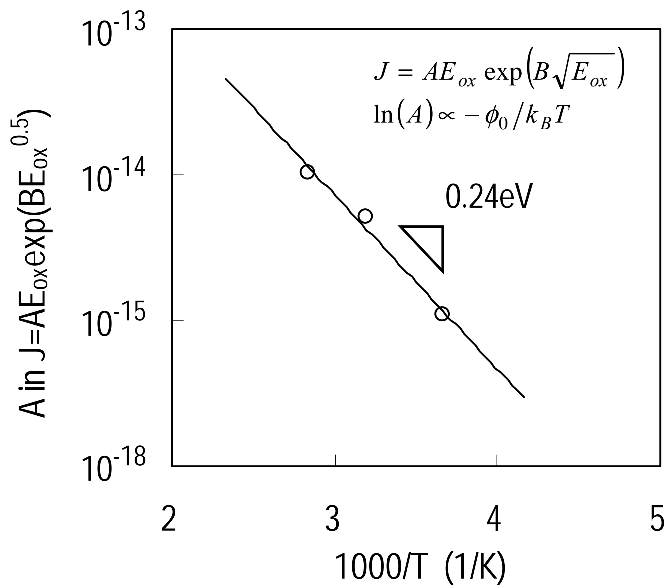


Fig. 4.6. Trap barrier height in P-F conduction for the Al gate electrode case. A of vertical axis, are the y-axis intercepts of the P-F plot shown in Fig. 4.5. Circle corresponds to the intercepts. Solid line correspond to a linear fit. Inserted equations were used to obtain the barrier height ϕ_0.

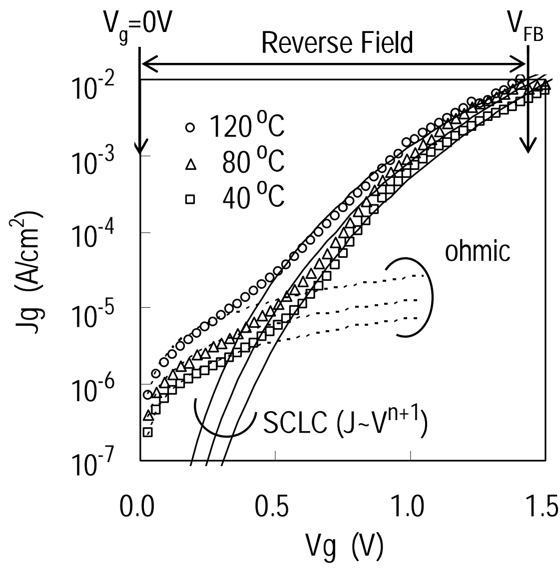


Fig. 4.7. Leakage current density for films of Ag gate electrode case as a function of the gate voltage. Values of n were found to be 4.7, 5.5, and 6.2 for 120, 80, and 40°C films, respectively. Symbols correspond to experimental results. Solid and dotted lines correspond to the best fits to experimental results obeying SCLC with exponential trap distribution and ohmic conductions, respectively. The films were annealed *in-situ* vacuum PDA. Relative dielectric constant, EOT and physical thickness are equal to those of Al electrode case. Reverse field means reverse oxide field contrary to carrier flow direction.

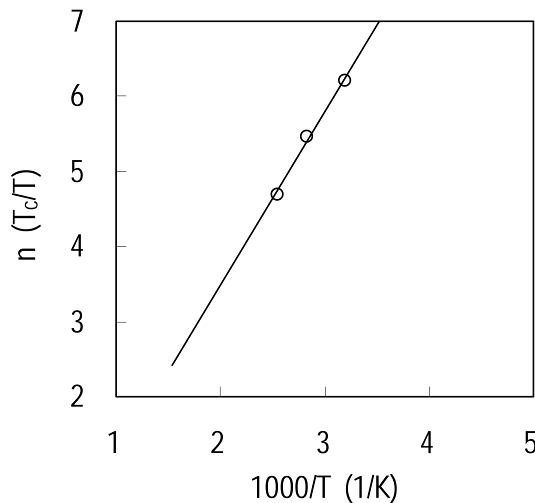


Fig. 4.8. The temperature dependence of the exponent n as a function of 1000/T with T as the operation temperature. The J-V characteristics of Fig. 4.7 were fitted by $J \sim V^{n+1}$. Circle correspond to the exponent n. Solid line represents a linear fit between n and 1/T.

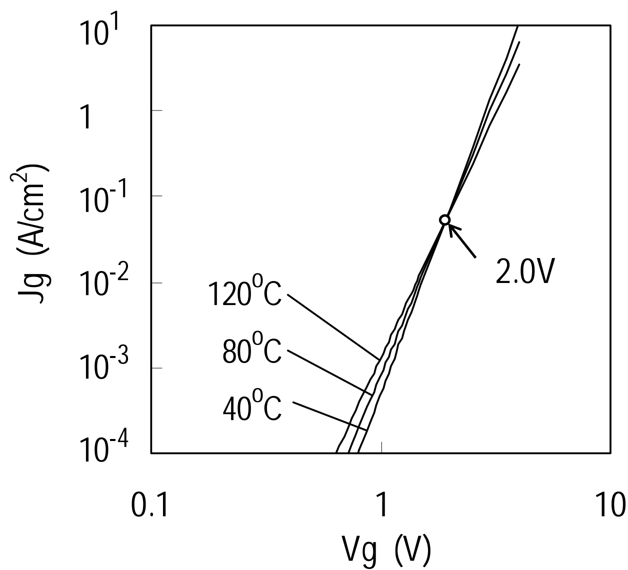


Fig. 4.9. SCLC currents with exponential trap distribution obtained from the fitting to the experimental results as depicted in Fig. 4.7. Lines cross at the common intersection point, marked with circle, suggested by Sussman [63]. At the point current is independent of temperature.

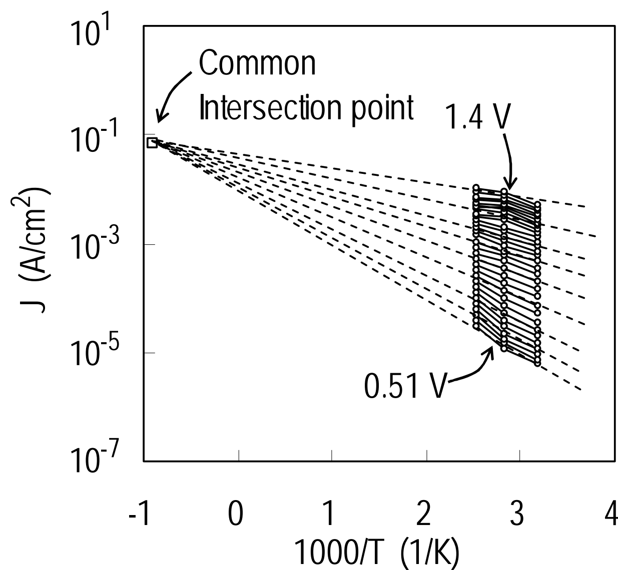


Fig. 4.10. Leakage currents for the Ag gate electrode case as a function of 1000/T with different applied voltages. Circles are experimental results and dotted lines are extrapolation of the results. Leakage currents are plotted in the voltage range from 0.51 to 1.4 V with 30 mV step. Dotted lines cross at the common intersection point suggested by Gould [62]. At the point, the current is independent of voltage. Coordinates of the point are T=-1111 K and J=0.07 A/cm^2.

Fig. 4.7 shows the leakage current versus the gate voltage for the case of Ag electrode. V_{FB} is found to be greater than zero, corresponding to case 1 shown in Fig. 4.3. In the low gate voltage region, ohmic conduction is predominant. when gate voltage is between 0.5 and 1.4 V, SCLC with exponential trap distribution becomes important. These conductions could be expected from the consideration of V_{FB} effect on the leakage current, since the leakage current is mostly in the reverse oxide field region. The current density J with exponential trap distribution case of SCLC is given by [40],

$$J = \frac{q\mu N_c V}{L}\frac{f(n)}{2^n}\cdot\left(\frac{2\varepsilon V}{qL^2 N_t}\right)^{T_c/T}, \qquad \text{(Eq.4.2)}$$

$$f(n) = \left(\frac{n}{1+n}\right)^n \left(\frac{2n+1}{1+n}\right)^{n+1}, \qquad \text{(Eq.4.3)}$$

$$n = T_c/T, \qquad \text{(Eq.4.4)}$$

where q is electronic charge, μ carrier mobility, N_c density of states of conduction band, V applied voltage, L film thickness, ε film dielectric constant ($\varepsilon=\varepsilon_0\varepsilon_\iota$: ε_0 is vacuum permittivity and ε_ι is relative dielectric constant), N_t trap density, T_c characteristic temperature, and T operation temperature. T_c and N_t correspond to those of Eq. (4-1). After Kumar [61], $f(n)/2^n$ is found to be about 0.5, which is nearly unrelated to temperature when n>2. By taking logarithmic form of Eq. (4-2), we can separate temperature sensitive and insensitive terms as follows:

$$\log_{10}(J) = \log_{10}\left(\frac{q\mu N_c V}{L}\frac{f(n)}{2^n}\right) + \log_{10}\left(\frac{2\varepsilon V}{qL^2 N_t}\right)\cdot\frac{T_c}{T}. \qquad \text{(Eq.4.5)}$$

The first tem on the right-hand side of Eq. (4-5) is insensitive to temperature but the second term is sensitive. At $T=-T_c$ where $T_c>0$, the current is irrelevant of temperature and is given by,

$$J = \frac{q^2 \mu N_c L N_t}{4\varepsilon} \quad \text{(Eq.4.6)}$$

and

$$V = \frac{qL^2 N_t}{2\varepsilon}. \quad \text{(Eq.4.7)}$$

Eq. (4-6) describes the common intersection point in $\log_{10}(J)$ versus 1/T relation. Eq. (4-6) is similar to that suggested by Gould [62] except constant 4 in the denominator. μN_c term can be obtained by using the first term on the right-hand side of Eq. (4-5) from $\log_{10}(J)$ versus 1/T relation. In addition to the intersection point described by Eq. (4-6), another intersection point can be obtained as follows. At $T_c>2T>0$, by differentiating Eq. (4-5) with 1/T, we can obtain V and J coordinates of the common intersection point in $\log_{10}(J)$ versus 1/T relation as follows:

$$V = \frac{qL^2 N_t}{2\varepsilon} \quad \text{(Eq.4.8)}$$

and

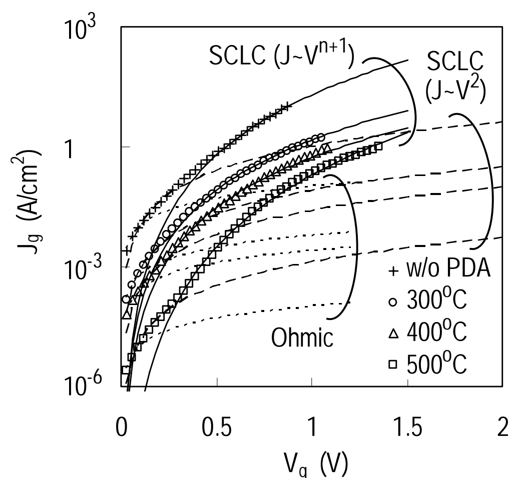
$$J = \frac{q\mu N_c V}{2L}. \quad \text{(Eq.4.9)}$$

Eqs. (4-8) and (4-9) are identical to those suggested by Sussman [63] except constant 2 in the denominator. Eq. (4-7) is same as Eq. (4-8). One can easily find that Eq. (4-9)

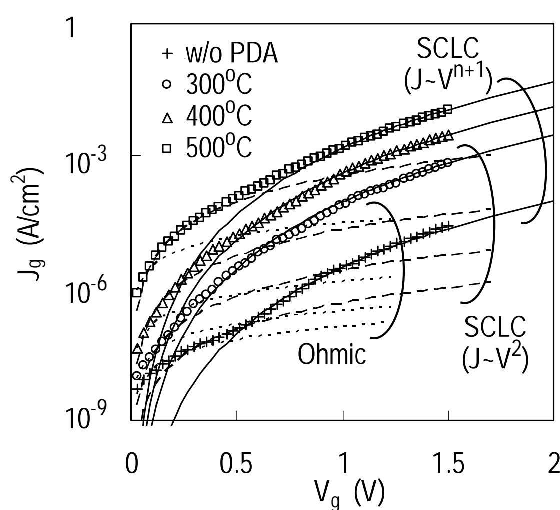
is identical to Eq. (4-6) by inserting Eq. (4-8) into Eq. (4-9).

For the exponential trap distribution case of SCLC, the current density is a function of the n power of voltage and n should be a linear function of inverse temperature, as depicted in Fig. 4.8, confirming that the leakage current at voltages between 0.5 and 1.4 V in Fig. 4.7 is SCLC.

Figs. 4-9 and 4-10 show the common intersection points of $\log_{10}$(J)-1000/T and $\log_{10}$(J)-Vg plots for the leakage current of Ag electrode case shown in Fig. 4.8, respectively. These intersection points are indicative of space-charge-limited flow with an exponential trap distribution [62, 63]. The intersection point shown in Fig. 4.9 is described by Eqs. (4-8) and (4-9). The intersection point shown in Fig. 4.10 is described by Eq. (4-6) when T=-1111 K, i.e., T_c=1111 K. μN_c was found to be $2x10^{11}$/V-s-cm. From the common intersection points in Figs. 4-9 and 4-10, trap density N_t was found to be the same value of $1.2x10^{20}/cm^3$-eV for both cases. This is similar to the oxide trap density obtained from the flicker noise [64].



(a) 3.5 nm



(b) 11nm

Fig. 4.11. Leakage current density of 3.5 nm (a) and 11 nm (b) films of Pt gate electrode case, as a function of the gate voltage. The films were annealed *ex-situ* vacuum PDA. Symbols correspond to experimental results of different PDA temperatures: without-annealing (cross), 300°C (circle), 400°C (triangle), and 500°C (square). Solid, dashed, and dotted lines correspond to the best fits to experimental results obeying SCLC with exponential trap distribution, SCLC with shallow trap, and ohmic conductions, respectively. Exponents n of (a) were 4 for all films. Exponents n of (b) were 4.0, 3.2, 3.2, and 5.0 for w/o, 300°C, 400°C, and 500°C PDAs, respectively.

4.6 Vacuum PDA temperature dependence

Fig. 4.11 shows leakage current densities with film thickness of 3.5 and 11 nm, at three different vacuum PDA temperatures. V_{FB} of the films are described in Fig. 4.2. For the case of 3.5 nm film shown in Fig. 4.11(a), leakage current density increased with increase in PDA temperature, while for the case of 11 nm film shown in Fig. 4.11(b), the current decreased with increase in PDA temperature. Although the leakage currents varied with the applied PDA conditions, predominant conduction mechanisms were found to be almost identical for all the films shown in Fig. 4.11.

At low voltage, ohmic conduction matches well to the currents. At intermediate voltage, the currents are described by square voltage law, which indicates that carrier concentration in conduction band of the oxide film is comparable to trapped carrier concentration. At high voltage, the currents are described by the power law of voltage, corresponding to SCLC with exponential trap distribution.

Since all the currents shown in Fig. 4.11 can be explained by SCLC conduction, the leakage currents are expected to be inversely proportional to oxide trap density N_t from Eq. (4-2), on condition of constant μN_c. As discussed in the section of V_{FB} characteristic, for the thin film (3.5 nm) case, higher vacuum PDA temperature induces more oxide trap density, while for the thick film (11 nm) case, higher vacuum PDA temperature leads less oxide trap density. In view of this, the opposite behavior of the leakage currents with PDA temperatures between the thin and thick films can be explained: higher PDA temperature results in smaller leakage currents for the thin film

(3.5 nm) and greater leakage currents for the thick film (11 nm).

4.7 Scaling law based on SCLC theory♠

Figure 4-12 shows normalized leakage current versus normalized voltage. According to SCLC theory [65], from all expressions for J-V characteristics, the general scaling rule for one-carrier SCLC conduction in any materials with any trap distributions can be expressed in terms of

$$J/L_{eff} \sim \left(V/L_{eff}^{2}\right)^{n+1} \quad \text{(Eq. 4.10)}$$

Here, L_{eff} is the effective film thickness. n corresponds to that in Eq. 4-3. The effective film thickness instead of the film thickness can be thought of as taking into account the effect of non-uniform spatial distribution of traps. This equation is universally valid provided that the carrier mobility is fiend independent and the effect of carrier diffusion is ignored.

Symbols in Fig. 4.12 correspond to leakage currents of 3.5 and 11 nm described in Fig. 4.11, obeying SCLC conduction with exponential trap distribution. Solid line corresponds to the best fit to the leakage currents for both 3.5 and 11 nm films without annealing, confirming SCLC conductions. The best fit is achieved when L_{eff}/L for 3.5 and 11 nm films are 1.0 and 1.5, respectively, indicating that traps of 11 nm film are spatially non-uniform.

♠ This section is prepared after submission to MEJ (Microelectronics Journal).

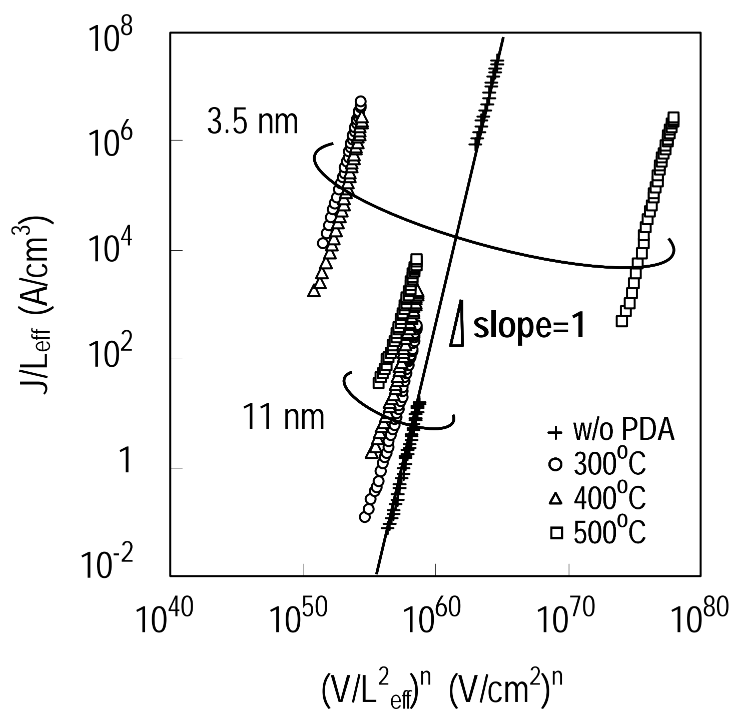


Fig. 4.12. Normalized gate leakage current versus normalized voltage according to SCLC theory.

4.8 Conclusion

The electrical properties of MOS devices with Lanthana film has been investigated. Change in film thickness and ΔV_{FB} with vacuum PDA conditions suggest that oxygen loss would exist at near both cathode and anode. It is found that the current-voltage characteristic with temperatures is significantly related to the traps due to the oxygen loss. Current conductions have been confirmed that the leakage currents are associated with ohmic and P-F conductions when V_{FB} is less than zero, and ohmic and SCLC conductions when V_{FB} is greater than zero. It should be noted that the confirmed conductions are all related to the traps in the oxide film.

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Chapter 5.
Low-Temperature Nitrogen PDA Effect on Lanthana MOS Capacitor[b]

5.1 Introduction

5.2 Experiment

5.3 Conduction models

5.4 Capacitance characteristic

5.5 Mechanisms eliminated

5.6 Mechanisms proposed for low leakage current

5.7 Mechanisms proposed for high leakage current

5.8 Temperature dependence of high leakage current

5.9 Trap spectroscopy of oxide band gap

5.10 SBD and SCLC

5.11 Conclusion

Reference

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[b] [c] This chapter is based on the **accepted** paper: Yongshik Kim, Shun-ichiro Ohmi, Kazuo Tsutsui, and Hiroshi Iwai, "Space-Charge-Limited Currents in La_2O_3 Thin Films Deposited by E-Beam Evaporation after Low Temperature Dry-Nitrogen Annealing," Japan Journal of Applied Physics.

5.1 Introduction

According to the International Technology Roadmap for Semiconductors (ITRS2003) [1], a gate oxide thickness of less than 1 nm is required for a MOSFET with 28 nm gate length. However, gate oxide scaling thinner than 2 nm leads to an exponentially higher gate tunneling current [2]. For this reason, much effort is currently underway on alternative high-*k* gate dielectrics. HfO_2 is expected to be used for the gate oxide of MOSFETs down to 1 nm. On the other hand, rare earth oxides (REO), especially Lanthanum oxide (La_2O_3) and Y_2O_3, are thought to be applied for the gate oxide thickness of less than 1 nm [1]. In fact, there have been several reports that La_2O_3 has superior electrical properties [3-11]. For all that, likewise in other high-k oxides, La_2O_3 have larger densities of charge traps and interface states than those of SiO_2, causing more significant trap-related conductions, such as Poole, P-F (Poole-Frenkel), TAT (Trap-Assisted Tunneling), Junction- like, VRH (Variable Range Hopping), or SCLC (Space-Charge-Limited Current).

In this chapter, we report the result of detailed analysis on the conduction mechanism of E-beam evaporated La_2O_3 films after low-temperature dry-nitrogen annealing.

The electrical characteristics of metal-oxide-semiconductor capacitors with Lanthanum oxide (La_2O_3) gate dielectrics with 1.1 nm EOT (Equivalent Oxide Thickness) are investigated. La_2O_3 was deposited by E-beam evaporation on n-Si(100), and annealed at 200°C in dry-nitrogen *ex-situ* for 5 min. From comparing leakage currents of as-deposited and annealed oxides, it is shown that leakage currents

of annealed oxide were two kinds: low and high leakage currents. Behavior of high leakage currents with applied voltage was similar to that of as-deposited oxide. For the explanation of these two kinds of leakage currents, it is shown that conduction mechanisms strongly related to oxide traps are not responsible for leakage currents, except SCLC (Space-Charge-Limited Current). From the applied voltage and temperature dependences of the current of the gate oxide, it is shown that the main conduction mechanisms for the two kinds of leakage currents are SCLC and Schottky conductions at low and high applied voltages, respectively. The dielectric constant obtained from Schottky conduction was 27 and consistent with the C-V result. Based on SCLC theory, trap levels in the oxide band gap composed of both exponential and localized distributions were extracted by using of the differential method.

5.2 Experiment

La_2O_3 thin films were deposited on HF dipped n-Si (100) substrate (HF-last) by E-beam evaporation at 250°C using MBE equipment. The pressure in the chamber before and during depositions was about 10^{-9} Torr. Then, wafers were annealed in the RTA (Rapid Thermal Annealing) chamber with 1.2 liter/min flow rate of dry-nitrogen gas. Annealing was carried out for 5 min at 200°C. Gas lines and RTA chamber were carefully vacuumed to minimize the oxygen gas prior to annealing. After annealing, Pt electrode was formed by metal evaporation with a metal shadow mask using bell-jar type evaporator at 10^{-5} Torr. An exposure time to the air before gate metal deposition was less than 1 hour. *C-V* and *J-V* measurements were performed using a HP4284A multi-frequency LCR meter and a HP4156C Semiconductor Parameter Analyzer,

respectively. The ramp-up speed of gate voltage in J-V test was 0.1 V/s to achieve steady-state of the oxide leakage current to probe trapping effects since occupied trap level with electron have a release time depending on trap level [12]. The film thickness was confirmed by Otsuka FE-5000 ellipsometer.

Table 5.1. Theoretical expressions of the bulk-limited conduction processes in oxides [12-18]. (a) Variable range hopping, (b) space-charge-limited current: single, uniform, and exponential/ Gaussian distributions.

	Mechanisms		Expressions	
Bulk-Limited	Ω		(1) $J = qn\mu\frac{V}{s} = qN_C \exp\left[-\frac{q}{kT}(F - E_C)\right]\mu\frac{V}{s}$	
	Poole		(2) $J = A\exp\left(-\frac{S_P E}{k_B T}\right) = A\exp\left(-\frac{qd}{2}\frac{E}{k_B T}\right)$	$S_P = \frac{1}{2}qd$
	Poole-Frenkel		(3) $J = qN_C\mu(T)\exp\left(-\frac{\phi_0}{k_B T}\right)\exp\left(\frac{\beta_{PF}}{k_B T}E^{1/2}\right)E$	$\beta_{PF} = 2\beta_S$
	Hopping		(4) $J = \frac{q^2}{k_B T}\frac{d^2}{\tau_0}n^*(T)E\exp\left(-\frac{4\pi m^*}{h}\phi_m d\right)$	$\beta_{PF} = \left(\frac{q}{\pi\varepsilon_0\varepsilon_i}\right)^{1/2}$
	VRH(a)		(5) $J = J_0 \sinh\left(\frac{qRE}{kT}\right)$	
	SCLC(b)	shallow	(6) $J_{shallow} = \frac{9}{8}\mu\varepsilon_i\varepsilon_0\theta(T)\frac{V^2}{s^3}$	
		uniform	(7) $J_{uniform} = 2qn_0\mu\frac{V}{s}\exp\left(\frac{2\varepsilon_0\varepsilon_i V}{N_t kTqs^2}\right)$	
		exponential	(8) $J_{exponential} = N_c\mu\ q^{(1-l)}\left[\frac{\varepsilon\ l}{N_t(l+1)}\right]\left(\frac{2l+1}{l+1}\right)^{(l+1)}\frac{V^{(l+1)}}{s^{(2l+1)}}$	$l = T_c/T$

(a) Variable Range Hopping, (b) Space-Charge-Limited Current: single, uniform and exponential/Gaussian distributions.

Here, m^* denotes the electron effective mass, q the electronic charge, h the Planck's constant, k_B the Boltzman's constant, T absolute temperature, ϕ_0 the metal-insulator barrier height, ε_0 the vacuum permittivity, ε_i the relative permittivity of the insulator, s

the insulator thickness, V the voltage of the insulator, E the electric field of the insulator.

Table 5.2. Theoretical expressions of the electrode-limited conduction processes in oxides [14,16,19-21]. (a) Thermionic current, (b) direct tunneling current, (c) trap-assisted tunneling.

	Mechanisms		Expressions
Bulk-Free (Electrode-Limited)	Schottky[(a)]	(1)	$J = \frac{4\pi m^* q}{h^3} k_B^2 T^2 \exp\left(-\frac{\phi_0}{k_B T}\right)\exp\left(\frac{\beta_S}{k_B T}E^{1/2}\right)$ $\quad \beta_S = \left(\frac{q}{4\pi\varepsilon_0\varepsilon_i}\right)^{1/2}$
	D-T[(b)]	(2)	$J = \frac{q^2}{\pi h}\frac{\phi_0}{s^2}\exp\left(-\alpha^* s\phi_0^{1/2}\right)\sinh\left(\frac{\alpha^* sV}{4\phi_0^{1/2}}\right)$ $\quad \alpha^* = \alpha\left(\frac{m^*}{m_0}\right)^{1/2}$
	Fowler-Nordheim	(3)	$J = \frac{q^2}{8\pi h}\frac{E^2}{\phi_0}\exp\left(-\frac{2}{3}\frac{\alpha^*\phi_0^{3/2}}{E}\right)$ $\quad \alpha = \frac{4\pi(2m_0 q)^{1/2}}{h} = \frac{10.25}{nm\sqrt{eV}}$
	TAT[(c)] deep trap	(4)	$J_{dt} = \frac{2C_t N_t q\Phi_t}{3E_{ox}}\exp\left(-\frac{8\pi\sqrt{2qm_{ox}}}{3h}\frac{\Phi_t^{3/2}}{E}\right)$
	shallow trap	(5)	$J_{sht} = qR_0\nu\left(\frac{s}{E}-\frac{\Phi_t}{E^2}\right)$
	Junction-like	(6)	$I = \frac{\eta V_t}{R_s}W\left\{\frac{I_0 R_s R_{p1}}{\frac{\eta V_t}{R_s}\left(R_{p1}+R_s\right)}\exp\left(\frac{R_{p1}\left(V+I_0R_s\right)}{\eta V_t\left(R_{p1}+R_s\right)}\right)\right\} + \frac{V-I_0R_{p1}}{R_{p1}+R_s}+\frac{V}{R_{p2}}$

(a) Thermionic Current, (b) Direct Tunneling Current, (c) Trap-Assisted Tunneling: deep and shallow traps

Here, C_t denotes a slowly varying function of electron energy, N_t the trap density, ϕ_t the trap energy, m_{ox} the effective electron mass in the insulator, R_0 tunneling rate of an electron from the silicon conduction band into a shallow trap, ν hopping frequency of an electron between shallow traps, η the junction ideality factor, V_t the thermal voltage (= kT/q), W the Lambert function [22,23] defined by the solutions of $W(x)exp(W(x))=x$, R_s the parasitic series resistance, R_{p1} the shunt loss resistance at the device, R_{p2} the shunt loss resistance at the device periphery, I_0 the junction reverse current, d the distance between the trap centers, F the quasi-Fermi potential of the insulator, E_C the conduction band edge of the insulator, N_C the effective density of states in the insulator conduction band, m the carrier mobility, τ_0 the time constant, n^* the density of free electrons in the insulator, ϕ_m the energy corresponding to the maximum of the barrier, R the hopping distance, J_0 the temperature dependent factor related to electron-phonon interactions, θ the trapping factor defined by the ration of the free electron density and the density of filled trapping sites.

5.3 Conduction models

Various conduction mechanisms are summarized in Table 1 and 2 and are examined to investigate the leakage conduction [12-21].

Conductions related with high trap density are Poole, P-F, TAT, Junction-like, VRH, and SCLC.

Poole and P-F conductions assume paired and isolated trap sites, respectively [24], depending on oxide trap density. Transition between two models has been reported [18,25]. As the oxide field becomes lower, current density following P-F conduction could be described by Poole conduction, because reduction in barrier height by electric field becomes smaller and the trap level becomes comparable to that of the Poole [25]. In Poole conduction, traps are close enough to perturb coulombic potential of neighbor trap, so that decrease in barrier height between two traps is determined by distance between traps and applied field, not by coulombic field as for the case of P-F. This leads to leakage current independent of film dielectric constant. VRH conduction involves thermally activated hopping conduction in localized electronic states near the Fermi energy. VRH is the dominant conduction at low applied voltage and high temperatures [26]. TAT conduction requires shallow and/or deep trap levels and occurs at oxide field, similar to F-N conduction case, greater than 4 MV/cm [27,28]. Fleming suggested that leakage current can flow through the defect band formed by localized large trap levels and then behavior of the current is similar to junction-like conduction due to difference in energy level between defect band and Fermi level at both electrodes [29]. As regard to relation between oxide trap density and leakage

current, traps enhance the leakage current for the case of Poole, VRH, TAT, and Junction-like, while they hinder it for SCLC case. This is the uniqueness of SCLC contrast to the others.

SCLC model has been developed and used continuously over four decades. Until now numerous attempts have been reported to interpret the current behavior of thin films within the frame of SCLC. Such films are: porous SiO_2 [30-32], TiO_2 [33], organic materials [34], porous silicon [35,36], SiO_2/Nitride [37], Si_3N_4 [38,39], $SrTiO_3$ [40-43], Ta_2O_5 [44,45], Al_2O_3 [46-48], Nb_2O_5 [49], and Nd_2O_3 [50], Gd-In-oxide [51], Dy_2O_3 [52,53] and La_2O_3 [54] in REO. From SCLC theory, trap density can be extracted from *J-V* relation using trap spectroscopy methods [13,55]. Among them, step-by-step [56] and differential [57-59] methods are known to be accurate to express real trap density distribution [60]. Trap density distribution is generally described by one of the following ways: 1) discrete level [61], 2) exponential distribution [55], 3) Gaussian distribution [62], and 4) uniform distribution [12,55]. Smeared Gaussian trap density distribution, discrete trap level with tails, or pseudo-uniform distribution can be described by exponential distribution [63]. Thus, since the trap density distribution is often spread out in nature, current-voltage relation of exponential trap distribution can be useful as the first evaluation method. Exponentially distributed traps are characterized by two parameters, namely trap density N_t and a characteristic constant of the distribution T_c, through the expression [12],

$$N_t(E) = \frac{N_t}{kT_c} \exp\left[\frac{E - E_c}{kT_c}\right] \tag{1}$$

where $N_t(E)$ is the trap concentration per unit energy range, k Boltzman's constant, E the energy, and E_c energy level of conduction band edge. This equation is valid when $E<E_c$.

5.4 Capacitance characteristic

Figure 5-1 shows the normalized physical film thickness as a function of PDA temperature with dry-nitrogen ambient for 5 min. Normalization is performed with respect to the physical film thickness of non-PDA film. One can find that the normalized thickness is minimized at around 300^oC PDA temperature. This could be achieved by the trade-off between the densification process which is effective less than 300^oC and the interfacial layer growth which becomes important greater than 300^oC. PDA at temperatures less than 300^oC mostly provides the densification of the film with a negligible interfacial layer growth. This is why we fabricated the film with a low temperature PDA, such as 200^oC.

Figure 5-2 shows typical *C-V* curve of dry-nitrogen annealed La_2O_3 capacitor. Physical thickness (T_{film}) measured by ellipsometer was 7.7 nm and EOT (Equivalent Oxide Thickness) with taking into account quantum effect was 1.1 nm. Obtained relative dielectric constant was 27, which is same to the previously reported value [6]. Considering the work function difference between the n-type Si substrate and the Pt electrode, flat-band voltage shift ΔV_{FB} is about -0.61 V. This means that positive fixed charges are present in the La_2O_3 gate dielectric and the effective density of these charges is estimated to be about 7.3x10^{12}/cm^2, which can be considered as interface trap density (N_{it}). Oxide trap density (N_{ot}) and distance between traps (d_{trap}) with uniform distribution assumption can be obtained from following relations: N_{ot}~N_{it}/T_{film} and d_{trap}= $(N_{ot})^{-3}$. N_{ot} and d_{trap} were found to be about 4.1x10^{19}/cm^3 and 2.9 nm, respectively. N_{it} at the flat-band voltage was about 10^{13}/cm^2 from Terman method, which is known to

be accurate for measuring interface trap densities above 10^{12}/cm^2/eV [62].

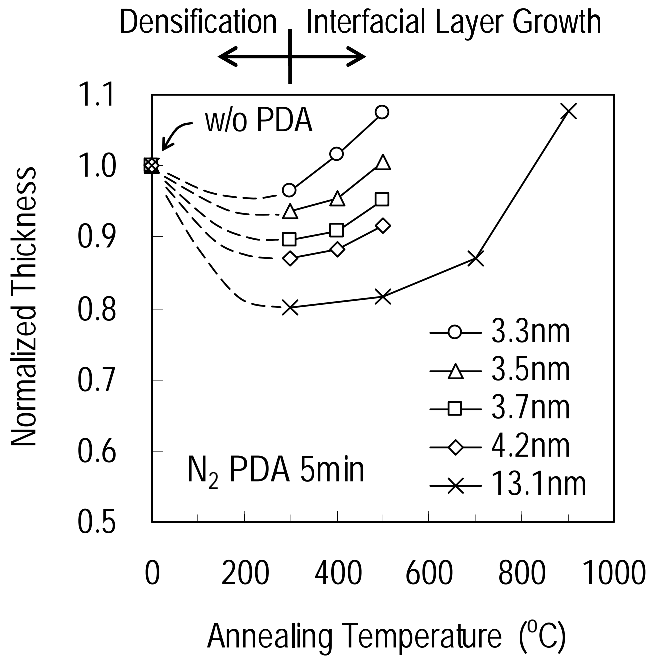


Fig. 5.1. Normalized La_2O_3 film thickness as a function of nitrogen PDA temperatures. Normalization is carried out with respect to the non-PDA film thickness.

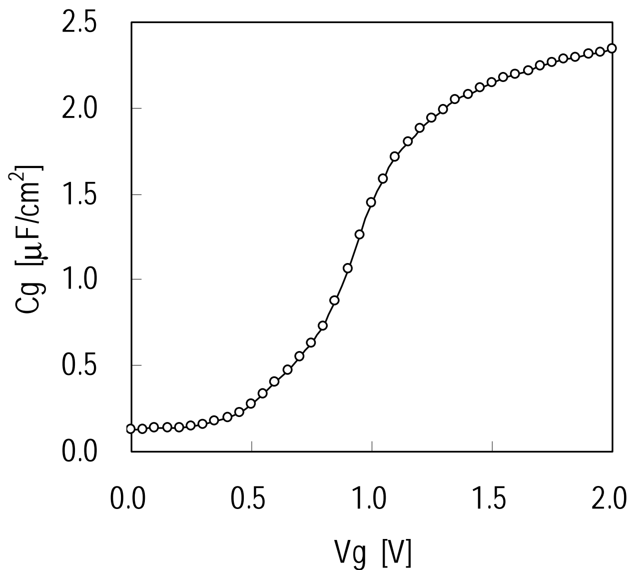


Fig. 5.2. Typical *C-V* curve of PMOS La_2O_3 capacitor. Frequency at measurement is 1 MHz. Physical film thickness obtained from the spectroscopic ellipsometry is 7.7 nm. Flat-band voltage V_{FB} is 0.88 V and ΔV_{FB} is -0.61 V.5.5 Mechanisms eliminated

5.5 Mechanisms Eliminated

Figure 5-3 shows typical *J-V* characteristics of La_2O_3 MOS capacitors before (A) and after (B) and (C) 200°C dry-nitrogen annealing. The capacitor films corresponding to (B) and (C) have the equal thickness 7.7 nm and the same *C-V* characteristic as shown in Fig. 5.2. After the annealing, the leakage current decreases significantly (B). Leakage current of (B) at 1 volt is 2.5x10^{-6} A/cm^{2}. This value is similar to previous report [6]. However, some of the samples show still high leakage current (C). The leakage currents shown in Fig. 5.3 are the common features even in the samples fabricated in a different way, although the magnitude in the leakage current is different.

Figure 5-4 shows Poole plot of *J-V* curve for both low and high leakage currents, corresponding to (B) and (C) in Fig. 5.3. Poole conduction describes leakage current in the range of voltages from 3.4 to 4.2 V. Obtained distance between traps in this voltage region was 0.3 nm, which is less than critical distance about 3 nm in transition between Poole and P-F conductions [18]. However, the obtained trap distance is less than the lattice constant about 1 nm of La_2O_3 [65]. This confirms that the Poole is not the mechanism of the leakage currents for both low and high leakage currents.

Figure 5-5 shows P-F plot of the *J-V* curve for both low and high leakage currents. The best fit of experiments to P-F conduction with permittivity of 27 was found at voltage around 1 V. Due to the narrow voltage range of the fit, P-F is hardly ascribed to the main conduction.

Figure 5-6 shows TAT plot of the J-V curve for both low and high leakage currents. Linear relationship is found at both low (1.9~3.5 V) and high (>4 V) voltages.

However, barrier height obtained from the two linearities of the low and high voltages were 0.01 and 0.03 eV, respectively. They are too small compared to the reported values at room temperature [64]. This observation is also in agreement with the fact that TAT contribution to leakage current is small at low applied voltage in oxides with thickness greater than 4.5 nm [67].

Figure 5-7 shows leakage current density versus voltage with a junction-like conduction model fitting. log(I) vs V_g can be fitted by a straight line with slope V_{th}/m, where V_{th} is thermal voltage, m the ideality factor. Without a consideration of parasitic effect such as series and parallel resistance, fitting was not good. These resistance effects were taken into account by using of non-ideal single-exponential diode equation [21]. Best fitted results considering the parasitic effects were obtained as shown in Fig. 5.7.

To the best of our knowledge, the leakage current can be described by junction-like conduction model in three cases. The first case is when oxide film has localized trap levels large enough to be considered as a defect band located across the film and slightly above cathode Fermi level and anode Fermi level with a large energy difference [29]. This results in the asymmetry of leakage current of MIM (Metal-Insulator-Metal) film with injection polarity. The second is the case of well-known Schottky tunnel diode [14]. The third is the case when oxide has locally high conducting paths introducing a kink in the I-V curves due to the disappearance of inversion layer at the flat band voltage [68]. These three cases are useful for the explanation of high leakage current conduction rather than low leakage current, because low leakage current in oxide can hardly be ascribed to junction-like leakage current. Thus, high leakage current of La_2O_3 oxide is worth being investigated by means of junction-like conduction. Regarding the first case, leakage current conduction is

described in terms of phonon-assisted tunneling (PAT) conduction [69]. According to PAT, temperature dependence of current is non-Arrehnius, with a feature of nearly zero activation energy at low temperature less than room temperature. This is qualitatively different from the La_2O_3 film case as depicted in Fig. 5.9. For the second case of Schottky tunnel diode, ideality factor m is known to be around 1 [70,71]. However, m for fitting in Fig. 5.7 was 2.1, which is about twice as large as the reported values. For the third case, there was no kink in *J-V* as can be seen in Fig. 5.3. In addition, at high voltage (>1 V) fitting was not good for high leakage currents.

Figure 5-8 shows a fit of experimental results to VRH conduction at high voltage region. From the fitting, hopping distance is obtained approximately as 0.2 nm, which is small compared to reported values [72,73]. In addition, fitting at low voltage ranges was not good.

Figure 5-9 shows activation energy of high leakage current versus applied voltage. Although current of VRH is inversely proportional to the one fourth power of Kelvin temperature, current could be described by Arrehnius relation in the limited range of measurement temperature. Despite Arrehnius relation overestimates the hopping energy [72], the activation energy could determine whether or not VRH dominates the leakage current. At low applied voltage the activation energy is around 0.4 eV, which is high to be considered as that of VRH, since activation energy of VRH is usually around 0.1 eV [26,72,74].

Therefore, trap-related conductions mentioned above can be ruled out except SCLC.

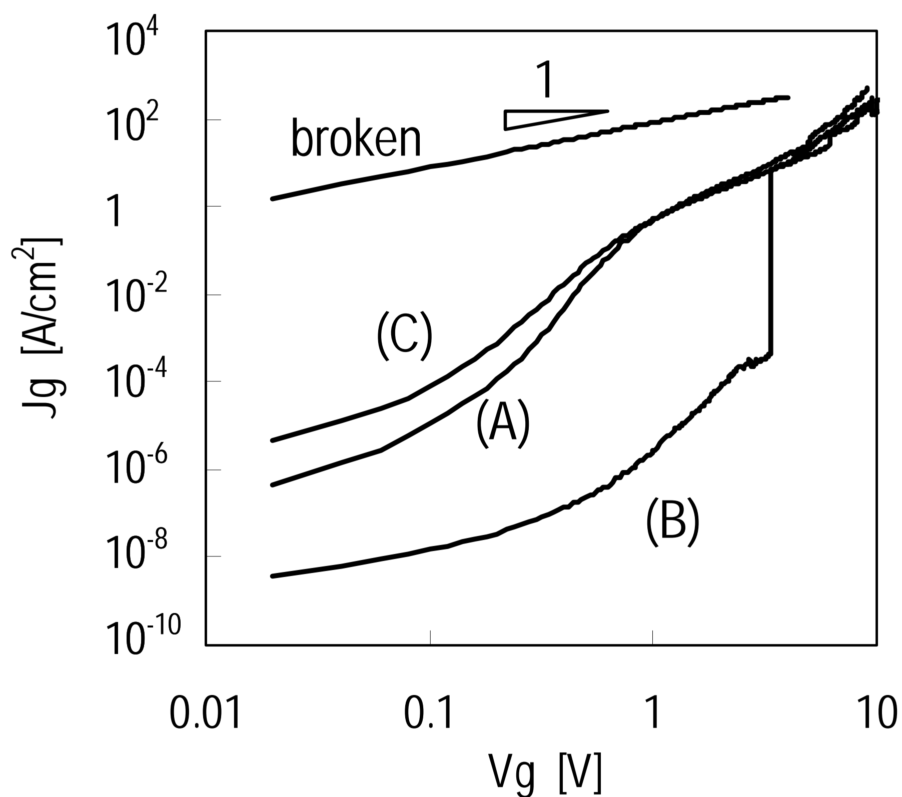


Fig. 5.3. Typical *J-V* characteristics: Before (A) and after (B) and (C) dry-nitrogen annealing at 200°C for 5 min. Films of (B) and (C) have the same *C-V* characteristic depicted in Fig. 5.2.

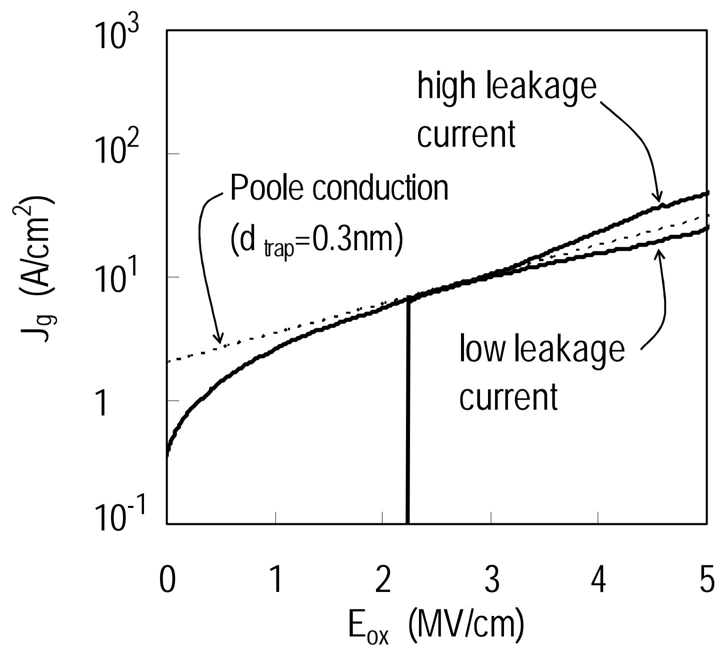


Fig. 5.4. Poole plot of dry-nitrogen annealed films: log(J_g) versus oxide field E_{ox}. Dotted line corresponds to the best fit to experimental results obeying Poole conduction model. Solid lines correspond to experimental results.

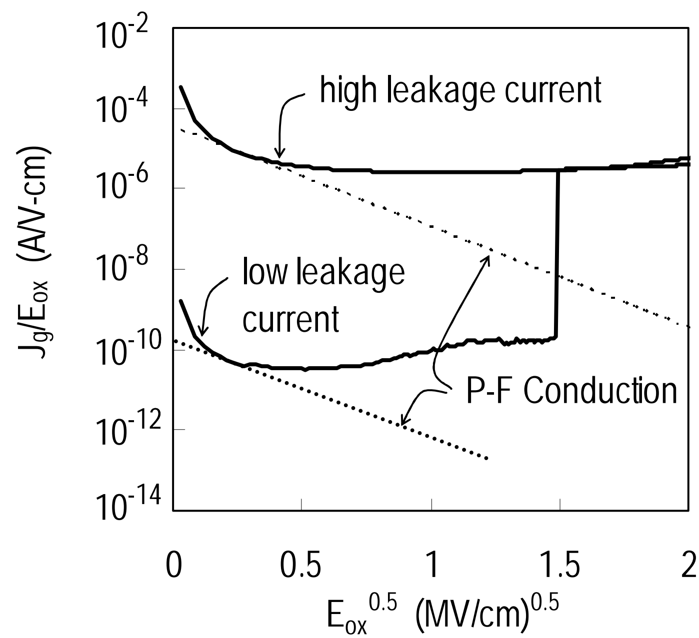


Fig. 5.5. P-F plot of dry-nitrogen annealed films: log(J_g/E_{ox}) versus square root of oxide field E_{ox}. Solid lines correspond to experimental results. Dotted lines correspond to the best fits to experimental results following P-F model with permittivity of 27.

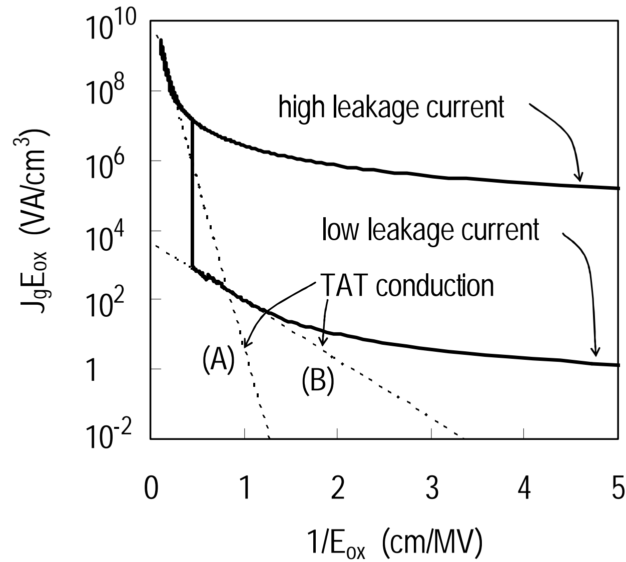


Fig. 5.6. TAT plot of dry-nitrogen annealed samples: log(J_gE_{ox}) versus inverse oxide field E_{ox}. Solid lines correspond to experimental results. Dotted lines are the best fits to experimental results obeying TAT model. Barrier heights were found to be 0.01 and 0.03 eV for (A) and (B), respectively.

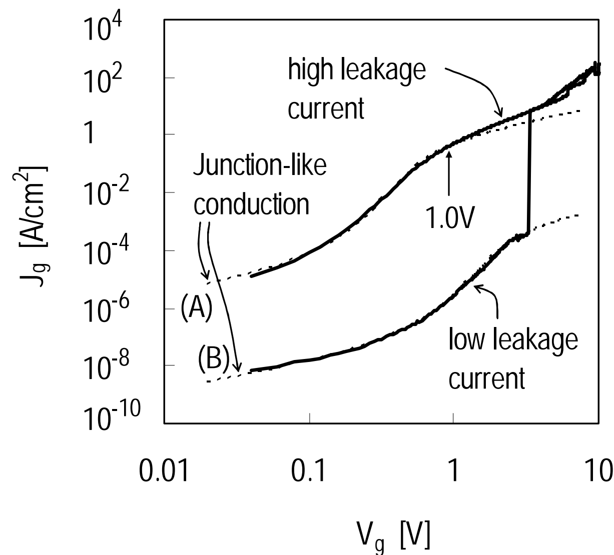


Fig. 5.7. Junction-like conduction of dry-nitrogen annealed samples. Solid lines correspond to experimental results. Dotted lines are the best fits to experimental results. Junction-like conduction includes parasitic effect of series resistance R_s, parallel junction resistance R_{p1}, and parallel periphery resistance R_{p2}. Fitting was carried out with following parameters. Parameter notation and equivalent circuit obey Oritz-Conde.[21)] For fit (A), Io=1.4x10^{-5}A/cm^2, m=2.1, R_s=1Ω, R_{p1}=5x10^{7}Ω, and R_{p2}=10^{8}Ω. For fit (B), Io=2x10^{-8}A/cm^2, m=8, R_s=3x10^{3}Ω, R_{p1}=5x10^{7}Ω, and R_{p2}=10^{8}Ω.

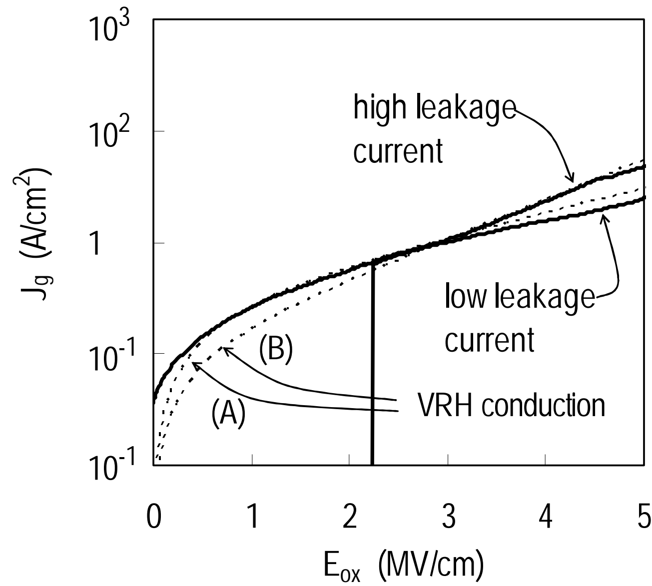


Fig. 5.8. VRH conduction of dry-nitrogen annealed films. Solid lines correspond to experimental results. Dotted lines correspond to the best fits to experimental results obeying VRH model. Hopping distances of fits (A) and (B) are 0.13 and 0.21 nm, respectively.

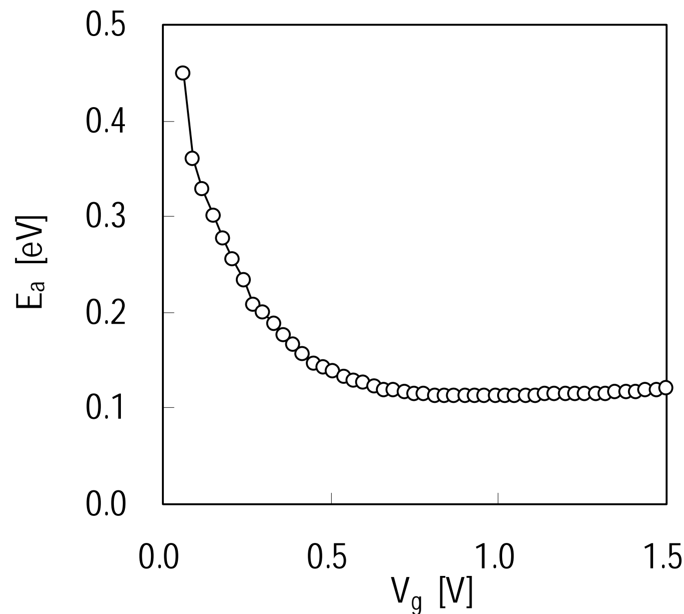


Fig. 5.9. Activation energy E_a of high leakage current density as a function of gate voltage. E_a is obtained from Arrehinus relation: $J{\sim}exp(qE_a/kT)$.

5.6 Mechanisms proposed for low leakage current

According to SCLC theory [12,13,15] and requirement for bulk-limited conduction [75], the J-V characteristics should initially be ohmic (J~V) at low applied voltage, as in region I in Fig. 5.10. Region II followed by ohmic region is fitted with the square gate voltage (J~V^2). If all the trap sites at the single trap level are filled with electrons, current increases suddenly due to the rapid increase of quasi Fermi level in the oxide band gap with applied voltage, which occurs between regions IV and V.

This transition voltage from region IV to region V in Fig. 5.10 is known as trap-filled limit voltage (V_{TFL}). With the assumption of single discrete trap energy level, V_{TFL} is expressed as follows [12,15]:

$$V_{TFL} = \frac{qN_t L^2}{2\varepsilon} \qquad (2)$$

where q is electronic charge, N_t total trap density, L film thickness, and ε film dielectric constant. From V_{TFL}=3.5V, it was found that N_t=1.8x10^{20}/(cm^{2}eV) which is in reasonable agreement with that from C-V. We can obtain the ratio of free carriers to trapped carriers from J(onset)/J(exit)=θ, where J(onset) and J(exit) are currents at bottom and top of vertical jump at V_{TFL}, and θ is the ratio called trapping factor [60]. Obtained trapping factor is 10^{-4}. Since trapping factor is reported as around 10^{-7} generally in SCLC [13], bigger trapping factor than the reported value indicates that trap distribution could be described by a combination of the full single level assumption and other distributions. This is discussed further in the section of trap spectroscopy.

The discontinuous increase in the leakage current at V_{TFL} looks like a hard breakdown, but is a widely accepted feature in the SCLC conduction [12]. It could not

be the breakdown due to the following reasons: 1) discrepancy in the magnitude of the current between the broken device and the SCLC conduction just after the abrupt current increase at the voltage called V_{TFL}, 2) the leakage current of (B) after V_{TFL} which is similar in magnitude to that of other types (A) or (C), 3) exact square law relation in log(J)-log(V) after the abrupt current increase at V_{TFL}: J~V^2. The easiest way to confirm the non-breakdown of the device is to check reproducibility of the J-V behavior over iterative voltage sweeps on the same device. However, after several voltage sweeps, J-V curve like (A) or (C) in Fig. 5.3 was observed instead of (B). This could be due to the high leakage current over 1 A/cm^2, which may lead to a change in the film state, with a possible joule-heating process. It can be expected that the trap density is changed during or after the abrupt increase of the leakage current.

The abrupt current jump at V_{TFL} can be also caused by the soft breakdown (SBD) of the film. In order to distinguish the soft breakdown from the SCLC process, the gate leakage currents for five films showing the abrupt current jump were compared as shown in Fig. 5.11. From the SCLC theory, current variation before V_{TFL} could be due to the difference in the exponential trap level distribution in the oxide band gap. This is because the current is proportional to the power law of voltage, as described by equation (8) of table 1. If the gate leakage currents after V_{TFL} obey the SCLC theory, the gate leakage current jumps occur at the nearly same voltage within a variation which might be caused by the trap density variation. On the other hand, if the current jump corresponds to the soft breakdown of the film, the gate voltages of the current jumps have statistical fluctuation. Figure 5-11 shows almost identical fluctuation in the voltages of the current jumps, current magnitudes after the jump, and the numbers of jump steps. Thus, the rapid current jump in Fig. 5.10 is probably associated with the SCLC process. As stated previously, high gate leakage current after the jump can

change the film state and then *J-V* behavior becomes irreproducible. From this viewpoint, the abrupt current jump could be also considered as being a kind of SBD. The abrupt current jumps by SBD and SCLC are schematically illustrated in Fig. 5.12. SBD current can be classified by two categories: analog SBD and digital SBD [76]. It has been reported that gate voltages at a fixed current in case of analog SBD varies widely [77-81], and SBD voltages, defined the gate voltage where gate current increases steeply in case of digital SBD, are distributed in a very wide range [77-79,81-84], as shown in Fig. 5.12(a). It is notable that switching behavior of digital SBD current with a small number of jumping-down steps, that is with a long span of applied voltage before jumping down of the current, may be similar to the abrupt current jump seen in Fig. 5.10 and 5-11. Switching behavior of digital SBD conduction is known to be ascribed to trapping-detrapping process, effective thickness fluctuation at locally damaged region, or on-off modulation of breakdown paths [84]. However, trap filled limit voltage V_{TFL} of SCLC, shown in Fig. 5.12(b), is ascribed to the decrease in trapping efficiency. Inset in Fig. 5.12(b) shows localized trap level distribution near to the carrier conduction band edge. These localized trap levels in the band gap of dielectric can be originated from the atomic defects [85-92]. With zero Kelvin degree consideration of Fermi level and trap-limited conduction of the SCLC theory, quasi-Fermi level below the trap levels indicates vacant localized trap levels, which are effective in reducing the current. This is simply because most of the injected carriers can be trapped at the trap levels. As the injection level increases, i.e., the applied voltage increases, the quasi-Fermi level moves up and becomes greater than the localized trap levels, for the case of electron injection. This indicates that all the localized trap levels are full with charges, loosing their effectiveness in depressing the current. Then, all the injected charges appear in the carrier conduction band and the

current increases rapidly to the trap free case. The current of the trap-limited and the trap free cases obeying SCLC theory is given by [12,13,15]:

$$J = \frac{9}{8}\mu\varepsilon\theta\frac{V^2}{L^3} \tag{3}$$

where, J is the space-charge-limited current, μ carrier mobility in dielectric film, ε film dielectric constant, θ trapping factor, V applied voltage, and L film thickness. Trapping factor θ is 1 for the trap-free case and around 10^{-7} for the trap-limited case. Smaller trapping factor indicates higher efficiency in trapping injected charges and reducing the current. It is noteworthy that the current is proportional to the square voltage, irrespective of whether trap-limited or trap free case, in other words, before and after the abrupt current jump at V_{TFL}.

From the single trap level case of SCLC, vertical jump in current between regions IV and V in Fig. 5.10 should be preceded and followed by the square voltage law. However, measured data deviates from the square voltage law in region III and leakage current is proportional to the 4.5 power law of voltage ($J\sim V^{4.5}$). This kind of J-V characteristics exactly fits with equation (8) of SCLC in table 1, where $(T_c/T+1)=4.5$ is similar to the reported value [54]. Equation (8) describes J-V characteristics of SCLC conduction when trap energy is distributed exponentially, while equation (6) describes those when trap energy is discrete and single.

At high voltage in region VI Schottky-like conduction was observed and the Schottky plot is presented in Fig. 5.13. From the Schottky conduction model, the dielectric constant was 27, which is in accordance with that of the C-V curve. A dielectric constant obtained from the Schottky plot should be between the optical dielectric constant (ODC, or high-frequency dielectric constant) and static dielectric constant (SDC), or close to ODC. If so, the dielectric constant is called self-consistent

[93,94]. From the Calusius-Mosotti equation, the dielectric constant of a material can be expressed as a sum of the contributions from the electronic polarizability, the ionic polarizability, and the dipolar polarizability [95]. ODC arises almost from the electronic polarizability. This is because dipolar and ionic contributions are small at optical frequencies. The electronic polarizability of an ion depends on its size, so that the negative ions are highly polarizable [96-97]. Thus, one would expect that ODC can be larger than that contributed by only the electronic polarizability. For this reason, the dielectric constant obtained from the P-F or Schottky plot is between the two dielectric constants and then called self-consistent. It is found that ODC of the Lanthana film is about 1.8 by spectroscopic ellipsometry. This value is in agreement with the value 2.0~2.1 of Kar [98]. Since ODC is 3.2 (=1.8^2) and SDC is 27, the dielectric constant 27 from the Schottky conduction is on the boundary of the two dielectric constants. This indicates that the dielectric constant 27 is self-consistent. Furthermore, since the leakage current is measured at the static voltage, the dielectric constant from the conduction is expected to be closer to SDC.

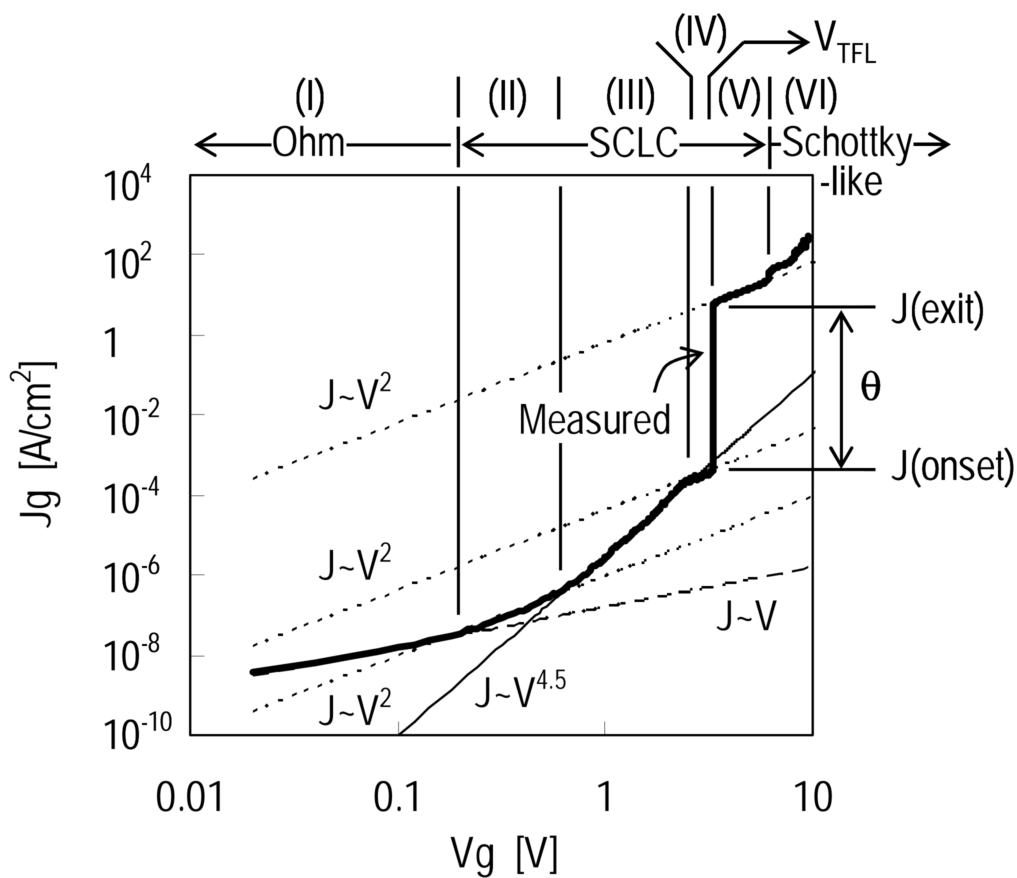


Fig. 5.10. Typical low leakage current density of dry-nitrogen annealed La_2O_3 film, in log(J)-log(V) scale, at room temperature. Thick solid line is experimental result and other lines are calculated curve. Current-voltage relations are shown near the calculated curve. θ is trapping factor [62,101].

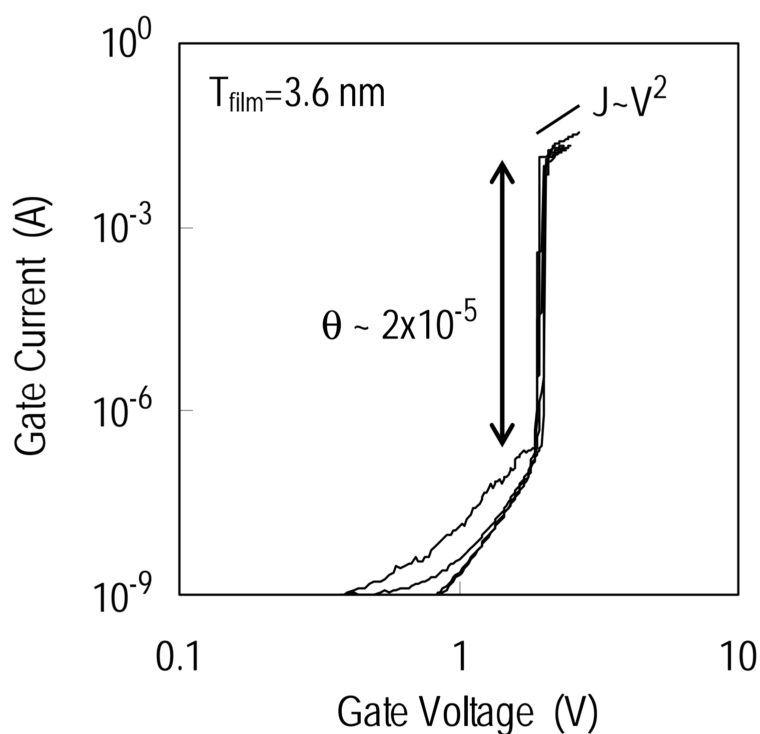
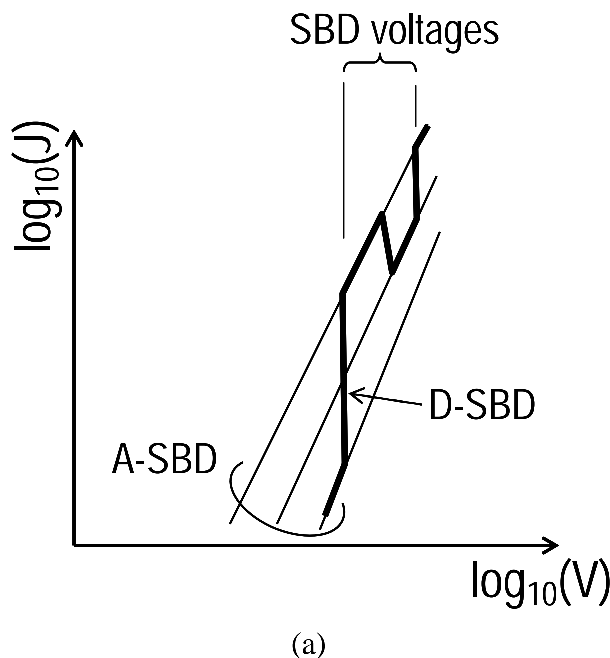
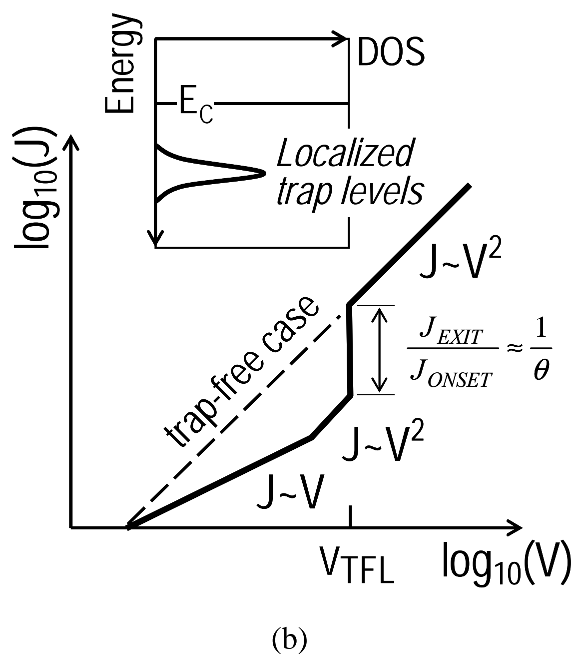


Fig. 5.11. *J-V* characteristic of La_2O_3 PMOS capacitor for five films annealed at 300°C in oxygen ambient, showing the abrupt current jump similar to (B) in Fig. 5.10. The physical film thickness from spectroscopic ellipsometry is 3.6 nm. Gate electrode is Pt and its area is 1.62x10^{-5} cm^2. Trapping factor θ from the SCLC theory is of the order of 10^{-5}. Abrupt current jumps occur at the voltages from 1.9 to 2 volt.



(a)



(b)

Fig. 5.12. Schematic drawing of logarithmic *J-V* showing (a) SBD and (b) SCLC conductions. A-SBD and D-SBD denote analog- and digital-SBD, respectively. Typical A-and D-SBD currents are schematically taken from the reports by E. Miranda *et al*. [78,82]. D-SBD voltages fluctuate widely as shown in (a) whereas V_{TFL} is constant shown in (b). In (b), square law current with dashed line corresponds to the trap free case and another square law current with solid line before the steep current jump corresponds to the trap-limited case, according to SCLC theory. Inset illustrates the localized trap levels near to the conduction band edge, corresponding to J-V

behavior in (b).

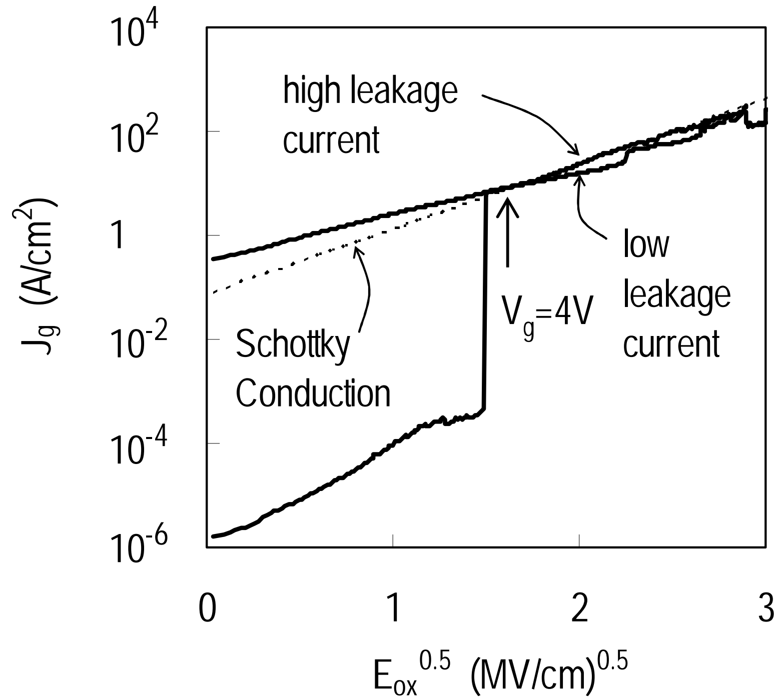


Fig. 5.13. Schottky plot of dry-nitrogen annealed films. Solid lines correspond to experimental results. Dotted line is the best fit to experimental results obeying Schottky conduction with permittivity of 27.

5.7 Mechanisms proposed for high leakage current

Behavior of high-level leakage current density shown in Fig. 5.14 is similar to the case of low-level leakage current, except no vertical jump in current. At low voltage range below 0.2 V, ohmic and voltage square law dominates the current for regions I and II respectively. Then, current of region III is proportional to 4.5 power of the

voltage following the exponential trap level case of SCLC, which is same to the case of region III in Fig. 5.10. At voltage greater than 0.9 V in region IV, square voltage law begins to prevail. Above the voltage of 4 V, i.e. region V, Schottky conduction describes well the measured data. This transition form the bulk-limited conduction of SCLC to emission-limited conduction of Schottky is the typical behavior at high voltage regions [99-103].

From the Schottky conduction model, the dielectric constant was 27 similarly to the low-level leakage current case shown in Figs. 5-10 and 5-13.

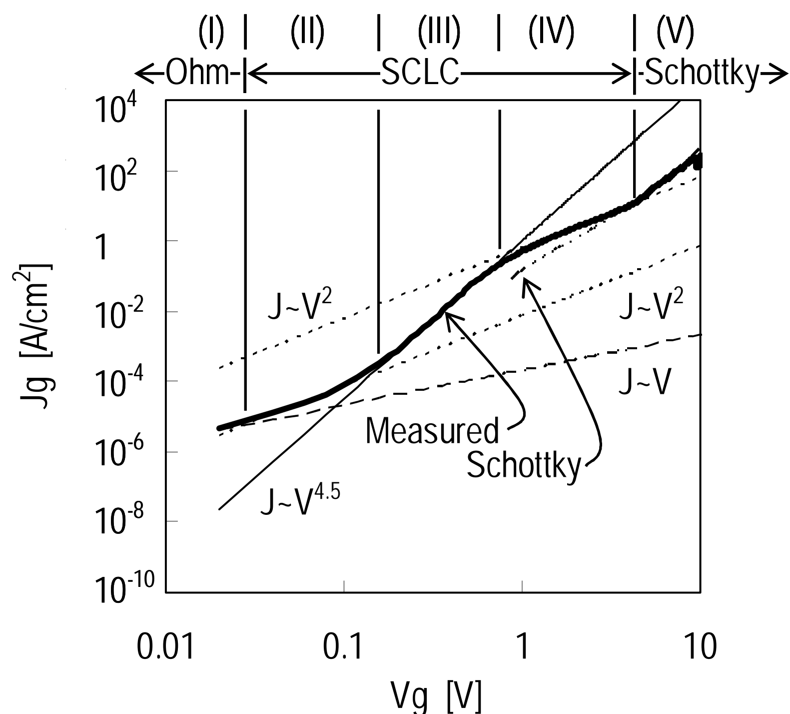


Fig. 5.14. Typical high leakage current density of dry-nitrogen annealed La_2O_3 film, in log(J)-log(V) scale, measured at room temperature. Thick solid line is experimental result and other lines are calculated curve. Current-voltage relations are shown near the

calculated curve.

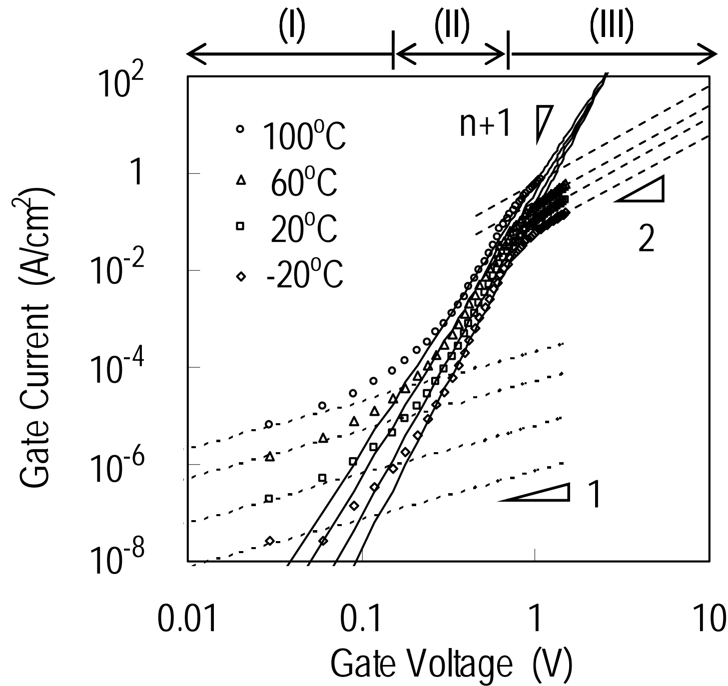


Fig. 5.15. High leakage current density at the low-gate-voltage region with four different temperatures. Numbers are power terms of the gate voltage V_g. Symbols correspond to experimental results. The solid lines represent a fit with the power law dependence. n ranges from 4.5 to 6.

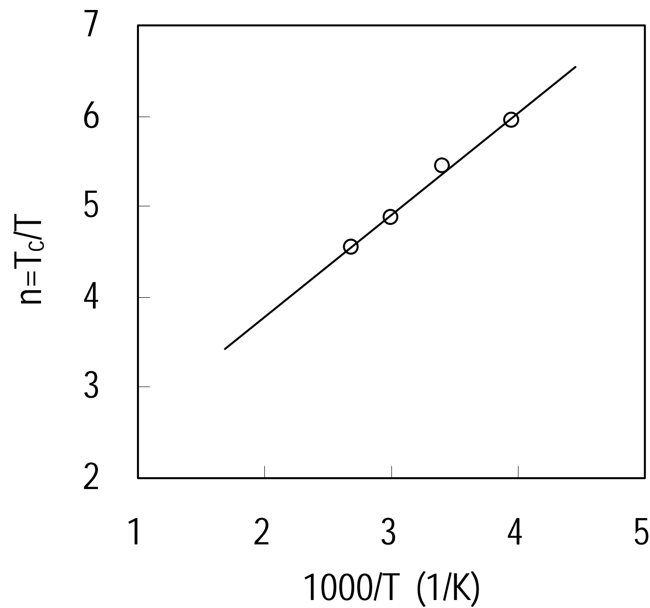


Fig. 5.16. The temperature dependence of the exponent n as a function of 1000/T with T

as the operation temperature. The *J-V* characteristics of Fig. 5.15 were fitted by $J \sim V^{n+1}$. The solid line represents a linear fit between n and 1/*T*.

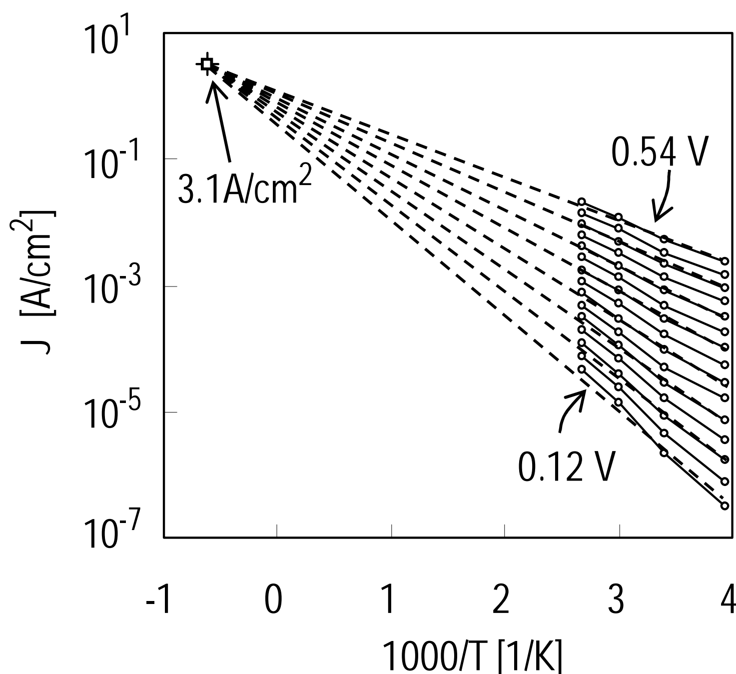


Fig. 5.17. High leakage currents as a function of 1000/*T* with different applied voltages. Circles are measured data shown in Fig. 5.15 and dotted lines are extrapolation of data. Leakage currents are plotted in the voltage range from 0.12 to 0.54 V with 30 mV step. Dotted lines cross at the common intersection point suggested by Gould [104]. At the point, the current is independent of voltage.

5.8 Temperature dependence of high leakage current

In order to further confirm the above estimations of the conduction mechanisms, temperature dependence of the high leakage currents were plotted as shown in Fig. 5.15. It is seen that the slopes of the curves in region II are temperature dependent such that as temperature increases the slopes decrease slightly, but the other regions I and III are

practically independent of temperature. This implies SCLC of exponential trap distribution in region II.

For the exponential trap distribution case of SCLC, current is determined by $T_c/T+1$ power law of voltage, where T_c is the characteristic temperature responsible for trap distribution. T_c determines the shape of the exponential trap level distribution and should be a linear function of inverse temperature, as shown in Fig. 5.16. This confirms that leakage current of region III in Fig. 5.14 is associated with SCLC.

Continuous decrease of activation energy of leakage current at voltage less than 0.7 V shown in Fig. 5.9 indicates continuous increase of quasi Fermi level in the band gap according to SCLC theory. Saturation of decrease in the activation energy above 0.7 V suggests that SCLC conduction with a shallow trap level [104]. DOS (Density Of States) tails of conduction band are responsible for SCLC conduction with the shallow trap level corresponding to region IV in Figs. 5-10 and 5-14. In addition to SCLC, current could be partially contributed by emission-limited conductions [99,100]. This is because Schottky conduction with larger permittivity than that obtained from C-V was found in the range of square root oxide field from 0 to 1.5 $(\mathrm{MV/cm})^{0.5}$, as shown in Fig. 5.13.

Figures 5-17 and 5-18 show the common intersection points of log(J)-1000/T and log(J)-Vg plots for high leakage current respectively. These intersection points are also indicative of space-charge-limited flow with an exponential trap distribution [104,105].

The intersection point suggested by Gould [104] shown in Fig. 5.17 is described by $J=q^2L\mu N_cN_t/4\varepsilon$ and $T=-T_c$., where q is electronic charge, L film thickness, μ mobility, N_c density of states of conduction band, N_t trap density, and ε dielectric constant. μN_c was obtained from the Arrhenius form of SCLC equation [106] and found to be

2x10^{13}/V-s-cm. The intersection point suggested by Sussman [105] shown in Fig. 5.18 is described by $V=qL^2N_t/2\varepsilon$. From the common intersection points in Figs. 5-17 and 5-18, total trap density N_t were obtained as 7.6x10^{19} and 1.4x10^{20}/(cm^{3}eV), respectively.

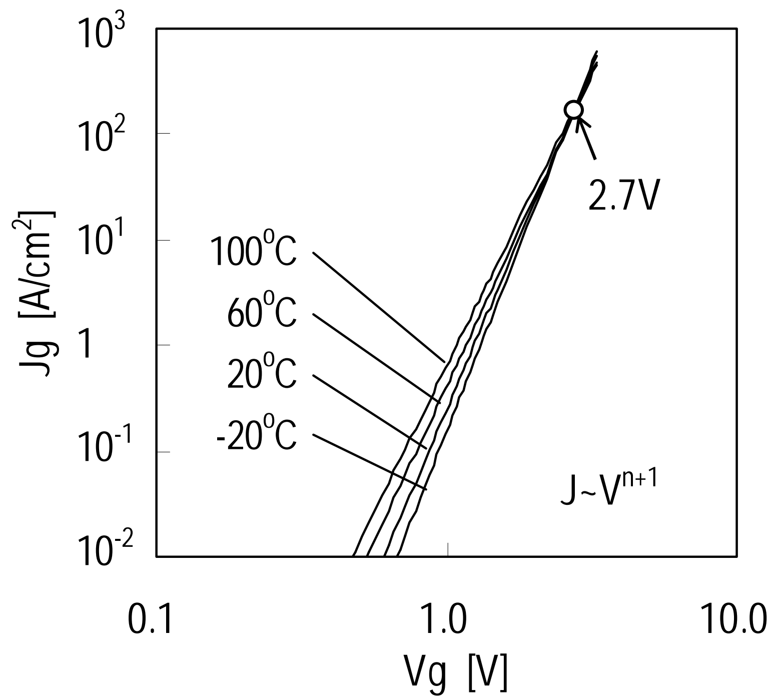


Fig. 5.18. High leakage currents as a function of voltage with different temperatures. Lines are extrapolation of the measured data in Fig. 5.15. They cross at the common intersection point suggested by Sussman [105]. At the point, the current is

independent of temperature.

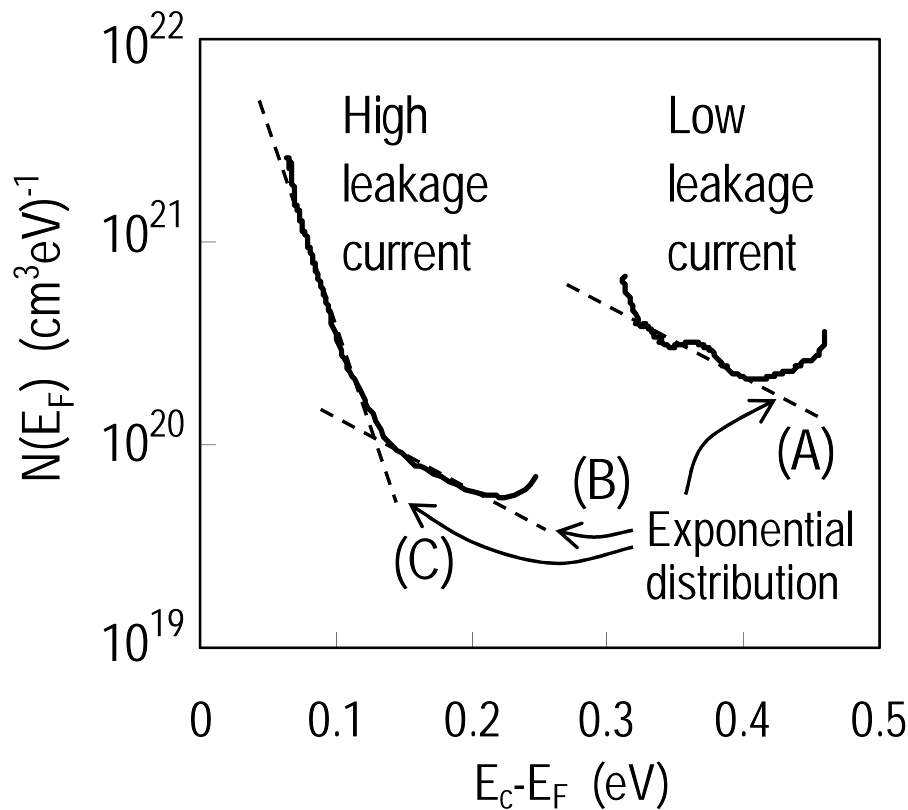


Fig. 5.19. Bulk trap spectroscopy from the *J-V* behavior of Figs. 5-10 and 5-14 with differential method. E_c-E_F is the distance between the conduction band edge and the quasi Fermi level. Solid lines represent trap density. Dotted lines (A), (B), and (C) are fits of the trap density to the exponential trap distribution.

5.9 Trap spectroscopy of oxide band gap

Figure 5-19 shows the trap level distribution of low and high leakage currents. Trap level distribution in the oxide band gap is characterized by the differential method of the SCLC theory [57,59,60].) The steep rise near quasi Fermi level at low applied voltage might not represent the real trap density of states, which is known as the inaccuracy of

differential method [107].

For the case of low leakage current, trap density *N(E)* fit the exponential distribution with E_F between E_c-0.31 and E_c-0.42 eV, marked with (A). The obtained trap density around $6x10^{20}/(cm^3eV)$ from the differential method is slightly greater than that from V_{TFL}. This discrepancy can be explained as follows. The differential method is valid at low temperatures since the method assumes that quasi-Fermi level distinguishes between filled and empty trap levels [57]. In order to describe current-voltage relation, ohmic field is approximated by average film field with a factor-of-two inaccuracy [57,63]. Furthermore, V_{TFL} probes the trap density throughout the film, while the differential method deals with the trap distribution near the anode of the film. The difference in the obtained trap densities from V_{TFL} and the difference method may indicate that trap distribution could be spatially non-homogenous.

For the case of high leakage current, trap density was fitted into two exponential distributions marked with (B) and (C), as shown in Fig. 5.19. The exponential distributions of (B) and (C) are between E_c-0.14 and E_c-0.2 eV and between E_c-0.14 and E_c-0.05 eV, respectively. Slope of distribution (A) is same to that of (B), which means the same T_c and shape in log(*J*)-log(*V*), as can be seen in Fig. 5.3. The trap distribution marked with (C) corresponds to applied voltages greater than 0.6 V. At this high voltage region, currents deviate from those of the exponential trap distribution case, corresponding to region IV in Fig. 5.14. Change in slope between two distributions (B) and (C) implies that contributions of other conductions could be possible. This is because quasi-Fermi level E_F expresses steady-state carrier concentration of conduction band, which is not likely to be affected by emission-limited process. In other words, leakage current can increase with applied voltage without a significant increase in the

carrier concentration. This is qualitatively in agreement with the result that Schottky conduction is responsible for the leakage currents at high applied voltage: regions (V) and (VI) in Fig. 5.10, and regions (IV) and (V) in Fig. 5.14.

Regarding fit (B), obtained trap density is around 10^{20}/(cm^{3}eV), which is in consistent with that calculated from the common intersection points suggested by Sussman and Gould. Small discrepancy exists, but is in good agreement because differential method has a factor-of-two inaccuracy [57].

From the linking of two distributions of low and high level currents, we expect that localized trap levels exist at E_c-E_F=0.28V, which corresponds to V_{TFL} shown in Fig. 5.10. These localized trap levels act as single trap level, which results in the vertical jump in current for the case of low leakage current as shown in Fig. 5.10.

Finally, it should be noted that trap density of low leakage current is greater than that of high leakage current and this behavior is expected by SCLC theory.

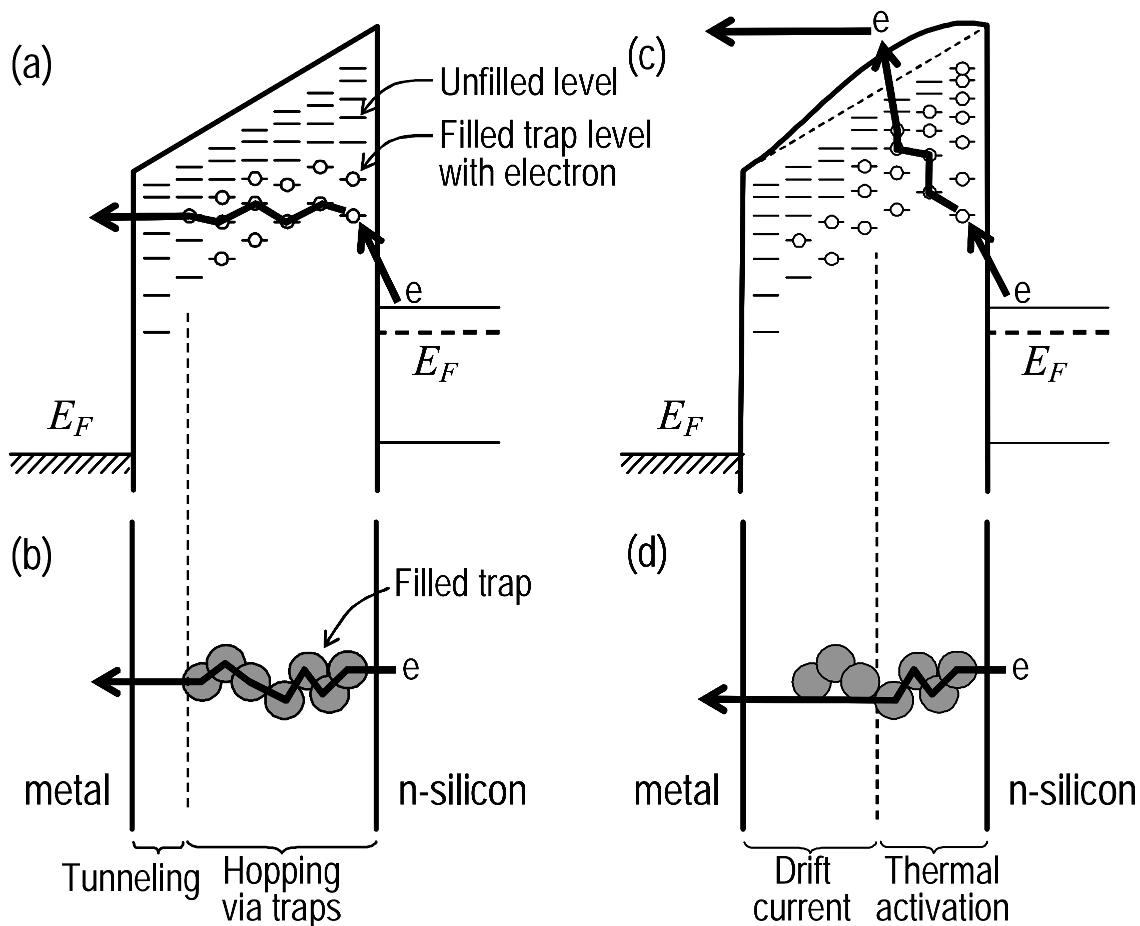


Fig. 5.20 Schematic drawing of SBD ((a) and (b)) and SCLC ((c) and (d)) processes. (a) and (c) describe SBD and SCLC processes, in energy, respectively. (b) and (d) correspond to (a) and (c), in space, respectively. Al metal gate and n-type silicon substrate are assumed. Thick arrowed lines express schematic electron conduction path. Spheres in (b) and (c) represent the traps filled with electron. Fermi-level difference corresponds to applied gate bias (V_g>0) with zero flat-band voltage. Traps are assumed to be exponentially in energy from the conduction band edge, as depicted in (a) and (c).

5.10 SBD and SCLC♣

Fig. 5.20 shows a schematic drawing of SBD and SCLC processes, which can give us a better understanding on the difference between SBD and SCLC processes. Fig. 5.20(a) and (c) illustrate SBD and SCLC conduction processes, respectively in energy. Fig. 5.19(b) and (d) describe the same processes in space. Charge transport after analog SBD can be explained in terms of a number of conduction mechanisms such as junction-like conduction, variable-range hopping, percolation model, tunneling, and quantum-point contact models.[a] Among the various models proposed, one of the closest models to SCLC conduction is believed to be the percolation model, since two processes are involved with large trap sites. As first suggested by Houssa et al,[b,c] SBD can be caused by a critical number of traps forming a percolation path. When the critical number of traps exists in the film, a percolation path can be connected between cathode and anode, leading to a sudden increase of the current. Before complete connection, percolation path can be viewed as illustrated in Fig. 5.20(a) and (b).

This situation is similar to the model suggested by Lee et al.,[d] who explained SBD in terms of local physically-damaged-region (LPDR) and direct tunneling at the LPDR. As shown in Fig. 5.20(a) and (b), which illustrates the situation before the complete connection of percolation path, i.e., the sudden increase of gate current, the current by SBD due to percolation and LPDR models can be composed of carrier

♣ This section is not included in the published paper.
a E. Miranda and J. Sune: Microelectronics Reliability 44 (2004) 1.
b M. Houssa, T. Nigam, P. Mertens, and M. Heyns: J. Appl. Phys. **84** (1998) 4351.
c M. Houssa, T. Nigam, P. Merens, and M. Heyns: Appl. Phys. Lett. 73 (1998) 514.
d S. Lee, B. Cho, J. Kim, and S. Choi: IEEE Tech. Dig. Int. Electron Devices Meet. (1994) 605.

injection into the dielectric thin film, hopping conduction near the injecting electrode, and tunneling conduction.

On the other hand, components of SCLC conduction are carrier injection to the thin film, thermal activation of charges to carrier conduction band, and drift current, as illustrated in Fig. 5.20(c) and (d). The carrier injection of SCLC can also be achieved by the formation of ohmic contact (Mott-Gurney contact) at the injecting electrode, which is the basic requirement for the bulk-limited conduction process.[a] However, thermal equilibrium concentration of electrons in the conduction band of the oxide film seems to be insufficient to support large gate leakage current, since carrier concentration in thermal equilibrium in dielectrics is small.[b] In addition to thermal injection, Schottky conduction can be responsible for the carrier injection at low applied voltage. This is because Schottky conduction is dominant at low oxide field region[c,d] and frequently observed in conduction of Lanthana films. What is more, in case that insulator film has large traps near to the injecting electrode, thermal injection of carriers to neighbor trap sites with a limited distance is known to be more efficient.[e,f] Moreover, if there are La-Si silicide bonds close to the substrate, they may play a role of providing injection path with low activation energy, since high metal concentration to oxygen concentration leads to silicide bonds at the interface between Lanthana and silicon substrate, which in turn becomes high interface trap density at the interface, as

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[a] J. Simmons: *Handbook of Thin Film Technology*, eds. L. Maissel and R. Glang (McGraw-Hill Book Company, 1970), Chap.14.

[b] W. Kingery, H. Bowen, and D. Uhlmann: *Introduction to ceramics*, (John Wiley & Sons Inc., 1976) 2nd ed., Chap.4 Structural Imperfections.

[c] F. Chiu, J. Wang, J. Lee, and S. Wu, "Leakage currents in amorphous Ta_2O_5 thin films," 81(10), 6911-15 (1997).

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[e] Y. Gartstein and E. Conwell: Chem. Phys. Lett. 255 (1996) 93.

[f] V. Arkhipov, E. Emelianova, Y. Tak, and H. Bassler: J. Appl. Phys. 84 (1998) 848.

HfO_2 [a]. These processes can lead to a small barrier height for carrier injection, which is clearly less than the barrier height originated from the carrier conduction band difference between the insulator and the silicon substrate. This is because trap energy levels distribute in the band gap of the oxide film and have a tail distribution which is closer to the Fermi level of the injecting electrode. As a result, we can propose trap-assisted thermal injection to the conduction band of the dielectric film, as being the first step of SCLC conduction, as illustrated in Fig. 5.20(c). Trap levels in the film and at the interface to the injecting electrode can support a multi-step jump with a small thermal activation energy. Moreover, it has been reported that shallow trap levels from the conduction band edge are difficult to be filled by the injected electrons.[b] This thermal emission is illustrated in Fig. 5.20(c) and also supports trap-assisted thermal injection of carriers to the insulator carrier conduction band. After reaching to the carrier conduction band, carriers can flow with electric field in the film. The electric field is induced by the linear combination of ohmic field and space-charge-induced field, according to SCLC theory [c,d,e]. Therefore, the main difference in carrier conduction between SBD and SCLC is considered as being in the conduction path energetically: conduction after SBD is associated with trap energy levels near quasi-Fermi level in the film, whereas SCLC conduction is involved with carrier conduction band of the film. Considering that carrier conduction via traps varies in magnitude with cross-sectional area and length of the connected traps while carrier conduction via carrier conduction band is uniform, we can speculate that gate current obeying SCLC conduction has an

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a **H. Wong**, K. Ng, N. Zhan, M. Poon, and C. Kok,, "Interface bonding structure of hafnium oxide prepared by direct sputtering of hafnium in oxygen," J. Vac. Sci. Technol. B, 22(3), 1094-1110 (2004).
b C. Sah: Solid-State Electronics 33 (1990) 147.
c M. Lamp ert and P. Mark: *Current Injection in Solids* (Academic, New York, 1970).
d D. Lamb: *Electrical Conduction Mechanisms in Thin Insulating Films* (Methuen and Co. Ltd., London, 1967).
e K. Kao and W. Hwang: *Electrical Transport in Solids* (Pergamon Press, Oxford, 1981).

almost same voltage at the abrupt current jump, single step jump, same current magnitude after the jump, and the same square-law dependence of current on voltage after the jump, in general.

5.11 Conclusion

Leakage current conduction mechanism of the *ex-situ* dry-nitrogen annealed La_2O_3 thin films were analyzed based on SCLC theory. It was found that SCLC and Schottky conductions are the major mechanisms of the leakage conduction. Trap densities in the oxide band gap composed of both exponential and localized distributions were extracted by using of the differential method.

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Chapter 6. Gate Leakage Current Variation of Lanthana MOS Capacitor[c]

6.1 Introduction

6.2 Experimental

6.3 Spectroscopic ellipsometry characteristic and TEM micrograph

6.4 Capacitance characteristic

6.5 Leakage current characteristic

6.6 Conclusion

Reference

[c] This chapter is based on the **accepted** paper: Yongshik Kim, Shun-ichiro Ohmi, Kazuo Tsutsui, and Hiroshi Iwai, "Analysis of Variation in Leakage Currents of Lanthana Thin Films," Solid-State Electronics 2005.

6.1 Introduction

Lanthana (La_2O_3) thin film of the rare earth oxides (REOs) is being focused for the gate dielectrics of MOSFET in the next generation of HfO_2 due to low leakage currents with sub-nm equivalent oxide thickness (EOT) region [1]. In fact, there have been several reports that Lanthana thin film has an outstanding low leakage current [2,3]. It is mandatory to understand the detailed conduction mechanism to ensure the low leakage current and the reliability. However, little is known about the mechanism. Recently, several studies have been made on the leakage currents of the film [2,3,4,5]. For the vacuum annealed Lanthana films, we reported that gate leakage currents are governed by the SCLC conduction [3].

Among the REOs, it has been reported that the conduction process of Nd_2O_3 can be explained by the space-charge-limited current (SCLC) theory with exponential or uniform trap distribution [6]. The SCLC mechanism relies on the trap density distributed energetically and spatially in the oxide film [7,8]. So far numerous attempts have been conducted to interpret the leakage current behavior of thin films within the frame of SCLC. Such films are: porous SiO_2 [9,10,11], TiO_2 [12], organic materials [13], porous silicon [14,15], SiO_2/Nitride [16], $SrTiO_3$ [17], and Ta_2O_5 [18]. In general, trap level distribution is described by one of the following ways: 1) discrete level [19], 2) exponential distribution [20], 3) Gaussian distribution [21], and 4) uniform distribution [7,20]. Since these trap density distribution are often diffused in nature and exponential trap distribution can express the other distributions by adjusting the two parameters of the trap density and the characteristic constant of the distribution, SCLC

with the exponential trap distribution can be useful as the first evaluation method [2,3].

Additionally, large density of trapping sites for electron has been reported in various deposited oxide films [22]. A local variation in the density of the trapping sites may be caused by an unoptimized deposition and/or following annealing processes. This could lead to the variation in the leakage current rather than in the capacitance, since the capacitance is relatively insensitive to the local defects in the film.

In this chapter, we report the result of detailed analysis in the conduction mechanisms of the as-deposited Lanthana films compared to *ex-situ* annealed films with nitrogen gas flow.

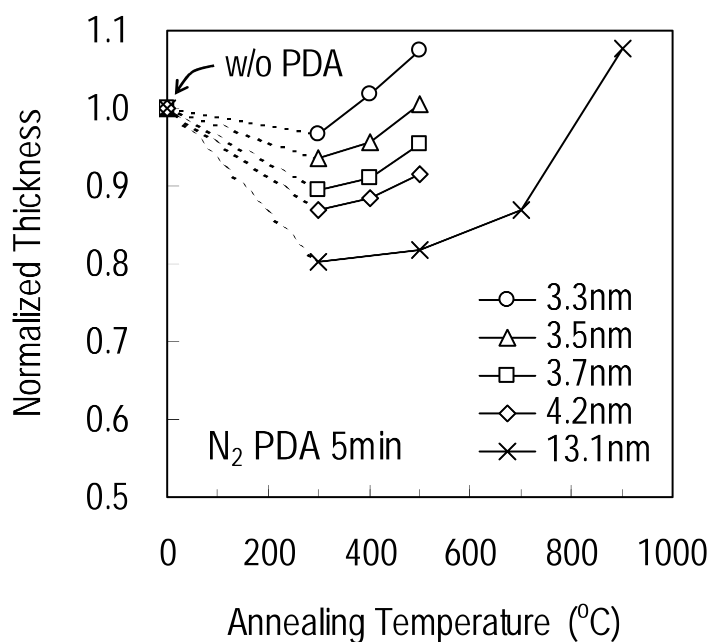
Lanthana (La_2O_3) films were deposited by E-beam evaporation on n-Si (100). Conduction mechanisms for the as-deposited film have been investigated. In order to study the annealing effect of the as-deposited films on the conduction mechanisms, some films were annealed in an ex-situ way at different temperatures with nitrogen or oxygen gas flow for 5 min. From current-voltage measurement of the as-deposited films, extremely low gate oxide leakage currents were observed while some films showed variation in the scale of the currents. It is shown that all the currents of as-deposited films obey the same conduction mechanisms irrelevant of the magnitude of the leakage currents. From the electric field and temperature dependences of the currents of the gate oxide, it is shown that the main conduction mechanisms are the space-charge-limited current (SCLC) at low oxide field region and Fowler-Nordheim (F-N) conduction at high oxide field region. It is also shown that conduction mechanisms of the nitrogen annealed films were basically the same as those of the

as-deposited films although the magnitude of the conduction current and flat-band voltage (V_{FB}) are different.

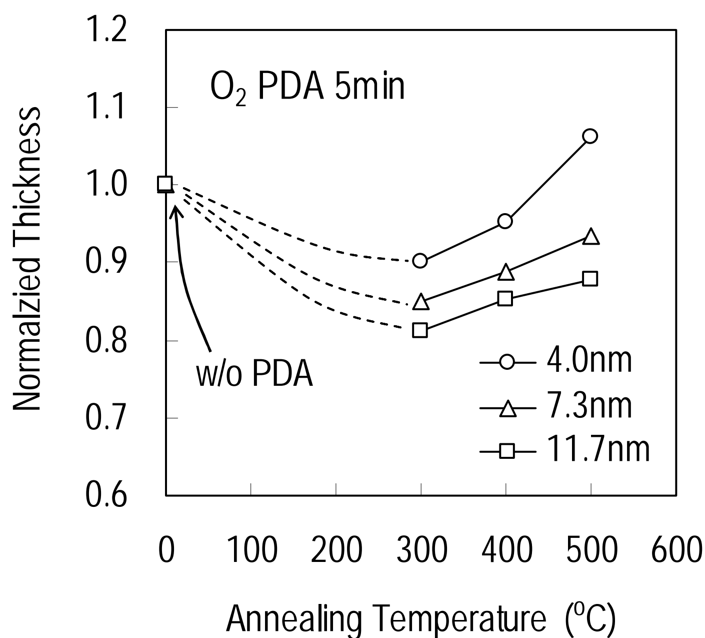
6.2 Experiment

Lanthana thin films were deposited on HF dipped n-Si (100) substrate (ph-doped, 0.8-1.2 Ωcm) by E-beam evaporation at 250°C using MBE equipment. The pressures in the chamber before and during depositions were about 10^{-10} and 10^{-9} Torr, respectively. Then, wafers were annealed in the rapid thermal annealing (RTA) chamber with a flow of 1.2 liter/min of dry-nitrogen or oxygen gas (99.999% purity). Annealing was carried out during 5 min at various temperatures. Gas lines and RTA chamber were carefully vacuumed to avoid diffusion of oxygen gas into the films prior to the nitrogen annealing. An exposure time to the air before annealing was kept less than 1 hour. After post-deposition anneal (PDA), the top gate electrode of metal dot was formed by metal evaporation with a metal shadow mask using bell-jar type evaporator at about 10^{-5} Torr. The bottom electrode for MOS capacitor was formed by the same metal evaporation method, on the backside of the silicon substrate. Capacitance vs. gate voltage (C-V) and gate oxide leakage current vs. gate voltage (J-V) measurements were performed using a HP4284A multi-frequency LCR meter and a HP4156C Semiconductor Parameter Analyzer. The ramp-up speed of gate voltage in J-V measurement was 10 sec/V to achieve steady-state of the oxide leakage current since occupied trap level with electron have a release time depending on trap level [7]. For all I-V experiments, a positive bias was applied on the gate, so that electrons were injected from the silicon substrate into the film. Typical electrical results were taken

from 50 to 200 samples for all fabrication conditions and their reproducibility was confirmed. The physical film thickness was optically extracted by Otsuka FE-5000 ellipsometer using a Cauchy model [23] and a single layer approximation. Incident angle was fixed to 70°. Photon energy varied from 1.55 to 4.14 eV for data fitting. Film thickness without PDA corresponds to the as-deposited film thickness.



(a)



(b)

Fig. 6.1. Normalized film thickness as a function of annealing temperatures for nitrogen (a) and oxygen (b) PDAs. Film thicknesses measured using spectroscopic ellipsometry were normalized with respect to that of as-deposited film.

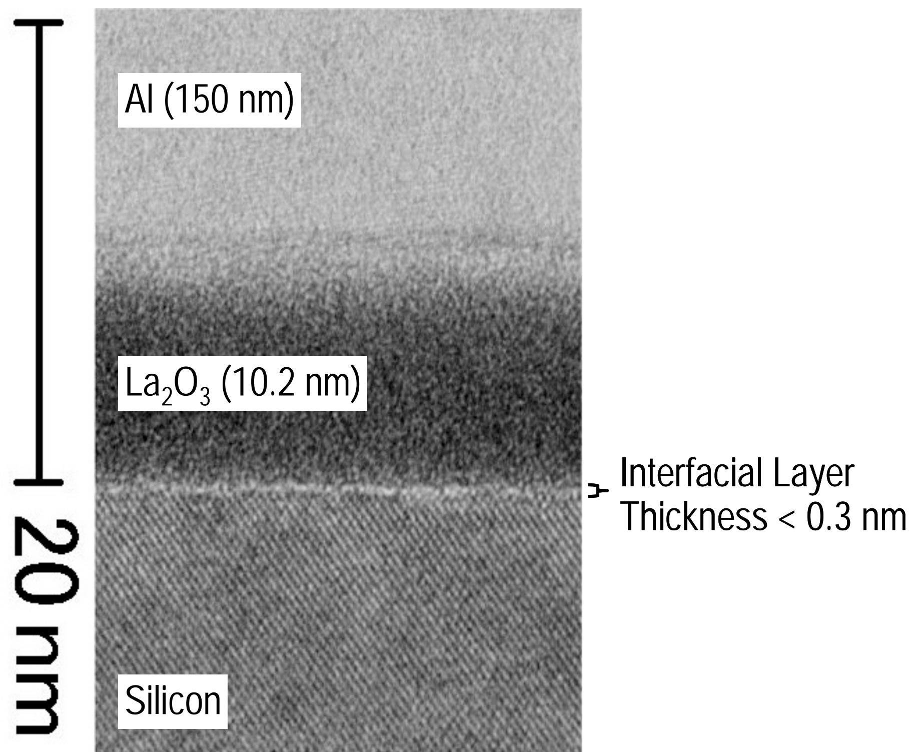
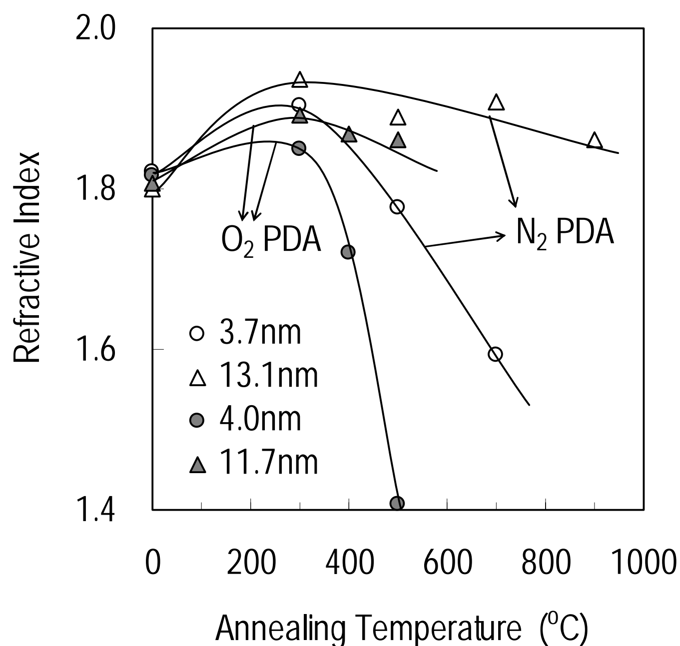
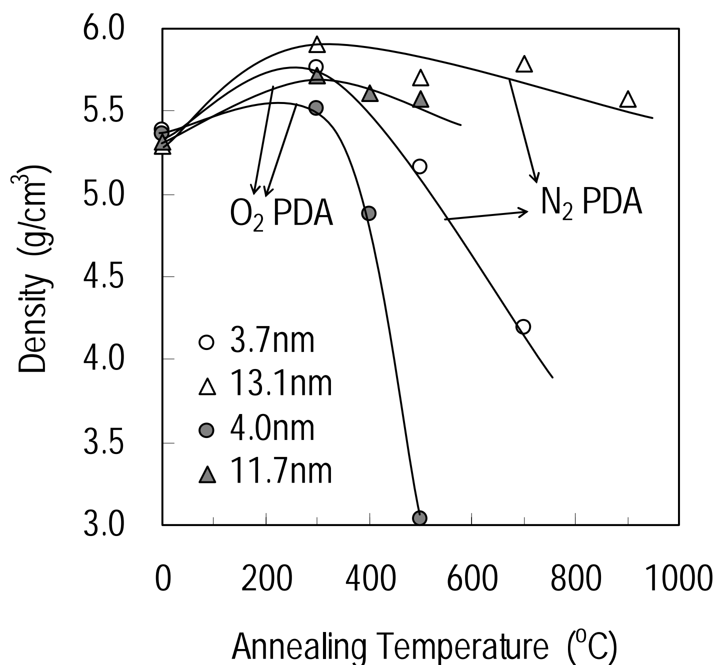


Fig. 6.2. High resolution transmission electron micrograph of the Lanthana film annealed at 300°C in nitrogen ambient. This film corresponds to the sample whose thickness for the as-deposited case is 13.1 nm, shown in Fig. 6.1. From the micrograph, Lanthana film thickness is 10.2 nm, which is consistent with the 10.5 nm from the spectroscopic ellipsometer.

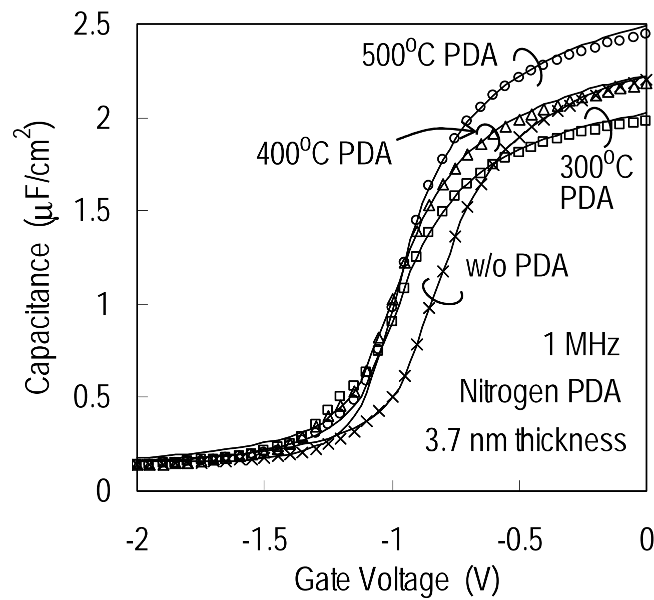


(a)

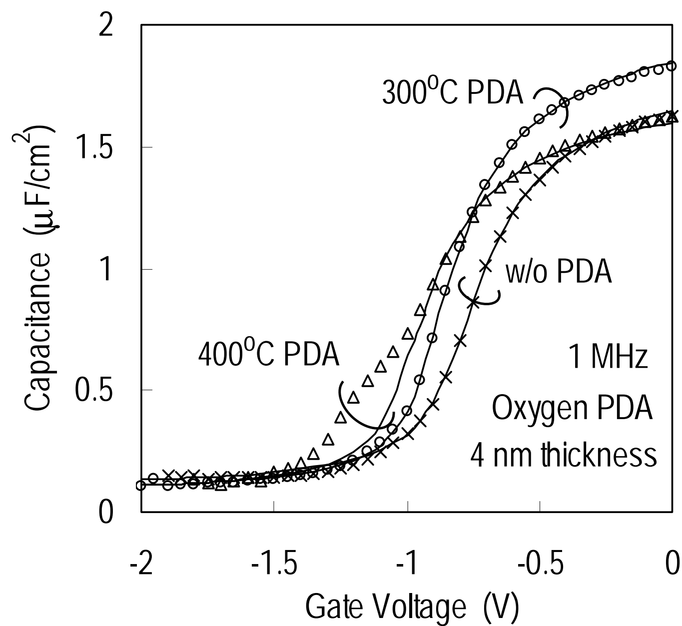


(b)

Fig. 6.3. Refractive index (a) and film density (b) obtained from the Lorentz-Lorenz relationship, as a function of the annealing temperature, for nitrogen and oxygen ambient PDAs. The refractive indexes were extracted by the Cauchy model at 4.14 eV (300 nm). Temperature 0°C corresponds to the as-deposited film case.

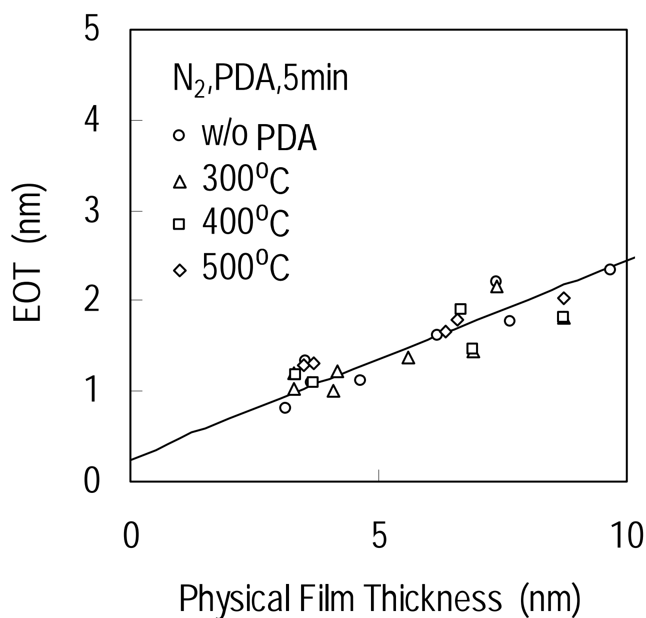


(a)

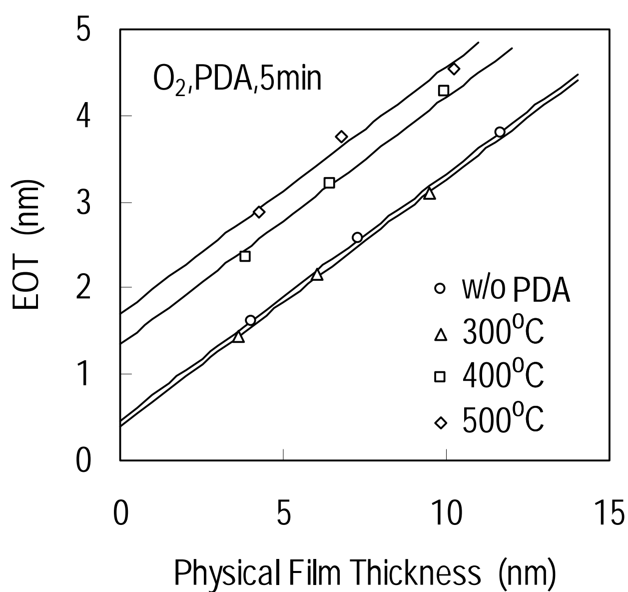


(b)

Fig. 6.4. High frequency PMOS capacitance as a function of gate voltage at 1 MHz for (a) nitrogen and (b) oxygen ambient PDAs. No frequency dispersion was observed at the frequency range from 1K to 1MHz. Symbols represent experimental results for films without PDA (cross), and with 300°C (circle), and 400°C (triangle) PDA temperatures. Solid lines represent theoretical values without consideration of interface state density using NCSU-CV program.



(a)



(b)

Fig. 6.5. EOT of Lanthana films as a function of the physical thickness without and with different PDA temperatures: (a) nitrogen ambient and (b) oxygen ambient. Solid lines are fits to symbols corresponding to the experimental results. Relative dielectric constants were found to be 17.7 and 13.6 for (a) nitrogen and (b) oxygen ambient PDAs, which was irrelevant of PDA conditions.

6.3 Spectroscopic ellipsometry characteristic and TEM micrograph

Fig. 6.1 shows normalized physical film thicknesses obtained by ellipsometry of various PDA temperatures with (a) nitrogen and (b) oxygen ambients. The normalization of the film thickness was carried out with respect to the as-deposited film thickness. With an application of PDA, the film thickness decreased, which indicates the film was densified, and remained practically constant when PDA temperature is less than 400°C for both nitrogen and oxygen ambiences. The structure of the Lanthana film annealed at 300°C in oxygen ambient was confirmed by High resolution electron micrograph (TEM). A typical image displays a fairly smooth interface between the substrate and the interfacial layer as shown in Fig. 6.3. It should be noted that the thickness of the interfacial layer is less than 3 nm, which implies that the interfacial layer can be minimized by the optimized the annealing condition. As PDA temperature increased further, however, the film thickness increased. This phenomenon was enhanced more for the case of thinner films, especially with oxygen PDA. This increase in the thickness can be explained in terms of interfacial layer growth between silicon and Lanthana films. Several studies have been reported that the interfacial layers were La-silicate without phase separation between silicon dioxide and Lanthana [24,25,27]. The origin of the interfacial layer growth is not understood at present, but is thought to be associated with silicon oxidation and/or La reduction processes near the interface. This view is reasonable because the interfacial growth was also observed for the case of ultra-high vacuum PDA [3]. Moreover, this reduction process is also known to be responsible for positive charge of the Lanthana

film [28].

Densification of the films with PDA temperatures can be evaluated by the film density obtained from the Lorentz-Lorenz relationship, in the similar fashion of SiO_2 thin film case [29]. From the refractive index n, the film density can be determined by the Clausius-Mossotti or Lorentz-Lorenz relationship [23].

$$\rho = K\frac{n^2-1}{n^2+2} \qquad \text{(Eq.6.1)}$$

where K is a constant, which can be evaluated using the values of bulk Lanthana. For Lanthana, n=2.08 and ρ=6.5g/cm^3 [30], then K=12.8. Refractive indexes measured by the spectroscopic ellipsometry and film densities determined from Eq. (1) are shown in Fig. 6.3. The refractive index (Fig. 6.3(a)) and the density (Fig. 6.3(b)) show maximum values at the annealing temperature of 300°C, irrespective of nitrogen or oxygen ambients and film thicknesses. The increase of the film density at 300°C compared to that of the as-deposited films indicates the densification. However, as annealing temperature increases further, the film density begins to decrease. This decrease of the film density could be due to the interfacial layer with a lower dielectric constant than the Lanthana film and the oxygen defects. The low dielectric constant of the interfacial layer is reasonable since the interfacial layer between the Lanthana film and the silicon substrate is reported as a silicate without a phase separation [24,25,26,27,28,30,31,32,33]. Then the dielectric constant of the silicate layer can be described by the general empirical relationship called the logarithmic mixture-rule [23]. This rule gives a value intermediate between the two extremes: one is when layers are parallel to the capacitor plates and the other is when layers are arranged normal to the capacitor plates. In other words, one can expect an intermediate dielectric constant of

the interlayer layer between the values of pure Lanthana film and SiO_2, from the logarithmic mixture-rule. The oxygen defects, causing positive fixed charges, are also reasonable because ΔV_{FB} is increased in the negative direction with higher annealing temperature, as shown in Fig. 6.6.

6.4 Capacitance characteristic

Fig. 6.4 shows typical C-V characteristic of the nitrogen and oxygen PDA films in the thinner film thickness case; physical thicknesses of the as-deposited film were 3.7 and 4.0 nm, respectively. Solid lines represent the theoretical capacitances with taking into account of quantum effect using NCSU-CV program [34]. One can see that solid lines exactly fit the experimental results, indicating that the interface state density is negligible for both as-deposited and 300°C PDA cases and becomes significant when PDA temperature increases to 400°C. This is more significant in the case of oxygen PDA.

Fig. 6.5 shows equivalent oxide thickness (EOT) as a function of physical film thickness for nitrogen (Fig. 6.5(a)) and oxygen (Fig. 6.5(b)) ambient PDAs. Intercept of fitted lines to vertical axis at zero film thickness, which describes interfacial layer thickness, is found to be non-zero. The EOT of the interfacial layer of as-deposited films was found to be 0.25 and 0.47 nm, as shown in Fig. 6.5(a) and 6-5(b) respectively. These values are in agreement with the physical thickness of the previous report [27,28] and comparable to the ZrO_2 case [35]. For the case of nitrogen ambient PDA, as shown in Fig. 6.5(a), the relation between the EOT and the physical thickness do not change significantly among the samples with non-PDA and different temperature PDAs.

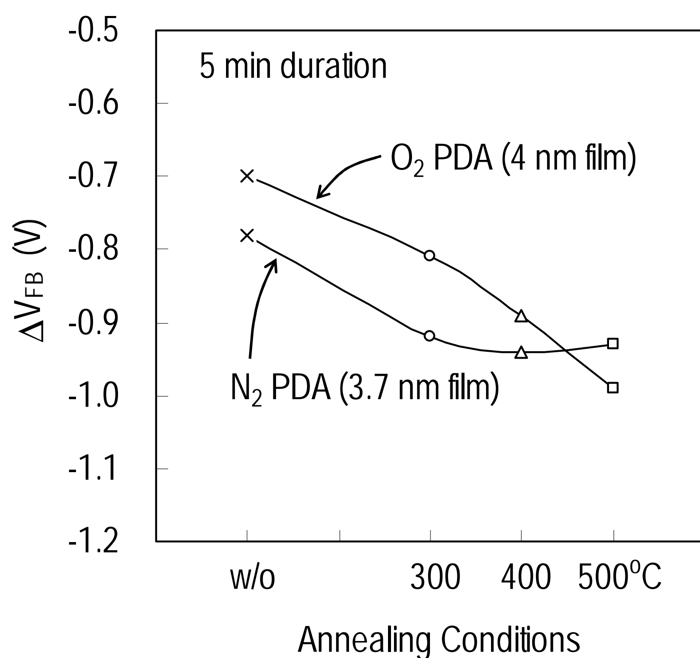
EOT vs. physical thickness plots distributed almost on the single line as shown in Fig. 6.5(a). This suggests that the interfacial layer thickness does not change by increasing annealing temperature up to 500°C. On the other hand, for the case of oxygen ambient PDA, as shown in Fig. 6.5(b), EOTs were increased with an increase of PDA temperature and fitted to linear lines with an equal slope. Intercepts to the vertical axis, corresponding to the interfacial layer thickness, increased with increase in PDA temperature. The slope of the EOT vs. physical thickness plot corresponds to the dielectric constant of the Lanthana film itself above the interfacial layer. The same slopes with different PDAs and non-PDA suggest that PDA does not alter the Lanthana dielectric constant but result in the growth of the interfacial layer. Additionally, small deviation of EOT vs. the physical film thickness for the nitrogen PDA might be the result of uncontrolled very small content of oxygen gas in the nitrogen ambient.

Fig. 6.6 shows flat-band voltage shift (ΔV_{FB}) as a function of PDA temperature (Fig. 6.6(a)) and physical film thickness (Fig. 6.6(b)). ΔV_{FB} increased in the negative direction with increase in PDA temperature for the case of oxygen PDA, while became saturated for the case of nitrogen PDA, as shown in Fig. 6.6(a). From the relation of ΔV_{FB} with the film thickness as shown in Fig. 6.6(b), both nitrogen and oxygen PDAs at 300°C decrease the physical thickness and increase the $|\Delta V_{FB}|$. Higher temperature PDA above 300°C with oxygen ambient leads to the increase in the physical thickness and $|\Delta V_{FB}|$. On the other hand, the nitrogen PDA results in the very small increase in the both physical thickness and $|\Delta V_{FB}|$. Therefore, densification and ΔV_{FB} are found to be trade-off, and PDA temperature less than 400°C is believed to be the optimized condition for achieving the film densification and the minimum of $|\Delta V_{FB}|$.

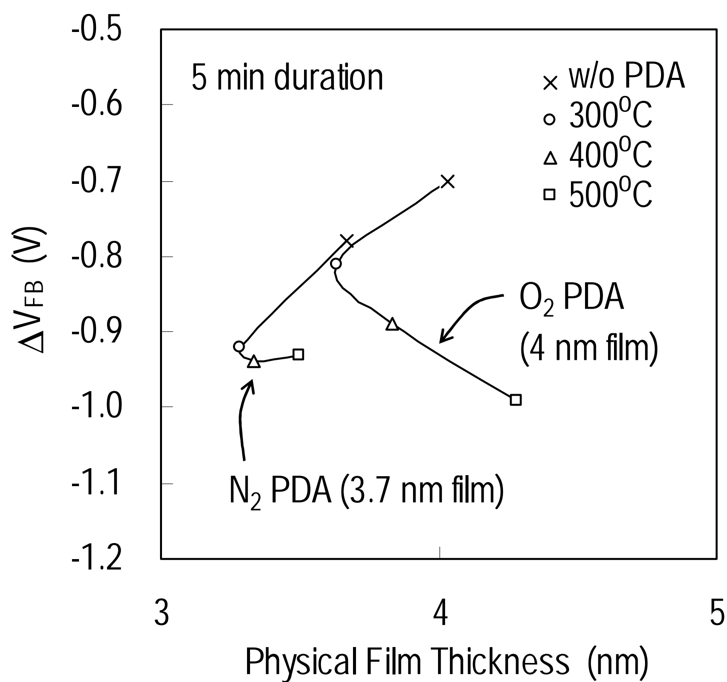
If the total or part of the Lanthana film is oxidized at higher annealing temperature in the oxygen ambient, the number of oxygen defects will be decreased and then $|\Delta V_{FB}|$

will be decreased. This is because negative ΔV_{FB} and positive fixed charges are mainly caused by oxygen defects [3]. However, this is contrary to the results shown in Fig. 6.6(a)

Additionally, low temperature annealing is requited to suppress the interfacial layer growth, as depicted in Fig. 6.1. In fact, the excellent low leakage current was observed at 200°C PDA with nitrogen ambient [2].



(a)



(b)

Fig. 6.6. Flat-band voltage shift (ΔV_{FB}) as a function of (a) PDA temperature and (b) physical film thickness. Symbols represent experimental results of different PDA temperatures: w/o PDA (cross), 300°C (circle), 400°C (triangle), and 500°C (square) PDAs.

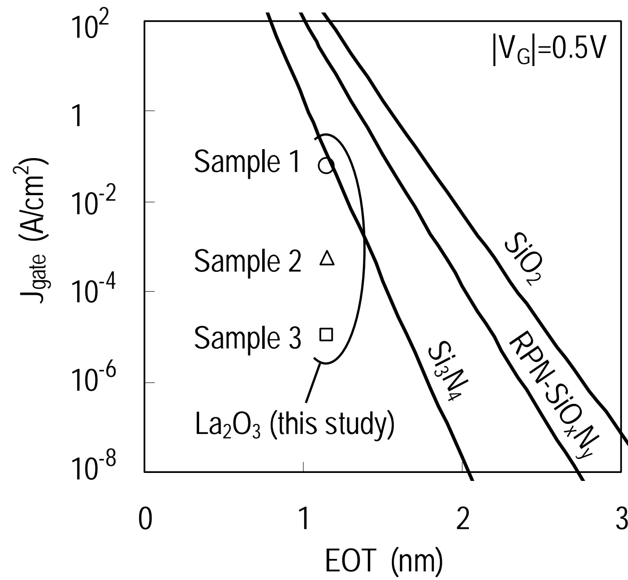


Fig. 6.7. Gate leakage currents of Lanthana samples 1, 2, and 3 in comparison to the theoretical direct tunneling currents of SiO_2, nitrided SiO_2, and Si_3N_4. Data for SiO_2, nitrided SiO_2, and Si_3N_4 are taken from Ref. 6-1 and re-calculated at $|V_g|$=0.5V to avoid the comparison of F-N tunneling region. Annealing after Lanthana film deposition was not carried out. Relative dielectric constant and V_{FB} of the Lanthana films were found to be 13.6 and -0.64 V, respectively.

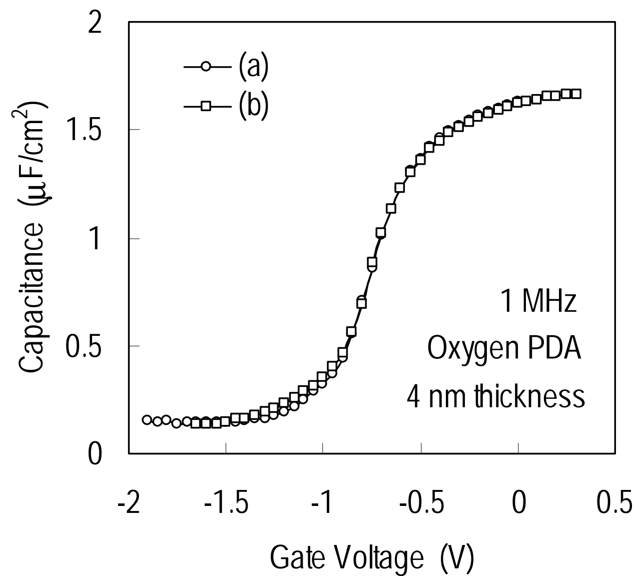
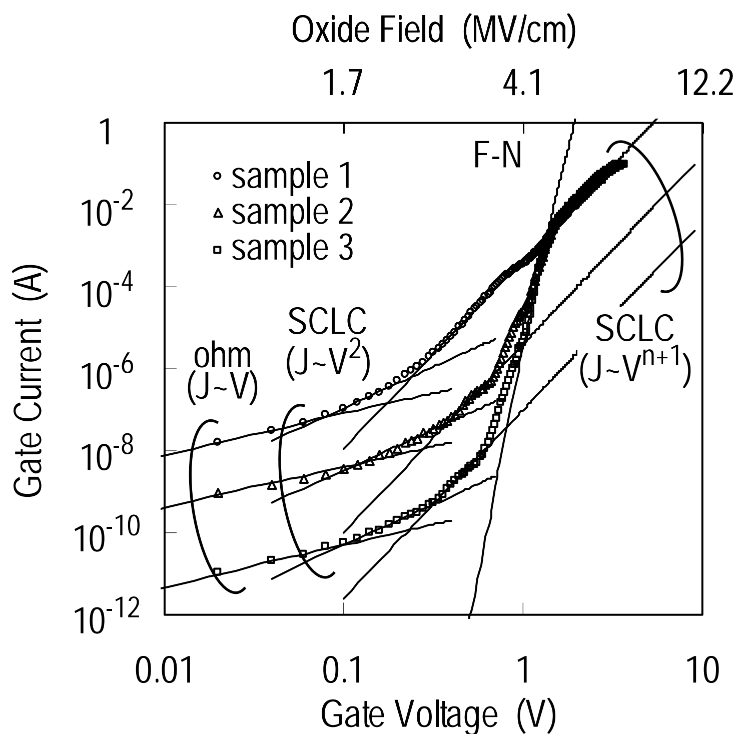
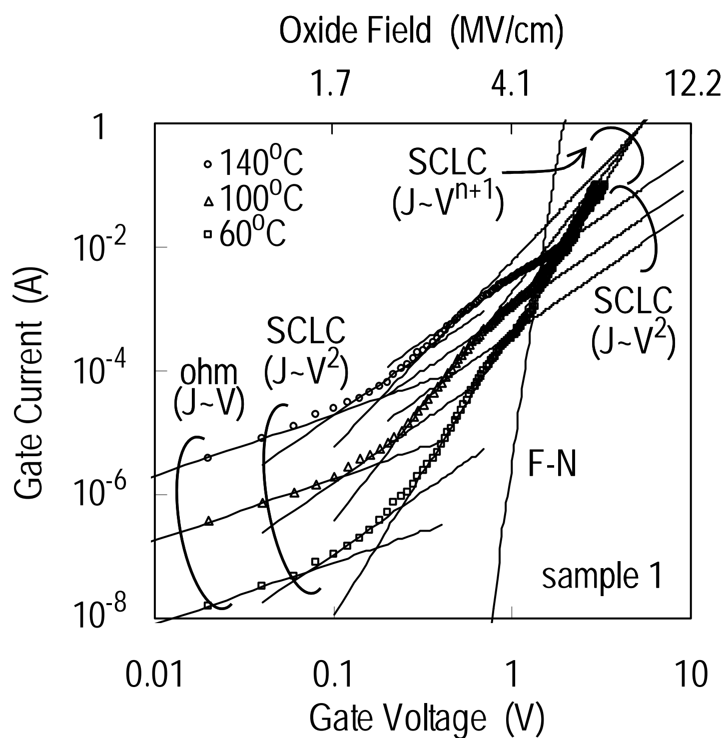


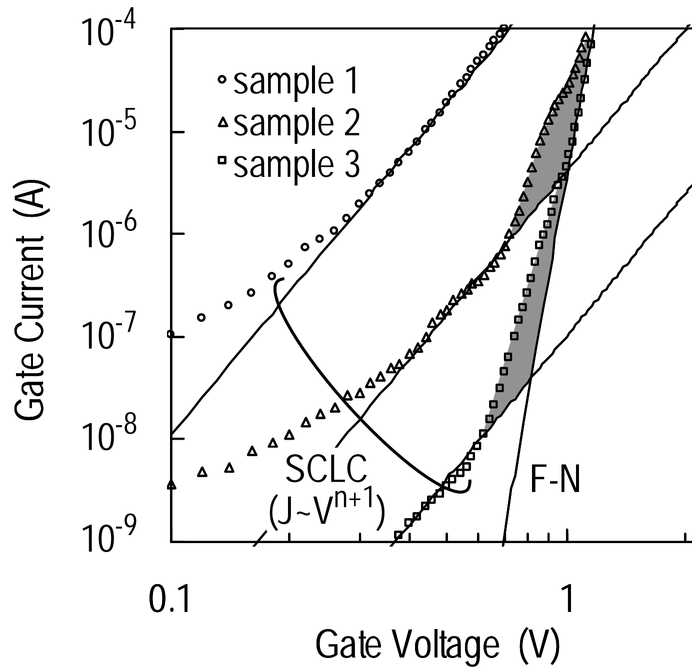
Fig. 6.8. High frequency PMOS capacitance as a function of gate voltage at 1 MHz. Films (a) and (b) are fabricated at the same time with the films shown in Fig. 6.7. Negligible sample-to-sample variation in the capacitance was observed.



(a) leakage current vs. gate voltage at 60°C, for three different samples on the same chip



(b) leakage current vs. gate voltage at different measurement temperatures for sample 1 of (a)



(c) Discrepancy, marked with shade, between experiments and F-N conduction.

Fig. 6.9. Gate leakage current of 4 nm film of Al gate electrode, as a function of gate voltage. Samples correspond to those shown in Fig. 6.7. Solid lines are the best fits to experimental results. Conduction models and current-voltage relation are described near the fitted lines. Gate area is 3.14×10^{-4} cm^2. Symbols in (a) correspond to experimental results of three samples showing variation in the currents at 60°C. Symbols in (b) correspond to the one sample marked with sample 1 in (a) at different measurement temperatures. Power term n of gate voltage of (a) is 3.6 for three samples. n powers in (c) are 3.6, 2.7, and 2.0 at 60, 100, and 140°C measurement temperatures, respectively.

6.5 Leakage current characteristic

Fig. 6.7 shows gate leakage currents of three Lanthana samples as a function of EOT in comparison to other dielectrics, such as SiO_2, nitrided SiO_2, and Si_3N_4. Three Lanthana samples have the same Al gate electrode on the same chip, which means that they are fabricated on the same chip at the same time. One can see that leakage current of the sample 3 is much lower than the theoretical tunneling currents of other dielectrics, whereas there is a significantly large variation in the magnitude of the leakage currents in the case of samples 1 and 2. The physical thicknesses of all the three samples are found to be 4 nm and the same from the exactly same C-V curves of the samples as that shown in Fig. 6.8.

Fig. 6.9 shows leakage current vs. gate voltage at 60°C, for three different samples which correspond to the samples shown in Fig. 6.7. From the fact that the leakage currents of all the three samples are the same in the gate voltage region above 1 V where Fowler-Nordheim (F-N) mechanism governs, it is also found that the physical film thickness of the three samples are the same. It should be also noted that the interface state density seems to be negligible from the comparison between experimental and theoretical C-V curves as depicted in Fig. 6.4(b).

The conduction mechanisms responsible for the three samples, however, were found to be essentially same, and associated with ohmic, SCLC, and F-N conductions. According to SCLC theory [7,8,36], the J-V characteristics should initially be ohmic ($J \sim V$) at low gate voltage as shown in Fig. 6.9(a). Following the ohmic region, currents fitted with the square gate voltage law ($J \sim V^2$) as shown in Fig. 6.9(a) and governed by SCLC. After the currents governed by the square gate voltage, currents

were found to be associated with the n power law of J-V relation ($J \sim V^{n+1}$) as shown in Fig. 6.9(a). n was found to be 3.6 for all the three samples. This power law relation of J-V can be explained by the exponential trap distribution case of SCLC [7,8]. The SCLC with the exponential trap distribution was also suggested by the temperature dependency as shown in Fig. 6.9(b). According to Sussman [37], the extrapolations of the fitted lines corresponding to the SCLC conduction of the exponential trap level distribution, with different temperatures, meet at the single point as shown in Fig. 6.9(b). This is a good indication of SCLC with the exponential trap distribution. Since ohmic and SCLC conductions are closely related to the oxide trap density, the variation of the leakage current could be associated with the variation of the trap density. Traps are thought to be introduced during the PDA because the ΔV_{FB} of the annealed film is more negative than the as-deposited film case, as shown in Fig. 6.6(a). Furthermore, it can be suggested that the traps can be generated by the deposition process (evaporation process) itself because the equilibrium vapor pressure of La is greater than that of Lanthana at the same temperature [38]. When Lanthana source is heated enough by e-beam, La atoms, as well as Lanthana molecules, can be evaporated and deposited to the silicon substrate. These La atoms in the film can function as positive charges.

When the gate voltage is around 1 V corresponding to 4.1 MV/cm, F-N conduction occurred. The barrier height, defined as the energy difference of the conduction band edges between Lanthana film and silicon substrate, was found to be 2.14 eV with 0.26 effective mass [1]. This barrier height is closer to the theoretical value 2.3 eV of Lanthana film, rather than 3.1 eV of SiO_2 [1]. This means that the interfacial layer is transparent for tunneling because it is too thin, which is consistent with the report on the Schottky diode where the oxide interfacial layer greater than 3 nm looses its

effectiveness [39]. The F-N conduction at high oxide field region is consistent with the previous result [4]. It should be noted that the currents of the three samples become exactly same at high voltage region and governed by the same F-N conduction. This clearly indicates that conduction process associated with the currents at high gate voltage region can be different from those associated with variation in the currents at low gate voltage region. In addition, the current variation is not originated from the film thickness non-uniformity which can be caused by silicon diffusion into Lanthana film [28]. On the other hand, experimental results deviate from SCLC and F-N conductions as shown in Fig. 6.9(c) marked with the shaded region. This can be explained in terms of the release of the trapped charge during the SCLC conduction, which is triggered by the high oxide field and the internal emission from trap levels into oxide conduction band. For this reason, the currents are enhanced greater than the sum of both SCLC and F-N conductions.

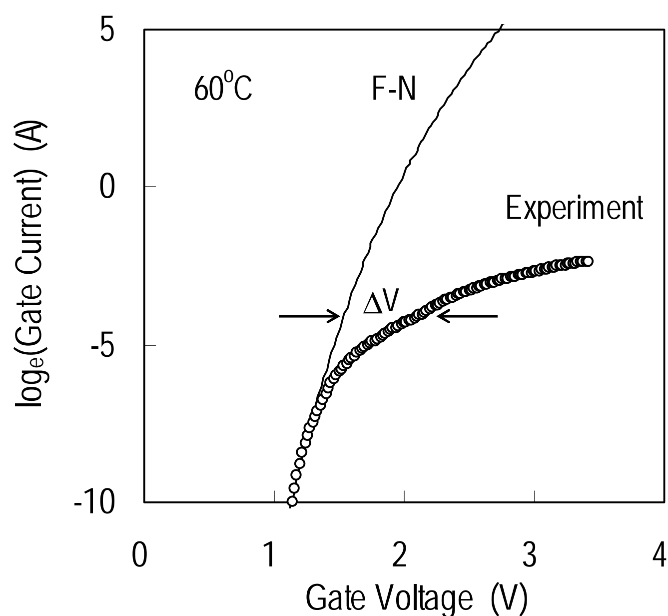
When the gate voltage is further increased over 1 V, currents becomes saturated. This is caused by a series resistance effect. The series resistance responsible for the saturation can be obtained by means of the graphical method [40]. Voltage drop (ΔV) from the ideal current of F-N conduction is defined as shown in Fig. 6.10(a). ΔV is plotted as a function of the leakage current as shown in Fig. 6.10(b) and the linear relationship was observed. Thus, the series resistance R_s can be determined from the slope of the straight line and found to be about 15 Ω.

Fig. 6.11 shows the gate leakage current characteristic of the film with 7 nm thickness, nitrogen PDA, and Pt gate electrode. It is found that conduction models except the F-N conduction are similar to those of the as-deposited films. The reason

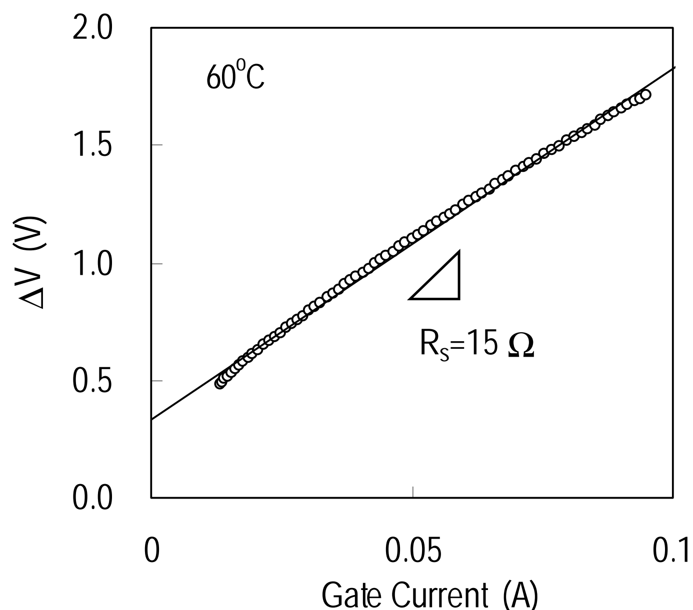
for the absence of the F-N conduction at the nitrogen annealed film is due to the lower oxide field, compared to the as-deposited film case, which comes from the difference in gate electrode materials.

6.6 Conclusion

The conduction mechanisms of the as-deposited and nitrogen-annealed Lanthana thin films were analyzed and compared. The conductions are found to be associated with the SCLC at the low oxide field region and the F-N current at the high field region. It is also found that the variation in the scale of the leakage currents at low oxide field is not caused by the film thickness non-uniformity and the interface-state density, but by the amount of traps incorporated during deposition and/or annealing. This is because the SCLC conduction, which is dominant at the low oxide field region, is determined by the trap distribution in the oxide film. From the barrier height of the F-N current, the thin interfacial layer seems to be ineffective to reduce the tunneling current.



(a) semilog plot of F-N and gate currents as gate voltage



(b) voltage deviation ΔV as gate current

Fig. 6.10. Graphical derivation of series resistance R_s associated with the F-N current at high gate voltage region shown Fig. 6.9(a). Voltage deviation ΔV of experiment from the theoretical F-N current was defined in (a). R_s was obtained from the slope of the linear line in (b).

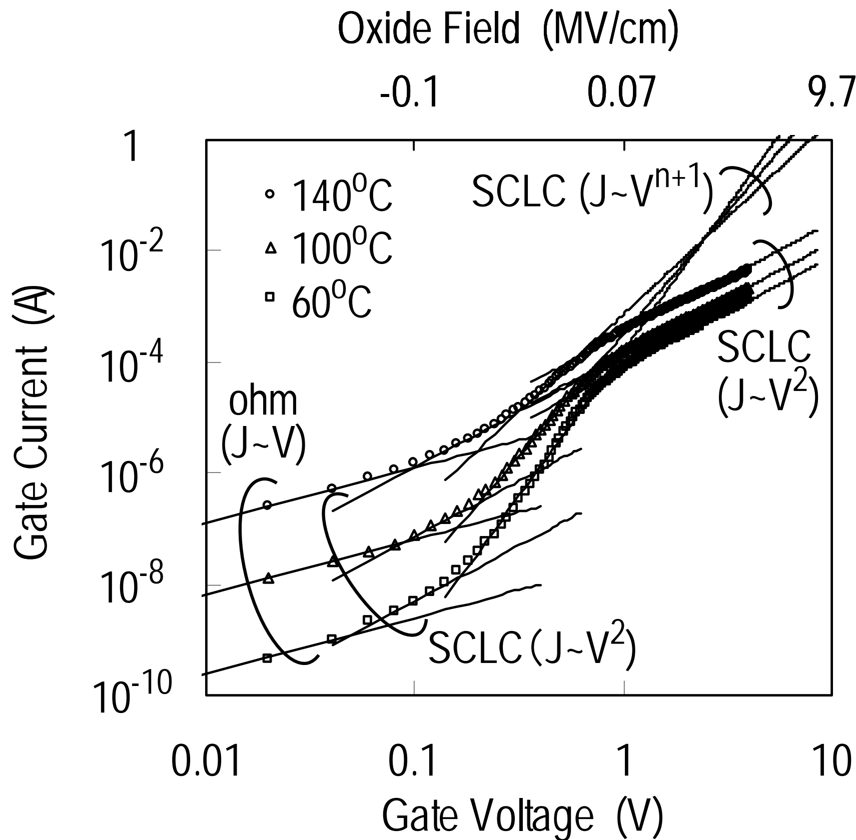


Fig. 6.11. Gate leakage current of 7.7 nm film of Pt gate electrode, as a function of gate voltage. The film was annealed with 400°C nitrogen PDA for 5 min. Relative dielectric constant and V_{FB} of the film were found to be 16.6 and 0.88 V, respectively. Gate area is 3.14×10^{-4} cm^2. Symbols correspond to experimental results of different measurement temperatures. Solid lines are the best fits to experimental results. Conduction model and current-voltage relation are described near the fitted lines. n powers of gate voltage are 2.5, 3.4, and 4.2 for 60, 100, and 140°C, respectively.

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Chapter 7. PDA Effect on Lanthana MIM Capacitor

7.1 Introduction

7.2 Experiment

7.3 C-V Characteristic

7.4 Typical J-V Characteristic

7.5 Conclusion

Reference

7.1 Introduction

Up to now, Lanthana MOS capacitors were evaluated for the C-V and J-V characteristics of the Lanthana film. Even though the Lanthana MOS capacitor has the small interface state density D_{it}, D_{it} can affect the conduction mechanism, such as interfacial state assisted tunneling conduction [1,2,3,4]. Furthermore, it is known that the frequency dispersion in C-V behavior comes mostly from the substrate resistance. With the metal substrate, we can evaluate the Lanthana film without the interface state density. This is because the metal substrate does not have the band gap like semiconductor, so that the carrier trapping and detrapping behavior does not occur. In other words, the interface state density between the Lanthana and metal are function of the metal Fermi level and the interface state is filled and emptied with the carrier from the carrier reservoir of the metal

This chapter includes the C-V and J-V characteristics of the Lanthana MIM structure.

7.2 Experiment

Silicon substrate was cleaned by HP dipping and Pt film was deposited by e-beam evaporation method. The deposited Pt film thickness was estimated as about 150 nm. Pt will react with the silicon substrate by the following heat process, making PtSi silicide. This silicide functions as the metal substrate with a low resistance. The background pressure during the depositions was $4x10^{-4}$ Pa. After marking of the

sample ID, the Si/Pt substrate was cleaned by the solution of H_2O_2 10ml and H_3PO_4 40ml to remove the organic contaminates. Lanthana films were deposited on the Si/Pt substrate as well as HF dipped n-Si (100) substrate (HF-last) by E-beam evaporation at 250°C using MBE equipment. The pressure in the chamber before and during depositions was about 10^{-9} Torr. Then, wafers were annealed in the RTA (Rapid Thermal Annealing) chamber with 1.2 liter/min flow rate of dry-nitrogen gas. Annealing was carried out for 5 min at various temperatures. Gas lines and RTA chamber were carefully vacuumed to minimize the oxygen gas prior to annealing. After annealing, Pt or Al electrode was formed. An exposure time to the air before gate metal deposition was less than 1 hour. C-V and J-V measurements were performed using a HP4284A multi-frequency LCR meter and a HP4156C Semiconductor Parameter Analyzer, respectively. The film thickness was confirmed by Otsuka FE-5000 ellipsometer.

7.3 C-V characteristic

Fig. 7.1 shows the typical C-V characteristic of the Lanthana MIM film structure. The measured capacitance was almost flat with respect to the applied gate voltage, which means that the carrier concentration with the gate voltage is small.

Fig. 7.2 shows transmission electron micrograph for the films annealed at 300°C and 700°C. One can see that the interfacial layer between Lanthana and PtSi substrate becomes thicker at higher PDA temperature. This point is also seen in Fig. 7.3 and 7-4. Higher PDA temperature leads to the lower capacitance and the dielectric constant. Compared to the MOS case, MIM structure has higher dielectric constant. Since the

top gate structure is same between the MOS and MIM structures, this is due to the difference in the substrate, which could result in the different deposition rate of the Lanthana film and the interfacial layer thickness. In the MIM films, the Pt gate electrode case shows higher dielectric constant than the Al gate electrode case. This could be associated with the reaction between Al and Lanthana, which creates the Aluminum oxide layer at the interface. For this reason, the capacitance of the Pt gate electrode is a little higher than that of the Pt electrode.

7.4 Typical J-V characteristic

Figure 7-5 shows the typical J-V characteristic of the Lanthana MIM structures. The films shown in Fig. 7.5 were deposited and annealed at the same time, so that the four types of J-V behavior correspond to the variation in the film property itself. This is true because the MIM structure gives very small parasitic resistance connected to the insulator. If the film is broken down at the deposition due to the various reasons, J-V will have ohmic conduction after a current jump of the hard breakdown case as depicted in Fig. 7.5(d).

Fig. 7.5 (a) and (b) show the discontinuous current at the almost same voltage. If the jump is originated from the soft breakdown, the voltage of the jump, the number of jump steps, and the current magnitude after the jump will show statistical fluctuation. However, Fig. 7.5 (a) and (b) show the small variation of the current jump and single step, although the current magnitude is different. To find the conduction mechanism, J-V relationship before and after the jump should be checked. Fig. 7.5 (a) and (b) show the same power law relationship of J on V: $J \sim V^2$. This means that the current

including the jump can be described by the SCLC theory. This point can be reasonable since the square law of J-V before and after the abrupt current increase is the case of localized trap levels in oxide band gap [5,6,7].

Figure 7-5 (c) shows the low leakage current compared to Fig. 7.5 (a) and (b). It should be noted that, at low voltage, current versus voltage relationship is same as those of Fig. 7.5(a) and (b). Instead of the current jump, gate leakage current is proportional to the 3 power of the gate voltage. This indicates that the trap level distribution is distributed exponentially energetically and not localized like in Fig. 7.5 (a) and (b), from the SCLC theory. At high voltage, F-N conduction governs the gate current. Since the F-N conduction is related to the band structure of the insulator film, is can be true that the film is relatively free from the localized defects and conducting path.

7.5 Conclusion

It is found that the capacitance of Lanthana film can be decreased by the reaction layer between metal gate and the Lanthana film, such as the Al gate case. Regarding the capacitance, Pt electrode is better than Al electrode in the capacitance of the Lanthana film.

It has been reported that gate leakage current of Lanthana MIM capacitor is dominated by the ohmic and SCLC conductions at low voltage and F-N conduction at high voltage. The abrupt current jump like soft breakdown is well explained by the SCLC theory. This suggests that the square law relationship of the gate leakage current on the gate voltage can support the SCLC conduction mechanism.

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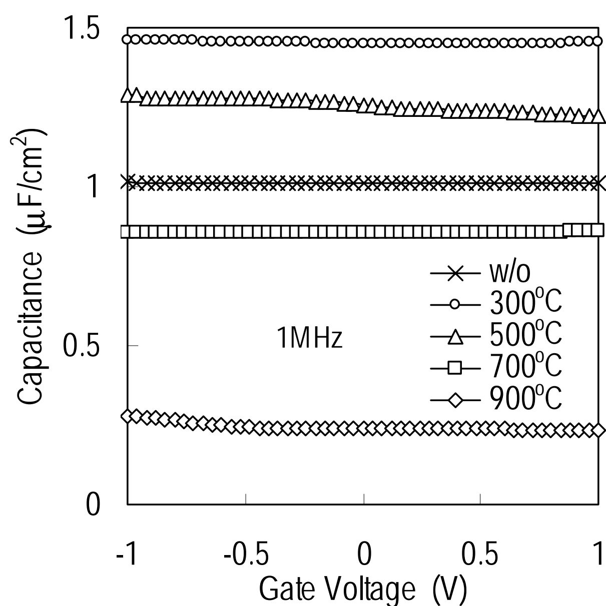


Fig. 7.1. Typical C-V characteristic of the MIM (Pt/Lanthana/PtSi) films, annealed at different temperatures compared to the as-deposited film. Capacitance was measured at 1 MHz. Gate electrode area was 3.14×10^{-4} cm^2.

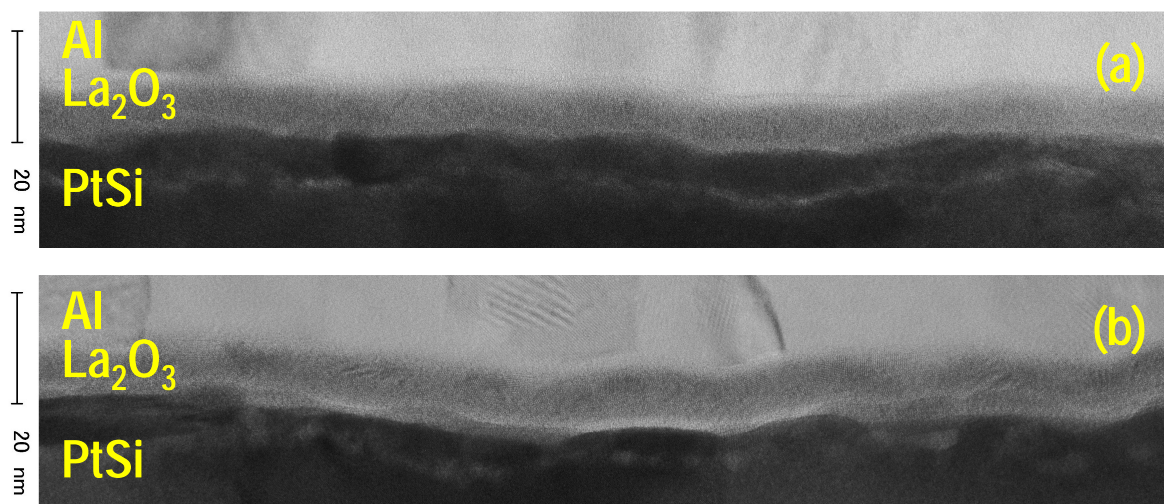
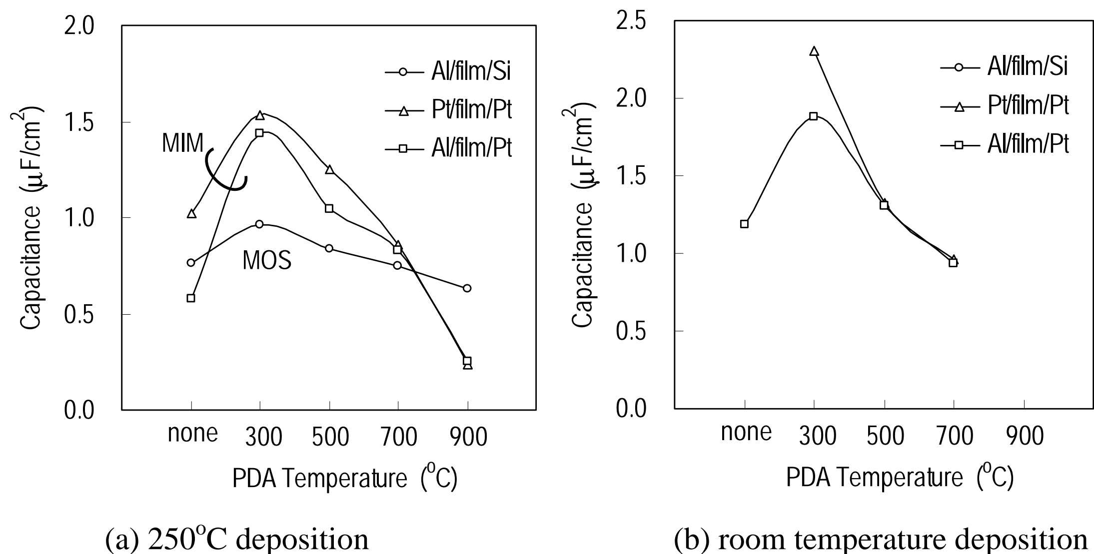


Fig. 7.2. TEM micrograph of the Lanthana MIM films annealed at (a) 300°C and (b) 700°C for 5 min in nitrogen ambient.



(a) 250°C deposition (b) room temperature deposition

Fig. 7.3. Capacitance as a function of PDA temperatures for the films deposited at (a) 250°C and (b) room temperature.

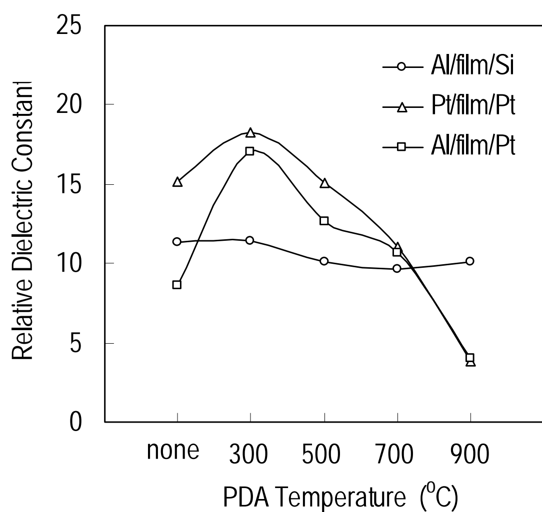


Fig. 7.4. Relative dielectric constant as a function of the PDA temperature. Films correspond to those in Fig. 7.3(a).

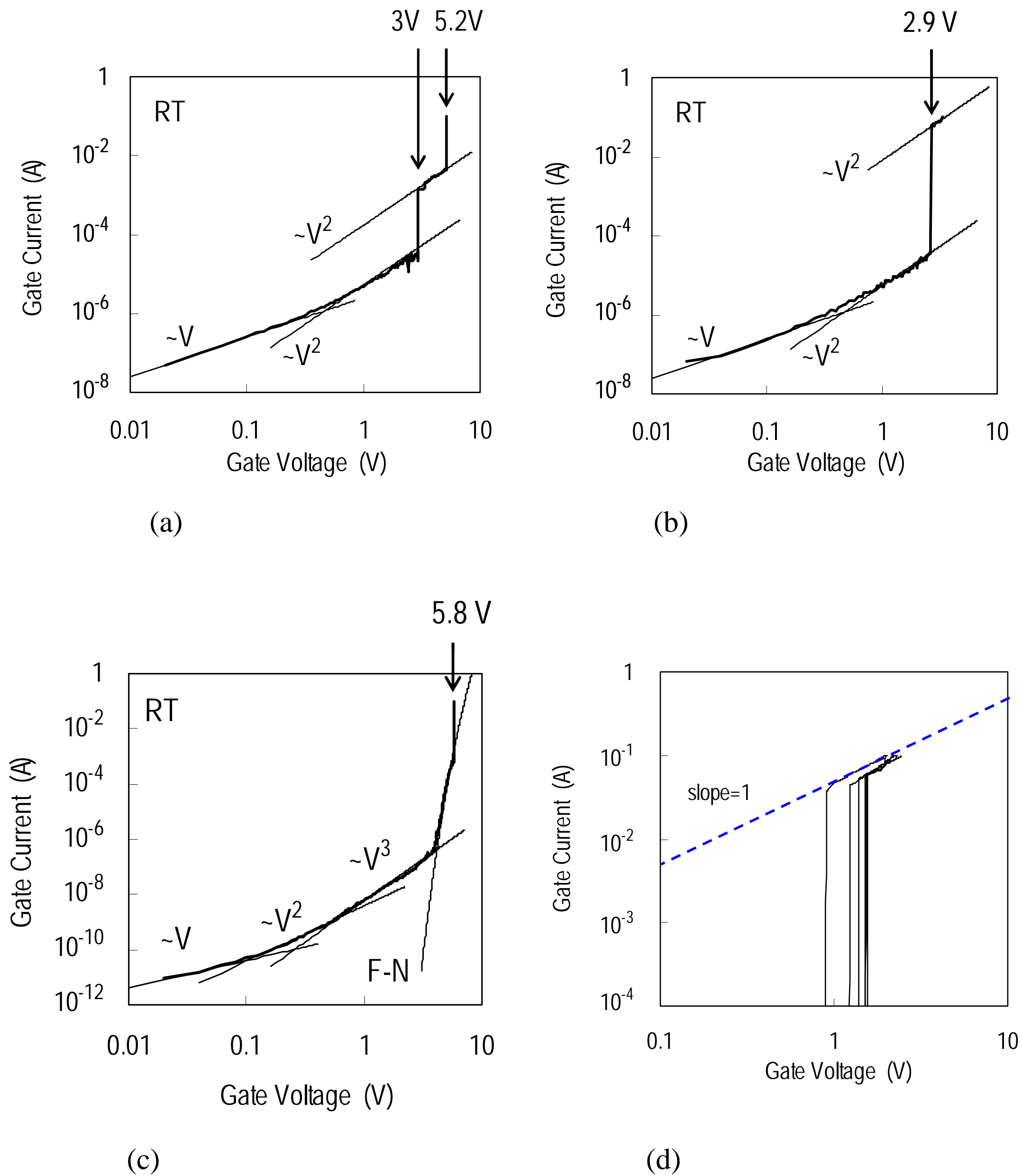


Fig. 7.5. Typical J-V characteristic of Lanthana MIM capacitor. Same are the fabrications for four films. The films were deposited and annealed with N_2,700°C PDA for 5 min, at the same time. Top and bottom gate electrodes are Al and Pt, respectively. Gate electrode area is 3.14×10^{-4} cm^2. (a) and (b) shows the abrupt current jumps while the current magnitude after the jump is different. (c) shows the low leakage current. (d) is the broken down case, which shows exact ohmic conduction after the current jump corresponding to the breakdown.

Chapter 8. Lanthana Gate Oxide MOSFET

8.1 Introduction

8.2 Experiment

8.3 Threshold voltage and drain current

8.4 Channel mobility

8.5 1/f noise

8.6 Conclusion

Reference

8.1 Introduction

Effective mobility and 1/f noise of Lanthana gate NMOSFET were compared to SiO_2 NMOSFET case. Lanthana gate transistor shows low subthreshold swing 85 mV/dec., well saturated drain current behavior, and high effective mobility 290 cm^2/V-s, comparable to SiO_2 case, although film trap density (N_{OT}) is high. Effective mobility was well correlated with N_{OT}. Flicker noise level and trap density N_{OT} of La_2O_3 gate NMOSFET is on the same order of the SiO_2 transistor case.

8.2 Experiment

Figure 8-1(a) shows the key steps for the fabrication of Lanthana gate NMOSFET. Lanthana thin films were deposited on silicon substrate with isolation and source/drain structures by e-beam evaporator after HF-dip or H_2O_2- H_3PO_4-solution dip to form chemical oxide functions as an interfacial layer (hereafter, we called HF-last and CO-last respectively). Pressure at the deposition was around 10^{-8}-10^{-10} Torr under the heating of wafers up to 250°C. The samples were then annealed by RTA (Rapid Thermal Anneal) chamber with oxygen or nitrogen gas. Especially for the case of nitrogen annealing, tube and gas lines were vacuumed carefully prior to flow the nitrogen gas to escape oxidation during nitrogen annealing. For comparison, two types of SiO_2 NMOSFET were fabricated: one is furnace-SiO_2 and the other is RTA-SiO_2. Furnace-SiO_2 was fabricated at the diffusion furnace with dry oxygen gas and chlorine gas at 950°C. RTA-SiO_2 was grown at RTA chamber at temperatures between 800 and

900°C. Physical thickness of thin films were measured by ellipsometer. Figure 8-1(b) shows top view of the MOSFET. The gate length of the MOSFET was 2.5, 5, and 10 μm.

8.3 Threshold voltage and drain current

Figure 8-2 shows threshold voltage and Id-Vgs of Lanthana gate NMOSFET. Low subthreshold swing 85 mV/dec and flat saturation region of Id-Vgs were obtained. Figure 8-3 shows the PDA temperature dependence of threshold voltage (V_{th}) of the Lanthana NMOSFET. V_{th} of HF-last gate oxide NMOSFET shows that threshold voltage decreased with increase in the PDA temperature, while V_{th} of the CO-last case increased. Eventually, at 500°C PDA temperature, two types of NMOSFET showed the same threshold voltage. Gate oxides shown in Fig. 8.3 were deposited at the same, so that the intrinsic property of the Lanthana film itself is expected to be equal. Furthermore, the thickness of the interfacial layer formed chemically could not make the difference in V_{th} between the CO-last and HF-last films of MOSFETS. This is because the interfacial layer thickness (EOT ~0.5 nm) is so small compared to the deposited Lanthana film thickness (EOT 1.7nm). For HF-last gate oxide, the decrease of V_{th} can be due to the interfacial layer growth between Lanthana film and silicon substrate, which leads to the oxygen deficient near the grown interfacial layer and makes flat band voltage more negative. On the contrary, for CO-last gate oxide, the increase of V_{th} can be due to the densification of interfacial layer which exists before the deposition. This estimation can be reasonable since the interface of the Lanthana film is covered with the chemical oxide and oxygen in the Lanthana film is difficult to bond

with silicon in the chemical oxide thermodynamically. This point is different from the HF-last film case. Thus, As CO-last Lanthana film becomes densified with higher temperature, so the absolute values of flat band voltage and V_{th} are decreased approaching the ideal value.

8.4 Channel mobility

Figure 8-4 shows effective channel mobility as a function of effective vertical field in the inversion channel, for HF-last and Co-last Lanthana gate oxides. The peak mobilities of the Lanthana NMOSFET were 290 and 241 $cm^2/V\text{-}s$ for HF-last and CO-last cases, respectively. When the effective channel field is greater than the 1.5 MV/cm, the effective mobility of the experiment coincide with the universal mobility. Higher PDA temperature results in higher mobility for the both cases.

To compare the mobility of the HF-last and CO-last cases, the effective mobility and the oxide trap density N_{ot} obtained from the noise measurement are plotted as a function of the flat band voltage shift ΔV_{FB} in Fig. 8.5. In the case of CO-last, the mobility increased as ΔV_{FB} decrease, while in the case of HF-last increased. This reverse behavior can be explained in terms of N_{ot}, as shown in Fig. 8.6. For both types of films, mobility was strongly correlated with N_{OT}. Mobility increase due to decrease of N_{OT} is in the same fashion of SiO_2 case as show in Fig. 8.6(b).

Figure 8-7 shows effective mobility of Lanthana NMOSFET as a function of oxygen PDA temperatures, for HF-last and CO-last cases. With the change of gate oxide EOT, the effective mobility is nearly same for the both cases.

8.5 1/f noise

Figure 8-8 shows noise spectral density of Lanthana and SiO_2 NMOSFETs. The number fluctuation model of 1/f nose is suggested by McWhorter [2]:

$$\frac{S_{ID}}{I_D^2} = \left(\frac{g_m}{I_D}\right)^2 S_{VG} \qquad \text{(Eq. 8.1)}$$

Voltage noise spectral density is related to the oxide trap [3]:

$$S_{VG} = \frac{q^2 kT\lambda N_{ot}}{8WLC_{ox}^2 f} \qquad \text{(Eq. 8.2)}$$

By plotting S_{VG} with N_{OT}, one can find the linear relationship as shown in Fig. 8.9 and evaluate the oxide trap density N_{OT}. Figure 8-9 shows normalized drain current noise S_{ID}/I_D^2 of Lanthana and SiO_2 NMOSFET for both linear and saturation regions to extract trap density N_{OT} [4].

8.6 Conclusion

Lanthana NMOSFETs with EOT values from 0.66 to 3.1 nm were fabricated using e-beam evaporation of Lanthana and process dependence on their mobility and 1/f noise were evaluated for the first time. It was found that La2O3 NMOSFET mobility was effectively correlated with NOT from S_{ID}/I_D^2. Mobility of CO-last film was increased by decrease of ΔV_{FB}. Low subthreshold swing 85 mV/dec. and very high drain current drive more than 45 μA/μm @ Lg=10μm was confirmed at EOT=1.7 nm. Although,

the vertical effective field became very high because of the negative flat-band shift, the effective mobility and 1/f noise of Lanthana NMOSFETs were considerably good and comparable level of SiO_2 depending on the conditions. Further optimization of the annealing condition would be necessary, but the above results obtained in this MOSFET experiments suggest that Lanthana is a strong candidate for post HfO_2 high-k dielectrics with EOT values of less than 1 nm.

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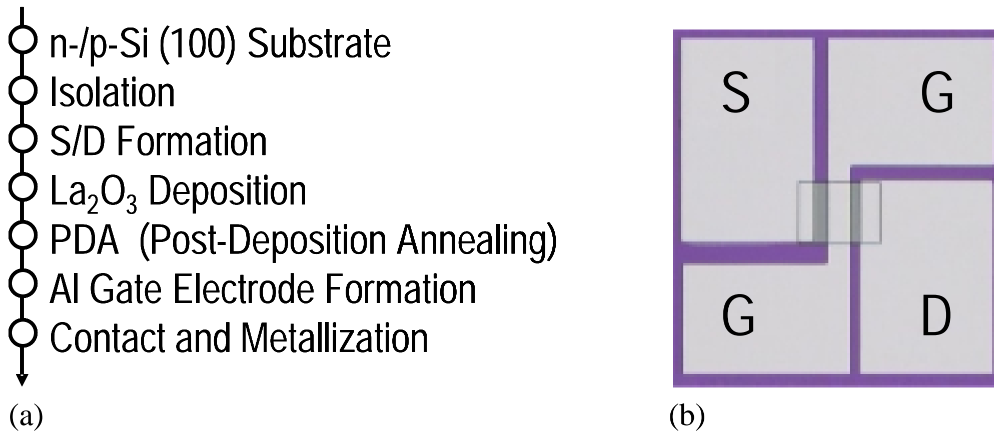


Fig. 8.1. Process flow (a) and micrograph (b) of MOSFET

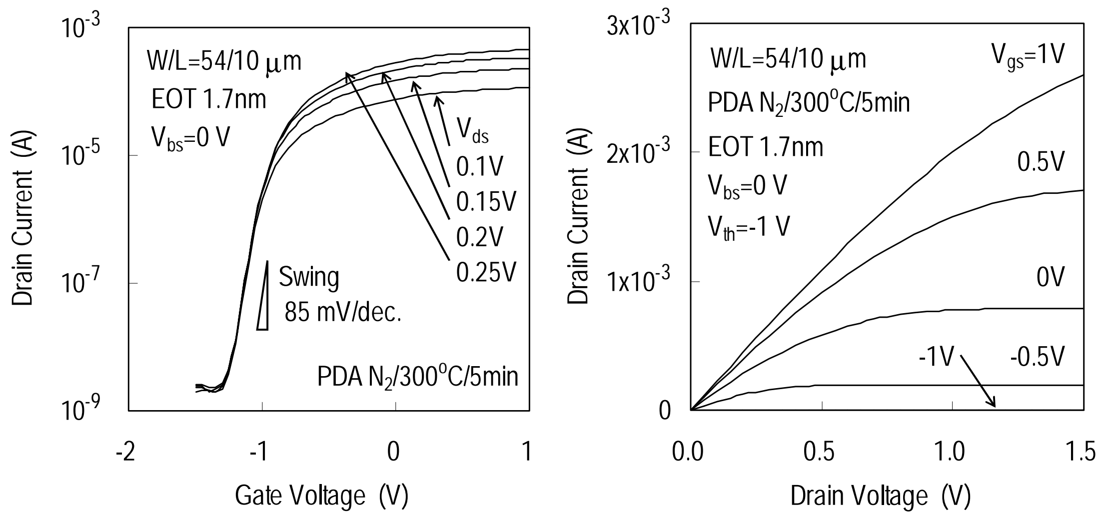


Fig. 8.2. Typical NMOSFET features with Lanthana as a gate dielectric: (a) subthreshold swing for four drain voltages and (b) drain saturation current.

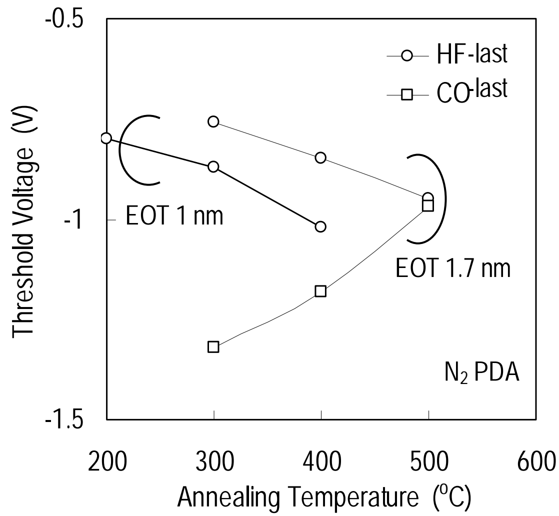


Fig. 8.3. Threshold voltages of Lanthana NMOSFET as a function of annealing temperature, for two types of gate oxide films fabricated with different surface treatments of the silicon substrate: HF-cleaned and chemical oxide formed. Annealing was carried out in nitrogen ambient for 5 min.

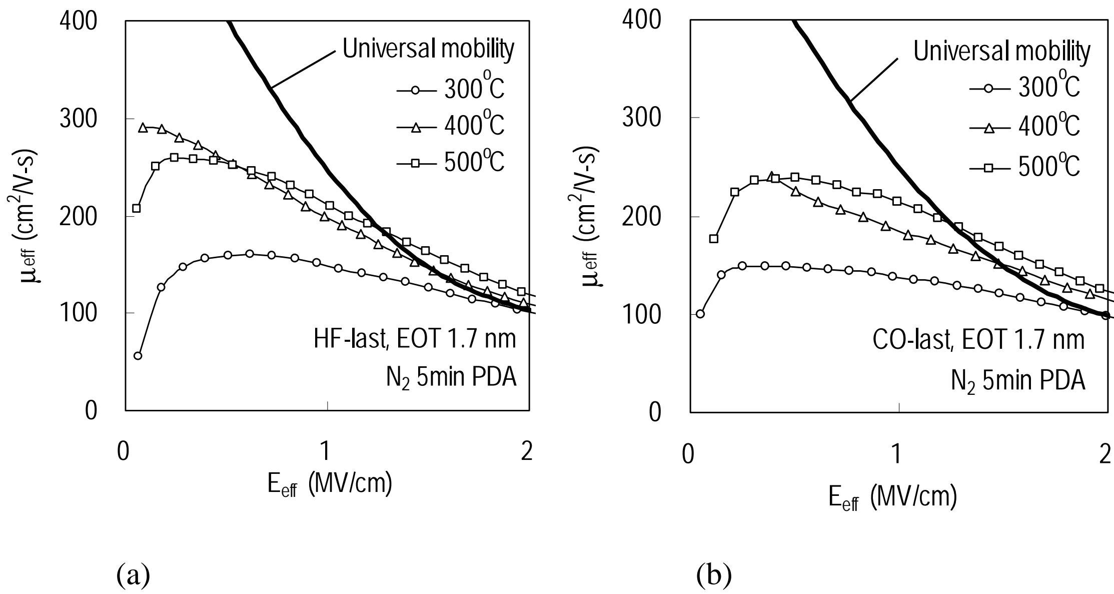
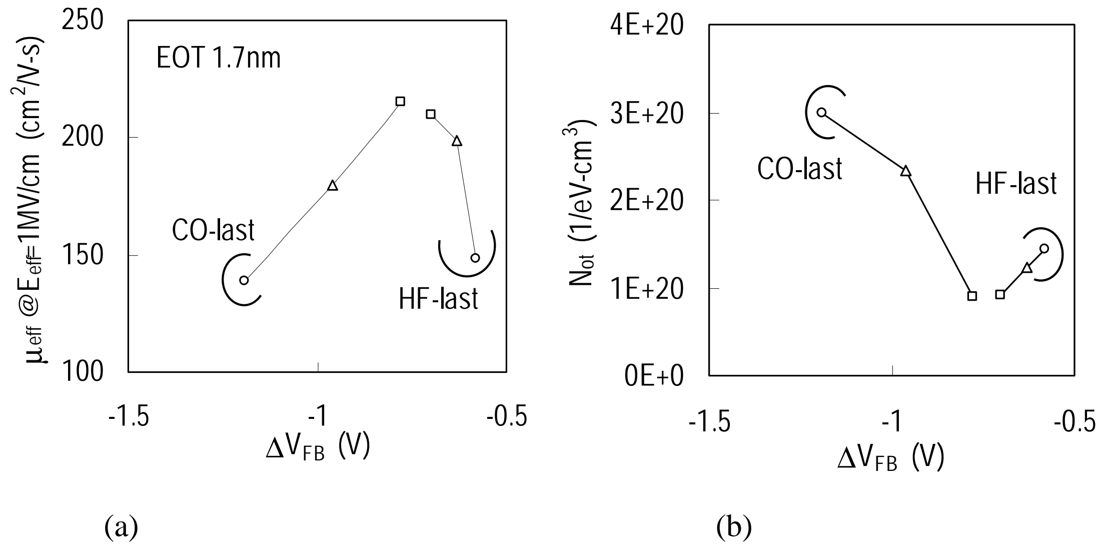
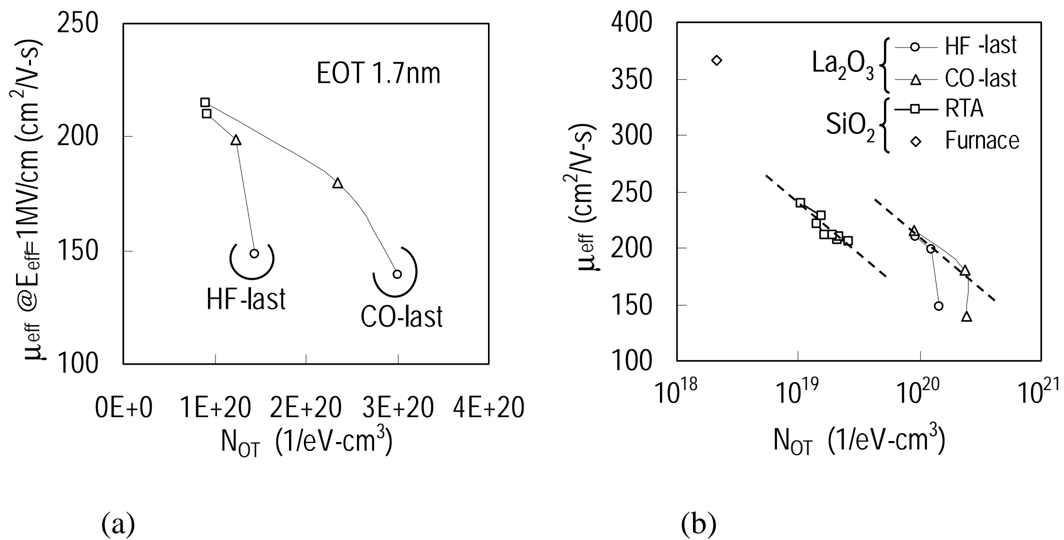


Fig. 8.4. Effective mobility of Lanthana NMOSFET as a function of nitrogen PDA temperatures, fabricated with two different surface treatments of the silicon substrate: (a) HF-cleaned and (b) chemical oxide formed.



(a) (b)

Fig. 8.5. Effective mobilities (a) at effective channel field 1 MV/cm and oxide trap density N_{ot} (b) obtained from flicker noise, as a function of flat band voltage shift ΔV_{FB}.



(a) (b)

Fig. 8.6. Correlation between effective mobility μ_{eff} and trap density N_{ot} of Fig. 8.5. Mobilities of Lanthana NMOSFET are compared with those of RTA-SiO_2 NMOSFET in (b).

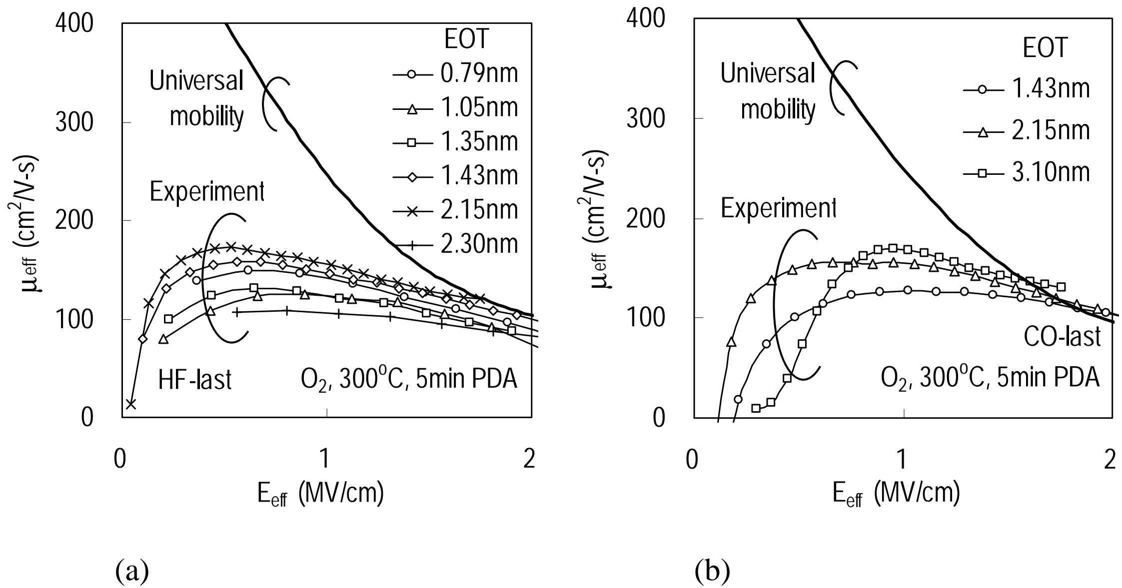


Fig. 8.7. Effective mobility of Lanthana NMOSFET as a function of oxygen PDA temperatures, fabricated with two different surface treatments of the silicon substrate: (a) HF-cleaned and (b) chemical oxide formed.

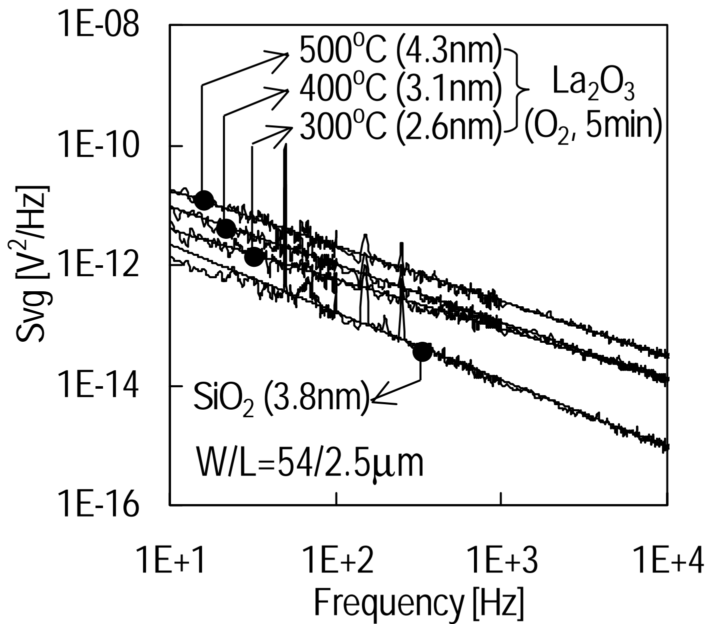


Fig. 8.8. Flicker noise characteristics of Lanthana NMOSFET compared with SiO_2 NMOSFET of the equivalent EOT. Numbers in parenthesis are EOT.

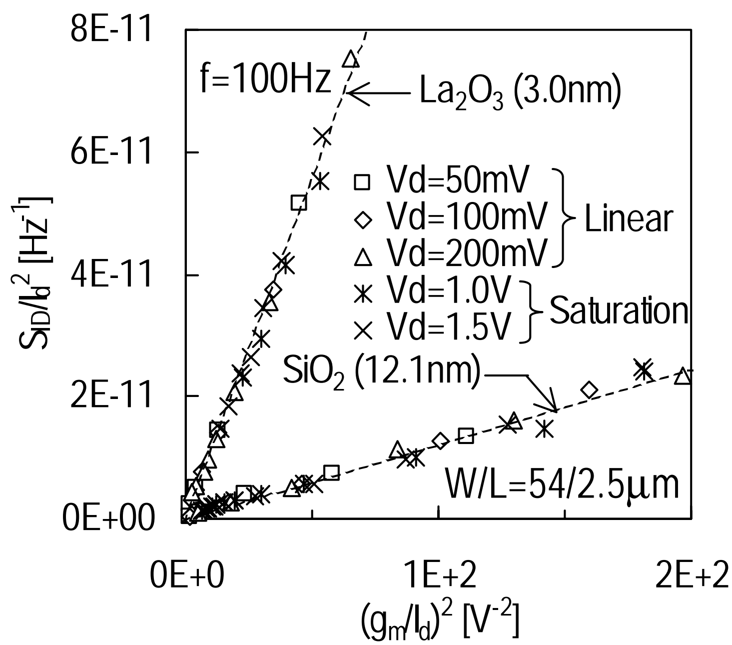


Fig. 8.9. Normalized drain current noise spectral density S_{ID} as a function of normalized transconductance at both linear and saturation regions of SiO_2 and Lanthana NMOSFETs. Slopes of each curves correspond to S_{VG} and Not can be evaluated from the equation of S_{VG}.

Chapter 9. Conclusions

9.1 Conduction mechanisms on La_2O_3 gate oxide

9.2 Recommendation for future work

9.3 Discussion to the future of La_2O_3 gate oxide

Reference

9.1 Conduction mechanisms on La_2O_3 gate oxide

Alternative dielectric for gate oxide is required for the fast and small devices of the future. Conduction mechanisms for Lanthana film as a promising alternative gate dielectric were studied for oxide thickness ranging from 3.5 to 14 nm in physical thickness. Lanthana films were annealed in oxygen or nitrogen ambient at temperatures from 200 to 900°C for 5 min.

From the spectroscopic ellipsometry and C-V characteristics, it is found that the fixed oxide charge was all positive and caused by the reduction process near the interface between the Lanthana and silicon substrate. This, in turn, results in trapping sites efficient for electron, which plays an important role in the conduction process. It is also found that positive charges can be generated in the bulk and interface to the gate electrode, as illustrated in Fig. 9.1. Additionally, it is interesting to note that achieving the negligible interface state density of Lanthana film to the silicon substrate is not difficult, almost independent of the existence of the interfacial layer.

The observed conduction mechanisms were ohmic and SCLC at low gate voltage region, and F-N, Schottky, and P-F conductions at high voltage region. It should be worth noting that ohmic, SCLC, and P-F conductions are related with the trap sites in the oxide. Furthermore, even if the current variation occurred, the conduction mechanisms were found to basically be same. It should be noted that the identified conduction mechanisms in La_2O_3 film are very similar to those in other high-k materials, which are summarized in appendix 8.

Among the identified conduction mechanisms, ohmic, SCLC, and F-N

conductions are considered to be originated in the intrinsic property of Lanthana film from the fact that conduction mechanisms responsible for MIM capacitors were similar to those of MOS capacitors.

From the investigation of Lanthana gate MOSFET, the subthreshold swing 85 mV/dec, the pretty flat saturation region in Id-Vg, and the maximum effective channel mobility 290 cm^2/V-s from split C-V were obtained. With the comparison of the oxide trap density from 1/f noise measurement to the effective channel mobility, chemical oxide layer formed before Lanthana deposition can be though of as trapping sites with positive charges.

Finally, regarding suggestion to the low gate leakage current of Lanthana film, it should be mentioned that gate leakage current can be minimized depending on the prevalent conduction mechanisms. If the tunneling conductions, such as direct and F-N tunneling, are important, the gate current can be decreased as much as the film is thin. If the SCLC conduction, among the trap-related conductions, is dominant, the gate current can be reduced by the amount of trap sites, as illustrated in Fig. 9.2.

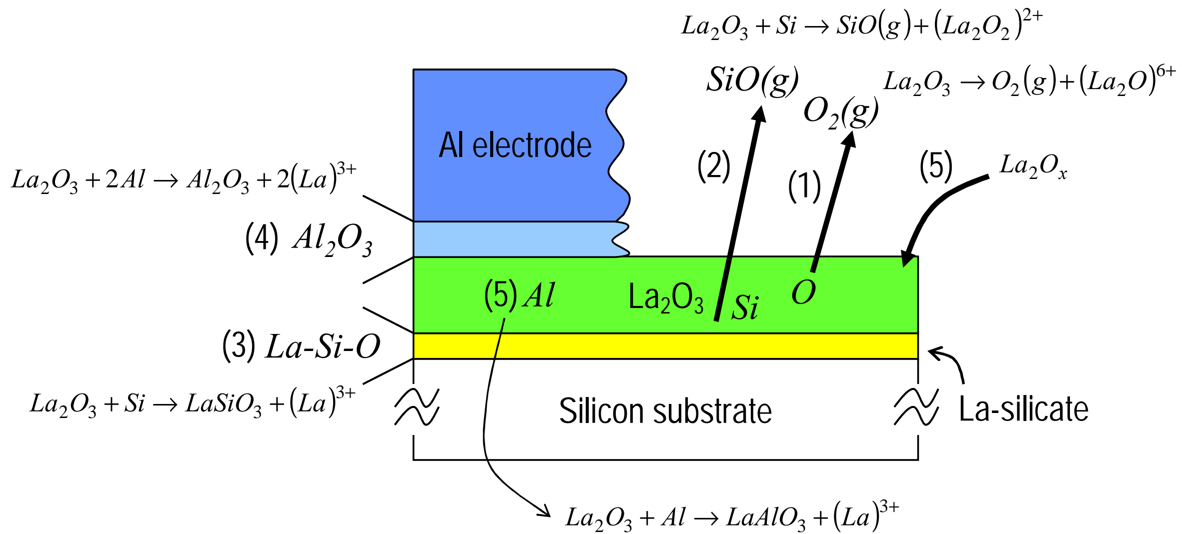


Fig. 9.1. Proposed mechanisms for positive charge creation

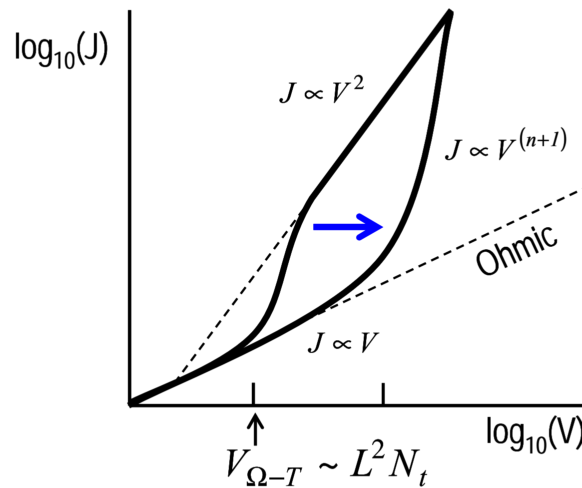


Fig. 9.2. Lampert triangle: the more trap levels, the less leakage current density. $V_{\Omega\text{-}T}$ expresses the transition point between J~V and $J\sim V^{(n+1)}$. n describes the trap energy level distribution in the oxide band gap. L and N_t denote film thickness and oxide trap density, respectively.

9.2 Recommendation for future work

There are numerous attempts to remove the interfacial layer growth between Lanthana and silicon substrate. However, it seems to be difficult because Lanthana film is porous enough for oxygen or silicon to diffuse into the Lanthana film. The best way is two-fold. First is to protect the silicon surface to remove the chance of the oxidation reaction before Lanthana film deposition. Second is to protect the deposited Lanthana film in-situ in the vacuum chamber to remove the oxygen vaporizing and the diffusion into the silicon substrate. Additionally, since stoichiometry film does not have the interfacial layer, an epitaxial growth of Lanthana film on the silicon substrate can be a solution.

Regarding the flat-band voltage shift of Lanthana film, since the shift is caused by the oxygen deficiency, any deposition method at the ultra high vacuum chamber could not be recommended. This is because the deposited film in the ultra high vacuum state is easy to loose its oxygen atom. This can probably explain the positive fixed oxide charges which is always in the as-deposited Lanthana films.

As for the application of Lanthana film, Lanthana MOSFET on germanium substrate can be promising as well, since thermally grown oxide of germanium substrate is known to be thermally unstable and water-soluble.

9.3 Discussion to the future of La_2O_3 gate oxide

In 2001, the very low gate leakage current at thin CET of Lanthana film has been reported [1,2]. Since then, several studies have been made, so that the Lanthana film is being focused as a replacement of gate dielectric in the next generation of HfO_2 gate film, due to high dielectric constant and low leakage current. As regards the conduction process, as stated in 9.2, Lanthana film has similarities compared to other high-k films including HfO_2, which is summarized in appendix 8. One can speculate that the similarities come from the growing method, that is, all the films are made by deposition method. Lanthana film has some challenges: flat-band voltage shift, low channel mobility, hygroscopic behavior, and quality variation. As for flat-band voltage shift, a change in annealing process and steps after film deposition can improve it. As shown in Fig. 9.3, PMA process recover the flat-band voltage to its original value, although it also shifts the flat-band voltage in the opposite direction. Regarding channel mobility, optimization in annealing can make a better channel mobility, as shown in Fig. 9.4. Since Lanthana film is easy to absorb moisture in the air, it is recommended that the film should be kept in vacuum or dry ambient after deposition. Besides, addition of some impurity materials and stacked structure are being studied in the same reason.

To sum up, Lanthana film has a prominent property as a gate dielectric, theoretically, although we have many challenges to realize it, experimentally and reproducibly.

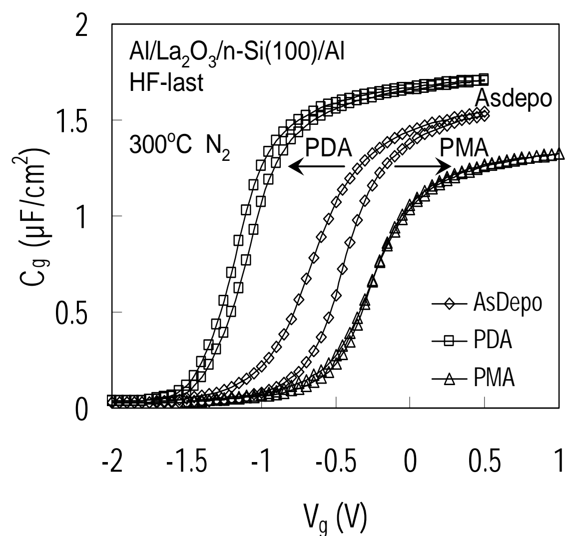


Fig. 9.3. *C-V* characteristics of PDA, PMA and as-deposited (control) samples [3].

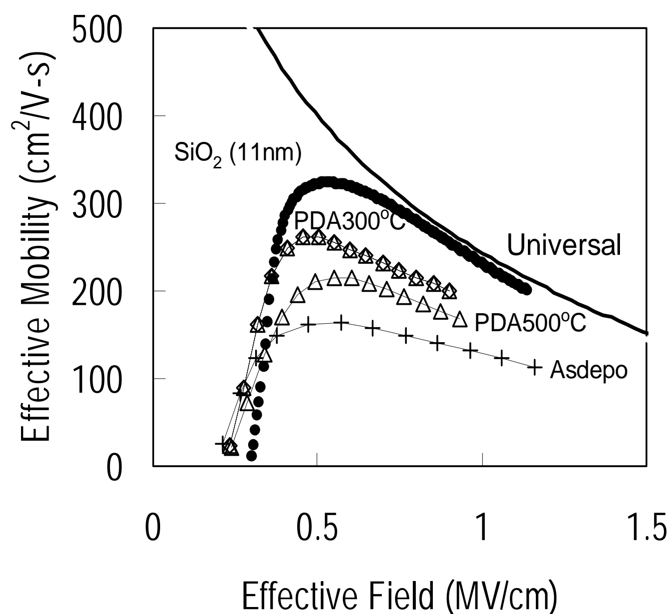


Fig. 9.4. Effective mobility of MOSFET with conventional SiO_2 and La_2O_3 (with or without PDA) as the gate dielectric [3].

Reference

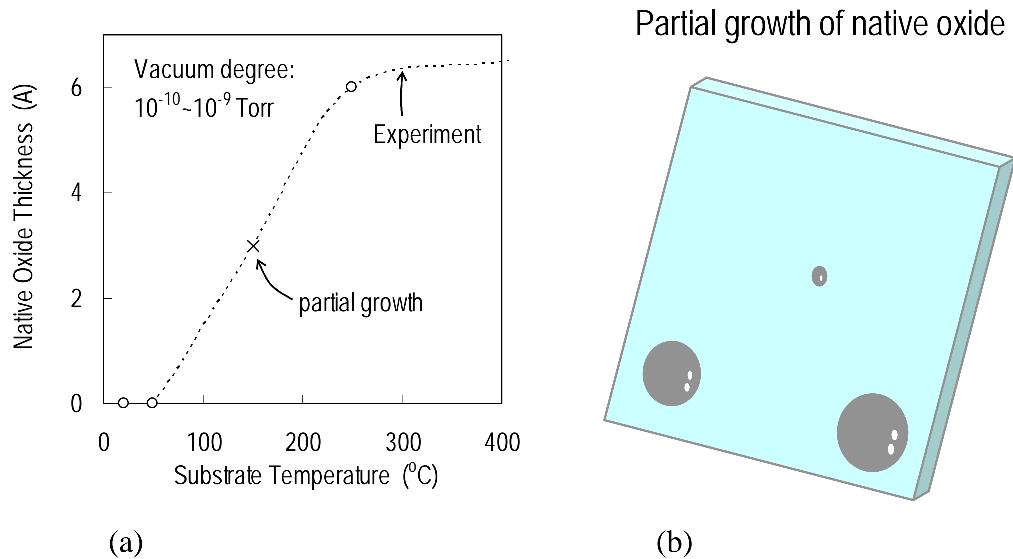
[1] S. Ohmi, C. Kobayashi, K. Aizawa, S. Yamamoto, E. Tokumitsu, H. Ishiwara, and H. Iwai: Proc. ESSDERC (2001) 235.

[2] S. Ohmi, C. Kobayashi, E. Tokumitsu, H. Ishiwara, and H. Iwai: Ext. Abst. SSDM (2001) 496.

[3] J.A. Ng, Y. Kuroki, N. Sugii, K. Kakushima, S.-I. Ohmi, K. Tsutsui, T. Hattori, H. Iwai and H. Wong, "ffects of Low Temperature Annealing on the Ultrathin La_2O_3 Gate Dielectric; Comparison of Post Deposition Annealing and Post Metallization Annealing," To be presented in INFOS 2005 and to be published in Microelectron. Eng.

Appendix

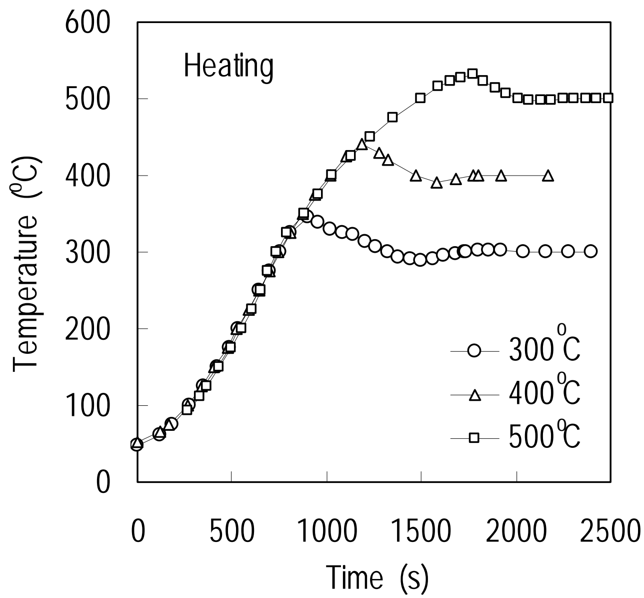
1. Native oxide growth while keeping in vacuum chamber



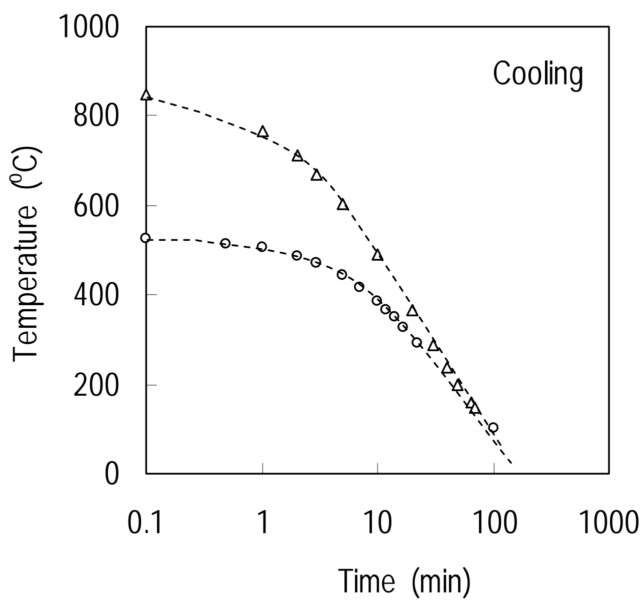
(a) (b)

Fig.A-1. Native oxide thickness as a function of substrate temperature (a) and schematic view of partial growth (b).

2. Substrate temperature at heating and cooling of the substrate



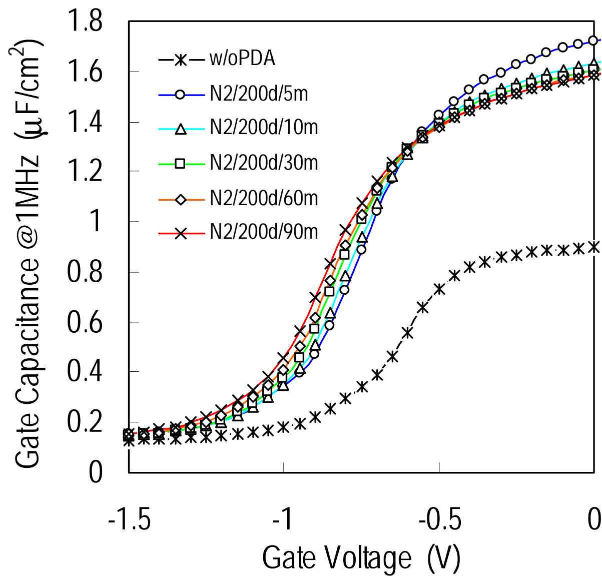
(a)



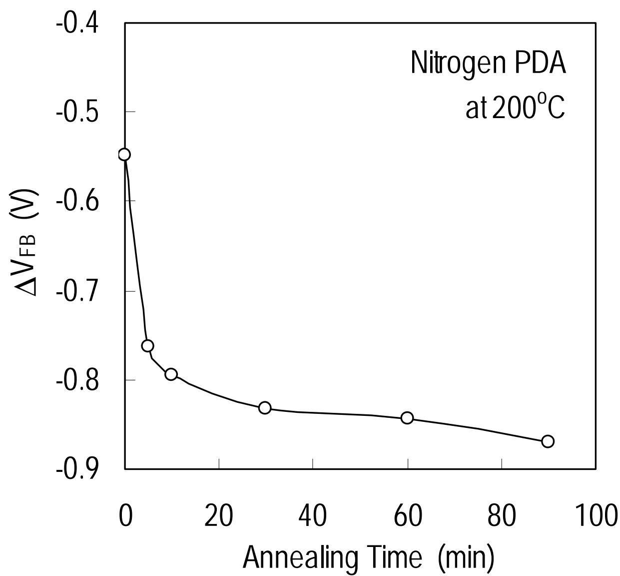
(b)

Fig. A-2 Temperature change of the substrate in deposition chamber for (a) heating and (b) cooling. No controller exists for cooling.

3. Capacitance and flat-band voltage shift with long time PDA in nitrogen ambient



(a)



(b)

Fig. A-3 Capacitance and flat band voltage shift ΔV_{FB} of Lanthana MOS capacitor with long time PDA in nitrogen ambient

4. C/C++ Code for conduction model fitting

```
/***************************************************************************
*/
#define MOUDLENAME "MosDiodeRegressor()"

#include "usrfunc.h"
uFuncTableTag uMosDiodeRegressorTag={
"MosDiodeRegressor(J-V)",
"type=MosDiodeRegressor                                              ¥n"
"argument=PF xyt=(1,2,40)(1,3,80)(1,4,120) unit=5 range=-2e6,2e6,0.97",
"[Y.Kim]                                                        ¥n"
"2003.0522-0721,0807,0820,0825-0829,0921-1008,1112                         ¥n"
"2004.0114-15,0211,0326,0409-0410,0611                                  ¥n"
"                                                               ¥n"
"[Input]                                                        ¥n"
"ARGUMENT=<MODEL>                                                 ¥n"
"! OHM (Ohmic Conduction) : |J|=a*|V|                                  ¥n"
"! OHM2 (Ohmic Conduction ) : |J|=a*|V|+yi                              ¥n"
"! SCLCEXP (SCLC with exponential trap level distribution) : |J|=a*|V|^(b+1) ¥n"
"! SCLCUNI (SCLC with uniform trap level distribution) : |J|=a*|V|*exp(b*|V|) ¥n"
"! SCLCSQR (Space-Charge-Limited Current with sqaure law of voltage) : |J|=a*|V|^2
¥n"
"! LAMPERT (Mixed Model of Ohmic and SCLC) : |J|=a*|V|+b*|V|^2          ¥n"
"! CUBE (SCLC) : |J|=a*|V|^3                                        ¥n"
"!              DT              (Direct              Tunneling)              :
|J|=a*sinh(b*|Eox|),b=3.125e-7*sq(Tox)*sqrt((m*/m0)/BarrierHeight) ¥n"
"!             DTLEE2             (Direct             Tunneling)             :
|J|=a*Eox^2*exp(-b/|Eox|*(1-(1-|Eox|*c)^(2/3))),c=Tox/BH ¥n"
"! FN (Flower-Nordheim Tunneling) : |J|=a*|Eox|^2*exp(-b/|Eox|)          ¥n"
"! POOLE : |J|=a*exp(b*|Eox|)                                        ¥n"
"! SCHOTTKY (Richardson-Schottky) : |J|=a*exp(b*|Eox|^0.5)              ¥n"
"! PF (Poole-Frenkel) : |J|=a*|Eox|*exp(b*|Eox|^0.5)                   ¥n"
"! STAT (Shallow Trap-Assisted Tunneling) : |J|=a(1-b/|Eox|)*exp(-c/|Eox|)/|Eox|
¥n"
"! DTAT (Deep Trap-Assisted Tunneling) : |J|=a/|Eox|*exp(-b/|Eox|)         ¥n"
"! Note 1) When <MODEL> is '*', every model is analyzed.                ¥n"
"! Note 2) J [=] A/cm2, V [=] V, Eox [=] V/cm                          ¥n"
"XYT=(X,Y,T)(X1,X2,Y,T)...(X,Y,T)                                     ¥n"
"! The first in parentheses is X vector index, which should be V [V] or Eox [V/cm],
and monotonic. ¥n"
"! The second is Y column index, which should be J [A/cm^2].             ¥n"
"! The third is temperature in Celcius degree, neither z-index nor floating. ¥n"
">>>>>>>>>>> (Vg,Jg,Temperature) (Vg,Eox,Jg,Temperature) <<<<<<<<<< "
"ARGUMENT3=TOX,MRATIO                                               ¥n"
"! TOX [nm] : Physical thickness of insulator. (for DT)                 ¥n"
"! MRATIO [] (=m*/m0) : Effective electron mass ratio. (for DT and FN)      ¥n"
"OPTION= NOT-USED                                                  ¥n"
"SUBOPTION|UNIT=<N>                                                 ¥n"
"! N [integer] : Defines minimum number of data point to fit.             ¥n"
"! Should be greater than 3 at least. Default is 5.                    ¥n"
"RANGE=[<L>,<H>,<G>|(<L>,<H>,<G>)]                                   ¥n"
```

```
"! L [double|*] : Lower limit X for fitting. <*> means data minimum.        ¥n"
"! H [double|*] : Upper limit X for fitting. <*> means data minimum.        ¥n"
"! G [double|*] : Lower limit of ¥"GoodnessOfFit¥". Usually 1> and >0.95    ¥n"
"                                                                      ¥n"
"[Output]                                                               ¥n"
"! See Log window.   "
};

/*************************************************************************
*/

#include <math.h>
#include <string.h>
#include "usrfunc.h"
#include "nrecipe.h"
#include "number.h"
#include "tools.h"
#include "str.h"
#include "semiconductor.h"

extern int Echo();
extern int GetFittingRange(
   VECTOR vX,int nRl,int nRh,int nFitTotal,double dL,double dH,
   int *nL,int *nH
   );

#if !defined(SIGN)
#define SIGN(x)   ((x)>=0 ? 1:-1)
#endif

/*
DT_HESTO     P.Hesto,Instabilities in silicon devices vol.1,1986,p.291,Eq.(5.28)
DT_LEE      2000,198-99,W.Lee,Symp.VLSI Tech.
DT_SCHUEGRAF 1992,18-19,K.Schuegraf,Symp.VLSI Tech.
*/
static char *qConductionModels[]={
   "OHM",
   "OHM2",
   "SCLCEXP",
   "SCLCUNI",
   "SCLCSQR",
   "LAMPERT",
   "CUBE",
   "DT",//"DT_HESTO","DT_SCHUEGRAF","DT_LEE"
   "DTLEE2",
   "FN",
   "POOLE",
   "SCHOTTKY",
   "PF",
   "STAT",
   "DTAT"
};
#define MODEL_OHM      0
#define MODEL_OHM2     1
#define MODEL_SCLCEXPONENTIAL 2
```

```
#define MODEL_SCLCUNIFORM    3
#define MODEL_SCLCSQUARE    4
#define MODEL_LAMPERT  5
#define MODEL_SCLCCUBE  6
#define MODEL_DT      7
#define MODEL_DT_LEE2  8
#define MODEL_FN      9
#define MODEL_POOLE    10
#define MODEL_SCHOTTKY  11
#define MODEL_PF      12
#define MODEL_STAT     13
#define MODEL_DTAT     14

/***************************************************************************
*/

static int GetModelTotal()
{
  return noof(qConductionModels);
}

static const char *qGetModelName( int nModelIndex ) /* STATIC */
{

  int nModels;

  nModels=GetModelTotal();
  if (nModelIndex<0||nModelIndex>nModels) return CNULL;
  return qConductionModels[nModelIndex];
}

static int GetModelIndex( const char *pModel )
{
  int nModelOptionTotal,nModelIndex;
  char qName[128];
  const char *qModelName;

  strcpy2buf(qName,pModel,noof(qName));
  strtoupper(qName);
  nModelOptionTotal=GetModelTotal();
  for (nModelIndex=0;nModelIndex<nModelOptionTotal;nModelIndex++) {
    qModelName=qGetModelName(nModelIndex);
    if (strequ(qName,qModelName)) return nModelIndex;
  }
  return -1;
}

/*---------------------------------------------------------------------------
*/

/* J=a*Eox+(yi) -> y=a[1]*x or y=a[1]+a[2]*x */
static void _OHM(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
```

```
   if (na==1) {
      *y=a[1]*x;
      dyda[1]=x;
   } else /* if (na==2) */ {
      *y=a[1]+a[2]*x;
      dyda[1]=1.;
      dyda[2]=x;
   }
}

/* J=a*Eox^(b+1) -> ln(J)=ln(a)+b+1)*Eox -> y=a[1]+a[2]*x */
static void _SCLCEXPONENTIAL(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
   _OHM(x,a,y,dyda,na);
}

/* D.R.Lamb,"Electrical Conduction Mechanisms in Thin Insulating Films,"
 * 1967,p.30,Eq.(4.28)
 * J=a*Eox*exp(b*Eox) -> ln(J/Eox)=ln(a)+b*Eox -> y=a[1]+a[2]*x */
static void _SCLCUNIFORM(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
   *y=a[1]+a[2]*x;
   dyda[1]=1;
   dyda[2]=x;
}

/* J=a*Eox^2 -> ln(J)=ln(a)+2*ln(Eox) -> y=a[1]+2*x */
static void _SCLCSHALLOW(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
   *y=a[1]+2*x;
   dyda[1]=1;
}

/* J=a*Eox+b*Eox^2 -> y=a[1]*x+a[2]*x^2 */
static void _LAMPERT(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
   double xx=x*x;
   *y=a[1]*x+a[2]*xx;
   dyda[1]=x;
   dyda[2]=xx;
}

/* J=a*Eox^3 -> ln(J)=ln(a)+3*ln(Eox) -> y=a[1]+3*x */
static void _SCLCCUBE(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
```

```
  *y=a[1]+3*x;
  dyda[1]=1;
}

/* P.Hesto,Instabilities in silicon devices vol.1,1986,p.291,Eq.(5.28)
 * J=a*sinh(b*Fox) -> ln(J)=ln(a)+ln(sinh(b*Fox)) -> y=a[1]+ln(sinh(a[2]*x))
 * where Fox=3.125e7*s^2*Eox and b=sqrt(MassRatio/BarrierHeight)
 */
static void _DT(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
  *y=a[1]+log(sinh(a[2]*x));
  dyda[1]=1;
  dyda[2]=x*cosh(a[2]*x)/sinh(a[2]*x);
}

/* Approximated Form of Lee Model [20041221]
 * Lee model:
 *   2000,198-99,W.Lee,Symp.VLSI Tech.pdf
 *   2000,21(11),540-42,Y.Yeo,IEEE Elec.Dev.Lett.pdf
 *   1999,20(6),268-70,W.Lee,IEEE Elec.Dev.Lett.pdf
 * Approximation of Lee model:
 *   E. Miranda. Submitted to APL 2004.
 *   1999,86(1),480-86,C.Chaneliere,J.Appl.Phys.pdf
 * Coding form:
 *   |J|=a*Eox^2*exp(-b/|Eox|*(1-(1-|Eox|*c)^(2/3))),c=Tox/BH
 *   -> ln(|J|/Eox^2)=ln(a)-b/|Eox|*(1-(1-|Eox|*c)^(2/3))
 *   -> y=a[1]-a[2]/|x|*(1-(1-|x|*a[3])^(2/3))
 *   y=ln(|J|/Eox^2), x=|Eox|, a[1]=ln(a), a[2]=b, a[3]=c
 */
static void _DTLEE2(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
  double z,z23,z13;

  z=1-x*a[3];
  /* If z<0, current will not be DT but FN.
   * So, following is under the assumption of positive z.
   */
  z23=exp(1./3*log(z*z)); /* Be carefule that wrong is "=exp(1/3*log(z*z));" */
  z13=sqrt(1/z23);
  *y=a[1]-a[2]/x*(1-z23);
  dyda[1]=1;
  dyda[2]=-1./x*(1-z23);
  dyda[3]=2./3*a[2]*z13; /* Be carefule that wrong is "=2/3*a[2]*z1;" */
}

/* P.Hesto,"Instabilities in silicon devices vol.1",1986
 * p.291,Eq.(5.30)
 * J=a*Eox^2*exp(-b/Eox) -> ln(J/Eox^2)=ln(a)-b/Eox -> y=a[1]-a[2]*x */
static void _FN(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
```

```
{
  *y=a[1]-a[2]*x;
  dyda[1]=1.;
  dyda[2]=-x;
}

/* "A general bulk-limited transport analysis of a 10 nm-thick oxide
 * stress-induced leakage current," B. De Salvo et al.,
 * Solid-State Electronics 44(2000)895-903
 * J=a*exp(b*Eox) -> ln(J)=ln(a)+b*Eox -> y=a[1]+a[2]*x */
static void _POOLE(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
  _OHM(x,a,y,dyda,na);
}

/* P.Hesto,"Instabilities in silicon devices vol.1",1986
 * p.287,Eq.(5.22)
 * J=a*exp(b*Eox^0.5) -> ln(J)=ln(a)+b*Eox^0.5 -> y=a[1]+a[2]*x */
static void _SCHOTTKY(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
  _OHM(x,a,y,dyda,na);
}

/* P.Hesto,"Instabilities in silicon devices vol.1",1986
 * p.304,Eq.(5.55)
 * J=a*Eox*exp(b*Eox^0.5) -> ln(J/Eox)=ln(a)+b*Eox^0.5 -> y=a[1]+a[2]*x */
static void _PF(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
  _OHM(x,a,y,dyda,na);
}

/*
 [Yang1996] B.Yang et al., "Modelling of trap-assisted electronic
 conduction in thin thermally nitrided oxide films,"
 Solid-State Electronics 39[3]385-390(1996).
 |J|=a(1-b/|Eox|)*exp(-c/|Eox|)/|Eox| ->
 |J*Eox|=a(1-b/|Eox|)*exp(-c/|Eox|) -->
 ln(|J*Eox|)=ln(a)+ln(1-b/|Eox|)-c/|Eox| --->
 y=a[1]+ln(1-a[2]*x)-a[3]*x
 */
static void _STAT(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
  *y=a[1]+log(1-a[2]*x)-a[3]*x;
  dyda[1]=1;
  dyda[2]=-x/(1-a[2]*x);
  dyda[3]=-x;
}
```

```
/*
 [Fleischer1993] S.Fleischer and P.T.Lai, “A new method for extracting
 the trap energy in insulators,” J.Appl.Phys. 73[7]3348-51(1993).
 |J|=a/|Eox|*exp(-b/|Eox|) ->
 ln(|J*Eox|)=ln(a)-b/|Eox| -->
 y=a[1]+a[2]*x
 */
static void _DTAT(x,a,y,dyda,na)
double x,a[],*y,dyda[];
int na;
{
   _OHM(x,a,y,dyda,na);
}

static int ComplyFittingVectorsWithModel(
   int nModel,VECTOR vX,VECTOR vY,
   int nL,int nH,
   double dTox // Physical Tox [cm]
)
{
   int j;
   double dX,dY;

   switch (nModel) {
   case MODEL_OHM :
   case MODEL_OHM2 :
   /* J=a*|V|+yi -> y=a[1]*x+a[2] */
      for (j=nL;j<=nH;j++) vX[j]=fabs(vX[j]); /* 20031006 */
      break;
   case MODEL_SCLCEXPONENTIAL :
   /* |J|=a*|V|^(b+1) -> ln(|J|)=ln(a)+(b+1)*ln(|V|) -> y=a[1]+a[2]*x */
      for (j=nL;j<=nH;j++) {
         vX[j]=log(fabs(vX[j]));
         vY[j]=log(fabs(vY[j]));
      }
      break;
   case MODEL_SCLCUNIFORM :
   /* |J|=a*|V|*exp(b*|V|) -> ln(|J|/|V|)=ln(a)+b*|V| -> y=a[1]+a[2]*x */
      for (j=nL;j<=nH;j++) vX[j]=fabs(vX[j]); /* 20031006 */
      for (j=nL;j<=nH;j++) vY[j]=log(fabs(vY[j]/vX[j]));
      break;
   case MODEL_SCLCSQUARE :
   /* |J|=a*|V|^2 -> ln(|J|)=ln(a)+2*ln(|V|) -> y=a[1]+2*x */
      for (j=nL;j<=nH;j++) {
         vX[j]=log(fabs(vX[j]));
         vY[j]=log(fabs(vY[j]));
      }
      break;
   case MODEL_LAMPERT :
   /* J=a*|Eox|+b*|Eox|^2 -> y=a[1]*x+a[2]*x^2 */
      for (j=nL;j<=nH;j++) vX[j]=fabs(vX[j]); /* 20031006 */
      break;
   case MODEL_SCLCCUBE :
   /* |J|=a*|V|^3 -> ln(|J|)=ln(a)+3*ln(|V|) -> y=a[1]+3*x */
```

```
      for (j=nL;j<=nH;j++) {
         vX[j]=log(fabs(vX[j]));
         vY[j]=log(fabs(vY[j]));
      }
      break;
   case MODEL_DT :
      /* P.Hesto,"Instabilities in silicon devices vol.1",1986,p.291,Eq.(5.28)
       *     J=a*sinh(b*|Eox|)     ->     ln(|J|)=ln(a)+ln(sinh(b*|Eox|))     ->
y=a[1]+ln(sinh(a[2]*x))
       * where Fox=3.125e7*s^2*Eox and b=sqrt(MassRatio/BarrierHeight)
       */
      for (j=nL;j<=nH;j++) {
         vX[j]=fabs(vX[j])*3.125e7*dTox*dTox; //Fox=3.125e7*s^2*Eox
         vY[j]=log(fabs(vY[j]));
      }
      break;
   case MODEL_DT_LEE2 :
     /*   |J|=a*Eox^2*exp(-b/|Eox|*(1-(1-|Eox|*c)^(2/3))),c=Tox/BH
      *   -> ln(|J|/Eox^2)=ln(a)-b/|Eox|*(1-(1-|Eox|*c)^(2/3))
      *   -> y=a[1]-a[2]/|x|*(1-(1-|x|*a[3])^(2/3))
      *   y=ln(|J|/Eox^2), x=|Eox|, a[1]=ln(a), a[2]=b, a[3]=c
      */
      for (j=nL;j<=nH;j++) {
         dX=vX[j];
         dY=vY[j];
         vX[j]=fabs(dX);
         vY[j]=log(fabs(dY/(dX*dX)));
      }
      break;
   case MODEL_FN :
   /*    |J|=a*|Eox|^2*exp(-b/|Eox|)    ->    ln(|J|/|Eox|^2)=ln(a)-b/|Eox|    ->
y=a[1]-a[2]*x */
      for (j=nL;j<=nH;j++) {
         dX=vX[j];
         dY=vY[j];
         vX[j]=fabs(1/dX);
         vY[j]=log(fabs(dY/(dX*dX)));
      }
      break;
   case MODEL_POOLE :
   /* |J|=a*exp(b*|Eox|) -> ln(|J|)=ln(a)+b*|Eox| -> y=a[1]+a[2]*x */
      for (j=nL;j<=nH;j++) vX[j]=fabs(vX[j]); /* 20031006 */
      for (j=nL;j<=nH;j++) vY[j]=log(fabs(vY[j]));
      break;
   case MODEL_SCHOTTKY :
   /* |J|=a*exp(b*|Eox|^0.5) -> ln(|J|)=ln(a)+b*|Eox|^0.5 -> y=a[1]+a[2]*x */
      for (j=nL;j<=nH;j++) {
         //vX[j]=pow(fabs(vX[j]),0.5)*SIGN(vX[j]);
         vX[j]=pow(fabs(vX[j]),0.5); /* 20031004 */
         vY[j]=log(fabs(vY[j]));
      }
      break;
   case MODEL_PF :
   /*   |J|=a*|Eox|*exp(b*|Eox|^0.5)   ->   ln(|J|/|Eox|)=ln(a)+b*|Eox|^0.5   ->
y=a[1]+a[2]*x */
```

```
      for (j=nL;j<=nH;j++) {
        dX=fabs(vX[j]);
        dY=vY[j];
        //vX[j]=pow(dX,0.5)*SIGN(vX[j]); /* 20030827 */
        vX[j]=pow(dX,0.5); /* 20031004 */
        vY[j]=log(dY/dX);
      }
      break;
    case MODEL_STAT :
      for (j=nL;j<=nH;j++) {
        vY[j]=log(fabs(vY[j]*vX[j]));
        vX[j]=1/fabs(vX[j]);
      }
      break;
    case MODEL_DTAT :
      for (j=nL;j<=nH;j++) {
        vY[j]=log(fabs(vY[j]*vX[j]));
        vX[j]=-1/fabs(vX[j]);
      }
      break;
  }

  return nH-nL+1;
}

static int EchoXYTArgumentsInParenthesis( //20041221
  const char *qXYT,const char *qDelimiter,int nIndex,
  int *nX1,int *nX2,int *nY,
  double *dKelvin
)
{
  int i,nCount;
  char *pXYT,*pTok;

  pXYT=(char*)qXYT;
  for (i=0;i<nIndex;i++) {
    pXYT=strchr(pXYT,'(');
    pXYT++;
  }

  nCount=strtokcount(pXYT,qDelimiter);
  if (nCount<=2||nCount>=4) return FALSE;

  nIndex=0;
  *nX1=atoi(pTok=strtokbyindex(pXYT,qDelimiter,nIndex++));
  freeEx(pTok);
  *nX2=nCount==4 ? atoi(pTok=strtokbyindex(pXYT,qDelimiter,nIndex++)):0;
  freeEx(pTok);
  *nY=atoi(pTok=strtokbyindex(pXYT,qDelimiter,nIndex++));
  freeEx(pTok);
  *dKelvin=atof(pTok=strtokbyindex(pXYT,qDelimiter,nIndex++));
  freeEx(pTok);
  *dKelvin+=KKelvin;

  switch (nCount) {
```

```
   case 3 : Echo("xyt(Vg,Jg,Temp)=%d,%d,%.1fK ",*nX1,*nY,*dKelvin);break;
   case          4          :          Echo("xxyt(Vg,Eox,Jg,Temp)=%d,%d,%d,%.1fK
",*nX1,*nX2,*nY,*dKelvin);break;
   }

   return nCount;
}

int MosDiodeRegressor( ARGUMENTS )
   ARGULIST
{
   int j,k;
   int nModelTotal,nModelIndex,iModelIndex;
   int nXYT,iXYT,nFitTotal,nXCol,nX2Col,nYCol,nRLAnswer,nRHAnswer;
   int aBoundary[3],nBoundary,iBoundary; /* 20031004 */
   char *pArgument,*pXYT,*qDelimiter=",()",*pTok,*pL,*pH;
   double
dKelvin/*[K]*/,dTox/*[cm]*/,dMRatio/*[]=m(*)/m(0)*/,dL,dH,dR2,dR2AtLeast;
   VECTOR vXData,vYData,vXCopy,vYCopy,vXMirror,vYMirror;
   int nVLow,nVHigh;

   /* Version */
   Echo(" V.1.9¥n");

   /* Check "ARGUMENT" */ {
      int nModelOptionTotal;
      char *pAddr;
      nModelOptionTotal=GetModelTotal();
      if (strequ(ARGUMENT,"*")) {
         nModelTotal=nModelOptionTotal;
         pArgument=strdpl(qGetModelName(0));
         for (j=1;j<nModelTotal;j++) {
            pAddr=strvcat(pArgument,",",qGetModelName(j),0);
            freeEx(pArgument);
            pArgument=pAddr;
         }
      } else {
         nModelTotal=strtokcount(ARGUMENT,qDelimiter);
         for (j=0;j<nModelTotal;j++) {
            pTok=strtokbyindex(ARGUMENT,qDelimiter,j);
            k=GetModelIndex(pTok);
            freeEx(pTok);
            if (k<0) {
               pTok=itostr2(j+1,"%d");
               Echo(0,"%s¥n%s model at your expression of <ARGUMENT=> is invalid:
¥n%s",
                  MOUDLENAME,pTok,ARGUMENT);
               freeEx(pTok);
               return FALSE;
            }
         }
         pArgument=strdpl(ARGUMENT);
      }
   }
   /* Check "XYT" */
```

```
   pXYT=ARGUMENT2[0]!='(' ? strvcat("(",ARGUMENT2,")",0):strdpl(ARGUMENT2);
   if (chrcount(pXYT,'(')!=chrcount(pXYT,')')) {
      Echo(0,"%s¥nNot paired parentheses at the expression of <XYZ=>¥n",
         MOUDLENAME);
      free(pXYT);
      return FALSE;
   }
   nXYT=strtokcount(pXYT,qDelimiter);
   if (nXYT%3) {
      Echo(0,"%s¥nTotal number is not a muliple of 3 at the expression of <XYT=>¥n",
         MOUDLENAME);
      free(pXYT);
      return FALSE;
   } else {
      nXYT/=3;
   }
   /* Check "NSUBOPTION" */
   nFitTotal=NSUBOPTION<5 ? 5:NSUBOPTION;
   /* Check "RANGE" */
   if (strtokcount(SWEEP,qDelimiter)!=3) {
      Echo(0,"%s¥nParameters are not counted to 3 at the expression of <RANGE=>¥n",
         MOUDLENAME);
      return FALSE;
   }
   pTok=strtokbyindex(SWEEP,qDelimiter,2);
   dR2AtLeast=pTok[0]!='*' ? atof(pTok):0.5; //20031112
   freeEx(pTok);
   /* Check "ARGUMENT3" */
   if (ARGUMENT3&&*ARGUMENT3
      &&strtokcount(ARGUMENT3,qDelimiter)==2) {

dTox/*[cm]*/=atof(pTok=strtokbyindex(ARGUMENT3,qDelimiter,0))*1e-7;freeEx(pTok
);
      dMRatio=atof(pTok=strtokbyindex(ARGUMENT3,qDelimiter,1));freeEx(pTok);
   } else {
      dTox=1e-7;
      dMRatio=0.5;
      Echo("  Following  parameters  are  defined  arbitrarily:  Tox[nm]=%.2f
m*/m0=%.3f¥n",
         dTox*1e7,dMRatio);
   }

   /* Echo */
   Echo(" Model=%s min.fit=%d r2=%g (tox[nm]=%.2f m*/m0=%.3f)¥n",
      ARGUMENT,nFitTotal,dR2AtLeast,dTox*1e7,dMRatio);

   /* Compute */
   for (iXYT=1;iXYT<=nXYT;iXYT++) {
      int nLBoundary,nHBoundary,nGuess;
      double vGuess[8],vAnswer[8];
      //nXCol,nX2Col,nYCol <-- (Vg,Jg,Temp) or (Vg,Eox,Jg,Temp)
      Echo(" [%d] ",iXYT);
      k=EchoXYTArgumentsInParenthesis(
         (const char*)pXYT,qDelimiter,iXYT,&nXCol,&nX2Col,&nYCol,&dKelvin);
      if ((k==3&&(nXCol<NCL||nXCol>NCH||nYCol<NCL||nYCol>NCH)) ||
```

```
(k==4&&(nXCol<NCL||nXCol>NCH||nX2Col<NCL||nX2Col>NCH||nYCol<NCL||nYCol>NCH))) {
         Echo(0,
            "%s¥nX(%d)(%d) or Y(%d) index is out of range."
            "compared to matrix columns [%d..%d] by the command of <XYT=>.¥n",
            MOUDLENAME,nXCol,nX2Col,nYCol,NCL,NCH);
         free(pXYT);
         return FALSE;
      }
      /* Allocate vXData,vYData,vXMirror,vYMirror,vXCopy,vYCopy */
      MGetSafeVectorPair(*MTX,TRUE,NRL,NRH,nXCol,nYCol,
         &vXData,&vYData,&nLBoundary,&nHBoundary);
      vXMirror=VDuplicate(vXData,nLBoundary,nHBoundary);
      vYMirror=VDuplicate(vYData,nLBoundary,nHBoundary);
      vXCopy=VDuplicate(vXData,nLBoundary,nHBoundary);
      vYCopy=VDuplicate(vYData,nLBoundary,nHBoundary);
      nVLow=nLBoundary;
      nVHigh=nHBoundary;
      /* Find out proper data range */
      VGetMinMaxValue(vXData,nLBoundary,nHBoundary,&dL,&dH);
      pTok=strtokbyindex(SWEEP,qDelimiter,0);
      if (pTok[0]!='*') dL=atof(pTok);
      freeEx(pTok);
      pTok=strtokbyindex(SWEEP,qDelimiter,1);
      if (pTok[0]!='*') dH=atof(pTok);
      freeEx(pTok);
      if (!GetFittingRange(vXData,nLBoundary,nHBoundary,nFitTotal,dL,dH,
         &nLBoundary,&nHBoundary)) {
         Echo("No valid range.¥n");
         goto N;
      }
      if                                  ((nHBoundary-nLBoundary+1)<nFitTotal)
nFitTotal=nHBoundary-nLBoundary+1;
      /* Echo various parameters */
      pL=dtostr(dL,"%.1z");
      pH=dtostr(dH,"%.1z");
      Echo("range(%dpts)=%s,%s¥n",nHBoundary-nLBoundary+1,pL,pH);
      freeEx(pL);
      freeEx(pH);
      /* Check Eox whether the change in sign is. [20031004] */
      nBoundary=2;
      aBoundary[0]=nLBoundary;
      aBoundary[1]=nHBoundary;
      for (j=nLBoundary;j<nHBoundary;j++) {
         if (SIGN(vXCopy[j])!=SIGN(vXCopy[j+1])) {
            nBoundary=3;
            aBoundary[1]=j+1;
            aBoundary[2]=nHBoundary;
            break;
         }
      }
      /* Fit by model */
      for (iModelIndex=0;iModelIndex<nModelTotal;iModelIndex++) { /* 20030820 */
         int nLFit,nHFit;
         void (*pFunc)();
```

```
        /* Set Model ID */
        pTok=strtokbyindex(pArgument,qDelimiter,iModelIndex);
        nModelIndex=GetModelIndex(pTok);
        freeEx(pTok);
        /* Handle Boundary issue */
        iBoundary=0;
B:      nLFit=aBoundary[iBoundary++];
        nHFit=aBoundary[iBoundary];
        if (nBoundary==3&&iBoundary==1) nHFit--;
        /* Vector Copy */
        VCopy(vXMirror,vXData,nLFit,nHFit);
        VCopy(vYMirror,vYData,nLFit,nHFit);
        VCopy(vXMirror,vXCopy,nLFit,nHFit);
        VCopy(vYMirror,vYCopy,nLFit,nHFit);
        //vXData,vYData,nHFit

ComplyFittingVectorsWithModel(nModelIndex,vXData,vYData,nLFit,nHFit,dTox);
        //nGuess
        switch (nModelIndex) {
        case MODEL_OHM:     pFunc=_OHM;     nGuess=1;break;
        case MODEL_OHM2:    pFunc=_OHM;     nGuess=2;break;
        case MODEL_SCLCEXPONENTIAL:pFunc=_SCLCEXPONENTIAL;nGuess=2;break;
        case MODEL_SCLCUNIFORM:pFunc=_SCLCUNIFORM;nGuess=2;break;
        case MODEL_SCLCSQUARE:pFunc=_SCLCSHALLOW;nGuess=1;break;
        case MODEL_LAMPERT:  pFunc=_LAMPERT;  nGuess=2;break;
        case MODEL_SCLCCUBE:    pFunc=_SCLCCUBE;    nGuess=1;break;
        case MODEL_DT:      pFunc=_DT;      nGuess=2;break;
        case MODEL_DT_LEE2:  pFunc=_DTLEE2;     nGuess=3;break;
        case MODEL_FN:      pFunc=_FN;      nGuess=2;break;
        case MODEL_POOLE:    pFunc=_POOLE;    nGuess=2;break;
        case MODEL_SCHOTTKY: pFunc=_SCHOTTKY; nGuess=2;break;
        case MODEL_PF:      pFunc=_PF;      nGuess=2;break;
        case MODEL_STAT:     pFunc=_STAT;     nGuess=3;break;
        case MODEL_DTAT:     pFunc=_DTAT;     nGuess=2;break;
        }
R:      /* Fit first and expand. 20040110 */ {
        VECTOR vAns;
        VChangeBase2(&vXData,&vYData,nLFit,1);
        for (k=1;k<=nGuess;k++) vGuess[k]=1; /* 20040614 */
        dR2=xxmrqmin(vXData,vYData,nHFit-nLFit+1,vGuess,nGuess,pFunc,
           nFitTotal,dR2AtLeast,
           &vAns,&nRLAnswer,&nRHAnswer);
        nRLAnswer+=(nLFit-1);
        nRHAnswer+=(nLFit-1);
        VChangeBase2(&vXData,&vYData,1,nLFit);
        for (k=1;k<=nGuess;k++) vAnswer[k]=vAns[k];
        VDestroy(vAns,1,nGuess);
        if (dR2<dR2AtLeast) { /* 20031006 */
           if ((iBoundary+1)<nBoundary) goto B;
           /* else */ continue;
        }
        }
        /* I gave up applying this module. 2004.2.11 TT
        * Check the calculated current divergence with respect to data.
           If then, worthless. However, be careful this method is not complete.
```

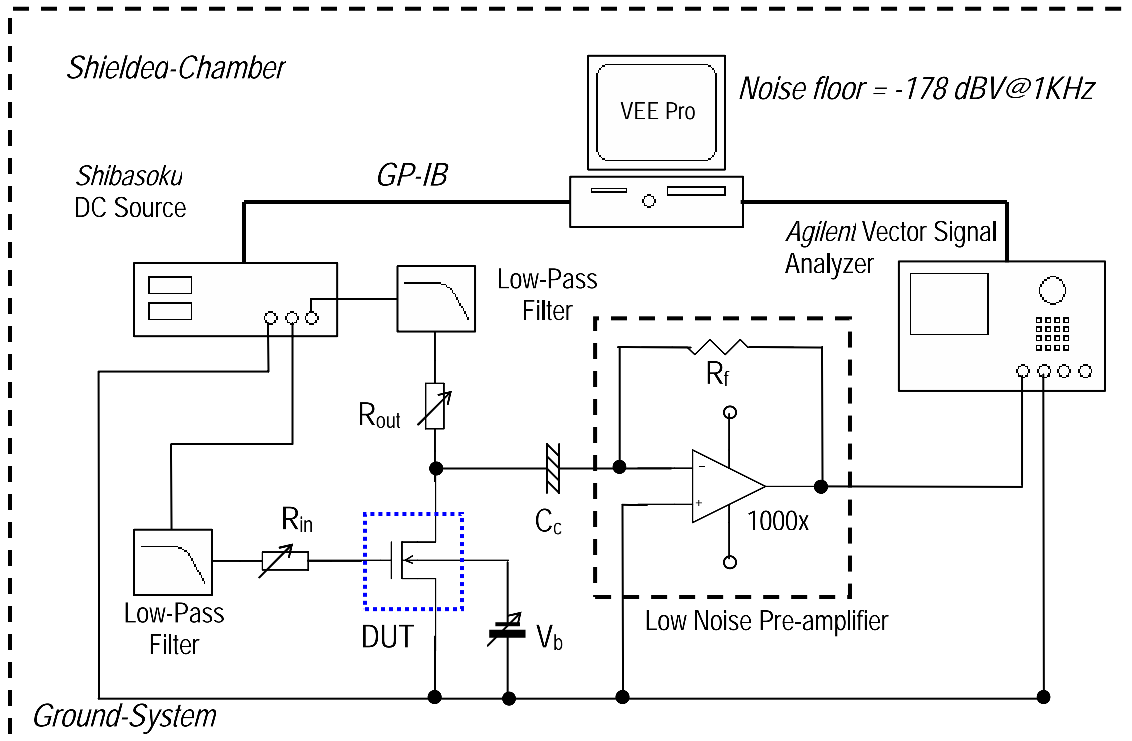
```
   Still have an hole.
   Check calculate current with extracted coeffs compared to the
   orginal data, always.
   20031003-4 * {
   int nCount=0;
   double dBase=12.,dYdata,dYcalc,dY,J,Eox,a,b;
   a=vAnswer[1];
   b=vAnswer[2];
   dYdata=dYcalc=0.;
   for (j=nLFit;j<=nHFit;j++) {
      Eox=(vXCopy[j]);
      dY=log(fabs(vYCopy[j]))+dBase;
      switch (nModelIndex) {
      case MODEL_OHM :     J=nGuess==1 ? a*Eox:a+b*Eox;break;
      case MODEL_SCLCEXPONENTIAL :J=a*pow(Eox,b+1.);break;
      case MODEL_SCLCUNIFORM :J=a*Eox*exp(b*Eox);break;
      case MODEL_SCLCSQUARE :J=a*pow(Eox,2.);break;
      case MODEL_LAMPERT :  J=a*Eox+b*pow(Eox,2.);break;
      case MODEL_SCLCCUBE :    J=a*pow(Eox,3.);break;
      case MODEL_DT :      J=a*sinh(3.13e7*b*fabs(Eox));break;
      case MODEL_FN :      J=a*pow(Eox,2.)*exp(-b/Eox);break;
      case MODEL_POOLE :    J=a*exp(b*Eox);break;
      case MODEL_SCHOTTKY : J=a*exp(b*sqrt(Eox));break;
      case MODEL_PF :      J=a*Eox*exp(b*sqrt(Eox));break;
      }
      J=SIGN(J)>0 ? log(fabs(J))+dBase:log(fabs(J))-dBase;
      if (J>dY) {
         dYdata+=dY;
         dYcalc+=J;
         nCount++;
      }
   }
   if (nCount) {
      dYdata/=nCount;
      dYcalc/=nCount;
      if ((dYcalc-dYdata)>=0.5) dR2=0.; // 0.5 order
   }
}
*/
/* Print out */ if (dR2>=dR2AtLeast) {
   const char *qName=qGetModelName(nModelIndex);
   char cEoxSign=SIGN(vXCopy[nLFit])>0 ? '+':'-';
   switch (nModelIndex) {
   case MODEL_OHM :
      Echo(" %s %c a=%.2e",qName,cEoxSign,vAnswer[1]);
      break;
   case MODEL_OHM2 :
      Echo(" %s %c a=%.2e yi=%.2e",qName,cEoxSign,vAnswer[2],vAnswer[1]);
      break;
   case MODEL_SCLCEXPONENTIAL:
      vAnswer[1]=exp(vAnswer[1]);
      vAnswer[2]-=1;
      Echo(" %s %c a=%.2e b=%.2e",qName,cEoxSign,vAnswer[1],vAnswer[2]);
      break;
   case MODEL_SCLCUNIFORM:
```

```
            vAnswer[1]=exp(vAnswer[1]);
            Echo(" %s %c a=%.2e b=%.2e",qName,cEoxSign,vAnswer[1],vAnswer[2]);
            break;
          case MODEL_SCLCSQUARE:
          case MODEL_SCLCCUBE:
            vAnswer[1]=exp(vAnswer[1]);
            Echo(" %s %c a=%.2e",qName,cEoxSign,vAnswer[1]);
            break;
          case MODEL_LAMPERT:
            vAnswer[1]=exp(vAnswer[1]);
            Echo(" %s %c a=%.2e b=%.2e",qName,cEoxSign,vAnswer[1],vAnswer[2]);
            break;
          case MODEL_DT:
            vAnswer[1]=exp(vAnswer[1]);
            Echo("                %s                  %c                  a=%.2e
b=%.2e",qName,cEoxSign,vAnswer[1],vAnswer[2]*3.125e7*dTox*dTox);
            break;
          case MODEL_DT_LEE2:
          case MODEL_FN:
          case MODEL_POOLE:
          case MODEL_SCHOTTKY:
          case MODEL_PF:
            vAnswer[1]=exp(vAnswer[1]);
            Echo(" %s %c a=%.2e b=%.2e",qName,cEoxSign,vAnswer[1],vAnswer[2]);
            break;
          case MODEL_STAT:
            vAnswer[1]=exp(vAnswer[1]);
            Echo("          %s          %c          a=%.2e          b(>0)=%.2e
c(>0)=%.2e",qName,cEoxSign,vAnswer[1],vAnswer[2],vAnswer[3]);
            break;
          case MODEL_DTAT:
            vAnswer[1]=exp(vAnswer[1]);
            Echo(" %s %c a=%.2e b=%.2e",qName,cEoxSign,vAnswer[1],vAnswer[2]);
            break;
          }

pL=dtostr(vXCopy[nRLAnswer]<vXCopy[nRHAnswer]?vXCopy[nRLAnswer]:vXCopy[nRHAnsw
er],"%.1z");

pH=dtostr(vXCopy[nRLAnswer]>vXCopy[nRHAnswer]?vXCopy[nRLAnswer]:vXCopy[nRHAnsw
er],"%.1z");
          Echo("          r2=%.3f          from          %d          pts
(%s..%s)¥n",dR2,nRHAnswer-nRLAnswer+1,pL,pH);
          freeEx(pL);
          freeEx(pH);
          /* Check validity */
          if (nModelIndex==MODEL_SCLCEXPONENTIAL) {
            Echo("   Tc[K]=%.1f ¥n",vAnswer[2]*dKelvin);
          } else if (nModelIndex==MODEL_DT) {
            /* vAnswer[2] <= a[2]=sqrt(MassRatio/BarrierHeight) */
            double dBarrier=dMRatio/SQUARE(vAnswer[2]);
            Echo("       tox[nm]=%.2f(arg)   m*/m0=%.2f(arg)   barrier[eV]=%.3g
Eox(ohm)[MV/cm]=%.2g ¥n",
              dTox*1e7,dMRatio,dBarrier,1e-6/(3.125e7*dTox*dTox*vAnswer[2]));
          } else if (nModelIndex==MODEL_DT_LEE2) {
```

```
            double dBarrier=vAnswer[3]*dTox;
            Echo("   tox[nm]=%.2f(arg) BH[eV]=%.3g ¥n",dTox*1e7,dBarrier);
         } else if (nModelIndex==MODEL_FN) { /* J=a[1]*Eox^2*exp(-a[2]/Eox) */
            double dK,dRatio,dBarrier;
            dK=vAnswer[1]*pow(vAnswer[2],2./3);

dRatio=4./9*pow(8*PI*KPlanck*dK/SQUARE(Qelectron),3.)/SQUARE(10.25e7);
            dBarrier=!_isnan(dRatio)                                        ?
pow(fabs(vAnswer[2])/(2./3*10.25e7*sqrt(dRatio)),2./3):0.;
            if (!_isnan(dRatio)&&1e-3<dRatio&&dRatio<10)
               Echo("   m*/m0=%.2f barrier[eV]=%.2f¥n",dRatio,dBarrier);
            //else
               Echo("   m*/m0=%.2f(arg) BH[eV]=%.2f¥n",

dMRatio,pow(fabs(vAnswer[2])/(2./3*10.25e7*sqrt(dMRatio)),2./3));
         } else if (nModelIndex==MODEL_POOLE) {
            double dTrapCenterDistance;

dTrapCenterDistance=vAnswer[2]/0.5*GetThermalVoltage(dKelvin)/cmoverA;
            Echo("                                                d[A]=%.2g
Nt[/cm^3]~%.2g¥n",dTrapCenterDistance,1/pow(dTrapCenterDistance*cmoverA,3));
         } else if (nModelIndex==MODEL_PF) {
            double dBeta,dRDC;
            dBeta=vAnswer[2]*GetThermalVoltage(dKelvin);
            dRDC=Qelectron/(PI*VacPermittivity*pow(dBeta,2));
            Echo("   betaPF[(Vcm)^0.5]=%.2e RDC[]=%.1f¥n",dBeta,dRDC);
         } else if (nModelIndex==MODEL_SCHOTTKY) {
            double dBeta,dRDC;
            dBeta=vAnswer[2]*GetThermalVoltage(dKelvin);
            dRDC=Qelectron/(4*PI*VacPermittivity*pow(dBeta,2));
            Echo("         betaS[(Vcm)^0.5]=%.2e   RDC[]=%.1f   RDC/4[]=%.1f
¥n",dBeta,dRDC,dRDC/4);
            /* Modified PF Equation : RDC/4
               1) M.Stuart,"Electrode-Limited to Bulk-Limited Conduction in
Silicon Oxide Films,"
               Phys.Stat.Sol.23,595(1967).
               2) J.G.Simmons,Phys.Rev,155,657(1967).
            */
         } else if (nModelIndex==MODEL_STAT) {
            if (vAnswer[3]>0) {
               double dBarrier;

dBarrier=vAnswer[3]/(4*sqrt(2*dMRatio*MFreeElectron)/(3*KReducedPlanck*Qelectr
on));
               dBarrier=pow(dBarrier,2./3)/Qelectron;
               Echo("   barrier[eV]=%.3f (%.3f)¥n",vAnswer[2]*dTox,dBarrier);
            } else {
               Echo("   barrier[eV]=%.3f¥n",vAnswer[2]*dTox);
            }
         } else if (nModelIndex==MODEL_DTAT) {
            double
dA=4*sqrt(2*Qelectron*dMRatio*MFreeElectron)/(3*KReducedPlanck);
            double dBarrier=pow(vAnswer[2]/dA,2./3);
            Echo("   barrier[eV]=%.3f¥n",dBarrier);
         }
```

```
        }
        /* Adjust fitted range to look up overlap region. 20031006 */ {
        /*
          int nLFitNew=nRHAnswer-(nFitTotal>>1)+2;
          int nHFitNew=nLFitNew+nFitTotal-1;
          if (nRLAnswer<nLFitNew&&nHFitNew<=nHFit) {
            nLFit=nLFitNew;
            nHFit=nHFitNew;
            goto R;
          }
          */
          /* Make it more simple and effective. 20040110 */
          j=nRHAnswer+(nFitTotal>>1)-nFitTotal;
          if (nRLAnswer<j&&(nRLAnswer+nFitTotal)<=aBoundary[iBoundary]) {
            nLFit=j;
            goto R;
          }
        }
        /* 20031005 */
        if ((iBoundary+1)<nBoundary)
          goto B;
      }
      /* Deallocate vXData,vYData,vXCopy */
N:    VDestroy(vXData,nVLow,nVHigh);
      VDestroy(vYData,nVLow,nVHigh);
      VDestroy(vXMirror,nVLow,nVHigh);
      VDestroy(vYMirror,nVLow,nVHigh);
      VDestroy(vXCopy,nVLow,nVHigh);
      VDestroy(vYCopy,nVLow,nVHigh);
  }

  freeEx(pArgument);
  return TRUE;
}

/******************************************************************************
*/
/* MosDiodeRegressor.c */
```

5. Schematic of 1/f Noise Measurement



6. Materials an Equipments in Experiment

Aluminum wire: 99.999% 0.1mm, made by Newmet Koch (A Division New Metals & Chemicals Ltd.)

La_2O_3 Target Fillet : made by ShinEtsu

Material	Method	Purity	Material	Method	Purity
La_2O_3	-	>99.999 wt%	Ho_2O_3	GDMS	<1 ppm
Y_2O_3	GDMS	<1 ppm	Er_2O_3	GDMS	<1 ppm
CeO_2	GDMS	1 ppm	Tm_2O_3	GDMS	<1 ppm
Pr_60_{11}	GDMS	<1 ppm	Yb_2O_3	GDMS	<1 ppm
Nd_2O_3	GDMS	<1 ppm	Lu_2O_3	GDMS	<1 ppm
Sm_2O_3	GDMS	<1 ppm	Ca	GDMS	3 ppm
Eu_2O_3	GDMS	<1 ppm	Fe	GDMS	<1 ppm
Gd_2O_3	GDMS	<1 ppm	Si	GDMS	10 ppm
Tb_4O_7	GDMS	<1 ppm			
Dy_2O_3	GDMS	<1 ppm	density	g/cm^3	4.111

7. ODC and SDC in Conduction Mechanisms

Type	Film	DC			Article
		ODC	SDC	CDC	
ODC	-	-	-	(PF)	J. Frenkel, Physical Review, 54, 647-48 (1938)
					L. Maissel and R. Glang, Handbook of Thin Film Technology, McGraw-Hill Book Company, 1970, p.14-29.
					R. Hill, Philosophical Magazine, 23, 59-86 (1971)
	SiO	-	-	(PF)	J. Simmons, Physical Review, 155(3), 657-60 (1967)
					A. Jonscher and A. Ansari, Philosophical Magazine, 8(23), 205-23 (1971)
	SiO_x	-	-	3.8 (PF)	I. Johansen, J. Appl. Phys., 37(2), 499-507 (1966)
	SiO_2	-	-	(SE)	A. Servini and K. Jonscher, Thin Solid Films, 3, 341-65 (1969)
	Si_3N_4	-	-	(PF)	J. Yeargan and H. Taylor, J. Appl. Phys., 39(12), 5600-04 (1968)
	$BaTa_2O_6$	2.4-2.9	-	1.8-2.1 (SE)	Y. Kim *et al.*, Solid-St. Elec., 43, 1189-93 (1999)
	Ta_2O_5	4.8	-	3.8-5.4 (PF)	C. Isobe and M. Saito, Appl. Phys. Lett., 56(10), 907-09 (1990)
		-	-	(PF)	C. Chaneliere *et al.*, J. Appl. Phys., 86(1), 480-86 (1999)
		~2.2	-	2.26-2.44 (PF)	M. Houssa *et al.*, J. Appl. Phys., 86(11), 6462-67 (1999)
	ZrO_2	-	-	(PF)	S. Ramanathan *et al.*, J. Appl. Phys., 91(7), 4521-27 (2002)

Type	Film	DC			Article
		ODC	SDC	CDC	
SDC	SiOC	-	3.0	3.18 (PF)	K.Yiang *et al.*, Appl. Phys. Lett., 83(3),526-28 (2003)
	$BaTiO_3$	-	9.9	11.2 (SE)	R.Avila *et al.*, Thin Solid Films, 348,44-48 (1999)
	Ta_2O_5	-	24.3	24.4 (PF)	F.Chiu *et al.*, J. Appl. Phys, 81(10),6911-15 (1997)
	Y_2O_3	-	9.3-9.6	10 (SE)	D.Basak and K. Sen,Thin Solid Films, 254,181-86 (1995)
Self-Consistent (Dynamic)	Si_3N_4	4	7	5.5 (PF)	S. Sze, J. Appl. Phys., 38(7), 2951-56 (1967)[a]
	SiO_2/Si_3N_4	-	7.5	6 (PF)	S. Berberich *et al.*, Diamond and Related Materials, 8(2-5), 305-8 (1999)
	Ta_2O_5	4	26	2.8-6.9 (PF)	C. Liu *et al.*, Materials Sci. and Eng. B, 106(3), 234-241 (2004)
		4.9	26.7	11.1 (PF)	G. Oehrlein, J. Appl. Phys., 59(5), 1587-95 (1986)
		8	4	14 (PF)	S. Chatterjee *et al.*, J. Phys. D: Appl.Phys., 36, 901-07 (2003)
		4	12.5-17.5	- (PF)	J. Lee *et al.*, Materials Chemistry and Physics, 77(1), 242-47 (2003)
		ε_{opt}<=CDC(PF)<$\varepsilon_{c\text{-}v}$(1MHz)			E. Atanassova *et al.*, Microelectronics Reliability, 45(1), 123-35 (2005)
	$SrTiO_3$	2.4^2	-	2^2 (SE)	C. Peng *et al.*, Appl. Phys. Lett., 63(8), 1038-40 (1993)

ODC = Optical Dielectric Constant / SDC = Static Dielectric Constant

PF = Poole-Frenkel Conduction / SE = Schottky Emission

[a] The dynamic dielectric constant obtained from the P-F plot should be between optical and static dielectric constants. If so, the value is self-consistent.

8. Conduction mechanisms found in high-*k* dielectrics

Oxide	Conduction	Fabrication	Article
HfO_2	SE,PF,FN	JVD	W.Zhu et al.,IEEE IEDM,463-66(2001).
	SE,PF,FN	JVD	W.Zhu et al., IEEE Elec.Dev.Lett.,23[2],97-99(2002).
	FN	E-beam evaporation	H.Ikeda et al., Jpn.J.Appl.Phys.,42,1949-53(2003).
	SILC	Ion-beam sputtering	D.Han et al.,Microelectronic Eng.,66,643-47(2003).
	DT	Plasma deposition	C.Hinkle et al.,Microelectronic Eng.,72,257-62(2004).
ZrO_2	PF,FN	PLD	T.Yamaguchi et.al.,IEEE IEDM,19-22 (2000).
	$SE^{@LF}$,$PF^{@HF}$	RTCVD	J.Chang and Y.Lin,Appl.Phys.Lett.,79[22],3666-68(2001).
	TAT	ALCVD	S.Jeon et al.,Jpn.J.Appl.Phys.,41,2390-93(2002).
	PF	UV-ozone oxidation	S.Ramanathan et al.,J.Appl.Phys.,91[7],4521-27(2002).
	PF	Reactive sputtering	W.Chim et al.,J.Appl.Phys.,93[8],4788-93(2003).
	PF,FN	PLD	T.Yamaguchi et al.,IEEE Trans.Elec.Dev.,51(5),774-79(2004).
Al_2O_3	SCLC	Al oxidation	T.Hickmott,J.Appl.Phys.,33[9],2669-82(1962).
	SCLC	Al oxidation	H.Birey,J.Appl.Phys.,49[5],2898-2904(1978).
	SCLC	Al oxidation	R.Gould and C.Hogarth, Thin Solid Films, 51, 237-50(1978).
	PF	AlN oxidation	J.Kolodzey et al., IEEE Trans. Elec. Dev., 47[1],121-28(2000).

SE = Schottky emission

JVD = Jet-vapor-deposition

PLD = Pulsed-laser-ablation deposition

RTCVD = Rapid thermal chemical vapor deposition

ALCVD = Atomic layer CVD

Publications and Presentations

1. Publications

(1) **Yongshik Kim**, Kunihiro Miyauchi, Shun-ichiro Ohmi, Kazuo Tsutsui, and Hiroshi Iwai, "Electrical Properties of Vacuum Annealed La_2O_3 Thin Films grown by E-Beam Evaporation," Microelectronics Journal, 36(1), pp 41-49 (2005).

(2) **Yongshik Kim**, Shun-ichiro Ohmi, Kazuo Tsutsui, and Hiroshi Iwai, "Space-Charge-Limited Currents in La_2O_3 Thin Films Deposited by E-Beam Evaporation after Low Temperature Dry-Nitrogen Annealing," Japanese Journal of Applied Physics. **Submitted on 16 May 2004**. **In press.**

(3) **Yongshik Kim**, Shun-ichiro Ohmi, Kazuo Tsutsui, and Hiroshi Iwai, "Analysis of Variation in Leakage Currents of Lanthana Thin Films," Solid State Electronics. **Submitted on 6 June 2004. In press.**

(4) E.Miranda, J.Molina, **Y.Kim**, and H.Iwai, "Modeling of the tunneling current in sub-5 nm La_2O_3 gate oxides," submitted to IEEE Elec. Dev. Lett., in July 2004.

(5) E.Miranda, J.Molina, **Y.Kim**, and H.Iwai, "Effects of high-field electrical stress on

the conduction properties of ultra-thin La_2O_3 films," submitted to Appl. Phys. Lett., in October 2004.

2. International conference

(1) **Y.Kim**, S.Ohmi, K.Tsutsui, and H.Iwai, "Electrical Conduction Processes in Lanthana Thin Films prepared by E-Beam Evaporation," 206th ECS symposium, Honolulu, Hawaii, USA, 2-8 October 2004. Published on pp.452-53 of Proceedings PV2004-04: Dielectrics for Nanosystems: Materials Science, Processing, Reliability, and Manufacturing.

(2) **Y.Kim**, S.Ohmi, K.Tsutsui, and H.Iwai, "Space-Charge-Limited Current Conductions in La2O3 Thin Films Deposited by E-Beam Evaporation after Low Temperature Dry-Nitrogen Annealing," ESSDERC/ESSCIRC Symposium, Leuven, Belgium 21-23 September 2004. Published on pp.81-84 of 2004 ESSDERC Proceedings.

(3) **Y.Kim**, A.Kuriyama, I.Ueda, S.Ohmi, K.Tsutsui, and H.Iwai, "Electrical Characteristics of High-k La_2O_3 Thin Film Deposited by E-Beam Evaporation Method," 204th ECS symposium, Orlando, Florida, USA, 12-16 October 2003. Published on pp.441-52 of Proceedings PV2003-22: Physics and Technology of High-k Gate Dielectrics II.

(4) **Y.Kim**, S.Ohmi, K.Tsutsui, and H.Iwai, "Analysis of Electrical Characteristics of

La_2O_3 Thin Films Annealed in Vacuum and Others," ESSDERC/ESSCIRC Symposium, Estoril, Portugal, 16-18 September 2003. Published on pp.569-72 of 2003 ESSDERC Proceedings.

(5) Ikumi Kashiwagi, Chizuru Ohshima, **Yongshik Kim**, Shun-ichiro Ohmi, Kazuo Tsutsui and Hiroshi Iwai, "Dependence of Gd_2O_3 Thin Film Properties on Si Substrate Orientation," IEEE Workshop on Microelectronics and Electron Devices (uE-ED2002), Ameritel Inn, Boise, Idaho, USA, 25 October 2002.

(6) H.Iwai, S.Ohmi, S.Akama, C.Ohshima, A.Kikuchi, I.Kashiwagi, J.Taguchi, H.Yamamoto, J.Tonotani, **Y.Kim**, I.Ueda, A.Kuriyama, and Y.Hoshihara, "Advanced Gate Dielectric Materials for Sub-100nm CMOS," IEEE IEDM, 625-28, 2002.

3. Domestic conference

(1) **Y.Kim**, I.Kashiwagi, S.Ohmi, K.Tsutsui, H.Iwai, "Characterization of high-k rare earth oxide films deposited on various si substrates", Japanese Society of Applied Physics, 63rd Fall Meeting, Nigata university, Nigata ken, 24-27 September, 2002.

(2) **Y.Kim**, S.Ohmi, K.Tsutsui, H.Iwai, "Electrical characteristics of high-k La_2O_3 thin film deposited by MBE", Japanese Society of Applied Physics, 50th Spring Meeting, Kanagawa university, Yokohama, 27-29 March 2003.

(3) K.Miyauchi, **Y.Kim**, S.Ohmi, K.Tsutsui, H.Iwai, "Leakage current characteristics of high-k La2O3 thin film deposited by e-beam evaporation", Japanese Society of Applied Physics, 64th Fall Meeting, Hukuoka university, Hukuoka ken, 29 August to 2 September 2003.

(4) **Y.Kim**, S.Ohmi, K.Tsutsui, H.Iwai, "Leakage mechanisms of high-k La_2O_3 thin film deposited by MBE", Japanese Society of Applied Physics, 51st Spring Meeting, Tokyo university of technology, Tokyo do, 28-31 March 2004.

(5) **Y.Kim**, A.Fukuyama, S.Ohmi, K.Tsutsui, H.Iwai, "Leakage mechanisms of high-k La_2O_3 thin film deposited by MBE", Japanese Society of Applied Physics, 65th Fall Meeting, Tohuku university, Sendai, 1-4 September 2004.

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