Direct Contact of High-k/Si Gate Stack for EOT below 0.7 nm using LaCe-silicate Layer with V_{fb} controllability

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Abstract

A direct high-k/Si gate stack has been proposed for gate oxide scaling. With LaCe-silicate, an EOT of 0.64 nm with an average dielectric constant (k_{av}) of 17.4 has been obtained and an extremely low gate leakage current (J_g) of 0.65 A/cm^2. The flatband voltage (V_{fb}) can be controlled by the compositional ratio of La in the LaCe-silicate layer. Furthermore, incorporation of Ge atom into the silicate layer can effectively shift the V_{fb} to positive direction.

Introduction

The scaling in gate dielectric below equivalent oxide thickness (EOT) of 0.7 nm essentially requires a technique to directly contact high-k dielectrics to Si substrate with good interfacial property [1]. Several techniques, including cycle deposition and annealing, or oxygen scavenging process, have been so far reported to achieve a direct contact of high-k/Si structure [2,3]. The high-k/Si interface with HfO_2 is sensitive to the oxygen partial pressure during the process, so that one must choose a process within a window to achieve a direct high-k/Si structure (Fig.1). On the other hand, La_2O_3 can achieve a direct high-k/Si interface by forming a silicate layer with fairly nice interface properties [4]. However, the excess formation of silicate results in the increase in EOT. CeO_2 has an advantage in the wide process window to achieve a direct high-k/Si interface. In terms of gate leakage current (J_g), silicates have advantage in widening the band gap at the cost of EOT (Fig.2). Therefore, this work focuses on the combination of a Si-rich Ce-silicate with La_2O_3 to achieve a direct high-k/Si interface with both reduction in J_g and EOT.

Experimental

MOS capacitors and transistors were fabricated on HF-last n-type Si (100) substrates (Fig.3). A thin layer of CeO_2 followed by La_2O_3 layer was successively deposited by MBE in an ultra high vacuum chamber. A sputter deposited metal gate stack of W(4 nm) and $TaSi_2$ (36 nm) was *in situ* deposited on the high-k. All samples went through 800 °C for 2 sec by rapid thermal annealing. The intermixing of La and Ce atoms were confirmed by XPS analysis, especially when annealed at high temperature (Fig.4).

Results and Discussion

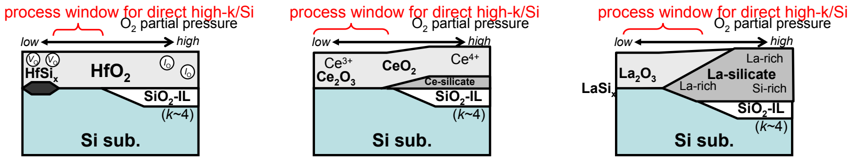
Cross sectional TEM image of LaCe-silicate layer formed by stacking and annealing of La_2O_3/CeO_2(2.7/1nm) shows a direct high-k/Si structure with a uniform contrast without any μ-crystallization (Fig.5). The formation of a LaCe-silicate layer was confirmed by x-ray photoelectron Si 1*s* spectra (Fig.6). Fig.7 shows the capacitance-voltage (*C-V*) characteristics of the capacitors with different amount of La_2O_3 by changing the stacking thickness on a 1-nm thick CeO_2 layer. Conductance method revealed that the interfacial state densities (D_{it}) were ~10^{11} cm^{-2}/eV. While increasing the thickness of La_2O_3 from 2.1 to 2.7 nm, an increase in accumulation capacitances was observed. The EOT dependence on the La_2O_3 thickness revealed a minimum point at La_2O_3 thickness of 2.7 nm, where the smallest EOT of 0.64 nm, corresponding to a k_{av} of 17.4, was obtained (Fig.8). Owing to the increase in k_{av} accompanied by possible increase in the conduction band (CB) offset, the smallest J_g was obtained with a La_2O_3 thickness of 2.7 nm (Fig.9). The J_g at V_g=1V decreased even with reducing the EOT (Fig.10). The composition of the silicate layer can be considered as $La_{1.5}Ce_{0.5}SiO_5$. The flatband voltage (V_{fb}) showed a positive shift while increasing the amount of La_2O_3, indicating the possibility to control the V_{th} (Fig.11). Further positive V_{fb} shift can be achieved by sub-mono layer (ML) incorporation of Ge atoms into the oxide (Fig.12). An additional positive V_{fb} shift of 0.15 V can be obtained by combining the incorporation of Ge atoms with the amount of La_2O_3 without any cost in EOT (Fig.13). I_d-V_g characteristics of nFETs showed a positive shift in V_{th} by increasing the amount of La_2O_3, which is in good agreement with the shift observed with MOS capacitors. The subthreshold swings (SS) of the nFETs were within 80 mV/dec., indicating fairly nice interface property of LaCe-silicate/Si sub.

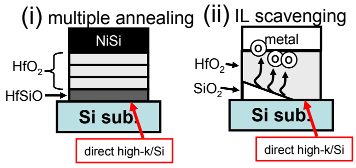
Conclusions

By employing La_2O_3 on a thin CeO_2, a direct high-k/Si gate stack can be achieved by forming a uniform LaCe-silicate gate dielectric. A dielectric constant of 17.4 with an excellent leakage current suppression and fairly nice interface properties has been obtained. An effective control of flatband voltage has been demonstrated by changing the composition of La atoms, and the incorporation of Ge atoms. LaCe-silicate can be a strong candidate to achieve a direct high-k/Si with large process window.

References

[1] ITRS 2008 update.
[2] M. Takahashi, et al., IEDM, p. 523 (2007).
[3] T. Ando, et al., IEDM, p. 423 (2009).
[4] K. Kakushima, et al., ESSDERC, p.126 (2008).





	Direct high-k/Si	High temperature annealing @high O_2 partial pressure
HfO_2	Small process window	Phase separation, SiO_2 formation
La_2O_3	Easy by silicate formation	excess silicate formation EOT growth
CeO_2	Under low oxygen partial pressure	SiO_2 formation

Fig.1 Control of O_2 partial pressure is essential to control the oxygen defects or the SiO_2 IL formation. Strategies to realize a direct high-k/Si gate stack with HfO_2 gate dielectric have been proposed. (i) cycle-deposition and annealing technique [2], (ii) oxygen scavenging technology by either oxides or metal to reduce the intentionally formed SiO_2-IL [3]. Table shows the advantage of CeO_2 over La_2O_3 and HfO_2 for direct high-k/Si structure.

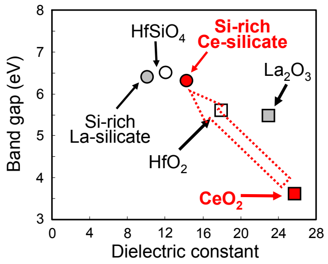


Fig.2 Summary of band gap and k of high-k gate dielectrics. This work focuses on the combination of La_2O_3 with Ce-silicate to suppress the SiO_2-IL growth, enabling higher k with reduced J_g.

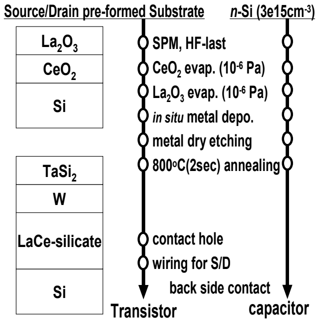


Fig.3 Fabrication process of MOS capacitors and transistors using gate last process.

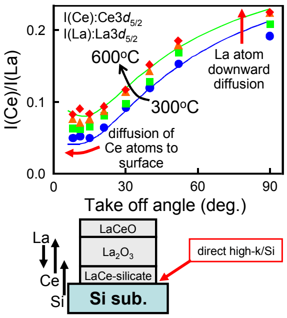


Fig.4 Intensity ratio of Ce 3$d_{5/2}$ to La 3$d_{5/2}$ by angle-resolved XPS analysis confirms the silicate layer and the intermixing of Ce and La atoms, especially when annealed at high temperature.

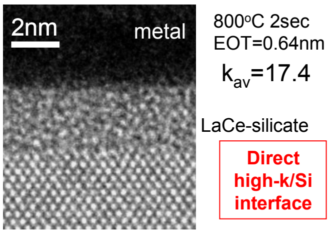


Fig.5 Cross sectional TEM image of La_2O_3/CeO_2 after annealing at 800 ºC. A direct high-k/Si structure is confirmed. A uniform contrast indicates a compositional uniformity.

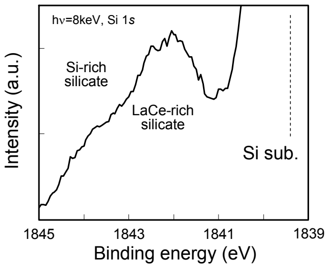


Fig.6 XP spectra of Si 1s of the sample shown in fig.5. LaCe-rich silicate was identified.

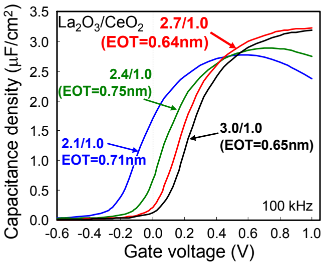


Fig.7 C-V characteristics with different La_2O_3 thickness on a 1-nm-thick CeO_2 layer. With La_2O_3 thickness of 2.7 nm, an EOT of 0.64 nm is achieved. Conductance method revealed the interfacial state density of ~10^{11} cm^{-2}/eV.

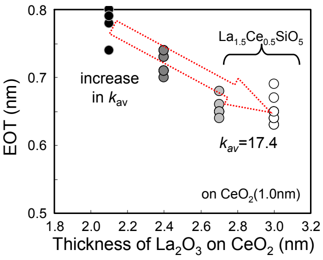


Fig.8 La_2O_3 thickness dependent EOT on a 1-nm thick CeO_2 after annealing at 800 ºC. With the increasing in La_2O_3 thickness, the reduction in EOT take place owing to the increase in k_{av}. A kav of 17.4 was obtained with La_2O_3 of 2.7 nm.

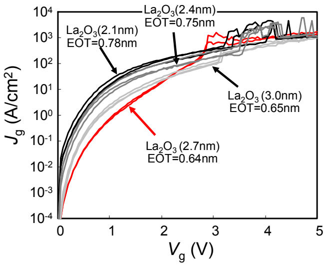


Fig.9 TZDB characteristics with different La_2O_3 thickness on a 1.0-nm thick CeO_x. La_2O_3 with a thickness of 2.7 nm showed the lowest J_g presumable due to optimum relation in the CB band offset with silicate thickness.

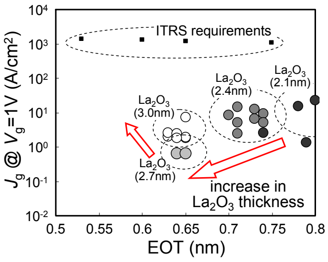


Fig.10 J_g-EOT relation with different La_2O_3 thickness on a 1.0-nm thick CeO_2. Reduction in J_g with smaller EOT can be obtained. A J_g of 0.51 A/cm² at EOT=0.64 nm was obtained, which is 10^4 times smaller than the ITRS requirements.

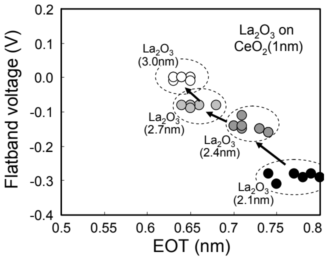


Fig.11 V_{fb} shift on EOT with different La_2O_3 thickness a 1.0-nm-thick CeO_2 layer. Positive shift in V_{fb} can be obtained by thickness control of La_2O_3 layer.

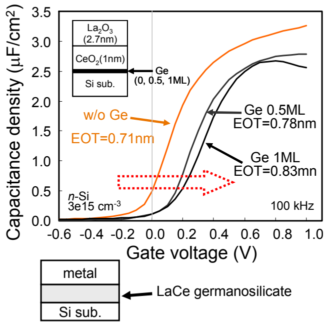


Fig.12 C-V characteristics with Ge of 0.5 and 1 ML at CeO_2/Si interface Further positive shift can be achieved by trace amount of Ge atoms.

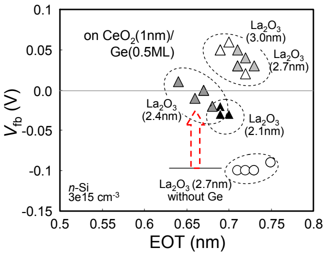


Fig.13 V_{fb} shift with different La_2O_3 thickness on a 1-nm thick CeO_2 with 0.5 ML of Ge atoms. Positive control in V_{fb} can be achieved without any degradation in the EOT.

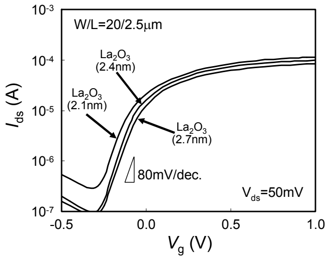


Fig.14 A shift in V_{th} was also confirmed with MOSFET. SS of 100 mV/dec. confirms a fairly nice interface property.