Direct Contact of High-k/Si Gate Stack for EOT below 0.7 nm using LaCe-silicate Layer with V<sub>fb</sub> controllability

Tokyo Institute of Technology, 4259, Nagatsuta, Midori-ku, Yokohama 226-8502, Japan
*Tokyo City University, 1-28-1, Tamazutsumi, Setagaya-ku, Tokyo 158-8557, Japan
**Waseda University, 513, Waseda Tsurumaki, Shinjyuku-ku, Tokyo 162-0041, Japan
Tel. +81-45-924-5847, Fax. +81-45-924-5846, kakushima@ep.titech.ac.jp

Abstract
A direct high-k/Si gate stack has been proposed for gate oxide scaling. With LaCe-silicate, an EOT of 0.64 nm with an average dielectric constant (k<sub>av</sub>) of 17.4 has been obtained and an extremely low gate leakage current (J<sub>g</sub>) of 0.65 A/cm². The flatband voltage (V<sub>fb</sub>) can be controlled by the compositional ratio of La in the LaCe-silicate layer. Furthermore, incorporation of Ge atom into the silicate layer can effectively shift the V<sub>fb</sub> to positive direction.

Introduction
The scaling in gate dielectric below equivalent oxide thickness (EOT) of 0.7 nm essentially requires a technique to directly contact high-k dielectrics to Si substrate with good interfacial property [1]. Several techniques, including cycle deposition and annealing, or oxygen scavenging process, have been so far reported to achieve a direct contact of high-k/Si structure [2,3]. The high-k/Si interface with HfO<sub>2</sub> is sensitive to the oxygen partial pressure during the process, so that one must choose a process within a window to achieve a direct high-k/Si structure (Fig.1). On the other hand, La<sub>2</sub>O<sub>3</sub> can achieve a direct contact high-k/Si structure with EOT dependence on the La<sub>2</sub>O<sub>3</sub> thickness revealed a minimum point at La<sub>2</sub>O<sub>3</sub> thickness of 2.7 nm, where the smallest EOT of 0.64 nm, corresponding to a k<sub>av</sub> of 17.4, was obtained (Fig.8). Owing to the increase in k<sub>av</sub> accompanied by possible increase in the conduction band (CB) offset, the smallest J<sub>g</sub> was obtained with a La<sub>2</sub>O<sub>3</sub> thickness of 2.7 nm (Fig.9). The J<sub>g</sub> at V<sub>y</sub>=1V decreased even with reducing the EOT (Fig.10). The composition of the silicate layer can be considered as La<sub>1-x</sub>Ce<sub>x</sub>SiO<sub>5</sub>. The flatband voltage (V<sub>fb</sub>) showed a positive shift while increasing the amount of La<sub>2</sub>O<sub>3</sub>, indicating the possibility to control the V<sub>fb</sub> (Fig.11). Further positive V<sub>fb</sub> shift can be achieved by sub-mono layer (ML) incorporation of Ge atoms into the oxide (Fig.12). An additional positive V<sub>fb</sub> shift of 0.15 V can be obtained by combining the incorporation of Ge atoms with the amount of La<sub>2</sub>O<sub>3</sub> without any cost in EOT (Fig.13). I<sub>d</sub>-V<sub>g</sub> characteristics of nFETs showed a positive shift in V<sub>fb</sub> by increasing the amount of La<sub>2</sub>O<sub>3</sub>, which is in good agreement with the shift observed with MOS capacitors. The subthreshold swings (SS) of the nFETs were within 80 mV/dec., indicating fairly nice interface property of LaCe-silicate/Si sub.

Experimental
MOS capacitors and transistors were fabricated on HF-last n-type Si (100) substrates (Fig.3). A thin layer of CeO<sub>2</sub> followed by La<sub>2</sub>O<sub>3</sub> layer was successively deposited by MBE in an ultra high vacuum chamber. A sputter deposited metal gate stack of W(4 nm) and TaSi<sub>2</sub> (36 nm) was in situ deposited on the high-k. All samples went through 800 °C for 2 sec by rapid thermal annealing. The intermixing of La and Ce atoms were confirmed by XPS analysis, especially when annealed at high temperature (Fig.4).

Results and Discussion
Cross sectional TEM image of LaCe-silicate layer formed by stacking and annealing of La<sub>2</sub>O<sub>3</sub>/CeO<sub>2</sub>(2.7/1nm) shows a direct high-k/Si structure with a uniform contrast without any μ-crystallization (Fig.5). The formation of a LaCe-silicate layer was confirmed by x-ray photoelectron Si 1s spectra (Fig.6). Fig.7 shows the capacitance-voltage (C-V) characteristics of the capacitors with different amount of La<sub>2</sub>O<sub>3</sub> by changing the stacking thickness on a 1-nm thick CeO<sub>2</sub> layer. Conductance method revealed that the interfacial state densities (D<sub>it</sub>) were ~10<sup>11</sup> cm<sup>-2</sup>/eV. While increasing the thickness of La<sub>2</sub>O<sub>3</sub> from 2.1 to 2.7 nm, an increase in accumulation capacitances was observed. The EOT dependence on the La<sub>2</sub>O<sub>3</sub> thickness revealed a minimum point at La<sub>2</sub>O<sub>3</sub> thickness of 2.7 nm, where the smallest EOT of 0.64 nm, corresponding to a k<sub>av</sub> of 17.4, was obtained (Fig.8). Further positive V<sub>fb</sub> shift can be achieved by sub-mono layer (ML) incorporation of Ge atoms into the oxide (Fig.12). An additional positive V<sub>fb</sub> shift of 0.15 V can be obtained by combining the incorporation of Ge atoms with the amount of La<sub>2</sub>O<sub>3</sub> without any cost in EOT (Fig.13). I<sub>d</sub>-V<sub>g</sub> characteristics of nFETs showed a positive shift in V<sub>fb</sub> by increasing the amount of La<sub>2</sub>O<sub>3</sub>, which is in good agreement with the shift observed with MOS capacitors. The subthreshold swings (SS) of the nFETs were within 80 mV/dec., indicating fairly nice interface property of LaCe-silicate/Si sub.

Conclusions
By employing La<sub>2</sub>O<sub>3</sub> on a thin CeO<sub>2</sub>, a direct high-k/Si gate stack can be achieved by forming a uniform LaCe-silicate gate dielectric. A dielectric constant of 17.4 with an excellent leakage current suppression and fairly nice interface properties has been obtained. An effective control of flatband voltage has been demonstrated by changing the composition of La atoms, and the incorporation of Ge atoms. LaCe-silicate can be a strong candidate to achieve a direct high-k/Si with large process window.

References
Fig. 1 Control of O₂ partial pressure is essential to control the oxygen defects or the SiO₂ IL formation. Strategies to realize a direct high-k/Si gate stack with HfO₂ gate dielectric have been proposed. (i) cycle-deposition and annealing technique [2], (ii) oxygen scavenging technology by either oxides or metal to reduce the intentionally formed SiO₂-IL [3]. Table shows the advantage of CeO₂ over La₂O₃ and HfO₂ for direct high-k/Si structure.

Fig. 2 Summary of band gap and k of high-k gate dielectrics. This work focuses on the combination of La₂O₃ with Ce-silicate to suppress the SiO₂-IL growth, enabling higher k with reduced Jₚ.

Fig. 3 Fabrication process of MOS capacitors and transistors using gate last process.

Fig. 4 Intensity ratio of Ce 3d₉/2, La 3d₉/2 by angle-resolved XPS analysis of the silicate layer and the intermixing of Ce and La atoms, especially when annealed at high temperature.

Fig. 5 Cross sectional TEM image of La₂O₃/CeO₂ after annealing at 800 °C. A direct high-k/Si structure is confirmed. A uniform contrast indicates a compositional uniformity.

Fig. 6 XP spectra of Si 1s of the sample shown in fig. 5. LaCe-rich silicate was identified.

Fig. 7 C-V characteristics with different La₂O₃ thickness on a 1-nm-thick CeO₂ layer. With La₂O₃ thickness of 2.7 nm, an EOT of 0.64 nm is achieved. Conductance method revealed the interfacial state density of ~10¹ⁱ cm⁻²/ev.

Fig. 8 La₂O₃ thickness dependent EOT on a 1-nm thick CeO₂ after annealing at 800 °C. With the increasing in La₂O₃ thickness, the reduction in EOT take place owing to the increase in kₐ. A kav of 17.4 was obtained with La₂O₃ of 2.7 nm.

Fig. 9 TDBB characteristics with different La₂O₃ thickness on a 1.0-nm thick CeO₂/La₂O₃ with a thickness of 2.7 nm showed the lowest Jₚ presumable due to optimum relation in the CB band offset with silicate thickness.

Fig. 10 Jₚ-EOT relation with different La₂O₃ thickness on a 1.0-nm thick CeO₂. Reduction in Jₚ with smaller EOT can be obtained. A Jₚ of 0.51 A/cm² at EOT=0.64 nm was obtained, which is 10⁴ times smaller than the ITRS requirements.