Future of Micro/Nano Electronics

August 12, 2011

@University of Science and Technology China
Hafei, China

Hiroshi Iwai,
Tokyo Institute of Technology

Tokyo Institute of Technology

Founded in 1881, Promoted to Univ. 1929

Institute Overview

Einstein Visit

Established in 1881→ 130th anniversary in 2011

3 undergraduate schools

School of Science, School of Engineering, School of Bioscience and Biotechnology

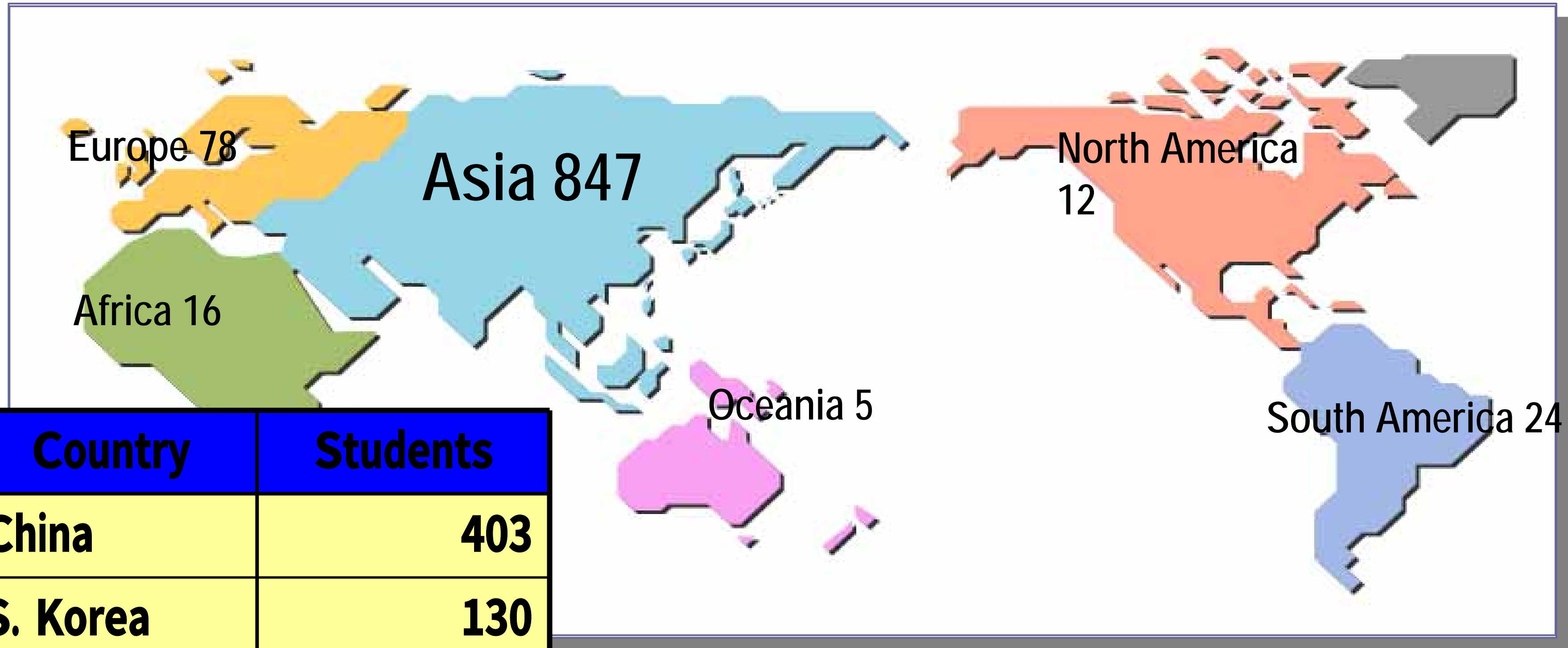
7 graduate schools

Science and Engineering Science, Science and Engineering Technology,
Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

	Undergraduate	Graduate	Master's	Doctoral	Teaching Staff	Student/Instructor	Staff
Tokyo Inst.	**5,000**	**5,000**	**3,500**	**1,500**	**1,200**	**8.3**	**550**
Per Year	**1,200**		**1,800**	**500**			

International Students



Country	Students
China	403
S. Korea	130
Indonesia	64
Thailand	55
Vietnam	60
Malaysia	28

Total 982

(As of May. 1, 2005)

東京工業大学大学院
総合理工学研究科

複合創造領域

Innovative Platform for Education and Research

先端ナノエレクトロニクス研究コアユニット研究室メンバー

Nanoelectronics Research Frontier Core Unit

（2010年10月1日現在）

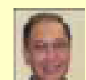
物理電子システム創造専攻
教授　岩井　洋

物理電子システム創造専攻
教授　筒井　一生

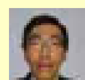
物理電子システム創造専攻
准教授　大見　俊一郎

フロンティア研究機構
特任准教授
アヘメト　パールハット

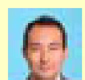
教員（10人）


Simon Min Sze
（客員教授）

（客員教授）


（特任教授）

（連携教授）


（連携教授）

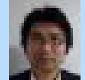
（助教）

技術員（1人）

博士研究員（1人）

Milan Kumar Bera

博士学生（19人）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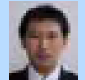
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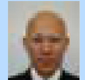
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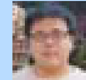
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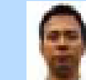
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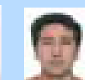
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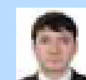
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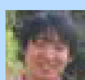
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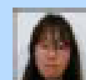
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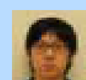
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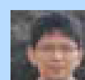
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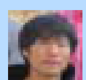
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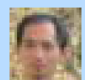
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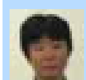
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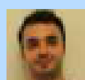
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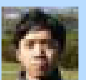
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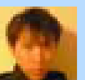
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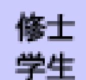
修士学生（26人）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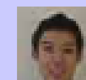
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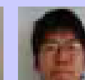
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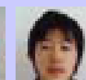
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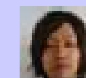
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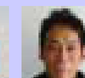
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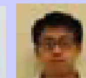
Dou Chunmeng
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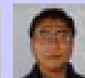
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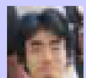
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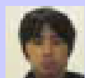
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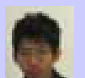
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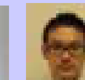
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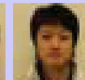
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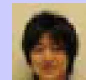
Li Wei
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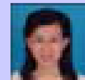
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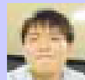
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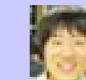
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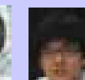
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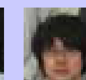
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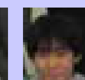
学部生（3人）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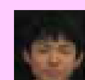
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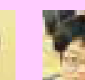
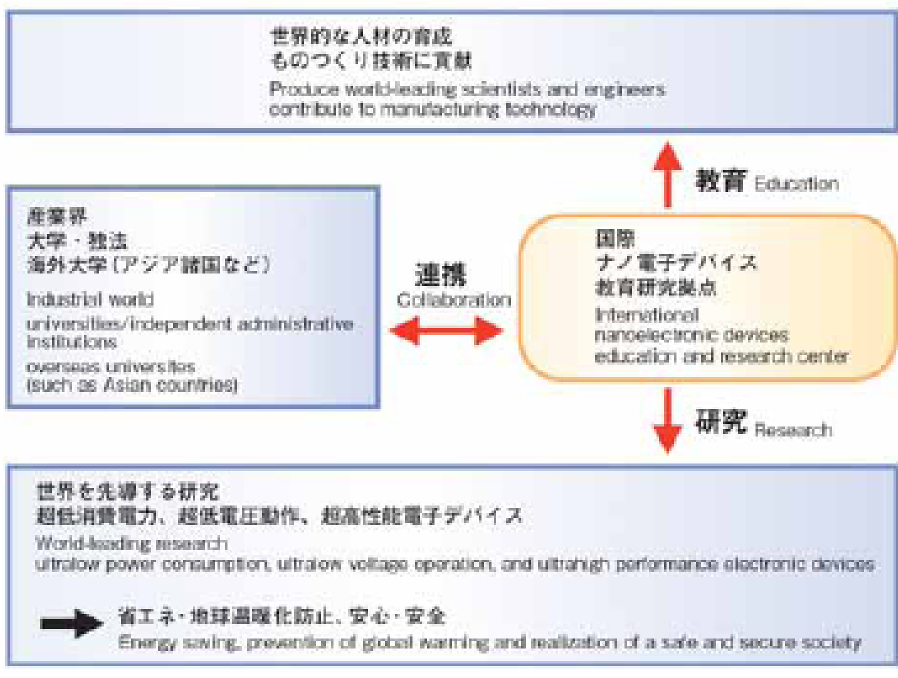
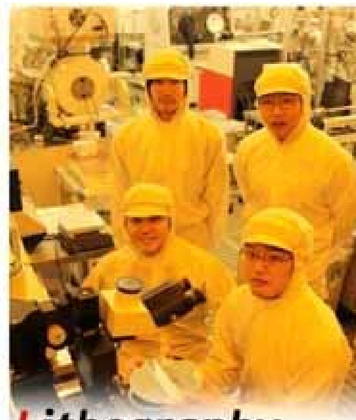
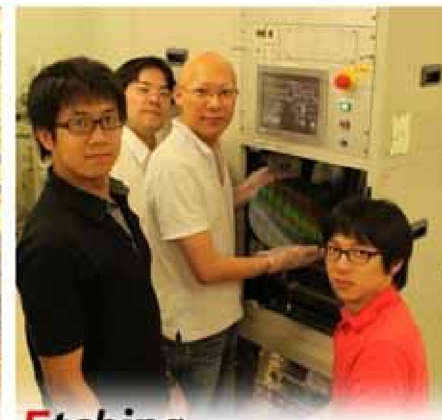
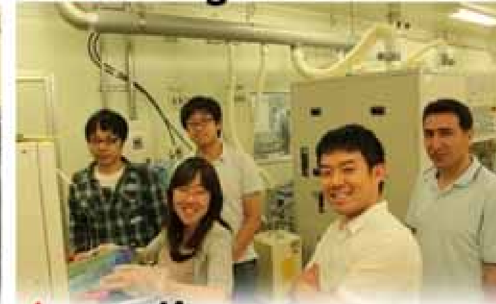




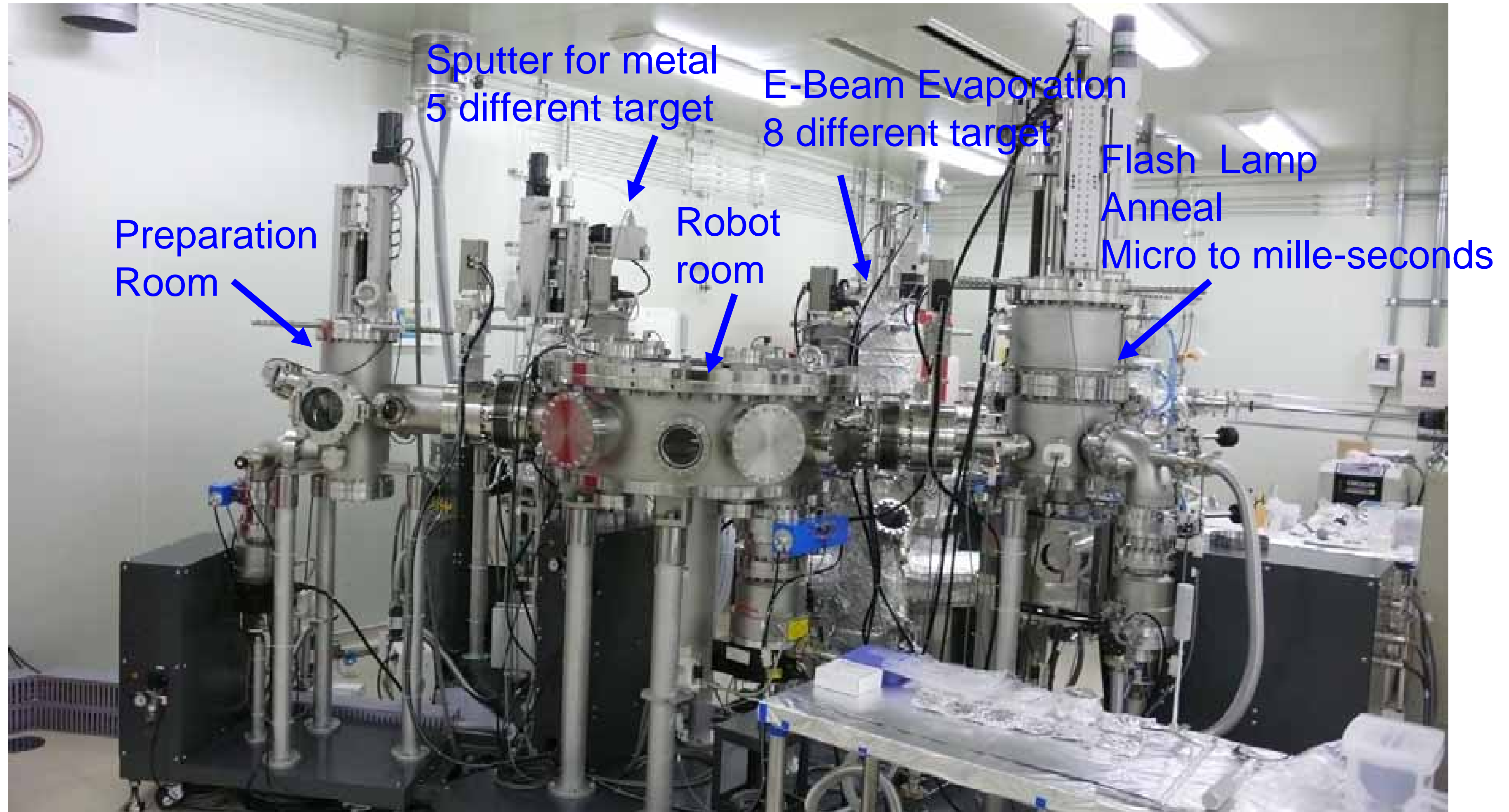
研究風景







Cluster tool for high-k thin film deposition



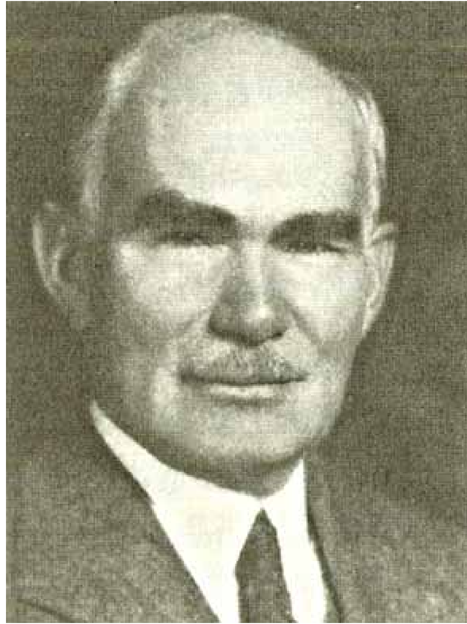
- There were many inventions in the 20th century:

  Airplane, Nuclear Power generation, Computer,

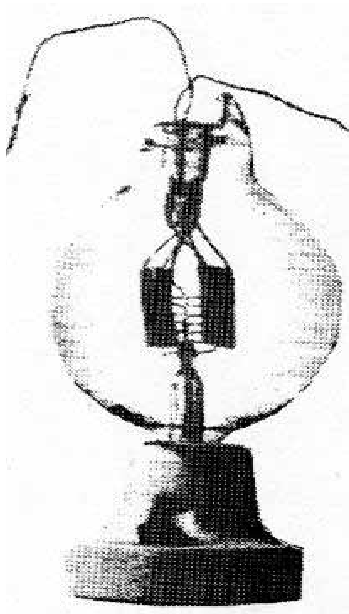
  Space aircraft, etc
- However, everything has to be controlled by electronics
- Electronics

  Most important invention in the 20th century
- What is Electronics: To use electrons,

  Electronic Circuits

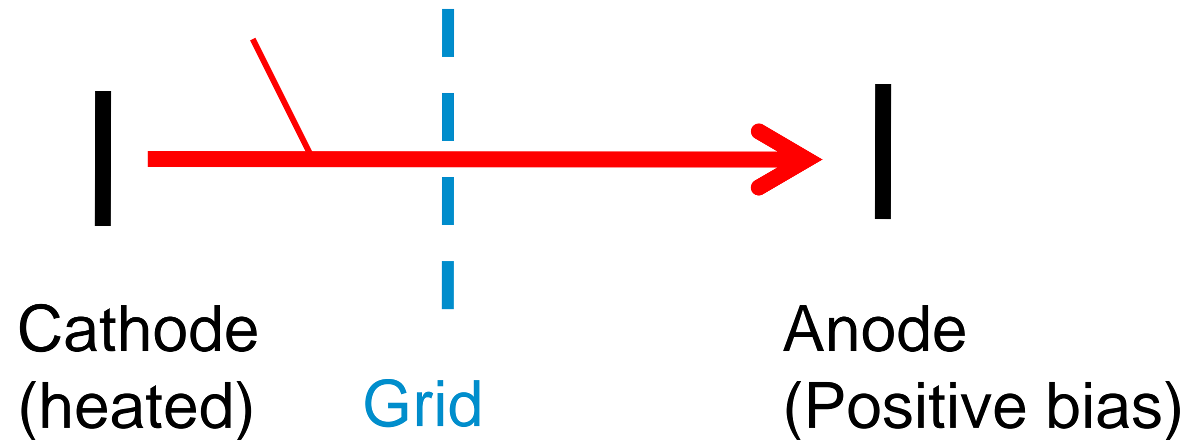


Lee De Forest



Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias



Same mechanism as that of transistor

First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

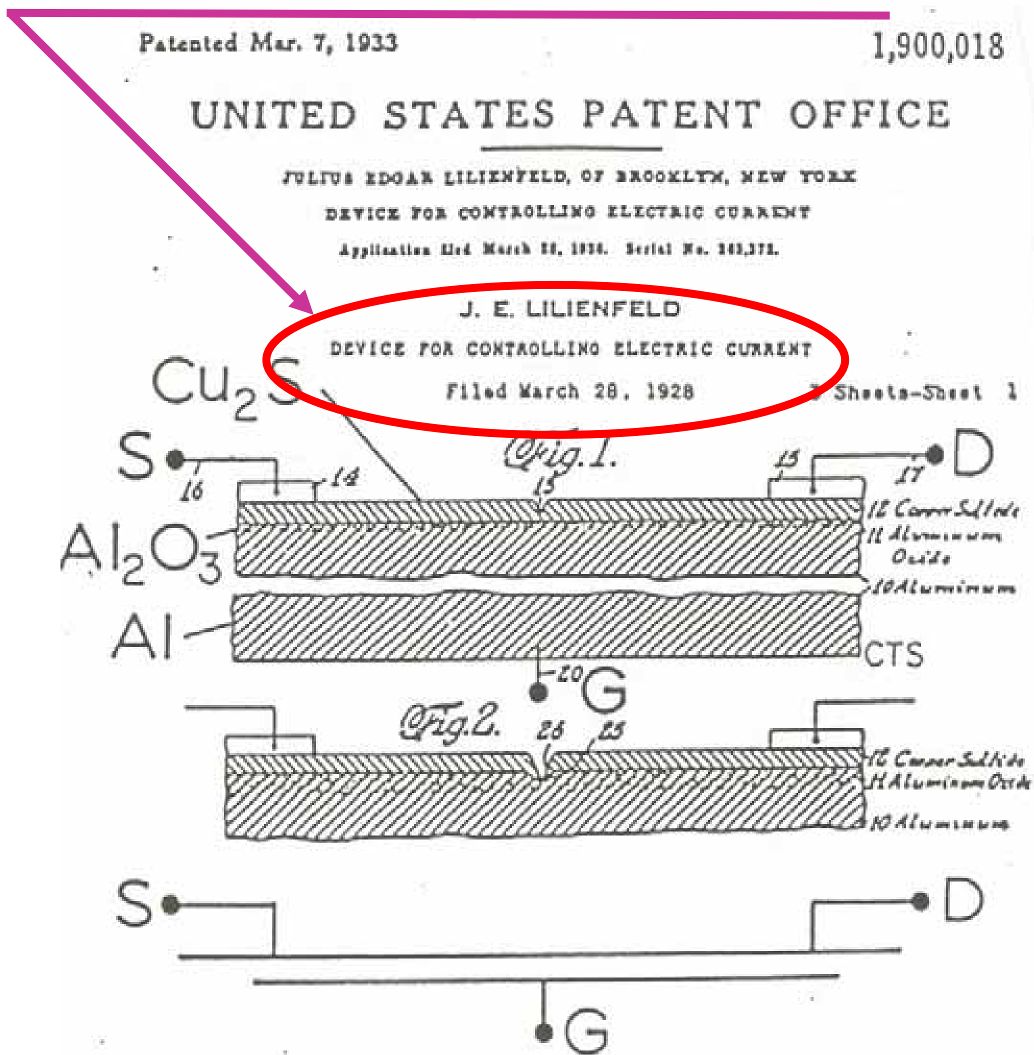
→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

J. E. LILIENFELD

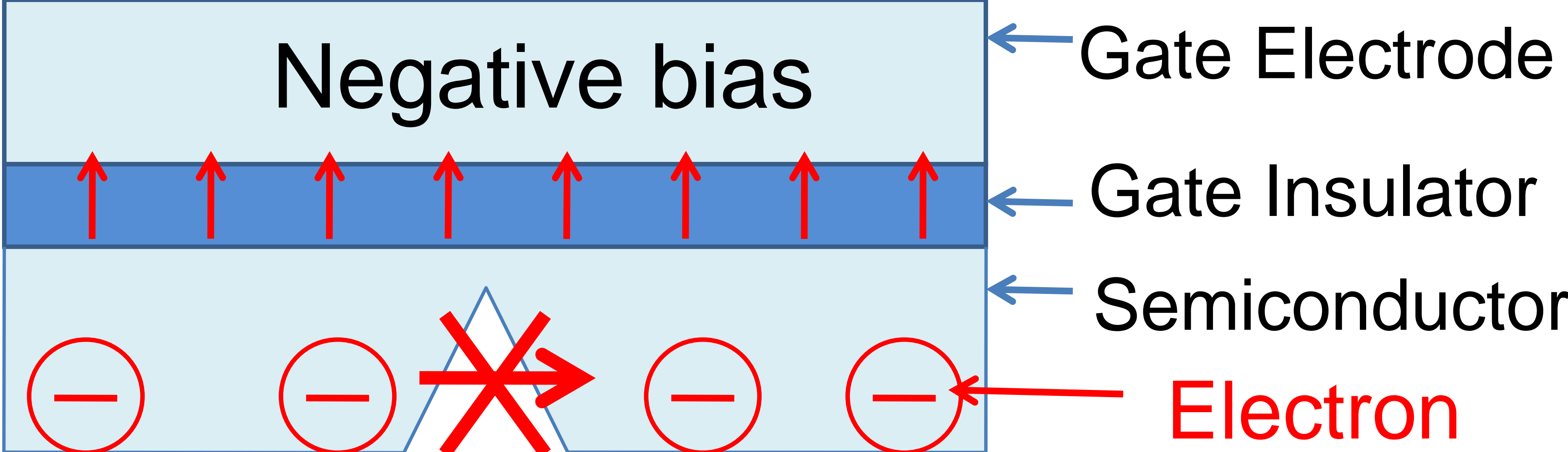
DEVICES FOR CONTROLLED ELECTRIC CURRENT

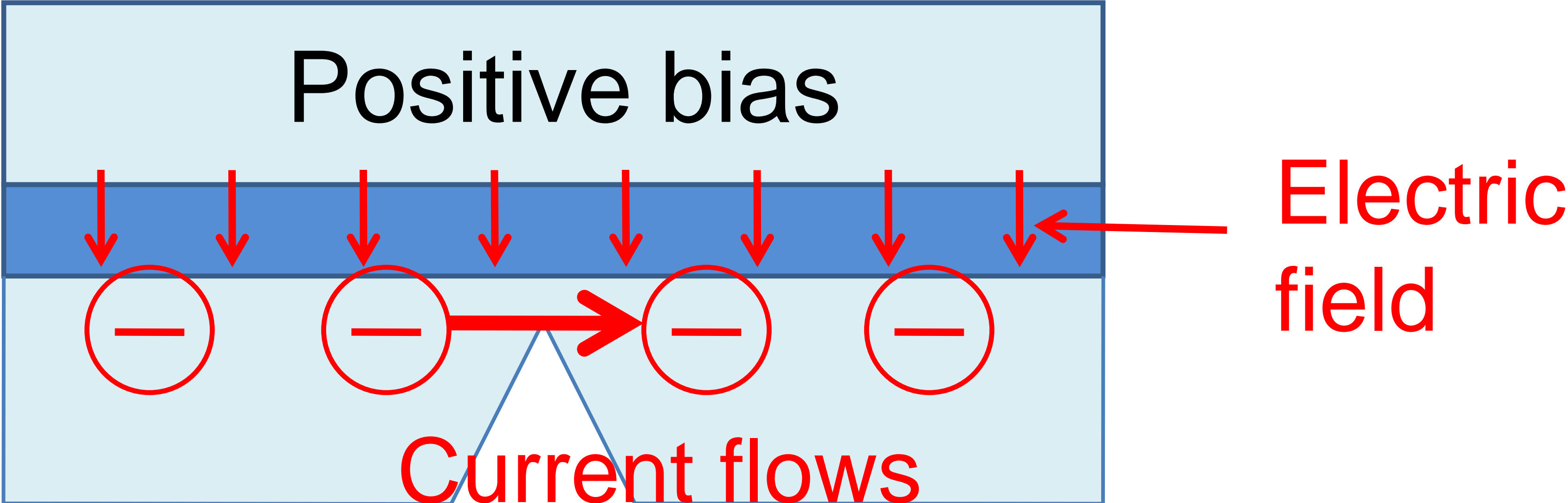
Filed March 28, 1928

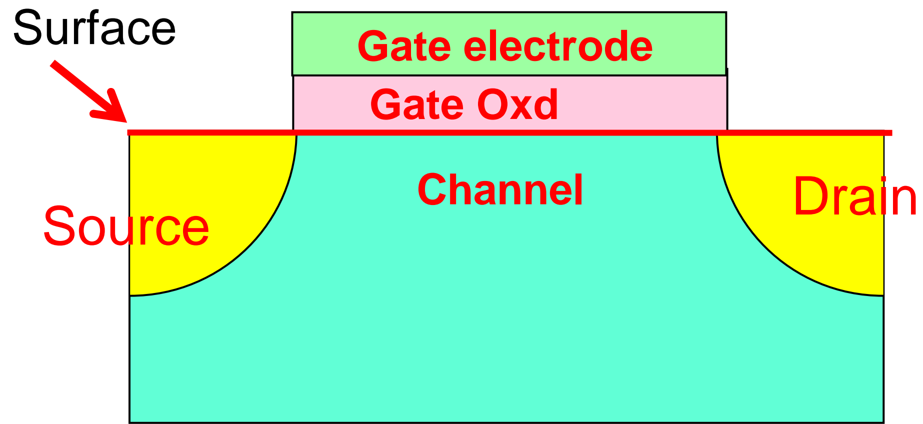


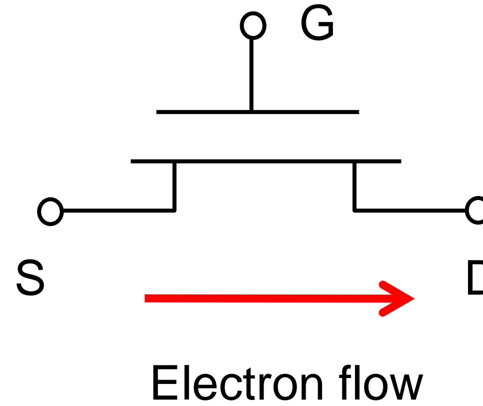
J.E.LILIENFELD

Capacitor structure with notch



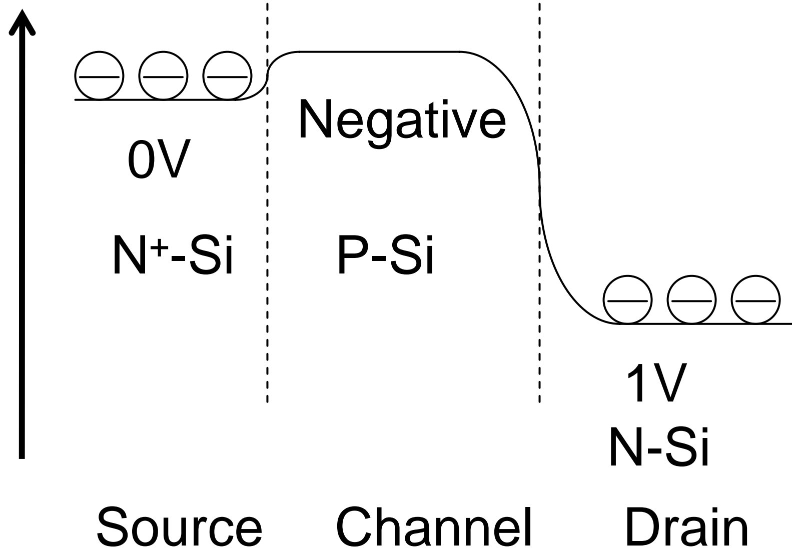




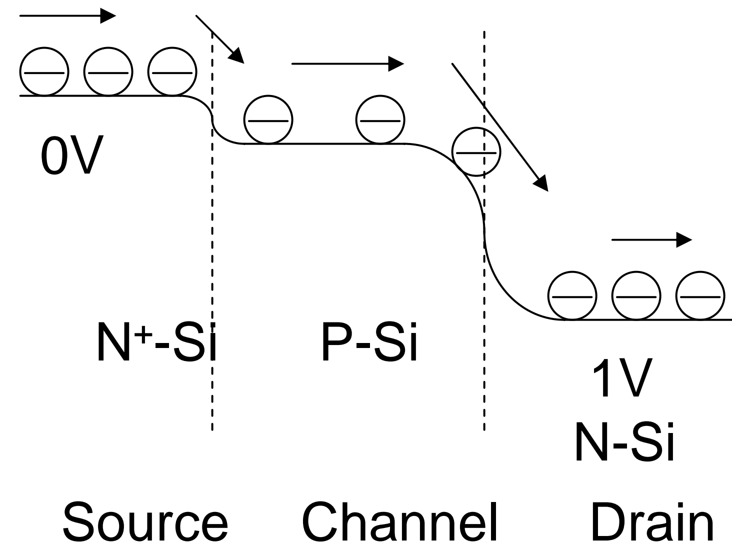


0 bias for gate

Surface Potential (Negative direction)



Positive bias for gate

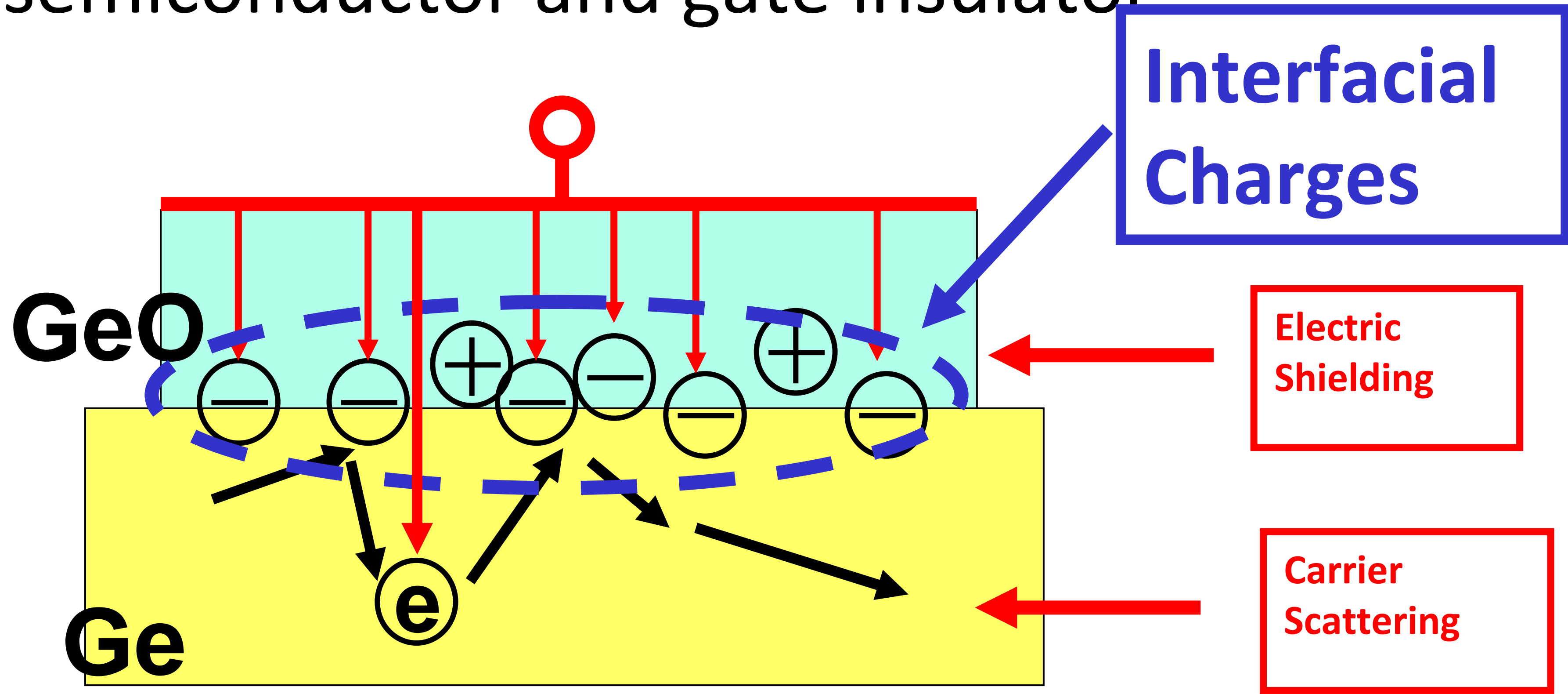


However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!

Very bad interface property between the semiconductor and gate insulator

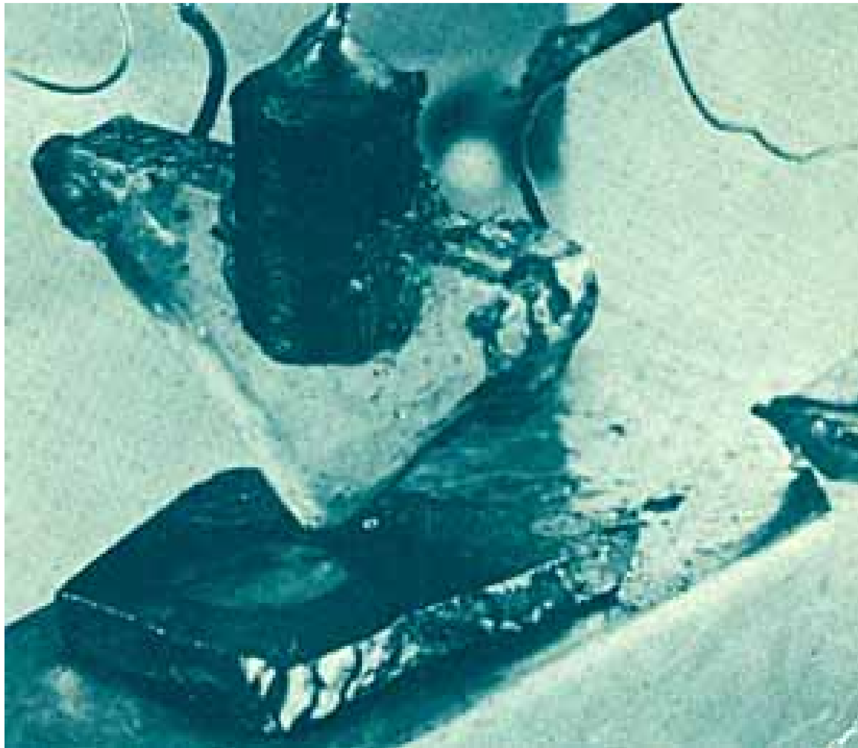


Drain Current was several orders of magnitude smaller than expected

Even Shockley!

However, they found amplification phenomenon when investigating Ge surface when putting needles.
This is the 1st Transistor:
Not Field Effect Transistor,
But Bipolar Transistor (another mechanism)

1947: 1st transistor



Bipolar using Ge

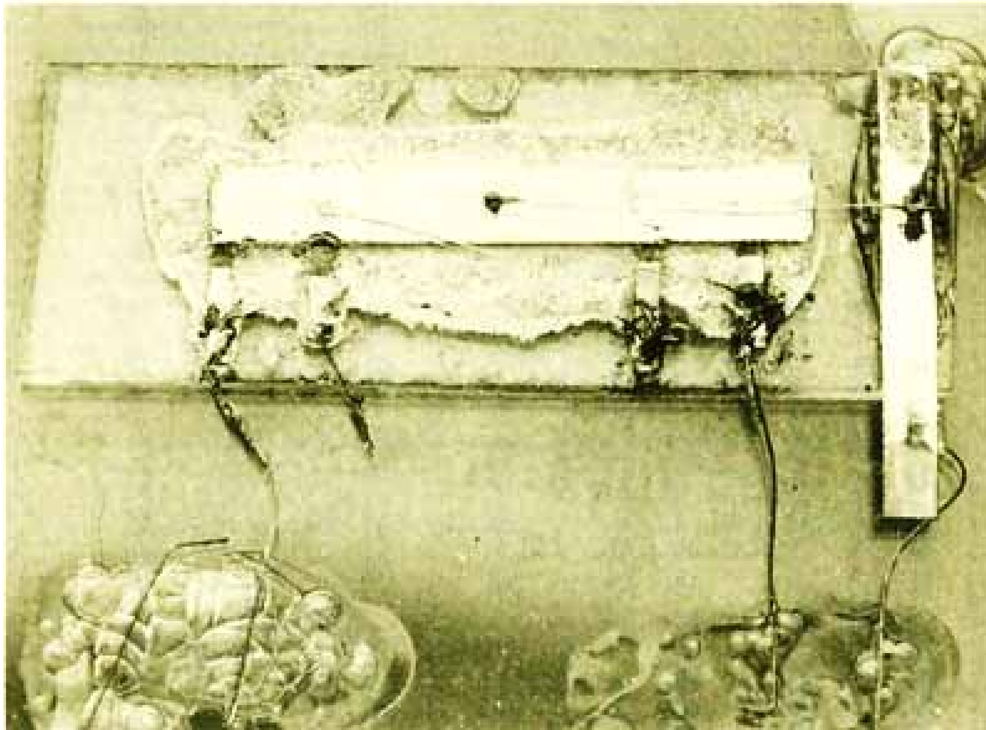
J. Bardeen W. Bratten,

W. Shockley

1958: 1st Integrated Circuit

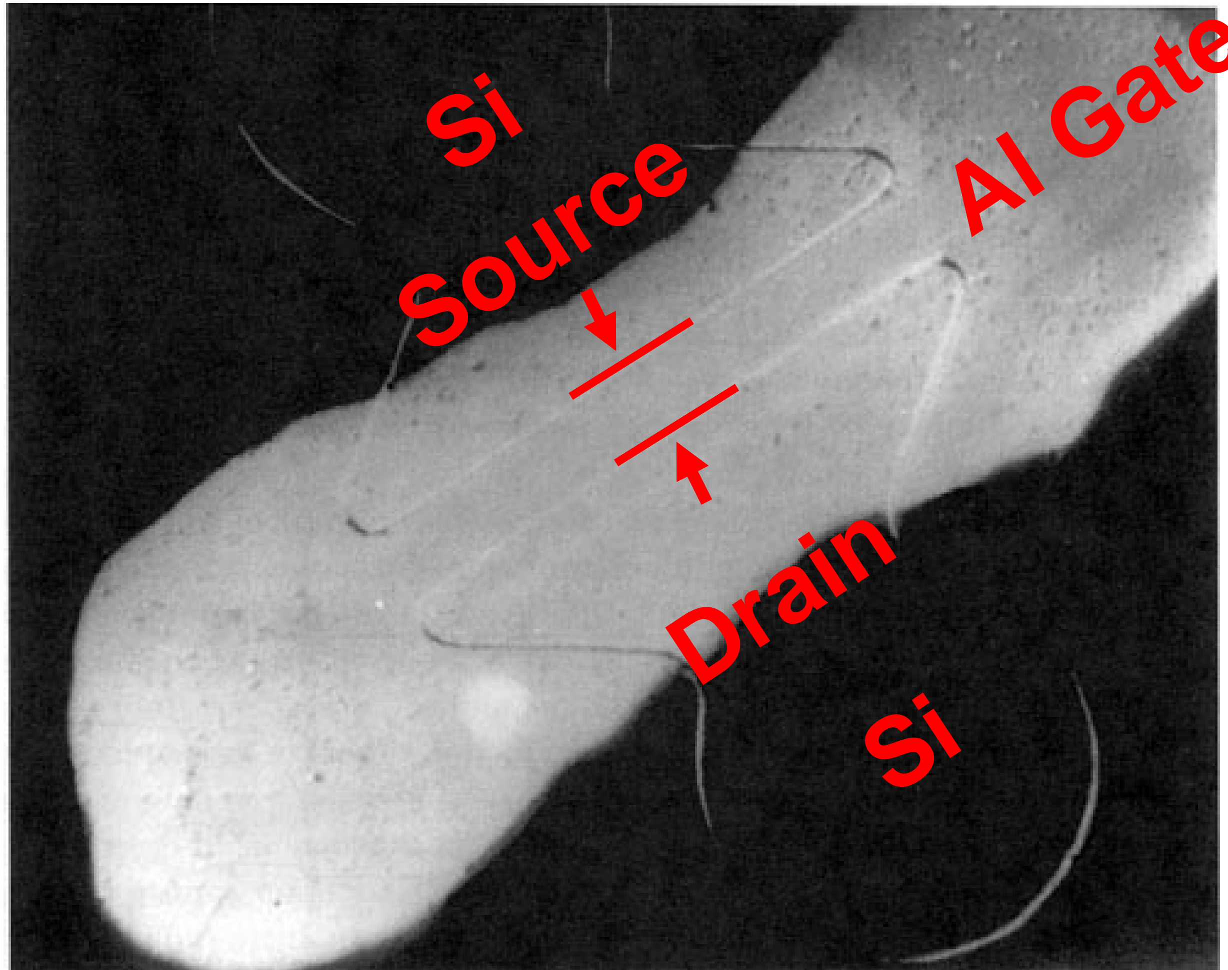
Jack S. Kilby

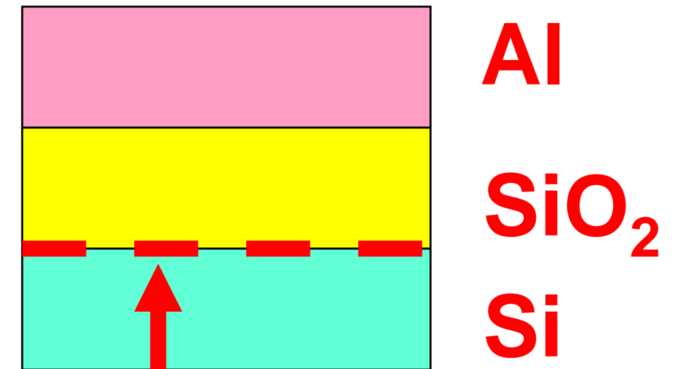
Connect 2 bipolar transistors in the
Same substrate by bonding wire.



1960: First MOSFET
by D. Kahng and M. Atalla

Top View

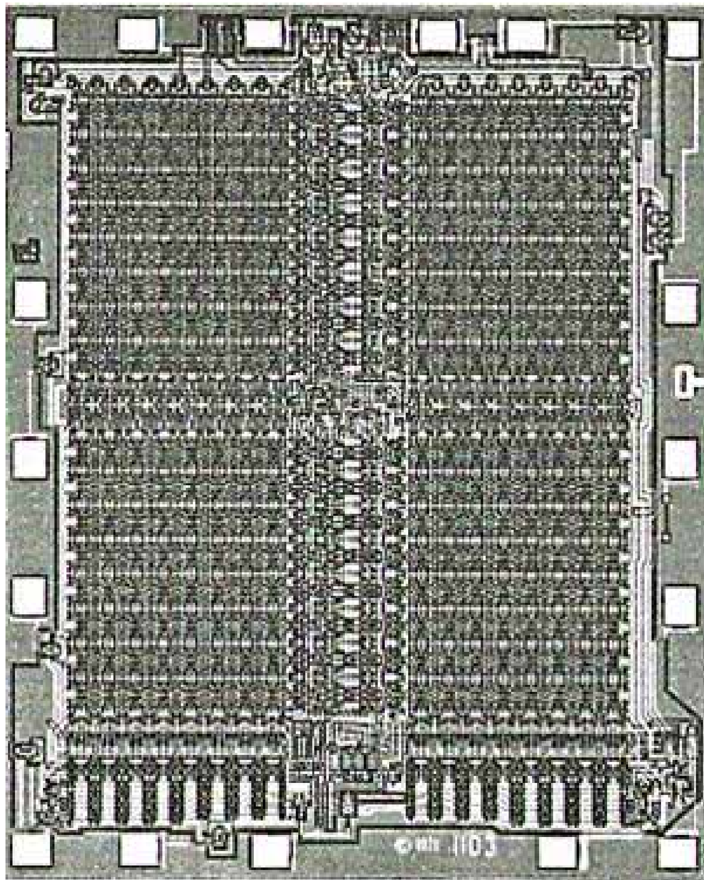




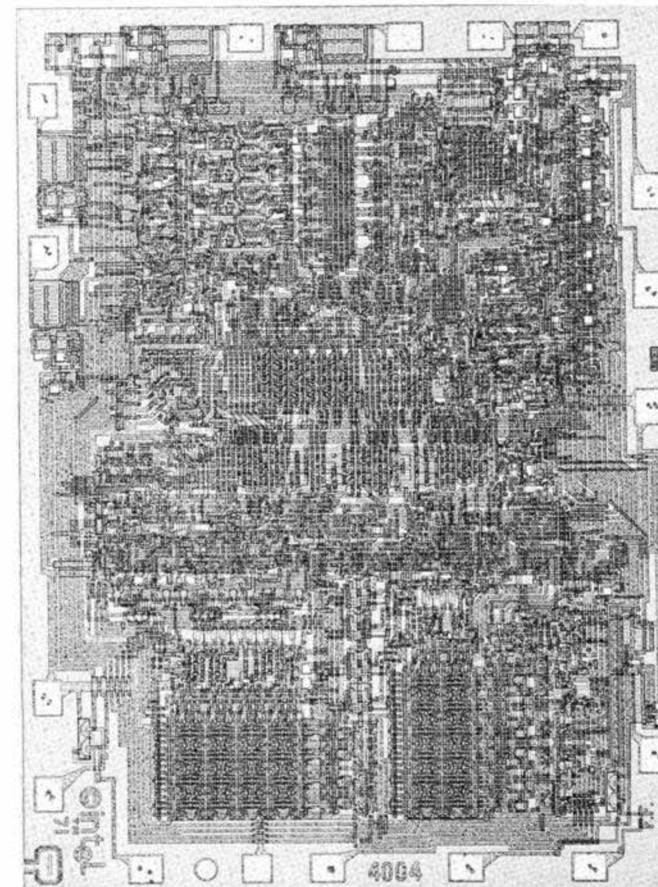
Si/SiO2 Interface is extraordinarily good

1970,71: 1st generation of LSIs

DRAM Intel 1103



MPU Intel 4004



MOS LSI experienced continuous progress for many years

	Name of Integrated Circuits	Number of Transistors
1960s	IC (Integrated Circuits)	~ 10
1970s	LSI (Large Scale Integrated Circuit)	~1,000
1980s	VLSI (Very Large Scale IC)	~10,000
1990s	ULSI (Ultra Large Scale IC)	~1,000,000
2000s	?LSI (? Large Scale IC)	~1000,000,000

Most recent SD Card

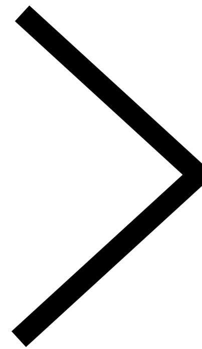
Most Recent SD Card

128GB = 128G Bite
= 128G X 8bit = 1024Gbit
= 1.024T(Tera)bit

1T = 10^{12} = 1Trillion

World Population：6 Billion
Brain Cell：10～100 Billion
Stars in Galaxy：100 Billion

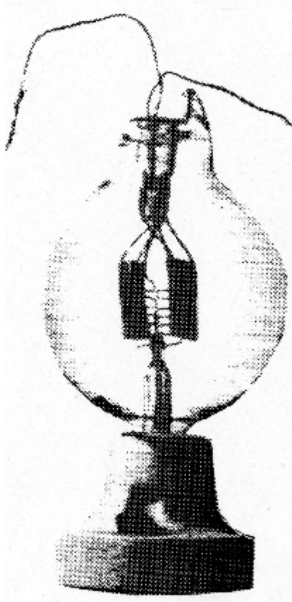
Most Recent SD Card



2.4cm X 3.2cm X 0.21cm

Volume：1. 6cm³ Weight：2g

Voltage：2.7 - 3.6V



Old Vacuum Tube：
5cm X 5cm X 10cm, 100g,100W

1Tbit = 10k X10k X 10k bit

Volume = 0.5km X 0.5km X 1km
= 0.25 km^3 = $0.25X10^{12}cm^3$

Weight = 0.1 $kgX10^{12}$ = $0.1X10^9$ton = 100 M ton

Power = $0.1kWX10^{12}$=50 TW

Supply Capability of Tokyo Electric Power Company: 55 BW

Gate Electrode
Poly Si

Gate Insulator
SiO_2

Substrate
Si

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Use Gate Field Effect for switching

Gate Electrode
Poly Si

Gate Insulator
SiO_2

Source

n-Si

n-Si

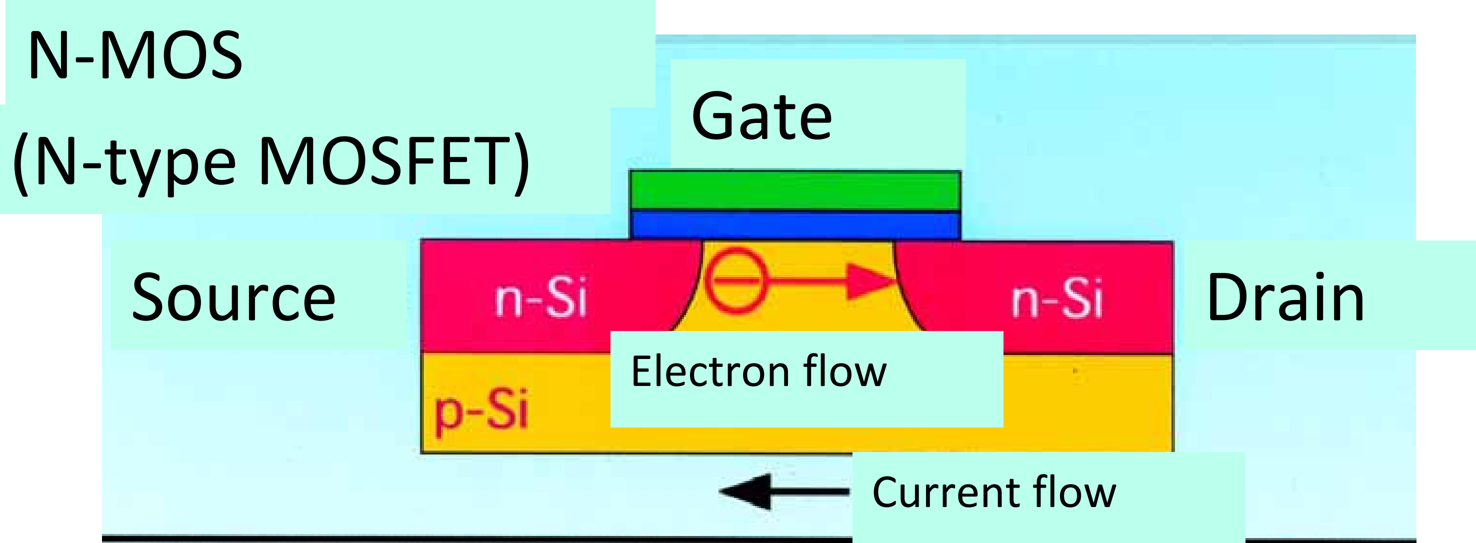
Drain

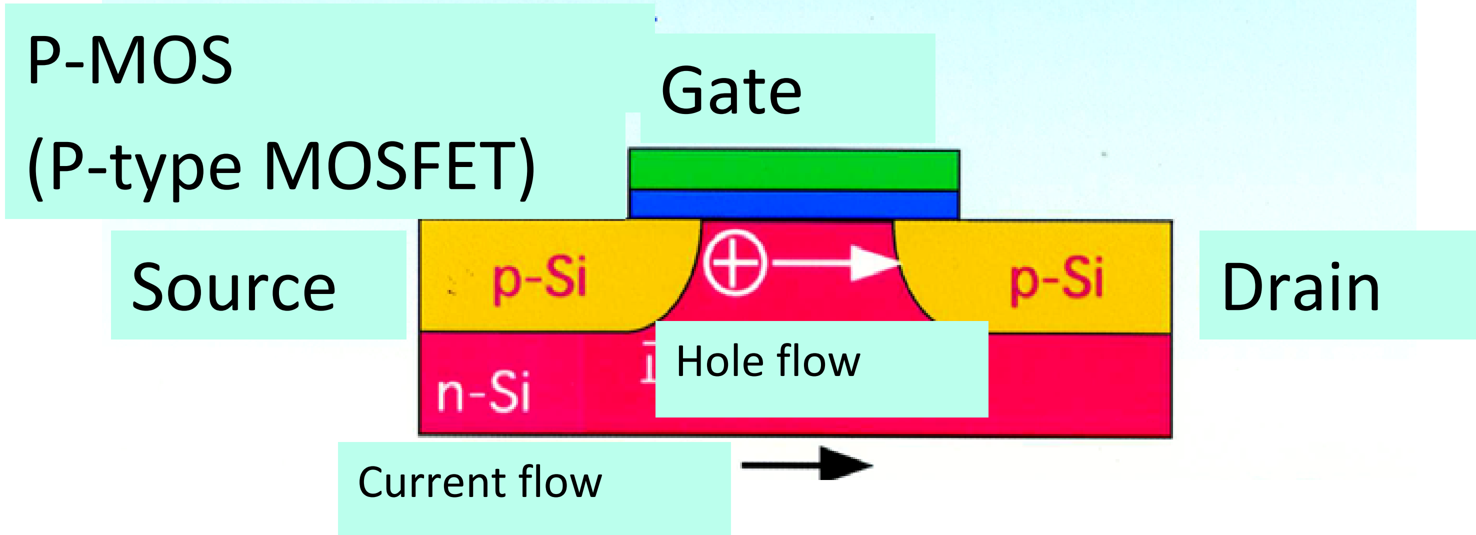
p-Si

Si
Substrate

Channel

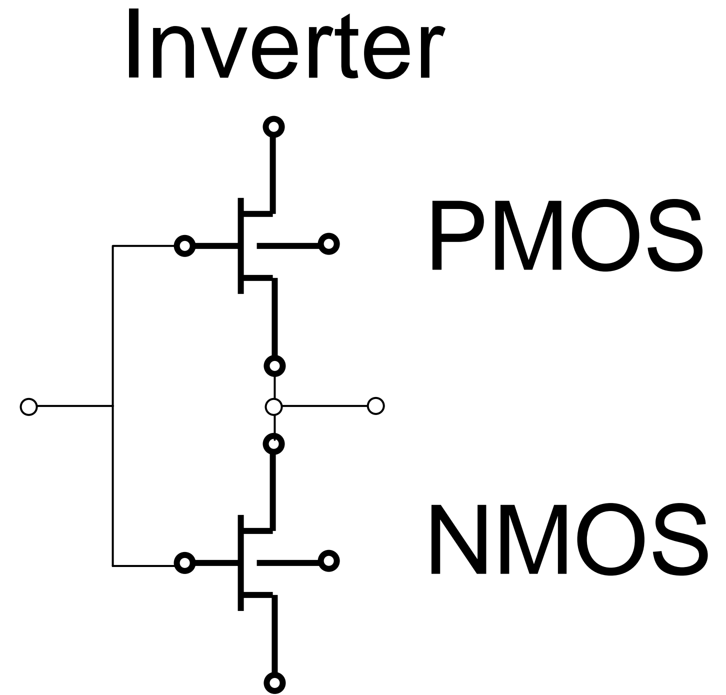
N-MOS (N-type MOSFET)


N-MOS
(N-type MOSFET)
Gate
Source
n-Si
n-Si
Drain
Electron flow
p-Si
Current flow


P-MOS
(P-type MOSFET)
Gate
Source
p-Si
p-Si
Drain
Hole flow
n-Si
Current flow

CMOS

Complimentary MOS



When NMOS is ON, PMOS is OFF

When PMOS is ON, NMOS is OFF

Needless to say, but….

CMOS Technology:

Indispensible for our human society

All the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:

There is no computer in banks, and

world economical activities immediately stop.

Cellarer phone dose not exists

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

→ **Increase clock frequency**

→ **Increase circuit operation speed**

2. **Increase number of Transistors**

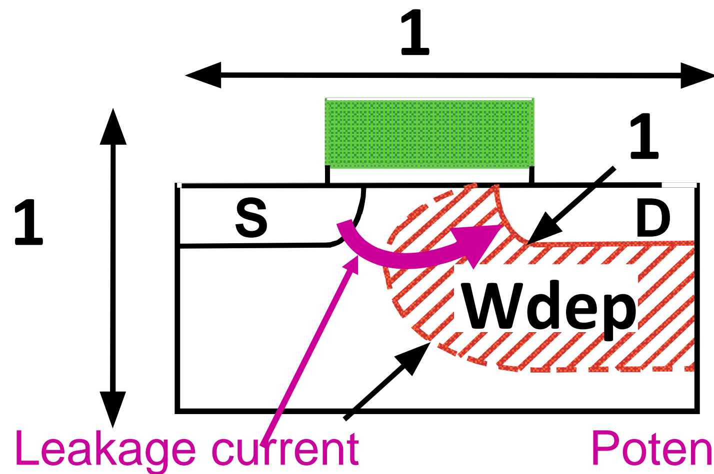
→ **Parallel processing**

→ **Increase circuit operation speed**

Downsizing contribute to the performance increase in double ways

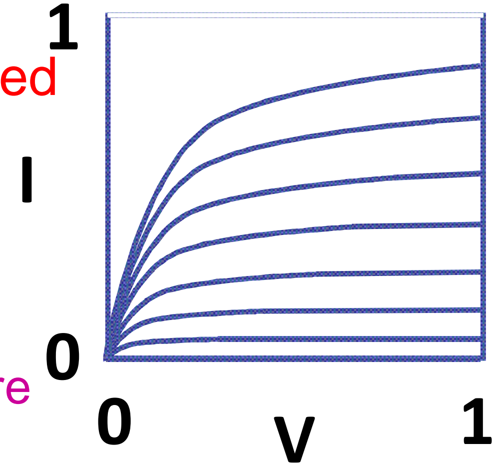
Thus, downsizing of Si devices is the most important and critical issue.

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

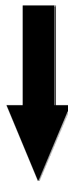
Wdep has to be suppressed
Otherwise, large leakage between S and D



Leakage current

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

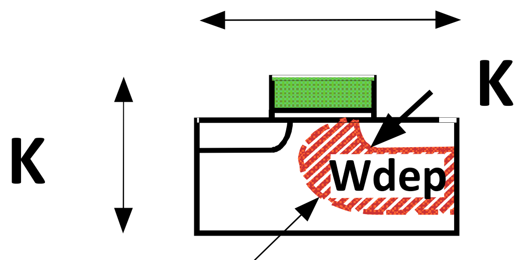
K=0.7 for example



X , Y , Z : K, V : K, Na : 1/K

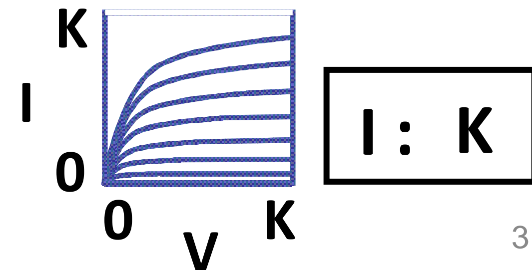
By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$\text{Wdep} \propto \sqrt{V/Na}$$

$: \quad K$



I : K

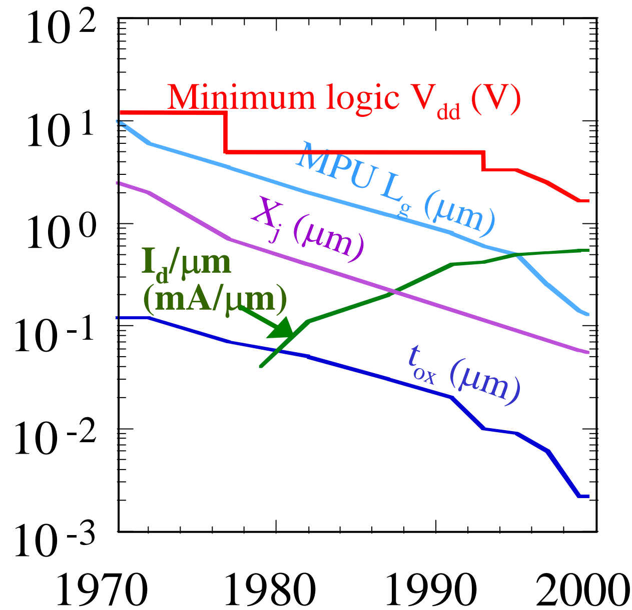
Downscaling merit: Beautiful!

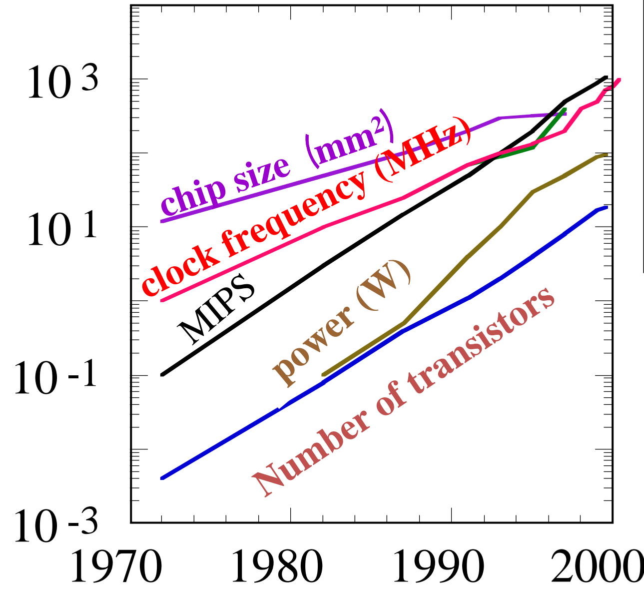
Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	**Scaling K : K=0.7 for example**
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o: gate C per unit area $\rightarrow W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox}$ $\rightarrow$ $KK/K = K$
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d$ $\rightarrow$ $KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α: Scaling factor $\rightarrow$ **In the past, $\alpha > 1$ for most cases**
Integration (# of Tr)	N	α/K^2	N $\rightarrow$ α/K^2 **$= 1/K^2$, when $\alpha = 1$**
Power per chip	P	α	$fNCV^2/2$ $\rightarrow$ $K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha$ **$= 1$, when $\alpha = 1$**

k= 0.7 and α =1	k= 0.7^2 =0.5 and α =1
Single MOFET Vdd → 0.7 Lg → 0.7 Id → 0.7 Cg → 0.7 P (Power)/Clock → $0.7^3 = 0.34$ τ (Switching time) → 0.7	Vdd → 0.5 Lg → 0.5 Id → 0.5 Cg → 0.5 P (Power)/Clock → $0.5^3 = 0.125$ τ (Switching time) → 0.5
Chip N (# of Tr) → $1/0.7^2 = 2$ f (Clock) → 1/0.7 = 1.4 P (Power) → 1	N (# of Tr) → $1/0.5^2 = 4$ f (Clock) → 1/0.5 = 2 P (Power) → 1

33

Actual past downscaling trend until year 2000





Past 30 years scaling

Merit: N, f increase

Demerit: P increase

V_{dd} scaling insufficient

⇓

Additional significant increase in I_d, f, P

Source. Iwai and S. Ohmi, Microelectronics Reliability 42 (2002), pp.1251-1268

Change in 30 years

	Ideal scaling	Real Change		Ideal scaling	Real Change		Ideal scaling	Real Change
L_g	K	10^{-2}	I_d	K (10^{-2})	10^{-1}	f	1/K(10^{2})	10^3
t_{ox}	K(10^{-2})	10^{-2}	I_d/μm	1	10^1	P = fαNCV²	α(10^{1})	10^5
V_{dd}	K(10^{-2})	10^{-1}	N	α/K²(10^{5})	10^4			
A_{chip}	α	10^1						

Vd scaling insufficient, α increased → N, Id, f, P increased significantly

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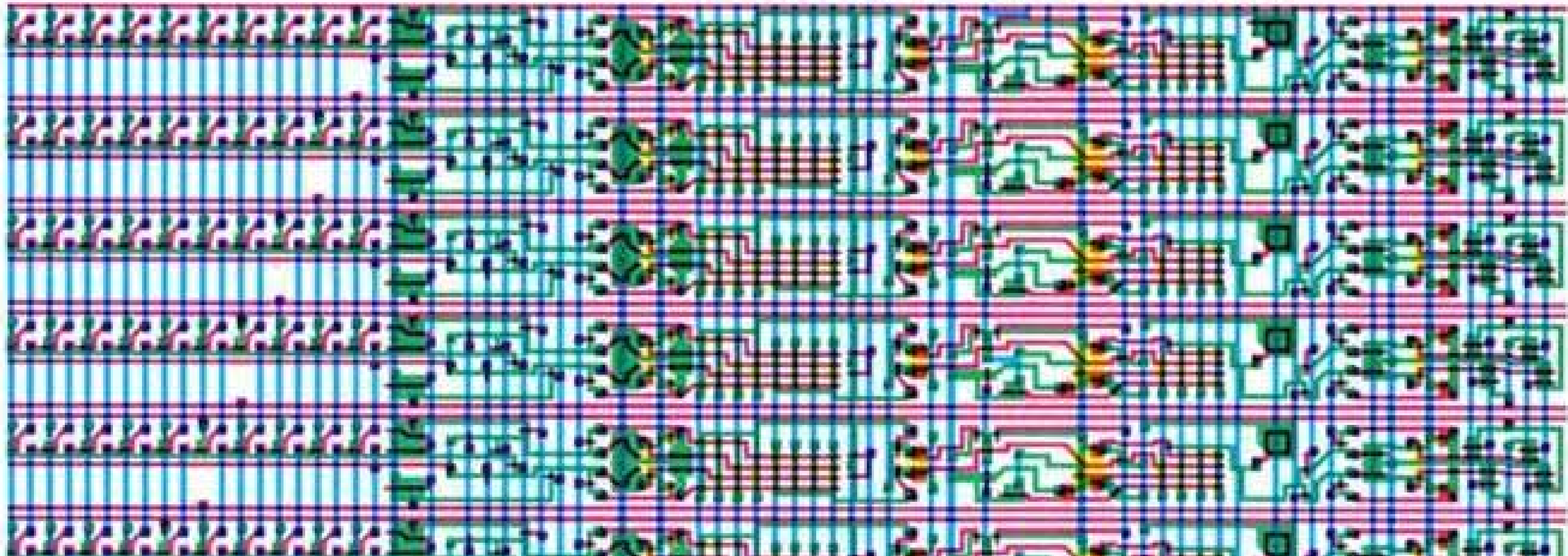
Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.

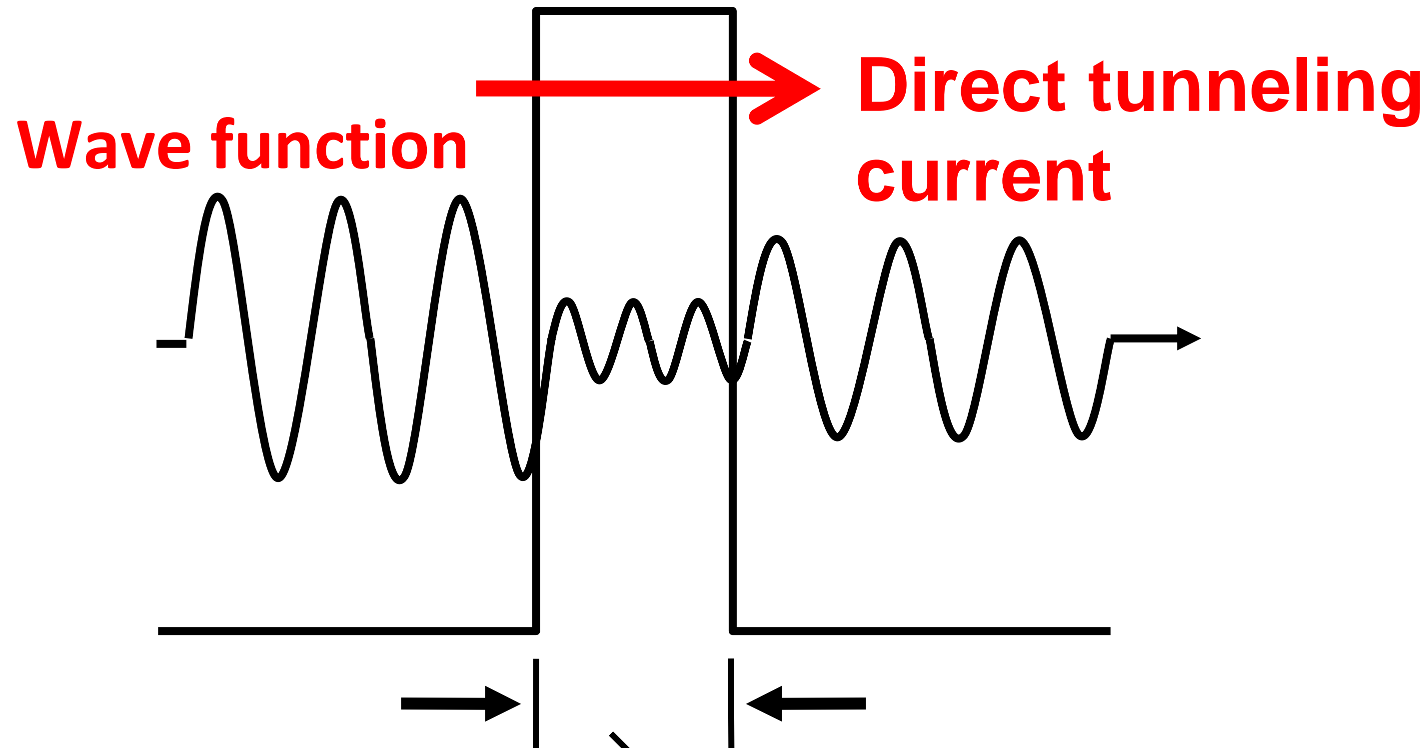


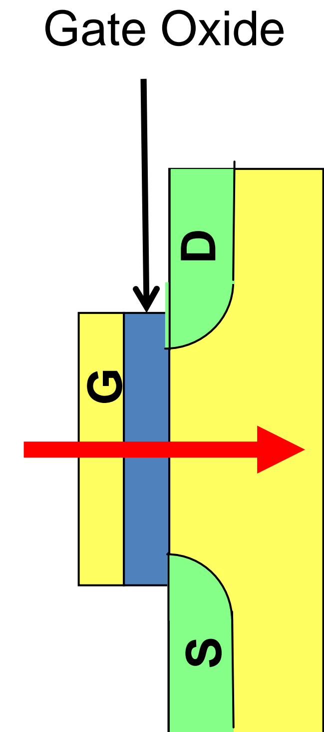
C. Mead L. Conway

VLSI textbook

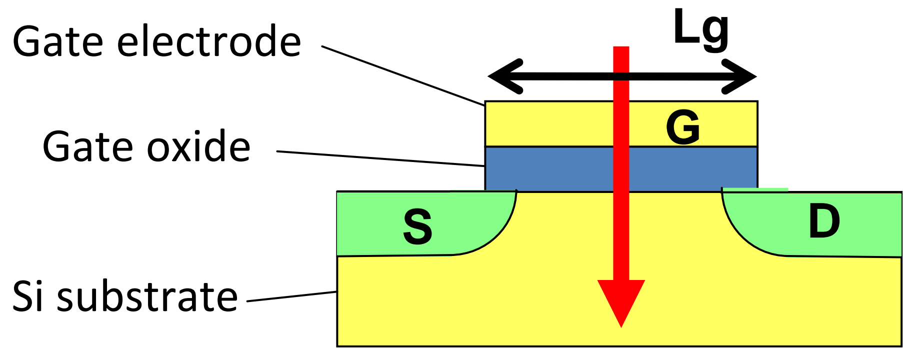
Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.

Direct-tunneling effect





Direct tunneling leakage current start to flow when the thickness is 3 nm.



Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide

Lg = 10 μm

Vg = 2.0V
1.5 V
1.0 V
0.5 V
0.0 V

Id (mA / μm)

0.03
0.02
0.01
0.00
0.01
-0.4

0.0 0.5 1.0 1.5

Vd (V)

Lg = 5 μm

Vg = 2.0V
1.5 V
1.0 V
0.5 V
0.0 V

0.08
0.06
0.04
0.02
0.00
-0.02

0.0 0.5 1.0 1.5

Vd (V)

Lg = 1.0 μm

Vg = 2.0V
1.5 V
1.0 V
0.5 V
0.0 V

0.4
0.3
0.2
0.1
0.0
-0.1

0.0 0.5 1.0 1.5

Vd (V)

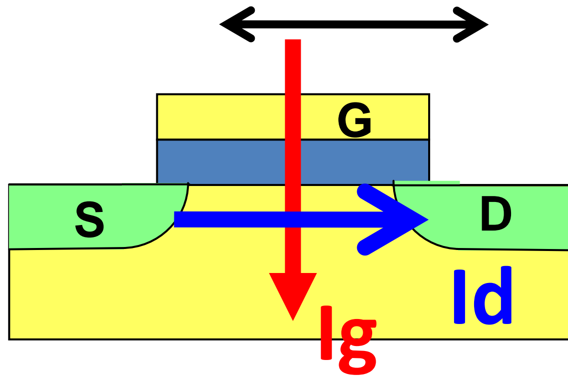
Lg = 0.1μm

Vg = 2.0V
1.5 V
1.0 V
0.5 V
0.0 V

1.6
1.2
0.8
0.4
0.0
-0.4

0.0 0.5 1.0 1.5

Vd (V)



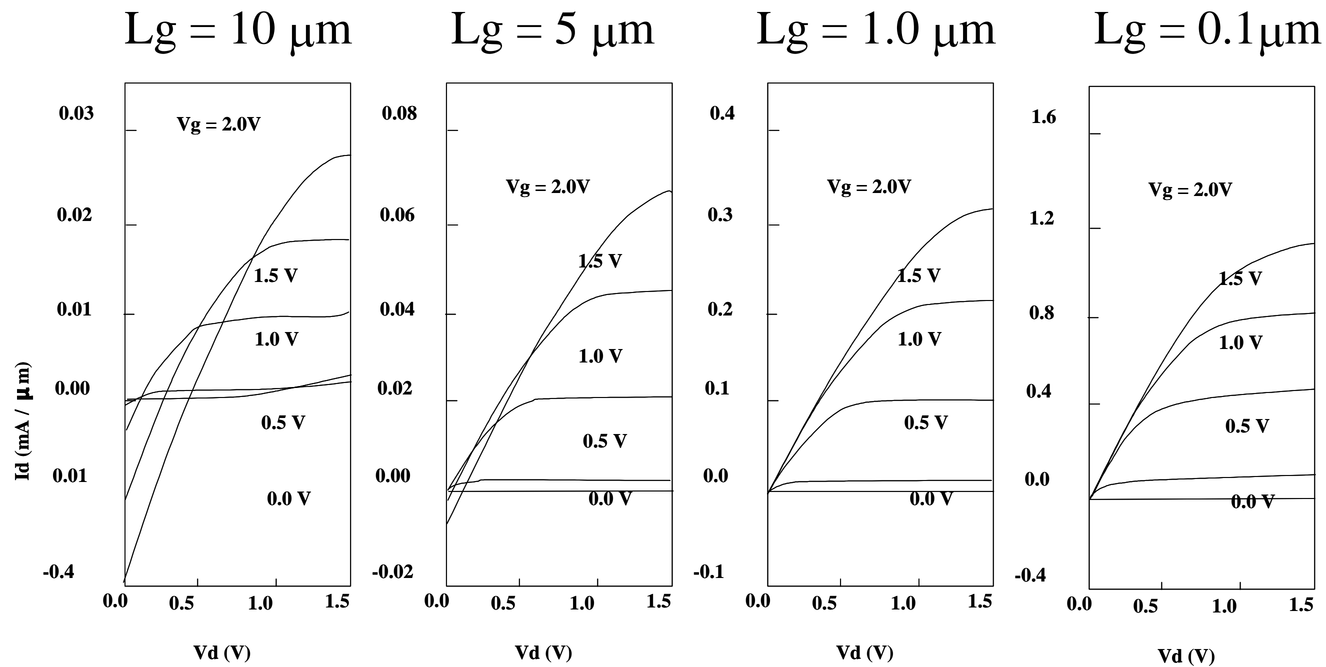
Gate leakage: Ig ∝ Gate Area ∝ Gate length (Lg)

Drain current: Id ∝ 1/Gate length (Lg)

Lg → small,

Then, Ig → small, Id → large, Thus, Ig/Id → very small

Id



Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

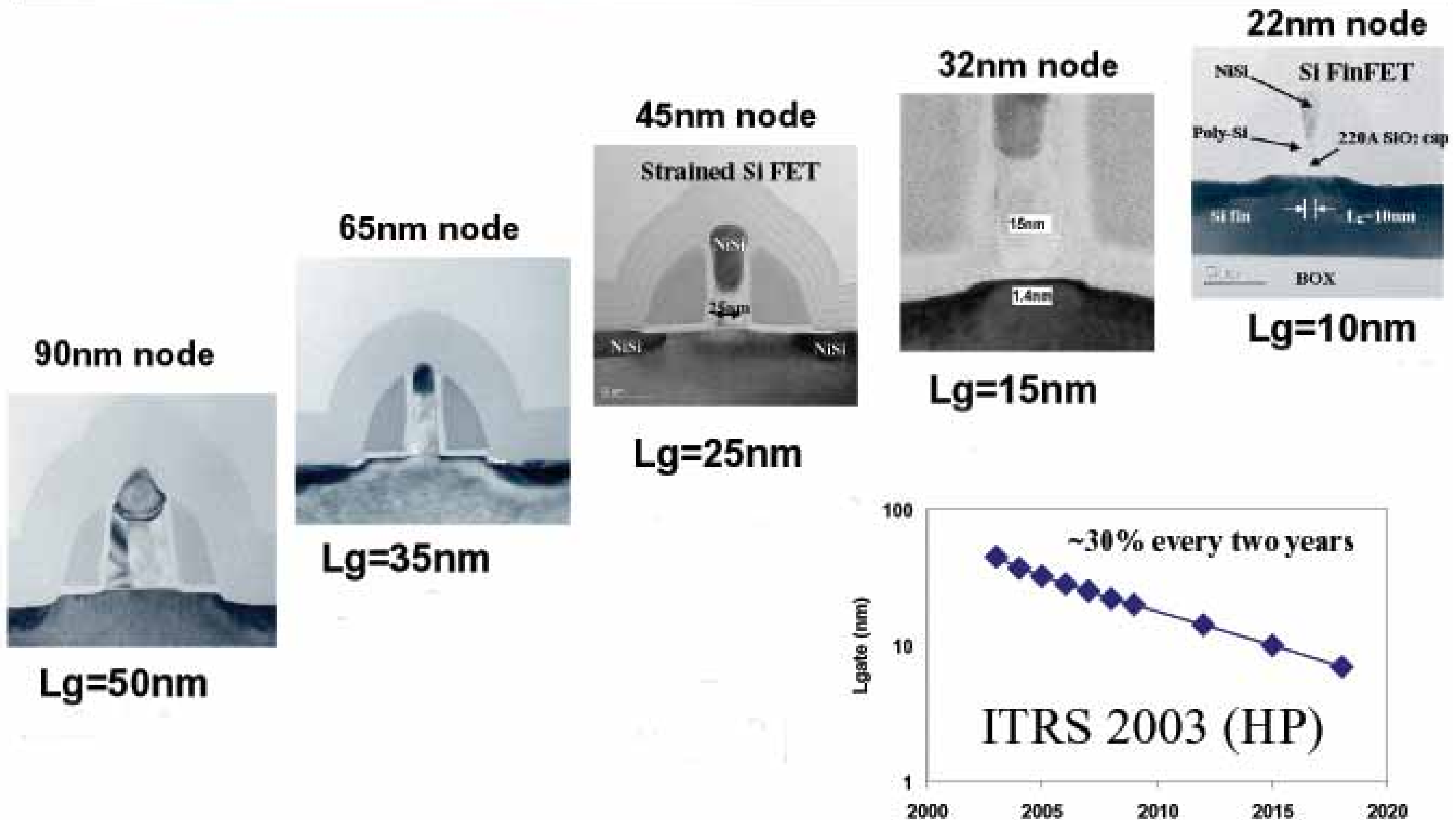
There would be a solution!

Think, Think, and Think!

Or, Wait the time!

Some one will think for you

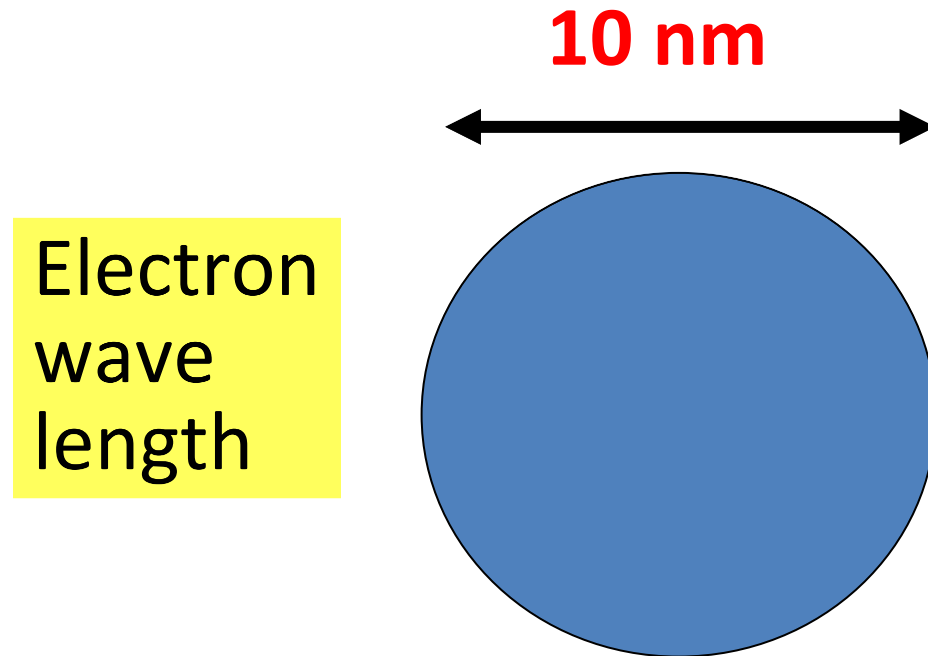
Transistor Scaling Continues

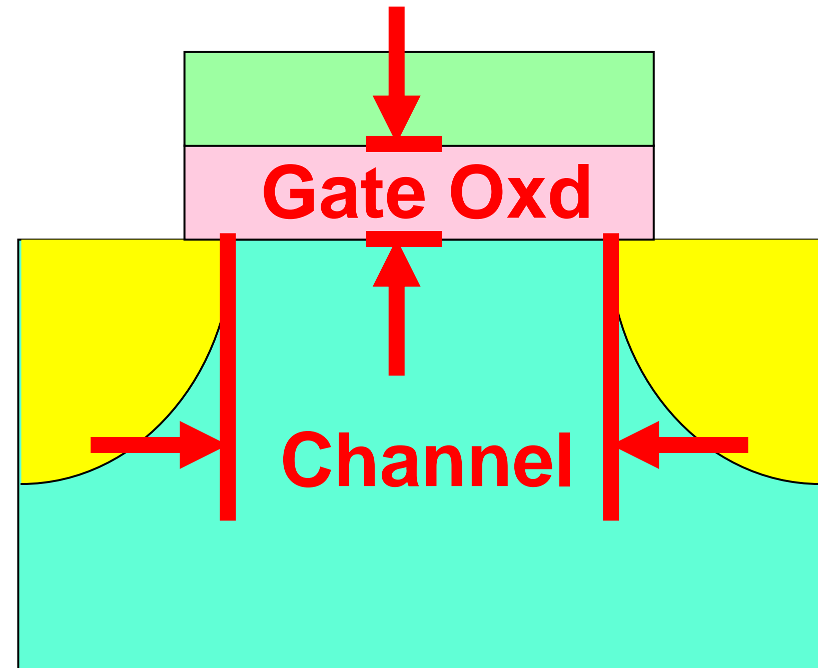


Qi Xinag, ECS 2004, AMD

Downsizing limit?

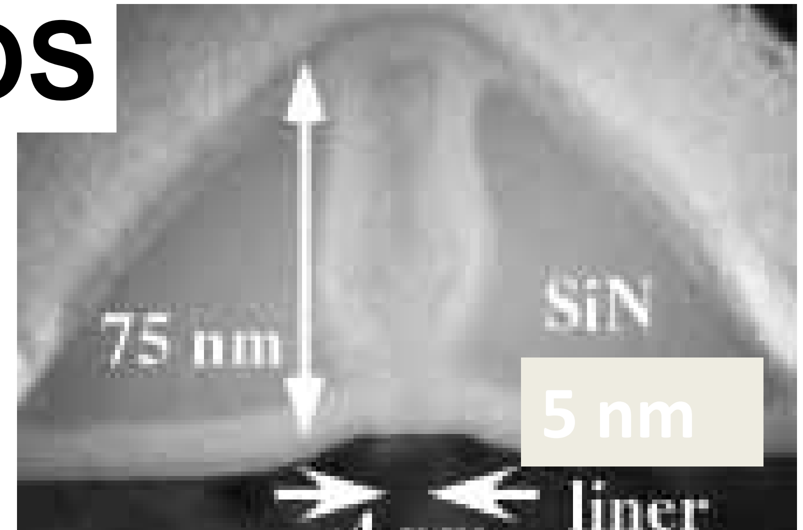
Channel length?



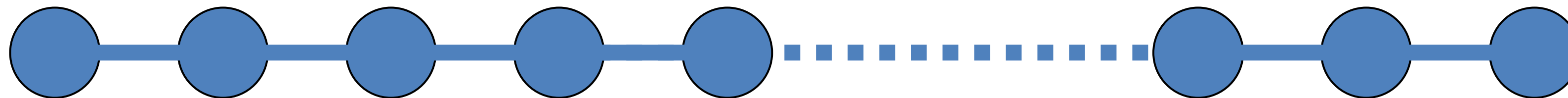


5 nm gate length CMOS

Is a Real Nano Device!!

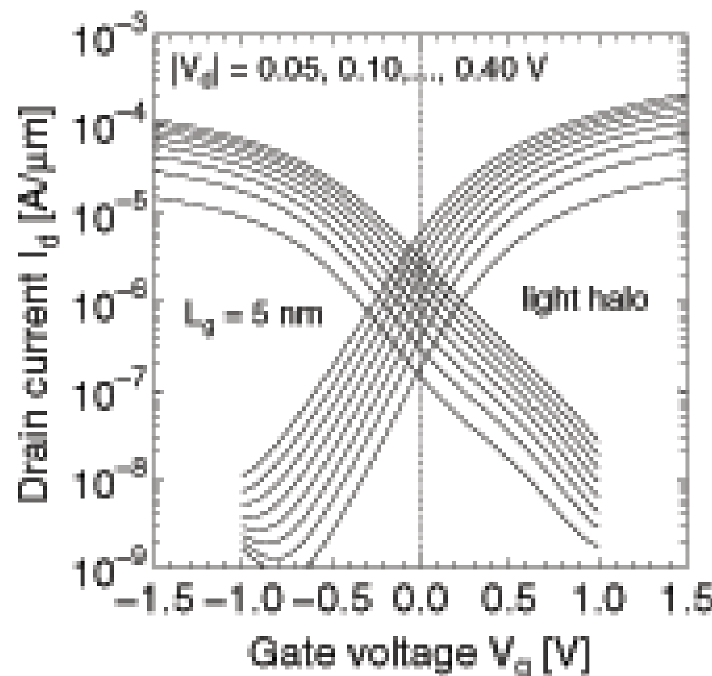


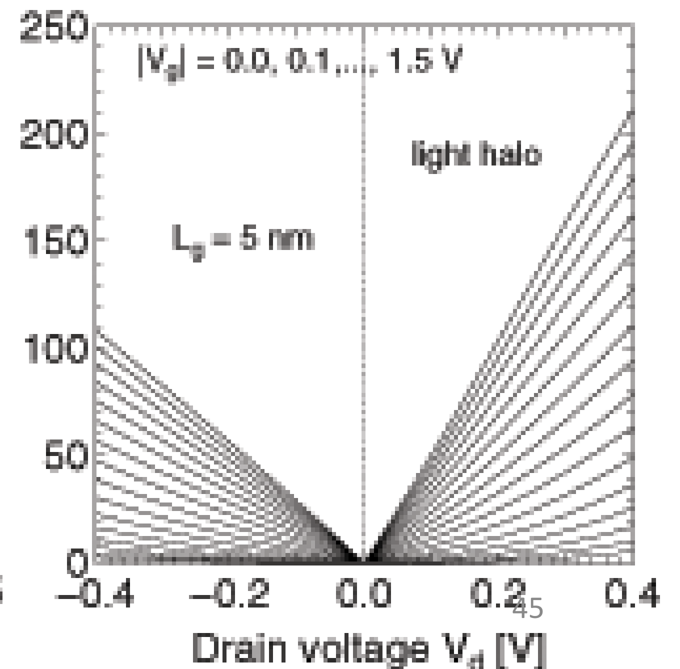
Length of 18 Si atoms



H. Wakabayashi
et.al, NEC

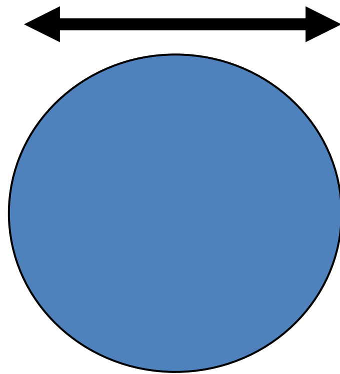
IEDM, 2003





Electron wave length

10 nm



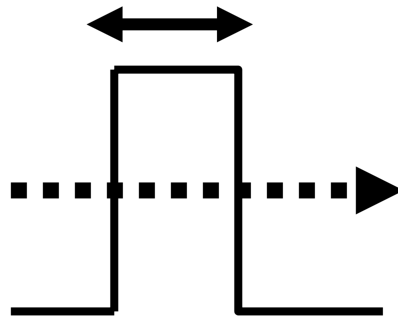
Downsizing limit!

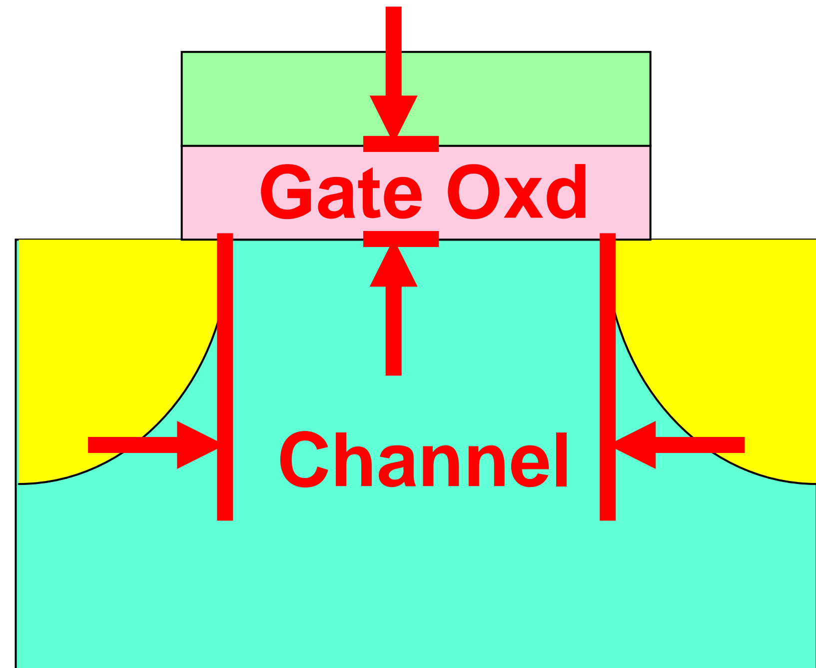
Channel length

Gate oxide thickness

Tunneling distance

3 nm

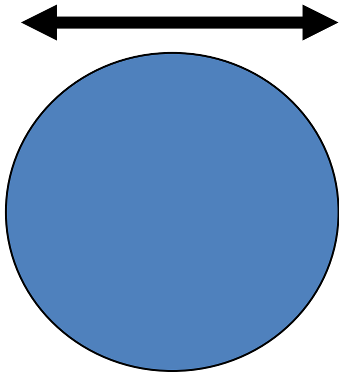




Prediction now!

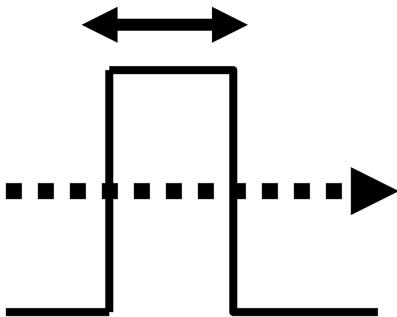
Electron wave length

10 nm



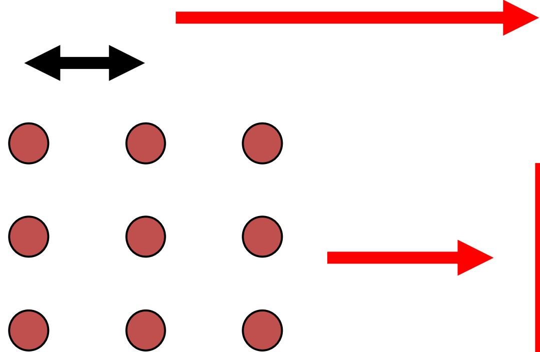
Tunneling distance

3 nm



Atom distance

0.3 nm

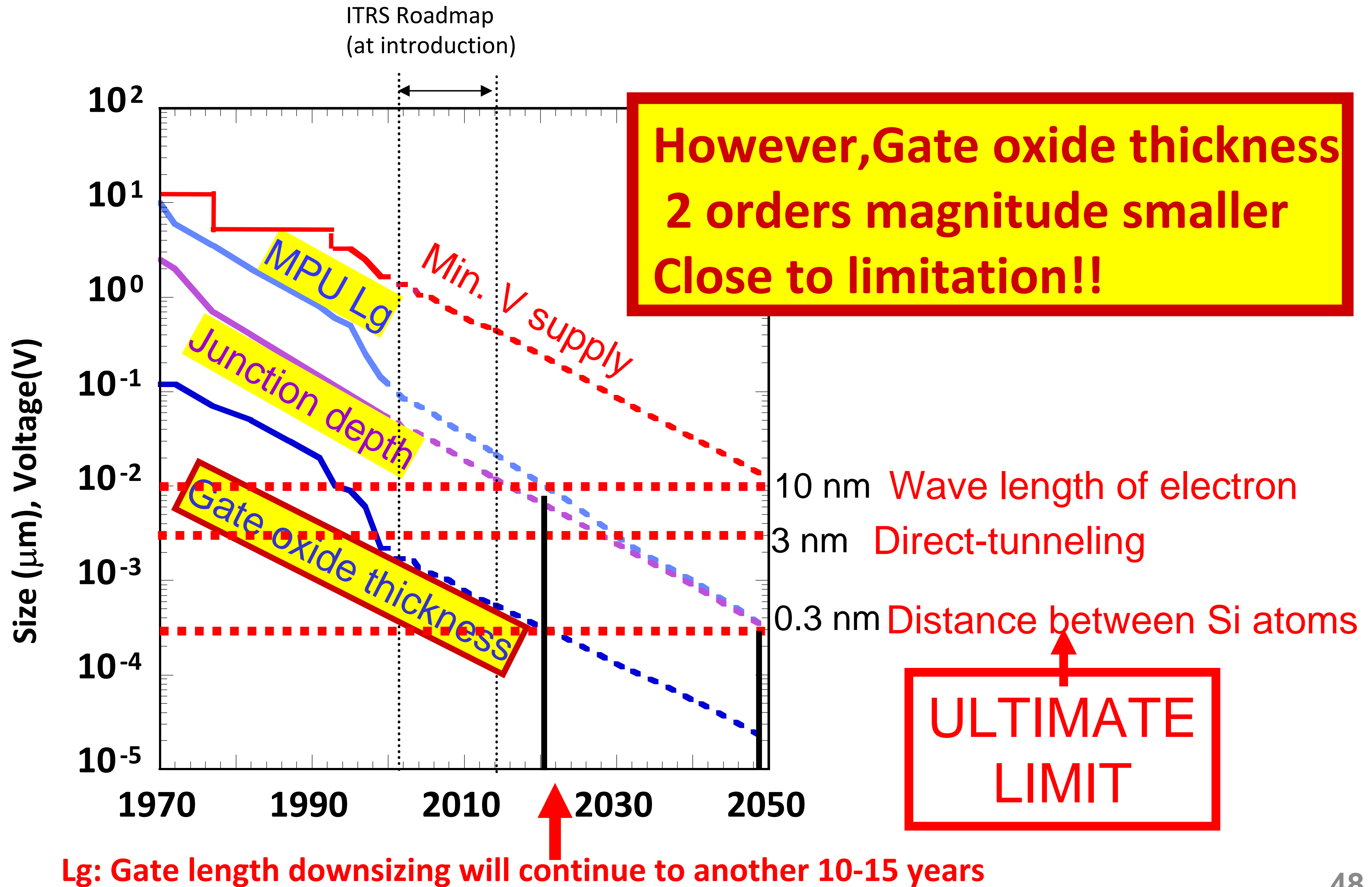


MOSFET operation

Lg = 2 ~ 1.5 nm?

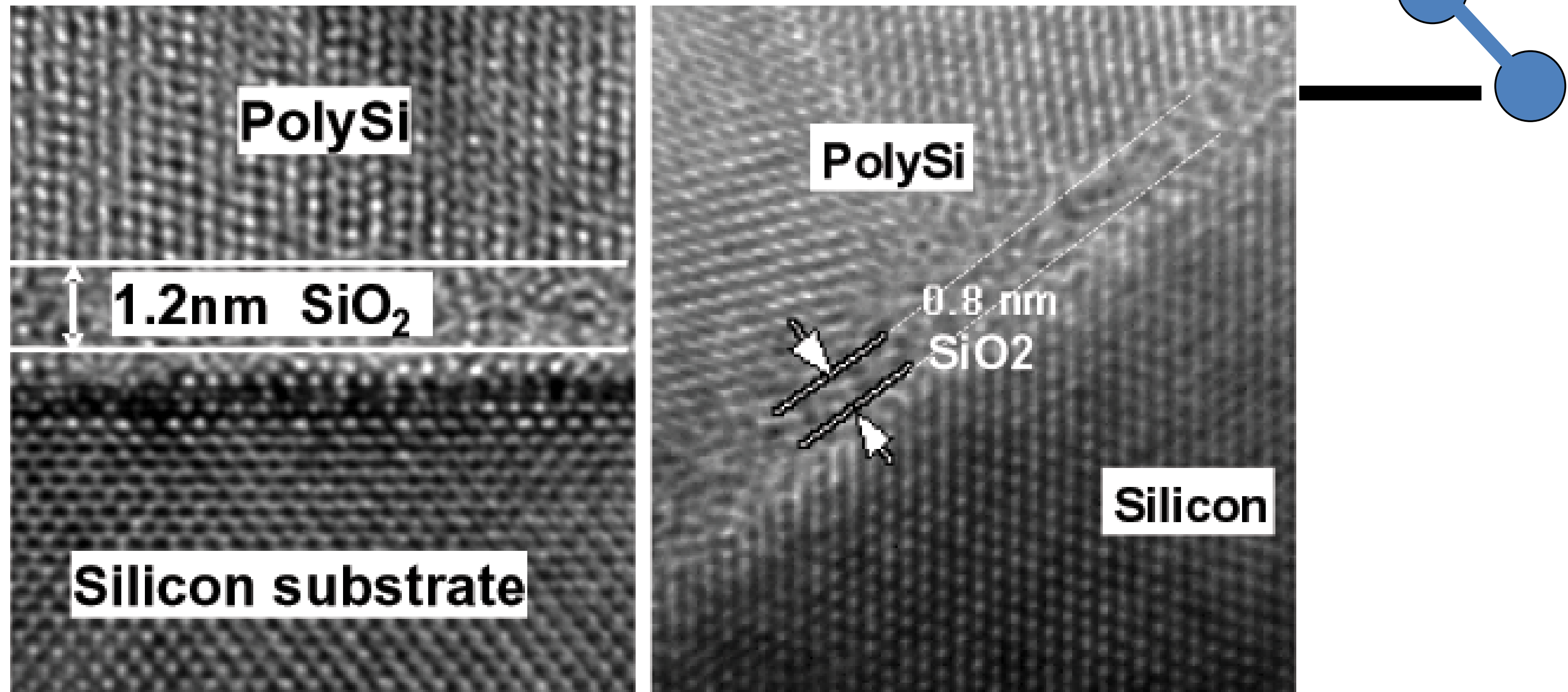
Below this, no one knows future!

Ultimate limitation



0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!



- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003

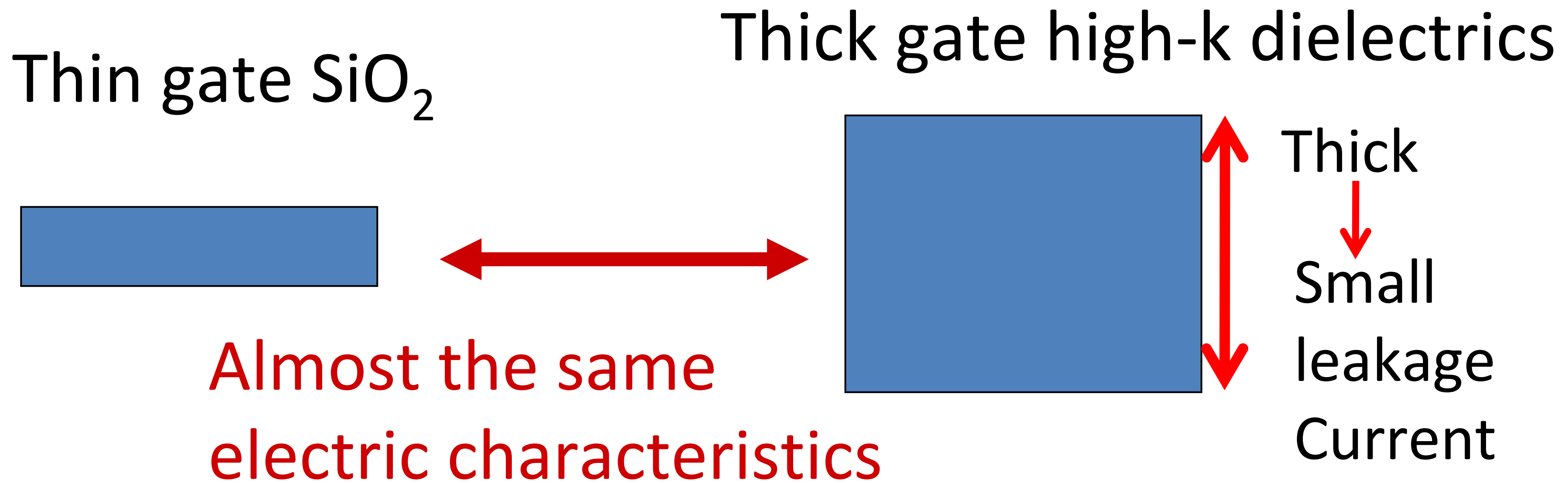
So, we are now in the limitation of downsizing?

Do you believe this or do not?

There is a solution!

K: Dielectric Constant

To use high-k dielectrics



However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO_2!

Choice of High-k elements for oxide

Candidates (cyan)

● Gas or liquid at 1000 K

○ Radio active

Unstable at Si interface

① $Si + MO_X \quad M + SiO_2$

② $Si + MO_X \quad MSi_X + SiO_2$

③ $Si + MO_X \quad M + MSi_XO_Y$

●H ●He

Li Be ●B ●C ●N ●O ●F ●Ne

①Na Mg Al Si ●P ●S ●Cl ●Ar

K Ca Sc ②Ti ①V ①Cr ①Mn ①Fc ①Co ①Ni ①Cu ①Zn ①Ga ①Ge ●As ●Se ●Br ●Kr

●Rh Sr Y Zr ①Nb ①Mo Tc ①Ru ①Rb ①Pd ●Ag ①Cd ①In ①Sn ①Sb ①Te ●I ●Xe

●Cs ③Ba ★ Hf ①Ta ①W ①Re ①Os ①Ir ●Pt ●Au ●Hg ●Tl ①Pb ①Bi ○Po ○At ○Rn

○Fr ○Ra ☆ ○Rf ○Ha ○Sg ○Ns ○Hs ○Mt

★ La Ce Pr Nd ○Pm Sm Eu Gd Tb Dy Ho Er Tm Yb Lu

☆ ○Ac ○Th ○Pa ○U ○Np ○Pu ○Am ○Cm ○Bk ○Cf ○Es ○Fm ○Md ○No ○Lr

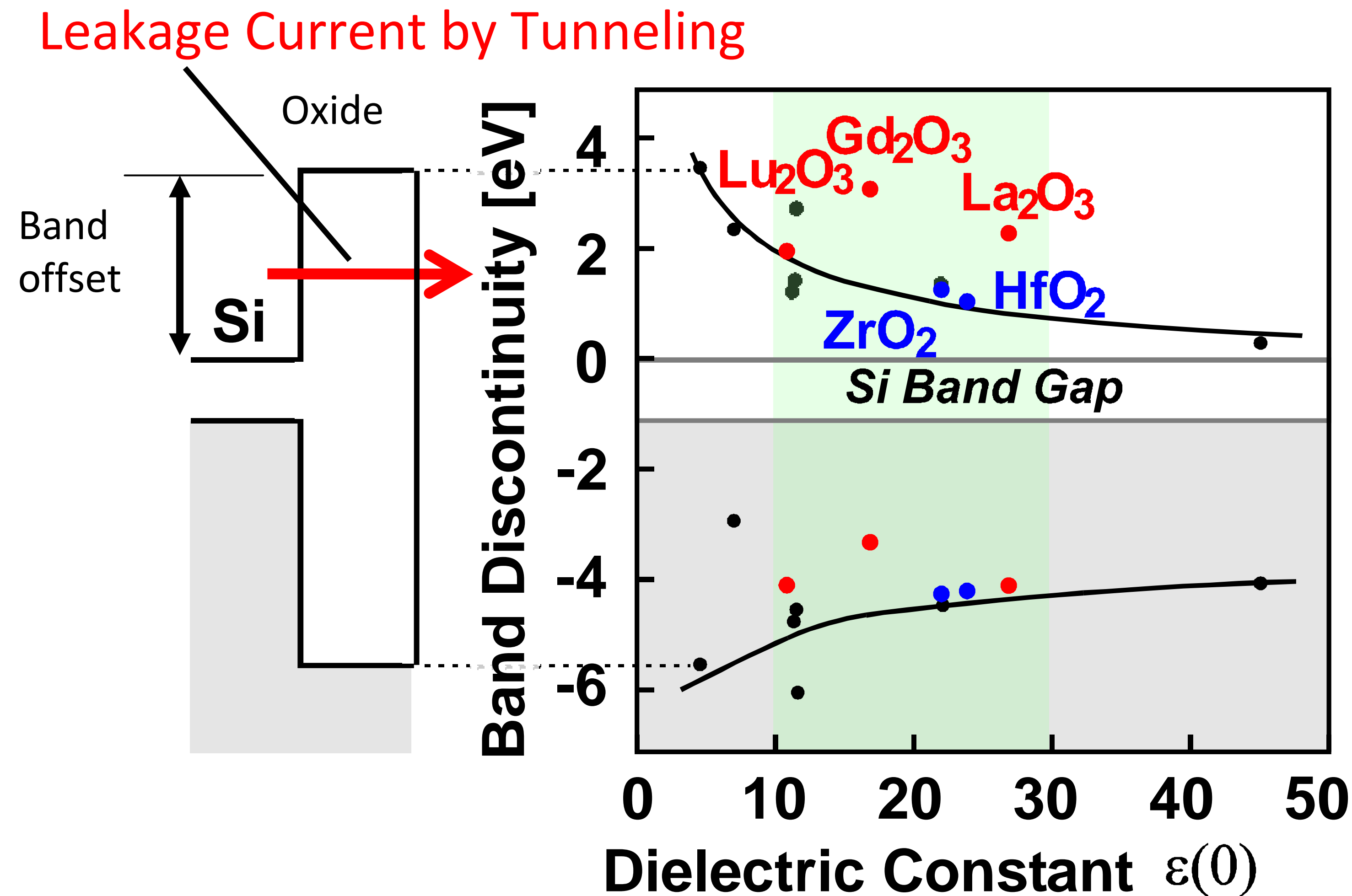
HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999

Hubbard and Schlom, J Mater Res 11 2757 (1996)

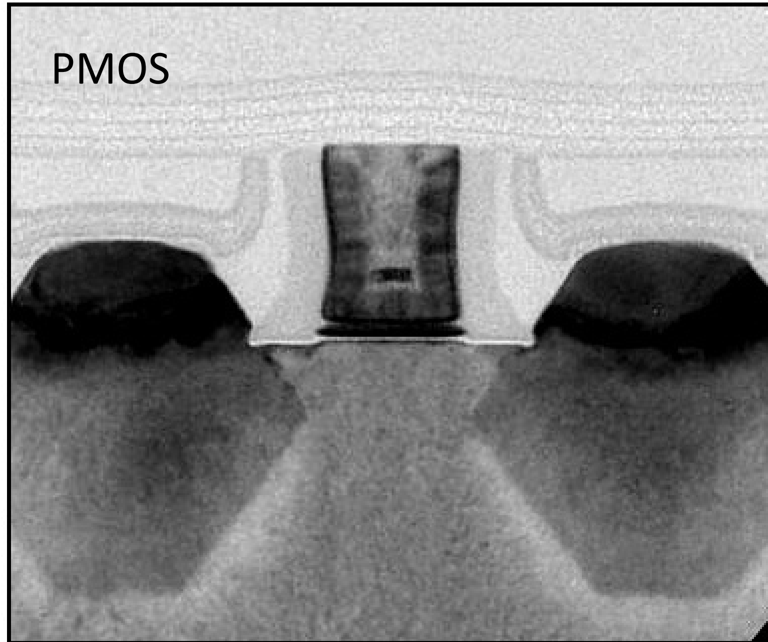
Conduction band offset vs. Dielectric Constant

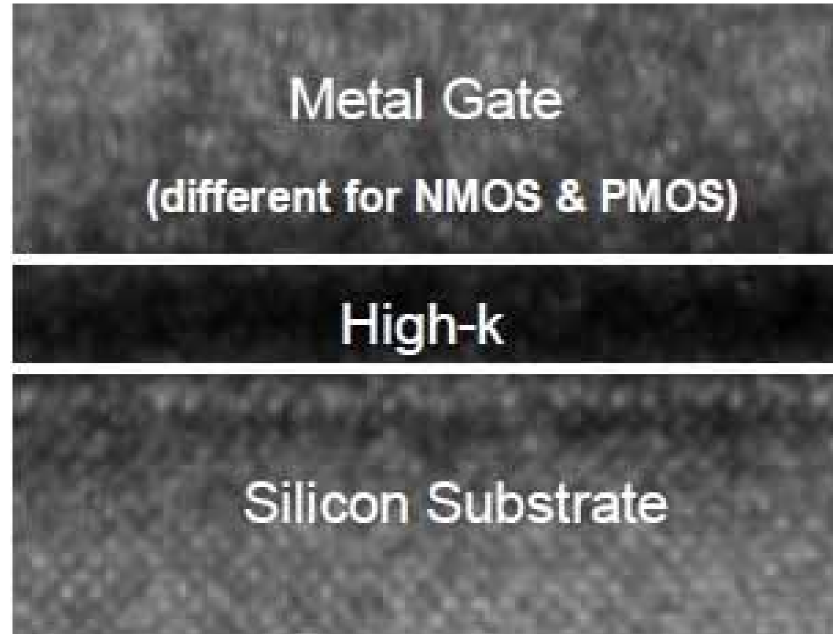


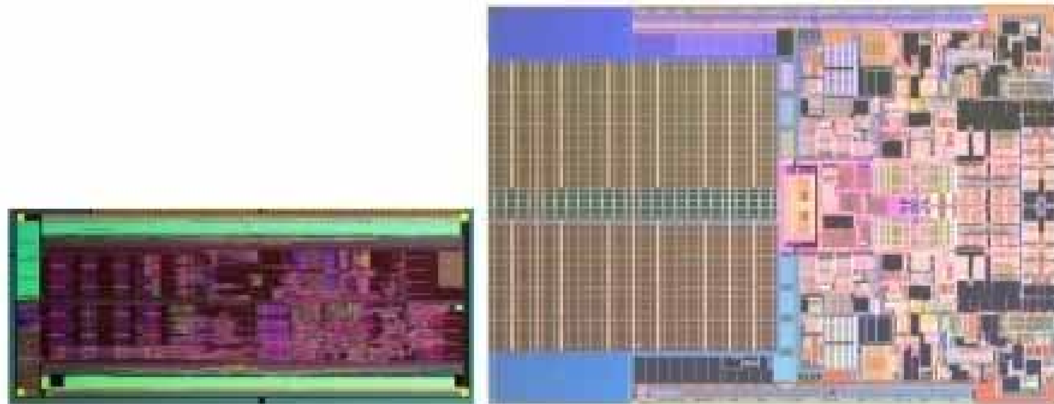
XPS measurement by Prof. T. Hattori, INFOS 2003

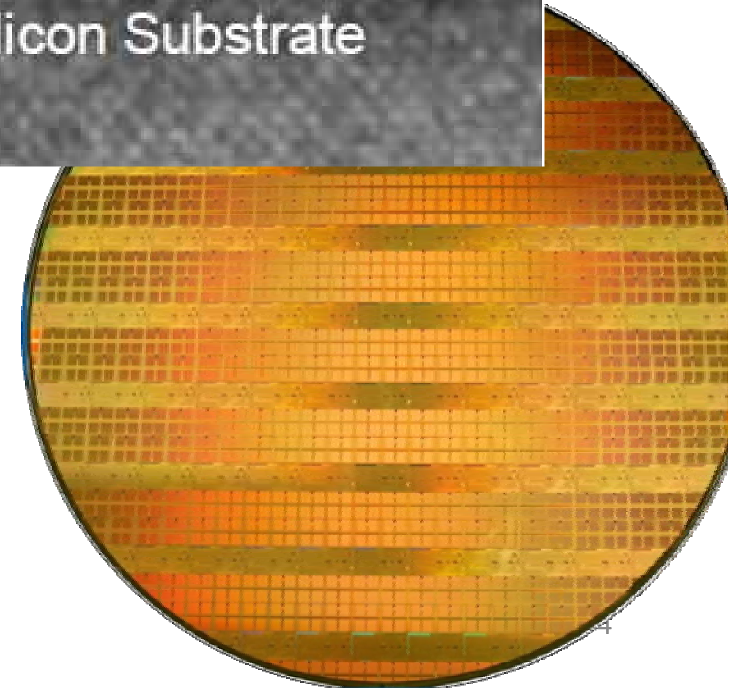
High-k gate insulator MOSFETs for Intel: EOT=1nm

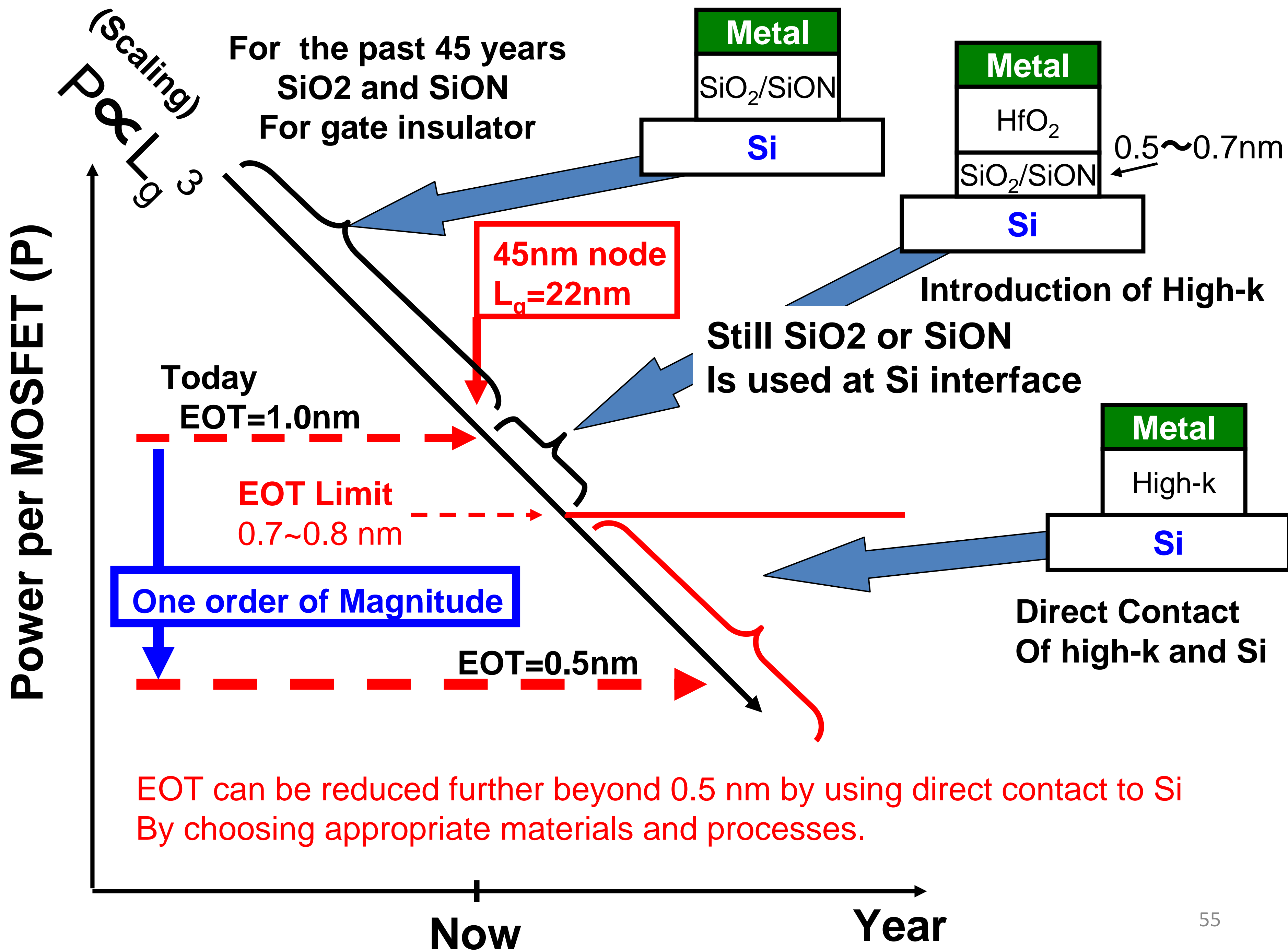
EOT: Equivalent Oxide Thickness





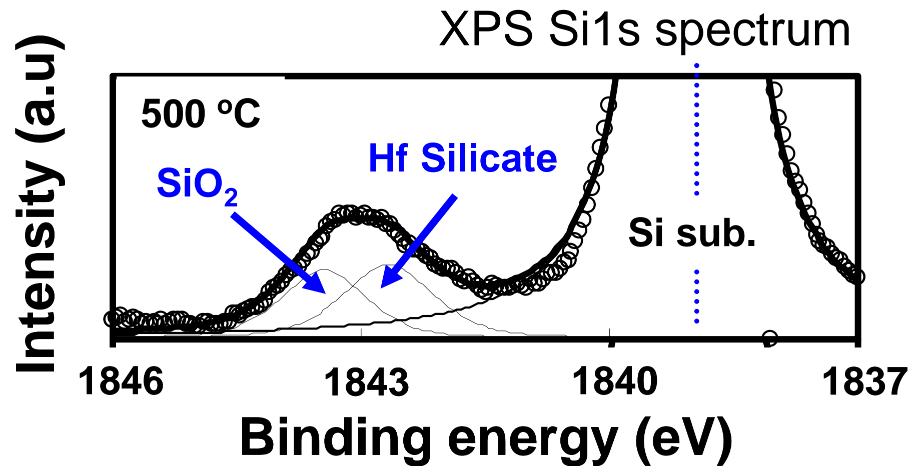




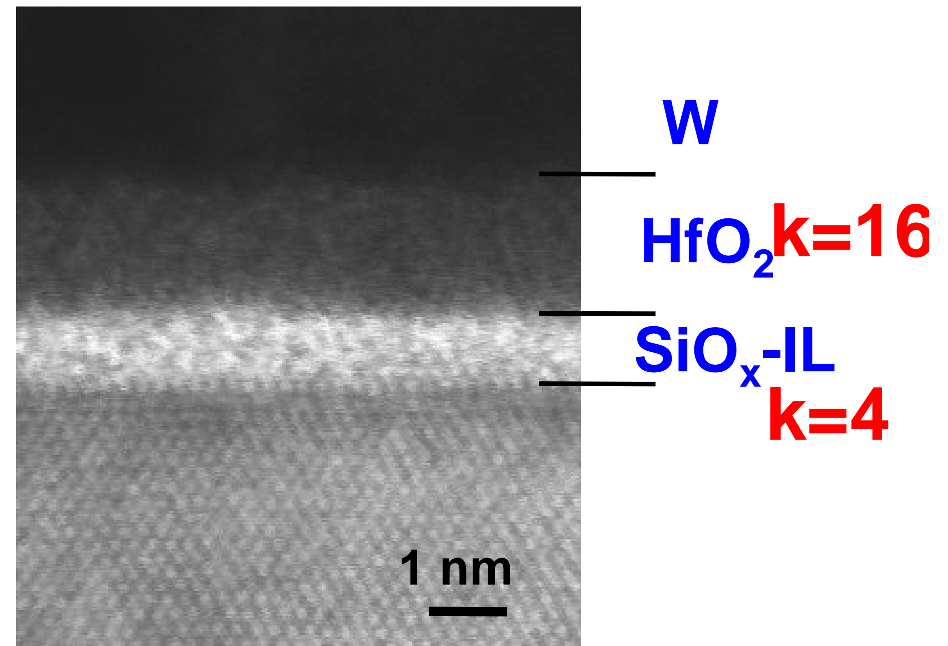

(Scaling)
P ∝ Lg3
For the past 45 years
SiO2 and SiON
For gate insulator
Metal
SiO2/SiON
Si
Metal
HfO2
0.5〜0.7nm
SiO2/SiON
Si
Introduction of High-k
45nm node
Lg=22nm
Still SiO2 or SiON
Is used at Si interface
Today
EOT=1.0nm
Metal
High-k
Si
EOT Limit
0.7~0.8 nm
One order of Magnitude
Direct Contact
Of high-k and Si
EOT=0.5nm
EOT can be reduced further beyond 0.5 nm by using direct contact to Si
By choosing appropriate materials and processes.
Power per MOSFET (P)
Now
Year

SiO_x-IL growth at HfO_2/Si Interface

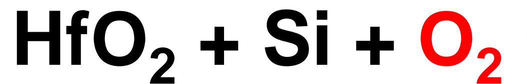
XPS Si1s spectrum

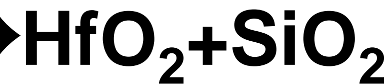


TEM image 500 °C 30min



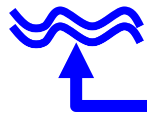
Phase separator





$$HfO_2 + Si + O_2 \rightarrow HfO_2 + Si + 2O^* \rightarrow HfO_2 + SiO_2$$

H. Shimizu, JJAP, 44, pp. 6131



Oxygen supplied from W gate electrode

D.J.Lichtenwalner, Tans. ECS 11, 319

SiO_x-IL is formed after annealing

Oxygen control is required for optimizing the reaction

Choice of High-k elements for oxide

Candidates (cyan)

● Gas or liquid at 1000 K

○ Radio active

Unstable at Si interface

① Si + MO_X M + SiO_2

② Si + MO_X MSi_X + SiO_2

③ Si + MO_X M + MSi_XO_Y

● H ● He

Li Be | ● B ● C ● N ● O ● F ● Ne

① Na Mg | Al Si ● P ● S ● Cl ● Ar

K Ca Sc ② Ti ① V ① Cr ① Mn ① Fc ① Co ① Ni ① Cu ① Zn ① Ga ① Ge ● As ● Se ● Br ● Kr

● Rh Sr Y Zr ① Nb ① Mo Tc ① Ru ① Rb ① Pd ● Ag ① Cd ① In ① Sn ① Sb ① Te ● I ● Xe

● Cs ③ Ba ★ Hf ① Ta ① W ① Re ① Os ① Ir ● Pt ● Au ● Hg ● Tl ① Pb ① Bi ○ Po ○ At ○ Rn

○ Fr ○ Ra ☆ ○ Rf ○ Ha ○ Sg ○ Ns ○ Hs ○ Mt

★ La Ce Pr Nd ○ Pm Sm Eu Gd Tb Dy Ho Er Tm Yb Lu

☆ ○ Ac ○ Th ○ Pa ○ U ○ Np ○ Pu ○ Am ○ Cm ○ Bk ○ Cf ○ Es ○ Fm ○ Md ○ No ○ Lr

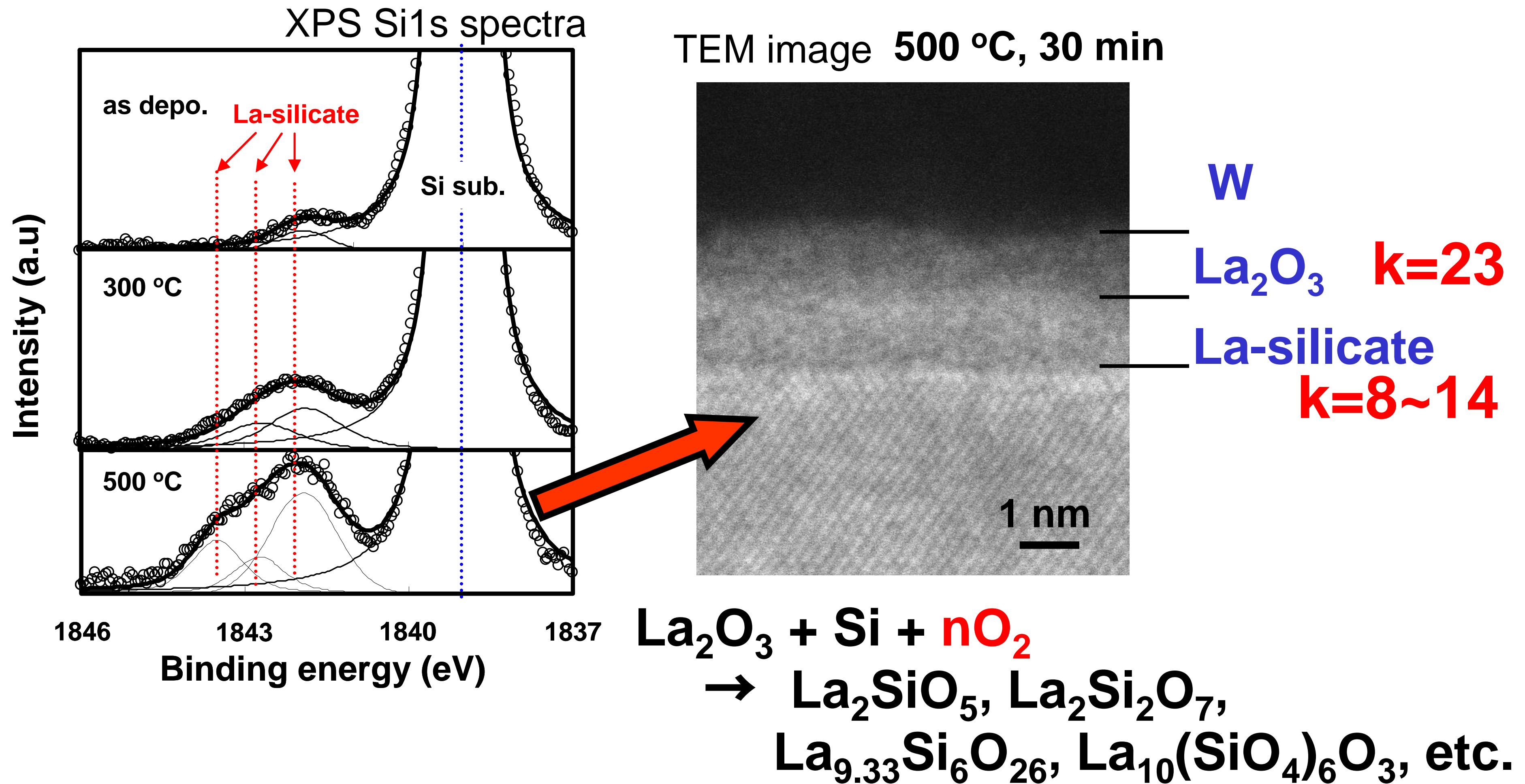
HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

La-Silicate Reaction at La_2O_3/Si

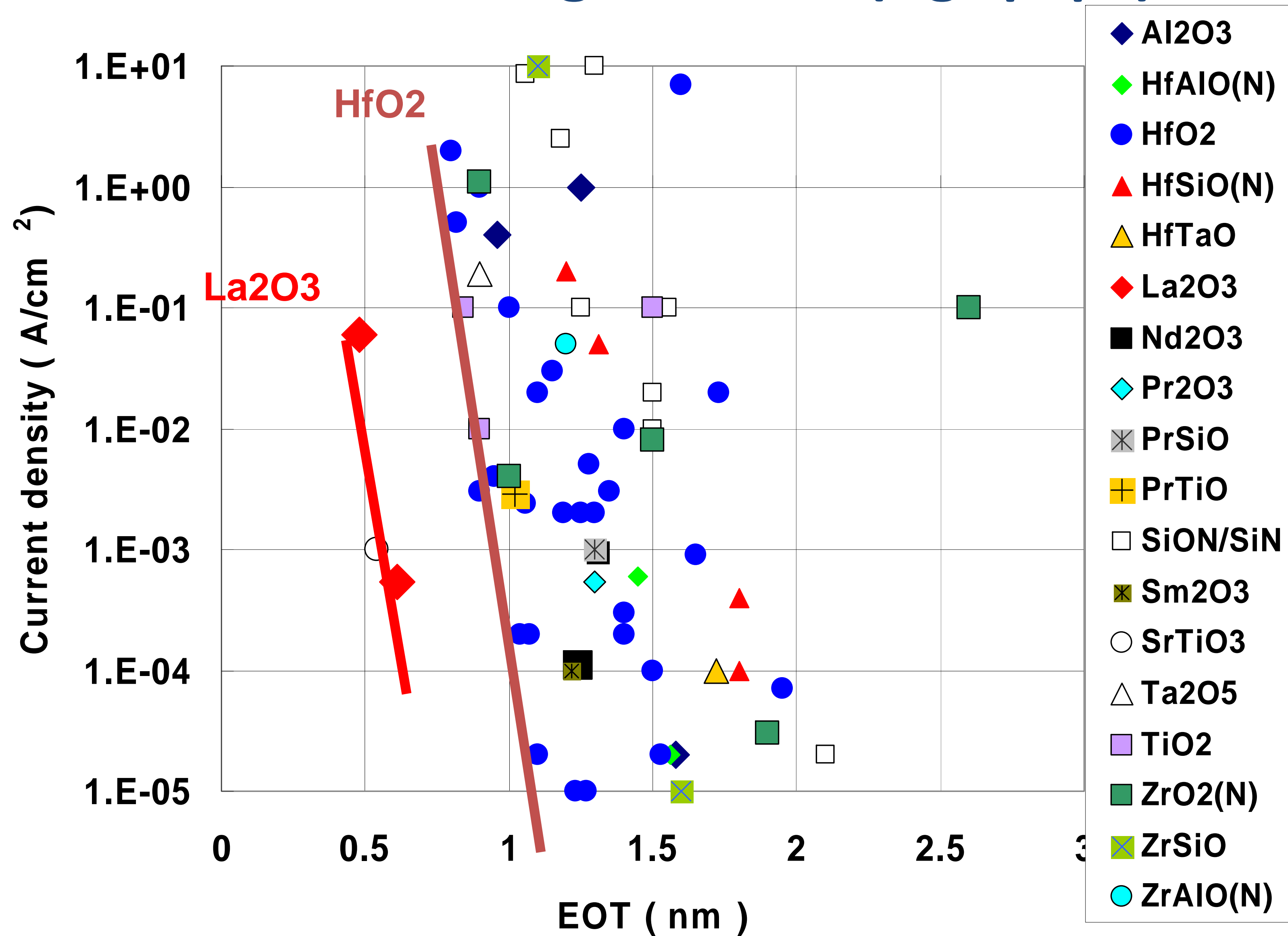
Direct contact high-k/Si is possible



$La_2O_3 + Si + nO_2$
$\rightarrow La_2SiO_5, La_2Si_2O_7,$
$La_{9.33}Si_6O_{26}, La_{10}(SiO_4)_6O_3$, etc.

La_2O_3 can achieve direct contact of high-k/Si

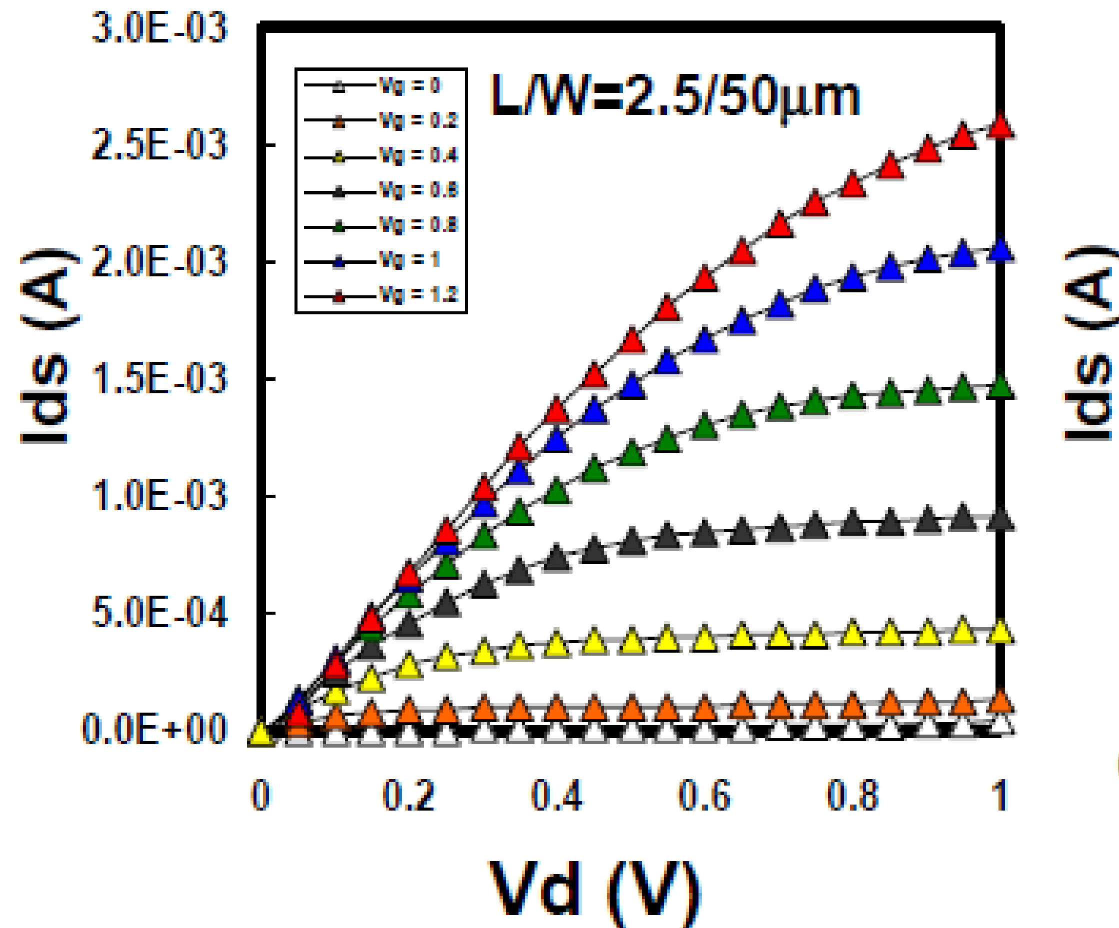
Gate Leakage vs EOT, (Vg=|1|V)



EOT = 0.48 nm

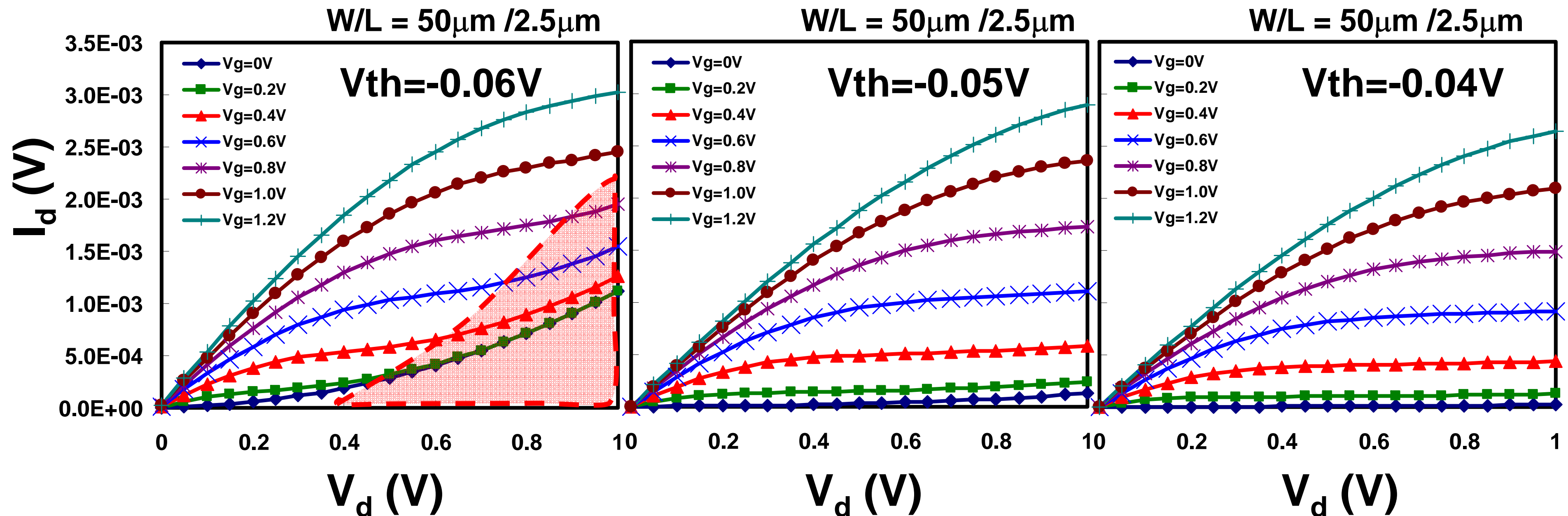
Our results

Transistor with La2O3 gate insulator



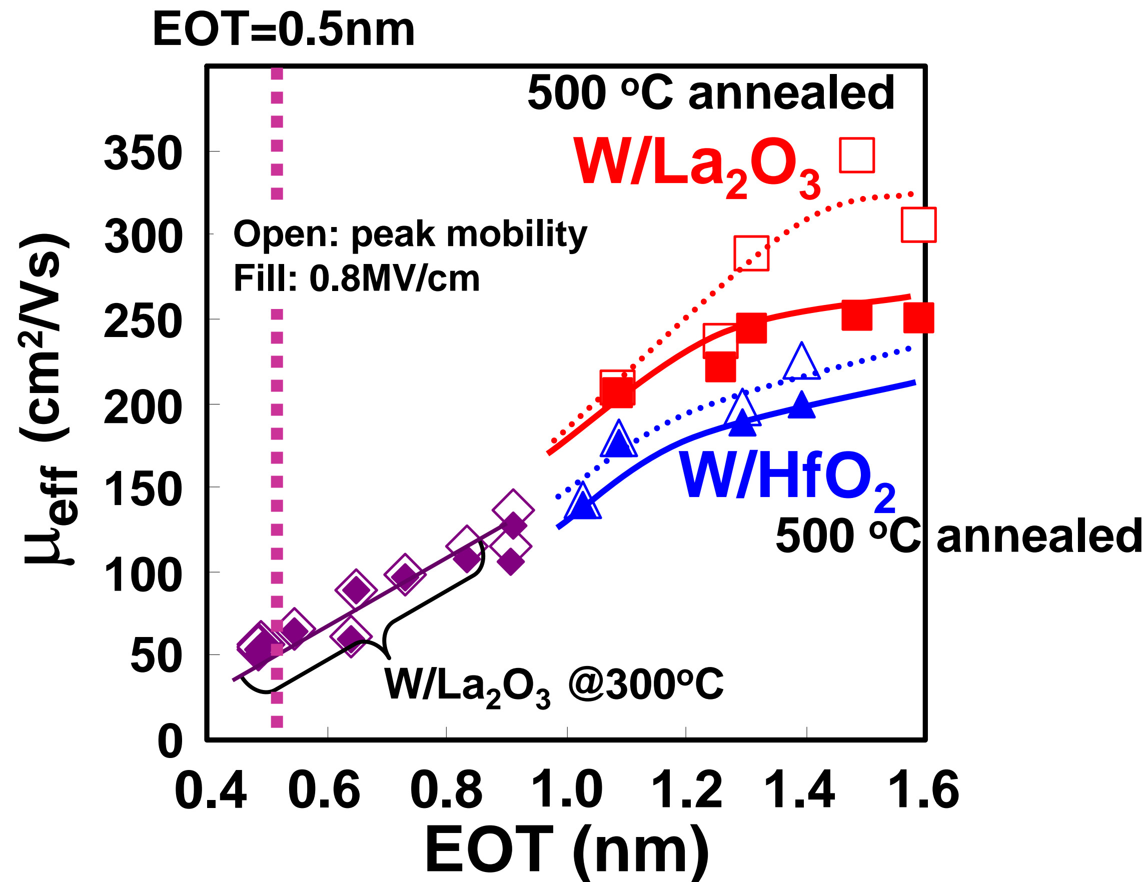
EOT=0.37nm

La2O3



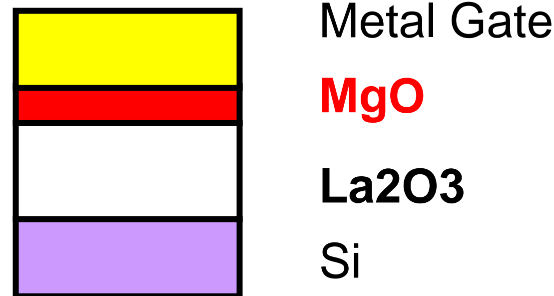
0.48 →0.37nm Increase of Id at 30%

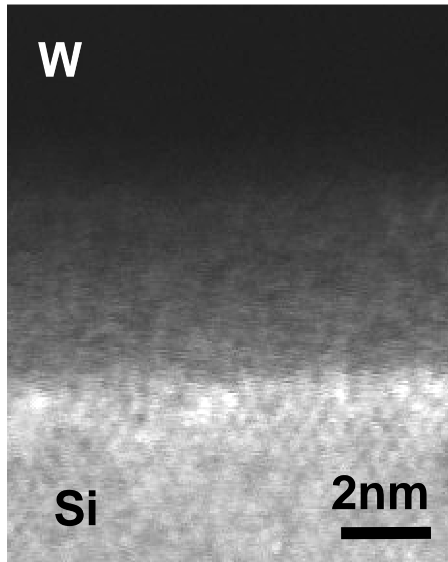
μ_{eff} of W/La_2O_3 and W/HfO_2 nFET on EOT



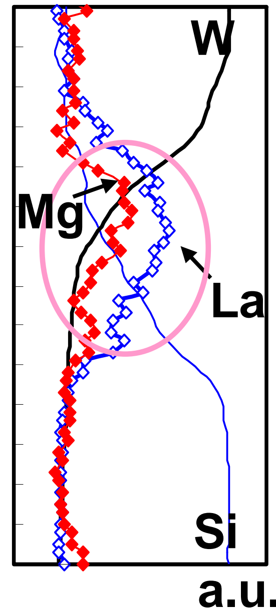
- W/La_2O_3 exhibits higher μ_{eff} than W/HfO_2
- μ_{eff} start degrades below EOT=1.4nm

Gate Metal Induced Defects Compensation

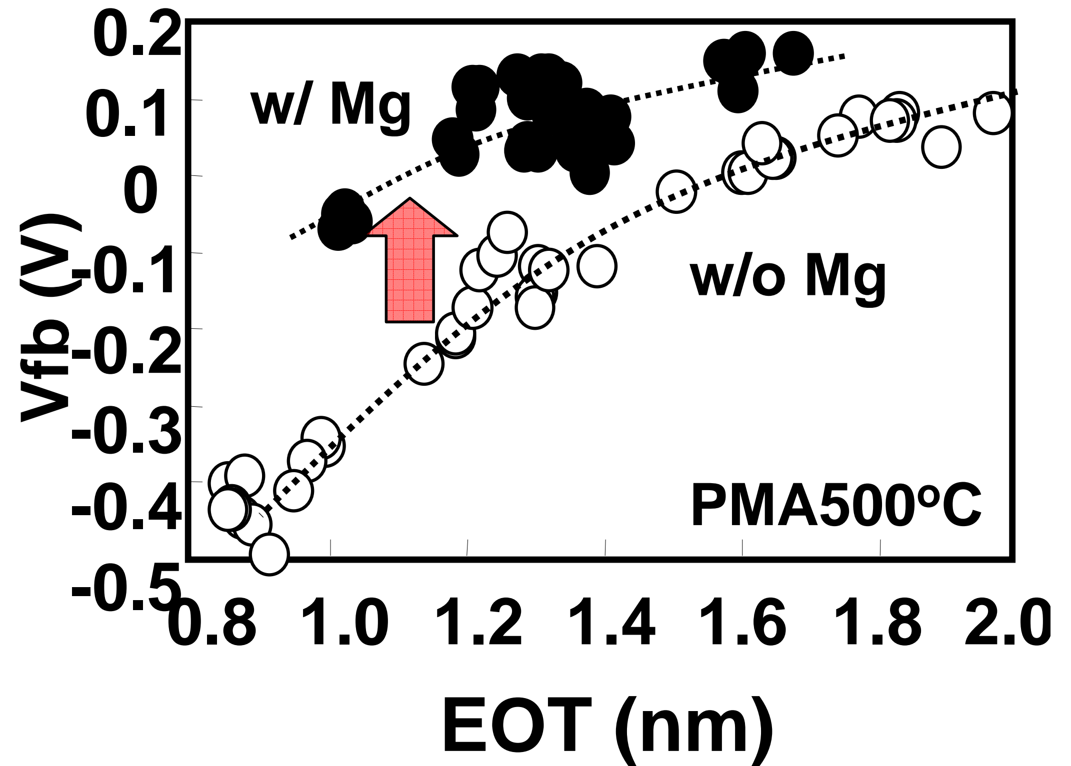




TEM

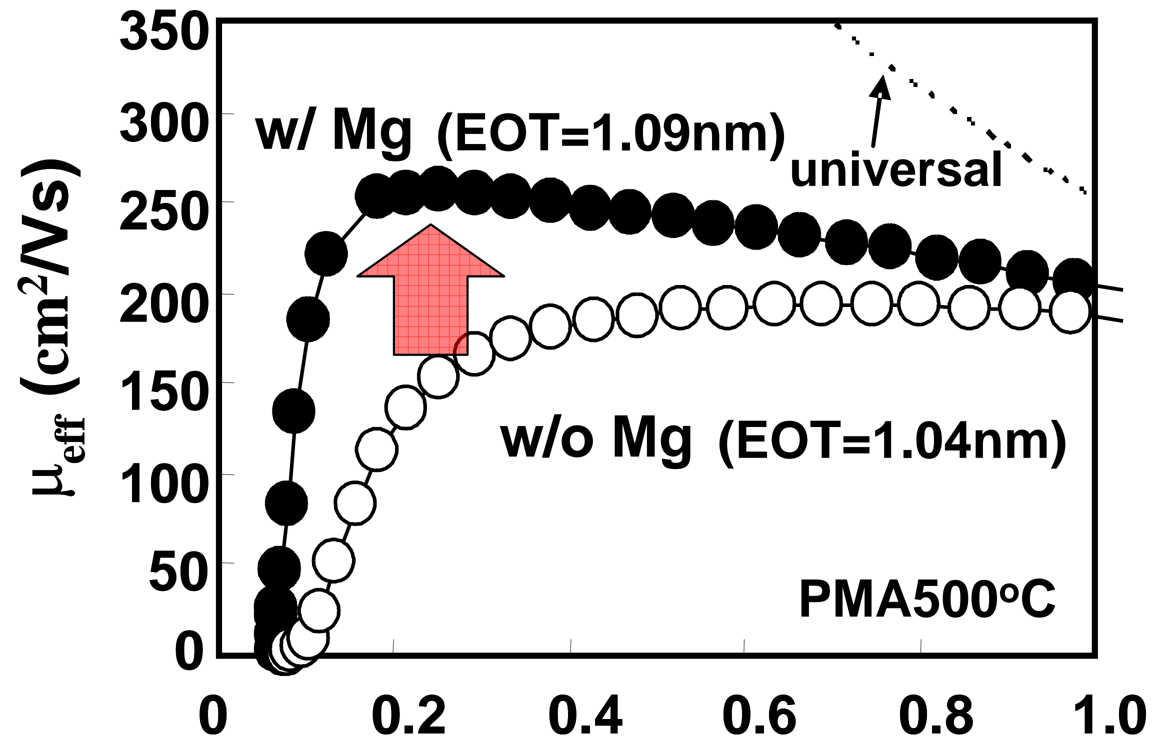


EDX



Suppression of aggressive shift in V_{fb}

Mobility Improvement with Mg Incorporation

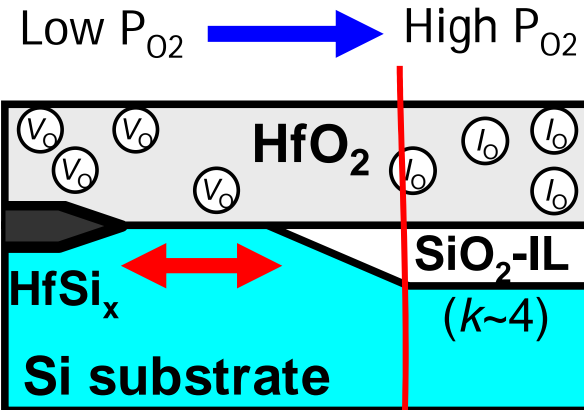


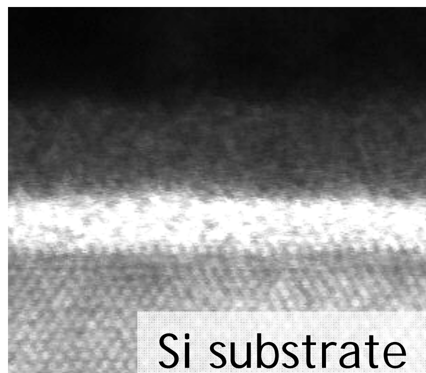
Recovery of μ_{eff} mainly at low E_{eff}

Interface and bulk properties of reactively formed La-silicate

Direct contact of high-k/Si by silicate formation

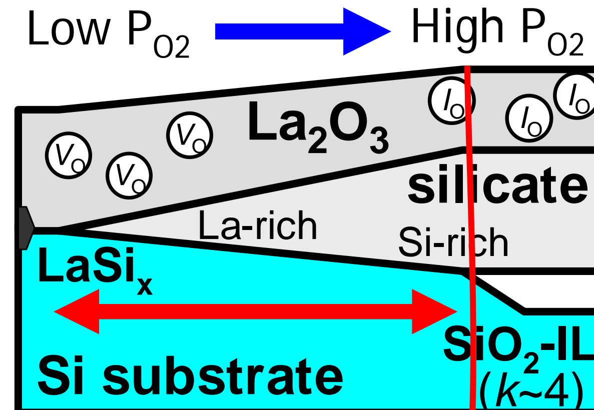
HfO_2 case

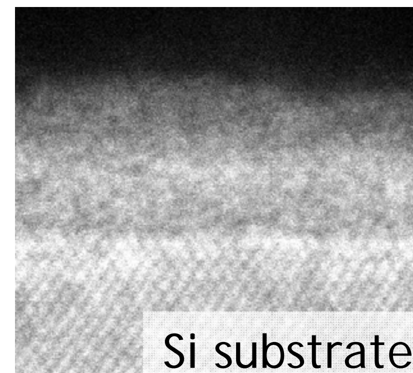




SiO_2 IL formation

La_2O_3 case

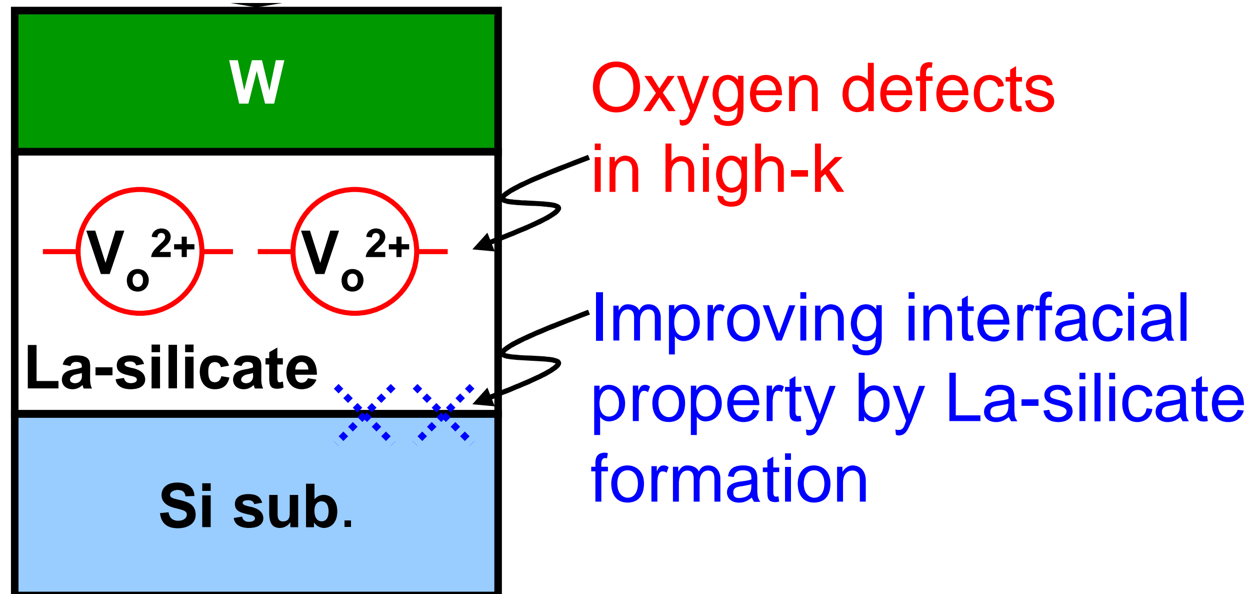




silicate formation

Direct contact can be achieved with La_2O_3 by forming silicate at interface
Control of oxygen partial pressusre is the key for processing

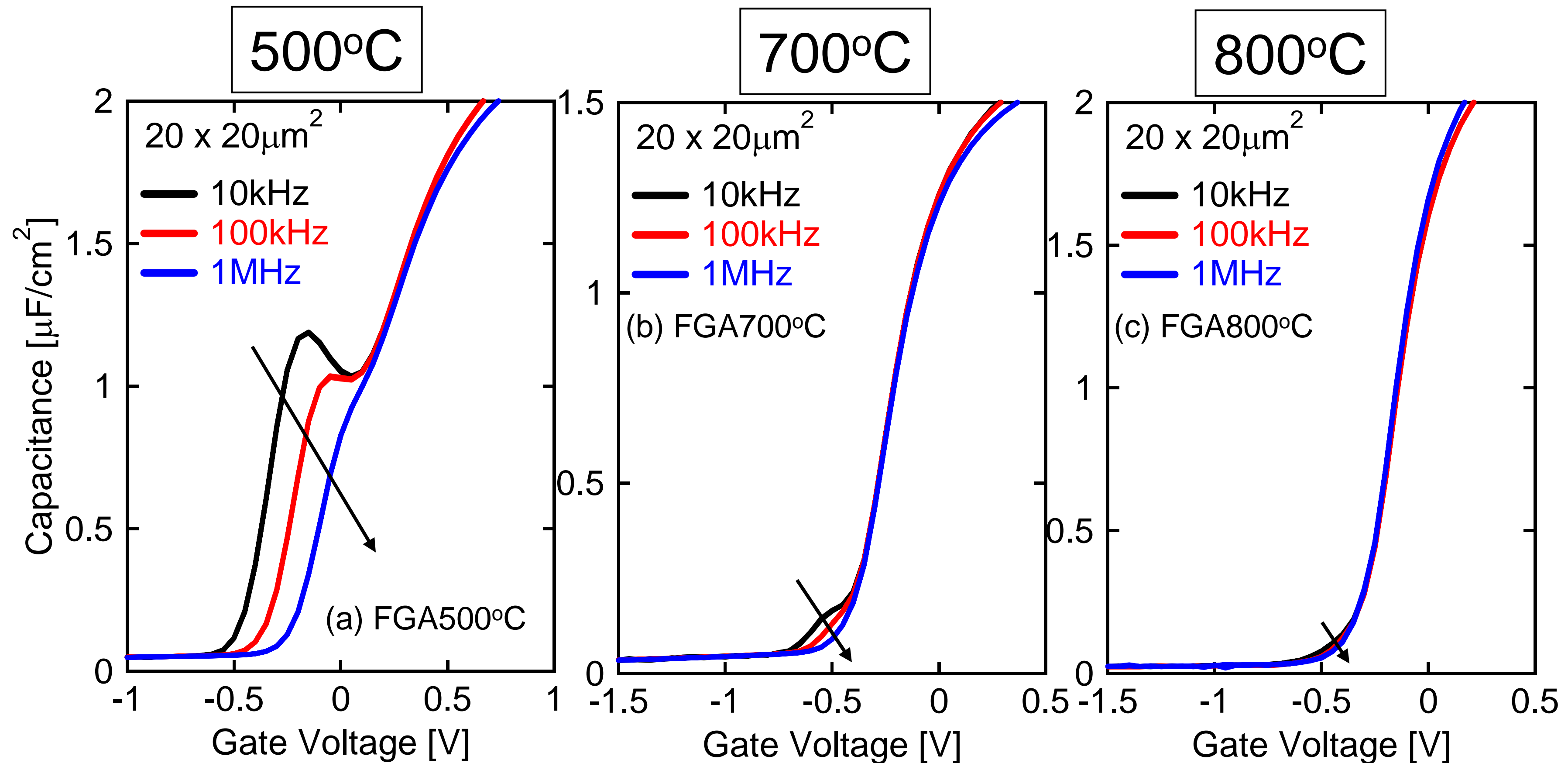
Issues in La-silicate/Si gate stack



(1) Interface property improvement by optimized annealing

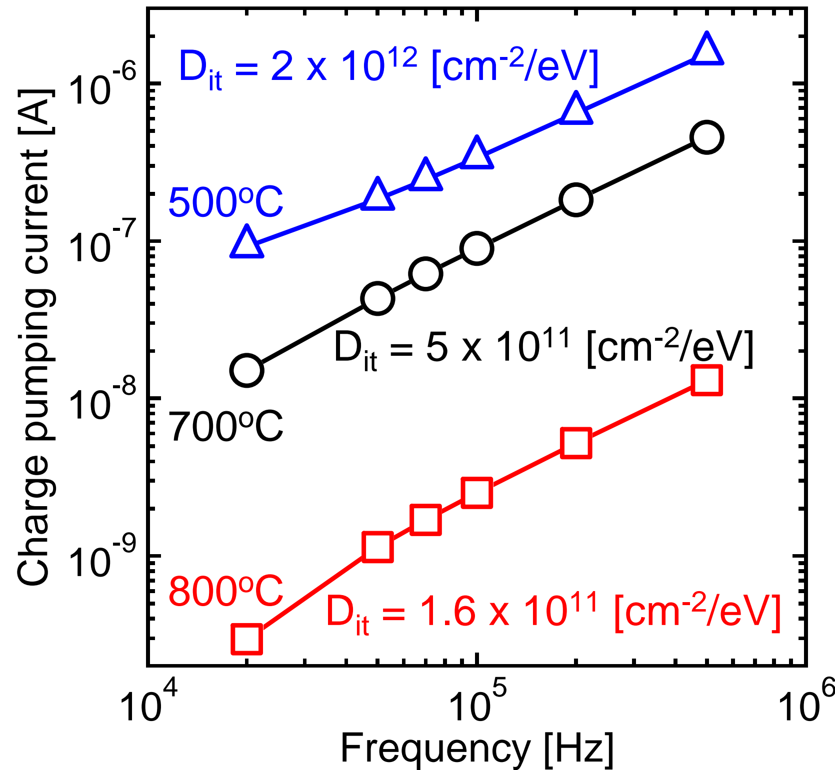
(2) Reduction of oxygen defects by oxygen partial pressure control

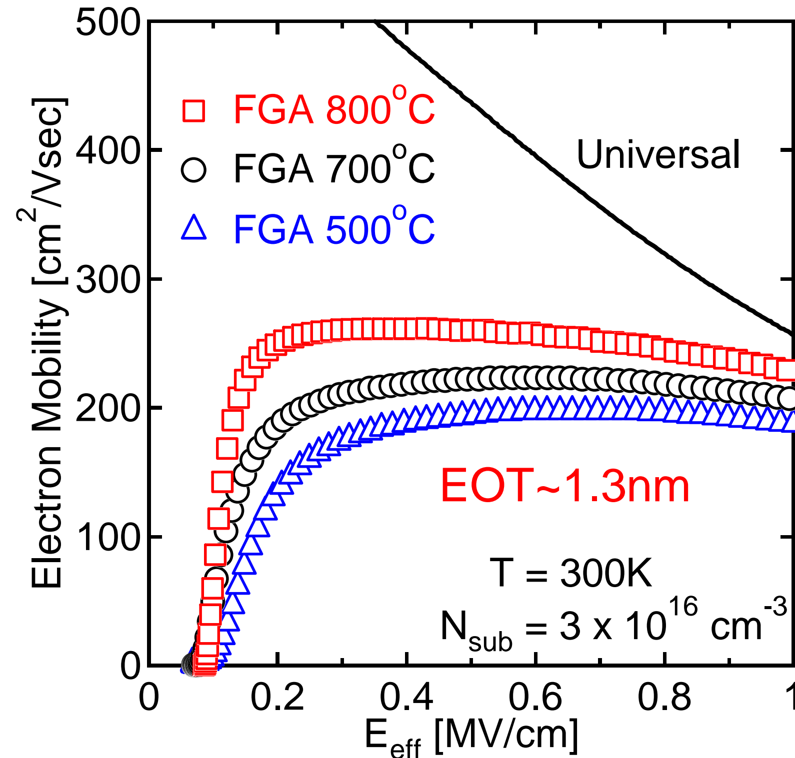
Interface properties of La-silicate/Si



A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)

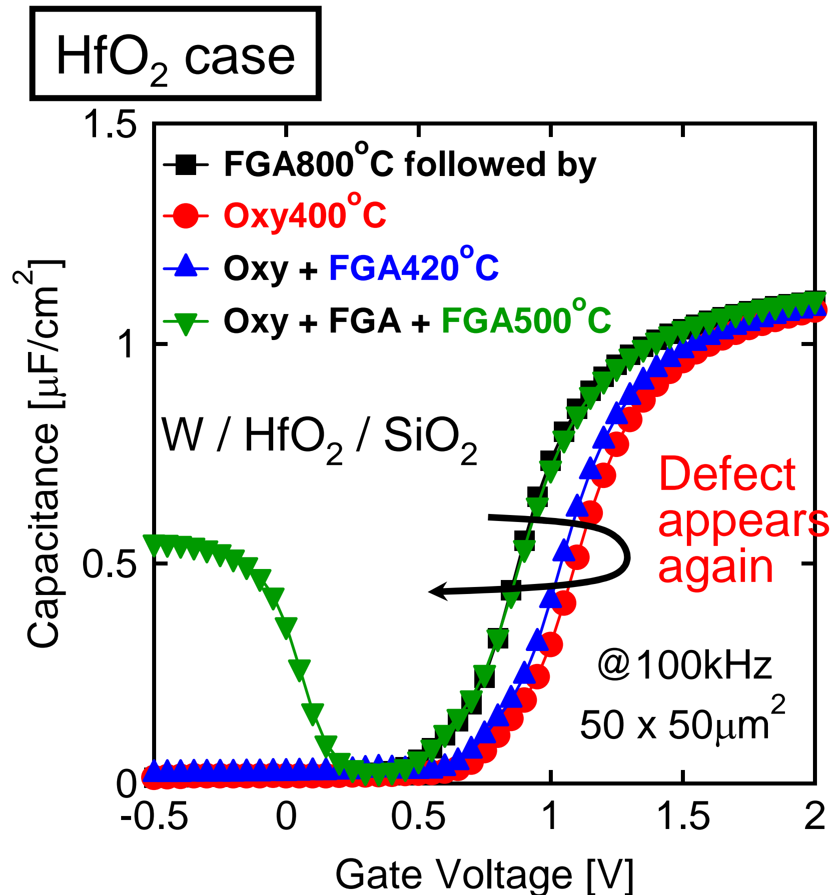
Interface properties of La-silicate/Si (cont.)

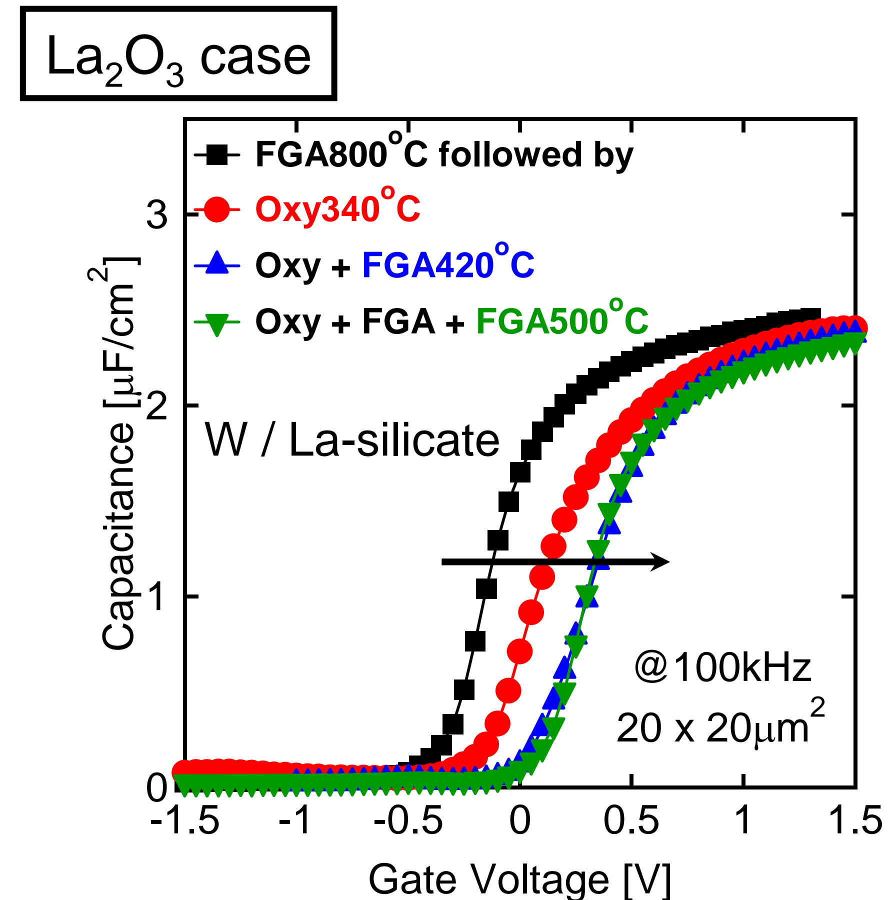




A low D_{it} of 1.6x10^{11} cm^{-2}/eV, results in better electron mobility.

Defect recovery by additional oxygen annealing

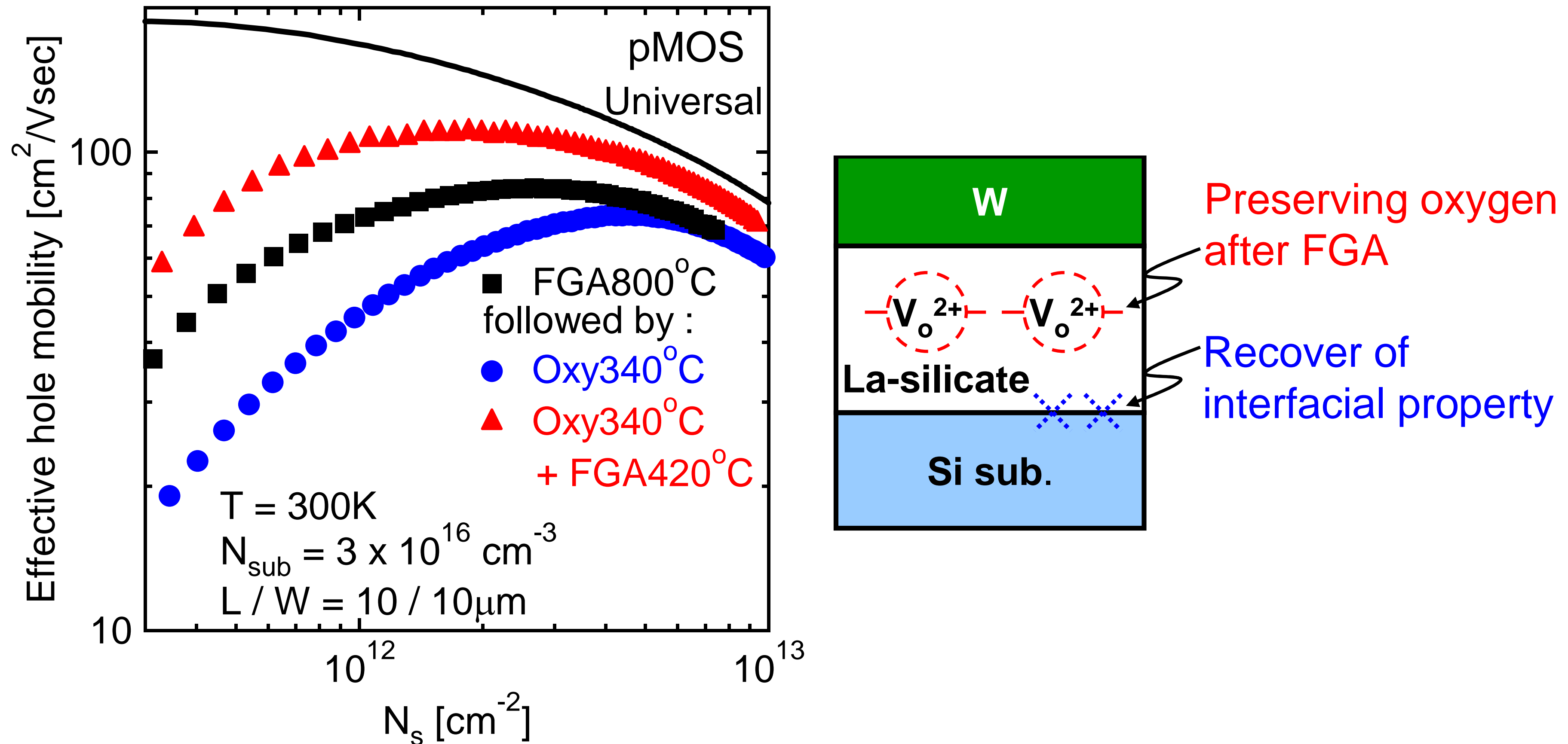




Additional oxygen atom supply recovers the oxygen defects

Complete recovery of defects with La-silicate, owing to strong bonding of covalent nature in silicate

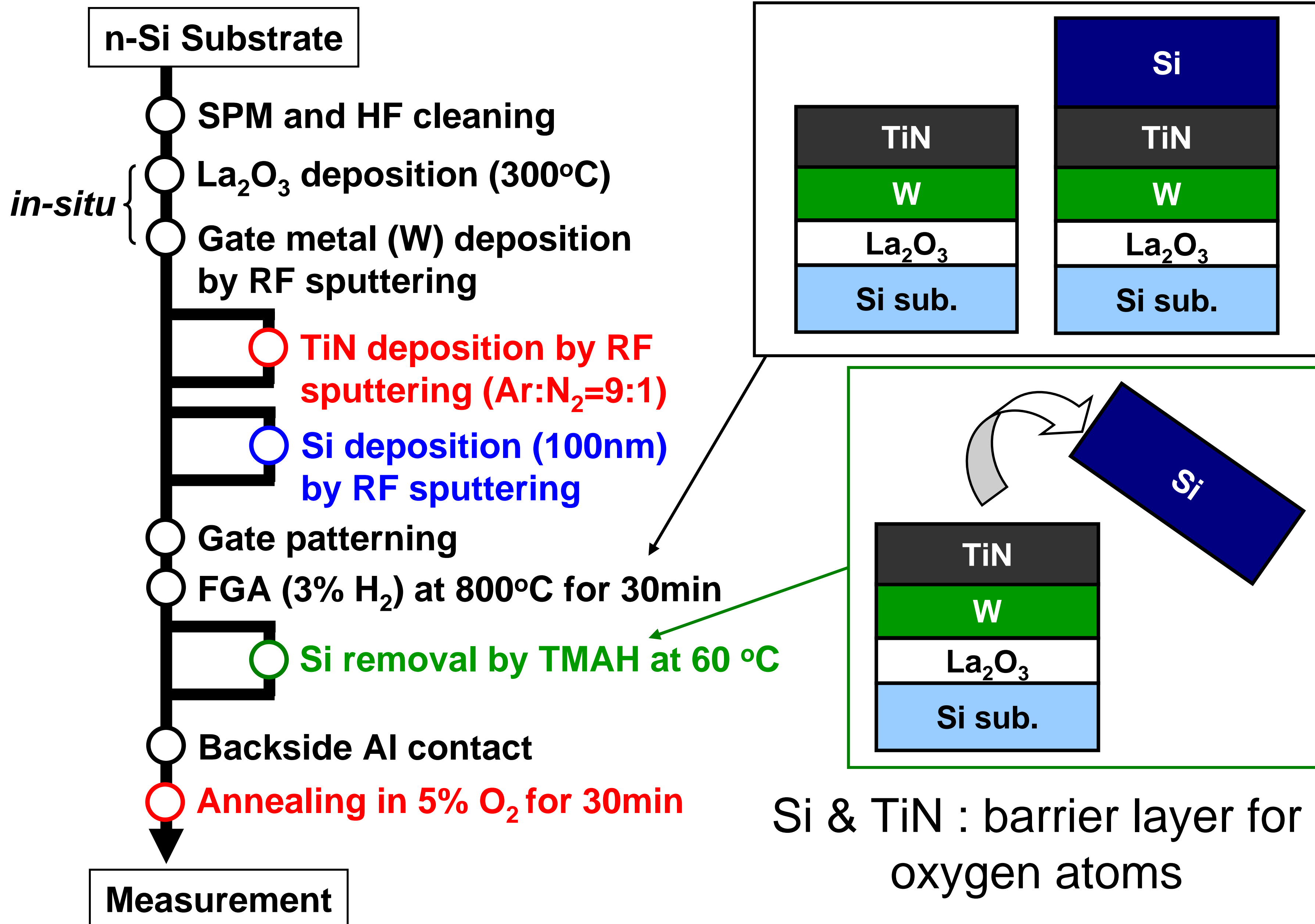
Mobility improvement by optimized interface & defect recovery process



Large improvement in mobility was confimed by combining the two processes

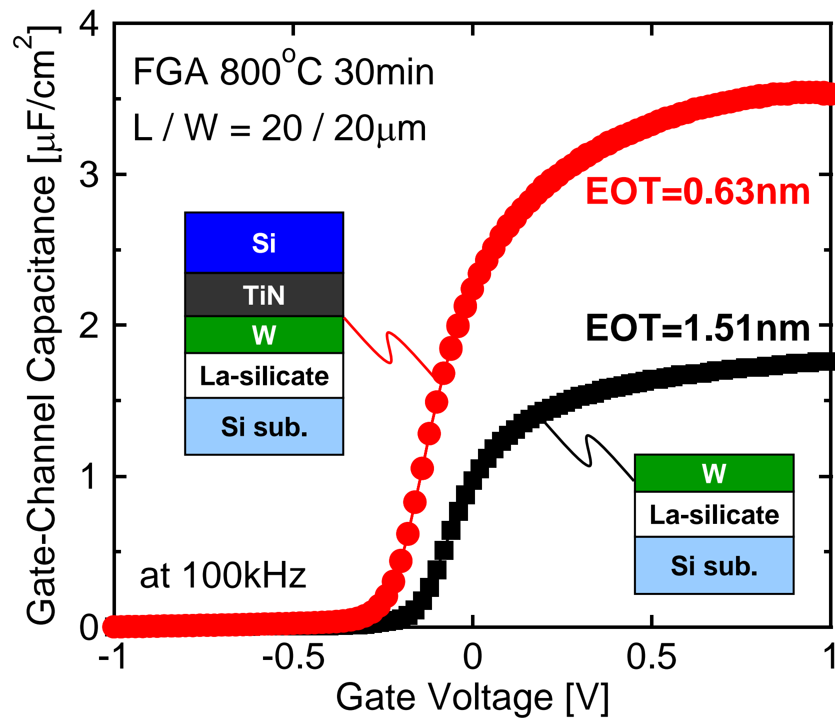
Oxygen partial pressure control by gate material selection

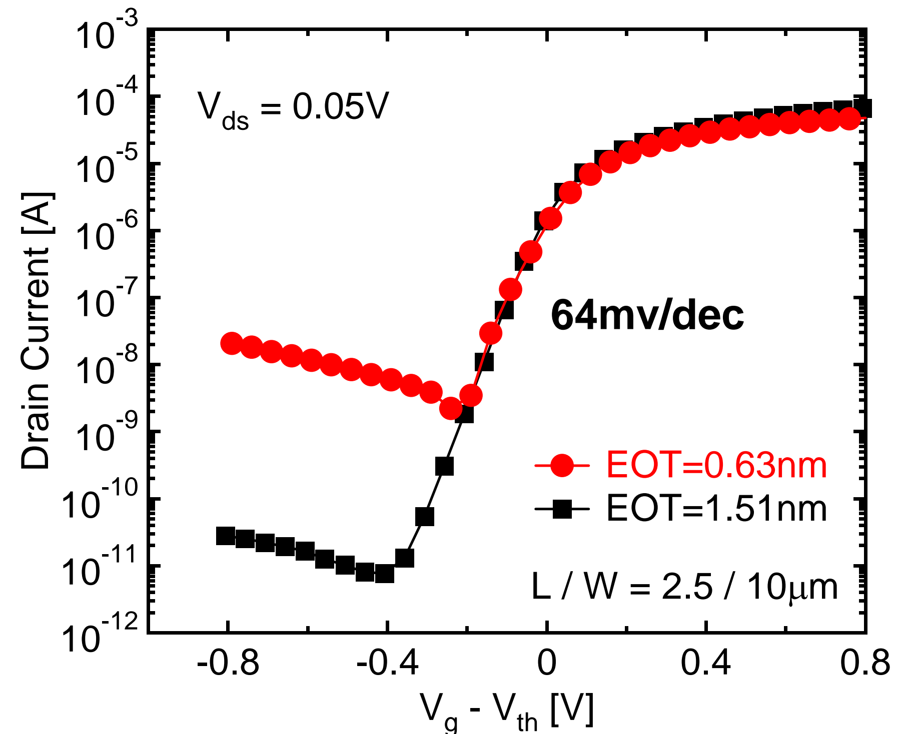
Si & TiN capping as oxygen barrier layer



Si & TiN : barrier layer for oxygen atoms

Si/TiN capping effect on CV characteristics

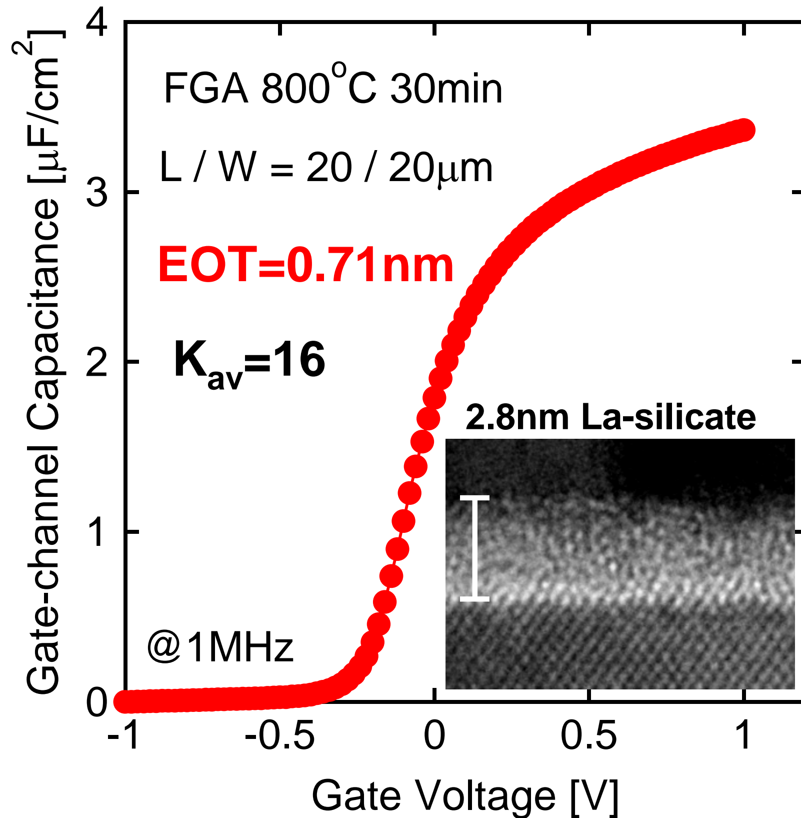


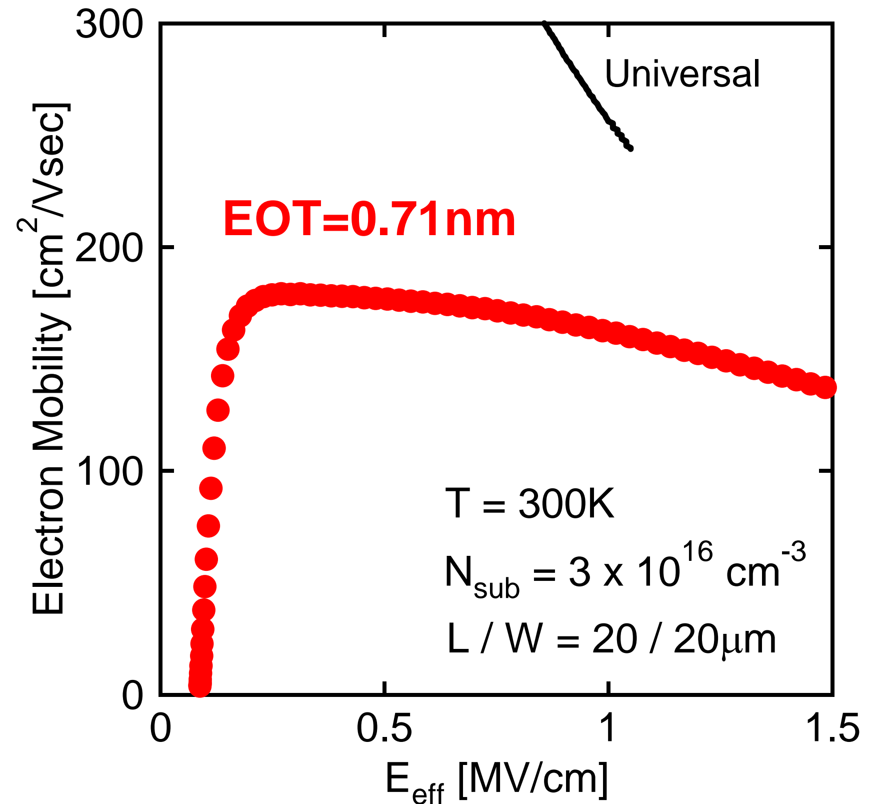


Si/TiN capping suppresses the EOT growth
→ suppress the excess silicate reaction

SS of 64 mV/dec. can be obtained

EOT scaling with Si/TiN capped metal gate





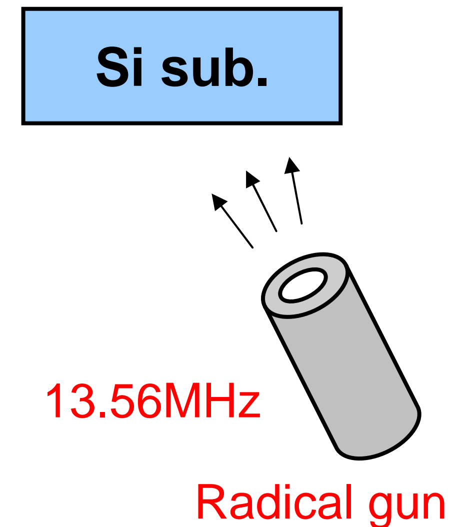
A small EOT of 0.71nm with fairly nice mobility can be obtained

Impact of nitrogen incorporation into La-silicate

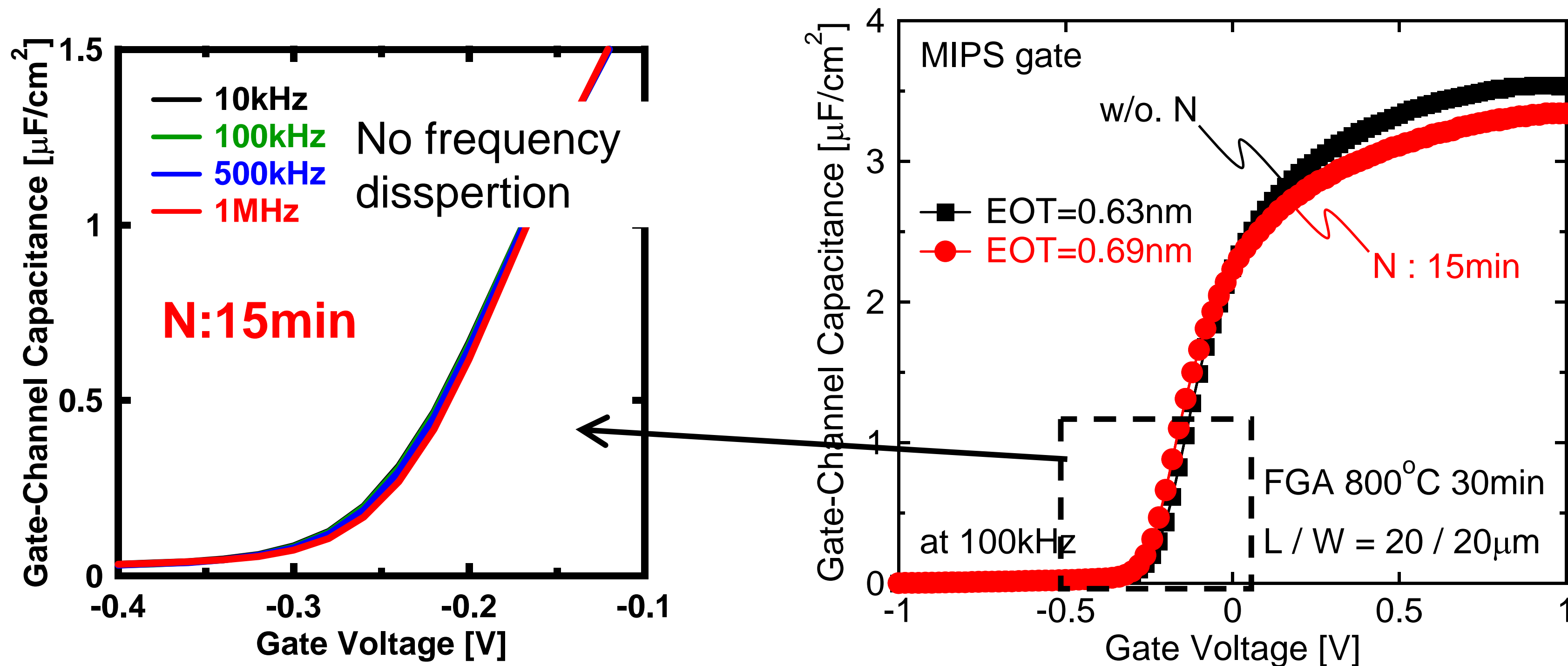
Fabrication procedure with nitridation

LOCOS isolated p-Si wafer (S/D pre-formed)

- **SPM and HF cleaning**
- **Radical Nitridation (300W, N_2:1sccm)**
  Nitrogen : ~ 1.5 x 10^{15} atoms/cm^2
- *in-situ*:
  - **La_2O_3 deposition (300^oC) by e-beam evaporation**
  - **Gate metal (W) deposition by RF sputtering**
- **TiN & Si deposition by RF sputtering for MIPS stacks**
- **Gate patterning**
- **FGA (H_2:N_2=3%:97%) at 800 ^oC for 30min**
- **S/D & Backside Al contact**
- **FGA (H_2:N_2=3%:97%) at 420 ^oC for 30min**

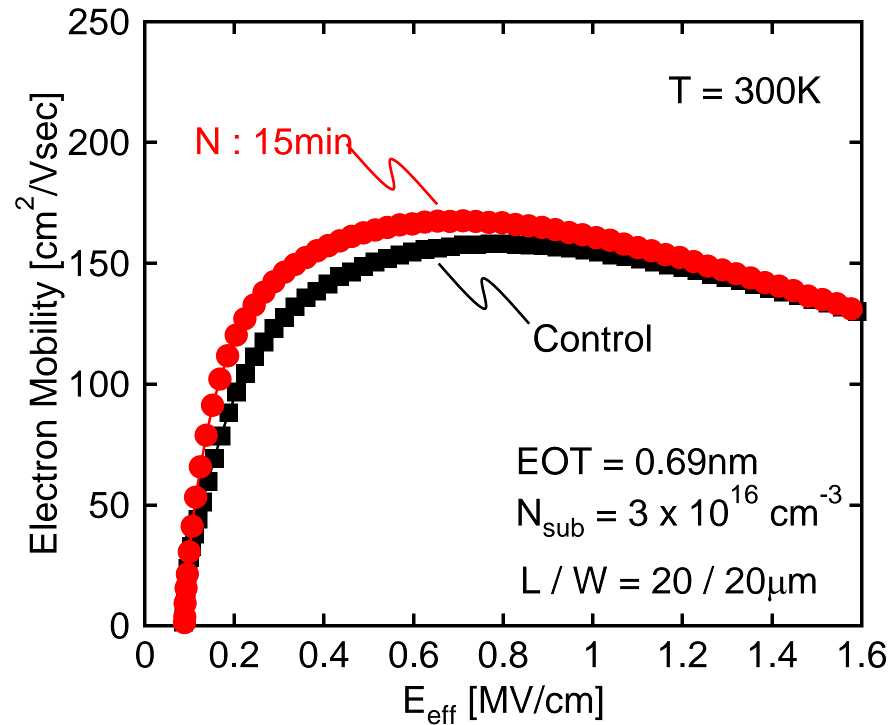


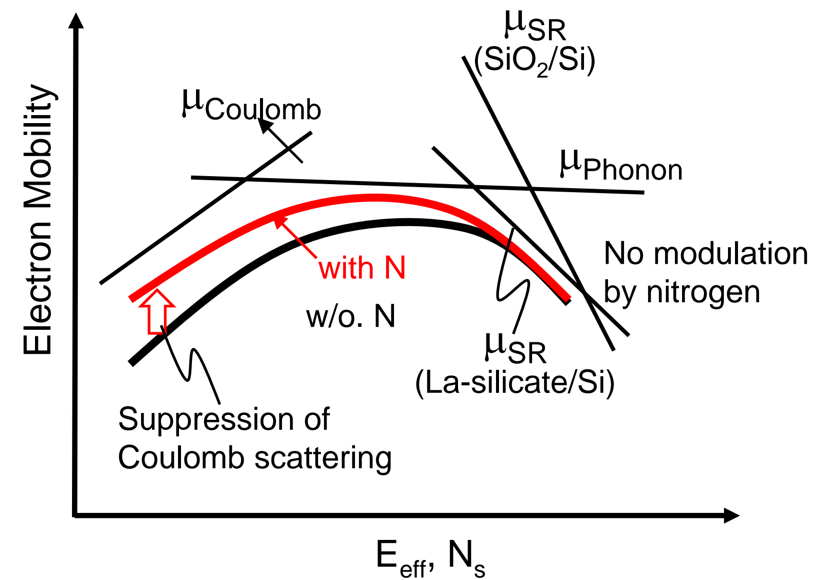
Interface properties of La-silicate with nitrogen



Nitrogen incorporation do not degrade the interface properties

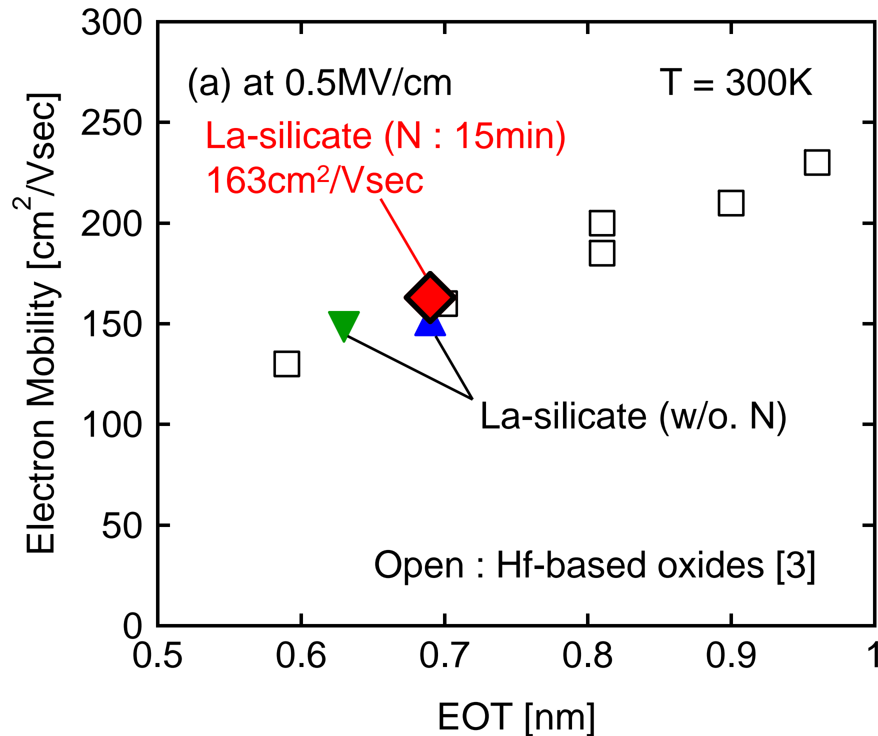
Improved mobility by La-silicate with nitrogen

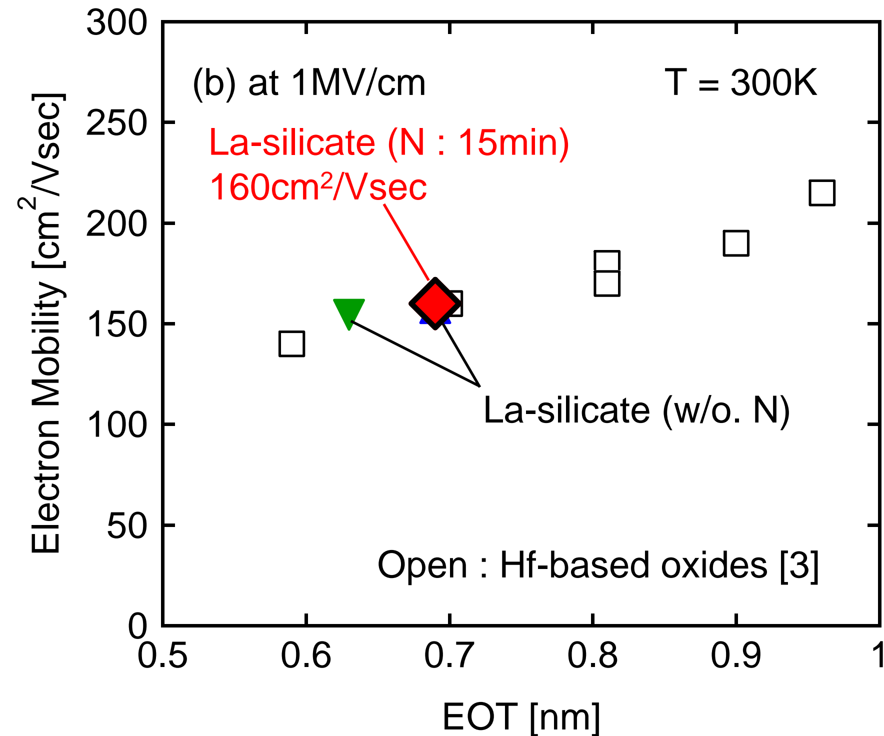




Nitrogen incorporation improves the mobility, especially at low field

Mobility benchmarking of La-silicate (with N)





La-silicate with nitrogen shows promissing performance for EOT towrads 0.5 nm

Question:

How far we can go with downscaling?

How far can we go?

Past

0.7 times per 3 years

In 40 years: 18 generations, Size 1/300, Area 1/100,000

Now

1970年

10μm → 8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm → 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

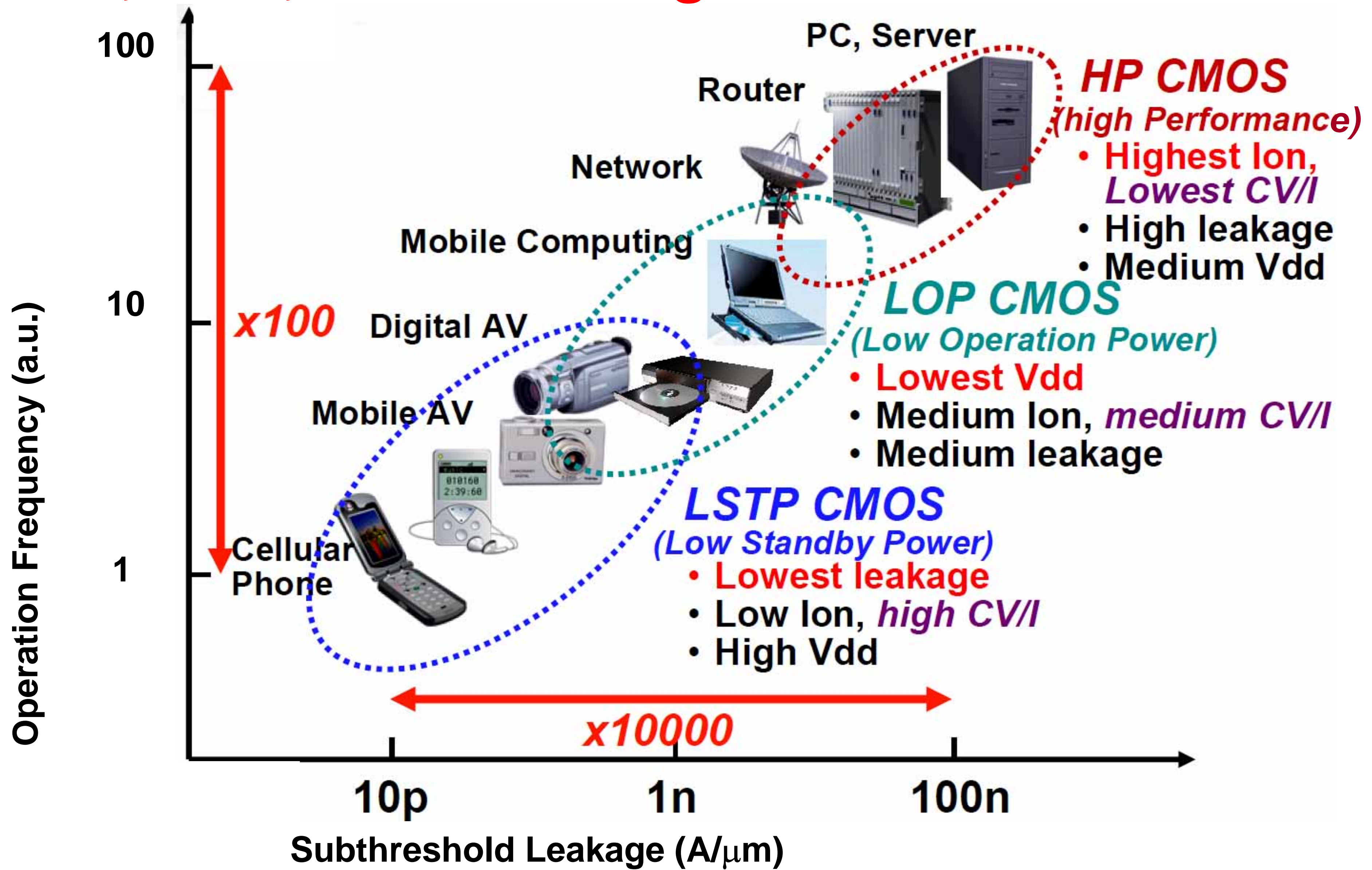
---

Future

→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

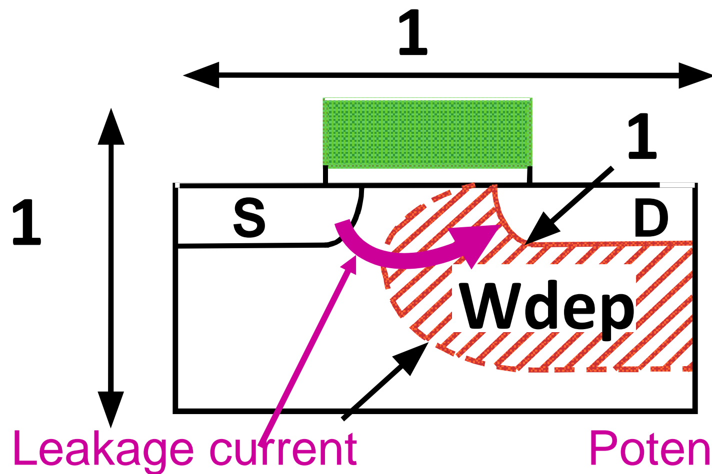
- **At least 4,5 generations to 8nm**
- **Hopefully 8 generations**

HP, LOP, LSTP for Logic CMOS



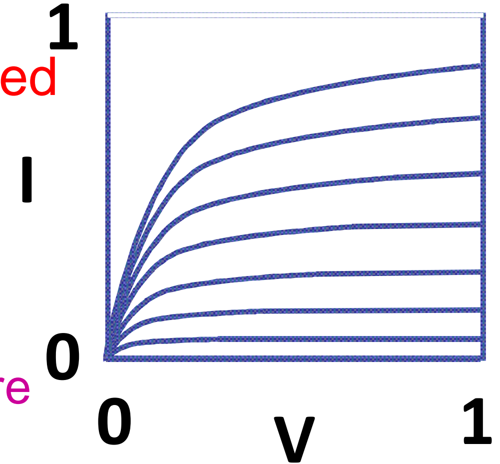
Source: 2007 ITRS Winter Public Conf.

Scaling Method: by R. Dennard in 1974



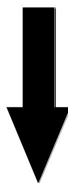
Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage between S and D



Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

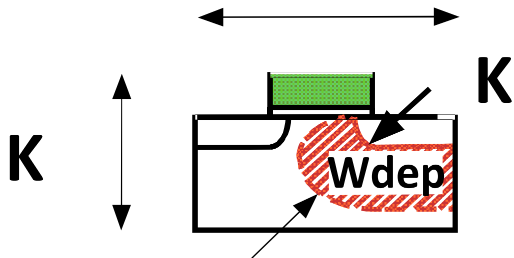
K=0.7 for example



X , Y , Z : K, V : K, Na : 1/K

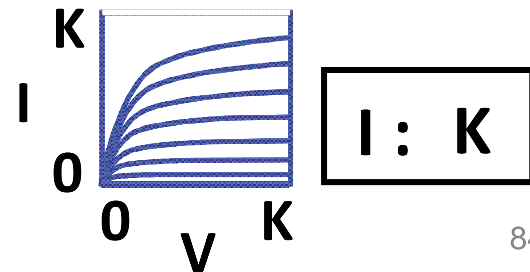
By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$\text{Wdep} \propto \sqrt{V/Na}$$

: K

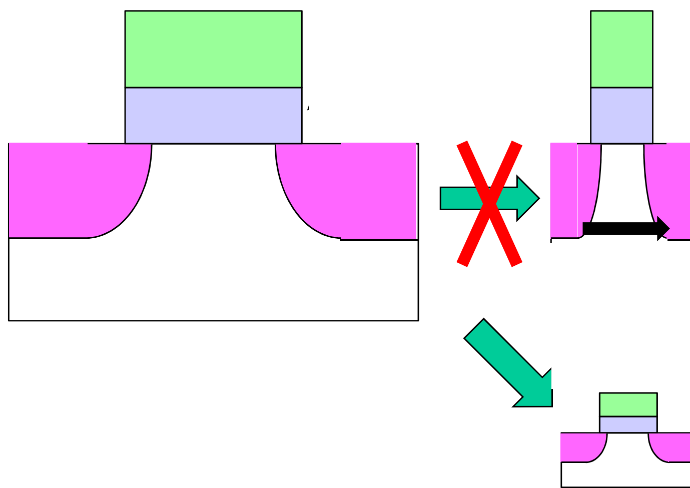


I : K

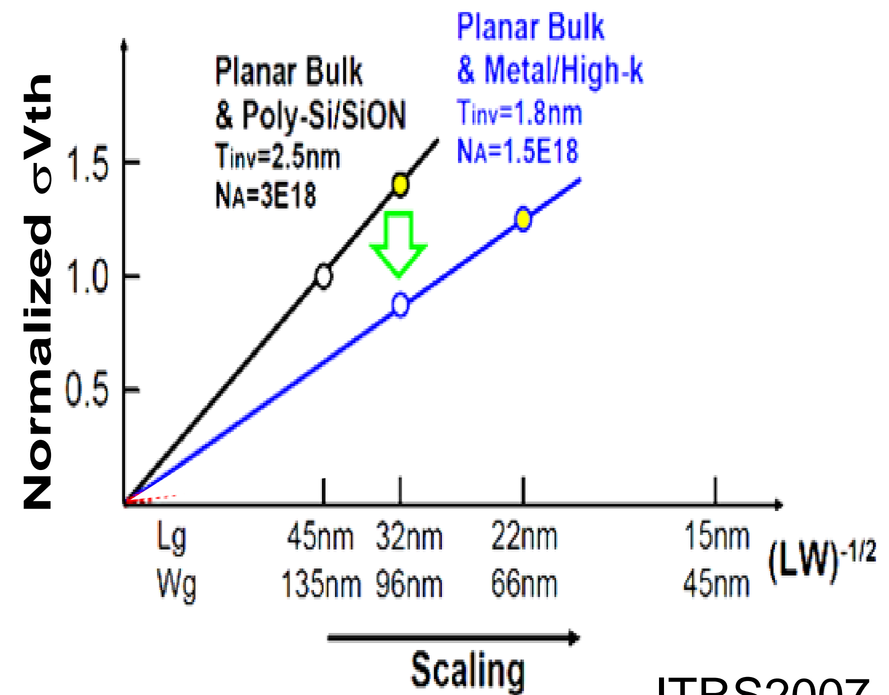
Scaling of high beyond 0.5 nm is important

Power of FET $= CV^2/2 \propto D^3$ $(=L^3)$

Problems
→SCE
→Variation in Vth
→Increase in Off-leakage current



Solution



ITRS2007

Down scaling is the most effective way of Power saving.

It has been always discussed about the limit of downscaling, but the down scaling of MOSFETs is still possible for another 10 or 20 years!

3 important technological items for DS.

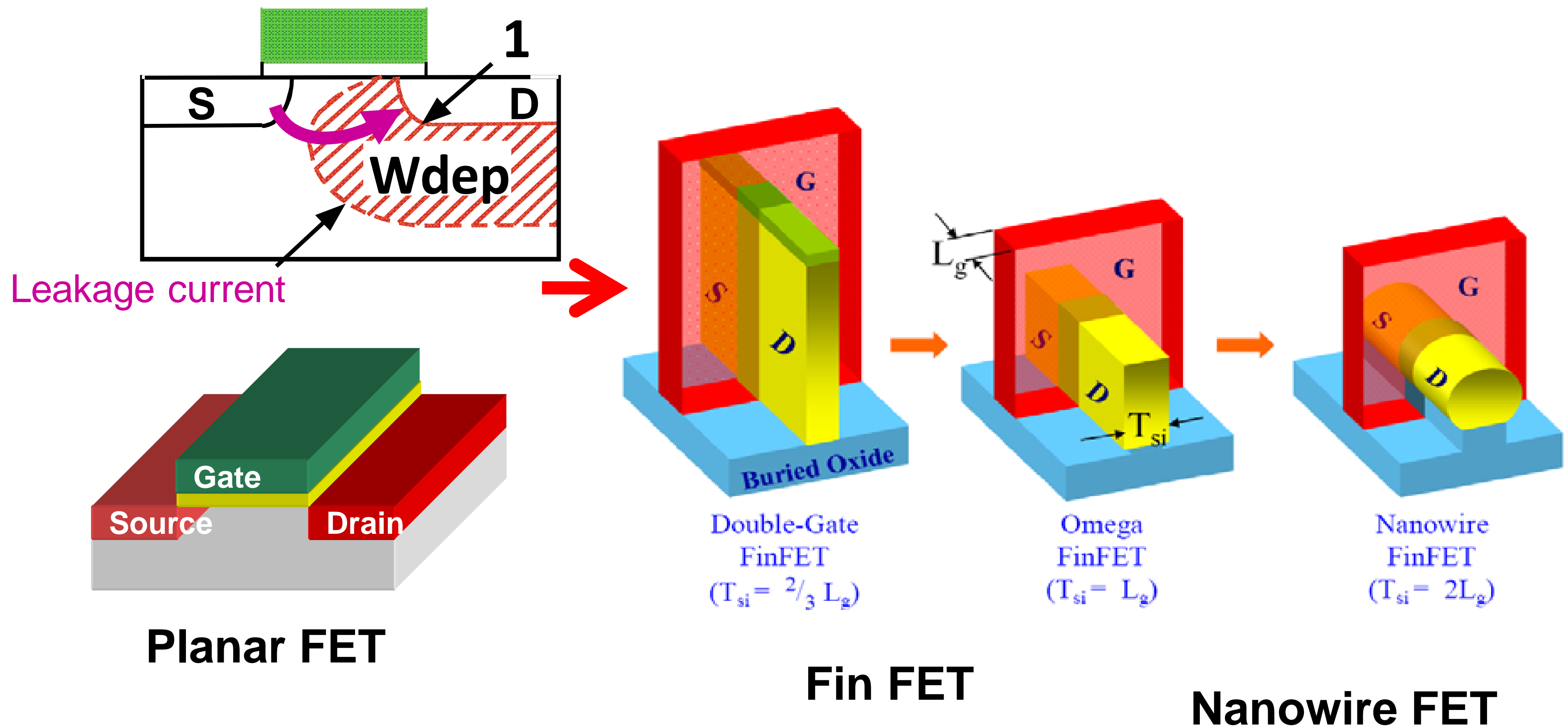
1. Thinning of high-k beyond 0.5 nm

2. Metal S/D

3. Si-Nanowire FET

Because of off-leakage control,

Planar → Fin→ Nanowire



Nanowire FET

First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
Device Structures																
Planar bulk																
FDSOI																
Multiple Gate																

2015

22 or 16nm node

Multiple Gate (Fin) FET

2020

11 or 8nm node

Nanowire FET

ITRS 2009

Bulk → Fin → Nanowire

Scaling Pathways

w and w/o 3rd gate ?

Bulk or SOI

Fin

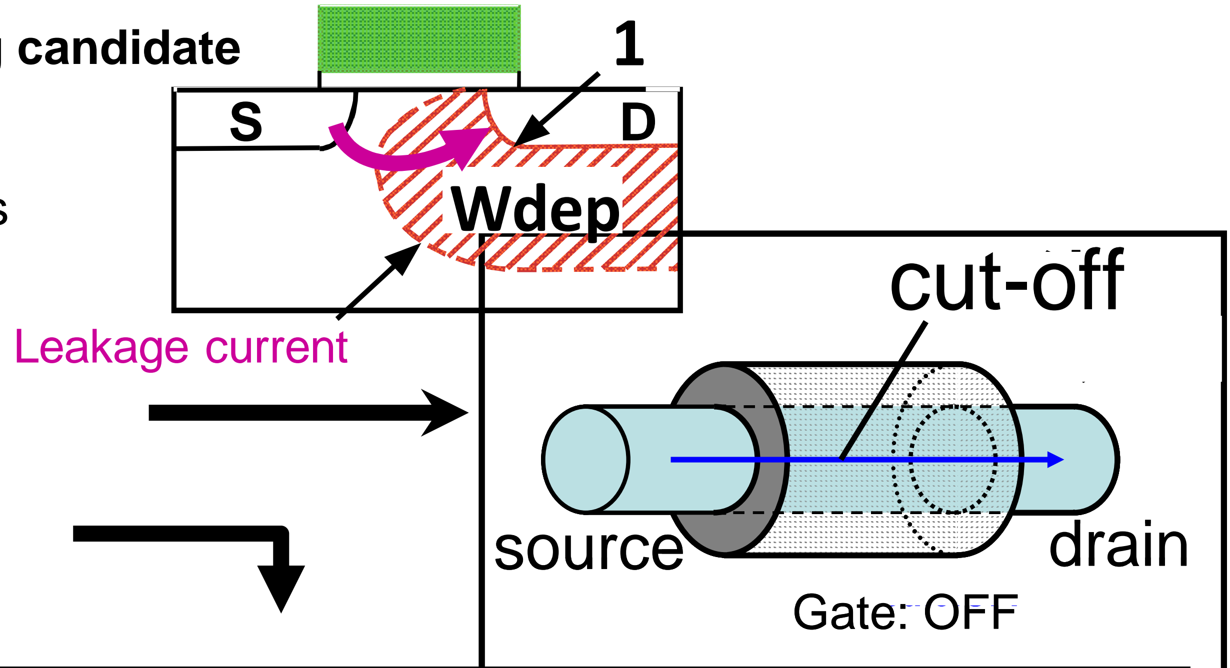
Si Nanowire

Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process

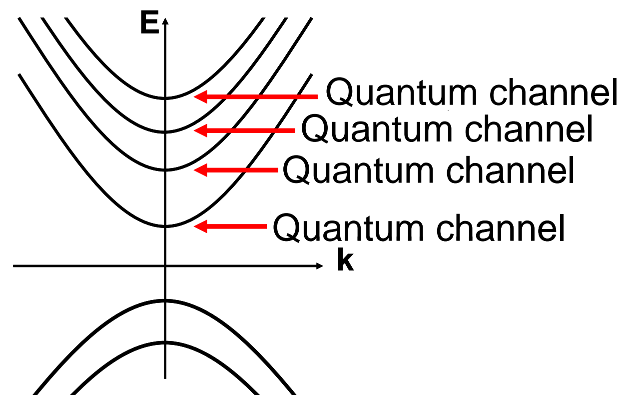
2. Good controllability of I_{OFF}

3. High drive current

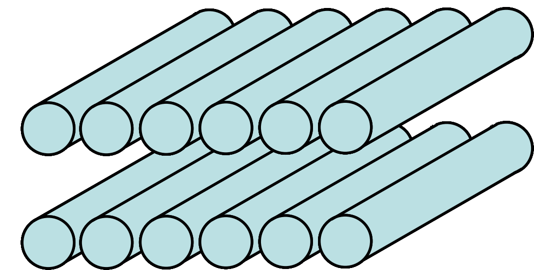


1D ballistic conduction

Multi quantum Channel

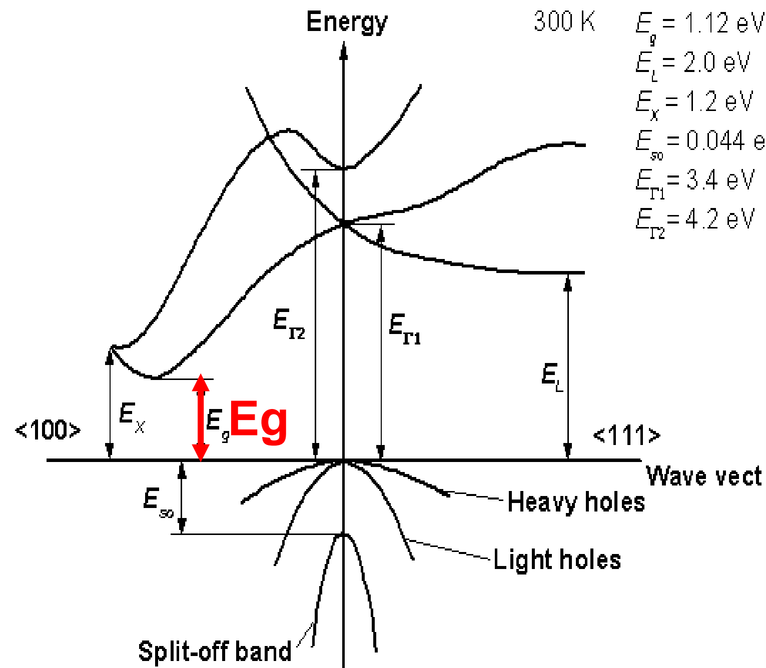


High integration of wires

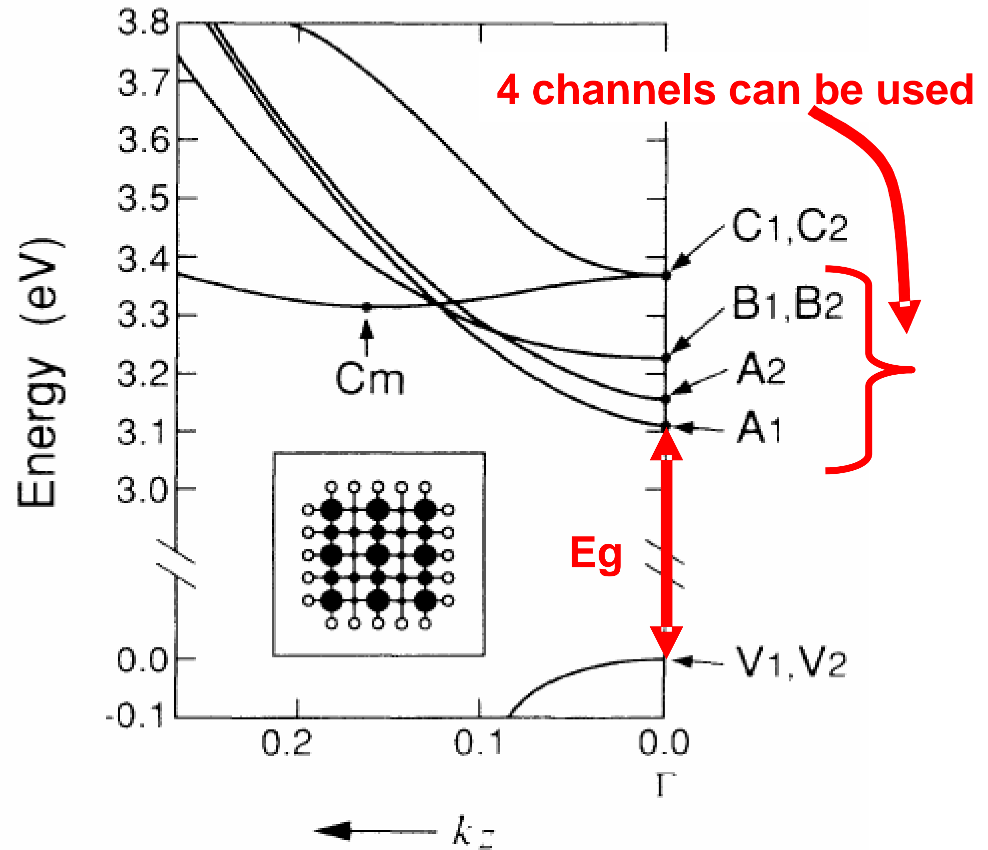


Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



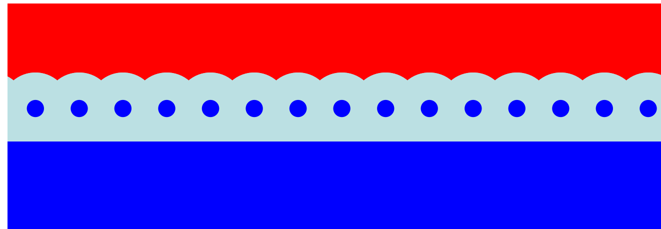
Energy band of Bulk Si



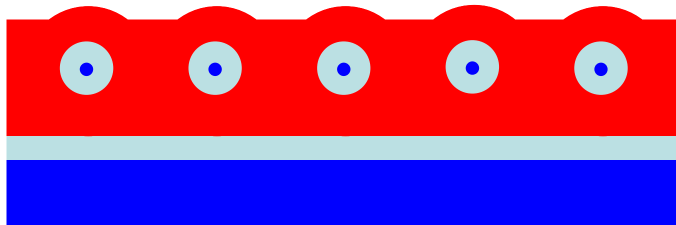
Energy band of 3 x 3 Si wire

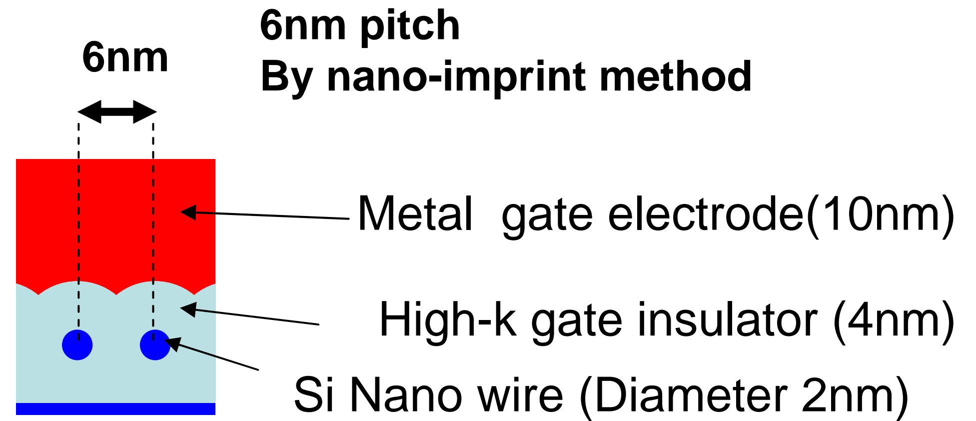
Maximum number of wires per 1 μm

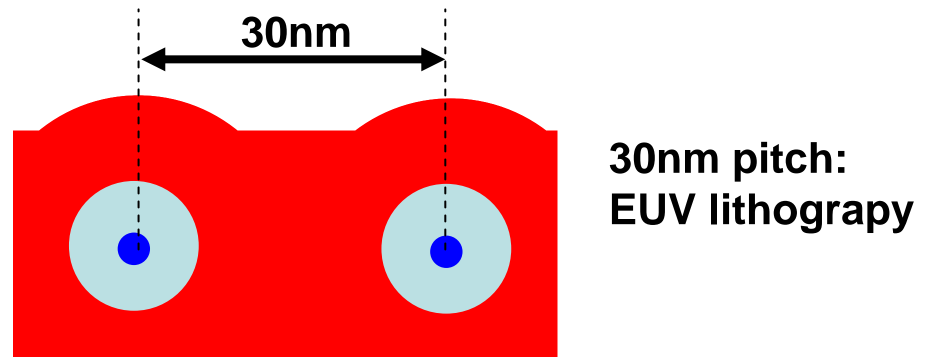
Front gate type MOS 165 wires /μm



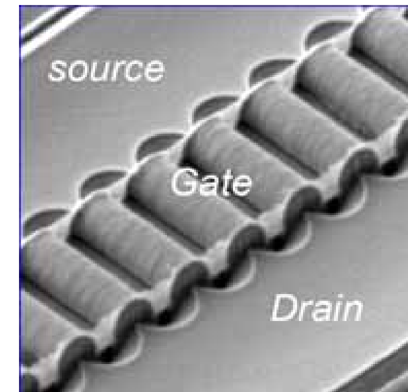
Surrounded gate type MOS 33 wires/μm





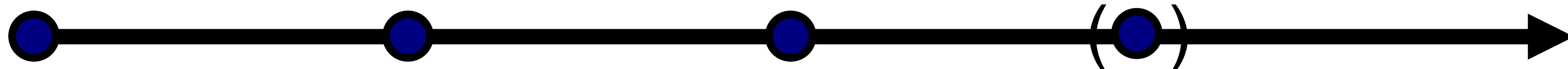


30nm pitch:
EUV lithograpy



Surrounded gate MOS

Device fabrication

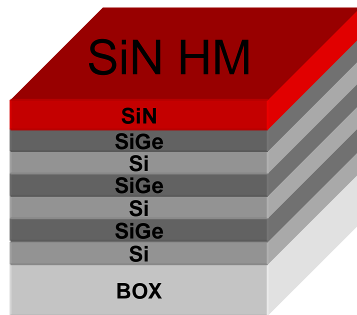


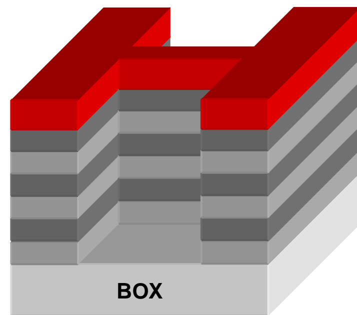
$Si/Si_{0.8}Ge_{0.2}$ superlattice epitaxy on SOI

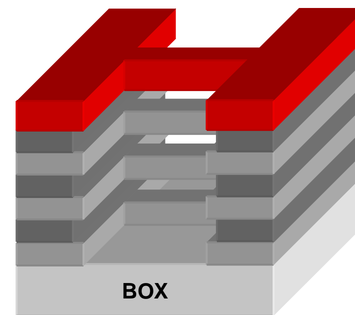
Anisotropic etching of these layers

Isotropic etching of SiGe

The NW diameter is controllable down to 5 nm by self limited oxidation.



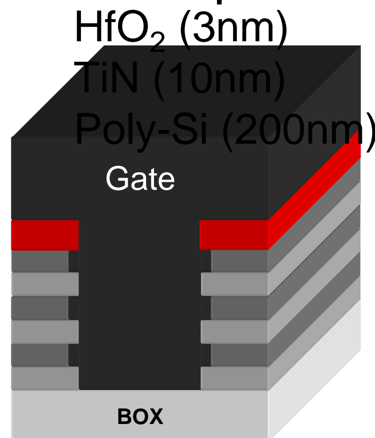


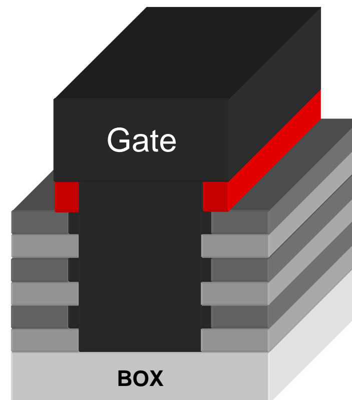


Gate depositions

HfO_2 (3nm)
TiN (10nm)
Poly-Si (200nm)

Gate etching



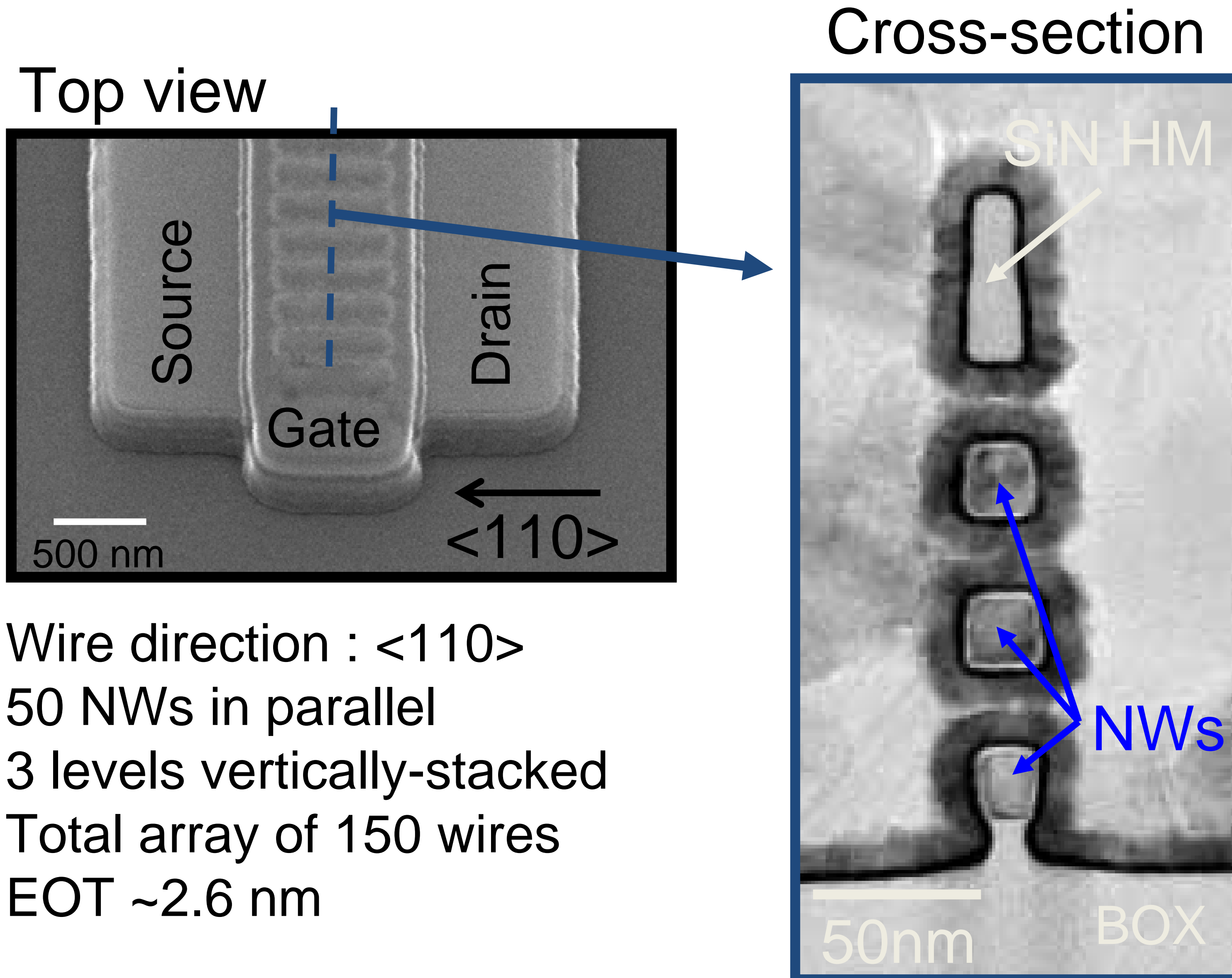


S/D implantation
Spacer formation
Activation anneal
Salicidation

Standard Back-End of-Line Process

Process Details :
C. Dupre *et al.*,
IEDM Tech. Dig., p.749, 2008

3D-stacked Si NWs with Hi-*k*/MG

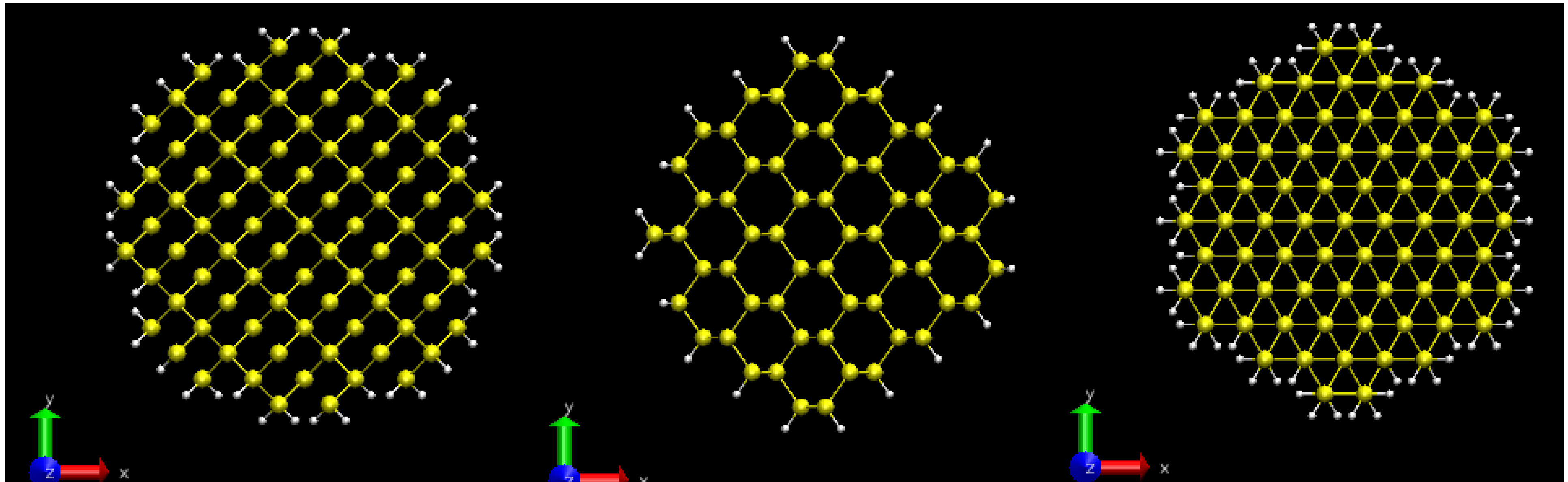


Wire direction : <110>
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT ~2.6 nm

SiNW Band structure calculation

Cross section of Si NW

First principal calculation,

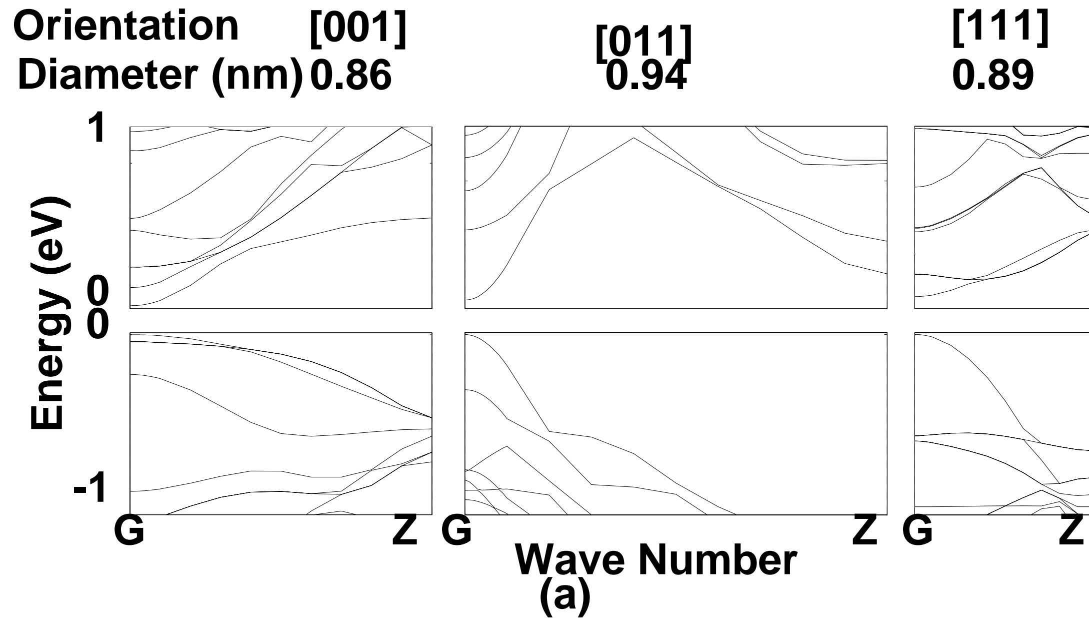


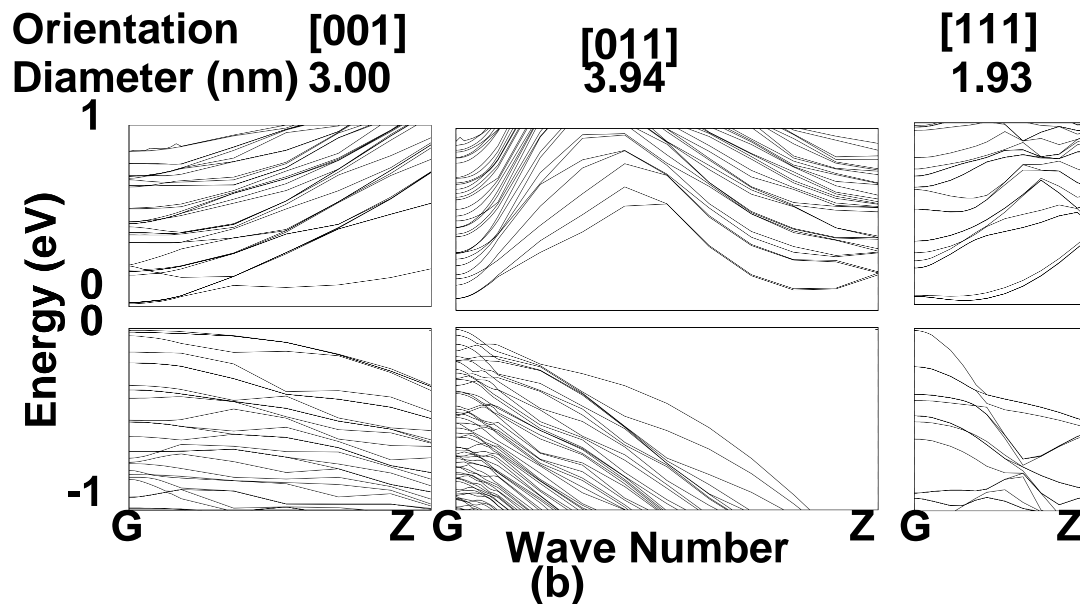
D=1.96nm [001]

D=1.94nm [011]

D=1.93nm [111]

Si nanowire FET with 1D Transport



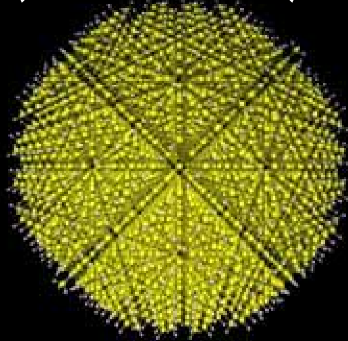


Small mass with [011]

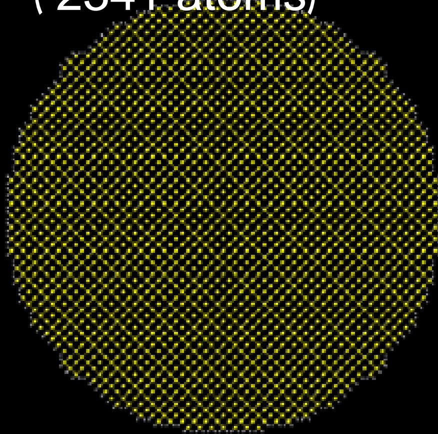
Large number of quantum channels with [001]

Atomic models of a Si quantum dot and Si nanowires

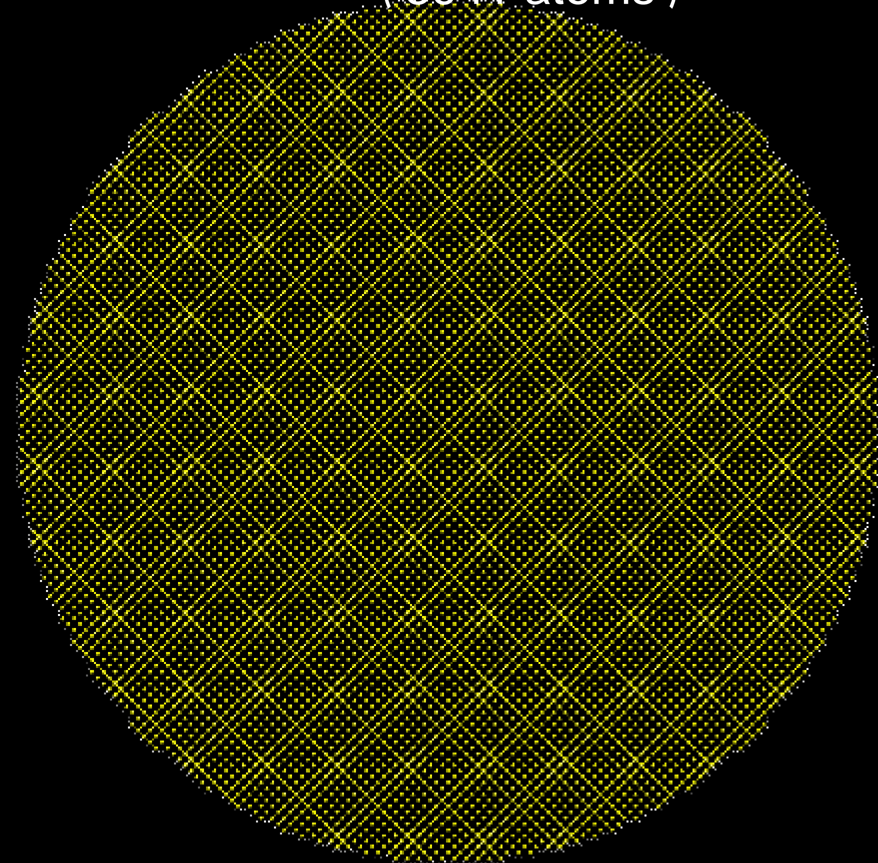
6.6 nm diameter SiQD
(8651 atoms)



10 nm diameter Si(100)NW
(2341 atoms)



20 nm diameter Si(100)NW
(8941 atoms)



RSDFT – suitable for parallel first-principles calculation -

- ✓Real-Space Finite-Difference
- ✓Sparse Matrix
- ✓FFT free (FFT is inevitable in the conventional plane-wave code)
- ✓MPI (Message Passing Interface) library

Higher-order finite difference pseudopotential method
J. R. Chelikowsky et al., Phys. Rev. B, (1994)

3D grid is divided by several regions for parallel computation.

Kohn-Sham eq. (finite-difference)

$$\left(-\frac{1}{2}\nabla^2 + v_s[\rho](\mathbf{r}) + \hat{v}_{nloc}^{PP}(\mathbf{r})\right)\phi_n(\mathbf{r}) = \varepsilon_n \phi_n(\mathbf{r})$$

Higher-order finite difference

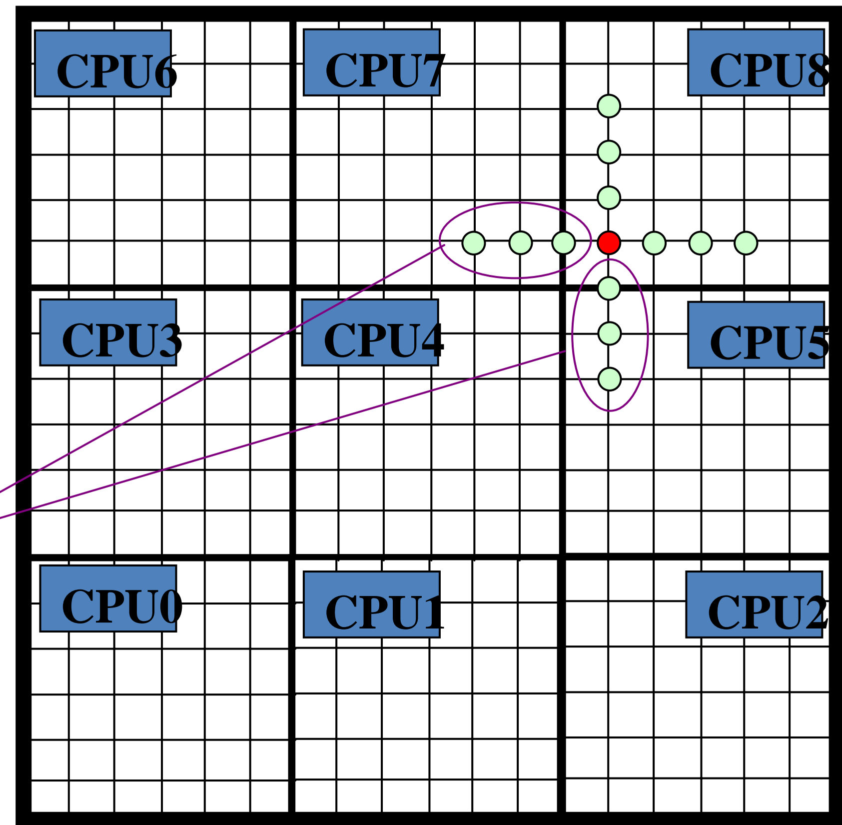
$$\frac{\partial^2}{\partial x^2}\psi_n(x,y,z) \approx \sum_{m=-6}^{6} C_m \psi_n(x+m\Delta x, y, z)$$

MPI_ISEND, MPI_IRECV

Integration

$$\int \psi_m(\mathbf{r})\psi_n(\mathbf{r})d\mathbf{r} \approx \sum_{i=1}^{Mesh} \psi_m(\mathbf{r}_i)\psi_n(\mathbf{r}_i)\Delta x \Delta y \Delta z$$

MPI_ALLREDUCE



Massively Parallel Computing

with our recently developed code "RSDFT"

Iwata et al, J. Comp. Phys., to be published

Real-Space Density-Functional Theory code (RSDFT)

Based on the finite-difference pseudopotential method (J. R. Chelikowsky et al., PRB1994)

Highly tuned for massively parallel computers

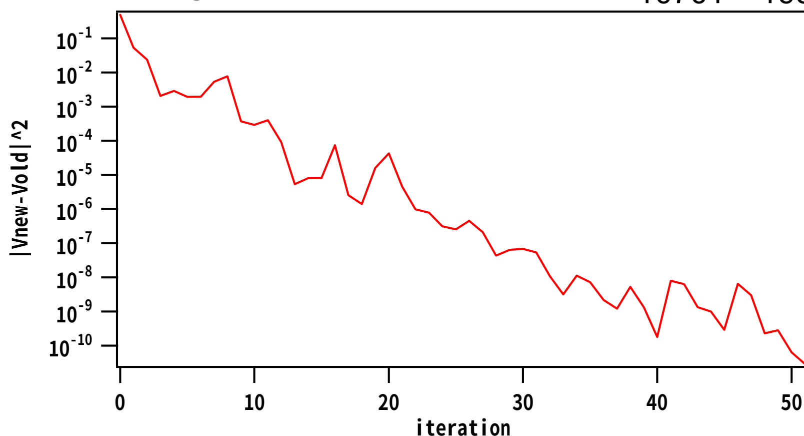
Computations are done on a massively-parallel cluster **PACS-CS** at University of Tsukuba.

(Theoretical Peak Performance = 5.6GFLOPS/node)

e.g.) The system over 10,000 atoms → $Si_{10701}H_{1996}$
(7.6 nm diameter Si dot)

Convergence behavior for $Si_{10701}H_{1996}$

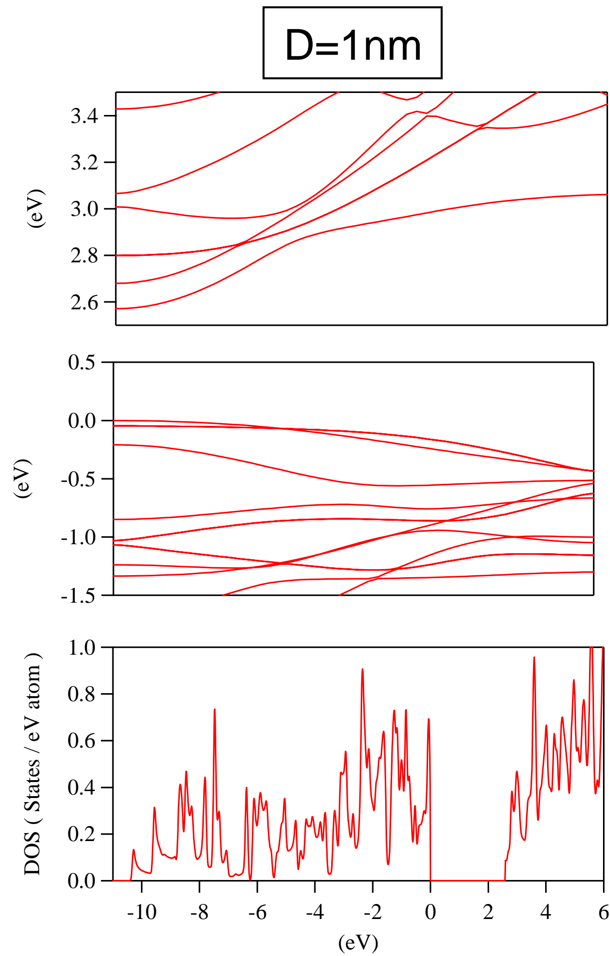
Grid points = 3,402,059
Bands = 22,432

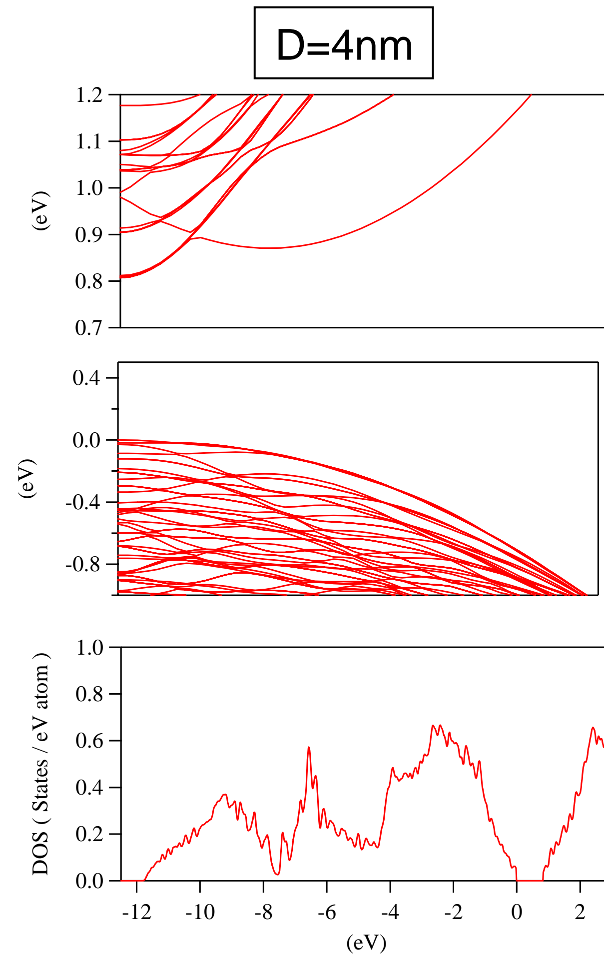


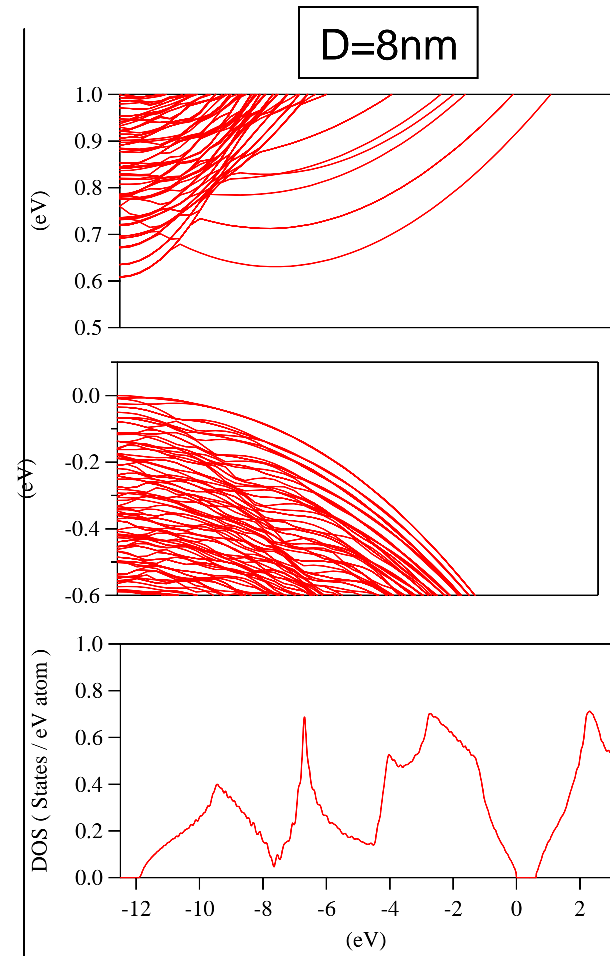
Computational Time (with 1024 nodes of PACS-CS

6781 sec. ✕ 60 iteration step = 113 hour

Band Structure and DOS of Si(100)NWs (D=1nm, 4nm, and 8nm)







D=1 nm
Si21H20 (41 atoms)
KS band gap=2.60eV

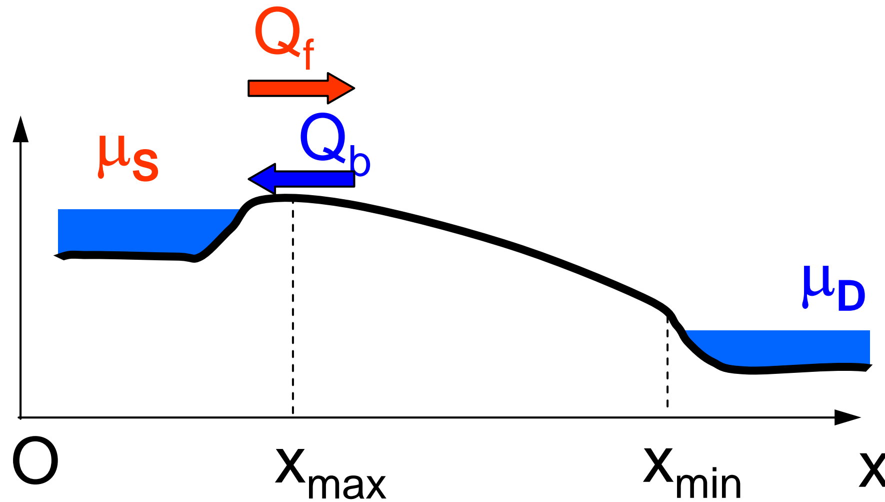
D = 4 nm
Si341H84 (425 atoms)
KS band gap = 0.81eV

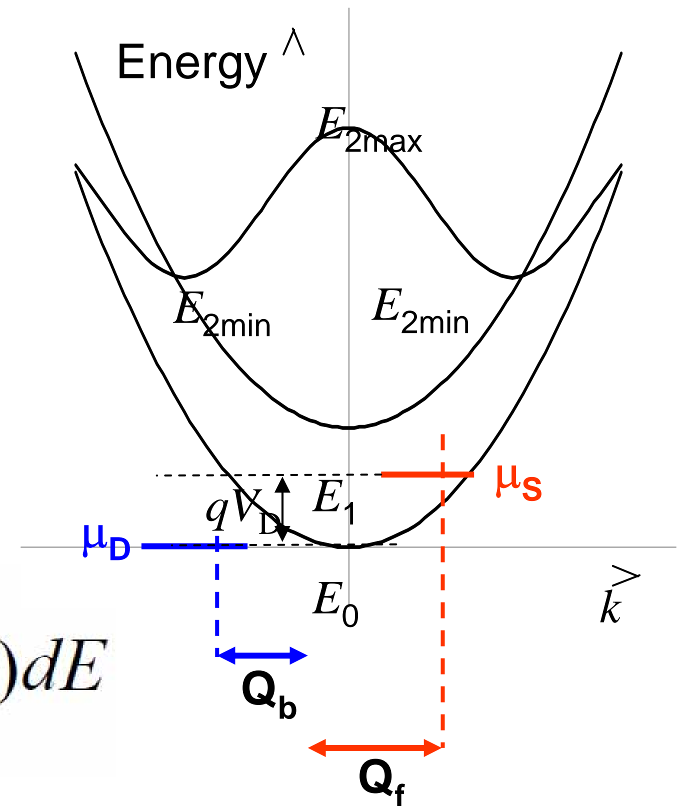
D=8 nm
Si1361H164 (1525 atoms)
KS band gap=0.61eV

KS band gap of bulk (LDA) = 0.53eV

SiNW Band compact model

Landauer Formalism for Ballistic FET



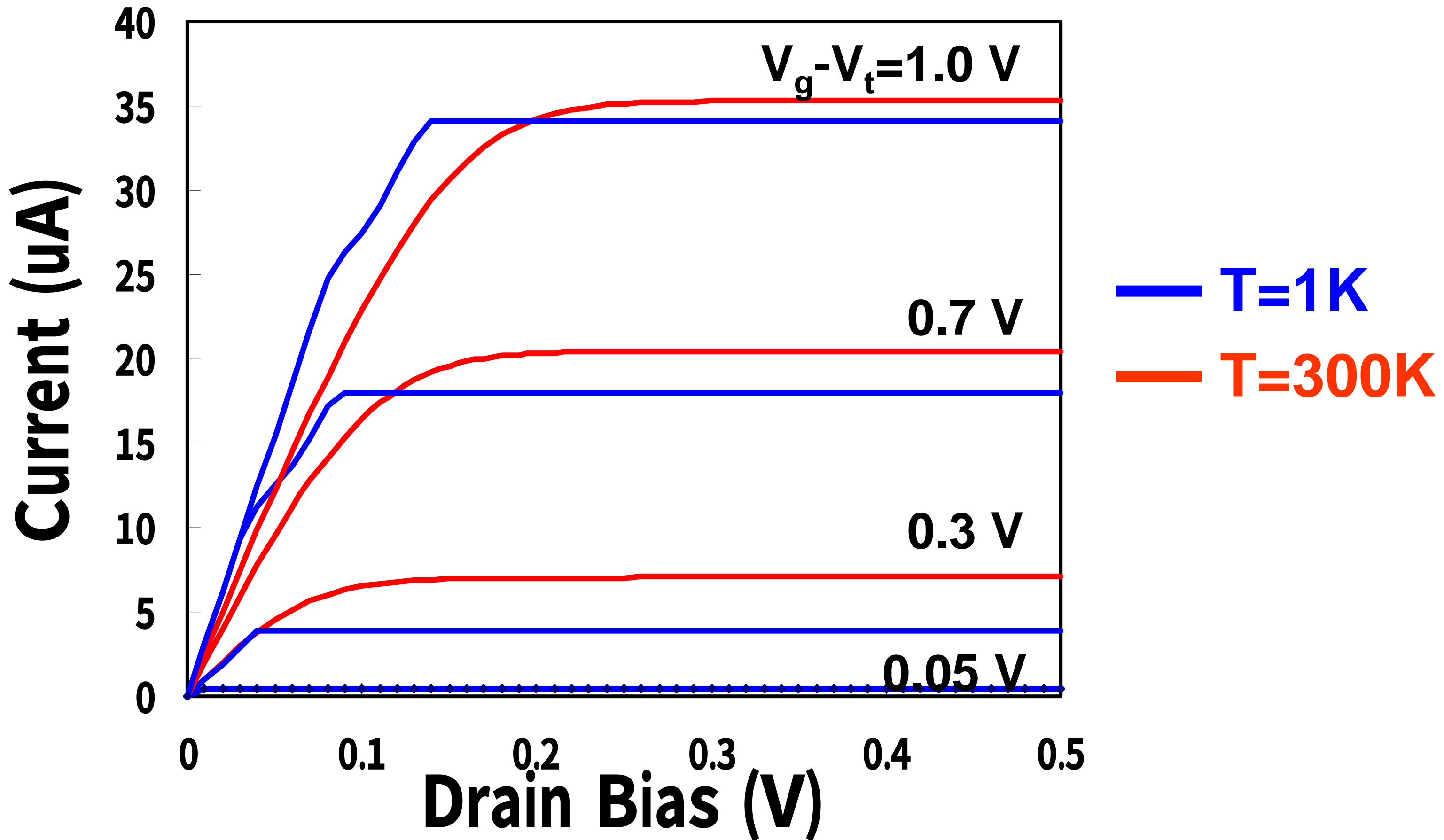


$$I_D = \frac{q}{\pi\hbar}\sum_i \int \left[f(E,\mu_S) - f(E,\mu_D)\right] T_i(E)\, dE$$

From x_{max} to x_{min} $\quad T_i(E) \approx 1$

$$I_D = G_0\left(\frac{k_B T}{q}\right)\sum_i g_i \ln\left\{\frac{1+\exp\left[(\mu_S - E_{i0})/k_B T\right]}{1+\exp\left[(\mu_D - E_{i0})/k_B T\right]}\right\}$$

IV Characteristics of Ballistic SiNW FET

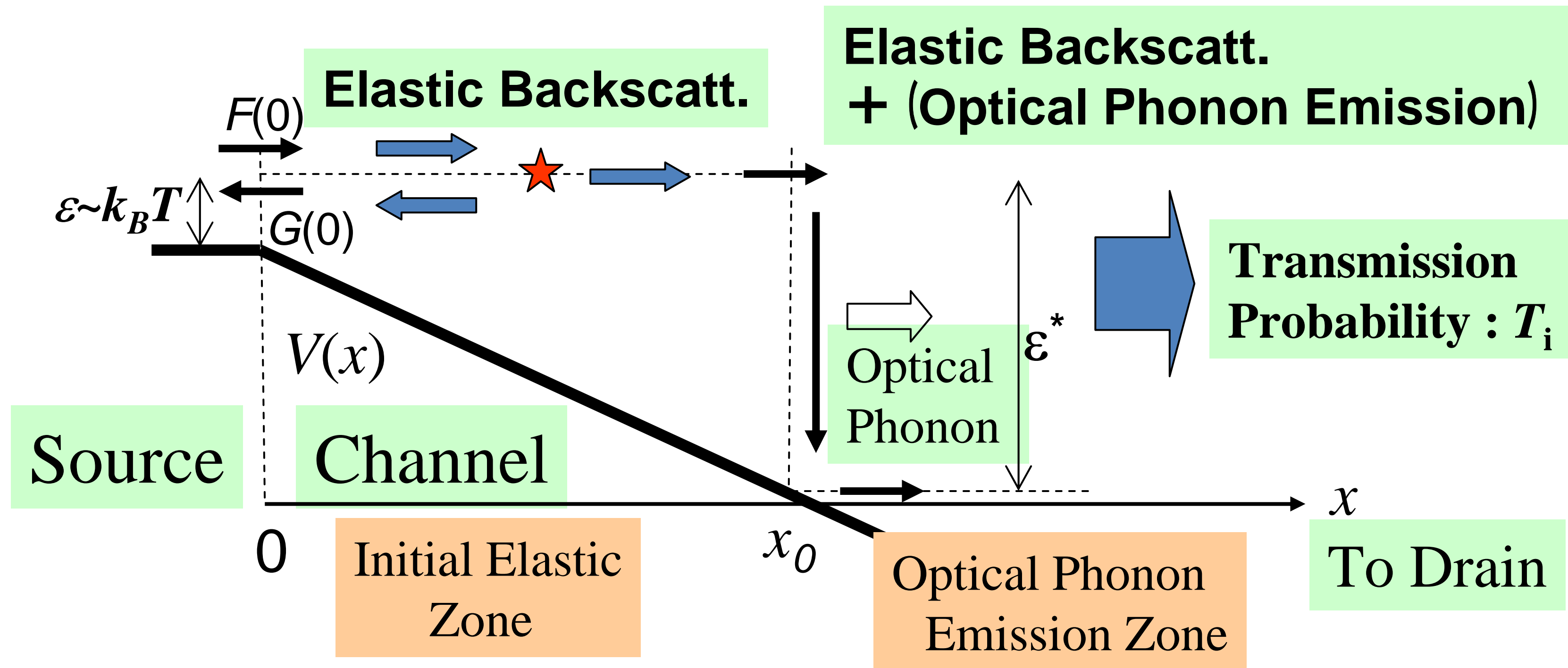


Small temperature dependency

35μA/wire for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx.：Electric Field E



Transmission Probability to Drain

$$T(\varepsilon) = \left.\frac{F(0) - G(0)}{F(0)}\right)_{\text{Injection from Drain}=0}$$

Résumé of the Compact Model

$$I = \frac{q}{\pi\hbar}\sum_i g_i \int \left[f(\varepsilon,\mu_s) - f(\varepsilon,\mu_D) \right] T_i \, d\varepsilon$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left\{ \frac{\sqrt{2r+t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r+t_{ox}} - \sqrt{t_{ox}}} \right\}}.$$

Planar Gate

$$(V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{|Q_f + Q_b|}{C_G}.$$

$$\mu_S - \mu_D = qV_D$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left(\frac{r+t_{ox}}{r} \right)}.$$

GAA

(Electrostatics requirement)

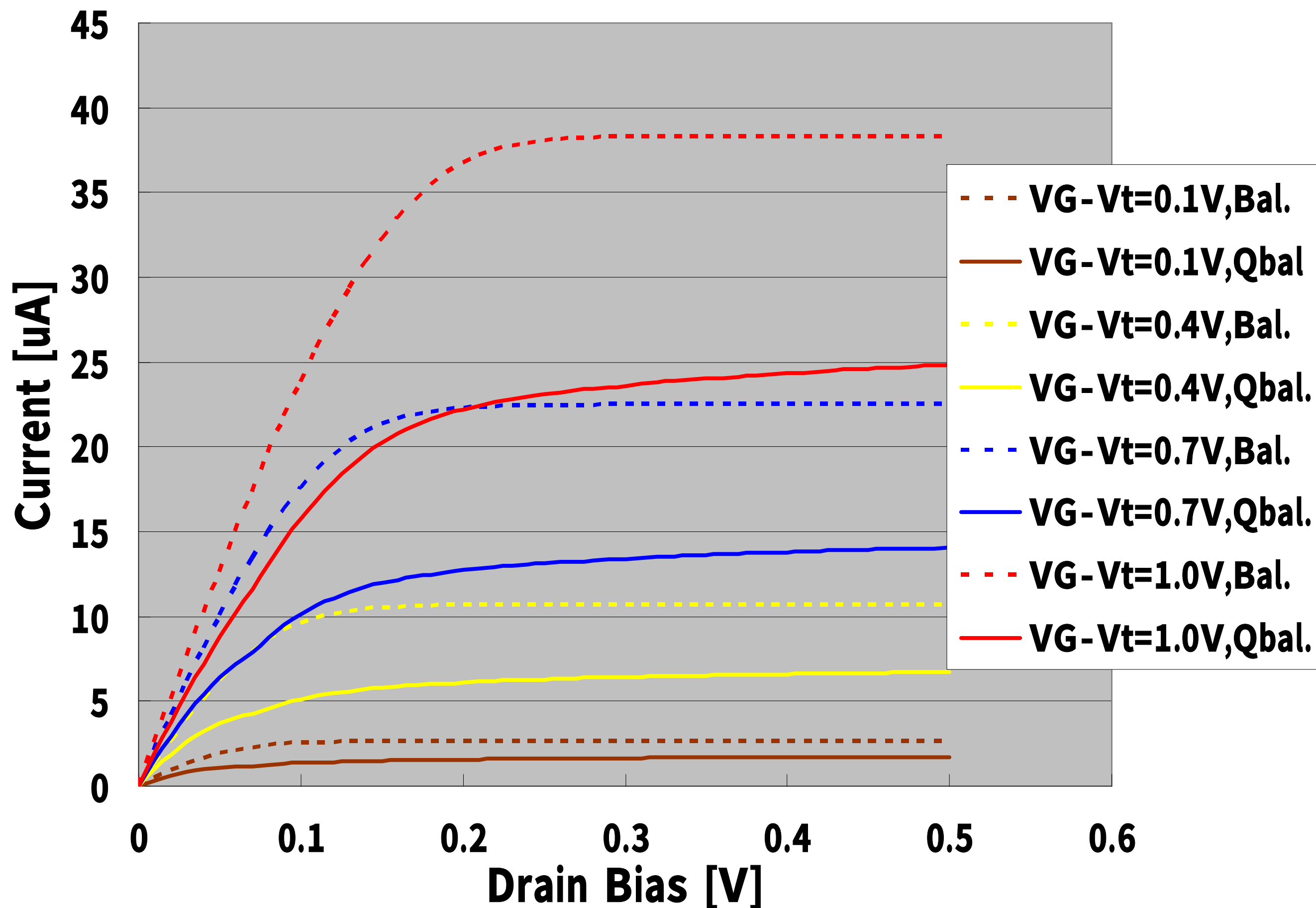
$$|Q_f + Q_b| = \frac{q}{\pi}\sum_i g_i \left[\int_{-\infty}^{\infty} \frac{dk}{1+\exp\left\{ \frac{\varepsilon_i(k)-\mu_S}{k_B T} \right\}} - \int_{-\infty}^{0} \left\{ \frac{1}{1+\exp\left\{ \frac{\varepsilon_i(k)-\mu_S}{k_B T} \right\}} - \frac{1}{1+\exp\left\{ \frac{\varepsilon_i(k)-\mu_D}{k_B T} \right\}} \right\} T_i(\varepsilon_i(k))dk \right]$$

$$T(\varepsilon) = \frac{\sqrt{2D_0}\, qE}{\left(\sqrt{B_0+D_0} + \sqrt{D_0}\right) qE + \sqrt{2mD_0}\, B_0 \ln\left(\frac{qEx_0 + \varepsilon}{\varepsilon} \right)}$$

(Carrier distribution in Subbands)

Unknowns are I_D, $(\mu_S - \mu_0)$, $(\mu_D - \mu_0)$, $(Q_f + Q_b)$

I-V_D Characteritics (RT)



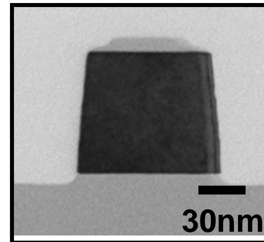
- Electric current 20～25 μA
- No satruration at Large V_D

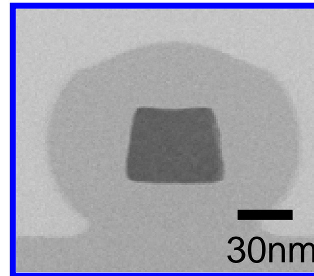
SiNW FET Fabrication

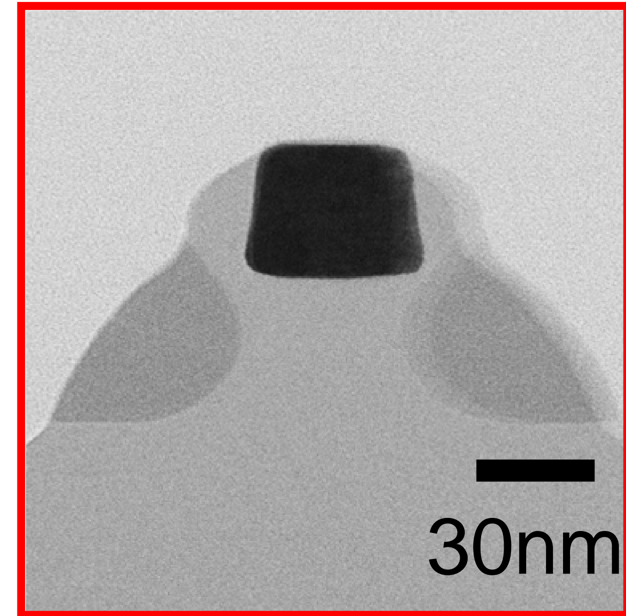
SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oixde etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

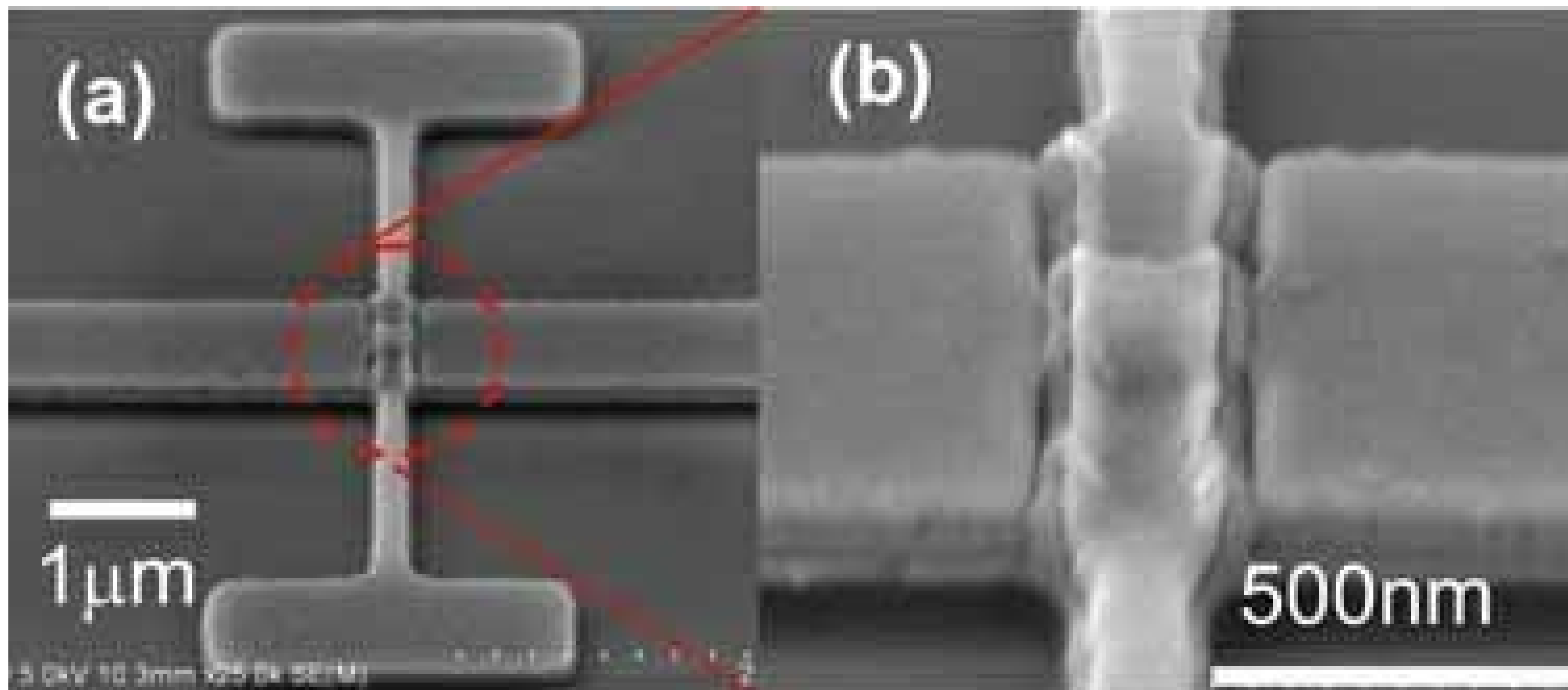
Standard recipe for gate stack formation





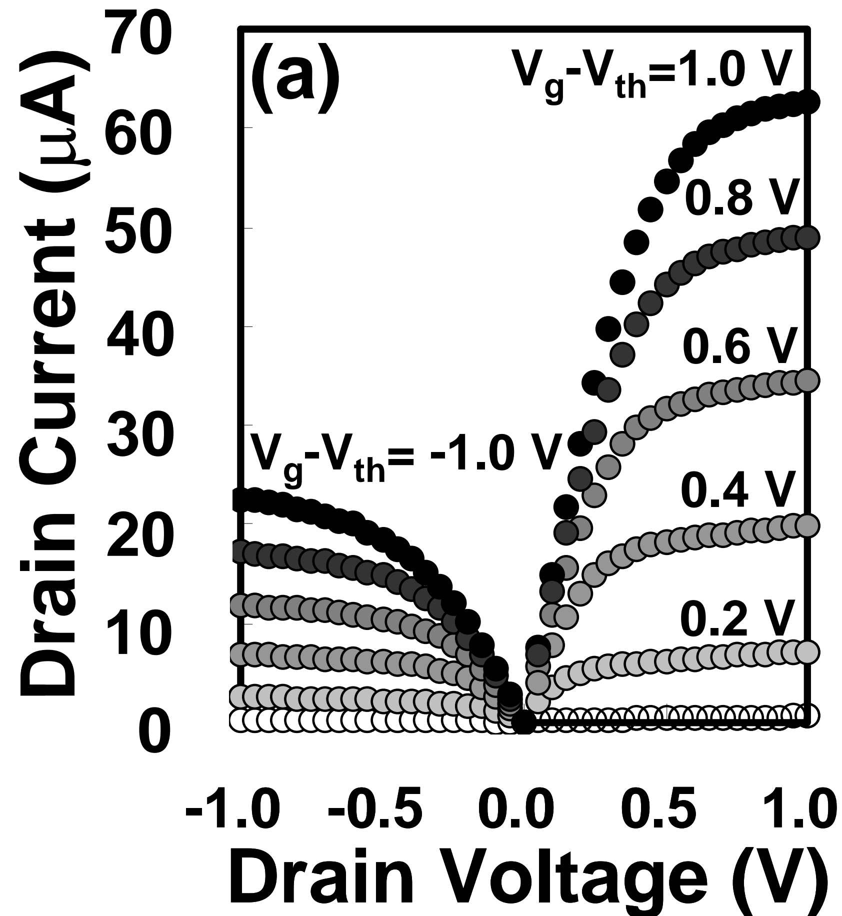


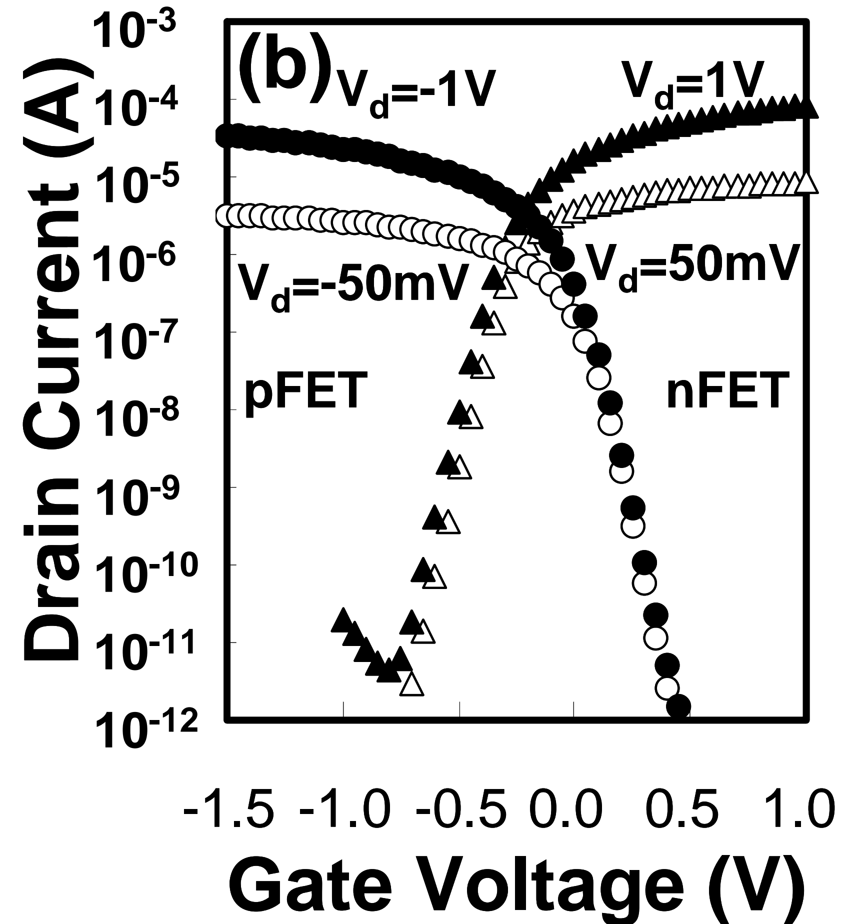
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.



Recent results to be presented by ESSDERC 2010 next week in Sevile

Wire cross-section: 20 nm X 10 nm

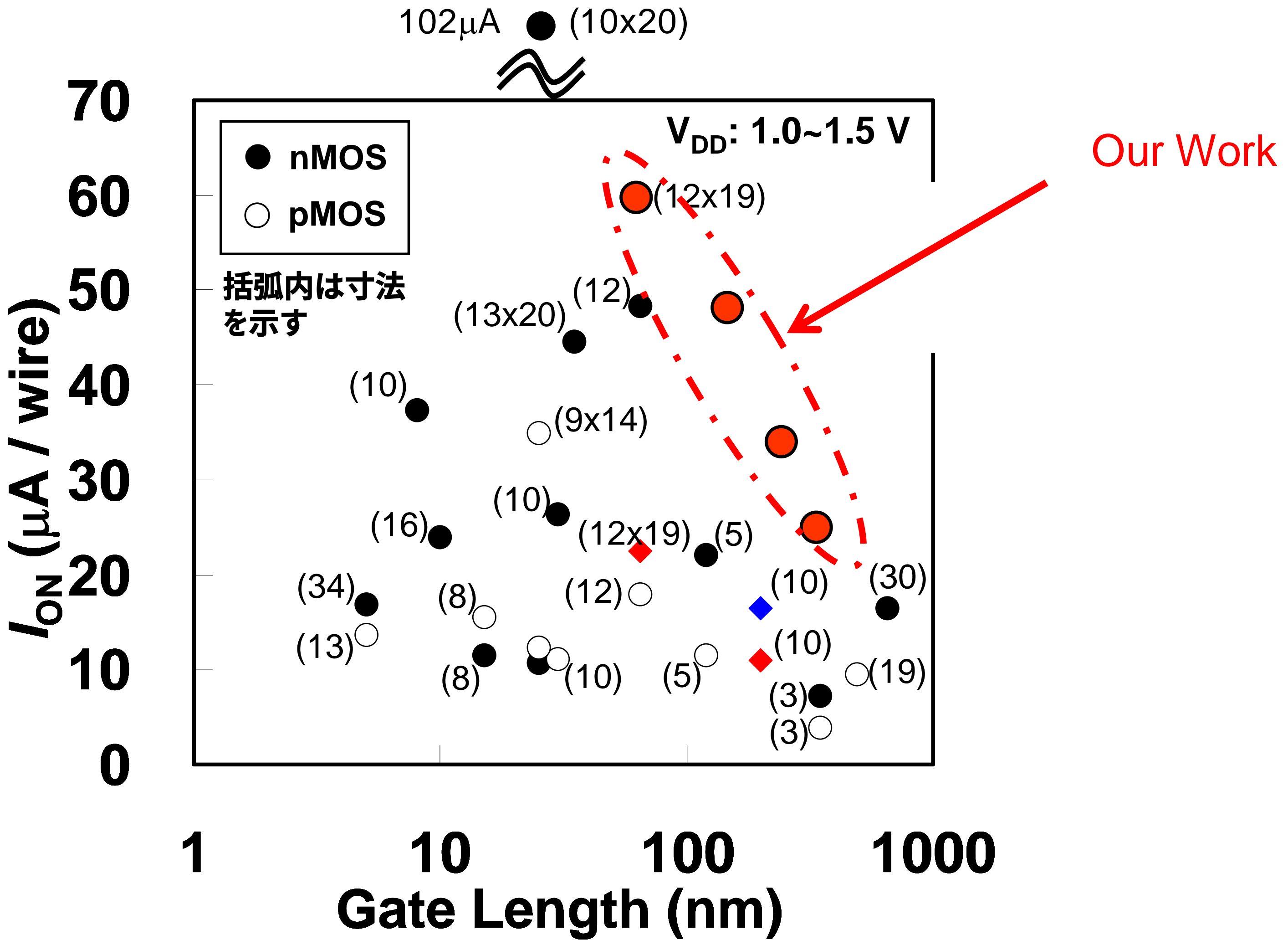




On/Off>10^6、60uA/wire

L_g=65nm, T_{ox}=3nm

Bench Mark



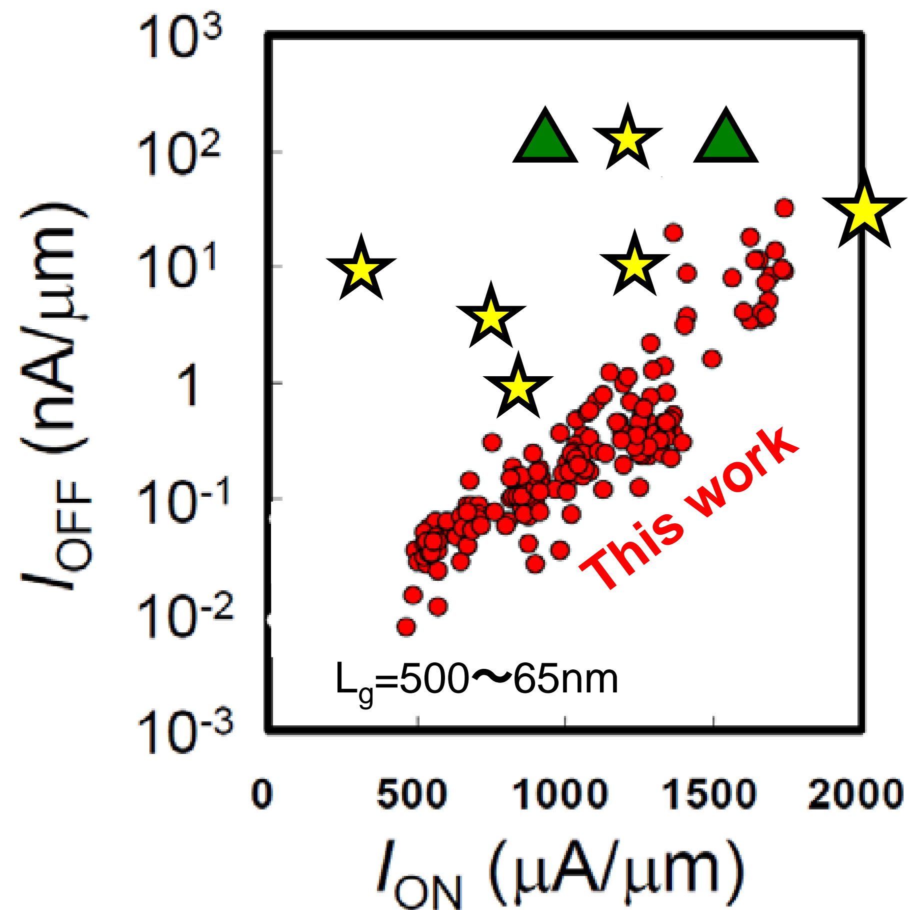
Bench Mark

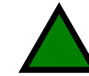
	This work	Ref[11]	Ref[12]	Ref[13]	Ref[14]	Ref[15]	Ref[4]
NW Cross-section (nm)	Rect.	Rect.	Rect.	Cir.	Cir.	Elliptical	Elliptical
NW Size (nm)	10x20	10x20	14	10	10	12	13x20
Lg (nm)	65	25	100	30	8	65	35
EOT or Tox (nm)	3	1.8	1.8	2	4	3	1.5
Vdd (V)	1.0	1.1	1.2	1.0	1.2	1.2	1.0
Ion(uA) per wire	60.1	102	30.3	26.4	37.4	48.4	43.8
Ion(uA/um) by dia.	3117	5010	2170	2640	3740	4030	2592
Ion(uA/um) by cir.	1609	2054	430	841	1191	1283	825
SS (mV/dec.)	70	79	68	71	75	~75	85
DIBL (mV/V)	62	56	15	13	22	40-82	65
Ion/Ioff	~1E6	>1E6	>1E5	~1E6	>1E7	>1E7	~2E5

Ref[11] by Stmicro Lg=25nm,Tox=1.8nm

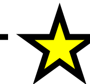
This work Lg=65nm,Tox=3nm

I_{ON}/I_{OFF} Bench mark

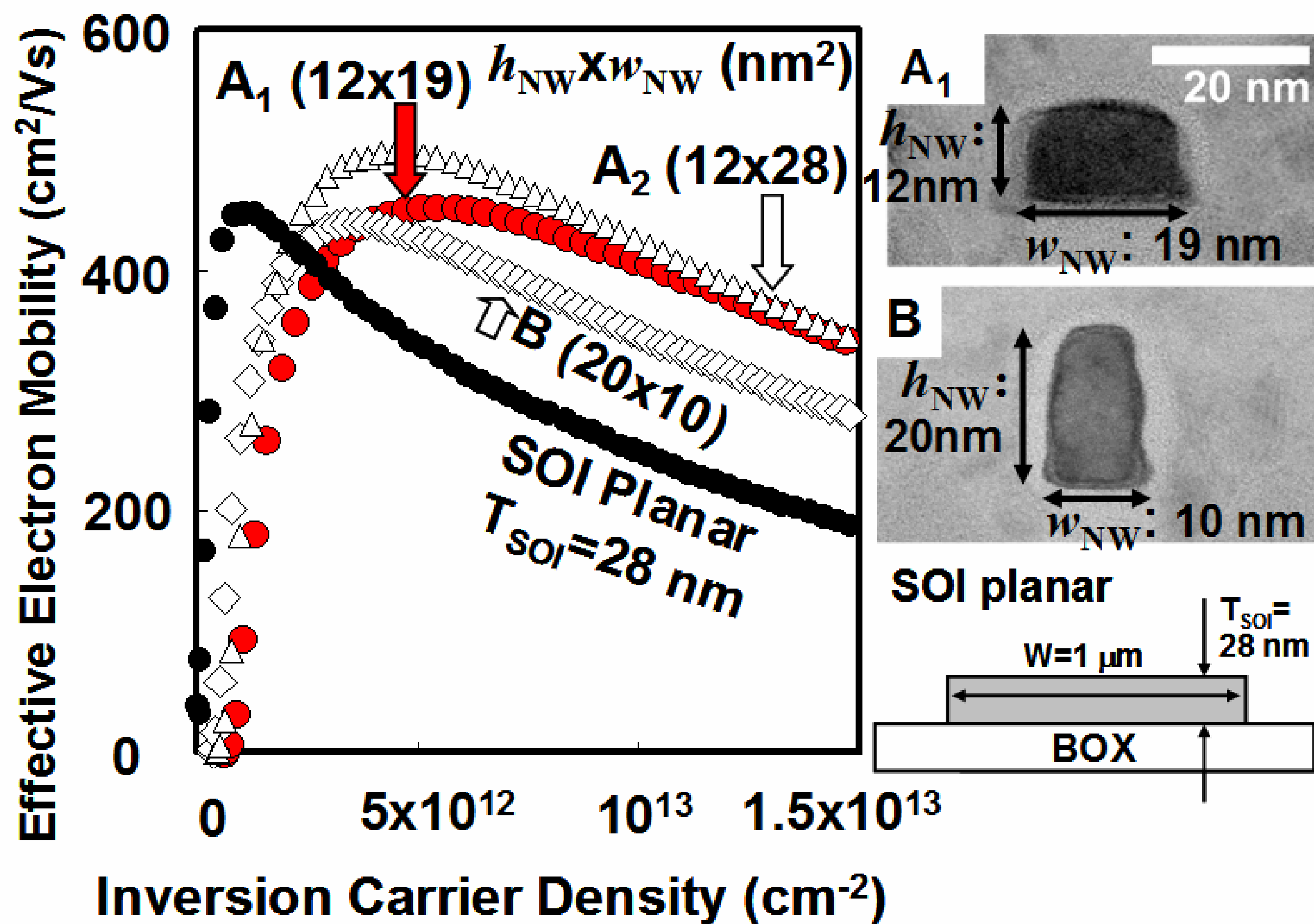


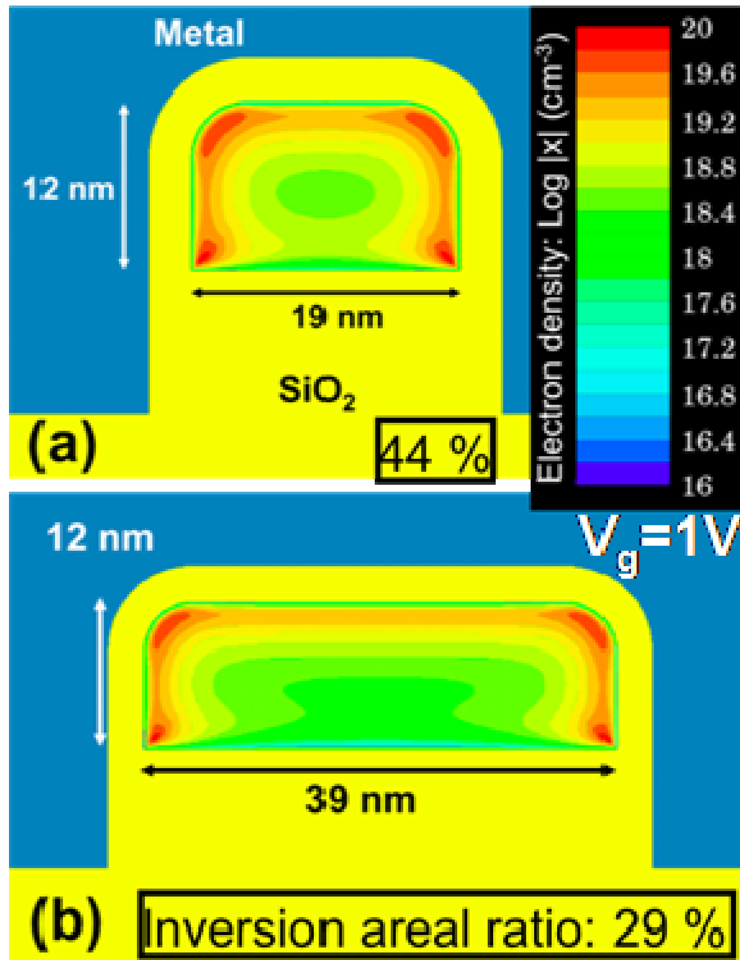
Planer FET  1.0〜1.1V

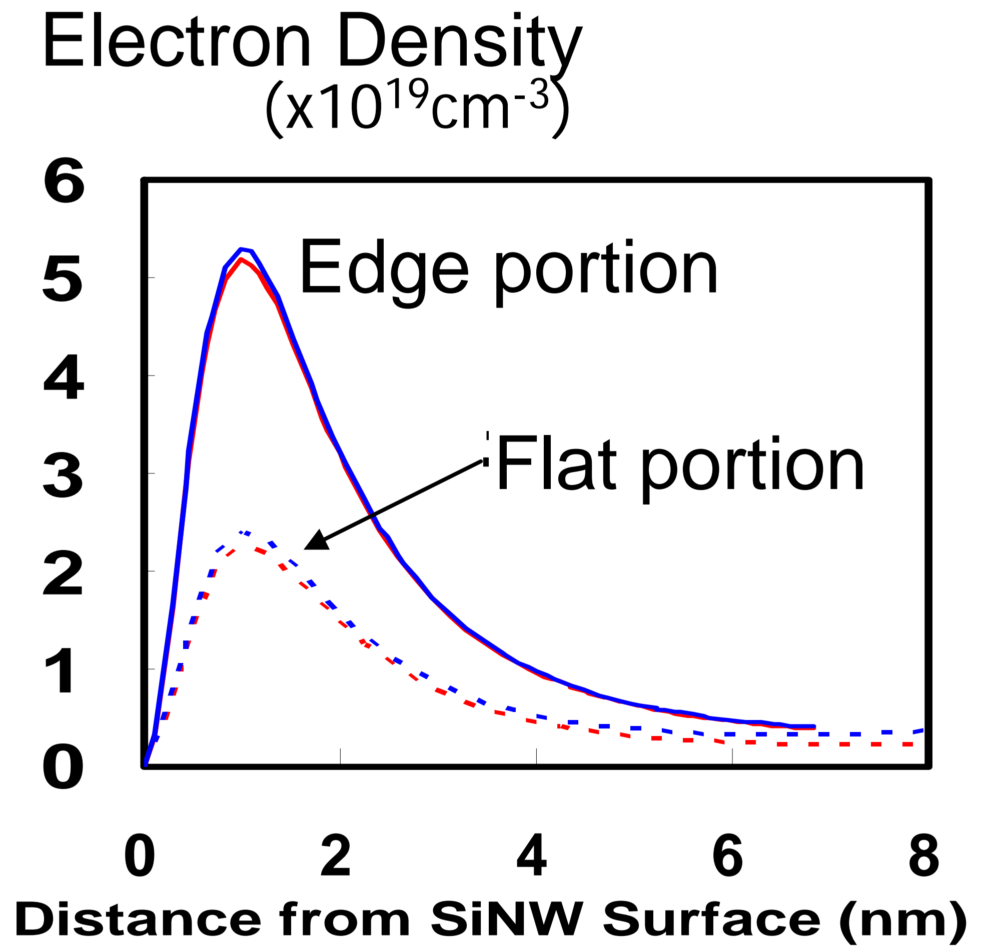
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

SiナノワイヤFET  1.2〜1.3V

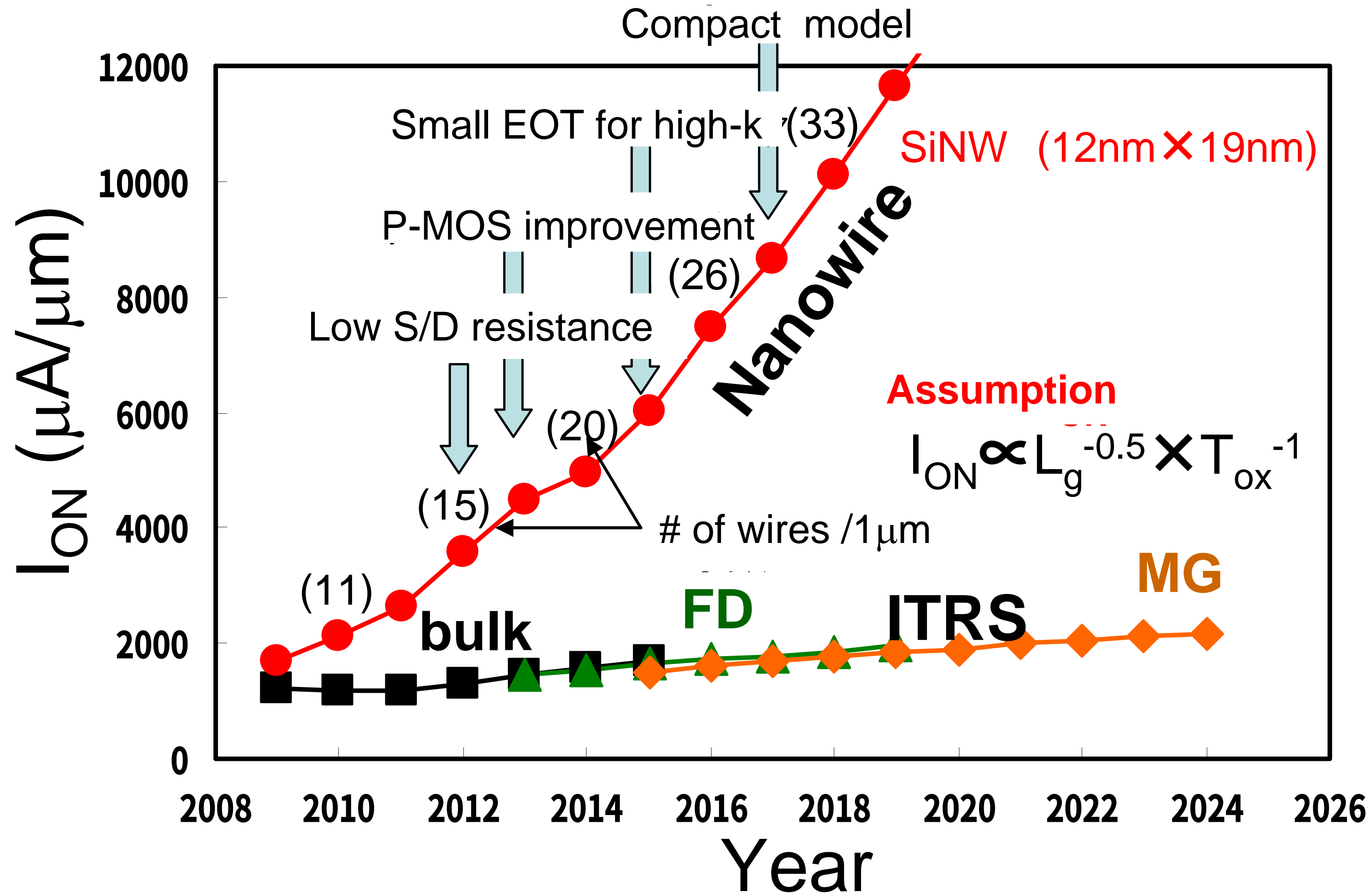
Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240

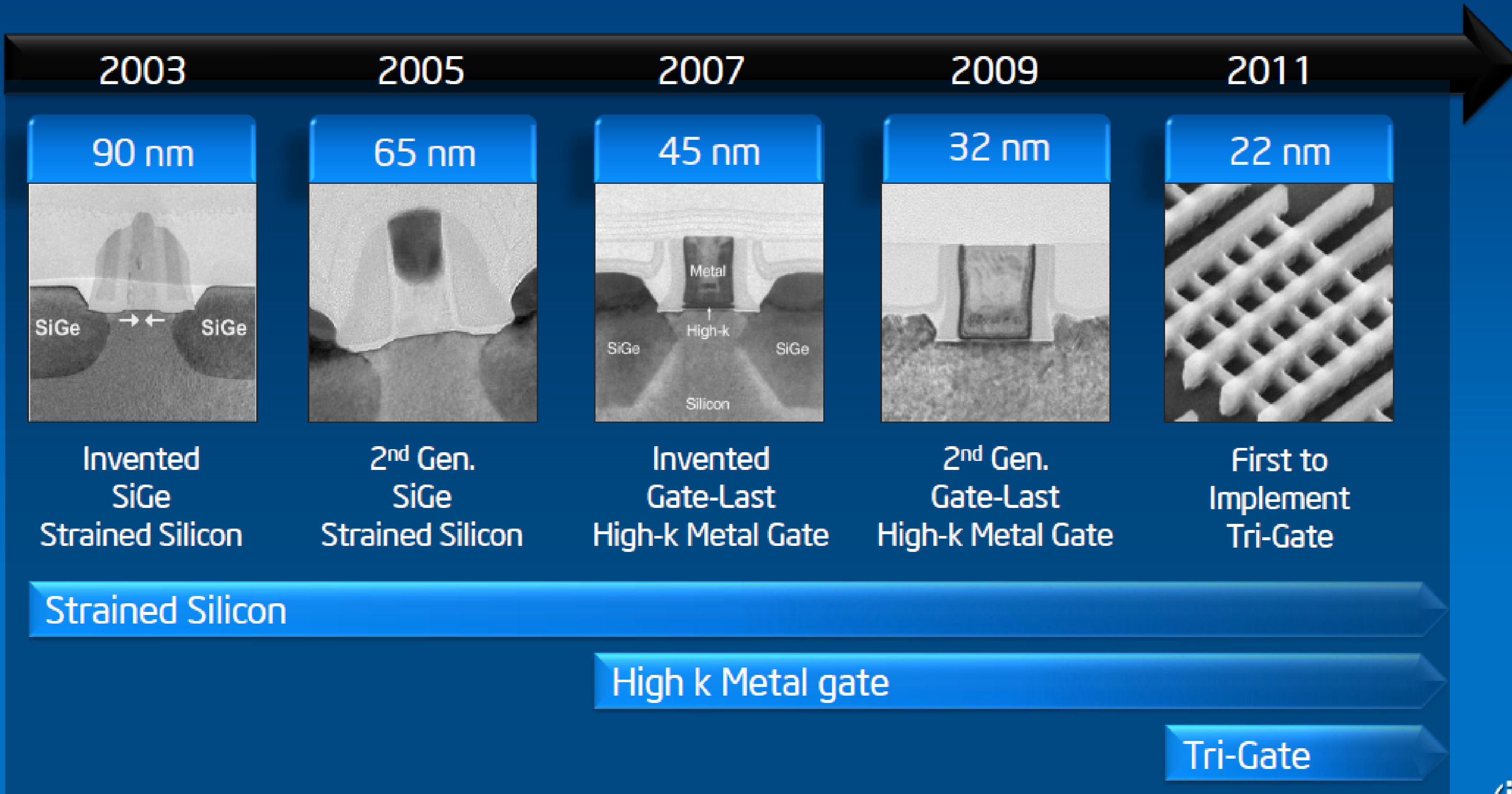

Effective Electron Mobility (cm2/Vs)
600
400
200
0
0
5x1012
1013
1.5x1013
Inversion Carrier Density (cm-2)
A1 (12x19)
hNWxwNW (nm2)
A2 (12x28)
B (20x10)
SOI Planar
TSOI=28 nm
A1
20 nm
hNW: 12nm
wNW: 19 nm
B
hNW: 20nm
wNW: 10 nm
SOI planar
TSOI= 28 nm
W=1 μm
BOX


Metal
12 nm
19 nm
SiO2
(a)
44 %
Electron density: Log |x| (cm-3)
20
19.6
19.2
18.8
18.4
18
17.6
17.2
16.8
16.4
16
Vg=1V
12 nm
39 nm
(b)
Inversion areal ratio: 29 %

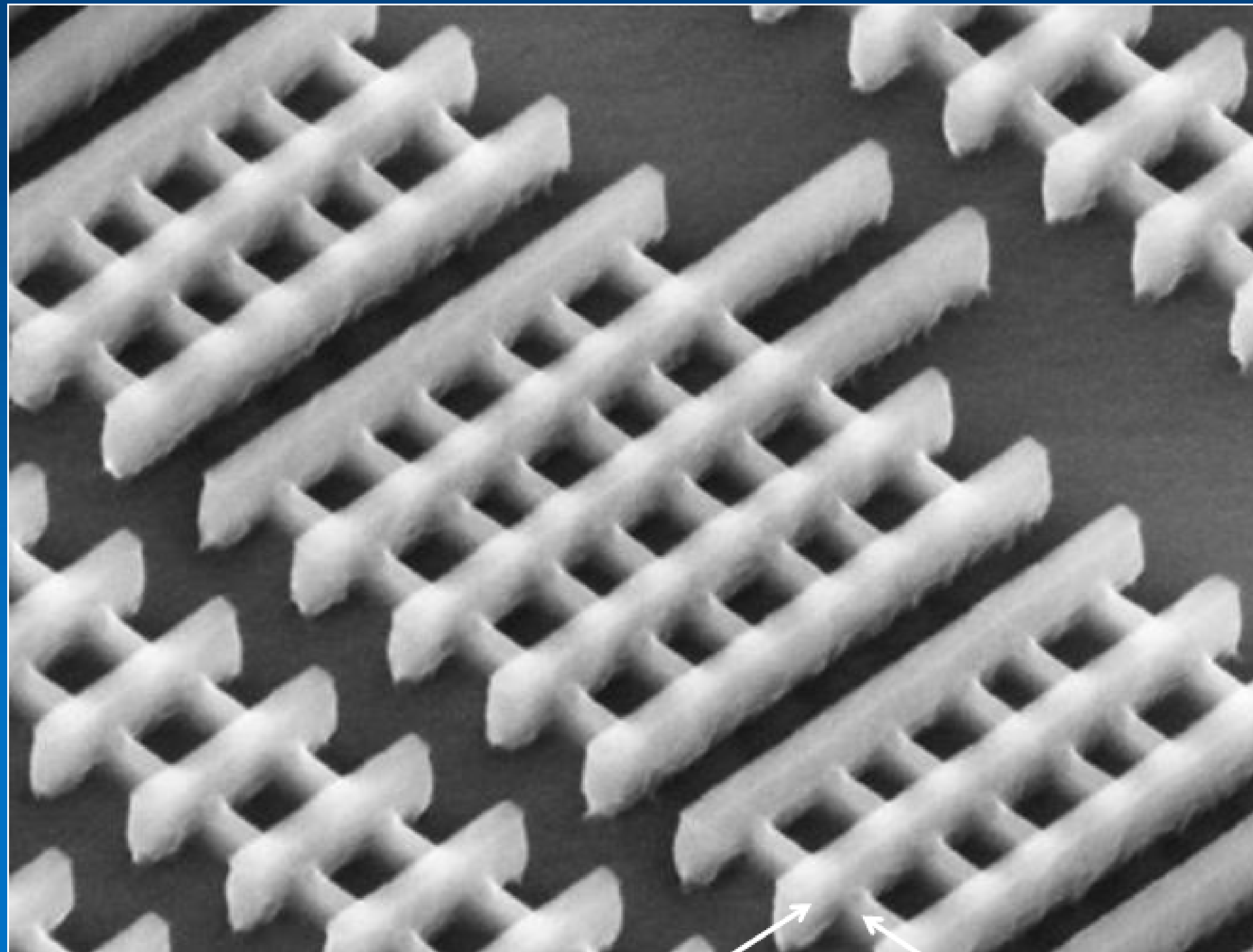

Electron Density
(x10^19cm-3)
6
5
4
3
2
1
0
Edge portion
Flat portion
0
2
4
6
8
Distance from SiNW Surface (nm)

Primitive estimation !

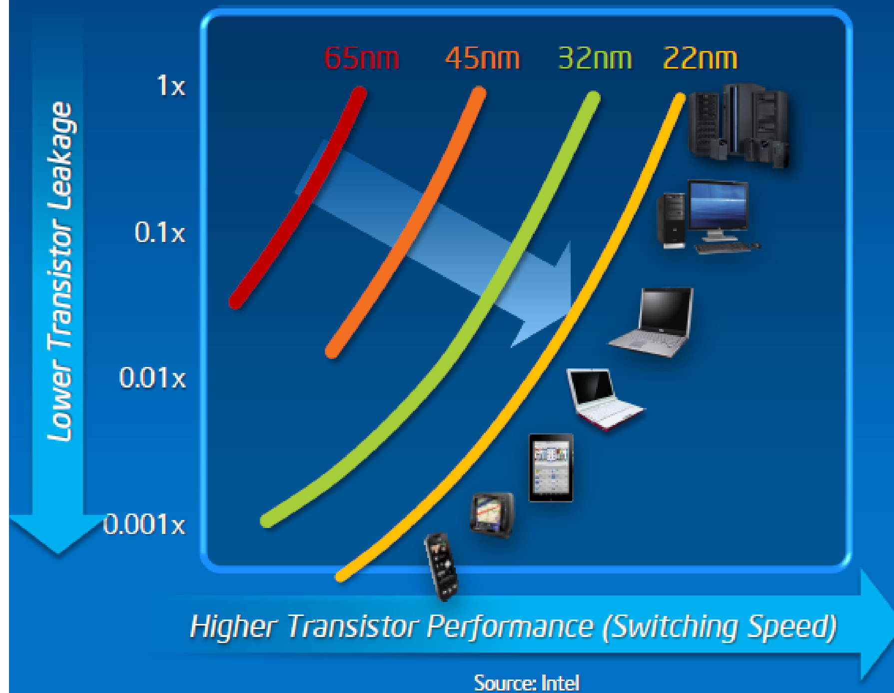



Transistor Innovations Enable Technology Cadence
2003
2005
2007
2009
2011
90 nm
65 nm
45 nm
32 nm
22 nm
SiGe
SiGe
Metal
High-k
SiGe
SiGe
Silicon
Invented
SiGe
Strained Silicon
2nd Gen.
SiGe
Strained Silicon
Invented
Gate-Last
High-k Metal Gate
2nd Gen.
Gate-Last
High-k Metal Gate
First to
Implement
Tri-Gate
Strained Silicon
High k Metal gate
Tri-Gate
intel

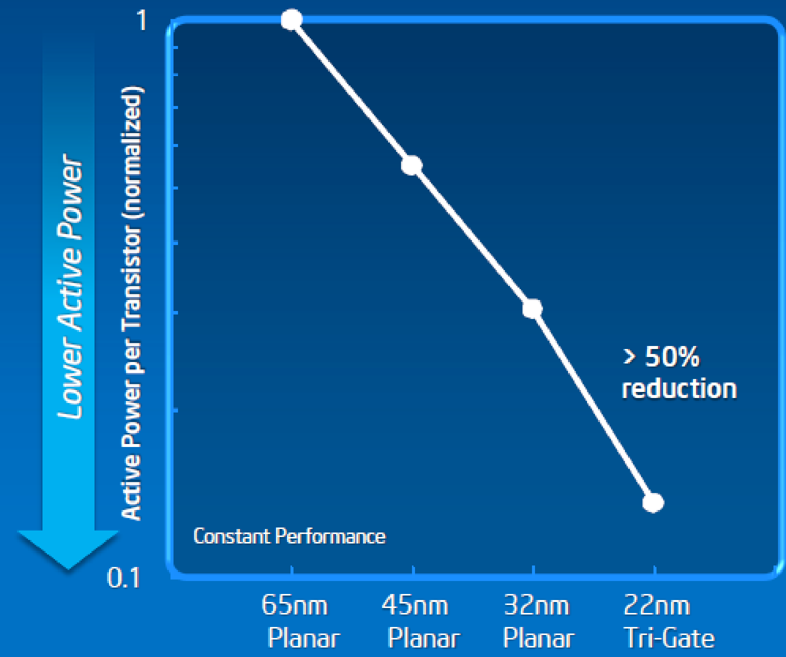
22 nm 3-D Tri-Gate Transistor



Energy-Efficient Performance Built on Moore's Law



Source: Intel

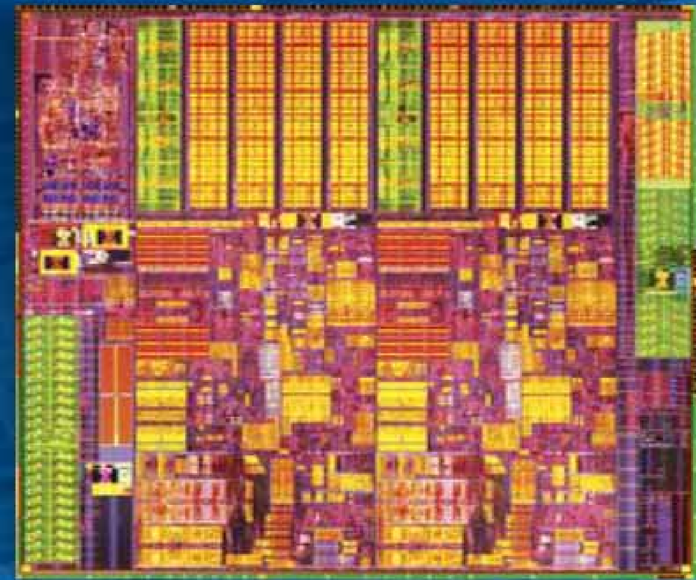


22 nm Tri-Gate transistors increase the benefit from a new technology generation

22nm Silicon Technology Breakthrough Benefits Broad Range of Intel Architecture Devices

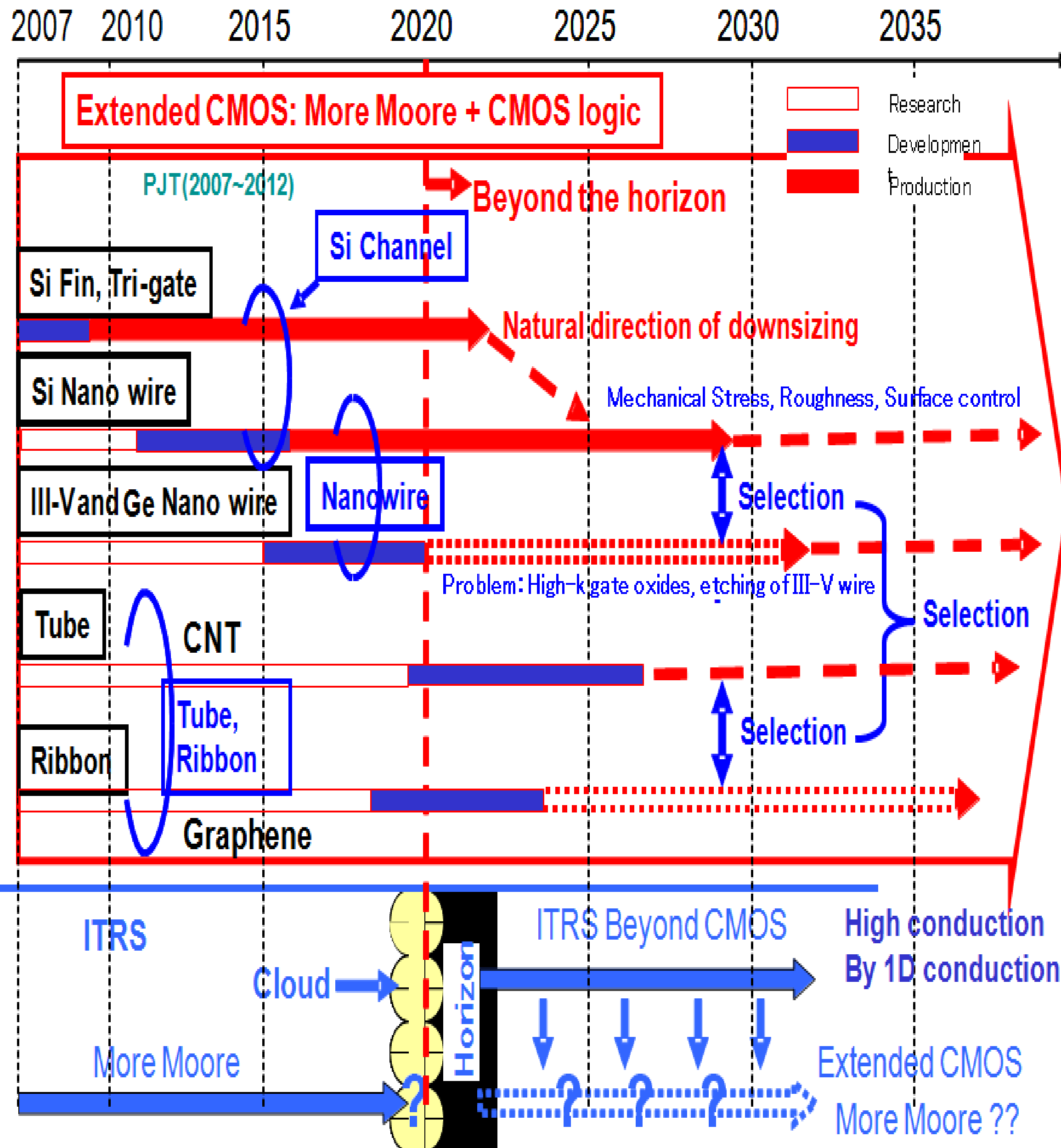
New 22nm 3-D transistors deliver unprecedented performance improvement and power reduction for Intel's product portfolio

- This benefits smallest handhelds to powerful cloud-based servers
- 37% performance increase at low voltage vs. 32nm planar transistors*
- Consumes only half the power at the same performance level as 2-D transistors on 32nm planar chips*



Our roadmap for R &D

Source: H. Iwai, IWJT 2008



Current Issues

Si Nanowire

Control of wire surface property
Source Drain contact
Optimization of wire diameter
Compact I-V model

III-V & Ge Nanowire

High-k gate insulator
Wire formation technique

CNT:

Growth and integration of CNT
Width and Chirality control
Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique
Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

Thank you
for your attention!