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Si nanowire FET and its modeling

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Abstract Because of its ability to effectively suppress off-leakage current with its gate-around configuration, the Si nanowire FET is considered to be the ultimate structure for ultra-small CMOS devices to the extent that the devices would be approaching their downsized limits. Recently, several experimental studies of Si nanowire FETs with on-currents much larger than those of planar MOSFETs have been published. Consequently, Si nanowire FETs are now gaining significant attention as the most promising candidate for mainstream CMOS devices in the 2020s. To enable the introduction of the Si nanowire FETs into integrated circuits, good compact models, which circuit designers can easily handle, are essential. However, it is a very challenging task to establish such a compact model, because the $I_{\rm D} - V_{\rm D}$ characteristics of Si nanowire FETs are affected by the band structure of the nanowire, which is very sensitive to the nanowire diameter, cross-sectional shape, crystal orientation, mechanical stress and interface states. In this paper, the recent status of research on Si nanowire FETs in experimental and theoretical studies is described.

Keywords Si nanowire, MOSFET, modeling

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1 Introduction

Three-dimensional Si nanowire structures provide us with many possibilities for new applications such as transistors, memories, sensors, light-emitting diodes and photovoltaic cells. In particular, Si nanowire FETs are now attracting significant attention. Because of its natural ability to effectively suppress the off-leakage current with its gate-around configuration, the Si nanowire FET is considered to be the ultimate structure for ultra-small CMOS devices to the extent that the devices would be approaching their downsized limits [1]. Recently, several high-performance experimental studies of Si nanowire FETs with an on-current much larger than that of planar MOSFETs have been published [2–10], and consequently, the Si nanowire FET is now regarded as the most promising candidate for mainstream CMOS devices in the 2020s. In fact, according to ITRS 2009, planar MOSFETs are predicted to disappear from advanced MOSFET structures, and 3D multiple gate (or Fin type) structures will be introduced because of their

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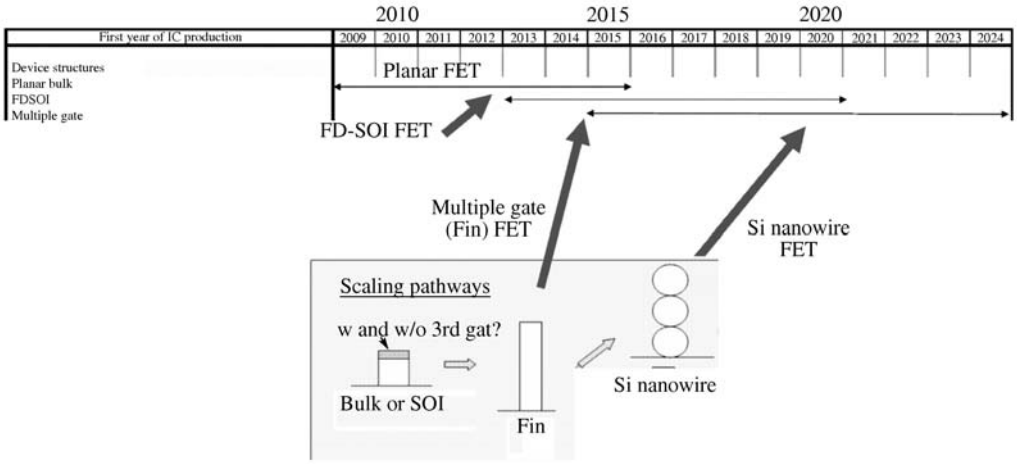

Figure 1 MOSFET structure trend in ITRS 2009.

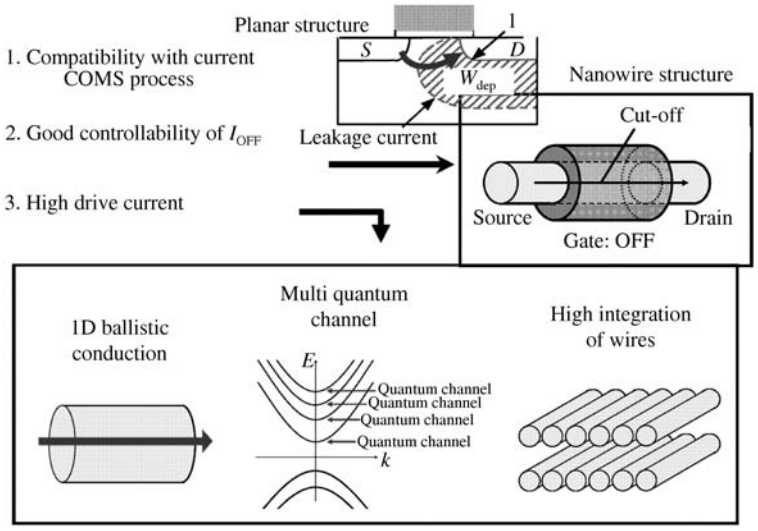

Figure 2 Advantages of Si nanowire FETs over planar.

ability to easily suppress the short-channel effects (SCE) as shown in Figure 1 [11]. It is inevitable that FinFETs will change to nanowire FETs, because of their greater control of SCE and larger channel area for the nanowire surface per unit area, also shown in the figure. Considering the introduction of Si nanowire FETs in integrated circuits, good compact models which circuit designers can easily handle in the design of integrated circuit are essential. Additional factors to many technological developments include reducing variations in the nanowire diameter, optimizing the nanowire strain and surface properties for higher conduction, decreasing the resistance using metal/silicide source drain technology and realizing the abrupt junction without dopant diffusion into the channel. Furthermore, it is a challenging task to establish a compact model, because the $I_{\rm D} - V_{\rm D}$ characteristics of the Si nanowire FETs are affected by the band structure, which is very sensitive to the nanowire diameter, cross-sectional shape, crystal orientation, mechanical stress and interface states. In this paper, the recent status of research on Si nanowire FETs in experimental and theoretical studies is described.

2 Si nanowire FET advantages

The Si nanowire FET has several advantages as a candidate for main stream CMOS devices in the 2020s as shown in Figure 2 [1].

The ability to suppress the SCE, and thus the suppression of off-leakage current in Si nanowire FETs, is expected to be very good because of the gate-surround configuration.

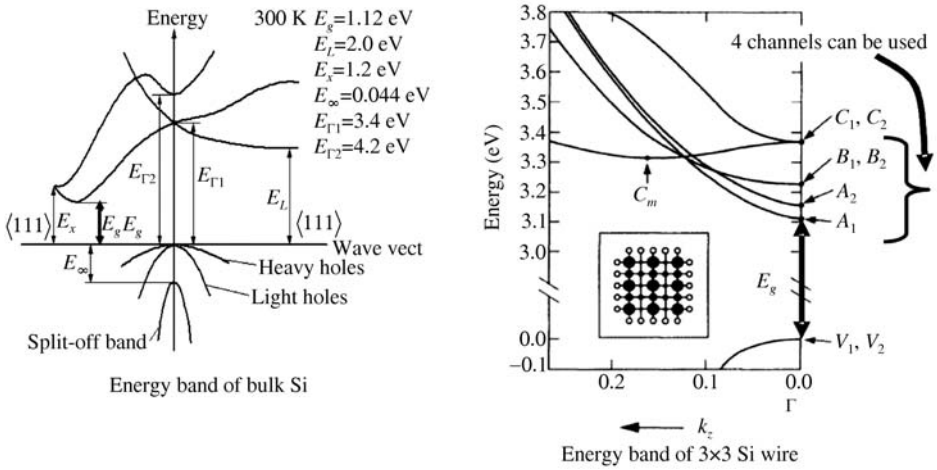

Figure 3 Band structures for Si bulk (left) and nanowire (right).

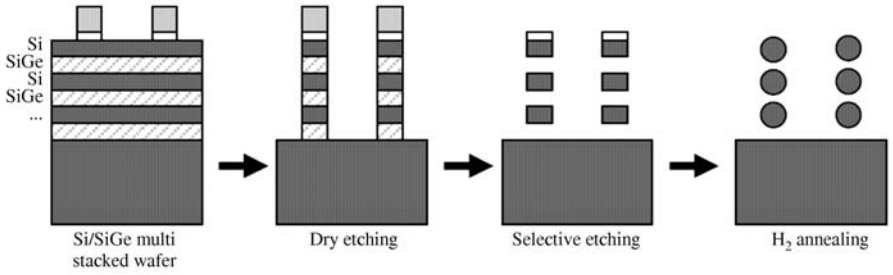

Figure 4 Fabrication of multilayer nanowire.

In addition Si nanowire FETs are expected to have high on-currents for three reasons. The first is the nature of quasi one-dimensional ballistic conduction of thin nanowires with restricted freedom for the carrier scattering angle [12]. Because of this restricted freedom for carrier scattering, its conduction will be high. The second is the use of multi-quantum channels for conduction. The band structures of Si nanowires are quite different from those of bulk Si conductors and many conduction sub-bands appear near the lowest sub-band [13] as shown in Figure 3. These sub-bands contribute to the conduction as the gate voltage increases.

The third is that multilayered nanowires can be implemented easily using Si/Ge multi-layers [3, 4, 6, 9] as shown in Figure 4. For fabrication, today's conventional Si CMOS integrated circuit production process can be used almost unchanged to fabricate the Si nanowire FET, although developing the tuning process is necessary. This is a great advantage for production because the risk and cost of developing new process technology is minimized. Furthermore, the number of Si nanowire FET fabrication processes will be smaller than for today's planar CMOS processes. It is assumed that no channel implantation, including that of halos, is necessary, because of the good SCE control using the nanowire structure, while threshold voltage control can be achieved by work function control of the gate stack. It is expected that at some future date a metal or silicide source/drain will be introduced into ultra-short channel Si nanowire FETs because of the necessity for abrupt junctions, resulting in further elimination of source/drain doping.

3 Modeling

When modeling the conduction of Si nanowire FETs, information on the band structure or E-k relationship of the band is necessary. Figure 5 shows the calculated nanowire band structures using the first principle method with different wire orientations and diameters [14, 15]. As the diameter of the Si nanowire increases from 0.86 nm (Figure 5(b)) to 3.0 nm (Figure 5(c)), the number of the sub-bands or the number of the quantum channels also increases. This means an increase in conduction [16].

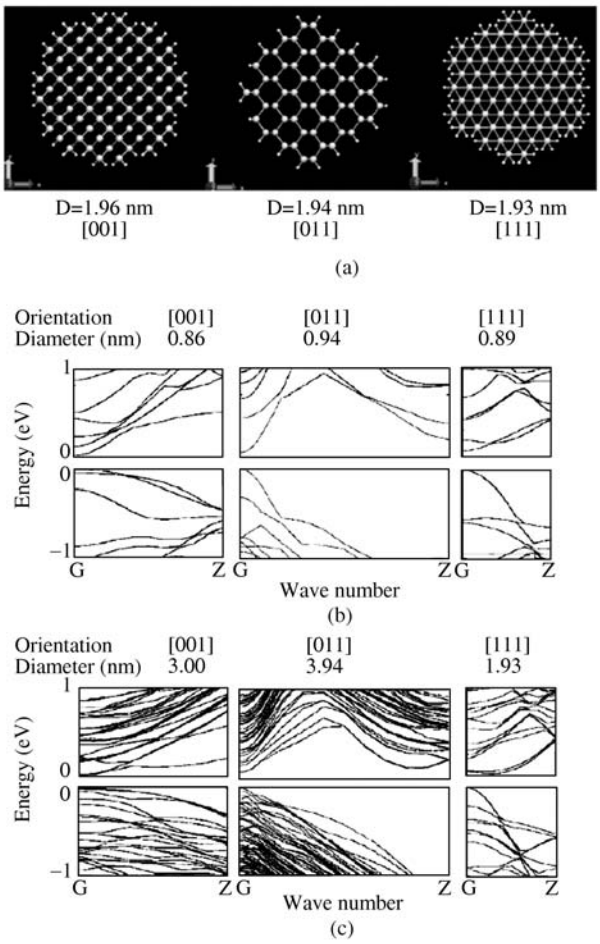

Figure 5 Calculated nanowire band structures.

However, it is noted that carrier scattering between the sub-bands increases with the increase in the number of sub-bands. Thus, there is an optimum diameter for the nanowires, taking into consideration the trade-off between quasi one-dimensional ballistic conduction and the number of quantum channels. The diameter also needs to be determined as a function of the suppression of SCE or the off-leakage current. Recently, the band structure of Si nanowires with diameters of up to 10 nm with 10000 Si atoms and surface roughness has been calculated using first-principle real space density functional theory (RSDFT) [17] as shown in Figure 6. The diameter and orientation dependence of nanowire FET conduction has been analyzed by this method on a massively parallel computer cluster with a theoretical peak performance of several TFLOPS.

A simple compact model of Si nanowire MOSFETs assuming ballistic conduction [18, 19] was obtained using the Landauer formula [20] as shown in Figure 7. Here, $f(E, \mu_S)$ is the Fermi distribution function, E is the energy, and μ_S and $\mu_D = \mu_S - qV_D$, are the Fermi levels associated with the source and drain electrodes. $T_i(E)$ and G_0 represent the transmission coefficient of the carrier in the ith sub-band from source to drain, and the quantum conductance ($G_0 \equiv 2q^2/h = 77.8\mu_S$). The drain current ($I_D$) is determined by the relationship between the gate overdrive and the carrier density, and the E-k relationship of the band structure. The $I_D - V_D$ characteristics of the 7×7-atom [110] square nanowire extended in the (100) direction is also shown in the figure, which are calculated using the sub-band parameters derived from the density functional calculation [21]. The room-temperature $I_D - V_D$ characteristics are similar to those of an ordinary MOSFET. On the other hand, at low temperatures, the curve shows kink structures when the Fermi level crosses the sub-band minimum level and displays a similar magnitude to that of the room-temperature curves.

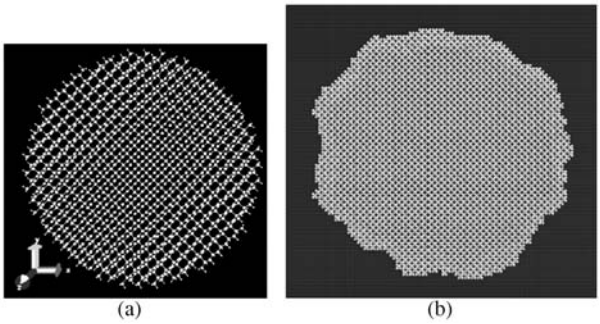

Figure 6 Cross-sections of the nanowires used for the calculation. (a) Si nanowire (8 nm) without roughness; (b) Si nanowire (10 nm) with roughness.

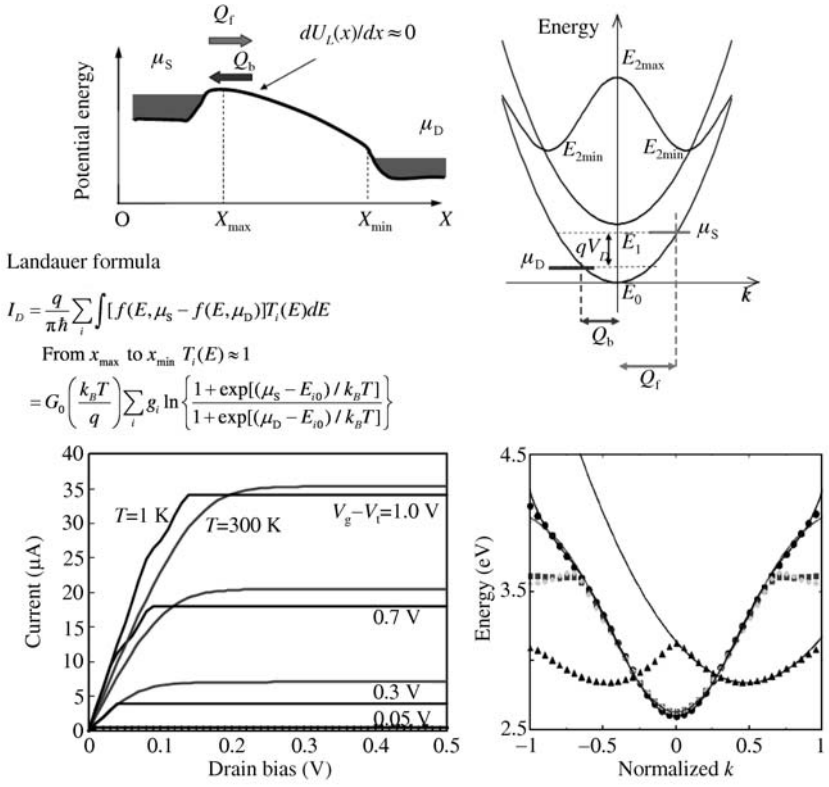

Figure 7 A compact model approach for a Si nanowire FET under the assumption of ballistic conduction.

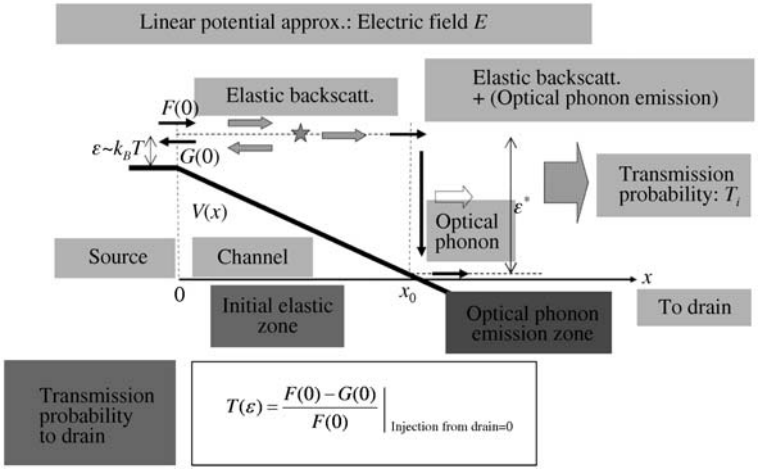

Figure 8 Compact model approach including scattering.

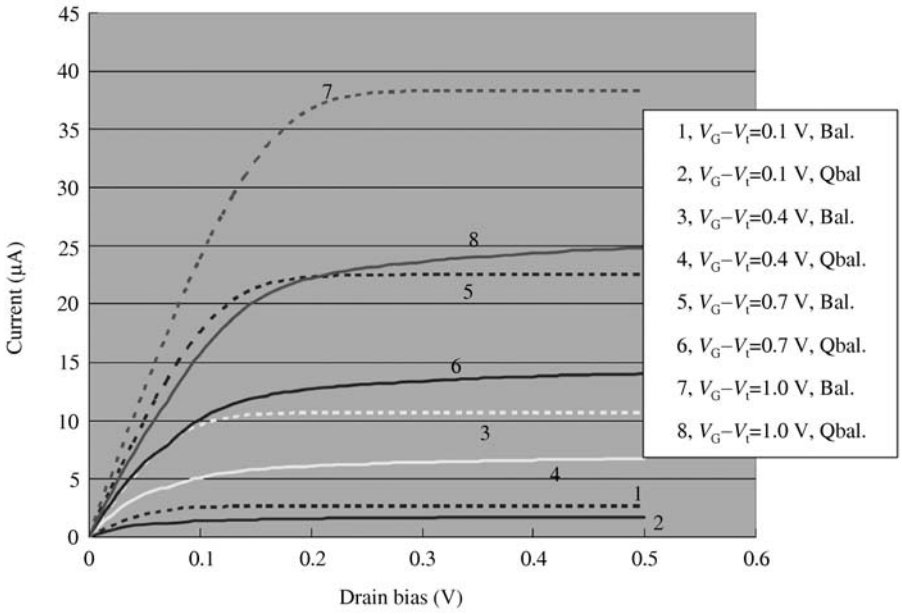

Figure 9 Calculated $I_D - V_D$ characteristics with the scattering model. Solid line: with scattering; broken line: ballistic model.

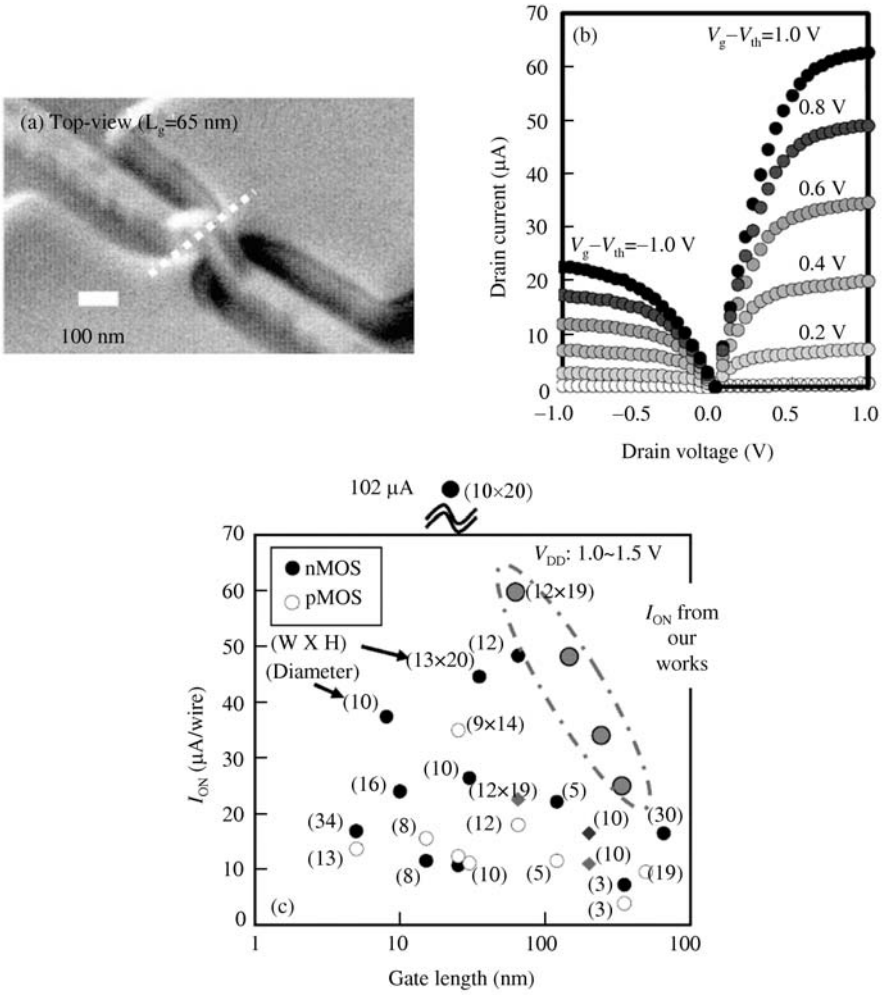

Figure 10 Experimental data. (a) SEM photograph; (b) $I_D - V_D$ characteristics; (c) bench marking with published data.

To include the carrier scattering effect, the channel area is modeled by dividing it into 2 regions [22]. The first region is next to the source, where the carrier energy is assumed to be smaller than the optical phonon energy and only elastic scattering occurs. The second region is next to the first, where the carrier has a larger energy than the optical phonon caused by the acceleration of the lateral electric field, and the inelastic scattering from the optical phonon decreases the carrier energy as shown in Figure 8 [23, 24]. The pseudo one-dimensional Boltzmann equation with a constant electric field is transformed into a pair of carrier flux equations. They are solved analytically, not solved with the relaxation time approximation or the perturbation expansion. The calculated results assuming some of the parameters are shown in Figure 9.

4 Experimental results

The experimental data for Si nanowire FETs show very high drain currents with good off-leakage control ($I_{\rm on}/I_{\rm off} = 10^6$); for example see [10]. Based on these experimental data, future Si nanowire FET on-current is estimated to be much higher than that predicted by ITRS 2009.

5 Conclusions

Si nanowire FETs show very good experimental results for future main stream CMOS devices. There is a need for further research into the modeling of Si nanowire FETs when introducing them into future products.

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