Future of Logic Nano CMOS Technology

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Frontier Research Center, Tokyo Institute of Technology
Outline

1. Brief history of logic device technology
2. Importance of downsizing
3. Current status of Si-CMOS device technologies
4. Major problems for downsizing
5. Increase of leakage current when downsizing
6. Degradation of on-current when downsizing
7. Emerging technologies
8. Summary and conclusions

Acknowledgement

Appendices
1. Brief history of logic device technology
1900 “Electronics” started.
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Cathode (heated)  Grid  Anode (Positive bias)

Same mechanism as that of transistor
1900 “Electronics” started.

Device: Vacuum tube

Device feature size: 10 cm

Major Appl.: Amplifier (Radio, TV, Wireless etc.)

→ Technology Revolution
because there had been no electronics before
(Vacuum tube new device, new application)
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's smart phone
made of semiconductor
has much higher performance with extremely low power consumption
1960: First MOSFET by D. Kahng and M. Atalla

Si/SiO₂ Interface is extraordinarily good
1970 “Micro-Electronics” started.
1970,71: 1st generation of LSIs (Si-MOSFETs)

1k bit DRAM   Intel 1103

MPU   Intel 4004
(Clock 750 KHz)
1970 “Micro-Electronics” started.

Device: Si MOS integrated circuits
Device feature size: 10 μm

Major Appl.: Digital (Computer, PC, etc.)

→ Technology Revolution
because there had been no micro-electronics before
(MOS IC new device, new application)
2000 “Nano-Electronics” started.
2000 “Nano-Electronics” started.

180 nm

Intel Pentium 4 : Clock 1 ~ 2 GHz
2000 “Nano-Electronics” started.

Device: Still, Si CMOS integrated circuits
Device feature size: 180 nm
Major Appl.: Digital (μ-processor, cell phone, etc.)

→ Technology Revolution??

Maybe, just evolution or innovation!
(MOS IC, the same device, similar application)

But very important so many innovations by reducing the size!

Downsizing increases performance and decreases the cost and power consumption.
Now, 2014 “Nano-Electronics” continued.

Device: Still, Si CMOS integrated circuits
Device feature size: a few 10 nm
Major Appl.: Still Digital (μ-processor, cell phone, etc.)

Still evolution and innovation are going on.

**Broadwell SoC (Intel)**

http://download.intel.com/newsroom/kits/14nm/pdfs/Intel_14nm_New_uArch.pdf
Downsizing of the components has been the driving force for circuit evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Vacuum</th>
<th>Transistor</th>
<th>IC</th>
<th>LSI</th>
<th>VLSI</th>
<th>VLSI</th>
</tr>
</thead>
<tbody>
<tr>
<td>1900</td>
<td>Tube</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 cm</td>
<td>cm</td>
<td>mm</td>
<td>10 μm</td>
<td>100 nm</td>
<td>14 nm</td>
<td></td>
</tr>
<tr>
<td>10^{-1}m</td>
<td>10^{-2}m</td>
<td>10^{-3}m</td>
<td>10^{-5}m</td>
<td>10^{-7}m</td>
<td>10^{-8}m</td>
<td></td>
</tr>
</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Feature Size / Technology Node

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm →
0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm →
90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm (2012)
→ 14 nm (2014)

From 1970 to 2013 (Last year)

43 years 1 generation
18 generations 2.5 years
Line width: 1/450 Line width: 1/1.43 = 0.70
Area: 1/200,000 Area: 1/2 = 0.5
2. Importance of downsizing
Downsizing

Important for

- Decreasing cost, and power consumption
- Increasing performance

This is true still for today’s 14 nm!
Merit for downsizing to 14 nm (Intel case)

http://download.intel.com/newsroom/kits/14nm/pdfs/Intel_14nm_New_uArch.pdf

Merit for cost, power consumption, and performance
In 2012

Most Recent SD Card

128GB (Bite)
= 128G X 8bit
= 1T(Tera)bit

$1T = 10^{12} = 1$ Trillion

World Population: 7 Billion
Brain Cell: 10~100 Billion
Stars in Galaxy: 100 Billion
In 2014

Most Recent SD Card

256GB (Bite)
= 256G X 8bit
= 2T(Tera)bit

2T = 10^{12} = 2Trillion

World Population: 7 Billion
Brain Cell: 10~100 Billion
Stars in Galaxy: 100 Billion
128 GB = 1Tbit
2.4cm X 3.2cm X 0.21cm
Volume: 1.6cm³   Weight: 2g
Voltage: 2.7 - 3.6V

Old Vacuum Tube:
5cm X 5cm X 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube:  
5cm X 5cm X 10cm

\[ 1 \text{Tbit} = 10,000 \times 10,000 \times 10,000 \text{ bit} \]

\[ \text{Volume} = (5\text{cm} \times 10,000) \times (5\text{cm} \times 10,000) \times (10\text{cm} \times 10,000) \]
\[ = 0.5\text{km} \times 0.5\text{km} \times 1\text{km} \]

Pingan International Finance Center  
Shanghai, China  
(Year 2016)

Indian Tower  
Mumbai, India  
(Year 2016)

Burj Khalifa  
Dubai, UAE  
(Year 2010)

1Tbit
Old Vacuum Tube: 50W/tube (assuming)

1Tbit = 10^{12}bit
Power = 0.05kWX10^{12}=50\ TW

Nuclear Power Generator

1MkW=1BW

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits by downsizing is extremely important for power saving.
Various semiconductor devices

Brain is very important

→ Brain: Integrated Circuits

→ Ear, Eye: Sensor

→ Mouth: RF/Opto device

→ Stomach: PV device

→ Hands, Legs: Power device
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
3. Current status of Si-CMOS device technologies
More Moore to More More Moore

Technology node

<table>
<thead>
<tr>
<th>Now</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td>65nm</td>
<td>14nm</td>
</tr>
<tr>
<td>45nm</td>
<td>10nm, 7nm, 5nm, 3.5nm</td>
</tr>
<tr>
<td>32nm</td>
<td></td>
</tr>
<tr>
<td>22nm</td>
<td></td>
</tr>
<tr>
<td>Lg 35nm</td>
<td></td>
</tr>
<tr>
<td>Lg 30nm</td>
<td></td>
</tr>
</tbody>
</table>

Main stream
(Fin, Tri, Nanowire)

Alternative
(FDSOI)

Si is still main stream for future !!

Planar

Tri-Gate

Si

Others

Alternative (III-V/Ge)
Channel FinFET

Emerging Devices

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)
High-k gate dielectrics

Continued research and development

<table>
<thead>
<tr>
<th>Hf-based oxides</th>
<th>EOT=0.9nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>45nm</td>
<td>HfO₂/SiO₂ (IBM)</td>
</tr>
<tr>
<td>EOT:1nm</td>
<td></td>
</tr>
<tr>
<td>32nm</td>
<td></td>
</tr>
<tr>
<td>EOT:0.95nm</td>
<td></td>
</tr>
<tr>
<td>22nm</td>
<td></td>
</tr>
<tr>
<td>EOT:0.9nm</td>
<td></td>
</tr>
<tr>
<td>14nm</td>
<td></td>
</tr>
<tr>
<td>EOT:0.9nm</td>
<td></td>
</tr>
<tr>
<td>10nm, 7nm, 5nm, 3.5nm,</td>
<td></td>
</tr>
</tbody>
</table>

SiO₂ IL (Interfacial Layer) is used at Si interface to realize good mobility

Technology for direct contact of high-k and Si is necessary

EOT=0.52 nm
Remote SiO₂-IL scavenging HfO₂ (IBM)

EOT=0.37nm
EOT=0.40nm
EOT=0.48nm

0.48 → 0.37nm Increase of I_d at 30%

Direct contact with La-silicate (Tokyo. Tech.)

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM2009, (IBM)
High-k is very important, however very difficult.

Thickness (EOT) decreased only 0.05 nm (or 0.5 Å, or 1 atom layer) for every generation.
### Benchmark of device characteristics

<table>
<thead>
<tr>
<th>Structure</th>
<th>Bulk Planar</th>
<th>Tri-Gate 22nm</th>
<th>Tri-Gate NW</th>
<th>ETSOI</th>
<th>Bulk Planar</th>
<th>GAA NW</th>
<th>GAA NW</th>
<th>Ω-gate NW</th>
</tr>
</thead>
<tbody>
<tr>
<td>L&lt;sub&gt;g&lt;/sub&gt; (nm)</td>
<td>35</td>
<td>30</td>
<td>30</td>
<td>14</td>
<td>22</td>
<td>20</td>
<td>35/25</td>
<td>22/30</td>
</tr>
<tr>
<td>Gate Dielectrics</td>
<td>Hf-based</td>
<td>Hf-based</td>
<td>SiO&lt;sub&gt;2&lt;/sub&gt;</td>
<td>HfO&lt;sub&gt;2&lt;/sub&gt;</td>
<td>HfO&lt;sub&gt;2&lt;/sub&gt; ?</td>
<td>Hf-based</td>
<td>HfZrO&lt;sub&gt;2&lt;/sub&gt;</td>
<td>SiO&lt;sub&gt;2&lt;/sub&gt;</td>
</tr>
<tr>
<td>EOT (nm)</td>
<td>1</td>
<td>0.95</td>
<td>0.9</td>
<td>3</td>
<td>~1</td>
<td>-</td>
<td>1.5</td>
<td>-</td>
</tr>
<tr>
<td>V&lt;sub&gt;th&lt;/sub&gt; (V)</td>
<td>~0.4</td>
<td>~0.3</td>
<td>~0.2</td>
<td>-0.15 (nFET)</td>
<td>0.3~0.4</td>
<td>~0.3</td>
<td>0.3~0.4</td>
<td>~0.5</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt; (V)</td>
<td>1</td>
<td>1</td>
<td>0.8</td>
<td>1</td>
<td>0.9</td>
<td>0.9</td>
<td>1</td>
<td>1.1</td>
</tr>
<tr>
<td>I&lt;sub&gt;ON&lt;/sub&gt; (mA/um)</td>
<td>1.36/1.07</td>
<td>1.53/1.23</td>
<td>1.26/1.1</td>
<td>0.83 (nFET)</td>
<td>0.59/0.62 (I&lt;sub&gt;eff&lt;/sub&gt;)</td>
<td>1.2/1.05</td>
<td>0.83/0.95</td>
<td>2.05/1.5</td>
</tr>
<tr>
<td>DIBL (mV/V) nFET/pFET</td>
<td>~150</td>
<td>~200</td>
<td>46/50</td>
<td>&lt;50</td>
<td>-</td>
<td>104/115</td>
<td>65/105</td>
<td>56/9</td>
</tr>
<tr>
<td>SS (mV/dec)</td>
<td>-</td>
<td>~100</td>
<td>~70</td>
<td>&lt;80</td>
<td>-</td>
<td>87</td>
<td>85</td>
<td>&lt;80</td>
</tr>
</tbody>
</table>
Supply voltage affects significantly!

**NMOS**

- **Intel [1]**
  - Bulk 32nm, $V_{DD}=0.8V$
  - Tri-Gate 22nm, $V_{DD}=0.8V$

- **Samsung [3]**
  - Bulk 20nm, $V_{DD}=0.9V$

- **IBM [5]**
  - GAA NW, $V_{DD}=1V$

- **IBM [6]**
  - FinFET 25nm, $V_{DD}=1V$

- **STMicro. [8]**
  - GAA NW, $V_{DD}=1.1V$

**PMOS**

- **Intel [1]**
  - Bulk 32nm, $V_{DD}=0.8V$
  - Tri-Gate 22nm, $V_{DD}=0.8V$

- **IBM [2]**
  - Bulk 45nm, $V_{DD}=1V$

- **IBM [7]**
  - ETSOI, $V_{DD}=1V$

- **IBM [10]**
  - ETSOI, $V_{DD}=0.9V$

- **IBM [7]**
  - ETSOI, $V_{DD}=1.1V$

- **Samsung [3]**
  - Bulk 20nm, $V_{DD}=0.9V$

**Notes:**

- Supply voltage affects significantly!

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**References:**

1. C. Auth et al., pp.131, VLSI2012 (Intel).
4. S. Saitoh et al., pp.11, VLSI2012 (Toshiba).
5. S. Bangsaruntip et al., pp.297, IEDM2009 (IBM).
7. A. Khakifirooz et al., pp.117, VLSI2012 (IBM).
9. S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)
10. K. Cheng et al., pp.419, IEDM2012 (IBM)
I\textsubscript{ON} and I\textsubscript{OFF} benchmark updating

Lower supply voltage degrades the ratio.

![Graph showing I\textsubscript{ON} and I\textsubscript{OFF} values for different devices with varying supply voltages.](image)

Examples of the state of the art
Current status of Si-CMOS device technologies

Fin, Tri gate FET
Multi-gate structures

**Fin**

**Tri-gate**

**Tri-gate (Variation)**

**Ω-gate**

**All-around**
How far can we go for production?

Rather than $I_{\text{off}}$ value, $I_{\text{on}}/I_{\text{off}}$ ratio is important.

Now, $I_{\text{on}}/I_{\text{off}}$ ratio is typically $10^6$.

However, it degrades significantly with decrease in $V_{\text{supply}}$. 
I\text{ON} \text{ and } I\text{OFF} \text{ benchmark}

### NMOS

- **Intel [a]**
  - Bulk 32nm
  - $V_{DD}=0.8V$
- **Intel [a]**
  - Tri-Gate 22nm
  - $V_{DD}=0.8V$
- **Intel [b]**
  - Bulk 45nm
  - $V_{DD}=1V$
- **Samsung [c]**
  - Bulk 20nm
  - $V_{DD}=0.9V$
- **IBM [j]**
  - GAA NW
  - $V_{DD}=1V$
- **Tokyo Tech. [i]**
  - Ω-gate NW
  - $V_{DD}=1V$

### PMOS

- **Intel [a]**
  - Bulk 32nm
  - $V_{DD}=0.8V$
- **Intel [b]**
  - Bulk 45nm
  - $V_{DD}=1V$
- **Intel [a]**
  - Tri-Gate 22nm
  - $V_{DD}=0.8V$
- **IBM [j]**
  - ETSOI
  - $V_{DD}=0.9V$
- **IBM [g]**
  - ETSOI
  - $V_{DD}=0.9V$
- **Samsung [c]**
  - Bulk 20nm
  - $V_{DD}=0.9V$
- **IBM [g]**
  - ETSOI
  - $V_{DD}=1V$
- **IBM [f]**
  - FinFET 25nm
  - $V_{DD}=1V$
- **IBM [g]**
  - ETSOI
  - $V_{DD}=1V$
- **IBM [j]**
  - ETSOI
  - $V_{DD}=1V$
- **STMicro. [h]**
  - GAA NW
  - $V_{DD}=1.1V$
- **IBM [e]**
  - GAA NW
  - $V_{DD}=1V$

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[a] C. Auth et al., pp.131, VLSI2012 (Intel).
[d] S. Saitoh et al., pp.11, VLSI2012 (Toshiba).
[g] A. Khakifirooz et al., pp.117, VLSI2012 (IBM).
Tri-gate has been implemented since 22nm node, enabling further scaling.
PMOS channel under the gate

S/D region showing the SiGe epitaxy

A fin width of 8nm to balance SCE and $R_{\text{ext}}$

A fin height of 34nm to balance drive current vs. capacitance

Intel’s fin is triangle shape!

C. Auth et al., pp.131, VLSI2012 (Intel)
SS of 71 and 72 mV/dec for HP NMOS and PMOS, respectively

DIBL of 30 and 35 mV/V for NMOS and PMOS, respectively

$V_{th}$ of 22 nm is about 0.1 ~0.2 V lower than that of 32nm
Low $V_{cc\min}$ 16nm node FinFETs (TSMC)

S. Wu et al., pp.224, IEDM2013 (TSMC)

- Fin patterning and formation on bulk with 48 nm fin pitch (pitch-splitting technique)
- Poly-silicon deposition and gate patterning with (gate pitch of 90 nm)
- High-k/Metal gate RPG process
- Raised source/drain with dual epitaxy

Static noise margin of 0.07 $\mu$m² high density SRAM cell at 0.8 V and 0.6 V

Low leakage (SVt : purple)
- $L_g = 34$ nm
- $SS < 65$ mV/dec.
- $DIBL < 30$ mV/V
- $I_{dsat} = 520/525$ uA/um at 0.75 V
- $I_{off} = 30$ pA/um
**Advanced RMG for 14 nm FinFETs (GF)**

- Dummy gate removal
- STI oxide extra recess
- WF adjust treatment
- W selective etch
- Contact formation with SAC

![Image of FinFET structures](image)

- STI oxide extra recess during replacement metal gate (RMG) module increases $I_{on}$
- W selective etch improves AC performance and gate-contact short yield
- Combination of novel work function adjust treatment and WFM provides $V_t$ turning

* No information about $L_{gate}$
Intel 14nm Technology by Mark Bohr, August 11, 2014

Interconnects

22 nm Process
- 80 nm minimum pitch

14 nm Process
- 52 nm (0.65x) minimum pitch

SRAM Cell

22 nm 1st Generation Tri-gate Transistor

14 nm 2nd Generation Tri-gate Transistor

.108 um² (Used on CPU products)

.0588 um² (0.54x area scaling)
DIBL ~ 40 - 50 mV for N/PFET for $L_g = 20$ nm

$\Rightarrow$ Controlled short channel effect

$I-V$ performance
- $L_g = 20$ nm
- $SS = 70$ mV/dec

SRAM performance
- $SNM = 140$ mV at 0.75V
- $SNM = 120$ mV at 0.55 V
Examples of the state of the art Si-CMOS device technologies

FD SOI FET
L. Grenouillet et al., pp.64, IEDM2012 (CEA-LETI)

- Wider back bias (BB) tunability with dual STI (shallow & deep)

- Successive performance boost and leakage current control by BB
Extremely Thin SOI (ETSOI) (IBM)

K. Cheng et al., pp.419, IEDM2012 (IBM)

Also, ET-SOI works very good!

- Hybrid CMOS
  - Si Channel nFET
  - Strained SiGe Channel pFET
- RO delay improvement over FinFET with FO = 2
nMOS => Si channel/SiC RSD
pMOS => SiGe channel/SiGe RSD

cSiGe formation at PFET area
STI RIE and liner deposition
STI fill and CMP
Ground plane (GP) implantation and annealing
High-k / metal gate patterning
SiN spacer deposition
NFET spacer formation and ISPD SiC
RSD EPI
Hard mask deposition
PFET spacer formation and ISBD
SiGe RSD EPI
2nd spacer formation
Rapid thermal annealing (RTA) +
laser annealing
Salicide
MOL and BEOL
14 nm FDSOI Technology (STMicroelectronics)

O. Weber et al., pp.14, VLSI2014 (STMicroelectronics)

New Front-End process elements
- Dual SOI/SiGeOI N/P channel
- Dual workfunction gate-first HKMG integration scheme
- Dual in-situ doped Si:CP/SiGeB N/P RSD

⇒ 30% speed boost at the same power
⇒ 55% power reduction at the same speed over the 28nm node
Silicon-on-Thin-Buried Oxide CMOS (LEAP)

S. Kamohara et al., pp.154, VLSI2014 (LEAP)

- Very small $V_{th}$ and $I_{on}$ variability was demonstrated for one million transistors.
- High performance due to less S/D doping and back bias controlling.
- Confirmed 6-T SRAM operation (2 Mbit) at less than 0.4 V with a 5.5-ps access time.
- Demonstrated that the minimum operating voltage can be controlled at <0.4 V by back-bias against temperature variation.
nFET - Strained SOI (SSDOI)  

pFET – SiGe-on-insulator (SGOI)  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Greene et al.</th>
<th>Packan et al.</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>CGP (nm)</td>
<td>130</td>
<td>112.5</td>
<td>100</td>
</tr>
<tr>
<td>L_G (nm)</td>
<td>26</td>
<td>35</td>
<td>22</td>
</tr>
<tr>
<td>N/P FET DIBL (mV)</td>
<td>-</td>
<td>140/180</td>
<td>75/130</td>
</tr>
<tr>
<td>N/P I_ON (mA/μm)</td>
<td>1.55/1.22</td>
<td>1.62/1.37</td>
<td>1.65/1.25</td>
</tr>
<tr>
<td>N/P I_EFF (mA/μm)</td>
<td>-</td>
<td>0.86/0.74</td>
<td>0.95/0.70</td>
</tr>
<tr>
<td>N/P I_dlin (μA/μm)</td>
<td>231/240</td>
<td>240/250</td>
<td></td>
</tr>
<tr>
<td>Stress element</td>
<td>eSi:C eSiGe</td>
<td>Dislocation, eSiGe</td>
<td>SSDOI, SGOI</td>
</tr>
</tbody>
</table>

\( t \sim 6 \text{ nm Channel} \)
Examples of the state of the art
Current status of Si-CMOS device technologies

Nanowire FET
Multi-gate structures

Fin

Tri-gate

Tri-gate (Variation)

Ω-gate

All-around
Lg = 25~35nm GAA NW

Hydrogen anneal provide smooth channel surface

Competitive with conventional CMOS technologies

Scaling the dimensions of NW leads to suppressed SCE
Gate All Around Nanowire (GAA NW)

- Gate all around structure
- \(L_g\) of 22~30nm
- Bulk wafer-based integration
- High drive currents by special stress and channel orientation design
- $L_g = 14\text{nm}$ Tri-Gate NW
- High SCE immunity at $L_g$ of 14nm
- $V_{th}$ tuning by applying $V_{sub}$ with thin BOX of 20nm

Vth control by back-gate bias
**Ω-gate Si Nanowire (TIT)**

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  
  \(1.32 \text{ mA/μm} @ I_{\text{OFF}}=117 \text{ nA/μm}\)
- DIBL of 62mV/V and SS of 70mV/dec for nFET
Examples of the state of the art
Current status of Si-CMOS device technologies

Planar Bulk FET
Isolation (wells, Vt)
IO EG gate growth
Dummy gate patterning
Logic SG, IO, SRAM extension/halo
Spacer dep/patterning
eSiGe formation
Raised source/drain formation
Advanced gate stack formation
Tungsten stud (TS) contact formation
CA/CB Tungsten contacts
M1 double patterning
Self Aligned V0
BEOL

- $L_{gate} = 20$ nm
- 0.55X density scaling
- N/P DIBL = 121/126 mV
- $SS = 90/86$ mV/dec.
- SNM = 160mV at 0.9V
Process technologies for State of the art CMOS

Appendix 1
4. Major problems for downsizing
1. Lithography of sub-10 nm pattern
   - Delay in EUV development.
   - Process step increase for double, triple, quadruple patterning as alternate

2. Increase of leakage current

3. Decrease of on-current

4. Interconnect problems
   - Increase of R and C

5. Variability, reliability, yield.

Explained in this tutorial
5. Increase of leakage current when downsizing
Leakage components

1. Punch through current between S and D
2. Subthreshold current between S and D
3. Direct-tunneling current between S and D
4. Gate leakage current between G and S/B/D
1. Punch-through between S and D

- **Region governed by gate bias**: 0V
- **Region governed by drain bias**: 1V

**Gate oxide**

**Gate metal**

**Source**

**Drain**

**Channel**

**Substrate** 0V

**0V < V_{dep} < 1V**

**Large I_{OFF}**

**Large I_{OFF} (Electron current)** 0V

**t_{ox}** and **V_{dd}** have to be decreased for better channel potential control \(\rightarrow I_{OFF} \) Suppression

**DL touch with S Region (DL)**

- No t_{ox}, V_{dd} thinning
- Large I_{OFF}

**Punch-through between S and D (Electron current)**

**t_{ox}** thinning

**V_{dd}**

0V

1V

0.5V
1. Punch-through between S and D

There are 3 solutions to suppress the depletion layer

A. Decrease supply voltage → Very difficult
   as explained later

B. Decrease $t_{ox}$ to enhance the channel potential controllability by gate bias

C. Gate/channel configuration change to enhance the channel potential controllability by gate bias
   Also, decrease $t_{Si}$

Fin-FET, ET-SOI, etc.
B. Decrease tox

A. Toriumi (Tokyo Univ), IEDM 2006, Short Course
C. Configuration change for channel and gate structures for better control of channel potential.

Also, decrease $t_{Si}$

Fin-FET, ET-SOI, etc.
Extremely Thin (or Fully-Depleted) SOI

- Make Si layer thin (decrease $t_{Si}$)
- Control channel potential also from the bottom
Surrounding gate structure (Multiple gates)

- Make Si layer thin (decrease $t_{Si}$)
- Control channel potential also by multiple gates not only from top & bottom but maybe also from side
Multi-gate structures

- Fin
- Tri-gate
- Tri-gate (Variation)
- Ω-gate
- All-around
Multi-gate MOSFETs have advantage not only suppressing $I_{\text{off}}$, but also for increasing $I_{\text{on}}$ over planer MOSFETs

1. Because of higher mobility due to lower vertical electric field and low dopant concentration in the channel

2. Because of higher carrier density at the round corner
Electron Density
\( \times 10^{19} \text{cm}^{-3} \)

Edge portion
Flat portion

Distance from SiNW Surface (nm)

Inversion areal ratio: 29 %
2. Direct-tunneling between S and D

Wave function of electron penetrates the channel potential barriers by quantum mechanical physics, when the channel length is around 3 nm.
There is no solutions!

Built-in potential between Source and Channel pn junction < 0.7 V

Tunneling distance 3 nm

When transistor is at off state

Direct-tunnel current

Energy or Potential for Electron

Source Channel Drain

Downsizing limit is @ Lg \cong 3 \text{ nm.}
3. Subthreshold leakage current of MOSFET

Subthreshold Leakage Current

\[ I_{off} \propto \exp(aV_g) \]

\[ V_g = 0V \]

Subthreshold region

\[ I_{on} \propto V_g - V_{th} \]

\[ V_{th} \]

(Threshold Voltage)
Subthreshold leakage current

Electron Energy
Boltzmann statics

Exp (qV/kT)

Lg $\rightarrow 1/2$
Vd, Vg $\rightarrow 1/2$
Vth $\rightarrow 1/2$

However
loff $\rightarrow 10^3$ in this example

Because of
log-linear dependence
Subthreshold leakage current of MOSFET

Subthreshold leakage current of MOSFET is OK at single transistor level but not OK for billions of transistors.

**Ion**

Subthreshold region

$V_{g} = 0\text{V}$

$\text{loff} \propto \exp(aV_{g})$

Subthreshold leakage current

$\text{Ion} \propto V_{g} - V_{th}$

(Threshold Voltage)
3. Subthreshold current between S and D

Solution: however very difficult

Keep Vth as high as possible

- Do not decrease supply voltage, Vd
  → However, punchthrough enhanced

- Suppress variability in Vth

Thus, subthreshold current will limit the downsizing, especially for mobile devices
4. Gate leakage current

Probably OK using high-k, until EOT=0.4 nm

See Appendix 2

Gate Leakage current

ITRS requirement

La silicate
Gate dielectrics

H. Iwai, SBMicro 2013
Our Work at TIT: High-k

Our result at TIT

EOT = 0.40nm

Electron Mobility [cm$^2$/Vsec]

L/W = 5/20µm
T = 300K
$N_{sub} = 3 \times 10^{16}$ cm$^{-3}$
All the 4 leakage components increase, when downsizing

1. Punch through current between S and D
   Solution: Enhance gate bias control to channel potential
   → Decrease $t_{ox}$ (EOT) for gate oxide, and $t_{Si}$ for SOI & Fin FETs

2. Subthreshold current between S and D
   Solution: Keep as high $V_{th}$ as possible
   → Keep as high $V_{supply}$ as possible, but difficult
   → This will limit the downsizing depending on application
      before $L_g = \sim 3 \text{ nm}$

3. Direct-tunneling current between S and D
   No solution. Limit the downsizing at $L_g = \sim 3 \text{ nm}$

4. Gate leakage current between G and S/B/D
   Solution. Introduction of new material for higher k and band offset
The limit is different depending on application.

- **HP CMOS** (High Performance)
  - Highest Ion
  - Lowest CV/I
  - High leakage
  - Medium Vdd

- **LOP CMOS** (Low Operation Power)
  - Lowest Vdd
  - Medium Ion, medium CV/I
  - Medium leakage

- **LSTP CMOS** (Low Standby Power)
  - Lowest leakage
  - Low Ion, high CV/I
  - High Vdd

Source: 2007 ITRS Winter Public Conf.
How far can we go for production?

<table>
<thead>
<tr>
<th>Past</th>
</tr>
</thead>
<tbody>
<tr>
<td>10(\mu)m (\rightarrow) 8(\mu)m (\rightarrow) 6(\mu)m (\rightarrow) 4(\mu)m (\rightarrow) 3(\mu)m (\rightarrow) 2(\mu)m (\rightarrow) 1.2(\mu)m (\rightarrow) 0.8(\mu)m (\rightarrow) 0.5(\mu)m (\rightarrow) 0.35(\mu)m (\rightarrow) 0.25(\mu)m (\rightarrow) 180nm (\rightarrow) 130nm (\rightarrow) 90nm (\rightarrow) 65nm (\rightarrow) 45nm (\rightarrow) 32nm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Intermediate node</th>
</tr>
</thead>
<tbody>
<tr>
<td>Now</td>
</tr>
<tr>
<td>28nm (\rightarrow) 22nm (\rightarrow) 14nm (\rightarrow) 10 nm (\rightarrow) 7nm (\rightarrow) 5nm? (\rightarrow) 3.5nm? (\rightarrow) 2.5 nm?</td>
</tr>
</tbody>
</table>

Limit depending on applications

Fundamental limit

Subthreshold punchthrough

Direct-tunnel

Future
However, careful about the commercial name of technology!

Recently,
Gate length (Lg) is much larger than the Technology name

22 nm Technology by Intel

Lg (Gate length) = 30 nm (HP), 34 nm (MP), 34 nm or larger (SP)
IEDM 2012, VLSI 2013

14 nm Technology by Global

Lg (Gate length) = 25 nm Euro SOI 2014

10 nm Technology by Leti (FD-SOI)

Lg (Gate length) = 15 nm ECS Fall 2013
<table>
<thead>
<tr>
<th></th>
<th>Commercial name (nm)</th>
<th>Year 2013</th>
<th>Year 2027</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal half pitch (nm)</td>
<td>X 0.70 / 2 years</td>
<td>14 (nm)</td>
<td>1.3 (nm)</td>
</tr>
<tr>
<td>Lg (nm)</td>
<td>X 0.80 / 2 years</td>
<td>40 (nm)</td>
<td>8 (nm)</td>
</tr>
<tr>
<td>Vdd (V)</td>
<td>X 0.83 / 2 years</td>
<td>20.2 (nm)</td>
<td>5.6 (nm)</td>
</tr>
<tr>
<td>EOT (nm)</td>
<td>X 0.96 / 2 years</td>
<td>0.86 (nm)</td>
<td>0.65 (nm)</td>
</tr>
<tr>
<td>T_{Si} (nm)</td>
<td>X 0.91 / 2 years</td>
<td>0.80 (nm)</td>
<td>0.43 (nm)</td>
</tr>
<tr>
<td></td>
<td>X 0.84 / 2 years</td>
<td>7.4 (nm)</td>
<td>2.0 (nm)</td>
</tr>
</tbody>
</table>

Only the commercial names decreases X0.7/ 2 years

Difference between the commercial name and physical parameters becomes larger

Recently, companies become not to disclose Lg values at conferences

1.3 nm technology!
but HP = 8nm
Lg = 5.6 nm
## ITRS 2013 (Just published in April 2014)

<table>
<thead>
<tr>
<th>Year</th>
<th>2013</th>
<th>2015</th>
<th>2017</th>
<th>2019</th>
<th>2021</th>
<th>2023</th>
<th>2025</th>
<th>2027</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Commercial name (nm)</strong></td>
<td>14</td>
<td>10</td>
<td>7</td>
<td>5</td>
<td>3.5</td>
<td>2.5</td>
<td>1.8</td>
<td>1.3</td>
</tr>
<tr>
<td><strong>Metal half pitch (HP) (nm)</strong></td>
<td>40</td>
<td>32</td>
<td>25.3</td>
<td>20</td>
<td>15.9</td>
<td>12.6</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td><strong>$L_g$ (nm)</strong></td>
<td>20.2</td>
<td>16.8</td>
<td>14.0</td>
<td>11.7</td>
<td>9.7</td>
<td>8.1</td>
<td>6.7</td>
<td>5.6</td>
</tr>
<tr>
<td><em>(L_g for ITRS 2007)</em></td>
<td>(13)</td>
<td>(10)</td>
<td>(8)</td>
<td>(6)</td>
<td>(5)</td>
<td>(4.5 in 2022)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>$L_g$ for low stand by power (nm)</strong></td>
<td>23</td>
<td>19</td>
<td>16</td>
<td>13.3</td>
<td>11.1</td>
<td>9.3</td>
<td>7.7</td>
<td>6.4</td>
</tr>
<tr>
<td><strong>$V_{dd}$ (V)</strong></td>
<td>0.86</td>
<td>0.83</td>
<td>0.80</td>
<td>0.77</td>
<td>0.74</td>
<td>0.71</td>
<td>0.68</td>
<td>0.65</td>
</tr>
<tr>
<td><em>(V_{dd} (V) for ITRS 2007)</em></td>
<td>(0.90)</td>
<td>(0.80)</td>
<td>(0.70)</td>
<td>(0.70)</td>
<td>(0.65)(0.65 in 2022)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>EOT (nm)</strong></td>
<td>0.80</td>
<td>0.73</td>
<td>0.67</td>
<td>0.61</td>
<td>0.56</td>
<td>0.51</td>
<td>0.47</td>
<td>0.43</td>
</tr>
<tr>
<td><em>(EOT (nm) for ITRS 2007)</em></td>
<td>(0.60)</td>
<td>(0.60)</td>
<td>(0.55)</td>
<td>(0.50)</td>
<td>(0.50)(0.50 in 2022)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>$T_{Si}$ (nm)</strong></td>
<td>7.4</td>
<td>6.1</td>
<td>5.1</td>
<td>4.3</td>
<td>3.6</td>
<td>3.0</td>
<td>2.5</td>
<td>2.0</td>
</tr>
<tr>
<td><em>(T_{Si} (nm) for ITRS 2007)</em></td>
<td>(6.0)</td>
<td>(6.0)</td>
<td>(4.5)</td>
<td>(3.8)</td>
<td>(3.2)</td>
<td>(3.0 in 2022)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Before, HP: X 0.70 / 2 years,  Lg: X 0.70 / 2 years

### Now, HP: X 0.80 / 2 years,  Lg: X 0.83 / 2 years

→ Thus, now more generations and more years until reaching limit
Intel kept $X \sim 0.7$ for pitch until 14 nm technology, but it is not certain for future.

**SRAM area**

**Logic area**

Gate Pitch $\times$ Metal Pitch (nm$^2$)

---

**Table:**

<table>
<thead>
<tr>
<th></th>
<th>22 nm Node</th>
<th>14 nm Node</th>
<th>Scale</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor Fin Pitch</td>
<td>60</td>
<td>42</td>
<td>.70x</td>
</tr>
<tr>
<td>Transistor Gate Pitch</td>
<td>90</td>
<td>70</td>
<td>.78x</td>
</tr>
<tr>
<td>Interconnect Pitch</td>
<td>80</td>
<td>52</td>
<td>.65x</td>
</tr>
</tbody>
</table>

---

**Graphs:**

- 22 nm Process: .108 um$^2$
- 14 nm Process: .0588 um$^2$

---

http://download.intel.com/newsroom/kits/14nm/pdfs/Intel_14nm_New_uArch.pdf
6. Degradation of on-current when downsizing
When downsizing

1. Mobility degradation
2. Carrier density decrease

1, 2 → decrease of on-current
$\mu$ (mobility) degradation

$t_{ox} \downarrow \quad \rightarrow \quad d \downarrow$

Strong interaction between carriers and metal/oxide interface

$\mu \downarrow$

$t_{Si} \downarrow \quad \rightarrow \quad d \downarrow$

Strong interaction between carriers and Si surface (or interface)

Gate electrode

Gate oxide

Si channel

Gate stack

$\text{Si surface}$

Nano-wire

Fin / Tri$_{94}$
<table>
<thead>
<tr>
<th>Year</th>
<th>2013</th>
<th>2015</th>
<th>2017</th>
<th>2019</th>
<th>2021</th>
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<td>0.51</td>
<td>0.47</td>
<td>0.43</td>
</tr>
<tr>
<td>$T_{Si}$ (nm)</td>
<td>7.4</td>
<td>6.1</td>
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<td>4.3</td>
<td>3.6</td>
<td>3.0</td>
<td>2.5</td>
<td>2.0</td>
</tr>
</tbody>
</table>

**Graphs:**

- **Graph 1:**
  - $t_{ox}$: Oxide thickness
  - $\mu$: Mobility
  - Ordinate: Mobility ($cm^2/Vsec$)
  - Abscissa: EOT (nm)
  - Solid: La-silicate oxide
  - Open: Hf-based oxides
  - Data at 1 MV/cm

- **Graph 2:**
  - $t_{Si}$: Silicon thickness
  - $\mu$: Mobility
  - Ordinate: Mobility ($cm^2/Vsec$)
  - Abscissa: $T_{SOI}$ [nm]
  - Data at $T=300K$, $E_{eff}=0.3MV/cm$

**References:**

- K. Uchida et al., pp.47, IEDM2002 (Toshiba)
Carrier density decrease

ITRS 2013

<table>
<thead>
<tr>
<th>Year</th>
<th>2013</th>
<th>2015</th>
<th>2017</th>
<th>2019</th>
<th>2021</th>
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<td>$T_{Si}$ (nm)</td>
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<td>6.1</td>
<td>5.1</td>
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<td>3.6</td>
<td>3.0</td>
<td>2.5</td>
<td>2.0</td>
</tr>
</tbody>
</table>

$t_{Si} \downarrow \Rightarrow$ Volume $\downarrow \Rightarrow$ DOS $\downarrow \Rightarrow$ Carrier density $\downarrow$

Si nanowire band structure

Diameter

1 nm
2 nm
3 nm
4 nm
6 nm

7. Emerging technologies
7.1 Alternative channel technologies
Current status

Good research results aiming for low voltage (= 0.5V) operation.

In general good mobility, but poor S-factor.

CMOS inverter results at primitive stage.

Production starting year predicted at 2018 by ITRS 2011 and 13, but premature to be ready for the today’s scale microprocessor production.

No or very few reports for circuits, large wafer, yield, variability, reliability, production cost etc.
Recently various device structures have been demonstrated on InGaAs platform for achieving higher performance at lower power supply.

Improvement in high-k/III-V interface and III-V growth technology has been a key factor.
Low Voltage CMOS

Source: S. Takagi
Multi-gate III-V and Si benchmark

InGaAs GAA, $L_{ch}=50$nm, Dielectric: 10nm Al$_2$O$_3$, $V_{DS}=0.5$V (Purdue Uni.)
J. J. Gu et al., pp.769, IEDM2011 (Purdue).

InGaAs Tri-gate, $L_g=60$ nm, EOT 12A
$V_{DS}=0.5$V (Intel)
M. Radosavljevic et al., pp.765, IEDM201(Intel).

InGaAs FinFET, $L_{ch}=130$nm EOT 3.8nm
$V_{DS}=0.5$V (NUS)
H. –C. Chin et al., EDL 32, 2 (2011) (NUS)

InGaAs Nanowire, $L_g= 200$nm, $T_{ox} 14.8$nm
$V_{DS}=0.5$V (Hokkaido Uni.)
K. Tomioka et al., pp.773, IEDM2011 (Hokkaido Uni.).

InGaAs FinFET, $L_{ch}=130$nm EOT 3.8nm
$V_{DS}=0.5$V (NUS)
H. –C. Chin et al., EDL 32, 2 (2011) (NUS)

InGaAs GAA, $L_{ch}=50$nm, Dielectric: 10nm Al$_2$O$_3$, $V_{DS}=0.5$V (Purdue Uni.)
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M. Radosavljevic et al., pp.765, IEDM201(Intel).

InGaAs FinFET, $L_{ch}=130$nm EOT 3.8nm
$V_{DS}=0.5$V (NUS)
H. –C. Chin et al., EDL 32, 2 (2011) (NUS)

Metal S/D InGaAs-OI, $L_{ch}= 55$nm, EOT 3.5nm
$V_{DS}=0.5$V (Tokyo Uni.)
S. H. Kim et al., pp.177, VLSI2012 (Tokyo Uni).

InAs Surface channel MOSFET, $L_{ch}=130$nm,
Dielectric: high- $k$  $V_{DS}=0.5$V (TSMC)

InGaAs QW Tri-gate, $L_{ch}=60$nm,
Dielectric: Al$_2$O$_3$/HfO$_2$  $V_{DS}=0.5$V (Sematech)

In$_{0.7}$Ga$_{0.3}$As FinFET, $L_{ch}=120$nm,
Dielectric: Al$_2$O$_3$/HfO$_2$  $V_{DS}=0.5$V (Penn State Uni.)

Recessed Channel Ge nMOSFET, $L_{ch}=60$nm,
Dielectric: Al$_2$O$_3$ $V_{DS}=0.5$V (Purdue Uni.)
H. Wu, et al., (Purdue Uni.) VLSI2014, p.82.

Regrown S/D In$_{0.7}$Ga$_{0.3}$As, $L_{ch}=40$nm,
Dielectric: Al$_2$O$_3$/HfO$_2$  $V_{DS}=0.5$V (Sematech)
Multi-gate III-V and Si benchmark (~2012)

nMOS

InGaAs GAA
$L_{ch}=50$nm, Dielectric: 10nm $\text{Al}_2\text{O}_3$
$V_{DS}=0.5V$ (Purdue Univ.) [1]

Si-FinFET 32nm
Intel $V_{DD}=0.8V$ [10]

InGaAs Tri-gate
$L_g=60$ nm, EOT 12A
$V_{DS}=0.5V$ (Intel) [2]

InGaAs FinFET
$L_{ch}=130$nm
EOT 3.8nm
$V_{DS}=0.5V$ (NUS)[3]

Si-FinFET 22nm
Intel $V_{DD}=0.8V$ [10]

InGaAs Nanowire
$L_g=200nm$, $T_{ox}$ 14.8nm
$V_{DS}=0.5V$ (Hokkaido Univ.)[4]

Si-bulk 45nm
Intel $V_{DD}=1V$[11]

Metal S/D InGaAs-OI
$L_{ch}=55$nm, EOT 3.5nm
$V_{DS}=0.5V$ (Tokyo Uni.)[5]

pMOS

GOI Tri-gate
$L_g$: 65nm, EOT 3.0nm
$V_D=-1V$ (AIST Tsukuba)[6]

Si-FinFET 22nm
Intel $V_{DD}=0.8V$ [10]

Ge FinFET
$L_g=4.5$ mm,
Dielectric: SiON, $V_{DS}=-1V$
(Stanford Uni.)[7]

Si-FinFET 32nm
Intel $V_{DD}=0.8V$ [10]

Ge GAA $L_g=300$nm,
dielectric: GeO$_2$(7nm)-HfO$_2$(10nm)
$V_D=-0.8V$ (ASTAR Singapore)[8]

Si-bulk 45nm
Intel $V_{DD}=1V$

Ge Tri-gate
$L_g=183$nm, EOT 5.5nm
$V_D=-1V$ (NNDL Taiwan)[9]

Si-bulk 45nm
Intel $V_{DD}=1V$

## III-V/Ge benchmark for various structures (2013 and 2014)

<table>
<thead>
<tr>
<th>Structure</th>
<th>$I_{ON}$ (mA/μm)</th>
<th>SS (mV/dec)</th>
<th>$L_{ch}$ (nm)</th>
<th>Dielectric/EOT</th>
<th>$V_{dd}$ (V)</th>
<th>DIBL (mV/V)</th>
<th>$G_{m\text{-max}}$ (μS/μm)</th>
<th>Peak Mobility (cm²/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ETB InGaAs-OI Tokyo Uni. 2013</td>
<td>0.2</td>
<td>187</td>
<td>5μm</td>
<td>Al₂O₃ 10nm</td>
<td>1</td>
<td>-</td>
<td>1500 (V&lt;sub&gt;DS&lt;/sub&gt;=0.5V)</td>
<td>-</td>
</tr>
<tr>
<td>Planar InAs TSMC 2013</td>
<td>0.6</td>
<td>85</td>
<td>130</td>
<td>-</td>
<td>0.5</td>
<td>40</td>
<td>2700 (V&lt;sub&gt;DS&lt;/sub&gt;=0.5V)</td>
<td>7100</td>
</tr>
<tr>
<td>Tri-Gate InGaAs SEMATECH 2013</td>
<td>0.5</td>
<td>77</td>
<td>60</td>
<td>Al₂O₃/HfO₂ 0.7nm/1.6nm</td>
<td>0.5</td>
<td>10</td>
<td>1500 (V&lt;sub&gt;DS&lt;/sub&gt;=0.5V)</td>
<td>760</td>
</tr>
<tr>
<td>QW FinFET InGaAs/InP IMEC 2014</td>
<td>0.36</td>
<td>190</td>
<td>50</td>
<td>HfO₂/Al₂O₃ EOT=1.9nm</td>
<td>0.5</td>
<td>-</td>
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## III-V/Ge benchmark for various structures

(2011 and 2012)

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<th>Planar (metal S/D, Strain, Buffer…)</th>
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<td>(V_D=~1V)</td>
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| Research Group                      |        |          |                       |          |
| Tokyo Uni VLSI 2012                 |        |          |                       |          |
| Tokyo Uni VLSI 2012                 |        |          |                       |          |
| Stanford Uni IEDM 2009              |        |          |                       |          |
| Stanford Uni ELD 2007               |        |          |                       |          |
| Intel IEDM 2011                     |        |          |                       |          |
| NNDL Taiwan IEDM 2011               |        |          |                       |          |
| Purdue Uni IEDM 2011                |        |          |                       |          |
| ASTAR Singapore IEDM 2009           |        |          |                       |          |
| Hokkaido Uni, IEDM 2011             |        |          |                       |          |
| AIST Tsukuba VLSI 2012              |        |          |                       |          |
7.2 T-FET technologies

(T: Tunnel)
Current status

Very small S-factor (21mV/dec) can be realized depending on the condition.

Very small $I_{on}$ (on-current) at low $V_d$ ($\sim 0.5$ V) is a big problem.

High $I_{on}$ can be obtained at high $V_d$ ($\sim 1$ V), but s-factor was more than 60 mV/dec.

Current problems/concerns

Large variation of $V_{th}$ is expected, because tunneling current is very sensitive to the small change of the size and structure of the junction.

Trap assisted tunneling would decreases the range of small s-factor region in $V_g$.

Change of $D_{it}$ (Interface state density) and $Q_{fix}$ (fixed charge) during long time operation would affect the characteristics $\rightarrow$ reliability concern.

Difficulty to realize idea structure in experiment, such as abrupt junction etc.

Expect improvement in future and more research reports.
Tunnel FET

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

Low $I_{OFF}$, Low $V_{DD}$, $SS < 60 \text{mV/decade}$
SS of TFET is function of $V_G$ due to Zener tunnel current

Minimum SS = 21 mV/dec is reached due to optimized series resistance of contact, undoped InAs and InAs/Si

$I_{ON}/I_{OFF} \approx 10^6$ at $V_{DS} = 1.0V$ (I\textsubscript{ON} = 1A/\mu m)
**I\textsubscript{ON} and I\textsubscript{OFF} of TFETs**

A.M. Ionescu, IEDM2013 Short Course (EPFL)
Q. Liu et al., pp.228, IEDM2013 (ST).
Y. Morita et al., pp. 236, VLSI2013 (AIST)

---

**Si, Ge TFET**
- 0.05 < V\textsubscript{DS} < 0.6 V
- 0.9 < V\textsubscript{DS} < 1.2 V

- SOI 14nm node (Lg=20nm) V\textsubscript{DD}=0.75V (ST)
- Tri-gate 22nm node (Lg=30nm)
- V\textsubscript{DD}=0.8V (Intel)
- Leonelli 2011 Si, silicides S/D
- Ghandi 2011 Si NW
- Villalon 2014 SiGe NW tri-gate
- Knoll 2012 strained Si NW tri-gate
- Knoll 2013 strained Si NW GAA
- Q. Huang 2011 Si NW tri-gate
- Q. Huang 2011 Si GAA
- MOSFET (IBM) 2012 Si/InAs
- Mayer 2008 Si
- Morita 2013 Si Fin
- Chang 2013 Si
- Jeon 2011 Si
- Moselund 2011 Si NW
- Q. Huang 2012 Si

**III-V TFET**
- 0.3 < V\textsubscript{DS} < 0.5 V
- 1.0 < V\textsubscript{DS} < 1.5 V

- Tri-gate 22nm node (Lg=30nm) V\textsubscript{DD}=0.8V (Intel)
- SOI 14nm node (Lg=20nm) V\textsubscript{DD}=0.75V (ST)
- Zhou 2012 InAs/GaAs
- Zhou 2012 InAs/GaSb
- Dey 2012 GaSb/InAs
- Zhou 2012 InGaAs
- Zhao 2011 InGaAs
- Li 2012 AlGaSb/InAs
- Mookerjea 2009 InGaAs
- Dewey (Intel) 2011 InGaAs
- Tomioka 2012 Si/InAs
- Schmid (IBM) 2011 Si/InAs
- Tomioka 2011 Si/InAs

---

- Si TFETs show the low I\textsubscript{OFF}, while I\textsubscript{ON} enhancement is still challenge.
- Strain is efficient for I\textsubscript{ON} enhancement in Si and Ge TFETs.
- III-V provide high I\textsubscript{ON}, however, suffer from unacceptably high I\textsubscript{OFF}. 110
Strained SiGe nanowire TFETs

- $I_{on}$ enhancement up to $760\mu A/\mu m$.
- Low bandgap of SiGe increase BTBT.
- SS lower than $60 \text{ mV/dec}$ is still challenge to be addressed.

A. Villalon et al., pp. 66, VLSI2014 (CEA-LETI)
7.3 2D channel material technologies
Why 2D channels?

- **High-drivability FinFET**
  - Large $W_{eff}/W_{footprint}$
    - Taller Fin
    - Narrow Fin pitch
  - Thinner Fin

- Mobility degradation in thin Si < 10 nm for both electron & hole.
  - **High-mobility 2D channels**

---


Family of 2D materials

Graphene
- 5.9

Silicene
- 3

Graphene family

Oxide family
- 2.7

Transition metal dichalcogenide (TMD) family
- 2.7

MX2
M: Cr, Mo, W, etc.
X: S, Se, Te, etc.

1.1
1.6
1.8
1.6
1.2
1.4
0.4

Si
MoSe2
MoTe2
WSe2
WS2
MoS2

Energy [eV]
Vacuum
- 7
Exfoliated single-layer MoS2 nMISFET

- 217 cm²/Vs, electron
- Depletion mode

B. Radisavljevic et al., Nature Nanotech. 6, 147 (2011)
7.4 Other emerging technologies
Other Emerging technologies

Carbon-based FET

Carbon nanotube

Graphene


A. D. Franklin et al., pp. 525, IEDM2011 (IBM)

GaAs mHEMT (20nm)

SiMOSET (29nm)

GaAs pHEMT (100nm)

Junctionless Transistor

J. P. Colinge et al., Nature Nano. 5(2010)225

All-spin logic device


Input and output related via Spin-coherent channel

J. P. Colinge et al., Nature Nano. 5(2010)266
8. Summary and conclusions
Summary and conclusions

Si-MOSFET is the main component nano-CMOS devices and will be so in future.

While the shrink rate of commercial node name will keep 0.7 for 2 years, the shrink rates of HP, $L_g$, $V_d$, $t_{ox}$, $t_{Si}$ are expected to be 0.80, 0.83, 0.96, 91 and 0.84, respectively, according to ITRS. Because of many reasons, the rate of physical shrinking will be smaller as the downsizing reach near the limit.

Increase of the $I_{off}$ due to subthreshold leakage and degradation of $I_{on}$ due to EOT and $t_{Si}$ reduction would limit the gate length scaling before $L_g$ reaches its limit of direct-tunneling ($@ L_g = \sim 3$nm).
Summary and conclusions (continued)

Problems and cost of the lithography and interconnects would also limit the downsizing.

There have been good challenges for the emerging technologies such as alternative channel, T-FET, 2D material and others. However, none of those technologies has yet reached the level for the industry to start R&D assuming mass production, such as yield, variability, reliability, large wafer production.
Acknowledgement

I would like to express appreciation to the following people for the great support for preparing the materials for the tutorial.

Slides for the 2D materials were made by Prof. Hitoshi Wakabayashi, Tokyo Institute of Technology.

Many slides except for the 2D materials were made by Dr. Takamasa Kawanago, Dr. Darius Zade, and Mr. Tomoya Shoji of Tokyo Institute of Technology, and Mr. Jing Neng Yao of National Chio Tung University.
Appendices
Appendices

Appendix 1. Process technologies for state of the art CMOS

Appendix 2. Alternative channel technologies

Appendix 3. T-FET technologies

Appendix 4. 2D channel material technologies

Appendix 5. Other emerging technologies
Appendix 1. Process technologies for state of the art CMOS

- Source/Drain formation
- Strain
- Gate Stack
- Others
- Source/Drain formation
Implant temperature has an impact on amorphization

Residual defects and dopant-defect complexes are formed at top-of-Fin and edge-of-Fin-side after Solid Phase Epitaxial Regrowth (SPER)
**Knock-in Doping Process** => Reduce amorphization/damage to Fins

- Deposition layer thickness important
- A single As ion can provide about 6 knocked-in As atoms for a 3keV 25° IADD process
- Sidewall doping by simultaneous deposition and knock-in with small angle implant is the key of the $I_{ON}$ boost
Heated Implantation with a-C mask (IMEC)

M. Togo et al., pp.T196, VLSI2013 (IMEC)

- **RT implantation (Upper)**
  - Forms amorphous layer
  - Residue twin defects at the corner after RTA

- **Heated implantation (Lower)**
  - a-Carbon mask (for high temp.)
  - No damage to fins after implantation

![Diagram](image_url)

### Results

- **Fin width: 15nm**
  - $I_{diff}$ vs $I_{on}$
    - RT imp
    - Heated imp

- **Imp dose/tilt: $1 \times 10^{15}$ cm$^{-2}$/45 deg**
  - $I_{diff}$ vs $I_{on}$

- **Long channel nFinFET**
  - All imp dose: $1 \times 10^{15}$ cm$^{-2}$
  - RT imp: 45 deg
  - RT imp: 10 deg
  - Heated imp: 10 deg
  - Heated imp tilt: 45 deg
Channel Doping to FinFETs for 22 nm (IBM)

C. -H. Lin et al., pp.15, VLSI2012 (IBM)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Vdd (V)</td>
<td>0.9</td>
</tr>
<tr>
<td>Lg (nm)</td>
<td>20-30</td>
</tr>
<tr>
<td>Gate Pitch (nm)</td>
<td>80-100</td>
</tr>
<tr>
<td>Fin Pitch (nm)</td>
<td>40</td>
</tr>
<tr>
<td>Dfin (nm)</td>
<td>12</td>
</tr>
<tr>
<td>Hfin (nm)</td>
<td>30</td>
</tr>
</tbody>
</table>

Channel doping ≤ $10^{18}$ cm$^{-3}$
⇒ Retain a variability advantage over planar technology
In situ Doped Source Drain Epitaxy for GAA (IBM)

S. Bangsaruntip et al., pp.526, IEDM2013 (IBM)

- Dopants placed right next to the spacer
- Equal diffusion distance of dopants to both the top and bottom of the NW
  \[ \Rightarrow \text{Reduced variation} \]
  \[ \Rightarrow \text{\sim} 30\% \text{ enhanced performance} \]
- Strain
- A strong degradation of the S/D stressors efficiency in reduced fin length
- Compressive STI keeps the performance variation
Unlike planar device, the n-FinFET drive current is also affected by mechanical stress.

TSV build-in stress affect both n and p-FinFET drive current with similar...
Epitaxial P-SiC Source/Drain Stressor (IMEC)

- Epitaxial Phosphorus doped SiC S/D stressor
- Narrower Fins and SiGe epitaxial growth on the Fins increase mobility
- Gate Stack
High-k/Metal Gate Stacks (IBM)

*M. M. Frank et al., pp.213, ECS Transactions 2014 (IBM)*

- SiO$_2$ interfacial layer helps optimize high-k/Si or high-k/SiGe interface quality.
- Interfacial layer thickness can be reduced by remote oxygen scavenging.

Remote oxygen scavenging
Positively charged oxygen vacancies ($V_o$) are generated only when $\text{TIN} \geq T_{crit}$.

Optimized
- Metal (TiN) thickness
- WF-setting annealing

$\Rightarrow$ 9nm more $L_g$ scaling with matched gate resistance

$\Rightarrow$ Aggressive $L_g$ scaling toward the 14 nm node and beyond
- $V_T$ modulation and minimized $\sigma(R_{\text{gate}})$ using ultra-thin TiN/TaN layers, grown for optimum Al diffusion control properties on HfO$_2$ and Co$_x$Al$_y$ fill-metal

- >500mV $\Delta V_T$ enabled low-$V_T$ FinFET NMOS with improved mobility, noise and reliability
L. Ragnarsson et al., pp.27, VLSI2012 (IMEC)

- Doped the HfO$_2$ by alternating ALD cycles of HfO$_2$ and metal oxides (MO$_{x}$)
  ⇒ EOT-scaling by increasing k-value

- Reduced Jg by 2 to 3 orders of magnitude at the cost of mobility reduction, however.
Low Resistance Co-Al Gate Fill for 20 nm node (IBM)

U. Kwon et al., pp.29, VLSI2012 (IBM)

Co-Al Gate Fill
(Al- Blue, Co-Pink)

Low resistance gate formation at smaller than $L_{gate} = 25$ nm
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band offset

Oxide

Si

Dielectric Constant $\varepsilon(0)$

Band Discontinuity [eV]

-6
-4
-2
0
2
4

Si Band Gap

$\text{SiO}_2$

$\text{Gd}_2\text{O}_3$

$\text{La}_2\text{O}_3$

$\text{Lu}_2\text{O}_3$

$\text{HfO}_2$

$\text{ZrO}_2$

XPS measurement by Prof. T. Hattori, INFOS 2003
Direct high-k/Si by silicate reaction

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface
Control of oxygen partial pressure is the key for processing.

$P_{O_2}$: Partial pressure of O$_2$ during high temperature annealing
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

\[
\text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2
\]

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Tans. ECS 11, 319

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Physical mechanisms for small Dit

① silicate-reaction-formed fresh interface

② stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress


However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Our Work at TIT: High-k

Our result at TIT

EOT = 0.40 nm

L/W = 5/20 μm
T = 300 K
N_sub = 3 × 10^{16} cm^{-3}

Electron Mobility [cm^2/Vsec]
Benchmark of La-silicate dielectrics

**Gate Leakage current**
- ITRS requirement
- Our data: La-silicate gate oxide

**Effective Mobility**
- Solid circle: Our data
- La-silicate gate oxide
- Open square: Hf-based oxides

*T. Ando, et al., (IBM) IEDM 2009, p.423*
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{\text{th}}$ control
- Interface dipole control for $V_{\text{th}}$ tuning
- Suppression of FLP
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
- Control of interface reaction and Si diffusion to high-k
- Suppression of gate leakage current
- Reliability: PBTI, NBTI, TDDB
- Flat metal/high-k interface for better mobility
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Small interfacial state density at high-k/Si
- Others
Variability and Parameter Correlations in FinFETs (GF)

A. Paul et al., pp.361, IEDM2013 (GF)

$I_{eff}$ variability is captured by the independent variations in $V_{tlin}$, $R_{ext}$ and $Gm$

- $R_{ext}$: External Resistance
- $Gm_{max}$: Maximum Transconductance
- $V_{tlin}$: Threshold Voltage

Increase in $I_{eff}$ variability

Effects on $I_{eff}$ variation

- $V_{tlin}$: more dominant in nFETs > pFETs
- $Gm$: Major contributor
  => Improve surface properties (e.g. H$_2$ bake)
- $R_{ext}$: Increases in larger $N_{fin}$
  => Improve S/D contacts
The ballisticity, self-heating, and temperature profiles of ultra-scaled Si NWFETs have been computed through coupled electro-thermal transport simulation.

Large temperature increase at drain side => Current decrease

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$L_g=15$ nm</th>
<th>$L_g=5$ nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage $V_{DD}$ (V)</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td>Ballisticity of $I_{ON}$ (%)</td>
<td>&lt;45</td>
<td>&lt;55</td>
</tr>
<tr>
<td>Ballisticity of $I_{OFF}$ (%)</td>
<td>70</td>
<td>94</td>
</tr>
<tr>
<td>Self-heating reduction of $I_{ON}$ (%)</td>
<td>35</td>
<td>29</td>
</tr>
<tr>
<td>Self-heating reduction of $I_{OFF}$ (%)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Maximum temperature $I_{ON}$ (K)</td>
<td>510</td>
<td>490</td>
</tr>
<tr>
<td>Maximum temperature $I_{OFF}$ (K)</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>Heat dissipated $I_{ON}$ ($\mu$W)</td>
<td>1.22</td>
<td>1.08</td>
</tr>
<tr>
<td>Heat dissipated $I_{OFF}$ (pW)</td>
<td>$\sim$5</td>
<td>$\sim$5</td>
</tr>
</tbody>
</table>
The time constant for self heating is much longer than characteristic switching times of CMOS logic and memory.

In special cases (e.g. analog I/O, ESD), the same design practices as used with planar devices can be applied.
Cumulative $\Delta V_t$ map of RTN shows that RTN in high-k/metal gate nFETs tends to be capture limited at normal supply voltage.

Thermal barrier of capture/emission shows little correlation to $V_g$ coupling.
Appendix 2

Alternative channel technologies
<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>electron mob. (cm²/Vs)</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
</tr>
<tr>
<td>electron effective mass</td>
<td>m_t: 0.19 m_1: 0.916</td>
<td>m_t: 0.082 m_1: 1.467</td>
<td>0.067</td>
<td>0.08</td>
<td>0.026</td>
<td>0.0135</td>
</tr>
<tr>
<td>hole mob. (cm²/Vs)</td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td>hole effective mass</td>
<td>m_{HH}: 0.49 m_{LH}: 0.16</td>
<td>m_{HH}: 0.28 m_{LH}: 0.044</td>
<td>m_{HH}: 0.45 m_{LH}: 0.082</td>
<td>m_{HH}: 0.45 m_{LH}: 0.12</td>
<td>m_{HH}: 0.57 m_{LH}: 0.35</td>
<td>m_{HH}: 0.44 m_{LH}: 0.016</td>
</tr>
<tr>
<td>band gap (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.14</td>
</tr>
<tr>
<td>permittivity</td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

- **Ge** ⇒ lightest hole $m^*$ (light electron $m^*$) ⇒ pMOS (CMOS)
- **III-V** ⇒ light electron $m^*$ ⇒ nMOS
- **GaAs•InP** ⇒ $E_g$ higher than that in Si ⇒ low power

*S. Takagi., IEDM2011, Short course (Tokyo Uni)*
### ITRS 2011 for III-V/Ge

*Manufacturing solutions are NOT known*

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2018</th>
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<tbody>
<tr>
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<td>9.3</td>
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<td>5.8</td>
</tr>
<tr>
<td>$V_{dd}$ (V)</td>
<td>0.63</td>
<td>0.61</td>
<td>0.58</td>
<td>0.56</td>
<td>0.54</td>
</tr>
<tr>
<td>$EOT$ (nm)</td>
<td>0.68</td>
<td>0.62</td>
<td>0.56</td>
<td>0.50</td>
<td>0.45</td>
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**Mobility enhancement factor due to channel material**

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<th>Ge</th>
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<tbody>
<tr>
<td>$C_g$ Ideal (fF/µm)</td>
<td>0.28</td>
<td>0.41</td>
</tr>
<tr>
<td>$V_{t,sat}$ (mV)</td>
<td>229</td>
<td>230</td>
</tr>
<tr>
<td>$CV/I$ (ps)</td>
<td>0.13</td>
<td>0.21</td>
</tr>
</tbody>
</table>

**Ideal (fF/µm)**

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</tr>
</tbody>
</table>

*http://www.itrs.net/Links/2011ITRS/Home2011.htm*
## ITRS 2011 for III-V/Ge, Contd


<table>
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</tr>
<tr>
<td>Equivalent Injection velocity $V_{inj}$ ($10^7$ cm/s)</td>
<td>II-V</td>
<td>4.29</td>
<td>4.58</td>
<td>5.32</td>
<td>5.93</td>
</tr>
<tr>
<td></td>
<td>Ge</td>
<td>2.26</td>
<td>2.44</td>
<td>2.86</td>
<td>3.19</td>
</tr>
<tr>
<td>$I_{d,sat}$ (mA/μm)</td>
<td>II-V</td>
<td>2.200</td>
<td>2.343</td>
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<tr>
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<td>Ge</td>
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<td>2.330</td>
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<tr>
<td>$I_{sd,leak}$ (nA/μm)</td>
<td></td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>$R_{sd}$ (Ω-μm)</td>
<td>II-V</td>
<td>131</td>
<td>113</td>
<td>96</td>
<td>82</td>
</tr>
<tr>
<td></td>
<td>Ge</td>
<td>149</td>
<td>126</td>
<td>105</td>
<td>85</td>
</tr>
<tr>
<td>$CV^2$ (fJ/μm)</td>
<td>II-V</td>
<td>0.18</td>
<td>0.15</td>
<td>0.13</td>
<td>0.11</td>
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<tr>
<td></td>
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Manufacturing solutions are **NOT** known.
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<table>
<thead>
<tr>
<th>Manufacturing solutions available</th>
<th></th>
<th>Manufacturing solutions not known</th>
</tr>
</thead>
<tbody>
<tr>
<td>exists or being optimized</td>
<td></td>
<td></td>
</tr>
<tr>
<td>are known</td>
<td></td>
<td></td>
</tr>
<tr>
<td>are <strong>NOT</strong> known</td>
<td></td>
<td></td>
</tr>
</tbody>
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**ITRS 2013 for III-V/Ge**

In span of two years (compared to ITRS 2011) significant improvements in alternative channel device performance has been achieved and manufacturing solutions provided.

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<td>126</td>
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<td>85</td>
<td>72</td>
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<tr>
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<td></td>
<td></td>
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<td>0.23</td>
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<td>0.16</td>
<td>0.14</td>
<td>0.11</td>
</tr>
</tbody>
</table>

Manufacturing solutions exist or being optimized

Manufacturing solutions are known

Manufacturing solutions are **NOT** known

[http://www.itrs.net/Links/2013ITRS/Home2013.htm](http://www.itrs.net/Links/2013ITRS/Home2013.htm)
### III-V/Ge benchmark for various structures (2013 and 2014)

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Fabrication</th>
<th>Substrates</th>
<th>$I_{ON}$ (mA/μm)</th>
<th>SS (mV/dec)</th>
<th>$L_{ch}$ (nm)</th>
<th>Dielectric/EOT</th>
<th>$V_{dd}$ (V)</th>
<th>DIBL (mV/V)</th>
<th>$G_{m-max}$ ($\mu$S/$\mu$m)</th>
<th>Peak Mobility (cm$^2$/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ETB InGaAs-OI</td>
<td>Tokyo Uni. 2013</td>
<td>InGaAs</td>
<td>0.2</td>
<td>187</td>
<td>5μm</td>
<td>Al$_2$O$_3$ 10nm</td>
<td>1</td>
<td>-</td>
<td>1500 (V$_{DS}$=0.5V)</td>
<td>-</td>
</tr>
<tr>
<td>Planar InAs</td>
<td>TSMC 2013</td>
<td>InAs</td>
<td>0.6</td>
<td>85</td>
<td>130</td>
<td>-</td>
<td>0.5</td>
<td>40</td>
<td>2700 (V$_{DS}$=0.5V)</td>
<td>7100</td>
</tr>
<tr>
<td>Tri-Gate InGaAs</td>
<td>SEMATECH 2013</td>
<td>InGaAs</td>
<td>0.5</td>
<td>77</td>
<td>60</td>
<td>Al$_2$O$_3$/HfO$_2$ 0.7nm/1.6nm</td>
<td>0.5</td>
<td>10</td>
<td>1500 (V$_{DS}$=0.5V)</td>
<td>760</td>
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<tr>
<td>QW FinFET InGaAs/InP</td>
<td>IMEC 2014</td>
<td>InGaAs/InP</td>
<td>0.36</td>
<td>190</td>
<td>50</td>
<td>HfO$_2$/Al$_2$O$_3$ EOT=1.9nm</td>
<td>0.5</td>
<td>-</td>
<td>450 (V$_{DS}$=0.5V)</td>
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<tr>
<td>Regrown S/D In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>SEMATECH 2014</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>1</td>
<td>105</td>
<td>40</td>
<td>HfO$_2$/Al$_2$O$_3$ 3nm/0.7nm</td>
<td>0.5</td>
<td>150</td>
<td>2000 (V$_{DS}$=0.5V)</td>
<td>5500</td>
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<tr>
<td>FinFET InGaAs (In 70%)</td>
<td>Penn State Uni. 2014</td>
<td>InGaAs (In 70%)</td>
<td>1.16</td>
<td>236</td>
<td>120</td>
<td>HfO$_2$/Al$_2$O$_3$ 3nm/1nm</td>
<td>0.5</td>
<td>119</td>
<td>1900 (V$_{DS}$=0.5V)</td>
<td>3000</td>
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<tr>
<td>Recessed channel Ge</td>
<td>Purdue Uni. 2014</td>
<td>Ge</td>
<td>0.55</td>
<td>-</td>
<td>60</td>
<td>Al$_2$O$_3$ 8nm</td>
<td>0.5</td>
<td>-</td>
<td>600 (V$_{DS}$=0.5V)</td>
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<td>QW MOSFET InGaAs</td>
<td>IMEC 2014</td>
<td>InGaAs</td>
<td>0.55</td>
<td>82</td>
<td>100</td>
<td>Al$_2$O$_3$ EOT=1.1nm</td>
<td>0.5</td>
<td>-</td>
<td>2000 (V$_{DS}$=0.5V)</td>
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<tr>
<td>CMOS InGaAs-OI</td>
<td>GNC 2014</td>
<td>InGaAs</td>
<td>0.05</td>
<td>80</td>
<td>10μm</td>
<td>Al$_2$O$_3$ 7.8nm</td>
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<td>CMOS SGOI</td>
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<td>0.02</td>
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<td>HfO$_2$ 4.5nm</td>
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<td>CMOS La$_2$O$_3$/GaAs nFET</td>
<td>Purdue Uni. 2014</td>
<td>La$_2$O$_3$/GaAs</td>
<td>0.15</td>
<td>74</td>
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<td>La$_2$O$_3$/Al$_2$O$_3$ 8nm/6nm</td>
<td>2</td>
<td>-</td>
<td>-</td>
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<td>CMOS La$_2$O$_3$/GaAs pFET</td>
<td>Purdue Uni. 2014</td>
<td>La$_2$O$_3$/GaAs</td>
<td>0.015</td>
<td>270</td>
<td>1μm</td>
<td>La$_2$O$_3$/Al$_2$O$_3$ 8nm/6nm</td>
<td>-2</td>
<td>-</td>
<td>-</td>
<td>1620</td>
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</table>
### III-V/Ge benchmark for various structures

(2011 and 2012)

<table>
<thead>
<tr>
<th>Planar (metal S/D, Strain, Buffer...)</th>
<th>FinFET</th>
<th>Tri-gate</th>
<th>Gate-all-around MOSFET</th>
<th>Nanowire</th>
</tr>
</thead>
<tbody>
<tr>
<td>material</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>InGaAs</td>
<td>Ge</td>
<td>InGaAs</td>
<td>Ge</td>
<td>InGaAs (multishell)</td>
</tr>
<tr>
<td>Al&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;3&lt;/sub&gt;/3.5 nm</td>
<td>7.6 Å &lt;sup&gt;o&lt;/sup&gt;</td>
<td>5nm ALD Al&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;3&lt;/sub&gt;</td>
<td>SiON</td>
<td>HfO&lt;sub&gt;2&lt;/sub&gt;: 11nm</td>
</tr>
<tr>
<td>Mobility</td>
<td>~600 (cm&lt;sup&gt;2&lt;/sup&gt;/Vs)</td>
<td>~700 (µS/µm)</td>
<td>-</td>
<td>~500 (µS/µm)</td>
</tr>
<tr>
<td>L&lt;sub&gt;ch&lt;/sub&gt; (nm)</td>
<td>55</td>
<td>W/L=30/5 µm</td>
<td>100</td>
<td>180</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>84</td>
<td>-</td>
<td>145</td>
<td>150</td>
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<tr>
<td>SS (mV/dec)</td>
<td>105</td>
<td>-</td>
<td>145</td>
<td>150</td>
</tr>
<tr>
<td>I&lt;sub&gt;ON&lt;/sub&gt; (µA/µm)</td>
<td>278 (V&lt;sub&gt;D&lt;/sub&gt;=0.5V)</td>
<td>4 (n,p) (V&lt;sub&gt;D&lt;/sub&gt;=0.5V)</td>
<td>-</td>
<td>10 (V&lt;sub&gt;D&lt;/sub&gt;=0.5V)</td>
</tr>
</tbody>
</table>

**III-V/Ge benchmark for various structures (2011 and 2012)**

- **Planar (metal S/D, Strain, Buffer...)**
- **FinFET**
- **Tri-gate**
- **Gate-all-around MOSFET**
- **Nanowire**

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</tr>
</tbody>
</table>
Multi-gate III-V and Si benchmark

---

- **InGaAs GAA**, $L_{ch}=50\text{nm}$, **Dielectric**: $10\text{nm Al}_2\text{O}_3$, $V_{DS}=0.5\text{V}$ (Purdue Uni.)
  - J. J. Gu et al., pp.769, IEDM2011 (Purdue).

- **InGaAs Tri-gate**, $L_g=60\text{ nm}, EOT\ 12\text{A}$
  - $V_{DS}=0.5\text{V}$ (Intel)
  - M. Radosavljevic et al., pp.765, IEDM201(Intel).

- **InGaAs FinFET**, $L_{ch}=130\text{nm} EOT\ 3.8\text{nm}$
  - $V_{DS}=0.5\text{V}$ (NUS)

- **Metal S/D InGaAs-OL**, $L_{ch}= 55\text{nm}, EOT\ 3.5\text{nm}$
  - $V_{DS}=0.5\text{V}$ (Tokyo Uni.)
  - S. H. Kim et al., pp.177, VLSI2012 (Tokyo Uni).

- **InAs Surface channel MOSFET**, $L_{ch}=130\text{nm}$, **Dielectric**: high-$k$ $V_{DS}=0.5\text{V}$ (TSMC)

- **InGaAs QW Tri-gate**, $L_{ch}=60\text{nm}$, **Dielectric**: $\text{Al}_2\text{O}_3/\text{HfO}_2$ $V_{DS}=0.5\text{V}$ (Sematech)

- **In$_{0.7}$Ga$_{0.3}$As FinFET**, $L_{ch}=120\text{nm}$, **Dielectric**: $\text{Al}_2\text{O}_3/\text{HfO}_2$ $V_{DS}=0.5\text{V}$ (Penn State Uni.)

- **Recessed Channel Ge nMOSFET**, $L_{ch}=60\text{nm}$, **Dielectric**: $\text{Al}_2\text{O}_3$ $V_{DS}=0.5\text{V}$ (Purdue Uni.)
  - H. Wu, et al., (Purdue Uni.) VLSI2014, p.82.

- **LP InGaAs QW MOSFET**, $L_{ch}=100\text{nm}$, **Dielectric**: $\text{Al}_2\text{O}_3$ $V_{DS}=0.5\text{V}$ (IMEC)

---

Multi-gate III-V and Si benchmark (~2012)

nMOS

InGaAs GAA
$L_{ch}=50$nm, Dielectric: $10$nm $\text{Al}_2\text{O}_3$
$V_{DS}=0.5$V (Purdue) [1]

Si-FinFET 32nm
Intel $V_{DD}=0.8$V [10]

InGaAs Tri-gate
$L_g=60$ nm, EOT 12A
$V_{DS}=0.5$V (Intel) [2]

Si-FinFET 22nm
Intel $V_{DD}=0.8$V [10]

InGaAs FinFET
$L_{ch}=130$nm
EOT 3.8nm
$V_{DS}=0.5$V (NUS) [3]

Si-bulk 45nm
Intel $V_{DD}=1$V [11]

InGaAs Nanowire
$L_g=200$nm, $T_{ox}=14.8$nm
$V_{DS}=0.5$V (Hokkaido Uni.) [4]

Ge FinFET
$L_g=4.5$ nm,
Dielectric: SiON, $V_{DS}=-1$V
(Stanford Uni.) [7]

Ge GAA $L_g=300$nm,
dielectric: GeO$_2$(7nm)-HfO$_2$(10nm)
$V_D=-0.8$V (ASTAR Singapore) [8]

Ge Tri-gate
$L_g=183$nm, EOT 5.5nm
$V_D=-1$V (NNDL Taiwan) [9]

Si-bulk 45nm
Intel $V_{DD}=1$V

pMOS

GOI Tri-gate
$L_g=65$nm, EOT 3.0nm
$V_D=-1$V (AIST Tsukuba) [6]

Si-FinFET 22nm
Intel $V_{DD}=0.8$V [10]

Si-FinFET 32nm
Intel $V_{DD}=0.8$V [10]

Si-bulk 45nm
Intel $V_{DD}=1$V

Si-bulk 45nm
Intel $V_{DD}=1$V

Si-bulk 45nm
Intel $V_{DD}=1$V

Si-bulk 45nm
Intel $V_{DD}=1$V

Si-bulk 45nm
Intel $V_{DD}=1$V

Si-bulk 45nm
Intel $V_{DD}=1$V

Multi-gate III-V and Si benchmark (~2012)

Recently various device structures have been demonstrated on InGaAs platform for achieving higher performance at lower power supply.

Improvement in high-k/III-V interface and III-V growth technology has been a key factor.
Outline

Alternative channel n-FETs
- Gate Stack
- On Insulator (OI) MOSFETs
- Fin, Tri-Gate, Nanowire (GAA) MOSFET

Ge channel p-FETs
- Planar MOSFET
- Tri-Gate, Nanowire, Recessed Channel

Hybrid CMOS
Alternative channel n-FETs

- Gate Stack
- On Insulator (OI) MOSFETs
- Fin, Tri-Gate, Nanowire (GAA) MOSFET

Ge channel p-FETs

- Planar MOSFET
- Tri-Gate, Nanowire, Recessed Channel

Hybrid CMOS
Implementing high-k material to III-V, Ge

III-V (InGaAs, InAs, InGaSb, …)

- ALD-Al$_2$O$_3$ is most commonly used as gate dielectric in planar or Multi-gate
- HfO$_2$-only stacks have high $D_{it}$ (combination of Al$_2$O$_3$ or Al or Si is used)

**Ge**

- By controlling the formation of GeO$_x$ at the interface, HfO$_2$ and Al$_2$O$_3$ show good results.
Alternative channel n-FETs
- Gate Stack
- On Insulator (OI) MOSFETs
- Fin, Tri-Gate, Nanowire (GAA) MOSFET

Ge channel p-FETs
- Planar MOSFET
- Tri-Gate, Nanowire, Recessed Channel

Hybrid CMOS
Metal S/D and InAs buffer layer are used as performance boosters.

- **DIBL=84 mV/V** and **SS=105 mV/V** was shown for \( L_{ch} = 55 \text{ nm} \) when In-content was higher.

---

S. H. Kim et al., pp.177, VLSI2012 (Tokyo Uni)
Strained InGaAs-OI layer on Si by DWB (direct wafer bonding) with optional CMP.

MOSFET with 1.7% tensile strain exhibits 1.65x effective mobility enhancement against InGaAs without strain with high $I_{on}/I_{off}$ ratio~$10^5$. 
Outline

Alternative channel n-FETs
- Gate Stack
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- Fin, Tri-Gate, Nanowire (GAA) MOSFET

Ge channel p-FETs
- Planar MOSFET
- Tri-Gate, Nanowire, Recessed Channel

Hybrid CMOS
Using the STI aspect ratio trapping (ART) technique to introduce high mobility channel to Si CMOS platform. Record performance:

$I_{on}=601\mu A/\mu m$ at $I_{off}=100nA/\mu m$ ($V_d=0.5V$)

$g_{m,ext}=2.72mS/\mu m$

$S=85mV/dec$ & $DIBL=40mV/V$

resulting from breakthroughs in epitaxy and III-V/dielectric interface engineering.
\[ \text{DIBL} = 135 \text{ mV/V and drive current} \]
\[ \text{over 840 } \mu \text{A/\mu m at } L_{ch} = 130 \text{nm} \]
\[ \text{and } V_{ds} = 1.5V \text{ was achieved} \]
Tri-gate InGaAs QW-FET (Intel)


- Tri-gate structure has superiority electrostatic controllability compared to ultra-thin body planar structure
- Steepest SS and smallest DIBL ever reported ($W_{\text{fin}} = 30\text{nm}$)
Process flow of InGaAs fin formation using the replacement fin process.

A CET value of 1.9nm is extracted from a MOSCAP test structure.
Performance:
SS = 190 mV/dec
$g_{m,ext} = 558 \mu S/ \mu m$
EOT = 1.9nm

High-k last processing outperforms High-k first processing in an RMG flow.
InGaAs QW Tri-Gate (EOT, 1.0nm)


Performance at $V_{ds} = 0.5V$
$SS = 77mV/dec$
$DIBL = 10 mV/V$
$g_{m,max} > 1.5mS/\mu m$

BEST balance of $g_{m,max}$ and SS!
Gate last InGaAs QW FET

Performance:
- $SS=80\text{mV/dec.}$
- $DIBL=22\text{mV/V}$
- $\mu_{n,\text{eff}}>5,500 \text{ cm}^2/\text{V-s}$ at $300\text{k}$

Further device optimization in the form of self-aligned S/D contact will improve $g_{m,\text{max}}$ at short-channel devices.
Best planar InGaAs-channel MOSFETs attributing to InAlAs buffer, III-V/oxide interface engineering and S/D regrowth.

Performance at $V_{ds}=0.5\text{V}$ ($L_g=100\text{nm}$ $EOT=1.1\text{nm}$):
- $I_{on}=550\mu\text{A/\mu m}$ @ $I_{off}=100\text{nA/\mu m}$
- $g_{m,ext}=2.12\text{mS/\mu m}$
- $SS=82\text{mV/dec}$
Gate all around InGaAs MOSFET (Purdue)


- Inversion mode $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFET with ALD $\text{Al}_2\text{O}_3$/WN with well electrostatic properties

- DIBL was suppressed down to $L_{ch} = 50\text{nm}$ and $G_{m,\text{max}} = 701\text{mS/mm}$ at $V_{ds} = 1\text{V}$
Core-multishell InGaAs nanowires grown without buffer layer on Si substrate (bottom up approach)

At $V_d = 1$ V peak transconductance of 500 mS/mm is achieved (roughly x3 InGaAs nanowire)
Outline

Alternative channel n-FETs
- Gate Stack
- On Insulator (OI) MOSFETs
- Fin, Tri-Gate, Nanowire (GAA) MOSFET

Ge channel p-FETs
- Planar MOSFET
- Tri-Gate, Nanowire, Recessed Channel

Hybrid CMOS
Ge pMOSFET with TaN/ZrO$_2$/Zr-cap/Ge(100) gate stack.

Performance:
Extremely low leakage: 250nA/cm$^2$
Extremely low EOT ~ 0.6nm
Low SS = 70mV/dec

Low hole mobility ~ 110cm$^2$/Vs!
Selective etching of high defect Ge near Ge/Si interface is used which improves gate controllability.

- $I_{ON}/I_{OFF} = 10^5$ and $SS= 130 \text{ mV/dec}$
- $I_{ON}= 235 \mu m/\mu m$ at $V_D= -1V$
Ge-nanowire pMOSFET (AIST, Tsukuba)


Using Ni-Ge alloy as metal S/D
Significantly reduces contact resistance

High saturation current and high mobility

\[ \mu_{\text{eff}} = 855 \text{ cm}^2/\text{Vs} \text{ at } N_s = 5 \times 10^{12} \text{cm}^{-2} \]
and saturation drain current of

\[ 731 \mu\text{A}/\mu\text{m at } V_d = -1\text{V} \]
Recessed channel Ge nMOSFET

Record performance (at $L_{ch} = 60$nm):

$I_{\text{max}} = 714$mA/mm

$g_{\text{max}} = 590$mS/mm

$I_{\text{on}}/I_{\text{off}}$ ratio = $1E5$
Alternative channel n-FETs
- Gate Stack
- On Insulator (OI) MOSFETs
- Fin, Tri-Gate, Nanowire (GAA) MOSFET

Ge channel p-FETs
- Planar MOSFET
- Tri-Gate, Nanowire, Recessed Channel

Hybrid CMOS
Common InGaAs-GeSn gate stack (NUS)

- Common gate stack (gate metal and dielectric) were used for both p- and n-type
- Si$_2$H$_6$ plasma passivation is employed which creates Si layer at interface.
- High intrinsic peak $G_{M,Sat} = \sim 465 \mu S/\mu m$ at $V_{DS} = -1.1$ V was achieved for $L_G = 250$ nm.

**SS:** nMOS: 90 (mV/decade)

**pMOS:** 190 (mV/decade)

$V_{GS} - V_{TH} = 0 \sim 2.0$ V

$L_G = 5 \mu m$
InGaSb as channel material (stanford)

Z. Yuan et al., pp.185, VLSI2012 (Stanford Uni)

Achieving both N- and P-type MOSFET on a single channel is possible

In-content of 20-40% improves performance

electron/hole mobility > 4000/900 cm²/Vs was gained in a single channel material

I_{ON} at L_G = 50 µm
pMOS: 4 µA/µm
nMOS: 3.8 µA/µm
First dual channel CMOS inverters composed of InGaAs nFETs and Ge pFETs utilizing stacked 3D integration.

No degradation of Ge pFETs after InGaAs nFETs processing!

Mobility enhancement of 2.6x and 3.0x for InGaAs nFETs and Ge pFETs against Si FETs respectively.

Inverter, successful down to $V_{dd}=0.2V$!
Schematic of fabricated ultimate CMOS structure composed of InGaAs-OI/SGOI wire channel MOSFET w/ independent back gate.

Mobility enhancement of 2.3x and 2.4x in InGaAs nMOSFET and SG-OI pMOSFET against Si MOSFET.

Inverter w/ high gain as $V_{dd}$ down to 0.2V.
Using DWB (direct wafer bonding) to get hybrid dual channel ETXOI substrate.

First co-integration of co-planar SiGe pFETs (65nm) and InGaAs nFETs (40nm). Height difference only 17nm!
InAs/GaSb CMOS


(a) Difficult to integrate due to the material difference, InGaAs and GaSb.

(b) Newly proposed single channel III-V CMOS on Si with UTB InAs/GaSb-OI layer.

Hole mobility of GaSb-OI PFET can exceed Si PFET as $(T_{\text{InAs}}, T_{\text{GaSb}}) = (2.5\text{nm}, 20\text{nm})$.

Electron mobility of InAs-OI NFET can exceed Si NFET as $(T_{\text{InAs}}, T_{\text{GaSb}}) = (5\text{nm}, 20\text{nm})$. 

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La2O3/GaAs CMOS

Flat and sharp interface.

GaAs CMOS inverter: a gain of ~12 is achieved with $V_{DD}=3V$.

Mobility in moderate $N_{inv}$ slightly increased due to less phonon scattering and the decreasing at low $N_{inv}$ is by the influence of Coulomb scattering.

Oscillation frequency increase from 0.35-3.87MHz as $V_{DD}$ from 1 – 2.75V.

Dit greatly reduced compared to amorphous $Al_2O_3$/GaAs interface.
Appendix 3

T-FET technologies
Tunnel FET

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

Low $I_{OFF}$, Low $V_{DD}$, $SS < 60$ mV/decade
Si, Ge TFETs show the low $I_{\text{off}}$, while $I_{\text{on}}$ enhancement is still challenge.

Strain is efficient for $I_{\text{on}}$ enhancement in Si and Ge TFETs.

III-V provide high $I_{\text{on}}$, however, suffer from unacceptably high $I_{\text{off}}$. 

- Si TFETs show the low $I_{\text{off}}$, while $I_{\text{on}}$ enhancement is still challenge.
- Strain is efficient for $I_{\text{on}}$ enhancement in Si and Ge TFETs.
- III-V provide high $I_{\text{on}}$, however, suffer from unacceptably high $I_{\text{off}}$. 

A.M. Ionescu, IEDM2013 Short Course (EPFL)
Q. Liu et al., pp.228, IEDM2013 (ST).
Y. Morita et al., pp. 236, VLSI2013 (AIST)

L. Knoll et al., pp. 100, IEDM2013 (Jülich)
A. Villalon et al., pp. 66, VLSI2014 (CEA-LETI)
C. Auth et al., pp.131, VLSI2012 (Intel).
The highest current is in the range of 1 ~ 10 nA/μm accompanied by sub-threshold swing below 60 mV/dec.
## Tunnel FET performance comparison

**A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)**

measured III-V channel TFETs

<table>
<thead>
<tr>
<th>Reference</th>
<th>Source</th>
<th>Channel</th>
<th>Dielectric</th>
<th>EOT (nm)</th>
<th>$I_{ON}$ (µA/µm)</th>
<th>$V_{DS}$ (V)</th>
<th>$V_{GS}=V_{ON}$ (V)</th>
<th>$V_{ON}-V_{OFF}$ (V)</th>
<th>$I_{ON}/I_{OFF}$</th>
<th>$S_{MIN}$ (mV/dec)</th>
<th>$S_{EFF}$ (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>this work</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.6</td>
<td>78</td>
<td>0.5</td>
<td>0.5</td>
<td>1.5</td>
<td>2,000</td>
<td>125</td>
<td>230</td>
</tr>
<tr>
<td>Li [4]</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$</td>
<td>3.9</td>
<td>20</td>
<td>0.3</td>
<td>2</td>
<td>6</td>
<td>210</td>
<td>830</td>
<td>1300</td>
</tr>
<tr>
<td>Mookerjea [5]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>5.6</td>
<td>10</td>
<td>0.5</td>
<td>2.5</td>
<td>2.5</td>
<td>10,000</td>
<td>240</td>
<td>310</td>
</tr>
<tr>
<td>Mohata [6]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>2.8</td>
<td>10</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>400,000</td>
<td>200</td>
<td>180</td>
</tr>
<tr>
<td>Zhao [7]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>20</td>
<td>0.45</td>
<td>1</td>
<td>1.5</td>
<td>30,000</td>
<td>86</td>
<td>170</td>
</tr>
<tr>
<td>Zhao [8]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>40</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>200,000</td>
<td>84</td>
<td>190</td>
</tr>
<tr>
<td>Ford [9]</td>
<td>InAs</td>
<td>InAs</td>
<td>ZrO$_2$</td>
<td>2</td>
<td>0.4</td>
<td>0.5</td>
<td>1</td>
<td>1</td>
<td>200</td>
<td>190</td>
<td>220</td>
</tr>
<tr>
<td>Zhou [10]</td>
<td>InP</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$,In$_{0.47}$As</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.3</td>
<td>20</td>
<td>0.5</td>
<td>1</td>
<td>1.75</td>
<td>450,000</td>
<td>93</td>
<td>150</td>
</tr>
</tbody>
</table>

**$S_{MIN}$:** Most common SS which is the inverse of $I_D-V_{GS}$ slope at the steepest part

**$S_{EFF}$:** Is the average swing when $V_{TH}=V_{DD}/2$, $V_{OFF}=0$

**Average SS:**

$$
V_{TH} - V_{OFF} 
\log\left(\frac{I_D}{I_{OFF}}\right)
$$

**Effective SS:**

$$
\frac{V_{DD}}{2\log\left(\frac{I_D}{I_{OFF}}\right)}
$$
I_{ON} and I_{OFF} of TFETs

[1] G. Zhou et al., pp. 782, vol. 33, no. 6, EDL 2012 (University of Notre Dame)

C. Auth et al., pp.131, VLSI2012 (Intel).
K. Mistry et al., pp.247, IEDM2007 (Intel).
Tunnel FET (III-V)

K. Tomioka et al., pp.47, VLSI2012 (Hokkaido University)

SS=21mV/dec  SS=110mV/dec

- SS of TFET is function of $V_G$ due to Zener tunnel current
- Minimum SS= 21 mV/dec is reached due to optimized series resistance of contact, undoped InAs and InAs/Si
- $I_{ON}/I_{OFF}$~$10^6$ at $V_{DS}= 1.0V$ ($I_{ON}= 1A_{\mu/m}$)

Conventional FET limit
SS= 60 mV/dec

NW Diameter= 30nm
Strained SiGe nanowire TFETs

A. Villalon et al., pp. 66, VLSI2014 (CEA-LETI)

- $I_{on}$ enhancement up to 760 $\mu$A/$\mu$m.
- Low bandgap of SiGe increase BTBT.
- SS lower than 60 mV/dec is still challenge to be addressed.
Ni(Al$_x$Si$_{1-x}$)$_2$ can avoid encroachment into channel region.

$I_{on}$ at 64 $\mu$A/$\mu$m at $V_{DD} = 1$V.

Scaling diameter of NW can improved performance.
Fin-shape Si-TFET

Y. Morita et al., pp. 236, VLSI2013 (AIST)

This study

Multi-gate can enhance electric field, particularly at the corner, resulting in better performance.

Scaling Fin-width provide SS lower than 60 mV/dec.
Al-N complex can introduce isoelectronic trap (IET) below Si CB.

- Tunneling probability is increased through the intermediary of IET.
TFET vs. MOSFET at low $V_{DD}$

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

$EOT = 1$ nm, $L_G = 20$ nm, $tlnAs = 5$ nm

<table>
<thead>
<tr>
<th>TFET @0.35V</th>
<th>Stage Delay (ps)</th>
<th>Switching Energy (fJ)</th>
<th>Leakage Power (nW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV (FO=3)</td>
<td>105</td>
<td>0.26</td>
<td>0.37</td>
</tr>
<tr>
<td>NAND (FO=3)</td>
<td>149</td>
<td>0.32</td>
<td>0.57</td>
</tr>
<tr>
<td>NOR (FO=3)</td>
<td>158</td>
<td>0.34</td>
<td>0.54</td>
</tr>
<tr>
<td>Combined</td>
<td>129</td>
<td>0.29</td>
<td>0.46</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CMOS @0.3V</th>
<th>Stage Delay (ps)</th>
<th>Switching Energy (fJ)</th>
<th>Leakage Power (nW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV (FO=3)</td>
<td>830</td>
<td>0.25</td>
<td>0.37</td>
</tr>
<tr>
<td>NAND (FO=3)</td>
<td>1364</td>
<td>0.32</td>
<td>0.56</td>
</tr>
<tr>
<td>NOR (FO=3)</td>
<td>1389</td>
<td>0.33</td>
<td>0.53</td>
</tr>
<tr>
<td>Combined</td>
<td>1103</td>
<td>0.29</td>
<td>0.46</td>
</tr>
</tbody>
</table>

$V_{DD}$ 0.3~0.35V

TFET 8x faster at the same power

“parameter variation is not a significant factor for differentiation between MOSFET and TFET”
Tunnel FET (Si)

A. Villalon, pp.49, VLSI 2012 (CEA-LETI)

- X in Si_{1-x}Ge_{x} is optimized to allow for efficient BTBT
- \( L_G = 200\text{nm} \)
- \( I_{ON}/I_{OFF} \sim 10^5 \)

Reducing SiGe Body thickness improves Subthreshold swing.

130mV/dec

190mV/dec
Device structure

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

- Nanowire TFET gate-all-around - best electrostatics
- Tunneling // to the gate oblique to the gate field
- Tunneling ⊥ to the gate in-line with the gate field

K. Tomioka et al., pp.47, VLSI2012 (Hokkaido University)
Appendix 4.

2D channel material technologies
Why 2D channels?

- High-drivability FinFET
  - Large $W_{eff}/W_{footprint}$
    - Taller Fin
    - Narrow Fin pitch
      - Thinner Fin

- Mobility degradation in thin Si < 10 nm for both electron & hole.

  $\rightarrow$ High-mobility 2D channels

---

$K. \text{Uchida, et. al., IEDM, 23.1, 2008.}$

$S. \text{Kobayashi, et. al., J. Appl. Phys. 106, 024511 (2009).}$
Family of 2D materials

**Graphene family**
- Graphene
- Silicene
- h-BN

**Oxide family**
- TiO$_2$
- RuO$_2$

**Transition metal dichalcogenide (TMD) family**
- MoS$_2$
- MoSe$_2$
- WSe$_2$
- MoTe$_2$
- WS$_2$
- WTe$_2$

Energy [eV]

Vacuum

<table>
<thead>
<tr>
<th>Material</th>
<th>Energy [eV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>-1.1</td>
</tr>
<tr>
<td>Graphene</td>
<td>-5.9</td>
</tr>
<tr>
<td>Silicene</td>
<td>-3</td>
</tr>
<tr>
<td>MoS$_2$</td>
<td>-1.6</td>
</tr>
<tr>
<td>MoSe$_2$</td>
<td>-1.6</td>
</tr>
<tr>
<td>WSe$_2$</td>
<td>-0.4</td>
</tr>
<tr>
<td>MoTe$_2$</td>
<td>-1.4</td>
</tr>
<tr>
<td>WS$_2$</td>
<td>-1.2</td>
</tr>
<tr>
<td>WTe$_2$</td>
<td>-1.6</td>
</tr>
</tbody>
</table>
TMD band structure

- **MX2**

- **MoX2 & WX2**


---

**Energy (eV)**

- Conduction Band
  - MoS$_2$: $-4.25$, $-3.91$, $-3.81$, $-3.93$, $-3.61$, $-3.67$
  - MoSe$_2$: $-3.71$, $-3.84$, $-3.61$, $-3.67$
  - MoTe$_2$: $-4.28$, $-4.59$
  - WS$_2$: $-5.24$, $-4.99$, $-5.16$, $-5.16$, $-5.82$, $-5.82$
  - WSe$_2$: $-5.87$, $-5.59$, $-5.48$, $-5.48$
  - WTe$_2$: $-6.27$, $-5.59$, $-4.86$, $-4.86$

**Valence Band**

*Tokyo Tech. 0.65 nm*
Dependence on # of layers in MoS2 & WS2

Synthesis of MoS2

- Exfoliation
  - Scotch tape
  - Liquid Exfoliation

- Dipping & annealing

Valeria Nicolosi et al., Science, 2013: Vol. 340 no. 6139
**Synthesis of MoS$_2$**

- **Chemical vapor deposition (CVD)**
- **RF magnetron sputtering**

*H. Wang, et. al., IEDM, 4.6, 2012.*
Exfoliated single-layer MoS2 nMISFET

- 217 cm²/Vs, electron

- Depletion mode

B. Radisavljevic et al., Nature Nanotech. 6, 147 (2011)
Exfoliated 6-layer MoS2 nMISFET

- ~ 4 nm 6 MLs
- Depletion mode

(a) Exfoliated MoS2 flake on 90nm SiO2/p-doped silicon substrate
(b) Chloride Doping - treat with 1,2-Dichloroethane
Cleaning Process - acetone, isopropanol 30 Min
S/D Contacts - metal deposition (30 nm Ni/60 nm Au)

CVD-single-layer MoS2 nMISFET

- **Mobility**
  \[ \sim 190 \text{ cm}^2/\text{Vs} \]

- **Depletion mode**

![Device structure and graph](image)

*H. Wang, et. al., IEDM, 4.6, 2012.*
Monolayer-MoS2 nMISFET simulation

- Non-equilibrium Green’s function
- Heavier electron effective mass
  - $m^* = 0.45m_0$
- Immunity to short channel effects
  - DIBL $\sim 10$ mV/V
  - S-factor: 60 mV/dec.
- Larger Ion/Ioff ratio than III-V FET

Table 1. Comparison of Key Device Performance Parameters of In$_{0.7}$Ga$_{0.3}$As Quantum-Well FET (ref 22) and Monolayer MoS$_2$ FET of Identical EOT and Channel Length

<table>
<thead>
<tr>
<th></th>
<th>$L_{ch}$ (nm)</th>
<th>EOT (Å)</th>
<th>$I_{max}$ (mA/μm)</th>
<th>peak $g_m$ (mS/μm)</th>
<th>max $I_{ON}/I_{OFF}$</th>
<th>min SS (mV/decade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As quantum-wall FET (ref 22)</td>
<td>75</td>
<td>22</td>
<td>0.49</td>
<td>1.75</td>
<td>312</td>
<td>85</td>
</tr>
<tr>
<td>monolayer MoS$_2$ FET</td>
<td>75</td>
<td>22</td>
<td>0.19</td>
<td>0.3</td>
<td>$1.4 \times 10^7$</td>
<td>60</td>
</tr>
</tbody>
</table>

**Summary of band-gaps of TMDs**

<table>
<thead>
<tr>
<th></th>
<th>Ti</th>
<th>Zr</th>
<th>Hf</th>
<th>V</th>
<th>Nb</th>
<th>Ta</th>
<th>Mo</th>
<th>W</th>
</tr>
</thead>
<tbody>
<tr>
<td>eV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S2</td>
<td>1.95 (D), 0.3 (I)</td>
<td>1.68 (D), 2.1 (I)</td>
<td>2.7 (D), 1.93 (I)</td>
<td>Metal</td>
<td>Metal</td>
<td>Metal</td>
<td>1.8 (SL), 1.72 (D), 1.2 (I)</td>
<td>1.93 (SL), 1.77 (D), 1.35 (I)</td>
</tr>
<tr>
<td>Se2</td>
<td>1.55 (D), 0.15 (I)</td>
<td>1.20 (D), 1.61 (I)</td>
<td>1.77 (D), 1.18 (I)</td>
<td>Metal</td>
<td>Metal</td>
<td>Metal</td>
<td>1.49 (SL), 1.38 (D), 1.1 (I)</td>
<td>1.6 (D), 1.1 (I)</td>
</tr>
<tr>
<td>Te2</td>
<td>1.0 (D) Semi-metal</td>
<td>Semi-metal</td>
<td>Semi-metal</td>
<td>Metal</td>
<td>Semi-metal</td>
<td>1.13 (SL), Semi-metal</td>
<td>Semi-metal</td>
<td>Semi-metal</td>
</tr>
</tbody>
</table>

*Ian Post, Symposium on VLSI Technology, 2013, Short Course*
Appendix 5.

Other emerging technologies
MEMS relay

I\textsubscript{ON}/I\textsubscript{OFF} of \(\sim 10^{10}\)

Ultra-low-power digital logic applications.

- Frequency of 1, 5, 25kHz under operation
Junctionless Transistor (Intel)

R. Rios et al., EDL. 32(2011)1170

- IM : Conventional Inversion Mode
- JAM LD : Junctionless Accumulation Mode with low dope
- JAM HD : Junctionless Accumulation Mode with high dope

- JAM devices have reduced gate control and degraded short-channel characteristics relative to IM

- Not suitable for high-performance logic (high $I_{on}$ and moderate $I_{off}$)
Near-ideal subthreshold slope, close to 60 mV/dec at room temperature, and extremely low leakage currents

- Silicon nanowire is uniformly doped
- Gate material is opposite polarity polysilicon

\[ \frac{I_{ON}}{I_{OFF}} \approx 1 \times 10^6 \quad (-1 < V_g < 1) \]

\[ I_{OFF} \text{ is smaller than } 10^{-15} \text{ A} \]
SWCNT: single wall carbon nanotube

GNR: graphene nano ribbon

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>SWCNT</th>
<th>GNR</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mobility cm²/V/s</strong></td>
<td>1400</td>
<td>&gt;10000</td>
<td>&gt;10000 for large widths</td>
</tr>
<tr>
<td><strong>Mean free path (nm) @ room temp</strong></td>
<td>30</td>
<td>&gt;1,000</td>
<td>~1,000</td>
</tr>
<tr>
<td><strong>Thermal conductivity (W/mK)</strong></td>
<td>150</td>
<td>5800</td>
<td>~5000</td>
</tr>
</tbody>
</table>

Carbon materials for FET applications

- an ultra-thin body for aggressive channel length scaling
- excellent intrinsic transport properties similar to carbon nanotubes
- pattern the desired device structures
Sub-10nm carbon nanotube transistor

Transistor operation with $L_{ch}$ of 9nm
Graphene Field-effect Transistor

- Ambipolar Characteristics
- Bi-layer graphene and double gates can open the gap

Z. Chen et al., pp.509, IEDM2008 (IBM)

Spin transfer Torque Switching MOSFET

Magnetic tunnel junction on S/D

Read/write are enabled by using ferromagnetic electrodes and Spin-polarized current