Future of Nano CMOS Technology

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Tokyo Institute of Technology
Background for nano-electronics
Feature Size / Technology Node

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm → 0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm → 90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm(2012) → 14 nm (2014)

From 1970 to 2013 (Last year)

43 years
18 generations
Line width: 1/450
Area: 1/200,000

1 generation
2.5 years
Line width: 1/1.43 = 0.70
Area: 1/2 = 0.5
Ballistic conduction will not happen even decreasing channel length. 

\[ L \gg \lambda \]

**Diffusive transport**

\[ L \sim \lambda \]

**Quasi-Ballistic transport**

\[ L < \lambda \]

**Ballistic transport**

Ballistic transport will never happen for MOSFET because of back scattering at drain.

With decreasing channel length, Drain current increase continue.

Ballistic conduction will not happen even decreasing channel length.

1D quantum conduction, or ballistic conduction will not happen. 
(1D quantum conduction: 77.8 \mu S regardless of the length and material).
Then, now!.

Noticed that the technology is difficult.

Development of EUV (Extreme Ultra Violet) lithography delayed significantly.
Noticed that the technology is difficult.

In addition with the significant delay in EUV (Extreme Ultra Violet) lithography delayed significantly,

- Reduction of the thickness of High-k gate oxide becomes very difficult.

- Decreasing supply voltage becomes difficult because of subtreshold leakage and variability of threshold voltage.
Now

Technology development delayed.

Shrink rate of gate length will become from 0.7 to 0.8 or 0.85.

Number of the semiconductor companies which can develop state of the art technology decreasing.

In the past, technologies come with the purchase of equipment's

But now, every company is facing threat of dropping off, unless they concentrated on the development of technologies.

Thus, technology development is becoming much important.
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years, even though, it is very matured market!!

2011
300B USD

2025
1,500B USD

Gartner: By K. Kim, CSTIC 2012
Question

What is the problem for downsizing?
The problem for downsizing
S and D distance small

→ Ion & Ioff increase

Ioff increase: Transistor cannot be turned-off.

Ioff (Off-leakage current) between S and D

1. Punch-through between S and D
2. Direct-tunneling between S and D
3. Subthreshold current between S and D
1. Punch-through between S and D
Problem for downsizing

Region governed by gate bias

Region governed by drain bias

DL touch with S Region (DL)

Large $I_{OFF}$

No $t_{ox}, V_{dd}$ thinning

Gate metal

Gate oxide

Source

Drain

Channel

Substrate

0V

0V

0V

0V

0V

0V

0V

0V

0V

0V

0V

0V

0V

$V_{dd}$

$V_{dd}$

$V_{dd}$

$V_{dd}$

$V_{dd}$

$t_{ox}$ and $V_{dd}$ have to be decreased for better channel potential control $\rightarrow I_{OFF}$ Suppression

$0V < V_{dep} < 1V$

$0V < V_{dep} < 1V$

Large $I_{OFF}$ (Electron current)
1. Punch-through between S and D

There are 3 solutions to suppress the depletion layer

A. Decrease supply voltage $\rightarrow$ Very difficult

B. Decrease tox to enhance the channel potential controllability by gate bias

C. Gate/channel configuration change to enhance the channel potential controllability by gate bias

Fin-FET, ET-SOI, etc.
B. Decrease tox

A. Toriumi (Tokyo Univ), IEDM 2006, Short Course
C. Configuration change for channel and gate structures for better control of channel potential.

Fin-FET, ET-SOI, etc.
Extremely Thin (or Fully-Depleted) SOI

- Make Si layer thin
- Control channel potential also from the bottom
Surrounding gate structure (Multiple gates)

- Make Si layer thin
- Control channel potential also by multiple gates not only from top & bottom but maybe also from side
New structures!

Multi-gate structures

Fin

Tri-gate

Tri-gate (Variation)

Ω-gate

All-around
Our work at TIT: Ω-gate Si Nanowire

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  (1.32 mA/μm @ $I_{OFF}=117$ nA/μm)
- DIBL of 62mV/V and SS of 70mV/dec for nFET
2. Direct-tunneling between S and D

Wave function of electron penetrates the channel potential barriers by quantum mechanical physics, when the channel length is around 3 nm.
Built-in potential between Source and Channel pn junction < 0.7 V

When transistor is at off state

Tunneling distance

3 nm

Direct-tunnel current

Energy or Potential for Electron

Source

Channel

Drain

There is no solutions!

Downsizing limit is @ Lg = 3 nm.
3. Subthreshold current between S and D
Subthreshold leakage current of MOSFET

\[ I_{on} \propto V_{g} - V_{th} \]

Subthreshold Leakage Current

\[ I_{off} \propto \exp(aV_{g}) \]

Subthreshold region

\( V_{g} = 0V \)
Subthreshold leakage current

Electron Energy Boltzmann statics

Exp (qV/kT)

$L_g \rightarrow 1/2$
$V_d, V_g \rightarrow 1/2$
$V_{th} \rightarrow 1/2$

However
$I_{off} \rightarrow 10^3$ in this example

Because of log-linear dependence
Subthreshold leakage current of MOSFET

Subthreshold Leakage Current

\[ I_{\text{off}} \propto \exp(aV_g) \]

Vg=0V

Subthreshold region

Vth (Threshold Voltage)

Subthreshold Current Is OK at Single Tr. level

But not OK For Billions of Trs.

\[ I_{\text{on}} \propto V_g - V_{\text{th}} \]
3. Subthreshold current between S and D

Solution: however very difficult

- Keep Vth as high as possible
  - Do not decrease supply voltage, Vd
  - However, punchthrough enhanced
  - Suppress variability in Vth

Thus, subthreshold current will limit the downsizing, especially for mobile devices
The limit is different depending on application.
How far can we go for production?

Past

0.7 times per 2.5 years

10μm → 8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm → 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

Direct-tunnel

Intermediate node

Subthreshold punchthrough

Limit depending on applications

Fundamental limit

Now

Future

(28nm) → 22nm → 14nm

→ 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm? →

• At least 4,5 generations to 8 ~ 5 nm
However, careful about the name of technology!

Recently, Gate length (Lg) is much larger than the Technology name

22 nm Technology by Intel

Lg (Gate length) = 30 nm (HP), 34 nm (MP), 34 nm or larger (SP)
IEDM 2012, VLSI 2013

14 nm Technology by Global

Lg (Gate length) = 25 nm Euro SOI 2014

10 nm Technology by Leti (FD-SOI)

Lg (Gate length) = 15 nm
## ITRS 2013 (Just published in April 2014)

<table>
<thead>
<tr>
<th>Year</th>
<th>2013</th>
<th>2015</th>
<th>2017</th>
<th>2019</th>
<th>2021</th>
<th>2023</th>
<th>2025</th>
<th>2027</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Commercial name (nm)</strong></td>
<td>14</td>
<td>10</td>
<td>7</td>
<td>5</td>
<td>3.5</td>
<td>2.5</td>
<td>1.8</td>
<td>1.3</td>
</tr>
<tr>
<td><strong>Metal half pitch (nm)</strong></td>
<td>40</td>
<td>32</td>
<td>25.3</td>
<td>20</td>
<td>15.9</td>
<td>12.6</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td><strong>$L_g$ (nm)</strong></td>
<td>20.2</td>
<td>16.8</td>
<td>14.0</td>
<td>11.7</td>
<td>9.7</td>
<td>8.1</td>
<td>6.7</td>
<td>5.6</td>
</tr>
<tr>
<td>($L_g$ for ITRS 2007)</td>
<td>(13)</td>
<td>(10)</td>
<td>(8)</td>
<td>(6)</td>
<td>(5)</td>
<td>(4.5 in 2022)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>$L_g$ for low stand by power (nm)</strong></td>
<td>23</td>
<td>19</td>
<td>16</td>
<td>13.3</td>
<td>11.1</td>
<td>9.3</td>
<td>7.7</td>
<td>6.4</td>
</tr>
<tr>
<td><strong>$V_{dd}$ (V)</strong></td>
<td>0.86</td>
<td>0.83</td>
<td>0.80</td>
<td>0.77</td>
<td>0.74</td>
<td>0.71</td>
<td>0.68</td>
<td>0.65</td>
</tr>
<tr>
<td>($V_{dd}$ (V) for ITRS 2007)</td>
<td>(0.90)</td>
<td>(0.80)</td>
<td>(0.70)</td>
<td>(0.70)</td>
<td>(0.65)</td>
<td>(0.65 in 2022)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>EOT (nm)</strong></td>
<td>0.80</td>
<td>0.73</td>
<td>0.67</td>
<td>0.61</td>
<td>0.56</td>
<td>0.51</td>
<td>0.47</td>
<td>0.43</td>
</tr>
<tr>
<td>(EOT (nm) for ITRS 2007)</td>
<td>(0.60)</td>
<td>(0.60)</td>
<td>(0.55)</td>
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<td>(3.0 in 2022)</td>
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<td></td>
</tr>
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</table>
The rate for the shrinkage for the gate length and line pitch will be larger than 0.7 in near future, because of the subthreshold leakage, and also because of the delay in EUV lithography.

As a result, we will have more technology generations until reaching the downsizing limit, and the time to reach the limit will be delayed.
How far can we go for production?

Thus, we may go down to “1.5 nm” technology node by choosing whatever gate length we want for the application.
More Moore to More More Moore

Technology node

<table>
<thead>
<tr>
<th>65nm</th>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lg 35nm</td>
<td>Lg 30nm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Now

Future

15nm, 11nm, 8nm, 5nm, 3nm

(Fin, Tri, Nanowire)

Si

Planar

Tri-Gate

28nm

Si is still main stream for future !!

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)

Others

Emerging Devices

Alternative (III-V/Ge)
Channel FinFET

ET: Extremely Thin

SiGe

ETSOI

High-k

Metal
Continued research and development of high-k gate dielectrics and the technology for direct contact of high-k and Si is necessary. SiO$_2$ IL (Interfacial Layer) is used at Si interface to realize good mobility.

<table>
<thead>
<tr>
<th>EOT (nm)</th>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
<th>15nm, 11nm, 8nm, 5nm, 3nm,</th>
</tr>
</thead>
<tbody>
<tr>
<td>HfO$_2$/SiO$_2$ (IBM)</td>
<td>EOT=0.9nm</td>
<td>Metal Gate (different for NMOS &amp; PMOS)</td>
<td>High-k</td>
<td>Silicon Substrate</td>
</tr>
</tbody>
</table>

- **T.C. Chen, et al., p.8, VLSI 2009, (IBM)**
- **T. Ando, et al., p.423, IEDM2009, (IBM)**
- **K. Kakushima, et al., p.8, IWDTF 2008, (Tokyo Tech.)**

**Hf-based oxides**

- **EOT=0.52 nm**
  - Remote SiO$_2$-IL scavenging HfO$_2$ (IBM)

- **EOT=0.37 nm**
  - TiN + M3 (0.5x) (IBM)
- **EOT=0.40 nm**
  - TiN + M3 (1.0x) (IBM)
- **EOT=0.48 nm**
  - MG (Tokyo Tech.)

0.48 $\rightarrow$ 0.37nm Increase of $I_d$ at 30%

**Direct contact with La-silicate (Tokyo. Tech.)**
High-k is very important, however very difficult.

Thickness (EOT) decreased only 0.05 nm (or 0.5 Å, or 1 atom layer) for every generation.
How far can we go for production?

Rather than loff value, Ion/loff ratio is important.

Now, Ion/loff ratio is typically $10^6$.

However, it degrades significantly with decrease in Vsupply.
**I\textsubscript{ON} and I\textsubscript{OFF} benchmark**

**NMOS**

- **Intel [a]**
  - Bulk 32nm \(V_{DD}=0.8\) V
  - Tri-Gate 22nm \(V_{DD}=0.8\) V
- **Samsung [c]**
  - Bulk 20nm \(V_{DD}=0.9\) V
- **Toshiba [d]**
  - Tri-Gate NW \(V_{DD}=1\) V
- **IBM [g]**
  - ETSOI \(V_{DD}=0.9\) V
  - GAA NW \(V_{DD}=1\) V
- **IBM [j]**
  - GAA NW \(V_{DD}=1.1\) V

**PMOS**

- **Intel [a]**
  - Bulk 32nm \(V_{DD}=0.8\) V
  - Tri-Gate 22nm \(V_{DD}=0.8\) V
- **Intel [b]**
  - Bulk 45nm \(V_{DD}=1\) V
- **IBM [e]**
  - GAA NW \(V_{DD}=0.9\) V
- **IBM [f]**
  - FinFET 25nm \(V_{DD}=1\) V
- **IBM [h]**
  - GAA NW \(V_{DD}=1.1\) V
- **STMicro. [h]**
  - GAA NW \(V_{DD}=1\) V

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[a] C. Auth et al., pp.131, VLSI2012 (Intel).
[d] S. Saitoh et al., pp.11, VLSI2012 (Toshiba).
[g] A. Khakifirooz et al., pp.117, VLSI2012 (IBM).
[i] S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)
[j] K. Cheng et al., pp.419, IEDM2012 (IBM)
Nanowire/Tri gate MOSFETs have advantage not only suppressing Ioff, but also for increasing Ion over planer MOSFETs

1. Because of higher mobility due to lower vertical electric field

2. Because of higher carrier density at the round corner
Electron Density (x10^{19} \text{cm}^{-3})

Distance from SiNW Surface (nm)

- **Edge portion**
- **Flat portion**

Inversion areal ratio: 29%
3. Now Problems for downsizing!

We have to decrease Si layer thickness to better control of channel potential by gate bias when we decrease the gate length.

Significant decrease in conduction or Ion.
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Short-channel effect

T. Skotnicki, IEDM 2009 Short Course (STMicroelectronics)

\[
\text{SCE} = 0.64 \frac{\varepsilon_s}{\varepsilon_{ox}} \times EI \times \Phi_d
\]

\[
\text{DIBL} = 0.8 \frac{\varepsilon_s}{\varepsilon_{ox}} \times EI \times V_{ds}
\]

\[
EI = 1 \times \left( 1 + \frac{T_{ox}^2}{L_{el}^2} \right) \times \left( 1 + \frac{T_{dep}^2}{L_{el}^2} \right)
\]

- if max. ch. doping is $10^{19}$ cm$^{-3}$ => Tdep~12nm then:
- if max. ch. doping is $10^{20}$ cm$^{-3}$ => Tdep~12nm then:

\[
T_{box} = 145 \text{ nm}
\]

\[
\lambda T_{box} = 18 \text{ nm}
\]

If Tsi $\approx 3$ nm then:

If Tsi $\approx 3$ nm then:

- Tbox = 10nm
- $\lambda T_{box} = 3 \text{ nm}$

If Tsi $\approx 3$ nm then:

If Tsi $\approx 3$ nm then:

- Tbox = 10nm
- $\lambda T_{box} = 0.46 \text{ nm}$

If minimum feasible Tsi is supposed 3nm, then:

- Tsi/2 plays role of Xj, and that of Tdep.

\[
\begin{align*}
\text{Le}_{el, \text{min}} &= 34 \text{ nm} \\
\text{Le}_{el, \text{min}} &= 34 \text{ nm} \\
\approx 30 \text{ nm} \\
\approx 10 \text{ nm} \\
\approx 6 \text{ nm} \\
\approx 2.7 \text{ nm}
\end{align*}
\]
Mobility degradation for small diameter nanowire FETs, because channel carriers become too close to all surrounding nanowire surface, and scattered strongly.
Problems in Multi-gate

Decreasing the diameter of NW

Improved short-channel control

Severe mobility degradation

S. Bangsaruntip et al., pp.297, IEDM2009 (IBM), K. Tachi et al., pp.313, IEDM2009 (CEA-LETI)

Need to decrease diameter for SCH

PFETs

NFETs

DIBL (mV/V)

L_G (nm)

0 25 50 75 100

W (nm) / H (nm)

~ 5 / ~ 6

6.8 / 9.5

9.0 / 13.9

11.2 / 20.0

NFET legend

6.8 / 9.5

12.3 / 15.1

16.5 / 22.1

21.6 / 23.8

W (nm) / H (nm)

0 25 50 75 100

Effective mobility [cm^2/Vs]

0 50 100 200 300 400

N_inv [x10^13 cm^-2]

0.2 0.4 0.6 0.8 1.0 1.2

Circular SNWT 5nm in dia.

Recangular SNWTs

Significant μ degradation at diameter < 10 nm
Problems in SOI

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

$< 10 \text{ nm}$

1. Mobility degradation

Extremely small distance between the electron and all around Si surface.

Strong scattering of electrons by interaction with all around Si surface.

2. Electron density decrease

Decrease of DOS in extremely narrow wire.

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-k is necessary.
Carrier density degradation for small diameter nanowire FET, because of the decrease in density of states.
Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Smaller wire/fin width is necessary for SCE suppression

But mobility and $I_{ON}$ severely degrade with wire/fin width reduction

Therefore even in multi-gate structures, EOT scaling should be accelerated to provide SCE immunity
New Materials!

High-k beyond 0.5 nm
To use high-k dielectrics

K: Dielectric Constant

Thin SiO₂

K=4

Almost the same electric characteristics

High-k

K=20

Thick high-k dielectrics

5 times thicker

Small leakage Current

However, very difficult and big challenge!
**Choice of High-k elements for oxide**

**Candidates**

- **Unstable at Si interface**
  1. Si + MOₓ M + SiO₂
  2. Si + MOₓ MSiₓ + SiO₂
  3. Si + MOₓ M + MSiₓOᵧ

- **Gas or liquid at 1000 K**
- **Radio active**

**HfO₂ based dielectrics** are selected as the first generation materials, because of their merit in:
1) band-offset,
2) dielectric constant,
3) thermal stability.

**La₂O₃ based dielectrics** are thought to be the next generation materials, which may not need a thicker interfacial layer.

R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Oxide

Band offset

Si

Leakage Current by Tunneling

Band Discontinuity [eV]

Conduction Band Offset vs. Dielectric Constant

Dielectric Constant \( \varepsilon(0) \)

XPS measurement by Prof. T. Hattori, INFOS 2003
Direct high-k/Si by silicate reaction

HfO₂ case

La₂O₃ case

Our approach

Direct contact can be achieved with La₂O₃ by forming silicate at interface
Control of oxygen partial pressure is the key for processing.

\[ P_{O_2} \text{: Partial pressure of } O_2 \text{ during high temperature annealing} \]
SiO\textsubscript{x}-IL growth at HfO\textsubscript{2}/Si Interface

\begin{itemize}
  \item XPS Si1s spectrum
  \item TEM image 500 °C 30min
  \item W
  \item HfO\textsubscript{2} \(k=16\)
  \item SiO\textsubscript{x}-IL \(k=4\)
  \item Phase separator

\end{itemize}

\begin{equation*}
\text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2
\end{equation*}

H. Shimizu, JJAP, 44, pp. 6131

\begin{itemize}
  \item Oxygen supplied from W gate electrode
  \item D.J. Lichtenwalner, Tans. ECS 11, 319
  \item SiO\textsubscript{x}-IL is formed after annealing
  \item Oxygen control is required for optimizing the reaction
\end{itemize}
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Physical mechanisms for small Dit

① silicate-reaction-formed fresh interface

② stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

SiO<sub>4</sub> tetrahedron network

FGA800°C is necessary to reduce the interfacial stress


However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Cluster tool for HKMG Stack

- EB Deposition for HK
- Flash Lamp
- Sputter for MG
- Robot
- ALD
- RTA
- Entrance

5m

5m

5m
Cluster Chambers for HKMG Gate Stack

EB Deposition: HK
Sputter: MG
Flash Lamp Anneal
ALD: HK

Entrance
Robot
RTA
ALD of La2O3


Precursor (ligand)

La(iPrCp)3

La(FAMD)3

ALD is indispensable from the manufacturing viewpoint - precise control of film thickness and good uniformity
Annealing temperature (°C)

EOT (nm)

Annealed for 2 s

La$_2$O$_3$ (3.5 nm)

W (60 nm)

TiN/W (12 nm)

TiN/W (6 nm)

TiN (45nm)/W (6nm)

EOT = 0.55 nm

TaN/(45nm)/W (3nm)

900°C, 30min

EOT = 0.55 nm

Experiment

C$_v$ fitting

Theory

Vg (V)

C$_g$ (μF/cm$^2$)
TaN(45nm)/W(3nm)

$Q_{fix} = 1 \times 10^{11} \text{ cm}^{-2}$

900°C, 30min

Fixed Charge density: $1 \times 10^{11} \text{ cm}^{-2}$
Our Work at TIT: High-k

Our result at TIT

EOT = 0.40nm

- L/W = 5/20\mu m
- T = 300K
- N_{sub} = 3 \times 10^{16} cm^{-3}

Electron Mobility [cm^2/Vsec]

- EOT = 0.40nm
- L/W = 5/20\mu m
- T = 300K
- N_{sub} = 3 \times 10^{16} cm^{-3}
Benchmark of La-silicate dielectrics

**Gate Leakage current**

- ITRS requirement

- $J_g$ at 1 V (A/cm$^2$)

- Our data: La-silicate gate oxide

**Effective Mobility**

- at 1 MV/cm

- Solid circle: Our data

- Open square: Hf-based oxides

- La-silicate gate oxide

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T. Ando, et al., (IBM) IEDM 2009, p.423
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Flat metal/high-k interface for better mobility
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for V$_\text{th}$ control
- Interface dipole control for V$_\text{th}$ tuning
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
- Reliability: PBTI, NBTI, TDDB
- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for V$_\text{th}$ control
- Interface dipole control for V$_\text{th}$ tuning
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
Thank you very much for your attention.
Appendix
What is Next Revolution for Device Technology?

1900: Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics
What is Next Revolution for Device Technology?

1900: Electronics

↓

1970: Micro Electronics

↓

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

↓

1970: Micro Electronics

?:: Nano Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

?: Nano Electronics
Maybe Not a Revolution
But Great Innovation
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

↑

1970: Micro Electronics

↑ ? years

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

70 years

1970: Micro Electronics

? years

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

↓ 70 years

1970: Micro Electronics

↓ 70 years

2040: Braintronics
Braintronics

We do know system and algorithms are important! But do not know how it can be by us for use of bio?
Long term roadmap for development

Source: H. Iwai, IPFA 2006

New Materials, New Process, New Structure

Hybrid integration of different functional Chip
Increase of SOC functionality

3D integration of memory cell
3D integration of logic devices

Miniaturization of Interconnects on PCB
(Printed Circuit Board)

Low cost for LSI process
Revolution for CR, Equipment

Introduction of algorithm of bio system
Brain of insects, human

We do not know how?

Some time in 2020-2030

After 2040?
Braintronics for 2040’s

It’s a task for you,
For young generations!