Future of Nano CMOS Technology

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Tokyo Institute of Technology
Background for nano-electronics
Feature Size / Technology Node

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm →
0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm →
90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm(2012)
→ 14 nm (2014)

From 1970 to 2013 (Last year)
43 years 1 generation
18 generations 2.5 years
Line width: 1/450 Line width: 1/1.43 = 0.70
Area: 1/200,000 Area: 1/2 = 0.5
Ballistic conduction will not happen even decreasing channel length.

\[ L \gg \lambda \]

**Diffusive transport**

\[ L \sim \lambda \]

**Quasi-Ballistic transport**

\[ L < \lambda \]

**Ballistic transport**

Ballistic transport will never happen for MOSFET because of back scattering at drain.

With decreasing channel length, Drain current increase continue.

Also, 1D quantum conduction, or ballistic conduction will not happen. (1D quantum conduction: \(77.8 \mu\text{S}\) regardless of the length and material).
Then, now!

Noticed that the technology is difficult.

Development of EUV (Extreme Ultra Violet) lithography delayed significantly.
Noticed that the technology is difficult.

In addition with the significant delay in EUV (Extreme Ultra Violet) lithography delayed significantly,

- Reduction of the thickness of High-k gate oxide becomes very difficult.

- Decreasing supply voltage becomes difficult because of subtreshold leakage and variability of threshold voltage.
Now

Technology development delayed.

Shrink rate of gate length will become from 07 to 0.8 or 0.85.

Number of the semiconductor companies which can develop state of the art technology decreasing.

In the past, technologies come with the purchase of equipment's

But now, every companies are facing threat of dropping off, unless they concentrated on the development of technologies.

Thus, technology development is becoming much important.
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years, even though, it is very matured market!!

2011: 300B USD → 2025: 1,500B USD

Gartner: By K. Kim, CSTIC 2012
Question

What is the problem for downsizing?
The problem for downsizing

S and D distance small

→ Ion & Ioff increase

Ioff increase: Transistor cannot be turned-off.

Ioff (Off-leakage current) between S and D

1. Punch-through between S and D
2. Direct-tunneling between S and D
3. Subthreshold current between S and D
1. Punch-through between S and D
Problem for downsizing

Region governed by gate bias
Region governed by drain bias

DL touch with $S$
Region (DL)

Large $I_{OFF}$

$V_{dd}$ thinning

$0V < V_{dep} < 1V$

$t_{ox}$ and $V_{dd}$ have to be decreased for better channel potential control $\rightarrow I_{OFF}$ Suppression
1. Punch-through between S and D

There are 3 solutions to suppress the depletion layer

A. Decrease supply voltage $\rightarrow$ Very difficult

B. Decrease tox to enhance the channel potential controllability by gate bias

C. Gate/channel configuration change to enhance the channel potential controllability by gate bias

Fin-FET, ET-SOI, etc.
B. Decrease tox

A. Toriumi (Tokyo Univ), IEDM 2006, Short Course
C. Configuration change for channel and gate structures for better control of channel potential.

Fin-FET, ET-SOI, etc.
Extremely Thin (or Fully-Depleted) SOI

- Make Si layer thin
- Control channel potential also from the bottom
Surrounding gate structure (Multiple gates)

- Make Si layer thin
- Control channel potential also by multiple gates not only from top & bottom but maybe also from side
New structures!

Multi-gate structures

Fin
Tri-gate
Tri-gate (Variation)
Ω-gate
All-around
Our work at TIT: \(\Omega\)-gate Si Nanowire

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  
  \((1.32 \text{ mA/\mu m} @ I_{\text{OFF}}=117 \text{ nA/\mu m})\)
- DIBL of 62mV/V and SS of 70mV/dec for nFET
2. Direct-tunneling between S and D

Wave function of electron penetrates the channel potential barriers by quantum mechanical physics, when the channel length is around 3 nm.
There is no solutions!

**Downsizing limit is @ Lg = 3 nm.**
3. Subthreshold current between S and D
Subthreshold leakage current of MOSFET

Subthreshold leakage current of MOSFET

Subthreshold Leakage Current

Subthreshold current

\[ I_{off} \propto \exp(aV_g) \]

\[ V_g = 0V \]

Subthreshold region

\[ I_{on} \propto V_g - V_{th} \]

Threshold Voltage

\( V_{th} \) (Threshold Voltage)
Subthreshold leakage current

Electron Energy Boltzmann statics

Exp (qV/kT)

Lg → 1/2
Vd, Vg → 1/2
Vth → 1/2

However
Ioff → 10^3 in this example

Because of log-linear dependence
Subthreshold leakage current of MOSFET

Subthreshold Leakage Current

$\text{loff} \propto \exp aVg$

$Vg=0V$

Subthreshold region

$\text{Ion} \propto Vg - Vth$

Subthreshold Current

Is OK at Single Tr. level

But not OK For Billions of Trs.
3. Subthreshold current between S and D

Solution: however very difficult

Keep Vth as high as possible

- Do not decrease supply voltage, Vd

→ However, punchthrough enhanced

- Suppress variability in Vth

Thus, subthreshold current will limit the downsizing, especially for mobile devices
The limit is different depending on application.
How far can we go for production?

Past: 0.7 times per 2.5 years

10μm → 8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm → 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

Now: (28nm) → 22nm → 14nm

Future:

- Limit depending on applications
- Fundamental limit
- Subthreshold punchthrough
- Direct-tunnel

- At least 4.5 generations to 8 ~ 5 nm
However, careful about the name of technology!

Recently, Gate length (Lg) is much larger than the Technology name

22 nm Technology by Intel

Lg (Gate length) = 30 nm (HP), 34 nm (MP), 34 nm or larger (SP)

IEDM 2012, VLSI 2013

14 nm Technology by Global

Lg (Gate length) = 25 nm Euro SOI 2014

10 nm Technology by Leti (FD-SOI)

Lg (Gate length) = 15 nm
ITRS 2013 (Just published in April 2014)

<table>
<thead>
<tr>
<th>Year</th>
<th>2013</th>
<th>2015</th>
<th>2017</th>
<th>2019</th>
<th>2021</th>
<th>2023</th>
<th>2025</th>
<th>2027</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Commercial name (nm)</strong></td>
<td>14</td>
<td>10</td>
<td>7</td>
<td>5</td>
<td>3.5</td>
<td>2.5</td>
<td>1.8</td>
<td>1.3</td>
</tr>
<tr>
<td><strong>Metal half pitch (nm)</strong></td>
<td>40</td>
<td>32</td>
<td>25.3</td>
<td>20</td>
<td>15.9</td>
<td>12.6</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td><strong>$L_g$ (nm)</strong></td>
<td>20.2</td>
<td>16.8</td>
<td>14.0</td>
<td>11.7</td>
<td>9.7</td>
<td>8.1</td>
<td>6.7</td>
<td>5.6</td>
</tr>
<tr>
<td>($L_g$ for ITRS 2007)</td>
<td>(13)</td>
<td>(10)</td>
<td>(8)</td>
<td>(6)</td>
<td>(5)</td>
<td>(4.5 in 2022)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>$L_g$ for low stand by power (nm)</strong></td>
<td>23</td>
<td>19</td>
<td>16</td>
<td>13.3</td>
<td>11.1</td>
<td>9.3</td>
<td>7.7</td>
<td>6.4</td>
</tr>
<tr>
<td><strong>$V_{dd}$ (V)</strong></td>
<td>0.86</td>
<td>0.83</td>
<td>0.80</td>
<td>0.77</td>
<td>0.74</td>
<td>0.71</td>
<td>0.68</td>
<td>0.65</td>
</tr>
<tr>
<td>($V_{dd}$ (V) for ITRS 2007)</td>
<td>(0.90)</td>
<td>(0.80)</td>
<td>(0.70)</td>
<td>(0.70)</td>
<td>(0.65)(0.65 in 2022)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>EOT (nm)</strong></td>
<td>0.80</td>
<td>0.73</td>
<td>0.67</td>
<td>0.61</td>
<td>0.56</td>
<td>0.51</td>
<td>0.47</td>
<td>0.43</td>
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<tr>
<td>(EOT (nm) for ITRS 2007)</td>
<td>(0.60)</td>
<td>(0.60)</td>
<td>(0.55)</td>
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</table>
The rate for the shrinkage for the gate length and line pitch will be larger than 0.7 in near future, because of the subthreshold leakage, and also because of the delay in EUV lithography.

As a result, we will have more technology generations until reaching the downsizing limit, and the time to reach the limit will be delayed.
How far can we go for production?

Thus, we may go down to “1.5 nm” technology node by choosing whatever gate length we want for the application.
More Moore to More More Moore

Technology node

Now
65nm  45nm  32nm  22nm
Lg 35nm  30nm

Future
15nm, 11nm, 8nm, 5nm, 3nm
(Fin,Tri, Nanowire)

Si
Planar

Si is still main stream for future !!

ET: Extremely Thin

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)

Others

Alternative (III-V/Ge)
Channel FinFET

Emerging
Devices
High-k gate dielectrics

Hf-based oxides

| 45nm EOT:1nm | 32nm EOT:0.95nm | 22nm EOT:0.9nm | 15nm, 11nm, 8nm, 5nm, 3nm, |

SiO₂ IL (Interfacial Layer) is used at Si interface to realize good mobility

Technology for direct contact of high-k and Si is necessary

EOT=0.52 nm
Remote SiO₂-IL scavenging HfO₂ (IBM)

EOT=0.37nm
EOT=0.40nm
EOT=0.48nm

0.48 → 0.37nm Increase of Iₖ at 30%

Direct contact with La-silicate (Tokyo. Tech.)

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM2009, (IBM)
High-k is very important, however very difficult.

Thickness (EOT) decreased only 0.05 nm (or 0.5 Å, or 1 atom layer) for every generation.
How far can we go for production?

Rather than I\textsubscript{off} value, ion/I\textsubscript{off} ratio is important.

Now, ion/I\textsubscript{off} ratio is typically $10^6$.

However, it degrades significantly with decrease in V\textsubscript{supply}.
$I_{\text{ON}}$ and $I_{\text{OFF}}$ benchmark

### NMOS

- **Intel** [a]: Bulk 32nm, $V_{DD}=0.8V$
- **Intel** [a]: Tri-Gate 22nm, $V_{DD}=0.8V$
- **Intel** [b]: Bulk 45nm, $V_{DD}=1V$
- **Samsung** [c]: Bulk 20nm, $V_{DD}=0.9V$
- **IBM** [d]: GAA NW, $V_{DD}=1V$
- **IBM** [e]: GAA NW, $V_{DD}=0.9V$
- **IBM** [f]: GAA NW, $V_{DD}=1.1V$
- **STMicro.** [h]: GAA NW, $V_{DD}=1.1V$
- **IBM** [j]: ETSOI, $V_{DD}=0.9V$
- **IBM** [g]: ETSOI, $V_{DD}=1V$

### PMOS

- **Intel** [a]: Bulk 32nm, $V_{DD}=0.8V$
- **Intel** [b]: Bulk 45nm, $V_{DD}=1V$
- **Intel** [a]: Tri-Gate 22nm, $V_{DD}=0.8V$
- **IBM** [g]: ETSOI, $V_{DD}=0.9V$
- **IBM** [f]: FinFET 25nm, $V_{DD}=1V$
- **Samsung** [c]: Bulk 20nm, $V_{DD}=0.9V$
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[a] C. Auth et al., pp.131, VLSI2012 (Intel).  
[d] S. Saitoh et al., pp.11, VLSI2012 (Toshiba).  
[g] A. Khakifirooz et al., pp.117, VLSI2012 (IBM).  
Nanowire/Tri gate MOSFETs have advantage not only suppressing Ioff, but also for increasing Ion over planer MOSFETs

1. Because of higher mobility due to lower vertical electric field

2. Because of higher carrier density at the round corner
The graph illustrates the effective electron mobility (cm²/Vs) as a function of inversion carrier density (cm⁻²) for different structures labeled as A₁, A₂, and B. The structures are characterized by their dimensions:

- **A₁**: (12x19) \( h_{NW} \times w_{NW} \) (nm²)
- **A₂**: (12x28) \( h_{NW} \times w_{NW} \) (nm²)
- **B**: (20x10) \( h_{NW} \times w_{NW} \) (nm²)

The SOI planar with \( T_{SOI} = 28 \) nm and BOX thickness \( T_{BOX} = 28 \) nm is also indicated.

The images on the right show the nanowire structures with dimensions:

- **A₁**: 20 nm height, 12 nm width, 19 nm thickness
- **B**: 20 nm height, 20 nm width, 10 nm thickness

This graph likely represents the electrical performance of nanowire devices under different conditions.
Electron Density
\((x10^{19}\text{cm}^{-3})\)

Edge portion

Flat portion

Distance from SiNW Surface (nm)

41
3. Now Problems for downsizing!

We have to decrease Si layer thickness to better control of channel potential by gate bias when we decrease the gate length.

Significant decrease in conduction or Ion.
### ITRS 2013

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Short-channel effect

T. Skotnicki, IEDM 2009 Short Course (STMicroelectronics)

\[
\text{SCE} = 0.64 \frac{\varepsilon_s}{\varepsilon_{ox}} \times EI \times \Phi_d \\
\text{DIBL} = 0.8 \frac{\varepsilon_s}{\varepsilon_{ox}} \times EI \times V_{ds}
\]

\[
EI = 1 \times \left(1 + \frac{X_j^2}{L_{el}^2}ight) \times \frac{T_{ox} T_{dep}}{L_{el} L_{0l}^2}
\]

if max ch. doping is 10^{19} cm^{-3} => T_{ox} = 12 nm

if max ch. doping is 10^{20} cm^{-3} => T_{ox} = 12 nm

T_{box} = 145 nm

\[\lambda T_{box} = 18 \text{nm}\]

If Tsi ≈ 3 nm then:

\[\lambda T_{box} = 3 \text{nm}\]

If Tsi ≈ 3 nm then:

\[\lambda T_{box} = 0.46 \text{nm}\]

If Tsi = 10 nm

\[\lambda T_{box} = 6 \text{nm}\]

If Tsi = 10 nm

\[\lambda T_{box} = 2.7 \text{nm}\]

\[
\begin{align*}
\text{L}_{el,\min} &\approx 34 \text{nm} \\
\text{L}_{el,\min} &\approx 34 \text{nm} \\
\text{L}_{el,\min} &\approx 30 \text{nm} \\
\text{L}_{el,\min} &\approx 10 \text{nm} \\
\text{L}_{el,\min} &\approx 6 \text{nm} \\
\text{L}_{el,\min} &\approx 2.7 \text{nm}
\end{align*}
\]

(DIBL=100mV/V)
Mobility degradation for small diameter nanowire FETs, because channel carriers become too close to all surrounding nanowire surface, and scattered strongly.
Problems in Multi-gate

Need to decrease diameter for SCH

Decreasing the diameter of NW

Improved short-channel control

Severe mobility degradation

Significant $\mu$ degradation at diameter $< 10$ nm

S. Bangsaruntip et al., pp.297, IEDM2009 (IBM),
K. Tachi et al., pp.313, IEDM2009 (CEA-LETI)
Problems in SOI

K. Uchida et al., pp.47, IEDM2002 (Toshiba)

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.

![Graph showing mobility vs. SOI thickness for nMOS and pMOS transistors.](image)
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

1. Mobility degradation
   Extremely small distance between the electron and all around Si surface.
   Strong scattering of electrons by interaction with all around Si surface.

2. Electron density decrease
   Decrease of DOS in extremely narrow wire.

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-k is necessary.
Carrier density degradation for small diameter nanowire FET, because of the decrease in density of states.
Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

300 K

- $E_g = 1.12 \text{ eV}$
- $E_L = 2.0 \text{ eV}$
- $E_X = 1.2 \text{ eV}$
- $E_{so} = 0.044 \text{ eV}$
- $E_n = 3.4 \text{ eV}$
- $E_{T2} = 4.2 \text{ eV}$

Energy band of 3 x 3 Si wire

4 channels can be used
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Smaller wire/fin width is necessary for SCE suppression

But mobility and $I_{ON}$ severely degrade with wire/fin width reduction

Therefore even in multi-gate structures, EOT scaling should be accelerated to provide SCE immunity
New Materials!

High-k beyond 0.5 nm
To use high-k dielectrics

K: Dielectric Constant

Thin SiO$_2$

K=4

High-k dielectrics

K=20

Almost the same electric characteristics

Thick high-k dielectrics

5 times thicker

Small leakage Current

However, very difficult and big challenge!
**Choice of High-k elements for oxide**

### Candidates

<table>
<thead>
<tr>
<th>Unstable at Si interface</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>He</td>
<td></td>
</tr>
<tr>
<td>Li Be Na Mg</td>
<td>B C N O F Ne</td>
<td></td>
</tr>
<tr>
<td>Ca Sc K</td>
<td>Al Si P S Cl Ar</td>
<td></td>
</tr>
<tr>
<td>Rh Sr Y Zr Hf</td>
<td>La Ce Pr Nd O Pm</td>
<td></td>
</tr>
<tr>
<td>Cs Ba Fr Ra O Rf</td>
<td>O Ac Th Pa U O Np Pu O Am Cm Bk O Cf Es O Fm O Md O No O Lr</td>
<td></td>
</tr>
</tbody>
</table>

- **Si + MO\textsubscript{X} M + SiO\textsubscript{2}**
- **Si + MO\textsubscript{X} MSi\textsubscript{X} + SiO\textsubscript{2}**
- **Si + MO\textsubscript{X} M + MSi\textsubscript{X}O\textsubscript{Y}**

**HfO\textsubscript{2}** based dielectrics are selected as the first generation materials, because of their merit in:
1. band-offset,
2. dielectric constant
3. thermal stability

**La\textsubscript{2}O\textsubscript{3}** based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

XPS measurement by Prof. T. Hattori, INFOS 2003
Direct high-k/Si by silicate reaction

**HfO$_2$ case**

<table>
<thead>
<tr>
<th>Low $P_{O_2}$</th>
<th>High $P_{O_2}$</th>
</tr>
</thead>
</table>

**La$_2$O$_3$ case**

<table>
<thead>
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<th>High $P_{O_2}$</th>
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**Our approach**

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface.
Control of oxygen partial pressure is the key for processing.

$P_{O_2}$: Partial pressure of $O_2$ during high temperature annealing

K. Kakushima, et al., VLSI2010, p.69
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O* $\rightarrow$ HfO$_2$ + SiO$_2$

Oxygen supplied from W gate electrode

SiO$_x$-IL is formed after annealing
Oxygen control is required for optimizing the reaction

H. Shimizu, JJAP, 44, pp. 6131

D.J. Lichtenwalner, Trans. ECS 11, 319
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Physical mechanisms for small Dit

① silicate-reaction-formed fresh interface

② stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress


However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Cluster Chambers for HKMG Gate Stack

EB Deposition: HK

Sputter: MG

Flash Lamp
Anneal

ALD: HK

Robot

RTA

Entrance
ALD of La2O3


Precursor (ligand)

La(iPrCp)3

La(FAMD)3

ALD is indispensable from the manufacturing viewpoint - precise control of film thickness and good uniformity
Annealing temperature (°C)

EOT (nm)

Annealed for 2 s

La$_2$O$_3$(3.5 nm)

W(60 nm)

TiN/W(12 nm)

TiN/W(6 nm)

TiN(45nm)/W(6nm)

EOT=0.55nm

TaN/(45nm)/W(3nm)

900°C, 30min

EOT=0.55nm

Vg (V)

C_g (uF/cm$^2$)

Experiment

CVC fitting

Theory

-1 -0.5 0 0.5

0 0.5 1 1.5 2 2.5 3 3.5 4 4.5

0 0.5 1 1.5 2 2.5 3 3.5 4 4.5
Flat-band voltage (V)

EOT (nm)

TaN(45nm)/W(3nm)

\[ Q_{\text{fix}} = 1 \times 10^{11} \text{ cm}^{-2} \]

900°C, 30min

Fixed Charge density: \(1 \times 10^{11} \text{ cm}^{-2}\)
Our result at TIT

EOT = 0.40nm

L/W = 5/20μm
T = 300K
N_{sub} = 3 \times 10^{16} \text{cm}^{-3}

Electron Mobility \text{[cm}^2\text{/Vsec]}

E_{eff} [\text{MV/cm}]

EOT = 0.40\text{nm}
L/W = 5/20\mu\text{m}
T = 300\text{K}
N_{sub} = 3 \times 10^{16} \text{cm}^{-3}
**Benchmark of La-silicate dielectrics**

**Gate Leakage current**

- ITRS requirement
- Our data: La-silicate gate oxide

**Effective Mobility**

- Solid circle: Our data
- Open square: Hf-based oxides

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T. Ando, et al., (IBM) IEDM 2009, p.423
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Reliability: PBTI, NBTI, TDDB
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Flat metal/high-k interface for better mobility
- Workfunction engineering for \( V_{\text{th}} \) control
- Suppression of FLP
- Interface dipole control for \( V_{\text{th}} \) tuning
- Remove contamination introduced by CVD
- Thinning or removal of SiO\(_2\)-IL for small EOT
- Suppression of gate oxidation control
- Flat metal/high-k interface for better mobility
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k
Thank you very much for your attention.
Appendix
What is Next Revolution for Device Technology?

1900: Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

?: Nano Electronics
What is Next Revolution for Device Technology?

- 1900: Electronics
- 1970: Micro Electronics
- ?: Nano Electronics
  Maybe Not a Revolution
  But Great Innovention
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

? years

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?

70 years

? years
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?

70 years

70 years

70 years
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

2040: Braintronics
We do know system and algorithms are important!
But do not know how it can be by us for use of bio?
Long term roadmap for development

Source: H. Iwai, IPFA 2006

New Materials, New Process, New Structure

Hybrid integration of different functional Chip
 Increase of SOC functionality

3D integration of memory cell
  3D integration of logic devices

Miniaturization of Interconnects on PCB
  (Printed Circuit Board)

Low cost for LSI process
 Revolution for CR, Equipment

Introduction of algorithm of bio system
 Brain of insects, human

We do not know how?

Some time in 2020-2030

After 2040?
Braintronics for 2040’s

It’s a task for you,
For young generations!