New Materials and Structures for Sub-10 nm CMOS Devices

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Tokyo Institute of Technology
Background for nano-electronics
Feature Size / Technology Node

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm → 0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm → 90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm (2012) → 14 nm (2014)

From 1970 to 2013 (Last year)

- 43 years 1 generation
- 18 generations 2.5 years
- Line width: 1/450  Line width: 1/1.43 = 0.70
- Area: 1/200,000  Area: 1/2 = 0.5
Nano-Electronics

In 1990’s, people expected completely new mechanism or operational principle due the nano size, like quantum mechanical effects.

However, no fancy new operational principle has not yet been confirmed for logic application.

Thus, importance of Beyond CMOS technology is increasing as CMOS approaches its downsizing limit now.

However, we have to stick to conventional Si Nano CMOS technology until other one can replace it.

For the future conventional Si Nano CMOS, high-k, multi-gate, Schottky SD technologies are important.
Ballistic conduction will not happen even decreasing channel length.

Ballistic transport will never happen for MOSFET because of back scattering at drain.

With decreasing channel length, Drain current increase continue.

Also, 1D quantum conduction, or ballistic conduction will not happen. (1D quantum conduction: $77.8\mu S$ regardless of the length and material).
Until a few years ago.

Technology developments for conventional Si CMOS were done successfully.

Duration for generation shirked from 3 to 2 years.

People assume to reach the limit of gate length very soon – that is 5 or 3 nm
Then, now!.

Noticed that the technology is difficult.

Development of EUV (Extreme Ultra Violet) lithography delayed significantly.
Noticed that the technology is difficult.

In addition with the significant delay in EUV (Extreme Ultra Violet) lithography delayed significantly,

- Reduction of the thickness of High-k gate oxide becomes very difficult.

- Decreasing supply voltage becomes difficult because of subthreshold leakage and variability of the threshold voltage.
Now

Technology development delayed.

Shrink rate of gate length will become from 0.7 to 0.8 or 0.85.

Number of the semiconductor companies which can develop state of the art technology decreasing.

In the past, technologies come with the purchase of equipment's

But now, every companies are facing threat of dropping off, unless they concentrated on the development of technologies.

Thus, technology development is becoming much important.
Importance of nano-CMOS
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power consumption
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si

Source

Al Gate

Drain

Si

Si/SiO₂ Interface is extraordinarily good
1970,71: 1st generation of LSIs

DRAM  Intel 1103  

MPU  Intel 4004
In 2012

Most Recent SD Card

128GB (Bite)  
= 128G X 8bit  
= 1T(Tera)bit

1T = 10^{12} = 1 Trillion

World Population: 7 Billion  
Brain Cell: 10 \sim 100 Billion  
Stars in Galaxy: 100 Billion
128 GB = 1Tbit

2.4cm X 3.2cm X 0.21cm

Volume: 1.6 cm³  Weight: 2g

Voltage: 2.7 - 3.6V

Old Vacuum Tube:
5cm X 5cm X 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube: 5cm X 5cm X 10cm

$1 \text{Tbit} = 10,000 \times 10,000 \times 10,000 \text{ bit}$

Volume = $(5\text{cm} \times 10,000) \times (5\text{cm} \times 10,000) \times (10\text{cm} \times 10,000)$

$= 0.5\text{km} \times 0.5\text{km} \times 1\text{km}$

Pingan International Finance Center
Shanghai, China (Year 2016)

Indian Tower
Mumbai, India (Year 2016)

Burj Khalifa
Dubai, UAE (Year 2010)

500 m

700 m

828 m

1Tbit
Old Vacuum Tube: 50W

1Tbit = 10^{12}bit

Power = 0.05kW \times 10^{12} = 50 \text{ TW}

Nuclear Power Generator

1MkW = 1BW

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving
Brain: Integrated Circuits

Ear, Eye: Sensor

Mouth: RF/Opto device

Stomach: PV device

Hands, Legs: Power device
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years, even though, it is very matured market!!

2011  2025
300B USD  1,500B USD

Gartner: By K. Kim, CSTIC 2012
2. Current status of Si-CMOS device technologies
Downsizing

→ Decreasing size
→ Decreasing capacitance

Thus, important for

- decreasing cost, power
- increasing performance

per MOSFET or function
Question

What is the problem for downsizing?
The problem for downsizing
S and D distance small

→ Ion & Ioff increase

Ioff increase: Transistor cannot be turned-off.

Ioff (Off-leakage current) between S and D

1. Punch-through between S and D
2. Direct-tunneling between S and D
3. Subthreshold current between S and D
1. Punch-through between S and D
Problem for downsizing

$t_{ox}$ and $V_{dd}$ have to be decreased for better channel potential control $\rightarrow I_{OFF}$ Suppression
1. Punch-through between S and D

There are 3 solutions to suppress the depletion layer

A. Decrease supply voltage $\rightarrow$ Very difficult as explained later

B. Decrease tox to enhance the channel potential controllability by gate bias

C. Gate/channel configuration change to enhance the channel potential controllability by gate bias

Fin-FET, ET-SOI, etc.
B. Decrease tox

A. Toriumi (Tokyo Univ), IEDM 2006, Short Course

![Graph showing the decrease in tox over time with projections for scaling using high-K dielectrics and scaling limit of SiON.](image)
C. Configuration change for channel and gate structures for better control of channel potential.

Fin-FET, ET-SOI, etc.
Extremely Thin (or Fully-Depleted) SOI

- Make Si layer thin
- Control channel potential also from the bottom
Surrounding gate structure (Multiple gates)

- Make Si layer thin
- Control channel potential also by multiple gates not only from top & bottom but maybe also from side
New structures!

Multi-gate structures

- Fin
- Tri-gate
- Tri-gate (Variation)
- $\Omega$-gate
- All-around
Our work at TIT: Ω-gate Si Nanowire

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  
  \( \text{I}_{\text{ON}} \quad \text{I}_{\text{OFF}} \)
  
  - Drain Current (A)
  - Drain Current (A)
  - L\(_g\)=65nm
  - L\(_g\)=65nm
  - V\(_d\)=1V
  - V\(_d\)=1V
  - V\(_d\)=50mV
  - V\(_d\)=50mV

\( \text{L}_{\text{g}}=65\text{nm} \)

- DIBL of 62mV/V and SS of 70mV/dec for nFET
2. Direct-tunneling between S and D

Wave function of electron penetrates the channel potential barriers by quantum mechanical physics, when the channel length is around 3 nm.
Built-in potential between Source and Channel pn junction < 0.7 V

There is no solutions!

Downsizing limit is @ Lg = 3 nm.
3. Subthreshold current between S and D
Subthreshold leakage current of MOSFET

\[ I_{off} \propto \exp(aV_g) \]

\[ I_{on} \propto V_g - V_{th} \]

Subthreshold leakage current of MOSFET

\( V_g = 0 \text{V} \)

Subthreshold region

\( V_{th} \) (Threshold Voltage)
Subthreshold leakage current

Electron Energy
Boltzmann statics
Exp (qV/kT)

Lg → 1/2
Vd, Vg → 1/2
Vth → 1/2

However
Ioff → 10^3 in this example

Because of
log-linear dependence
Subthreshold leakage current of MOSFET

- **Subthreshold Leakage Current**: $I_{off} \propto \exp(aV_g)$
- **$V_g=0V$**: Subthreshold region
- **$I_{on} \propto V_g - V_{th}$**: Subthreshold Current Is OK at Single Tr. level
- **But not OK For Billions of Trs.**

Graph showing $I_d$ vs. $V_g$ with $V_{th}$ (Threshold Voltage) and $I_{on}$ orientation.
3. Subthreshold current between S and D

Solution: however very difficult

Keep Vth as high as possible

- Do not decrease supply voltage, Vd
  → However, punchthrough enhanced
- Suppress variability in Vth

Thus, subthreshold current will limit the downsizing, especially for mobile devices
The limit is different depending on application.
How far can we go for production?

**Past**

0.7 times per 2.5 years

\[ 10 \mu m \rightarrow 8 \mu m \rightarrow 6 \mu m \rightarrow 4 \mu m \rightarrow 3 \mu m \rightarrow 2 \mu m \rightarrow 1.2 \mu m \rightarrow 0.8 \mu m \rightarrow 0.5 \mu m \rightarrow 0.35 \mu m \rightarrow 0.25 \mu m \rightarrow 180 \text{nm} \rightarrow 130 \text{nm} \rightarrow 90 \text{nm} \rightarrow 65 \text{nm} \rightarrow 45 \text{nm} \rightarrow 32 \text{nm} \]

**Future**

- Subthreshold punchthrough
- Direct-tunnel

At least 4.5 generations to 8 ~ 5 nm

**Intermediate node**

\[(28 \text{nm}) \rightarrow 22 \text{nm} \rightarrow 14 \text{nm} \rightarrow 11.5 \text{nm} \rightarrow 8 \text{nm} \rightarrow 5.5 \text{nm}\]
However, careful about the name of technology!

Recently, Gate length (Lg) is much larger than the Technology name

**22 nm** Technology by Intel

Lg (Gate length) = 30 nm (HP), 34 nm (MP), 34 nm or larger (SP)

IEDM 2012, VLSI 2013

**14 nm** Technology by Global

Lg (Gate length) = 25 nm  
Euro SOI 2014

**10 nm** Technology by Leti (FD-SOI)

Lg (Gate length) = 15 nm
### ITRS 2013 (Just published in April 2014)

<table>
<thead>
<tr>
<th>Year</th>
<th>2013</th>
<th>2015</th>
<th>2017</th>
<th>2019</th>
<th>2021</th>
<th>2023</th>
<th>2025</th>
<th>2027</th>
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<tbody>
<tr>
<td><strong>Commercial name (nm)</strong></td>
<td>14</td>
<td>10</td>
<td>7</td>
<td>5</td>
<td>3.5</td>
<td>2.5</td>
<td>1.8</td>
<td>1.3</td>
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<tr>
<td><strong>Metal half pitch (nm)</strong></td>
<td>40</td>
<td>32</td>
<td>25.3</td>
<td>20</td>
<td>15.9</td>
<td>12.6</td>
<td>10</td>
<td>8</td>
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<tr>
<td><strong>$L_g$ (nm)</strong></td>
<td>20.2</td>
<td>16.8</td>
<td>14.0</td>
<td>11.7</td>
<td>9.7</td>
<td>8.1</td>
<td>6.7</td>
<td>5.6</td>
</tr>
<tr>
<td>(L$_g$ for ITRS 2007)</td>
<td>(13)</td>
<td>(10)</td>
<td>(8)</td>
<td>(6)</td>
<td>(5)</td>
<td>(4.5 in 2022)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>$L_g$ for low stand by power (nm)</strong></td>
<td>23</td>
<td>19</td>
<td>16</td>
<td>13.3</td>
<td>11.1</td>
<td>9.3</td>
<td>7.7</td>
<td>6.4</td>
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<tr>
<td><strong>$V_{dd}$ (V)</strong></td>
<td>0.86</td>
<td>0.83</td>
<td>0.80</td>
<td>0.77</td>
<td>0.74</td>
<td>0.71</td>
<td>0.68</td>
<td>0.65</td>
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<td>($V_{dd}$ (V) for ITRS 2007)</td>
<td>(0.90)</td>
<td>(0.80)</td>
<td>(0.70)</td>
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<td>(0.65)</td>
<td>(0.65 in 2022)</td>
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<tr>
<td><strong>EOT (nm)</strong></td>
<td>0.80</td>
<td>0.73</td>
<td>0.67</td>
<td>0.61</td>
<td>0.56</td>
<td>0.51</td>
<td>0.47</td>
<td>0.43</td>
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<tr>
<td>(EOT (nm) for ITRS 2007)</td>
<td>(0.60)</td>
<td>(0.60)</td>
<td>(0.55)</td>
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<td>(0.50 in 2022)</td>
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<td><strong>$T_{Si}$ (nm)</strong></td>
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<td>3.6</td>
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<td>2.5</td>
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<td>($T_{Si}$ (nm) for ITRS 2007)</td>
<td>(6.0)</td>
<td>(6.0)</td>
<td>(4.5)</td>
<td>(3.8)</td>
<td>(3.2)</td>
<td>(3.0 in 2022)</td>
<td></td>
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</tr>
</tbody>
</table>
The rate for the shrinkage for the gate length and line pitch will be larger than 0.7 in near future, because of the subthreshold leakage, and also because of the delay in EUV lithography.

As a result, we will have more technology generations until reaching the downsizing limit, and the time to reach the limit will be delayed.
How far can we go for production?

Thus, we may go down to “1.5 nm” technology node by choosing whatever gate length we want for the application.
More Moore to More More Moore

Technology node

<table>
<thead>
<tr>
<th></th>
<th>65nm</th>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>L&lt;sub&gt;g&lt;/sub&gt;</td>
<td>35nm</td>
<td></td>
<td>30nm</td>
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</tr>
</tbody>
</table>

Now

Future

15nm, 11nm, 8nm, 5nm, 3nm

(Fin,Tri, Nanowire)

Si

Planar

Tri-Gate

ET: Extremely Thin

Si channel

28nm

Si is still main stream for future !!

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)
High-k gate dielectrics

Continued research and development

SiO₂ IL (Interfacial Layer) is used at Si interface to realize good mobility

Technology for direct contact of high-k and Si is necessary

EOT=0.52 nm
Remote SiO₂-IL scavenging HfO₂ (IBM)

Hf-based oxides

<table>
<thead>
<tr>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
<th>15nm, 11nm, 8nm, 5nm, 3nm,</th>
</tr>
</thead>
<tbody>
<tr>
<td>EOT: 1nm</td>
<td>EOT: 0.95nm</td>
<td>EOT: 0.9nm</td>
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</tr>
</tbody>
</table>

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM2009, (IBM)

Direct contact with La-silicate (Tokyo Tech.)
High-k is very important, however very difficult.

Thickness (EOT) decreased only 0.05 nm (or 0.5 Å, or 1 atom layer) for every generation.
How far can we go for production?

Rather than $I_{off}$ value, $I_{on}/I_{off}$ ratio is important.

Now, $I_{on}/I_{off}$ ratio is typically $10^6$. However, it degrades significantly with decrease in $V_{supply}$. 
**ION and IOFF benchmark**

**NMOS**

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Technology</th>
<th>V_{DD}</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel [a]</td>
<td>Bulk 32nm</td>
<td>V_{DD}=0.8V</td>
<td></td>
</tr>
<tr>
<td>Intel [a]</td>
<td>Tri-Gate 22nm</td>
<td>V_{DD}=0.8V</td>
<td></td>
</tr>
<tr>
<td>Intel [b]</td>
<td>Bulk 45nm</td>
<td>V_{DD}=1V</td>
<td></td>
</tr>
<tr>
<td>Samsung [c]</td>
<td>Bulk 20nm</td>
<td>V_{DD}=0.9V</td>
<td></td>
</tr>
<tr>
<td>Tokyo Tech. [i]</td>
<td>Ω-gate NW</td>
<td>V_{DD}=1V</td>
<td></td>
</tr>
<tr>
<td>IBM [g]</td>
<td>ETSOIV</td>
<td>V_{DD}=1V</td>
<td></td>
</tr>
<tr>
<td>IBM [g]</td>
<td>FinFET 25nm</td>
<td>V_{DD}=1V</td>
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<tr>
<td>IBM [j]</td>
<td>ETSOI</td>
<td>V_{DD}=0.9V</td>
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<tr>
<td>IBM [j]</td>
<td>GAA NW</td>
<td>V_{DD}=0.9V</td>
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<tr>
<td>IBM [h]</td>
<td>GAA NW</td>
<td>V_{DD}=1.1V</td>
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<tr>
<td>STMicro. [h]</td>
<td>GAA NW</td>
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**PMOS**

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[a] C. Auth et al., pp.131, VLSI2012 (Intel).  
[d] S. Saitoh et al., pp.11, VLSI2012 (Toshiba).  
[g] A. Khakifirooz et al., pp.117, VLSI2012 (IBM).  
[i] S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)  
[j] K. Cheng et al., pp.419, IEDM2012 (IBM)
Nanowire/Tri gate MOSFETs have advantage not only suppressingloff, but also for increasing Ion over planer MOSFETs

1. Because of higher mobility due to lower vertical electric field

2. Because of higher carrier density at the round corner
Electron Density (x10^{19} cm^{-3})

Edge portion

Flat portion

Distance from SiNW Surface (nm)
3. Now Problems for downsizing!

We have to decrease Si layer thickness to better control of channel potential by gate bias when we decrease the gate length.

↓

Significant decrease in conduction or Ion.
## ITRS 2013

<table>
<thead>
<tr>
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<td><em>(TSi (nm) for ITRS 2007)</em></td>
<td>(6.0)</td>
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<td>(3.2)</td>
<td>(3.0 in 2022)</td>
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<td>(0.50 in 2022)</td>
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</tr>
</tbody>
</table>
# Short-channel effect

**T. Skotnicki, IEDM 2009 Short Course (STMicroelectronics)**

**Short-channel Effect (SCE):**

\[
SCE = 0.64 \frac{\varepsilon_s}{\varepsilon_{ox}} \times E_l \times \Phi_d
\]

**Deflection Induced Band-Loss (DIBL):**

\[
DIBL = 0.8 \frac{\varepsilon_s}{\varepsilon_{ox}} \times E_l \times V_{ds}
\]

<table>
<thead>
<tr>
<th>Type</th>
<th>SCE Formula</th>
<th>DIBL Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk</td>
<td>( E_l = 1 \times \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \times \frac{T_{ox} T_{dep}}{L_{el} L_{el}} )</td>
<td>( E_l = 1 \times \left( 1 + \frac{T_{si}^2}{L_{el}^2} \right) \times \frac{T_{ox} T_{si} + \lambda T_{box}}{L_{el} L_{el}} )</td>
</tr>
<tr>
<td>PD SOI</td>
<td>( E_l = 1 \times \left( 1 + \frac{T_{si}^2}{L_{el}^2} \right) \times \frac{T_{ox} T_{si} + \lambda T_{box}}{L_{el} L_{el}} )</td>
<td>( E_l = 1 \times \left( 1 + \frac{T_{si}^2}{L_{el}^2} \right) \times \frac{T_{ox} T_{si} + \lambda T_{box}}{L_{el} L_{el}} )</td>
</tr>
<tr>
<td>Thick BOX FD SOI</td>
<td>( E_l = 1 \times \left( 1 + \frac{T_{si}^2}{L_{el}^2} \right) \times \frac{T_{ox} T_{si} + \lambda T_{box}}{L_{el} L_{el}} )</td>
<td>( E_l = 1 \times \left( 1 + \frac{T_{si}^2 / 4}{L_{el}^2} \right) \times \frac{T_{ox} T_{si} / 2}{L_{el} L_{el}} )</td>
</tr>
<tr>
<td>UTBB (FD SOI or SON)</td>
<td>( E_l = 1 \times \left( 1 + \frac{T_{si}^2 / 4}{L_{el}^2} \right) \times \frac{T_{ox} T_{si} / 2}{L_{el} L_{el}} )</td>
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</tr>
<tr>
<td>FinFET (independent gates)</td>
<td>( E_l = 1 \times \left( 1 + \frac{T_{si}^2 / 4}{L_{el}^2} \right) \times \frac{T_{ox} T_{si} / 2}{L_{el} L_{el}} )</td>
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</tr>
<tr>
<td>FinFET (common gates)</td>
<td>( E_l = 1 \times \left( 1 + \frac{T_{si}^2 / 4}{L_{el}^2} \right) \times \frac{T_{ox} T_{si} / 2}{L_{el} L_{el}} )</td>
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</tr>
</tbody>
</table>

- **Le** = minimum length
- **DIBL** = deflection induced band loss

<table>
<thead>
<tr>
<th>Type</th>
<th>( Le_{min} ) (DIBL=100mV/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk</td>
<td>( \approx 30 \text{ nm} )</td>
</tr>
<tr>
<td>PD SOI</td>
<td>( \approx 30 \text{ nm} )</td>
</tr>
<tr>
<td>Thick BOX FD SOI</td>
<td>( \approx 10 \text{ nm} )</td>
</tr>
<tr>
<td>UTBB (FD SOI or SON)</td>
<td>( \approx 6 \text{ nm} )</td>
</tr>
<tr>
<td>FinFET (independent gates)</td>
<td>( \approx 2.7 \text{ nm} )</td>
</tr>
<tr>
<td>FinFET (common gates)</td>
<td>( \approx 2.7 \text{ nm} )</td>
</tr>
</tbody>
</table>
Drain-induced barrier lowering

\[ DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left(1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{DS} \]

- **BULK**
  - \( T_{dep} = \frac{3}{4} L_{el} \)
  - Xj = \( \frac{3}{4} L_{el} \)
  - 140 mV/V

- **III-V**
  - \( T_{ox} + 2A \)
  - \( \varepsilon_{si} + 15\% \)
  - 210 mV/V

- **FDSOI**
  - \( T_{dep} = T_{si}/2 \)
  - Xj = \( T_{si}/2 \)
  - \( T_{si} \geq 10\text{nm} \)

- **ETSOI**
  - \( T_{dep} = T_{si} + A T_{box} \)
  - Xj = \( T_{si} \geq 6\text{nm} \)

- **UTBB**
  - \( T_{dep} = T_{si}/2 \)
  - Xj = \( T_{si}/2 \)
  - \( T_{si} \geq 10\text{nm} \)

- **FinFET**
  - \( T_{dep} = T_{si}/2 \)
  - Xj = \( T_{si}/2 \)
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  - \( T_{dep} = T_{si}/2 \)
  - Xj = \( T_{si}/2 \)
  - \( T_{si} \geq 10\text{nm} \)
Sub-threshold Slope

T. Skotnicki, IEDM 2010 Short Course (STMicroelectronics)

\[ S = \frac{kT}{q} \ln \left( 1 + \frac{C_{\text{dep}}}{C_{\text{ox}}} + \frac{\varepsilon_{\text{Si}}}{\varepsilon_{\text{ox}}} \frac{T_{\text{ox}}}{L_{\text{el}}} \frac{X_j}{L_{\text{el}}} \left( 1 + \frac{3T_{\text{dep}}}{4L_{\text{el}}} \right) \sqrt{1 + 2 \frac{V_{ds}}{\Phi_d}} \right) \]

- BULK: 95 mV/dec
- III-V: 110 mV/dec
- ETSOI: 85 mV/dec
- UTBB: 75 mV/dec
- FinFET: 65 mV/dec

Subthreshold Slope

\( S \) - Subthreshold Slope

Log(Id) vs. \( V_g \)

\( T_{\text{dep}} = T_{\text{Si}} + \lambda T_{\text{box}} \)

\( X_j = T_{\text{Si}} \)

\( T_{\text{dep}} = T_{\text{Si}}/2 \)

\( X_j = T_{\text{Si}}/2 \)

RBB \( \Rightarrow \) Pstat
Mobility degradation for small diameter nanowire FETs, because channel carriers become too close to all surrounding nanowire surface, and scattered strongly.
Problems in Multi-gate

S. Bangsaruntip et al., pp.297, IEDM2009 (IBM),
K. Tachi et al., pp.313, IEDM2009 (CEA-LETI)

Decreasing the diameter of NW

Need to decrease diameter for SCH

Improved short-channel control

Severe mobility degradation

Significant $\mu$ degradation at diameter < 10 nm
Problems in SOI

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

$< 10 \text{ nm}$

1. Mobility degradation

Extremely small distance between the electron and all around Si surface.

Strong scattering of electrons by interaction with all around Si surface.

2. Electron density decrease

Decrease of DOS in extremely narrow wire.

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-k is necessary.
Carrier density degradation for small diameter nanowire FET, because of the decrease in density of states.
Number of quantum channels

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

By Prof. Shiraishi of Tsukuba univ.

4 channels can be used
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Wire cross section dependence.

What cross section gives best solution for SCE suppression and drive current?
Significant increase in $V_{th}$ variability with decreasing Fin width
Smaller wire/fin width is necessary for SCE suppression

But mobility and $I_{ON}$ severely degrade with wire/fin width reduction

Therefore even in multi-gate structures, **EOT scaling should be accelerated** to provide SCE immunity
New Materials!

High-k beyond 0.5 nm
To use high-k dielectrics

K: Dielectric Constant

Thin SiO$_2$

K=4

Almost the same electric characteristics

K=20

Thick high-k dielectrics

5 times thicker

Small leakage Current

Solution

However, very difficult and big challenge!
Combination of high-k and metal gate is important

\[ T_{\text{inv}} \approx \text{EOT} + 0.4 \text{nm} \]

Metal gate can eliminate the poly-Si depletion.

\[ \text{C}_{\text{metal}} \text{ is finite because of quantum effect. In other words, electron is not a point charge located at the interface but distributed charge.} \]

**Equivalent Oxide Thickness (EOT)**: gate dielectrics itself, \( \text{C}_{\text{ox}} \)

**Capacitance Equivalent Thickness (CET)**: entire gate stack,
Considering that channel carrier layer has equivalent capacitance of 0.5 nm, thinning of high-k until 0.4 or 0.3 nm is meaningful.
### Choice of High-k elements for oxide

#### Candidates

<table>
<thead>
<tr>
<th>H</th>
<th>Li</th>
<th>Be</th>
<th>Mg</th>
<th>Na</th>
<th>Ca</th>
<th>Sc</th>
<th>Ti</th>
<th>V</th>
<th>Cr</th>
<th>Mn</th>
<th>Fe</th>
<th>Co</th>
<th>Ni</th>
<th>Cu</th>
<th>Zn</th>
<th>Ga</th>
<th>Ge</th>
<th>As</th>
<th>Se</th>
<th>Br</th>
<th>Kr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gas or liquid at 1000 K</td>
<td>○ Radio active</td>
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<tr>
<td>He</td>
<td>Ne</td>
<td>F</td>
<td>O</td>
<td>N</td>
<td>B</td>
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</tbody>
</table>

#### Unstable at Si interface

1. Si + MOₓ M + SiO₂
2. Si + MOₓ MSiₓ + SiO₂
3. Si + MOₓ M + MSiₓOᵧ

<table>
<thead>
<tr>
<th>Choice of High-k elements for oxide</th>
</tr>
</thead>
<tbody>
<tr>
<td>HfO₂ based dielectrics are selected as the first generation materials, because of their merit in 1) band-offset, 2) dielectric constant 3) thermal stability</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer</th>
</tr>
</thead>
</table>

R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band offset

Oxide

Si

Band Discontinuity [eV]

Dielectric Constant \( \varepsilon(0) \)

XPS measurement by Prof. T. Hattori, INFOS 2003
Direct high-k/Si by silicate reaction

Our approach

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface. Control of oxygen partial pressure is the key for processing.

PO$_2$: Partial pressure of O$_2$ during high temperature annealing

K. Kakushima, et al., VLSI2010, p.69
SiO$_x$-IL growth at HfO$_2$/Si Interface

XPS Si1s spectrum

**Phase separator**

\[
\text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2
\]

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Tans. ECS 11, 319

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$Si$_4$O$_{36}$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Physical mechanisms for small $D_{it}$

1. Silicate-reaction-formed fresh interface

2. Stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress


However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Cluster tool for HKMG Stack

- EB Deposition for HK
- Flash Lamp
- Sputter for MG
- Robot
- ALD
- RTA
- Entrance

5m

82
ALD of La2O3


Precursor (ligand)

La(iPrCp)3

La(FAMD)3

1 cycle

ALD is indispensable from the manufacturing viewpoint - precise control of film thickness and good uniformity.
Annealing temperature (°C)

EOT (nm)

Annealed for 2 s
La$_2$O$_3$(3.5 nm)

W(60 nm)

TiN/W(6 nm)

TiN(45nm)/W(6nm)

Annealing temperature (°C)

EOT=0.55nm

-1 -0.5 0 0.5

Vg (V)

Cg (μF/cm$^2$)

Experiment

Theory

EOT=0.55nm

TaN/(45nm)/W(3nm)

900°C, 30min

EOT=0.55nm
TaN(45nm)/W(3nm)

Flat-band voltage (V)

EOT (nm)

$Q_{fix} = 1 \times 10^{11} \text{ cm}^{-2}$

900°C, 30min

Fixed Charge density: $1 \times 10^{11} \text{ cm}^{-2}$
Our Work at TIT: High-k

Our result at TIT

\[ EOT = 0.40 \text{nm} \]

\[ \text{Electron Mobility} \left[ \text{cm}^2/\text{Vsec} \right] \]

L/W = 5/20\( \mu \)m
T = 300K
\( N_{\text{sub}} = 3 \times 10^{16} \text{cm}^{-3} \)
Benchmark of La-silicate dielectrics

**Gate Leakage current**

- ITRS requirement
- Our data: La-silicate gate oxide

**Effective Mobility**

- Solid circle: Our data
- Open square: Hf-based oxides

T. Ando, et al., (IBM) IEDM 2009, p.423
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Flat metal/high-k interface for better mobility
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Interface dipole control for $V_{th}$ tuning
- Suppression of FLP
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
- Reliability: PBTI, NBTI, TDDB
- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Suppression of gate leakage current
- Endurance for high temperature process
Conclusions 1

Downsizing of MOSFETs is still important for high-speed low-power operation of logic LSIs.

Ioff will limit the downsizing.

Punchthrough component of Ioff will be suppressed by thinning tox and adopting new configuration such as FinFET or nanowire FET.

Direct tunneling will limit the downsizing @Lg = 3 nm.

Even before that, subthreshold leakage would limit the downsizing @Lg > 3nm, depending on the application.
Conclusions 2

In the application, Ion/Ioff ratio is important.

The ratio is typically $10^6$ for the present devices, however, it degrades significantly with decreasing the supply voltage.

Si nanowire FET has advantage not only on Ioff over planer FET, but also on Ion, because of better mobility and higher channel carrier density.

In order to suppress Ioff with decrease in Lg, the diameter of nanowire, width of fin, or thickness of Si film of SOI need to be shirked.

However, with decreasing the above diameter, width or thickness less than several nano-meter, very significant decrease in Ion occurs, because of the degradation on mobility and carrier concentration.
Conclusions 3

If the diameter, width or thickness cannot be decreased, we need to decrease the EOT of high-k aggressively in order to suppress Ioff.

High-k EOT reduction trend is very slow – 0.05 nm for each generation --, for the moment.

The limit of EOT scaling is expected to be around 0.4 nm or so, considering the additional capacitances of channel and metal gate.

By changing the high-k material from HfO$_2$ to La-silicate, we can obtain the good operation of MOSFET with EOT = 0.4 nm,

· Metal silicide Shottoky S/D will become important in order to suppress the S/D encroachment to the channel by dopant diffusion.
Conclusions 3

Downsizing of MOFET is becoming more and more important for low power high performance application in the future smart society, and will be accomplished in another 10 to 15 years, although the rate of the downsizing will become slow.

Thus, many challenging technology development will be necessary for another 10 to 15 years.
Thank you very much for your attention.
Appendix
What is Next Revolution for Device Technology?

1900: Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

?: Nano Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

?: Nano Electronics
Maybe Not a Revolution
But Great Innovation
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

? years

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

\[ \downarrow \]

70 years

1970: Micro Electronics

\[ \downarrow \]

\[ ? \text{ years} \]

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

70 years

1970: Micro Electronics

70 years

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

2040: Braintronics
We do know system and algorithms are important!
But do not know how it can be by us for use of bio?
Long term roadmap for development

Source: H. Iwai, IPFA 2006

New Materials, New Process, New Structure

Hybrid integration of different functional Chip
Increase of SOC functionality

3D integration of memory cell
3D integration of logic devices

Miniaturization of Interconnects on PCB
(Printed Circuit Board)

Low cost for LSI process
Revolution for CR, Equipment

Introduction of algorithm
of biosystem
Brain of insects, human

After 2040?
We do not know how?
Braintronics

Some time in 2020-2030
Braintronics for 2040’s

It’s a task for you,
For young generations!