Future of Nano-CMOS Technology

Hiroshi Iwai

Frontier Research Center
Tokyo Institute of Technology

January 20, 2014,
DL Talk at URV (Universitat Rovira i Virgili), Tarragona, Spain
Background for nano-electronics
Feature Size / Technology Node

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm →
0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm →
90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm (2012)

From 1970 to 2013 (Last year)

43 years 1 generation
18 generations 2.5 years
Line width: 1/450 Line width: 1/1.43 = 0.70
Area: 1/200,000 Area: 1/2 = 0.5
Nano-Electronics

In 1990’s, people expected completely new mechanism or operational principle due the nano size, like quantum mechanical effects.

However, no fancy new operational principle has not yet been confirmed for logic application.

Thus, importance of Beyond CMOS technology is increasing as CMOS approaches its downsizing limit now.

However, we have to stick to conventional Si Nano CMOS technology until other one can replace it.

For the future conventional Si Nano CMOS, high-k, multi-gate, Schottky SD technologies are important.
Ballistic conduction will not happen even decreasing channel length.

$L >> \lambda$

**Diffusive transport**

$L \sim \lambda$

**Quasi-Ballistic transport**

$L < \lambda$

**Ballistic transport**

Ballistic transport will never happen for MOSFET because of back scattering at drain.

With decreasing channel length, Drain current increase continue.

Also, 1D quantum conduction, or ballistic conduction will not happen. (1D quantum conduction: 77.8μS regardless of the length and material).
Until a few years ago.

Technology developments for conventional Si CMOS were done successfully.

Duration for generation shirked from 3 to 2 years.

People assume to reach the limit of gate length very soon – that is 5 or 3 nm
Then, now!

Noticed that the technology is difficult.

Development of EUV (Extreme Ultra Violet) lithography delayed significantly.

Reduction of the thickness of High-k gate oxide becomes very difficult.

Decreasing supply voltage becomes difficult because of subthreshold leakage and variability of threshold voltage.
Now

Technology development delayed.

Shrink rate of gate length will become from 0.7 to 0.8 or 0.85.

Number of the semiconductor companies which can develop state of the art technology decreasing.

In the past, technologies come with the purchase of equipment's

But now, every companies are facing threat of dropping off, unless they concentrated on the development of technologies.

Thus, technology development is becoming much important.
Importance of nano-CMOS
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si Source  Al Gate  Drain  Si

Si/SiO₂ Interface is extraordinarily good

Al  SiO₂  Si
1970,71: 1st generation of LSIs

DRAM   Intel 1103

MPU    Intel 4004
In 2012

Most Recent SD Card

128GB (Bite)
= 128G X 8bit
= 1T (Tera)bit

1T = 10^{12} = 1 Trillion

World Population: 7 Billion
Brain Cell: 10 ~ 100 Billion
Stars in Galaxy: 100 Billion
128 GB = 1Tbit

2.4cm × 3.2cm × 0.21cm

Volume: 1.6 cm³  Weight: 2g

Voltage: 2.7 - 3.6V

Old Vacuum Tube:
5cm × 5cm × 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube: 
5cm X 5cm X 10cm

1Tbit = 10,000 X 10,000 X 10,000 bit

Volume = (5cm X 10,000) X (5cm X 10,000) X (10cm X 10,000) 
= 0.5km X 0.5km X 1km

Pingan International Finance Center
Shanghai, China (Year 2016)

Indian Tower
Mumbai, India (Year 2016)

Burj Khalifa
Dubai, UAE (Year 2010)

500 m

1,000 m

1Tbit
Old Vacuum Tube: 50W

1Tbit = $10^{12}$ bit

Power = $0.05 \text{kW} \times 10^{12} = 50 \text{ TW}$

Nuclear Power Generator

1MkW = 1BW

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years, even though, it is very matured market!!

2011  
300B USD

→

2025  
1,500B USD

Gartner: By K. Kim, CSTIC 2012
2. Current status of Si-CMOS device technologies
Downsizing
→ Decreasing size
→ Decreasing capacitance

Thus, important for
Decreasing cost, power
Increasing performance
Question

What is the problem problem for downsizing?
The problem for downsizing

S and D distance small

→ Ion & Ioff increase

**Ioff increase: Transistor cannot be turned-off.**

**Ioff (Off-leakage current) between S and D**

1. Punch-through between S and D
2. Direct-tunneling between S and D
3. Subthreshold current between S and D
1. Punch-through between S and D
Problem for downsizing

Region governed by gate bias

Region governed by drain bias

DL touch with S
Region (DL)

Large $I_{OFF}$

No $t_{ox}$, $V_{dd}$ thinning

$0V < V_{dep} < 1V$

Large $I_{OFF}$ (Electron current)

$0V$

$t_{ox}$ and $V_{dd}$ have to be decreased for better channel potential control $\rightarrow I_{OFF}$ Suppression
1. Punch-through between S and D

There are solutions to suppress the depletion layer

1. Decrease supply voltage $\rightarrow$ Very difficult

   as explained later

2. Decrease tox to enhance the channel potential controllability by gate bias

3. Gate/channel configuration change to enhance the channel potential controllability by gate bias

   Fin-FET, ET-SOI, etc.
$L_{\text{gate}}$ and $t_{\text{ox}}$ (EOT) scaling trend

A. Toriumi (Tokyo Univ), IEDM 2006, Short Course
Configuration change for channel and gate structures for better control of channel potential.

Fin-FET, ET-SOI, etc.
Extremely Thin (or Fully-Depleted) SOI

- Make Si layer thin
- Control channel potential also from the bottom

Planar

ET (or FD) SOI
Surrounding gate structure (Multiple gates)

- Make Si layer thin
- Control channel potential also by multiple gates not only from top & bottom but maybe also from side

![Diagram of Planar and Multi gate structures](image-url)
Multi-gate structures

Fin

Tri-gate

Tri-gate (Variation)

Ω-gate

All-around
Our work at TIT: Ω-gate Si Nanowire

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  \(1.32 \text{ mA/µm @ } I_{\text{OFF}} = 117 \text{ nA/µm}\)
- DIBL of 62mV/V and SS of 70mV/dec for nFET
2. Direct-tunneling between S and D

Wave function of electron penetrates the channel potential barriers by quantum mechanical physics, when the channel length is around 3 nm.
There is no solutions!

Downsizing limit is @ $L_g = 3$ nm.
3. Subthreshold current between S and D
Subthreshold leakage current of MOSFET

\[ I_{on} \propto V_g - V_{th} \]

\[ I_{off} \propto \exp(aV_g) \]

Subthreshold Leakage Current

\( V_g = 0 \text{V} \)

Subthreshold region

\( V_{th} \) (Threshold Voltage)
Subthreshold leakage current

\[ I_d (A/\mu m) \]

\[ I_{on}, I_{off} \]

\[ 10^{-11}, 10^{-9}, 10^{-7}, 10^{-5} \]

\[ V_g (V), V_d, V_{th} \]

\[ 0.15 V, 0.3 V, 0.5 V, 1.0 V \]

Electron Energy
Boltzmann statics
Exp (qV/kT)

Lg \rightarrow 1/2
Vd, Vg \rightarrow 1/2
V_{th} \rightarrow 1/2

However
I_{off} \rightarrow 10^3 \text{ in this example}

Because of
log-linear dependence
Subthreshold leakage current of MOSFET

Subthreshold Leakage Current

$\text{loff} \propto \exp(aVg)$

$Vg=0V$

Subthreshold region

Threshold Voltage

$Vth$

$\text{ion} \propto Vg - Vth$

Subthreshold Current Is OK at Single Tr. level

But not OK For Billions of Trs.
3. Subthreshold current between S and D

Solution: however very difficult

Keep Vth as high as possible

- Do not decrease supply voltage, Vd
  → However, punchthrough enhanced
- Suppress variability in Vth

Thus, subthreshold current will limit the downsizing, especially for mobile devices
The limit is different depending on application.
How far can we go for production?

**Past**

0.7 times per 2.5 years

10μm → 8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm → 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

**Fundamental limit**

Limit depending on applications

Subthreshold punchthrough

Direct-tunnel

- At least 4,5 generations to 8 ~ 5 nm
However, careful about the name of technology!

Recently, Gate length (Lg) is much larger than the Technology name

**22 nm Technology by Intel**

Lg (Gate length) = 30 nm (HP), 34 nm (MP), 34 nm or larger (SP)

IEDM 2012, VLSI 2013

**14 nm Technology by Global**

Lg (Gate length) = 25 nm

Euro SOI 2014

**10 nm Technology by Leti (FD-SOI)**

Lg (Gate length) = 15 nm
The rate for the shrinkage for the gate length and line pitch will be larger than 0.7 in near future, because of the subthreshold leakage, and also because of the delay in EUV lithography.

As a result, we will have more technology generations until reaching the downsizing limit, and the time to reach the limit will be delayed.
How far can we go for production?

Thus, we may go down to “2 nm” technology by choosing whatever gate length we want for the application.
More Moore to More More Moore

Technology node
65nm | 45nm | 32nm | 22nm
Lg 35nm | 30nm

Now
15nm, 11nm, 8nm, 5nm, 3nm
(Fin, Tri, Nanowire)

Future

Si

Planar
Tri-Gate

28nm

Si is still main stream for future !!

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)

Others

Alternative (III-V/Ge)
Channel FinFET

Emerging Devices

ET: Extremely Thin
**High-k gate dielectrics**

Hf-based oxides

| 45nm EOT:1nm | 32nm EOT:0.95nm | 22nm EOT:0.9nm | 15nm, 11nm, 8nm, 5nm, 3nm, |

SiO₂ IL (Interfacial Layer) is used at Si interface to realize good mobility.

Technology for direct contact of high-k and Si is necessary.

Remote SiO₂-IL scavenging HfO₂ (IBM)

EOT=0.52 nm

Direct contact with La-silicate (Tokyo. Tech.)

0.48 → 0.37nm Increase of I_d at 30%

---

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM2009, (IBM)
High-k is very important, however very difficult.

Thickness (EOT) decreased only 0.05 nm (or 0.5 Å, or 1 atom layer) for every generation.
How far can we go for production?

Rather than loff value, Ion/loff ratio is important.

Now, Ion/loff ratio is typically $10^6$.

However, it degrades significantly with decrease in $V_{supply}$. 
Nanowire/Tri gate MOSFETs have advantage not only suppressing $I_{off}$, but also for increasing $I_{on}$ over planer MOSFETs

1. Because of higher mobility due to lower vertical electric field

2. Because of higher carrier density at the round corner
Electron Density (x10^{19} \text{cm}^{-3})

- Edge portion
- Flat portion

Distance from SiNW Surface (nm)
3. Now Problems for downsizing!

We have to decrease Si layer thickness to better control of channel potential by gate bias when we decrease the gate length.

Significant decrease in conduction or Ion.
## Short-channel effect

**T. Skotnicki, IEDM 2009 Short Course (STMicroelectronics)**

<table>
<thead>
<tr>
<th><strong>Type</strong></th>
<th><strong>SCE</strong></th>
<th><strong>DIBL</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk</td>
<td>$SCE = 0.64 \frac{\varepsilon_s}{\varepsilon_{ox}} \times EI \times \Phi_d$</td>
<td></td>
</tr>
<tr>
<td>PD SOI</td>
<td>$\times T_{dep}$</td>
<td>$DIBL = 0.8 \frac{\varepsilon_s}{\varepsilon_{ox}} \times EI \times V_{ds}$</td>
</tr>
<tr>
<td>Thick BOX FD SOI</td>
<td>$\times T_{dep}$</td>
<td></td>
</tr>
<tr>
<td>UTBB (FD SOI or SON)</td>
<td>$\times T_{dep}$</td>
<td></td>
</tr>
<tr>
<td>FinFET (independent gates)</td>
<td>$\times T_{dep}$</td>
<td></td>
</tr>
<tr>
<td>FinFET (common gates)</td>
<td>$\times T_{dep}$</td>
<td></td>
</tr>
</tbody>
</table>

**EI**

<table>
<thead>
<tr>
<th><strong>Type</strong></th>
<th><strong>EI</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk</td>
<td>$E1 \times 1$</td>
</tr>
<tr>
<td>PD SOI</td>
<td>$E1 \times 1$</td>
</tr>
<tr>
<td>Thick BOX FD SOI</td>
<td>$E1 \times 1$</td>
</tr>
<tr>
<td>UTBB (FD SOI or SON)</td>
<td>$E1 \times 1$</td>
</tr>
<tr>
<td>FinFET (independent gates)</td>
<td>$E1 \times 1$</td>
</tr>
<tr>
<td>FinFET (common gates)</td>
<td>$E1 \times 1$</td>
</tr>
</tbody>
</table>

If max ch. doping is $10^{15} \text{cm}^{-3} =\to T_{ch} \approx 12 \text{nm}$:

- **Tbox** = 145nm
- $\lambda Tbox = 18 \text{nm}$

If Tsi min $\approx 3 \text{nm}$:

- **Tbox** = 10nm
- $\lambda Tbox = 3 \text{nm}$

If Tsi min $\approx 3 \text{nm}$, then:

- **Tbox** = 10nm
- $\lambda Tbox = 0.46 \text{nm}$

- Tsi/2 plays role of $X_j$, and that of Ddep, if minimum feasible Tsi is supposed 3nm, then:

**LeL, min**

<table>
<thead>
<tr>
<th><strong>Type</strong></th>
<th><strong>LeL, min</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk</td>
<td>$= 34 \text{nm}$</td>
</tr>
<tr>
<td>PD SOI</td>
<td>$= 34 \text{nm}$</td>
</tr>
<tr>
<td>Thick BOX FD SOI</td>
<td>$\approx 30 \text{nm}$</td>
</tr>
<tr>
<td>UTBB (FD SOI or SON)</td>
<td>$\approx 10 \text{nm}$</td>
</tr>
<tr>
<td>FinFET (independent gates)</td>
<td>$\approx 6 \text{nm}$</td>
</tr>
<tr>
<td>FinFET (common gates)</td>
<td>$\approx 2.7 \text{nm}$</td>
</tr>
</tbody>
</table>
Drain-induced barrier lowering

\[ DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{DS} \]

**T. Skotnicki, IEDM 2010 Short Course (STMicroelectronics)**

**BULK**
- \( T_{dep} = \frac{3}{4} L_{el} \)
- \( X_j = \frac{3}{4} L_{el} \)
- \( 140 \text{ mV/V} \)

**III-V**
- \( T_{ox} + 2A \)
- \( \varepsilon_{Si} + 15\% \)
- \( 210 \text{ mV/V} \)

**FDSOI**
- \( T_{dep} = T_{si}/2 \)
- \( X_j = T_{si}/2 \)
- \( T_{si} \geq 10 \text{ nm} \)

**ETSOI**
- \( 110 \text{ mV/V} \)

**UTBB**
- \( 80 \text{ mV/V} \)

**FinFET**
- \( 70 \text{ mV/V} \)

**Log(\text{Id})**

\( V_{dd} \rightarrow 0.1 \text{ V} \)

\( V_{gg} \)
Sub-threshold Slope

\[
S = \frac{kT}{q} \ln\left(1 + \frac{C_{\text{dep}}}{C_{\text{ox}}} + \frac{\varepsilon_{\text{Si}} T_{\text{ox}} X_j}{\varepsilon_{\text{ox}} L_{\text{el}} L_{\text{el}}} \left(1 + \frac{3 T_{\text{dep}}}{4 L_{\text{el}}} \right) \frac{V_{\text{ds}}}{\Phi_d} \right)
\]

- BULK: \( T_{\text{dep}} = 3/4 L_{\text{el}}, X_j = 3/4 L_{\text{el}} \) - 95 mV/dec
- III-V: \( T_{\text{ox}} + 2A \varepsilon_{\text{Si}} + 15\% \) - 110 mV/dec
- ETSOI: \( T_{\text{dep}} = T_{\text{Si}}/2, X_j = T_{\text{Si}}/2 \) - 85 mV/dec
- UTBB: \( T_{\text{dep}} = T_{\text{Si}} + A T_{\text{box}} \) - 75 mV/dec
- FDSOI: \( X_j = T_{\text{Si}} \) - 65 mV/dec

Log(\( I_d \))

\( \Delta S \) - Subthreshold Slope

Vg
Mobility degradation for small diameter nanowire FETs, because channel carriers become too close to all surrounding nanowire surface, and scattered strongly.
Problems in Multi-gate

Decreasing the diameter of NW

Improved short-channel control

Severe mobility degradation

S. Bangsaruntip et al., pp.297, IEDM2009 (IBM),
K. Tachi et al., pp.313, IEDM2009 (CEA-LETI)

Need to decrease diameter for SCH

Significant $\mu$ degradation at diameter $< 10$ nm

PFET legend
$W$ (nm) / $H$ (nm)
- $\sim 5 / \sim 6$
- 6.8 / 9.5
- 9.0 / 13.9
- 11.2 / 20.0

NFET legend
$W$ (nm) / $H$ (nm)
- 6.8 / 9.5
- 12.3 / 15.1
- 16.5 / 22.1
- 21.6 / 23.8

Effective mobility [$\text{cm}^2/\text{Vs}$]

$N_{\text{inv}}$ [$\times 10^{13} \text{ cm}^{-2}$]
Problems in SOI

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

1. Mobility degradation
   Extremely small distance between the electron and all around Si surface.
   Strong scattering of electrons by interaction with all around Si surface.

2. Electron density decrease
   Decrease of DOS in extremely narrow wire.

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-k is necessary.
Carrier density degradation for small diameter nanowire FET, because of the decrease in density of states.
Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Wire cross section dependence.

What cross section gives best solution for SCE suppression and drive current?

By Profs. Oshiyama and Iwata, U. of Tokyo
Significant increase in $V_{th}$ variability with decreasing Fin width.
Smaller wire/fin width is necessary for SCE suppression

But mobility and $I_{ON}$ severely degrade with wire/fin width reduction

Therefore even in multi-gate structures, **EOT scaling should be accelerated** to provide SCE immunity
High-k beyond 0.5 nm
To use high-k dielectrics

K: Dielectric Constant

Thin SiO$_2$

\[ K=4 \]

Thick high-k dielectrics

\[ K=20 \]

Almost the same electric characteristics

5 times thicker

Small leakage Current

However, very difficult and big challenge!
Combination of high-k and metal gate is important

K. Natori, et al., (Tsukuba Univ) SSDM 2005, p.286

Equivalent Oxide Thickness (EOT): gate dielectrics itself, $C_{ox}$

Capacitance Equivalent Thickness (CET): entire gate stack,

Metal gate can eliminate the poly-Si depletion.

Inversion CET = $T_{inv} \approx EOT + 0.4\text{nm}$ with metal gate electrode

$C_{metal}$ is finite because of quantum effect. In other words electron is not a point charge located at the interface but distributed charge.
Considering that channel carrier layer has equivalent capacitance of 0.5 nm, thinning of high-k until 0.4 or 0.3 nm is meaningful.
Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>Unstable at Si interface</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
<th>He</th>
<th>B</th>
<th>C</th>
<th>N</th>
<th>O</th>
<th>F</th>
<th>Ne</th>
</tr>
</thead>
<tbody>
<tr>
<td>Li</td>
<td>Si + MO(_X) M + SiO(_2)</td>
<td>●</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
</tr>
<tr>
<td>Be</td>
<td>Si + MO(_X) MSi(_X) + SiO(_2)</td>
<td>●</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
</tr>
<tr>
<td>Na</td>
<td>Si + MO(_X) M + MSi(_X)O(_Y)</td>
<td>●</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
</tr>
</tbody>
</table>

La\(_2\)O\(_3\) based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

HfO\(_2\) based dielectrics are selected as the first generation materials, because of their merit in:
1) band-offset
2) dielectric constant
3) thermal stability

R. Hauser, IEDM Short Course, 1999
Dielectric Constant

SiO$_2$

Band Discontinuity [eV]

Leakage Current by Tunneling

Oxide

Si

Conduction band offset vs. Dielectric Constant

XPS measurement by Prof. T. Hattori, INFOS 2003

Si Band Gap

Dielectric Constant $\varepsilon(0)$
Direct high-k/Si by silicate reaction

HfO₂ case

Low $P_{O_2}$  
High $P_{O_2}$

SiO₂-IL

HfSiₓ  
(k~4)

Si substrate

La₂O₃ case

Low $P_{O_2}$  
High $P_{O_2}$

La₂O₃

silicate

La-rich  
Si-rich

Si substrate

Direct contact can be achieved with La₂O₃ by forming silicate at interface

Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

\[ \text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2 \]

H. Shimizu, JJAP, 44, pp. 6131

D.J. Lichtenwalner, Trans. ECS 11, 319

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction

Oxygen supplied from W gate electrode

TEM image 500 $^\circ$C 30min

$W$

HfO$_2$ $k=16$

SiO$_x$-IL $k=4$

1 nm

XPS Si1s spectrum

Intens. (a.u.)

Binding energy (eV)

500 $^\circ$C

SiO$_2$

Hf Silicate

Si sub.
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$  
$\rightarrow$  La$_2$SiO$_5$, La$_2$Si$_2$O$_7$,  
La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Physical mechanisms for small Dit

① silicate-reaction-formed fresh interface

② stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress


However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Cluster tool for HKMG Stack

- EB Deposition for HK
- Flash Lamp
- Sputter for MG
- Robot
- ALD
- Entrance
- RTA

5m

79
Cluster Chambers for HKMG Gate Stack

- EB Deposition: HK
- Flash Lamp Anneal
- Sputter: MG
- ALD: HK
- Entrance
- Robot
- RTA
ALD of La2O3


Precursor (ligand)

La(iPrCp)3

La(FAMD)3

ALD is indispensable from the manufacturing viewpoint - precise control of film thickness and good uniformity.
Annealed for 2 s
La$_2$O$_3$(3.5 nm)

W(60 nm)

TiN/W(6 nm)

Annealing temperature (°C)

EOT (nm)

0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0

600 700 800 900 1000

Vg (V)

Cg (uF/cm$^2$)

Experiment

Cvc fitting

EOT=0.55nm

TaN/(45nm)/W(3nm)

900°C, 30min

EOT=0.55nm

TiN/W(6 nm)
Flat-band voltage (V)

EOT (nm)

TaN(45nm)/W(3nm)

$Q_{fix} = 1 \times 10^{11} \text{ cm}^{-2}$

900$^\circ$C, 30min

Fixed Charge density: $1 \times 10^{11} \text{ cm}^{-2}$
Our Work at TIT: High-k

Our result at TIT

EOT = 0.40nm

- Drain Voltage (V)
- Drain Current (mA)
- Vg = 0.4V
- Vg = 0.6V
- Vg = 0.8V
- Vg = 1.0V
- Vg = 0.2V
- Vg = 0V
- L/W = 5/20μm
- T = 300K
- N_{sub} = 3 \times 10^{16} \text{cm}^{-3}

- Electron Mobility \text{ [cm}^2/\text{Vsec]\n
- EOT = 0.40nm
- L/W = 5/20μm
- T = 300K
- N_{sub} = 3 \times 10^{16} \text{cm}^{-3}
Benchmark of La-silicate dielectrics

Gate Leakage current

Effective Mobility


T. Ando, et al., (IBM) IEDM 2009, p.423
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Reliability: PBTI, NBTI, TDDB
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Suppression of FLP
- Interface dipole control for $V_{th}$ tuning
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
- Flat metal/high-k interface for better mobility
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k

Si-sub.

Metal

High-k

SiO$_2$-IL
Conclusions 1

Downsizing of MOSFETs is still important for high-speed low-power operation of logic LSIs.

Ioff will limit the downsizing.

Punchthrough component of Ioff will be suppressed by thinning tox and adopting new configuration such as FinFET or nanowire FET.

Direct tunneling will limit the downsizing @Lg = 3 nm.

Even before that, subthreshold leakage would limit the downsizing @Lg > 3nm, depending on the application.
Conclusions 2

In the application, Ion/Ioff ratio is important.

The ratio is typically $10^6$ for the present devices, however, it degrades significantly with decreasing the supply voltage.

Si nanowire FET has advantage not only on Ioff over planer FET, but also on Ion, because of better mobility and higher channel carrier density.

In order to suppress Ioff with decrease in Lg, the diameter of nanowire, width of fin, or thickness of Si film of SOI need to be shirked.

However, with decreasing the above diameter, width or thickness less than several nano-meter, very significant decrease in Ion occurs, because of the degradation on mobility and carrier concentration.
Conclusions 3

If the diameter, width or thickness cannot be decreased, we need to decrease the EOT of high-k aggressively in order to suppress Ioff.

High-k EOT reduction trend is very slow – 0.05 nm for each generation --, for the moment.

The limit of EOT scaling is expected to be around 0.4 nm or so, considering the additional capacitances of channel and metal gate.

By changing the high-k material from HfO$_2$ to La-silicate, we can obtain the good operation of MOSFET with EOT = 0.4 nm,

- Metal silicide Shottoky S/D will become important in order to suppress the S/D encroachment to the channel by dopant diffusion.
Conclusions 3

Downsizing of MOFET is becoming more and more important for low power high performance application in the future smart society, and will be accomplished in another 10 to 15 years, although the rate of the downsizing will become slow.

Thus, many challenging technology development will be necessary for another 10 to 15 years.
What is Next Revolution for Device Technology?

1900: Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

?: Nano Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

?: Nano Electronics
Maybe Not a Revolution
But Great Innovation
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?

? years
What is Next Revolution for Device Technology?

1900: Electronics

↓

70 years

1970: Micro Electronics

↓

? years

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

↓ 70 years

1970: Micro Electronics

↓ 70 years

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

2040: Braintronics
Braintronics

- Ultra small volume
- Small number of neuron cells
- Extremely low power
- Real time image processing
- (Artificial) Intelligence
- 3D flight control

Sensor
Infrared
Humidity
CO₂

Brain

Mosquito

Dragonfly brain has even further higher performance

We do know system and algorithms are important! But do not know how it can be by us for use of bio?
Long term roadmap for development

Source: H. Iwai, IPFA 2006

New Materials, New Process, New Structure

Hybrid integration of different functional Chip
Increase of SOC functionality

3D integration of memory cell
3D integration of logic devices

Miniaturization of Interconnects on PCB
(Printed Circuit Board)

Low cost for LSI process
Revolution for CR, Equipment

Introduction of algorithm of bio system
Brain of insects, human

We do not know how?

Due time in 2020 - 2030

After 2040?
Braintronics for 2040’s

It’s a task for you,
For young generations!
Thank you very much for your attention.