January 20, 2014,
DL Talk@ IIT-Bombay, Mumbai, India

Futur of Nano CMOS Technology

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Frontier Research Center
Tokyo Institute of Technology
Background for nano-electronics
1900 “Electronics” started.
Device: Vacuum tube
Device feature size: Several cm
Major Appl.: Amplifier (Radio, TV, Wireless etc.)

→ Technology Revolution

1970 “Micro-Electronics” started.
Device: Si MOS integrated circuits
Device feature size: 10 µm
Major Appl.: Digital (Computer, PC, etc.)

→ Technology Revolution
2000 “Nano-Electronics” started.

Device: Still, Si CMOS integrated circuits
Device feature size: 100 nm
Major Appl.: Digital (μ-processor, cell phone, etc.)

→Technology Revolution??

Maybe, just evolution and innovation!

But great evolution or innovations!

and so many innovations!
Now, 2014 “Nano-Electronics” continued.

Device: **Still, Si CMOS integrated circuits**

Device feature size: **a few 10 nm**

Major Appl.: Still Digital (µ-processor, cell phone, etc.)

**Still evolution and innovation.**
What is special or new for Nano-Electronics?

In 1990’s, people expected completely new mechanism or operational principle due the nano size, like quantum mechanical effects.

However, no fancy new operational principle was found.

At least for logic application, there is no success story for “Beyond CMOS devices” to replace Si-CMOS.

Of course, I do not deny the importance of Beyond CMOS technology development. It is becoming very important as CMOS approach its limit.
Ballistic conduction will not happen even decreasing channel length. 

\[ L >> \lambda \]  

Diffusive transport

\[ L \sim \lambda \]  

Quasi-Ballistic transport

\[ L < \lambda \]  

Ballistic transport

Ballistic transport will never happen for MOSFET because of back scattering at drain

With decreasing channel length, Drain current increase continue.

Also, 1D quantum conduction, or ballistic conduction will not happen. (1D quantum conduction: 77.8\(\mu\)S regardless of the length and material).
Today’s talk:

For VLSI designers, it would be interested to know the Nano CMOS future.

Prediction of Nano CMOS future

Until 10 years ago, Wulf boy.

Wolf (The limit of downsizing) will come very soon, but never.
Then, until a few years ago.

- Technology developments were done successfully.

- Duration for generation shirked from 3 to 2 years.

- People assume to reach fundamental limit of gate length at several to a few nm.
Feature Size / Technology Node

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm → 0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm → 90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm (2012)

From 1970 to 2013 (Last year)

43 years 1 generation
18 generations 2.5 years
Line width: 1/450 Line width: 1/1.43 = 0.70
Area: 1/200,000 Area: 1/2 = 0.5
Then, now!.

Noticed the technology is difficult.

Development of EUV (Extreme Ultra Violet) lithography delayed significantly.

Reduction of the thickness of High-k gate oxide becomes very difficult.

Decreasing supply voltage becomes very difficult because of subthreshold leakage and variability of threshold voltage.
Now

Technology development delayed.

Shrink rate of gate length will become from 0.7 to 0.8 or 0.85.

Number of the semiconductor companies which can develop state of the art technology decreasing.

In the past, technologies come with the purchase of equipment's

But now, every companies are facing threat of dropping off, unless they concentrated on the development of technologies.

Thus, technology development is becoming much important..
Importance of nano-CMOS
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power
consumption
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

Drain
Al Gate

Si

Si/SiO₂ Interface is extraordinarily good

Al
SiO₂
Si
1970,71: 1st generation of LSIs

DRAM  Intel 1103

MPU    Intel 4004
In 2012

Most Recent SD Card

128GB (Bite)
= 128G X 8bit
= 1T (Tera) bit

1T = 10^{12} = 1 Trillion

World Population: 7 Billion
Brain Cell: 10\sim100 Billion
Stars in Galaxy: 100 Billion
128 GB = 1Tbit

2.4cm X 3.2cm X 0.21cm

Volume: 1.6cm³  Weight: 2g

Voltage: 2.7 - 3.6V

Old Vacuum Tube:
5cm X 5cm X 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube: 5cm X 5cm X 10cm

Volume = (5cm X 10,000) X (5cm X 10,000) X (10cm X 10,000)
= 0.5km X 0.5km X 1km

1Tbit = 10,000 X 10,000 X 10,000 bit

Pingan International Finance Center
Shanghai, China (Year 2016)
700 m

Indian Tower
Mumbai, India (Year 2016)
700 m

Burj Khalifa
Dubai, UAE (Year 2010)
828 m

500 m
Old Vacuum Tube: 50W

1Tbit = $10^{12}$ bit

Power = $0.05 \text{kW} \times 10^{12} = 50 \text{ TW}$

Nuclear Power Generator

$1 \text{ MkW} = 1 \text{ BW}$

We need **50,000 Nuclear Power Plant** for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer **Tokyo Electric Power Company (TEPCO)** can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving
Brain: Integrated Circuits

Ear, Eye: Sensor

Mouth: RF/Opto device

Stomach: PV device

Hands, Legs: Power device
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years, even though, it is very matured market!!

2011
300B USD

2025
1,500B USD

Gartner: By K. Kim, CSTIC 2012
2. Current status of Si-CMOS device technologies
Downsizing

→ Decreasing size

→ Decreasing capacitance

Thus, important for

Decreasing cost, power

Increasing performance
Feature Size / Technology Node

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm→ 0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm → 90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm(2012)

From 1970 to 2013 (Last year)

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Line width: 1/450 Line width: 1/1.43 = 0.70
Area: 1/200,000 Area: 1/2 = 0.5
Question

What is the problem problem for downsizing?
The problem for downsizing

S and D distance small

→ Ion & Ioff increase

Ioff increase: Transistor cannot be turned-off.

Ioff (Off-leakage current) between S and D

1. Punch-through between S and D
2. Direct-tunneling between S and D
3. Subthreshold current between S and D
1. Punch-through between S and D
Problem for downsizing

Region governed by gate bias
Region governed by drain bias

Gate metal
Gate oxide

Source 0V
Channel

Substrate 0V

Drain 0V

0V < \( V_{\text{dep}} \) < 1V

Depletion Region (DL) by Drain Bias

DL touch with S Region (DL)

Large \( I_{\text{OFF}} \)

Large \( I_{\text{OFF}} \) (Electron current)

\( t_{\text{ox}} \) and \( V_{\text{dd}} \) have to be decreased for better channel potential control \( \rightarrow I_{\text{OFF}} \) Suppression
1. Punch-through between S and D

There are solutions to suppress the depletion layer:

1. Decrease supply voltage $\rightarrow$ Very difficult as explained later

2. Decrease tox to enhance the channel potential controllability by gate bias

3. Gate/channel configuration change to enhance the channel potential controllability by gate bias

Fin-FET, ET-SOI, etc.
Decrease tox

→ Increase the Electric field between Gate & Channel

→ Increase the channel potential controllability by gate bias.
  
  → Keep channel potential 0V

→ Suppress the depletion layer
$L_{\text{gate}}$ and $t_{\text{ox}}$ (EOT) scaling trend

A. Toriumi (Tokyo Univ), IEDM 2006, Short Course
Configuration change for channel and gate structures for better control of channel potential.

Fin-FET, ET-SOI, etc.
Extremely Thin (or Fully-Depleted) SOI

- Make Si layer thin
- Control channel potential also from the bottom

Planar

ET (or FD) SOI

Extremely thin Si

Drain bias induced depletion

SiO₂

Si
Surrounding gate structure (Multiple gates)

- Make Si layer thin
- Control channel potential also by multiple gates not only from top & bottom but maybe also from side

Planar

Multi gate

Drain bias induced depletion

Si fin or nanowire
Nanowire structures in a wide meaning

Fin
Tri-gate
Tri-gate (Variation)
Ω-gate
All-around
Our work at TIT: Ω-gate Si Nanowire

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  (1.32 mA/µm @ $I_{OFF}=117$ nA/µm)
- DIBL of 62mV/V and SS of 70mV/dec for nFET
2. Direct-tunneling between S and D

Wave function of electron penetrates the channel potential barriers by quantum mechanical physics, when the channel length is around 3 nm.
There is no solutions!

Downsizing limit is @ Lg = 3 nm.
3. Subthreshold current between S and D
Subthreshold leakage current of MOSFET

$\text{Subthreshold Leakage Current}$

$\text{loff} \propto \exp (aVg)$

$Vg=0\text{V}$

Subthreshold region

$\text{Ion} \propto Vg - V_{th}$

(Threshold Voltage)
Subthreshold leakage current

Electron Energy Boltzmann statics

Exp (qV/kT)

Lg $\rightarrow$ 1/2
Vd, Vg $\rightarrow$ 1/2
Vth $\rightarrow$ 1/2

However
loff $\rightarrow$ 10³ in this example

Because of log-linear dependence
Subthreshold leakage current of MOSFET

Subthreshold Leakage Current

$\text{loff} \propto \exp aVg$

$Vg=0V$

Subthreshold region

$V_{th}$ (Threshold Voltage)

$\text{Ion} \propto Vg - V_{th}$

Subthreshold Current Is OK at Single Tr. level

But not OK For Billions of Trs.
3. Subthreshold current between S and D

Solution: however very difficult

Keep Vth as high as possible

- Do not decrease supply voltage, Vd
  → However, punchthrough enhanced
- Suppress variability in Vth

Thus, subthreshold current will limit the downsizing, especially for mobile devices
The limit is different depending on application.
How far can we go for production?

**Past** 0.7 times per 2.5 years
10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm → 0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

Past

**Future**

- Limit depending on applications
- Subthreshold punchthrough
- Direct-tunnel
- Fundamental limit

Now

Intermediate node

- At least 4,5 generations to 8 ~ 5 nm
However, careful about the name of technology!

Recently, Gate length (Lg) is much larger than the Technology name.

**22 nm Technology by Intel**

Lg (Gate length) = **30 nm** (HP), **34 nm** (MP), **34 nm** or larger (SP)

IEDM 2012, VLSI 2013

**10 nm Technology by Leti (FD-SOI)**

Lg (Gate length) = **15 nm**

ECS 2013
The rate for the shrinkage for the gate length and line pitch will be larger than 0.7 in near future, because of the subthreshold leakage, and also because of the delay in EUV lithography.

As a result, we will have more technology generations until reaching the downsizing limit, and the time to reach the limit will be delayed.
Tri-gate implementation for transistors

Tri-gate has been implemented since 22nm node, enabling further scaling

<table>
<thead>
<tr>
<th></th>
<th>HP</th>
<th>MP</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{OX,E}$ (nm)</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>$L_{GATE}$ (nm)</td>
<td>30</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>$I_{OFF}$ (nA/um)</td>
<td>20-100</td>
<td>5-20</td>
<td>1-5</td>
</tr>
</tbody>
</table>

C. Auth et al., pp.131, VLSI2012 (Intel)
How far can we go for production?

Thus, we may go down to “2 nm” technology by choosing whatever gate length we want for the application.
More Moore to More More Moore

Technology node  
- 65nm
- 45nm
- 32nm
- 22nm

Now

Future
- 15nm
- 11nm
- 8nm
- 5nm
- 3nm

Alternative (III-V/Ge)

Emerging Devices

Planar

Tri-Gate

Si is still main stream for future !!

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)
High-k gate dielectrics

Hf-based oxides

<table>
<thead>
<tr>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
<th>15nm, 11nm, 8nm, 5nm, 3nm,</th>
</tr>
</thead>
<tbody>
<tr>
<td>EOT:1nm</td>
<td>EOT:0.95nm</td>
<td>EOT:0.9nm</td>
<td></td>
</tr>
</tbody>
</table>

SiO₂ IL (Interfacial Layer) is used at Si interface to realize good mobility

Technology for direct contact of high-k and Si is necessary

EOT=0.52 nm
Remote SiO₂-IL scavenging HfO₂ (IBM)

EOT=0.9nm
HfO₂/SiO₂ (IBM)

Continued research and development

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM2009, (IBM)

0.48 → 0.37nm Increase of I_d at 30%
Direct contact with La-silicate (Tokyo. Tech.)
High-k is very important, however very difficult.

Thickness (EOT) decreased only 0.05 nm (or 0.5 Å, or 1 atom layer) for every generation.
How far can we go for production?

Rather than Ioff value, Ion/Ioff ratio is important.

Now, Ion/Ioff ratio is typically $10^6$. However, it degrades significantly with decrease in Vsupply.
Nanowire/Tri gate MOSFETs have advantage not only suppressing Ioff, but also for increasing Iion over planer MOSFETs

1. Because of higher mobility due to lower vertical electric field

2. Because of higher carrier density at the round corner
Electron Density (x10^{19} \text{cm}^{-3})

Distance from SiNW Surface (nm)

Edge portion

Flat portion

Inversion areal ratio: 29 %
3. Now Problems for downsizing!

We have to decrease Si layer thickness to better control of channel potential by gate bias when we decrease the gate length.

↓

Significant decrease in conduction or Ion.
# Short-channel effect

T. Skotnicki, IEDM 2009 Short Course (STMicroelectronics)

### Short-channel effect equation

\[
SCE = 0.64 \frac{V_s}{V_{ox}} \times EI \times \Phi_d
\]

\[
DIBL = 0.8 \frac{V_s}{V_{ox}} \times EI \times V_{ds}
\]

- **EI** = \(1 \times \left(1 + \frac{X_j^2}{L_0^2}\right)\)
  - If max ch. doping is \(10^{20} \text{cm}^{-3}\) then: \(T_{ox} T_{dep} L_{el}^2 / L_0^2\)
  - \(T_{ox} T_{dep} L_{el}^2 / L_0^2\)

- **EI** = \(1 \times \left(1 + \frac{T_{si}^2}{L_0^2}\right)\)
  - If minimum \(T_{si} \approx 3 \text{nm}\) then: \(T_{ox} T_{si} L_{el}^2 / L_0^2\)
  - \(T_{ox} T_{si} L_{el}^2 / L_0^2\)

- **EI** = \(1 \times \left(1 + \frac{T_{si}^2}{4 L_0^2}\right)\)
  - If minimum \(T_{si} \approx 3 \text{nm}\) then: \(T_{ox} T_{si}^2 / 4 L_{el}^2\)
  - \(T_{ox} T_{si} / 2 L_{el}^2\)

- **EI** = \(1 \times \left(1 + \frac{T_{si}^2}{2 L_0^2}\right)\)
  - If minimum \(T_{si} \approx 3 \text{nm}\) then: \(T_{ox} T_{si}^2 / 2 L_{el}^2\)
  - \(T_{ox} T_{si} / 2 L_{el}^2\)

### Example Values

- **L_{el,min}** (DIBL=100mV/V) = \(34\text{nm}\)
- **L_{el,min}** (DIBL=100mV/V) = \(34\text{nm}\)
- **L_{el,min}** (DIBL=100mV/V) = \(30\text{nm}\)
- **L_{el,min}** (DIBL=100mV/V) = \(10\text{nm}\)
- **L_{el,min}** (DIBL=100mV/V) = \(6\text{nm}\)
- **L_{el,min}** (DIBL=100mV/V) = \(2.7\text{nm}\)
Drain-induced barrier lowering

\[
DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{DS}
\]

**T. Skotnicki, IEDM 2010 Short Course (STMicroelectronics)**

- BULK: $T_{\text{dep}} = 3/4 L_{el}$, $X_j = 3/4 L_{el}$, $140 \text{mV/V}$
- III-V: $T_{\text{ox}} + 2A$, $\varepsilon_{Si} + 15\%$, $210 \text{mV/V}$
- ETSOI: $110 \text{mV/V}$
- FDSOI: $T_{\text{dep}} = T_{\text{si}}/2$, $X_j = T_{\text{si}}/2$, $80 \text{mV/V}$
- UTBB: $70 \text{mV/V}$
- FinFET: $T_{\text{si}} \geq 10\text{nm}$, $T_{\text{dep}} = T_{\text{si}}/2$, $X_j = T_{\text{si}}/2$
Sub-threshold Slope

\[ S = \frac{kT}{q} \ln \left( 1 + \frac{C_{dep}}{C_{ox}} + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \frac{T_{ox}}{L_{el}} \frac{X_j}{L_{el}} \left( 1 + \frac{3T_{dep}}{4L_{el}} \right) \sqrt{1 + 2 \frac{V_{ds}}{\Phi_d}} \right) \]

- **BULK**
  - \( X_j = 3/4L_{el} \)
  - \( T_{dep} = 3/4L_{el} \)
  - 95 mV/dec

- **III-V**
  - 110 mV/dec

- **ETSOI**
  - 85 mV/dec

- **FDSOI**
  - \( T_{dep} = T_{si} + \lambda T_{box} \)
  - \( X_j = T_{si} \)

- **UTBB**
  - 75 mV/dec

- **FinFET**
  - \( T_{dep} = T_{si}/2 \)
  - \( X_j = T_{si}/2 \)
  - 65 mV/dec

- RBB => Pstat
Mobility degradation for small diameter nanowire FETs, because channel carriers become too close to all surrounding nanowire surface, and scattered strongly.
Decreasing the diameter of NW

Improved short-channel control

Severe mobility degradation

Problems in Multi-gate

Need to decrease diameter for SCH

Significant $\mu$ degradation at diameter < 10 nm

S. Bangsaruntip et al., pp.297, IEDM2009 (IBM), K. Tachi et al., pp.313, IEDM2009 (CEA-LETI)
Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

1. Mobility degradation

Extremely small distance between the electron and all around Si surface.

Strong scattering of electrons by interaction with all around Si surface.

2. Electron density decrease

Decrease of DOS in extremely narrow wire.

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-k is necessary.
Carrier density degradation for small diameter nanowire FET, because of the decrease in density of states.
Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

4 channels can be used

Energy band of Bulk Si

Energy band of 3 x 3 Si wire
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Wire cross section dependence.

What cross section gives best solution for SCE suppression and drive current?.
Significant increase in $V_{\text{th}}$ variability with decreasing Fin width
Smaller wire/fin width is necessary for SCE suppression

But mobility and $I_{ON}$ severely degrade with wire/fin width reduction

Therefore even in multi-gate structures, EOT scaling should be accelerated to provide SCE immunity
High-k beyond 0.5 nm
Gate oxide should be thicker than mono atomic layer.

0.8 nm gate oxide thickness MOSFETs operate
0.8 nm → Distance of 3 Si atoms → 2 mono layers

R. Chau, et al., (Intel) IWGI 2003
Gate Leakage Power Density becomes significantly large with $L_g$ reduction, and thus, with $t_{ox}$ thinning!!
To use high-k dielectrics

K: Dielectric Constant

Thin SiO₂

K=4

Almost the same electric characteristics

K=20

Thick high-k dielectrics

5 times thicker

Small leakage Current

Solution

However, very difficult and big challenge!
**Equivalent Oxide Thickness (EOT)**

Combination of high-k and metal gate is important

K. Natori, et al., (Tsukuba Univ) SSDM 2005, p.286

- **Poly-Si** $10^{20}$ cm$^{-3}$
- **Depletion**
- **SiO$_2$**
- **C$_{Poly}$**
- **C$_{Ox}$**
- **C$_{Si}$**
- **C$_{Metal}$** (EOT: 0.1 nm)
- **High-k**

**Silicon Substrate**

**Equivalent Oxide Thickness (EOT):** gate dielectrics itself, $C_{ox}$

**Capacitance Equivalent Thickness (CET):** entire gate stack,

Metal gate can eliminate the poly-Si depletion.

**Inversion CET = $T_{inv} \approx EOT + 0.4nm$**

with metal gate electrode

$C_{metal}$ is finite because of quantum effect. In other words electron is not a point charge located at the interface but distributed charge.
Considering that channel carrier layer has equivalent capacitance of 0.5 nm, thinning of high-k until 0.4 or 0.3 nm is meaningful.
### Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>Unstable at Si interface</th>
<th>Radio active</th>
<th>Gas or liquid at 1000 K</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Si + MO_x M + SiO_2</td>
<td>He</td>
<td></td>
</tr>
<tr>
<td>Li Be</td>
<td>Si + MO_x MSi_x + SiO_2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Na Mg</td>
<td>Si + MO_x M + MSi_xO_y</td>
<td></td>
<td></td>
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</tbody>
</table>

- **Unstable at Si interface**
  1. Si + MO_x M + SiO_2
  2. Si + MO_x MSi_x + SiO_2
  3. Si + MO_x M + MSi_xO_y

- **Gas or liquid at 1000 K**
  - HfO_2 based dielectrics are selected as the first generation materials, because of their merit in:
    1. band-offset
    2. dielectric constant
    3. thermal stability

- **La_2O_3 based dielectrics** are thought to be the next generation materials, which may not need a thicker interfacial layer.

---

R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band offset

Oxide

Si

XPS measurement by Prof. T. Hattori, INFOS 2003
Direct high-k/Si by silicate reaction

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface. Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
Direct high-k/Si by silicate reaction

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface. Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

\[
\text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2
\]

Oxygen supplied from W gate electrode

H. Shimizu, JJAP, 44, pp. 6131

D.J. Lichtenwalner, Trans. ECS 11, 319

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-$k$/Si is possible

La$_2$O$_3$ can achieve direct contact of high-$k$/Si

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.
Cluster tool for HKMG Stack

EB Deposition for HK

Flash Lamp

Sputter for MG

Robot

ALD

RTA

Entrance

5m
Cluster Chambers for HKMG Gate Stack

EB Deposition: HK

Sputter: MG

Flash Lamp Anneal

ALD: HK

Robot

RTA

Entrance
Shutter movement

Chip

15cm

high-k

Metal

Si

Metal

Si

Metal

Si

Metal

Si

Id (V)

Vg=0V

Vg=0.2V

Vg=0.4V

Vg=0.6V

Vg=0.8V

Vg=1.0V

Vg=1.2V

Vth=-0.04V

Vth=-0.05V

Vth=-0.06V
L = 0.5~100 µm (8 kinds)
W = 10, 20, 50, 100 µm (4 kinds)

30 different Trs

26 chips

1 cm × 1 cm
Physical mechanisms for small Dit

① silicate-reaction-formed fresh interface

② stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress


Gate Leakage vs EOT, (Vg=|1|V)

- Al2O3
- HfAlO(N)
- HfO2
- HfSiO(N)
- HfTaO
- La2O3
- Nd2O3
- Pr2O3
- PrSiO
- PrTiO
- SiON/SiN
- Sm2O3
- SrTiO3
- Ta2O5
- TiO2
- ZrO2(N)
- ZrSiO
- ZrAlO(N)
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
ALD of La2O3


ALD is indispensable from the manufacturing viewpoint - precise control of film thickness and good uniformity.
Annealed for 2 s
La$_2$O$_3$(3.5 nm)

W(60 nm)

TiN/W(6 nm)

As depo

Annealing temperature (°C)

EOT (nm)

EOT=0.55 nm

TaN/(45nm)/W(3nm)
900°C, 30min

EOT=0.55nm

Experiment
Theory

$C_g$ (uF/cm$^2$)

Vg (V)
Flat-band voltage (V)

EOT (nm)

Fixed Charge density: $1 \times 10^{11} \text{ cm}^{-2}$

TaN(45nm)/W(3nm)

$Q_{fix} = 1 \times 10^{11} \text{ cm}^{-2}$

900°C, 30min
Our Work at TIT: High-k

Our result at TIT

EOT = 0.40nm

Electron Mobility [cm²/Vsec]

L/W = 5/20µm
T = 300K
N_{sub} = 3 \times 10^{16} \text{cm}^{-3}

EOT = 0.40nm
L/W = 5/20µm
T = 300K
N_{sub} = 3 \times 10^{16} \text{cm}^{-3}
Benchmark of La-silicate dielectrics

Gate Leakage current

ITRS requirement

Our data: La-silicate gate oxide

Effective Mobility

Solid circle: Our data
La-silicate gate oxide

Open square : Hf-based oxides

T. Ando, et al., (IBM) IEDM 2009, p.423
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Flat metal/high-k interface for better mobility
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Suppression of FLP
- Interface dipole control for $V_{th}$ tuning
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
- Suppression of oxygen vacancy formation
- Suppression of metal diffusion
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k
- Reliability: PBTI, NBTI, TDDB
Conclusions 1

Downsizing of MOSFETs is still important for high-speed low-power operation of logic LSIs.

$\text{I}_{\text{off}}$ will limit the downsizing.

Punchthrough component of $\text{I}_{\text{off}}$ will be suppressed by thinning tox and adopting new configuration such as FinFET or nanowire FET.

Direct tunneling will limit the downsizing @ $L_g = 3$ nm.

Even before that, subthreshold leakage would limit the downsizing @ $L_g > 3$nm, depending on the application.
Conclusions 2

In the application, Ion/Ioff ratio is important.

The ratio is typically $10^6$ for the present devices, however, it degrades significantly with decreasing the supply voltage.

Si nanowire FET has advantage not only on Ioff over planer FET, but also on Ion, because of better mobility and higher channel carrier density.

In order to suppress Ioff with decrease in Lg, the diameter of nanowire, width of fin, or thickness of Si film of SOI need to be shirked.

However, with decreasing the above diameter, width or thickness less than several nano-meter, very significant decrease in Ion occurs, because of the degradation on mobility and carrier concentration.
Conclusions 3

If the diameter, width or thickness cannot be decreased, we need to decrease the EOT of high-k aggressively in order to suppress Ioff.

High-k EOT reduction trend is very slow – 0.05 nm for each generation --, for the moment.

The limit of EOT scaling is expected to be around 0.4 nm or so, considering the additional capacitances of channel and metal gate.

By changing the high-k material from HfO₂ to La-silicate, we can obtain the good operation of MOSFET with EOT = 0.4 nm,

- Metal silicide Shottoky S/D will become important in order to suppress the S/D encroachment to the channel by dopant diffusion.
Conclusions 3

Downsizing of MOFET is becoming more and more important for low power high performance application in the future smart society, and will be accomplished in another 10 to 15 years, although the rate of the downsizing will become slow.

Thus, many challenging technology development will be necessary for another 10 to 15 years.

Thank you very much for your attention.
What is Next Revolution for Device Technology?

1900: Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

?: Nano Electronics
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

?: Nano Electronics
Maybe Not a Revolution
But Great Innovation
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

? years

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

↓ 70 years

1970: Micro Electronics

↓ ? years

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

↓

70 years

1970: Micro Electronics

↓

70 years

When?: What?
What is Next Revolution for Device Technology?

1900: Electronics

1970: Micro Electronics

2040: Braintronics

70 years

70 years

70 years
We do know system and algorithms are important! But do not know how it can be by us for use of bio?
Long term roadmap for development

Source: H. Iwai, IPFA 2006

New Materials, New Process, New Structure

Hybrid integration of different functional Chip
Increase of SOC functionality

3D integration of memory cell
3D integration of logic devices

Miniaturization of Interconnects on PCB
(Printed Circuit Board)

Low cost for LSI process
Revolution for CR, Equipment

Introduction of algorithm of bio system
Brain of insects, human

Saturation of Downsizing

Scaling proceeds

Size

Braintronics

Some time in 2020 - 2030

After 2040?

We do not know how?
Braintronics for 2040’s

It’s a task for you,
For young generations!
Thank you very much for your attention.