Problems and some solutions for future Nano CMOS Technology

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Frontier Research Center
Tokyo Institute of Technology
I came Stanford in March, 1983
Now October, 2013

Increase 31 plates
Now, I am working with 3 permanent professors, 5 visiting professors, and 40 graduate students

On nano-CMOS, III-V MOSFETs, GaN Power devices, Si Nanowire solar cell, Silicide Solar cell, etc.
1. Background for nano-CMOS
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power
consumption
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si

Source

Drain

Si

Al Gate

Al

SiO₂

Si

Si/SiO₂ Interface is extraordinarily good
1970,71: 1st generation of LSIs

DRAM      Intel 1103

MPU       Intel 4004
In 2012

Most Recent SD Card

128GB (Bite) = 128G X 8bit = 1T(Tera)bit

1T = 10^{12} = 1 Trillion

World Population: 7 Billion
Brain Cell: 10~100 Billion
Stars in Galaxy: 100 Billion
128 GB = 1Tbit

2.4cm X 3.2cm X 0.21cm

Volume: 1.6cm³  Weight: 2g

Voltage: 2.7 - 3.6V

Old Vacuum Tube:
5cm X 5cm X 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube: 5cm X 5cm X 10cm

Volume = (5cm X 10,000) X (5cm X 10,000) X (10cm X 10,000)
= 0.5km X 0.5km X 1km

1Tbit = 10,000 X 10,000 X 10,000 bit

Pingan International Finance Center, Shanghai, China (Year 2016)
Indian Tower, Mumbai, India (Year 2016)
Burj Khalifa, Dubai, UAE (Year 2010)

500 m
1,000 m
Old Vacuum Tube:  
50W

Nuclear Power Generator:  
1MkW=1BW

1Tbit = $10^{12}$ bit

Power = $0.05kWX10^{12}=50$ TW

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving
Brain: Integrated Circuits
Ear, Eye: Sensor
Mouth: RF/Opto device
Stomach: PV device
Hands, Legs: Power device
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years, even though, it is very matured market!!

Gartner: By K. Kim, CSTIC 2012
2. Current status of Si-CMOS device technologies
Downsizing

Important for

Decreasing cost, power

Increasing performance
Feature Size / Technology Node

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm →
0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm →
90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm (2012)

From 1970 to 2013 (This year)

43 years 1 generation
18 generations 2.5 years
Line width: 1/450 Line width: 1/1.43 = 0.70
Area: 1/200,000 Area: 1/2 = 0.5
Question

What is the problem for downsizing?
The problem for downsizing Transistor cannot be turned-off.

Off-leakage current between S and D

1. Punch-through between S and D
2. Direct-tunneling between S and D
3. Subthreshold current between S and D
1. Punch-through between S and D
Problem for downsizing

Region governed by gate bias

Region governed by drain bias

DL touch with S Region (DL)

Large $I_{OFF}$

No $t_{ox}$, $V_{dd}$ thinning

$0V < V_{dep} < 1V$

Large $I_{OFF}$ (Electron current)

Depletion Region (DL) by Drain Bias

$t_{ox}$ and $V_{dd}$ have to be decreased for better channel potential control $\rightarrow I_{OFF}$ Suppression
1. Punch-through between S and D

Solutions

Decreasing supply voltage $\rightarrow$ Very difficult to suppress depletion layer

Decreasing tox

Configuration change

Fin-FET, ET-SOI, etc.
Our Work at TIT: High-k

Our result at TIT

EOT=0.40nm

- Drain Current (mA) vs. Drain Voltage (V)
  - Vg= 0.2V
  - Vg= 0.4V
  - Vg= 0.6V
  - Vg= 0.8V
  - Vg= 1.0V
  - L/W = 5/20μm
  - T = 300K
  - N_{sub} = 3 \times 10^{16} \text{cm}^{-3}

- Electron Mobility [cm^2/Vsec] vs. E_{eff} [MV/cm]
  - EOT = 0.40nm
  - L/W = 5/20μm
  - T = 300K
  - N_{sub} = 3 \times 10^{16} \text{cm}^{-3}
Extremely Thin (or Fully-Depleted) SOI

Make thin Si layer

Control channel also from the bottom

Planar

ET (or FD) SOI
Surrounding gate structure (Multiple gates)

Make thin Si layer

Control channel also by multiple gates

Planar

Multi gate
Nanowire structures in a wide meaning

- Fin
- Tri-gate
- Tri-gate (Variation)
- Ω-gate
- All-around
Our work at TIT: $\Omega$-gate Si Nanowire

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  - (1.32 mA/\(\mu\)m @ \(I_{\text{OFF}}=117\) nA/\(\mu\)m)
- DIBL of 62mV/V and SS of 70mV/dec for nFET

\(L_g=65\)nm

\(V_d=-1V, V_d=1V, V_d=-50mV, V_d=50mV\)

Drain Current (A)

Gate Voltage (V)

\(I_{\text{ON}}\) and \(I_{\text{OFF}}\) characteristics

Conventional CMOS process

High drive current

DIBL of 62mV/V and SS of 70mV/dec for nFET
2. Direct-tunneling between S and D
What would be the limit of downsizing!

Tunneling distance

Source

Channel

Drain

Direct-tunnel current

3 nm

Energy or Potential for Electron
2. Direct-tunneling between S and D

Almost no solution!
3. Subthreshold current between S and D
Subthreshold leakage current of MOSFET

Subthreshold leakage current of MOSFET is OK at Single Tr. level but not OK for Billions of Trs.

- $V_g=0V$
- $I_{on}$
- $I_{off}$
- Subthreshold region
- $V_{th}$ (Threshold Voltage)
Subthreshold leakage current will limit the downsizing

Electron Energy
Boltzmann statistics
\( \text{Exp} \left( \frac{qV}{kT} \right) \)
3. Subthreshold current between S and D

Solution

Keep Vth as high as possible

- Do not decrease supply voltage

- Suppress variability in Vth
The limit is different depending on application.

- **HP CMOS** (high Performance)
  - Highest Ion, Lowest CV/I
  - High leakage
  - Medium Vdd

- **LOP CMOS** (Low Operation Power)
  - Lowest Vdd
  - Medium Ion, medium CV/I
  - Medium leakage

- **LSTP CMOS** (Low Standby Power)
  - Lowest leakage
  - Low Ion, high CV/I
  - High Vdd

Source: 2007 ITRS Winter Public Conf.
How far can we go for production?

Past 0.7 times per 2.5 years
10\(\mu\)m \(\rightarrow\) 8\(\mu\)m \(\rightarrow\) 6\(\mu\)m \(\rightarrow\) 4\(\mu\)m \(\rightarrow\) 3\(\mu\)m \(\rightarrow\) 2\(\mu\)m \(\rightarrow\) 1.2\(\mu\)m \(\rightarrow\) 0.8\(\mu\)m \(\rightarrow\) 0.5\(\mu\)m \(\rightarrow\) 0.35\(\mu\)m \(\rightarrow\) 0.25\(\mu\)m \(\rightarrow\) 180nm \(\rightarrow\) 130nm \(\rightarrow\) 90nm \(\rightarrow\) 65nm \(\rightarrow\) 45nm \(\rightarrow\) 32nm

Future

Limit depending on applications
Fundamental limit

Direct-tunnel
Subthreshold punchthrough

Now
Intermediate node

(28nm) \(\rightarrow\) 22nm \(\rightarrow\) 14nm \(\rightarrow\) 11.5 nm \(\rightarrow\) 8nm \(\rightarrow\) 5.5nm? \(\rightarrow\) 4nm? \(\rightarrow\) 2.9 nm? \(\rightarrow\)

•At least 4,5 generations to 8 ~ 5 nm
However, careful about the name of technology!

Reentry,
Gate length (Lg) is much larger than the Technology name

**22 nm** Technology by Intel

Lg (Gate length) = **30 nm** (HP), **34 nm** (MP), **34 nm** or larger (SP)

IEDM 2012, VLSI 2013

**10 nm** Technology by Leti (FD-SOI)

Lg (Gate length) = **15 nm**

ECS 2013
Tri-gate has been implemented since 22nm node, enabling further scaling

<table>
<thead>
<tr>
<th></th>
<th>HP</th>
<th>MP</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{OX,E}$ (nm)</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>$L_{GATE}$ (nm)</td>
<td>30</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>$I_{OFF}$ (nA/um)</td>
<td>20-100</td>
<td>5-20</td>
<td>1-5</td>
</tr>
</tbody>
</table>
- SS of 71 and 72 mV/dec for HP NMOS and PMOS, respectively
- DIBL of 30 and 35 mV/V for NMOS and PMOS, respectively
- $V_{th}$ of 22 nm is about 0.1 ~0.2 V lower than that of 32nm
How far can we go for production?

Thus, we may go down to “5 nm” technology with whatever gate length we want for the application.
More Moore to More More Moore

Technology node

<table>
<thead>
<tr>
<th>Now</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td>65nm 45nm</td>
<td>15nm 11nm 8nm</td>
</tr>
<tr>
<td>32nm 22nm</td>
<td>5nm 3nm</td>
</tr>
</tbody>
</table>

Lg 35nm
Lg 30nm

Emerging Devices

Si is still main stream for future!!

Alternative (III-V/Ge)
Channel FinFET
Emerging Devices

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)
High-k gate dielectrics

Hf-based oxides

<table>
<thead>
<tr>
<th>45nm EOT:1nm</th>
<th>32nm EOT:0.95nm</th>
<th>22nm EOT:0.9nm</th>
<th>15nm, 11nm, 8nm, 5nm, 3nm,</th>
</tr>
</thead>
</table>

SiO₂ IL (Interfacial Layer) is used at Si interface to realize good mobility

Technology for direct contact of high-k and Si is necessary

EOT=0.52 nm

Remote SiO₂-IL scavenging HfO₂ (IBM)

Continued research and development

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM2009, (IBM)

Direct contact with La-silicate (Tokyo Tech.)
How far can we go for production?

Ion/loff ratio is typically $10^6$.

However, it degrades significantly with decrease in $V_{supply}$. 
$I_{ON}$ and $I_{OFF}$ benchmark

**NMOS**

- **Intel [a]**
  - Bulk 32nm Tri-Gate 22nm
  - $V_{DD}=0.8V$
  - $V_{DD}=1V$
- **Samsung [c]**
  - Bulk 20nm
  - $V_{DD}=0.9V$
- **Tokyo Tech. [i]**
  - Ω-gate NW
  - $V_{DD}=1V$
- **IBM [g]**
  - FinFET 25nm
  - $V_{DD}=0.9V$
  - GAA NW
  - $V_{DD}=1V$
- **STMicro. [h]**
  - GAA NW
  - $V_{DD}=1.1V$

**PMOS**

- **Intel [a]**
  - Bulk 32nm Tri-Gate 22nm
  - $V_{DD}=0.8V$
  - $V_{DD}=1V$
- **Samsung [c]**
  - Bulk 20nm
  - $V_{DD}=0.9V$
- **IBM [j]**
  - ETSOI
  - $V_{DD}=0.9V$
  - $V_{DD}=1V$
- **STMicro. [h]**
  - GAA NW
  - $V_{DD}=1.1V$

[References]

[a] C. Auth et al., pp.131, VLSI2012 (Intel).
[d] S. Saitoh et al., pp.11, VLSI2012 (Toshiba).
[g] A. Khakifirooz et al., pp.117, VLSI2012 (IBM).
Nanowire/Tri gate MOSFETs have advantage also for ion over planer MOSFETs

1. Because of higher mobility due to lower vertical electric field

2. Because of higher carrier density at the round corner
Electron Density
(x\(10^{19}\text{cm}^{-3}\))

Distance from SiNW Surface (nm)

Edge portion

Flat portion

Inversion areal ratio: 29 %
3. Problems

We have to decrease Si layer thickness to better control of channel potential by gate bias.

Significant decrease in conduction or Ion.
Short-channel effect

T. Skotnicki, IEDM 2009 Short Course (STMicroelectronics)

\[
SCE = 0.64 \frac{\varepsilon_s}{\varepsilon_{ox}} \times EI \times \Phi_d
\]
\[
DIBL = 0.8 \frac{\varepsilon_s}{\varepsilon_{ox}} \times EI \times V_{ds}
\]

\[
EI = 1 \times 
\begin{cases}
1 + \frac{X^2}{L_{el}} & \text{if max ch. doping is } 10^{16} \text{cm}^{-3} \Rightarrow T_{ep} \sim 12 \text{nm} \\
1 + \frac{X^2}{L_{el}^2} & \text{if max ch. doping is } 10^{20} \text{cm}^{-3} \Rightarrow T_{ep} \sim 12 \text{nm}
\end{cases}
\]

\[
\begin{align*}
&T_{ox} \times \frac{T_{dep}}{L_{el}^2} \times \frac{L_{el}}{L_{el}} \\
&T_{ox} \times \frac{T_{dep}}{L_{el}} \times \frac{L_{el}}{L_{el}} \\
&T_{ox} \times \frac{T_{si} + \lambda T_{box}}{L_{el}} \\
&T_{ox} \times \frac{T_{si}^2}{L_{el}^2} \\
&T_{ox} \times \frac{T_{si}^2}{L_{el}^2}
\end{align*}
\]

if max ch. doping is 10^{16} cm^{-3} \Rightarrow T_{ep} \sim 12 nm

if max ch. doping is 10^{20} cm^{-3} \Rightarrow T_{ep} \sim 12 nm

T_{box} = 145 \text{ nm} \quad \lambda T_{box} = 18 \text{ nm}

T_{box} = 10 \text{ nm} \quad \lambda T_{box} = 3 \text{ nm}

T_{box} = 10 \text{ nm} \quad \lambda T_{box} = 0.46 \text{ nm} \quad \approx 0 \text{ nm}

T_{si}/2 \text{ plays role of } X_{j}, \quad \text{and that of } T_{dep} \text{, if max ch. feasible}

\text{Tsi is supposed 3nm; then:

\text{Le}_{el, min} \quad \text{(DIBL=100mV/V)}
\]

\begin{align*}
&= 34 \text{ nm} \\
&= 34 \text{ nm} \\
&\approx 30 \text{ nm} \\
&\approx 10 \text{ nm} \\
&\approx 6 \text{ nm} \\
&\approx 2.7 \text{ nm}
\end{align*}
Drain-induced barrier lowering

\[ DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{DS} \]

- **BULK**
  - \( X_j = 3/4 L_{el} \)
  - \( T_{dep} = 3/4 L_{el} \)
  - **VDD** = 140 mV/V

- **III-V**
  - \( T_{ox} + 2A \)
  - \( \varepsilon_{si} + 15\% \)
  - **VDD** = 210 mV/V

- **FDSOI**
  - \( T_{dep} = T_{si}/2 \)
  - \( X_j = T_{si} \geq 6 \text{nm} \)
  - **VDD** = 110 mV/V

- **ETSOI**
  - \( T_{dep} = T_{si} + \lambda T_{box} \)
  - \( X_j = T_{si} \geq 6 \text{nm} \)
  - **VDD** = 80 mV/V

- **FinFET**
  - \( T_{dep} = T_{si}/2 \)
  - \( X_j = T_{si}/2 \)
  - \( T_{si} \geq 10 \text{nm} \)
  - **VDD** = 70 mV/V
Sub-threshold Slope

\[ S = \frac{kT}{q} \ln \left( 1 + \frac{C_{\text{dep}}}{C_{\text{ox}}} + \frac{\varepsilon_{\text{Si}}}{\varepsilon_{\text{ox}}} \frac{T_{\text{ox}}}{L_{\text{el}}} \frac{X_j}{L_{\text{el}}} \left( 1 + \frac{3T_{\text{dep}}}{4L_{\text{el}}} \right) \sqrt{1 + 2\frac{V_{ds}}{\Phi_d}} \right) \]

- BULK: \( X_j = 3/4L_{\text{el}} \), \( T_{\text{dep}} = 3/4L_{\text{el}} \), 95 mV/dec
- III-V: \( T_{\text{ox}} + 2A \), \( \varepsilon_{\text{Si}} + 15\% \), 110 mV/dec
- ETSOI: 85 mV/dec
- UTBB: 75 mV/dec
- FDSOI: \( T_{\text{dep}} = T_{\text{si}} / 2 \), \( X_j = T_{\text{si}} / 2 \), \( T_{\text{dep}} = T_{\text{si}} + \lambda T_{\text{box}} \), 65 mV/dec
- FinFET: \( R_{\text{BB}} \Rightarrow P_{\text{stat}} \)
3. Problems

Mobility degradation.
Decreasing the diameter of NW

Improved short-channel control

Severe mobility degradation

Significant $\mu$ degradation at diameter < 10 nm

Need to decrease diameter for SCH

Decreasing the diameter of NW
Problems in SOI

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

1. Mobility degradation

Extremely small distance between the electron and all around Si surface.

Strong scattering of electrons by interaction with all around Si surface.

2. Electron density decrease

Decrease of DOS in extremely narrow wire.

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-k is necessary.
3. Problems

Carrier density degradation.
Number of quantum channels

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

By Prof. Shiraishi of Tsukuba univ.

4 channels can be used
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Wire cross section dependence.

What cross section gives best solution for SCE suppression and drive current?
Significant increase in $V_{\text{th}}$ variability with decreasing Fin width
Smaller wire/fin width is necessary for SCE suppression

But mobility and $I_{ON}$ severely degrade with wire/fin width reduction

Therefore even in multi-gate structures, EOT scaling should be accelerated to provide SCE immunity
High-k beyond 0.5 nm
Gate oxide should be thicker than mono atomic layer

0.8 nm gate oxide thickness MOSFETs operate

0.8 nm $\rightarrow$ Distance of 3 Si atoms $\rightarrow$ 2 mono layers

*R.Chu, et al., (Intel) IWGI 2003*
Gate Leakage Power Density becomes significantly large with $L_g$ reduction, and thus, with $t_{ox}$ thinning!!

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors
To use high-k dielectrics

K: Dielectric Constant

Thin SiO$_2$

K=4

Almost the same K=20 electric characteristics

Thick high-k dielectrics

5 times thicker

Small leakage Current

However, very difficult and big challenge!
Combination of high-k and metal gate is important

K. Natori, et al., (Tsukuba Univ) SSDM 2005, p.286

Equivalent Oxide Thickness (EOT): gate dielectrics itself, $C_{OX}$
Capacitance Equivalent Thickness (CET): entire gate stack,

Metal gate can eliminate the poly-Si depletion.

Inversion CET = $T_{inv} \approx EOT + 0.4\text{nm}$ with metal gate electrode

$C_{metal}$ is finite because of quantum effect. In other words, electron is not a point charge located at the interface but distributed charge.
Choice of High-k elements for oxide

Candidates

Unstable at Si interface

- Si + MOX → M + SiO2
- Si + MOX → MSiX + SiO2
- Si + MOX → M + MSiXOY

Gas or liquid at 1000 K
- Radio active

HfO₂ based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

Choice of High-k elements for oxide

R. Hauser, IEDM Short Course, 1999
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Flat metal/high-k interface for better mobility
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Interface dipole control for $V_{th}$ tuning
- Suppression of FLP
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
- Reliability: PBTI, NBTI, TDDB
- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Interface dipole control for $V_{th}$ tuning
- Suppression of FLP
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

XPS measurement by Prof. T. Hattori, INFOS 2003
Direct high-k/Si by silicate reaction

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface. Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
Direct high-k/Si by silicate reaction

HfO₂ case

Low $P_{O2}$ → High $P_{O2}$

HfSiₓ

Si substrate

$k \sim 4$

La₂O₃ case

Low $P_{O2}$ → High $P_{O2}$

LaSiₓ

Si substrate

La-rich

Si-rich

Our approach

Direct contact can be achieved with La₂O₃ by forming silicate at interface
Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
SiO$_x$-IL growth at HfO$_2$/Si Interface

XPS Si1s spectrum

Phase separator

HfO$_2$ + Si + O$_2$ → HfO$_2$ + Si + 2O* → HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Trans. ECS 11, 319

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ can achieve direct contact of high-k/Si

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Cluster tool for HKMG Stack

- EB Deposition for HK
- Flash Lamp
- Sputter for MG
- Robot
- ALD
- RTA
- Entrance

5m 5m 5m
Cluster Chambers for HKMG Gate Stack

EB Deposition: HK

Sputter: MG

Flash Lamp Anneal

ALD: HK

Robot

RTA

Entrance
Deposited thin film

Substrate

Moving Mask

Flux

Source

Electron Beam
L = 0.5~100 µm (8 kinds)
W = 10, 20, 50, 100 µm (4 kinds)

26 chips

1 cm × 1 cm

30 different Trs
Shutter movement

Chip

Metal

Si

high-k

Thin

Thick

Vth=-0.04V
Vth=-0.05V
Vth=-0.06V

Id(V)
Gate Leakage vs EOT, (Vg=|1|V)
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small $D_{it}$

1. Silicate-reaction-formed fresh interface

2. Stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA$800^\circ$C is necessary to reduce the interfacial stress


La$_2$O$_3$

No interfacial layer can be confirmed with Si/TiN/W

$K_{av} \sim 8$

$K_{av} \sim 12$

$K_{av} \sim 16$
La$_2$O$_3$/silicate/$n$-Si CV

![Graph showing capacitance density vs. gate voltage for W/La$_2$O$_3$(4nm)/$n$-Si at 600°C, 30min.](image)

- Capacitance density (µF/cm$^2$)
- Gate voltage (V)

- 1kHz
- 1MHz
- $\Delta V_{fb}$
- $C_{fb}$
It is important to change the La2O3 to La-silicate completely
**TiN(45nm)/W(6nm)**

- **Annealed for 2 s**
  - La$_2$O$_3$(3.5 nm)
  - W(60 nm)

- **TiN/W(6 nm)**

**Annealing temperature (°C)**

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>EOT (nm)</th>
</tr>
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<tbody>
<tr>
<td>700</td>
<td>0.6</td>
</tr>
<tr>
<td>800</td>
<td>1.0</td>
</tr>
<tr>
<td>900</td>
<td>1.5</td>
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<td>1000</td>
<td>2.0</td>
</tr>
</tbody>
</table>

**Cg (μF/cm²)**

- **Experiment**
- **Theory**

**TaN/(45nm)/W(3nm)**

- 900°C, 30min
- EOT=0.55nm

**EOT=0.55nm**

- Experiment
- Theory
Flat-band voltage (V) vs. EOT (nm) for TaN(45nm)/W(3nm)

- $Q_{fix} = 1 \times 10^{11} \, \text{cm}^{-2}$

- 900°C, 30 min

Fixed Charge density: $1 \times 10^{11} \, \text{cm}^{-2}$
Gate current (A/cm²)

\[10^{-5} \quad 10^{-4} \quad 10^{-3} \quad 10^{-2} \quad 10^{-1} \quad 10^{0} \quad 10^{1} \quad 10^{2} \quad 10^{3} \quad 10^{4}\]

Gate voltage (V)

ITRS

x1/100

TaN/W/LaSiO\(_x\)/nFET

\[W_g/L_g=20/20\,\mu m\]

EOT=0.55nm
Benchmark of La-silicate dielectrics

Gate Leakage current

Effective Mobility

- Open square: Hf-based oxides
- Solid circle: Our data
- La-silicate gate oxide

T. Ando, et al., (IBM) IEDM 2009, p.423
## Si benchmark (nMOSFET)

<table>
<thead>
<tr>
<th>Gate stack</th>
<th>EOT</th>
<th>Mobility</th>
<th>$V_{th}$</th>
<th>SS</th>
<th>DIBL</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN/Cap/HfO₂</td>
<td>0.52nm</td>
<td>110cm²/Vs (at 1x10¹³cm⁻²)</td>
<td>~0.4V (L₉=24nm)</td>
<td>90mV/dec</td>
<td>147mV/V</td>
<td>IBM VLSI2011</td>
</tr>
<tr>
<td>TiN/Cap/HfO₂</td>
<td>0.55nm</td>
<td>140cm²/Vs (at 1MV/cm)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>TiN/Cap/HfO₂</td>
<td>0.45nm</td>
<td>115cm²/Vs (at 1x10¹³cm⁻²)</td>
<td>0.3V (L₉=10um)</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Metal/HfO₂</td>
<td>0.59nm</td>
<td>130cm²/Vs (at 1MV/cm)</td>
<td>0.45V (L₉=1um)</td>
<td>75mV/dec</td>
<td>—</td>
<td>Sematech VLSI2009</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.65nm</td>
<td>—</td>
<td>0.3~0.4V (L₉=~30nm)</td>
<td>90mV/dec</td>
<td>100mV/V</td>
<td>Samsung VLSI2011</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.95nm</td>
<td>—</td>
<td>~0.3V (L₉=30nm)</td>
<td>100mV/dec</td>
<td>~200mV/V</td>
<td>Intel IEDM2009</td>
</tr>
<tr>
<td>W/La-silicate 95</td>
<td>0.62nm</td>
<td>155cm²/Vs (at 1MV/cm)</td>
<td>-0.08V (L₉=10um)</td>
<td>~70mV/dec</td>
<td>—</td>
<td>Tokyo Tech. T-ED2012</td>
</tr>
</tbody>
</table>
ALD of La2O3


ALD is indispensable from the manufacturing viewpoint - precise control of film thickness and good uniformity
Advantages of metal S/D
- atomically abrupt junction
- low parasitic resistance
- reduced channel dopant concentration

Issues in metal S/D
- two different $\phi_B$ for p/n-ch FETs
- underlap/overlap to the gate
- narrow process temperature window

- Metal S/D is considered for alternative channel material such as InGaAs and Ge

Ni is used both on InGaAs and Ge to form alloy.