Future of Nano CMOS Technology

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Tokyo Institute of Technology
1. Background for nano-electronics
1900 “Electronics” started.

Device: Vacuum tube

Device feature size: 10 cm

Major Appl.: Amplifier (Radio, TV, Wireless etc.)

→ Technology Revolution

1970 “Micro-Electronics” started.

Device: Si MOS integrated circuits

Device feature size: 10 µm

Major Appl.: Digital (Computer, PC, etc.)

→ Technology Revolution
2000 “Nano-Electronics” started.

Device: Still, Si CMOS integrated circuits
Device feature size: 100 nm
Major Appl.: Digital (µ-processor, cell phone, etc.)

→ Technology Revolution??

   Maybe, just evolution or innovation!

But very important so many innovations!
Now, 2013 “Nano-Electronics” continued.

Device: Still, Si CMOS integrated circuits
Device feature size: near 10 nm
Major Appl.: Still Digital (μ-processor, cell phone, etc.)

Still evolution and innovation..

But, so many important emerging applications for smart society.
Questions for future

Future, “Nano-Electronics” still continued?

Device: Still, Si CMOS integrated circuits?

Device feature size: ? nm, what is the limit?

Application: New application?

→ Any Technology Revolution?
What is special or new for Nano-Electronics?

In 1990’s, people expected completely new mechanism or operational principle due the nano size, like quantum mechanical effects.

However, no fancy new operational principle was found.

At least for logic application, there is no success story for “Beyond CMOS devices” to replace Si-CMOS.

Of course, I do not deny the importance of Beyond CMOS technology development. It is becoming very important as CMOS approach its limit.
Ballistic conduction will not happen even decreasing channel length. 

\[ L \gg \lambda \quad \text{Diffusive transport} \]

\[ L \sim \lambda \quad \text{Quasi-Ballistic transport} \]

\[ L < \lambda \quad \text{Ballistic transport} \]

Ballistic transport will never happen for MOSFET because of back scattering at drain.

With decreasing channel length, Drain current increase continue.

Also, 1D quantum conduction, or ballistic conduction will not happen. (1D quantum conduction: 77.8\( \mu \)S regardless of the length and material)
2. Importance of nano-electronics as integrated circuits
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher performance with extremely low power consumption
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si Gate
Source
Drain
Si/SiO2 Interface is extraordinarily good
1970,71: 1st generation of LSIs

DRAM   Intel 1103

MPU    Intel 4004
In 2012

Most Recent SD Card

128GB (Bite) = 128G X 8bit = 1T(Tera)bit

1T = 10^{12} = 1 Trillion

World Population: 7 Billion
Brain Cell: 10~100 Billion
Stars in Galaxy: 100 Billion
128 GB = 1Tbit

2.4cm × 3.2cm × 0.21cm

Volume: 1.6 cm³  Weight: 2g

Voltage: 2.7 - 3.6V

Old Vacuum Tube:
5cm × 5cm × 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube: 5cm X 5cm X 10cm

Volume = (5cm X 10,000) X (5cm X 10,000) X (10cm X 10,000)
= 0.5km X 0.5km X 1km

1Tbit = 10,000 X 10,000 X 10,000 bit

Pingan International Finance Center, Shanghai, China (Year 2016)

Indian Tower, Mumbai, India (Year 2016)

Burj Khalifa, Dubai, UAE (Year 2010)
Old Vacuum Tube: 50W

1Tbit = 10^{12} \text{bit}

Power = 0.05 \text{kW} \times 10^{12} = 50 \text{ TW}

Nuclear Power Generator

1 \text{MkW} = 1 \text{BW}

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving
Brain: Integrated Circuits
Ear, Eye: Sensor
Mouth: RF/Optto device
Stomach: PV device
Hands, Legs: Power device
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years, even though, it is very matured market!!

2011  2025

300B USD  1,500B USD

Gartner: By K. Kim, CSTIC 2012
2. Current status of Si-CMOS device technologies
Downsizing

Important for

Decreasing cost, power

Increasing performance
Feature Size / Technology Node

(1970) 10 \( \mu \text{m} \rightarrow 8 \ \mu \text{m} \rightarrow 6 \ \mu \text{m} \rightarrow 4 \ \mu \text{m} \rightarrow 3 \ \mu \text{m} \rightarrow 2 \ \mu \text{m} \rightarrow 1.2 \ \mu \text{m} \rightarrow \\
0.8 \ \mu \text{m} \rightarrow 0.5 \ \mu \text{m} \rightarrow 0.35 \ \mu \text{m} \rightarrow 0.25 \ \mu \text{m} \rightarrow 180 \ \text{nm} \rightarrow 130 \ \text{nm} \\
90 \ \text{nm} \rightarrow 65 \ \text{nm} \rightarrow 45 \ \text{nm} \rightarrow 32 \ \text{nm} \rightarrow (28 \ \text{nm} \rightarrow) 22 \ \text{nm}(2012)

From 1970 to 2013 (This year)

<table>
<thead>
<tr>
<th>43 years</th>
<th>18 generations</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 generation</td>
<td>2.5 years</td>
</tr>
<tr>
<td>Line width: 1/450</td>
<td>Line width: 1/1.43 = 0.70</td>
</tr>
<tr>
<td>Area: 1/200,000</td>
<td>Area: 1/2 = 0.5</td>
</tr>
</tbody>
</table>
Problem for downsizing

- Gate oxide
- Gate metal
- Source Drain
- Substrate
- Source Drain
- Channel
- Substrate

Region governed by gate bias
Region governed by drain bias

0V > V_{dep} < 1V

Large $I_{OFF}$
Region (DL)

No $t_\text{ox}$, $V_{dd}$ thinning

$V_{dd}$ thinning

Large $I_{OFF}$
(Electron current)

$t_\text{ox}$ and $V_{dd}$ have to be decreased for better channel potential control $\rightarrow I_{OFF}$ Suppression
$L_{\text{gate}}$ and $t_{\text{ox}}(\text{EOT})$ scaling trend

A. Toriumi (Tokyo Univ), IEDM 2006, Short Course
EOT=0.40nm

Our Work at TIT: High-k

EOT = 0.40nm

L/W = 5/20μm
T = 300K
N_{sub} = 3 \times 10^{16} cm^{-3}
What would be the limit of downsizing!
Subthreshold leakage current of MOSFET

Subthreshold leakage current of MOSFET

- Ion
-loff

Vg=0V

Subthreshold region

Vth (Threshold Voltage)

Subthreshold Current Is OK at Single Tr. level

But not OK For Billions of Trs.
Subthreshold leakage current will limit the downsizing

\[ I_d (A/\mu m) \]

\[ V_g (V) \]

\[ I_{on} \]

\[ I_{off} \]

\[ 0 \]

\[ 0.15 \text{ V} \quad 0.3 \text{ V} \]

\[ 0.5 \text{ V} \quad 1.0 \text{ V} \]

\[ 10^{-11} \]

\[ 10^{-9} \]

\[ 10^{-7} \]

\[ 10^{-5} \]

Electron Energy
Boltzmann statics
Exp (qV/kT)

Injection
The limit is different depending on application.
How far can we go for production?

Past 0.7 times per 2.5 years
10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm → 0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

Limit depending on applications
Fundamental limit

Subthreshold
Drain bias induc

Intermediate node

• At least 4,5 generations to 8 ~ 5 nm
Extremely Thin SOI

Planar

Extremely Thin SOI

Drain bias induced depletion

Extremely thin Si

SiO₂

Si
Suppression of subthreshold leakage by surrounding gate structure

Planar

Multi gate

Drain bias induced depletion

Si fin or nanowire
Because of off-leakage control, Planar $\rightarrow$ Fin $\rightarrow$ Nanowire
Nanowire structures in a wide meaning

- Fin
- Tri-gate
- Tri-gate (Variation)
- Ω-gate
- All-around
Our work at TIT: Ω-gate Si Nanowire

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
- DIBL of 62mV/V and SS of 70mV/dec for nFET
More Moore to More More Moore

Technology node:
- Now:
  - 65nm, Lg 35nm
  - 45nm
  - 32nm, Lg 30nm
- Future:
  - 15nm, 11nm, 8nm, 5nm, 3nm
  - (Fin, Tri, Nanowire)

Si is still mainstream for future!!

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)
**High-k gate dielectrics**

Hf-based oxides

<table>
<thead>
<tr>
<th>Thickness</th>
<th>EOT</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>45nm</td>
<td>1nm</td>
<td>EOT=0.52 nm</td>
</tr>
<tr>
<td>32nm</td>
<td>0.95nm</td>
<td>Remote SiO₂-IL scavenging HfO₂ (IBM)</td>
</tr>
<tr>
<td>22nm</td>
<td>0.9nm</td>
<td>EOT=0.52 nm</td>
</tr>
<tr>
<td>15nm, 11nm, 8nm, 5nm, 3nm,</td>
<td></td>
<td></td>
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SiO₂ IL (Interfacial Layer) is used at Si interface to realize good mobility

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM2009, (IBM)

Direct contact with La-silicate (Tokyo Tech.)
## Benchmark of device characteristics

<table>
<thead>
<tr>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Lg (nm)</td>
<td>35 45nm 32nm</td>
<td>30 30</td>
<td>22</td>
<td>20 22</td>
<td>35/25 (nFET/pFET)</td>
<td>22/30 (nFET/pFET)</td>
<td>65</td>
<td></td>
</tr>
<tr>
<td>Gate Dielectrics</td>
<td>Hf-based</td>
<td>Hf-based</td>
<td>SiO2</td>
<td>HfO2</td>
<td>HfO2</td>
<td>Hf-based</td>
<td>HfZrO2</td>
<td>SiO2</td>
</tr>
<tr>
<td>EOT (nm)</td>
<td>1 0.95 0.9</td>
<td>0.9 3</td>
<td>~1</td>
<td>-</td>
<td>1.5</td>
<td>-</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Vth (V)</td>
<td>~0.4 0.3</td>
<td>~0.2 -0.15 (nFET)</td>
<td>0.3~0.4</td>
<td>~0.3</td>
<td>0.3~0.4</td>
<td>~0.5</td>
<td>-0.2 (nFET)</td>
<td></td>
</tr>
<tr>
<td>VDD (V)</td>
<td>1 1 0.8</td>
<td>1 0.9</td>
<td>0.9</td>
<td>1</td>
<td>1.1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_on (mA/um) nFET/pFET</td>
<td>1.36/1.07 1.53/1.23</td>
<td>1.26/1.1</td>
<td>0.83 (nFET)</td>
<td>0.59/0.62 (I_eff)</td>
<td>1.2/1.05</td>
<td>0.83/0.95</td>
<td>2.05/1.5</td>
<td>1.32 (nFET)</td>
</tr>
<tr>
<td>DIBL (mV/V) nFET/pFET</td>
<td>~150 ~200</td>
<td>46/50 &lt;50</td>
<td>-</td>
<td>104/115</td>
<td>65/105</td>
<td>56/9</td>
<td>62</td>
<td></td>
</tr>
<tr>
<td>SS (mV/dec)</td>
<td>- ~100</td>
<td>~70 &lt;80</td>
<td>-</td>
<td>87</td>
<td>85</td>
<td>&lt;80</td>
<td>70</td>
<td></td>
</tr>
</tbody>
</table>
**Ω-gate Si Nanowire**

- Conventional CMOS process
- High drive current
- DIBL of 62mV/V and SS of 70mV/dec for nFET

**Graphs and Figures**

- Drain Current (A) vs. Gate Voltage (V)
- Drain Current (mA/µm) vs. Drain Current (nA/µm)

**Key Numbers**

- **19 nm**
- **12 nm**

**References**

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)
Electron Density
(x10^{19} \text{cm}^{-3})

- **Edge portion**
- **Flat portion**

Distance from SiNW Surface (nm)

(a) Metal
(b) Inversion areal ratio: 29 %

V_g = 1 V
Tri-gate implementation for transistors

C. Auth et al., pp.131, VLSI2012 (Intel)

<table>
<thead>
<tr>
<th></th>
<th>HP</th>
<th>MP</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>(T_{\text{OX,E}}) (nm)</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>(L_{\text{GATE}}) (nm)</td>
<td>30</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>(I_{\text{OFF}}) (nA/um)</td>
<td>20-100</td>
<td>5-20</td>
<td>1-5</td>
</tr>
</tbody>
</table>

Tri-gate has been implemented since 22nm node, enabling further scaling
• $L_g$ and EOT are larger than ITRS requirements

• Implementation of Tri-gate and lower $V_{th}/V_{dd}$ since 22nm

*K. Mistry et al., pp.247, IEDM2007 (Intel).*

*P. Packan et al., pp.659, IEDM2009 (Intel).*

*C. Auth et al., pp.131, VLSI2012 (Intel).*
Tri-gate width/height optimization

C. Auth et al., pp.131, VLSI2012 (Intel)

Intel’s fin is triangle shape!

PMOS channel under the gate
S/D region showing the SiGe epitaxy

A fin width of 8nm to balance SCE and $R_{\text{ext}}$
A fin height of 34nm to balance drive current vs. capacitance
SS of 71 and 72 mV/dec for HP NMOS and PMOS, respectively

DIBL of 30 and 35 mV/V for NMOS and PMOS, respectively

Vth of 22 nm is about 0.1 ~0.2 V lower than that of 32 nm
Extremely Thin SOI (ETSOI)

K. Cheng et al., pp.419, IEDM2012 (IBM)

Also, ET-SOI works very good!

- Hybrid CMOS
- Si Channel nFET
- Strained SiGe Channel pFET

RO delay improvement over FinFET with FO = 2
• \( L_g = 25\sim35 \text{nm} \) GAA NW

• Hydrogen anneal provide smooth channel surface

• Competitive with conventional CMOS technologies

• Scaling the dimensions of NW leads to suppressed SCE
3. Problems
Short-channel effect

T. Skotnicki, IEDM 2009 Short Course (STMicroelectronics)

\[ SCE = 0.64 \frac{\varepsilon_s}{\varepsilon_{ox}} \times E_I \times \Phi_d \]
\[ DIBL = 0.8 \frac{\varepsilon_s}{\varepsilon_{ox}} \times E_I \times V_{ds} \]

\[ E_I = 1 \times \left(1 + \frac{X^2}{L_{el}}\right) \times T_{ox} \frac{T_{dep}}{L_{el}} \]
\[ E_I = 1 \times \left(1 + \frac{T_{si}^2}{L_{el}}\right) \times T_{ox} \frac{T_{si} + \lambda T_{box}}{L_{el}} \]
\[ E_I = 1 \times \left(1 + \frac{T_{si}^2}{L_{el}}\right) \times T_{ox} \frac{T_{si} + \lambda T_{box}}{L_{el}} \]
\[ E_I = 1 \times \left(1 + \frac{T_{si}^2 / 4}{L_{el}}\right) \times T_{ox} \frac{T_{si} / 2}{L_{el}} \]

If max ch. doping is \(10^{20}\) cm\(^{-3}\) := Tep~12nm then:
If max ch. doping is \(10^{21}\) cm\(^{-3}\) := Tep~12nm then:
\(T_{box} = 145\) nm
\(\lambda T_{box} = 18\) nm
\(T_{box} = 10\) nm
\(\lambda T_{box} = 3\) nm

If \(T_{si}\) mm \(\approx 3\) nm then:
If \(T_{si}\) mm \(\approx 3\) nm then:
If \(T_{si}\) mm \(\approx 3\) nm then:
If \(T_{si}\) mm \(\approx 3\) nm then:

\(L_{el,\text{min}}\)
\(= 34\) nm
\(= 34\) nm
\(\approx 30\) nm
\(\approx 10\) nm
\(\approx 6\) nm
\(\approx 2.7\) nm

(DIBL=100mV/V)
Sub-threshold Slope

\[ S = \frac{kT}{q} \ln \left( 1 + \frac{C_{dep}}{C_{ox}} + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \frac{L_{ox}}{L_{el}} \left( 1 + \frac{3T_{dep}}{4L_{el}} \right) \left( 1 + 2 \frac{V_{ds}}{\Phi_d} \right) \right) \]

**BULK**
- \( X_j = 3/4L_{el} \)
- \( T_{dep} = 3/4L_{el} \)
- 95 mV/dec

**III-V**
- \( T_{ox} + 2A \)
- \( \varepsilon_{Si} + 15\% \)
- 110 mV/dec

**FDSOI**
- \( T_{dep} = T_{si}/2 \)
- \( X_j = T_{si}/2 \)
- 85 mV/dec

**UTBB**
- \( RBB \rightarrow P_{stat} \)
- 75 mV/dec

**FinFET**
- 65 mV/dec
Problems in Multi-gate

S. Bangsaruntip et al., pp.297, IEDM2009 (IBM),
K. Tachi et al., pp.313, IEDM2009 (CEA-LETI)

Decreasing the diameter of NW

Improved short-channel control ↔ Severe mobility degradation

Need to decrease diameter for SCH

Significant μ degradation at diameter < 10 nm

Decreasing the diameter of NW

Effective mobility [cm²/Vs]

Circular SNWT 5nm in dia.

Rectangular SNWTS

PFETs

NFETs

DIBL (mV/V)

L_G (nm)

W (nm) / H (nm)

~ 5 / ~ 6
6.8 / 9.5
9.0 / 13.9
11.2 / 20.0

W (nm) / H (nm)

6.8 / 9.5
12.3 / 15.1
16.5 / 22.1
21.6 / 23.8
Impact of Si thickness in FinFET

- Replacement Gate process
- TaN/HfO₂ gate stack
- Reduced $g_m$ and higher $V_{th}$ with decreasing Fin width
Problems in SOI

K. Uchida et al., pp.47, IEDM2002 (Toshiba)

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

$< 10 \text{ nm}$

1. Mobility degradation
   
   Extremely small distance between the electron and all around Si surface.

   Strong scattering of electrons by interaction with all around Si surface.

2. Electron density decrease
   
   Decrease of DOS in extremely narrow wire.

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-k is necessary.
Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used

Energy (eV)

3.8
3.7
3.6
3.5
3.4
3.3
3.2
3.1
3.0
0.0
0.1
0.2
0.3
0.4
0.5

Energy (eV)

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0.2
0.3
0.4
0.5

Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used

Energy (eV)
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Wire cross section dependence.

What cross section gives best solution for SCE suppression and drive current?
Significant increase in $V_{th}$ variability with decreasing Fin width
Smaller wire/fin width is necessary for SCE suppression

But mobility and $I_{ON}$ severely degrade with wire/fin width reduction

Therefore even in multi-gate structures, **EOT scaling should be accelerated** to provide SCE immunity
High-k beyond 0.5 nm
Limit in $t_{ox}$ thinning

Gate oxide should be thicker than mono atomic layer
0.8 nm gate oxide thickness MOSFETs operate
0.8 nm $\rightarrow$ Distance of 3 Si atoms $\rightarrow$ 2 mono layers

*R.Chau, et al., (Intel) IWGI 2003*
Gate Leakage Power Density becomes significantly large with $L_g$ reduction, and thus, with $t_{ox}$ thinning!!
To use high-k dielectrics

K: Dielectric Constant

Thin SiO₂

K=4

Almost the same electric characteristics

Thick high-k dielectrics

K=20

5 times thicker

Small leakage Current

However, very difficult and big challenge!
Combination of high-k and metal gate is important

*K. Natori, et al., (Tsukuba Univ) SSDM 2005, p.286*

**Equivalent Oxide Thickness (EOT):**
- gate dielectrics itself, $C_{OX}$
- Capacitance Equivalent Thickness (CET): entire gate stack,
  \[ \text{Inversion CET} = T_{inv} \approx \text{EOT} + 0.4 \text{nm} \]

With metal gate electrode

$C_{metal}$ is finite because of quantum effect. In other words, electron is not a point charge located at the interface but distributed charge.
### Choice of High-k elements for oxide

**Candidates**

<table>
<thead>
<tr>
<th>H</th>
<th>Unstable at Si interface</th>
</tr>
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<tbody>
<tr>
<td>Li</td>
<td>Si + MO\textsubscript{x} M + SiO\textsubscript{2}</td>
</tr>
<tr>
<td>Be</td>
<td>Si + MO\textsubscript{x} MSi\textsubscript{x} + SiO\textsubscript{2}</td>
</tr>
<tr>
<td>Mg</td>
<td>Si + MO\textsubscript{x} M + MSi\textsubscript{x}O\textsubscript{y}</td>
</tr>
</tbody>
</table>

**Gas or liquid at 1000 K**

- Radio active
  - He
  - B
  - C
  - N
  - O
  - F
  - Ne

**La\textsubscript{2}O\textsubscript{3} based dielectrics** are thought to be the next generation materials, which may not need a thicker interfacial layer.

**HfO\textsubscript{2} based dielectrics** are selected as the first generation materials, because of their merit in:
1) band-offset,
2) dielectric constant
3) thermal stability

---

**Choice of High-k elements for oxide**

- R. Hauser, IEDM Short Course, 1999
Issues in high-k/metal gate stack

Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
Flat metal/high-k interface for better mobility
Suppression of metal diffusion
Suppression of oxygen vacancy formation
Small interfacial state density at high-k/Si
Control of interface reaction and Si diffusion to high-k
Suppression of gate leakage current
Endurance for high temperature process
Reliability: PBTI, NBTI, TDDB
Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
Workfunction engineering for $V_{th}$ control
Suppression of FLP
Interface dipole control for $V_{th}$ tuning
Remove contamination introduced by CVD
Thinning or removal of SiO$_2$-IL for small EOT

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Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band Discontinuity [eV] vs. Dielectric Constant $\varepsilon(0)$

XPS measurement by Prof. T. Hattori, INFOS 2003
Direct high-k/Si by silicate reaction

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface. Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI 2010, p.69
Direct high-k/Si by silicate reaction

HfO₂ case

La₂O₃ case

Our approach

Direct contact can be achieved with La₂O₃ by forming silicate at interface
Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
**SiO$_x$-IL growth at HfO$_2$/Si Interface**

Phase separator

\[ \text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{SiO}_x-\text{IL} \]

\[ \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2 \]

Oxygen supplied from W gate electrode

\[ \text{SiO}_x-\text{IL} \text{ is formed after annealing} \]

Oxygen control is required for optimizing the reaction

D.J.Lichtenwalner, Trans. ECS 11, 319

H. Shimizu, JJAP, 44, pp. 6131
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Cluster tool for HKMG Stack

EB Deposition for HK

Flash Lamp

Sputter for MG

Robot

ALD

RTA

Entrance

5m

5m

5m
Cluster Chambers for HKMG Gate Stack

EB Deposition: HK
Flash Lamp
Anneal
ALD: HK
Sputter: MG
Robot
RTA
Entrance
Deposited thin film

Substrate

Moving Mask

Flux

Source

Electron Beam

77
L = 0.5~100 µm (8 kinds)
W = 10, 20, 50, 100 µm (4 kinds)

26 chips

1 cm x 1 cm

30 different Trs
Gate Leakage vs EOT, \( (V_g=|1|V) \)

- **Materials:**
  - Al\(_2\)O\(_3\)
  - HfAlO(N)
  - HfO\(_2\)
  - HfSiO(N)
  - HfTaO
  - La\(_2\)O\(_3\)
  - Nd\(_2\)O\(_3\)
  - Pr\(_2\)O\(_3\)
  - PrSiO
  - PrTiO
  - SiON/SiN
  - Sm\(_2\)O\(_3\)
  - SrTiO\(_3\)
  - Ta\(_2\)O\(_5\)
  - TiO\(_2\)
  - ZrO\(_2\)(N)
  - ZrSiO
  - ZrAlO(N)

- **Graph:**
  - Y-axis: Current density (A/cm\(^2\))
  - X-axis: EOT (nm)

- **Legend:**
  - Diamond: Al\(_2\)O\(_3\)
  - Green: HfAlO(N)
  - Blue: HfO\(_2\)
  - Red: HfSiO(N)
  - Yellow: HfTaO
  - Orange: La\(_2\)O\(_3\)
  - Black: Nd\(_2\)O\(_3\)
  - Blue: Pr\(_2\)O\(_3\)
  - Grey: PrSiO
  - Yellow: PrTiO
  - Red: SiON/SiN
  - Black: Sm\(_2\)O\(_3\)
  - Yellow: SrTiO\(_3\)
  - Yellow: Ta\(_2\)O\(_5\)
  - Magenta: TiO\(_2\)
  - Green: ZrO\(_2\)(N)
  - Green: ZrSiO
  - Green: ZrAlO(N)
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small Dit

1. Silicate-reaction-formed fresh interface

La<sub>2</sub>O<sub>3</sub> La-silicate

Si sub.

2. Stress relaxation at interface by glass type structure of La silicate.

FGA 800°C is necessary to reduce the interfacial stress


La$_2$O$_3$

No interfacial layer can be confirmed with Si/TiN/W
La$_2$O$_3$/silicate/$n$-Si CV

Capacitance density ($\mu$F/cm$^2$)

Gate voltage (V)

W/La$_2$O$_3$(4nm)/$n$-Si

600°C, 30min

$\Delta V_{fb}$

$C_{fb}$
$D_{it}$, $D_{slow}$

(FG anneal)

$D_{slow}$

400°C

500°C

600°C

$D_{it}$

Annealing temperature (°C)

$D_{it}$, $D_{slow}$ (cm$^{-2}$/eV)

$G_p/\omega$ (F/cm$^2$)

$\omega$ (rad/s)

$10^1$ $10^2$ $10^3$ $10^4$ $10^5$ $10^6$ $10^7$

$10^1$ $10^2$ $10^3$ $10^4$ $10^5$ $10^6$ $10^7$

$10^{11}$ $10^{12}$ $10^{13}$ $10^{14}$

as

200 400 600 800 1000
It is important to change the La2O3 to La-silicate completely.
Annealed for 2 s
La$_2$O$_3$(3.5 nm)

W(60 nm)

TiN/W(6 nm)

As depo

EOT=0.55nm

TaN/(45nm)/W(3nm)
900°C, 30min
EOT=0.55nm

Vg (V)
Cg (μF/cm$^2$)

Experiment
Theory
TaN(45nm)/W(3nm) 900°C, 30min

$Q_{fix} = 1 \times 10^{11}$ cm$^{-2}$

Fixed Charge density: $1 \times 10^{11}$ cm$^{-2}$
$E_{\text{OT}} = 0.53\text{nm}$

- $L/W = 20/20\mu\text{m}$
- $T = 300\text{K}$
- $N_{\text{sub}} = 3 \times 10^{16}\text{cm}^{-3}$
- $V_g = 0\text{V}$
- $E_{\text{eff}} = 1\text{MV/cm}$
- $151\text{cm}^2/\text{Vs}$
- $150\text{cm}^2/\text{Vs}$
The diagram shows the gate current (A/cm²) as a function of gate voltage (V) for a TaN/W/LaSiOₓ/nFET device. The graph includes a logarithmic scale for both axes, with the current ranging from 10⁻⁵ to 10⁴ A/cm² and the voltage from 0.0 to 1.2 V. The ITRS line is marked at 10⁻¹ A/cm², and the device parameters are indicated as Wₓ/Lₓ = 20/20 μm and EOT = 0.55 nm.
Benchmark of La-silicate dielectrics

**Gate Leakage current**

![Gate Leakage current graph]

- ITRS requirement
- Our data: La-silicate gate oxide

**Effective Mobility**

![Effective Mobility graph]

- Solid circle: Our data
- Open square: Hf-based oxides


*T. Ando, et al., (IBM) IEDM 2009, p.423*
<table>
<thead>
<tr>
<th>Gate stack</th>
<th>EOT</th>
<th>Mobility</th>
<th>$V_{th}$</th>
<th>SS</th>
<th>DIBL</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.52nm</td>
<td>110cm$^2$/Vs (at 1x10$^{13}$cm$^{-2}$)</td>
<td>~0.4V (L$_g$=24nm)</td>
<td>90mV/dec</td>
<td>147mV/V</td>
<td>IBM VLSI2011</td>
</tr>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.55nm</td>
<td>140cm$^2$/Vs (at 1MV/cm)</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>IBM VLSI2009</td>
</tr>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.45nm</td>
<td>115cm$^2$/Vs (at 1x10$^{13}$cm$^{-2}$)</td>
<td>0.3V (L$_g$=10um)</td>
<td>–</td>
<td>–</td>
<td>IMEC MEE2011</td>
</tr>
<tr>
<td>Metal/HfO$_2$</td>
<td>0.59nm</td>
<td>130cm$^2$/Vs (at 1MV/cm)</td>
<td>0.45V (L$_g$=1um)</td>
<td>75mV/dec</td>
<td>–</td>
<td>Sematech VLSI2009</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.65nm</td>
<td>–</td>
<td>0.3~0.4V (L$_g$=~30nm)</td>
<td>90mV/dec</td>
<td>100mV/V</td>
<td>Samsung VLSI2011</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.95nm</td>
<td>–</td>
<td>~0.3V (L$_g$=30nm)</td>
<td>100mV/dec</td>
<td>~200mV/V</td>
<td>Intel IEDM2009</td>
</tr>
<tr>
<td>W/La-silicate 93</td>
<td>0.62nm</td>
<td>155cm$^2$/Vs (at 1MV/cm)</td>
<td>-0.08V (L$_g$=10um)</td>
<td>~70mV/dec</td>
<td>–</td>
<td>Tokyo Tech. T-ED2012</td>
</tr>
</tbody>
</table>
ALD of La$_2$O$_3$


ALD is indispensable from the manufacturing viewpoint primarily for the precise control of film thickness and good uniformity.
Advantages of metal S/D
- atomically abrupt junction
- low parasitic resistance
- reduced channel dopant concentration

Issues in metal S/D
- two different $\phi_B$ for $p/n$-ch FETs
- underlap/overlap to the gate
- narrow process temperature window

Metal S/D is considered for alternative channel material such as InGaAs and Ge

Ni is used both on InGaAs and Ge to form alloy.

L. Hutin, pp. 45, IEDM2009 (CEA-LETI)

S.-H. Kim, IEDM (2010) 596

K. Ikeda, VLSI (2012) 165
4. Alternative channel devices
## Ge, III-V bulk properties

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>electron mob. (cm²/Vs)</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
</tr>
<tr>
<td>electron effective mass (/m₀)</td>
<td>m₁: 0.19  m₁: 0.916</td>
<td>m₁: 0.082  m₁: 1.467</td>
<td>0.067</td>
<td>0.08</td>
<td>0.026</td>
<td>0.0135</td>
</tr>
<tr>
<td>hole mob. (cm²/Vs)</td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td>hole effective mass (/m₀)</td>
<td>m_HH: 0.49  m_LH: 0.16</td>
<td>m_HH: 0.28  m_LH: 0.044</td>
<td>m_HH: 0.45  m_LH: 0.082</td>
<td>m_HH: 0.45  m_LH: 0.12</td>
<td>m_HH: 0.57  m_LH: 0.35</td>
<td>m_HH: 0.44  m_LH: 0.016</td>
</tr>
<tr>
<td>band gap (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.14</td>
</tr>
<tr>
<td>permittivity</td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

- Ge ⇒ lightest hole $m^*$ (light electron $m^*$) ⇒ pMOS (CMOS)
- III-V ⇒ light electron $m^*$ ⇒ nMOS
- GaAs ∙ InP ⇒ $E_g$ higher than that in Si ⇒ low power
nMOS

- InGaAs GAA
  - $L_{ch}=50\, \text{nm}$, Dielectric: $10\, \text{nm} \, \text{Al}_2\text{O}_3$
  - $V_{DS}=0.5\, \text{V}$ (Purdue Uni.) [a]

- Si-FinFET 32nm
  - Intel $V_{DD}=0.8\, \text{V}$ [10]

- InGaAs Tri-gate
  - $L_g=60\, \text{nm}$, EOT 12A
  - $V_{DS}=0.5\, \text{V}$ (Intel) [b]

- Si-FinFET 22nm
  - Intel $V_{DD}=0.8\, \text{V}$ [j]

- Si-bulk 45nm
  - Intel $V_{DD}=1\, \text{V}$ [k]

- InGaAs Nanowire
  - $L_g=200\, \text{nm}$, $T_{ox} = 14.8\, \text{nm}$
  - $V_{DS}=0.5\, \text{V}$ (Hokkaido Uni.) [d]

- Metal S/D InGaAs-OI
  - $L_{ch}=55\, \text{nm}$, EOT 3.5nm
  - $V_{DS}=0.5\, \text{V}$ (Tokyo Uni.) [e]

- Ge GAA $L_g = 300\, \text{nm}$,
dielectric: GeO$_2$(7nm)-HfO$_2$(10nm)
  - $V_D=-0.8\, \text{V}$ (ASTAR Singapore) [h]

- Ge Tri-gate
  - $L_g=183\, \text{nm}$, EOT 5.5nm
  - $V_D=-1\, \text{V}$ (NNDL Taiwan) [i]

- Si-FinFET 32nm
  - Intel $V_{DD}=0.8\, \text{V}$ [j]

pMOS

- GOI Tri-gate
  - $L_g=65\, \text{nm}$, EOT 3.0nm
  - $V_D=-1\, \text{V}$ (AIST Tsukuba) [f]

- Si-FinFET 22nm
  - Intel $V_{DD}=0.8\, \text{V}$ [j]

- Ge FinFET $L_g=4.5\, \text{mm}$,
  Dielectric: SiON, $V_{DS}=-1\, \text{V}$

- Si-bulk 45nm $V_{DD}=1\, \text{V}$

- Ge Tri-gate
  - $L_g=183\, \text{nm}$, EOT 5.5nm
  - $V_D=-1\, \text{V}$ (NNDL Taiwan) [i]

References:

[a] J. J. Gu et al., pp.769, IEDM2011 (Purdue).
[b] M. Radosavljevic et al., pp.765, IEDM201 (Intel).
[e] S. H. Kim et al., pp.177, VLSI2012 (Tokyo Uni)
[g] J. Feng et al., IEEE EDL 28(2007)637 (Stanford Uni)
[h] J. Peng et al., pp.931, IEDM2009 (ASTAR Singapore)
[i] S. Hsu et al., pp.825, IEDM2011 (NNDL Taiwan)
[j] C. Auth et al., pp.131, VLSI2012 (Intel).
ION/I_OFF Benchmark of Ge pMOSFET

K. J. Kuhn, ECS Transactions, 33 (6) 3-17 (2010)

Optimization of short channel Ge p-MOSFETs is still under investigation
## III-V/Ge Benchmark for Various Structures

<table>
<thead>
<tr>
<th>Material</th>
<th>Planar (metal S/D, Strain, Buffer...)</th>
<th>FinFET</th>
<th>Tri-gate</th>
<th>Gate-all-around MOSFET</th>
<th>Nanowire</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric /EOT</td>
<td>Al₂O₃/3.5 nm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>7.6 Å HfO₂+ Al₂O₃+ GeO₂</td>
<td>5 nm ALD Al₂O₃</td>
<td>5 nm ALD Al₂O₃</td>
<td>5.5 nm (Al₂O₃+ GeO₂)</td>
<td>10 nm- ALD Al₂O₃</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SiON</td>
<td>1.2 nm</td>
<td></td>
<td>HfO₂: 11 nm</td>
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<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td>HfAlO: 14.8 nm</td>
</tr>
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<td></td>
<td></td>
<td>3.0 nm (ALD Al₂O₃)</td>
</tr>
<tr>
<td>Mobility</td>
<td>-</td>
<td>~600 (cm²/Vs)</td>
<td>~700 (μS/μm)</td>
<td>-</td>
<td>701 (μS/μm)</td>
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<td></td>
<td>~500 (μS/μm)</td>
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<td>~850 (cm²/Vs)</td>
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<tr>
<td>Lₙ (nm)</td>
<td>55</td>
<td>W/L=50/5 μm</td>
<td>50 μm</td>
<td>100</td>
<td>50</td>
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<td>DIBL (mV/V)</td>
<td>84</td>
<td>-</td>
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<td>210</td>
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<td></td>
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<td>~50</td>
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<td>SS (mV/dec)</td>
<td>105</td>
<td>-</td>
<td>145</td>
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<tr>
<td>Iₜₜ (µA/µm) (Vₒ=0.5V)</td>
<td>278</td>
<td>3</td>
<td>4 (n,p)</td>
<td>-</td>
<td>10</td>
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<tr>
<td></td>
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<td>(Vₒ=0.2V)</td>
<td>(Vₒ=0.5V)</td>
<td>400</td>
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<td>NNDL Taiwan IEDM 2011</td>
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<td>ASTAR Singapore IEDM 2009</td>
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<td>Hokkaido Uni, IEDM 2011</td>
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<td>AIST Tsukuba VLSI 2012</td>
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<td>AIST Tsukuba VLSI 2012</td>
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</tbody>
</table>
Achieving both N- and P-type MOSFET on a single channel is possible

In-content of 20-40% improves performance

electron/hole mobility > 4000/900 cm²/Vs was gained in a single channel material

I_{ON} at L_G = 50 µm

pMOS: 4 µA/µm
nMOS: 3.8 µA/µm
Metal S/D and InAs buffer layer are used as performance boosters.

- DIBL=84 mV/V and SS=105 mV/V was shown for $L_{ch} = 55$ nm when In-content was higher.

S. H. Kim et al., pp.177, VLSI2012 (Tokyo Uni)
Common gate stack (NUS)

Common InGaAs-GeSn gate stack (NUS)


- Common gate stack (gate metal and dielectric) were used for both p- and n-type
- Si$_2$H$_6$ plasma passivation is employed which creates Si layer at interface.
  
  **SS**: $n$MOS: 90 (mV/decade)
  
  **pMOS**: 190 (mV/decade)

- High intrinsic peak $G_{M,\text{Sat}}$ of ~465 $\mu$S/ $\mu$m at $V_{DS}=-1.1$ V was achieved for $L_G=250$ nm.

V$_{GS}-V_{TH} = 0 \sim 2.0$V

$L_G = 5 \mu$m
Core-multishell InGaAs nanowires grown without buffer layer on Si substrate (bottom up approach)

At $V_d = 1$ V peak transconductance of 500 mS/mm is achieved (roughly x3 InGaAs nanowire)
Tri-gate structure has superiority electrostatic controllability compared to ultra-thin body planar structure

Steepest SS and smallest DIBL ever reported ($W_{\text{fin}} = 30$nm)
Inversion mode In$_{0.53}$Ga$_{0.47}$As MOSFET with ALD Al$_2$O$_3$/WN with well electrostatic properties

DIBL was suppressed down to

$L_{ch} = 50\text{nm}$ and $G_{m,max} = 701\text{mS/mm}$ at $V_{ds} = 1V$
DIBL = 135 mV/V and drive current over 840 μA/µm at \( L_{ch} = 130\)nm and \( V_{ds} = 1.5V \) was achieved
**Ge-nanowire pMOSFET (AIST, Tsukuba)**

Using Ni-Ge alloy as metal S/D

Significantly reduces contact resistance

High saturation current and high mobility

\[ \mu_{\text{eff}} = 855 \text{ cm}^2/\text{Vs} \text{ at } N_s = 5 \times 10^{12} \text{cm}^{-2} \]

and saturation drain current of

\[ 731 \mu \text{A/\mu m at } V_d = -1\text{V} \]
Selective etching of high defect Ge near Ge/Si interface is used which improves gate controllability.

\[
\frac{I_{ON}}{I_{OFF}} = 10^5 \text{ and } SS = 130 \text{ mV/dec}
\]

And \( I_{ON} = 235 \, \mu \text{m/\mu m at } V_D = -1V \)
Implementing high-k material to III-V, Ge

**III-V** (InGaAs, InAs, InGaSb, …)
- ALD-$\text{Al}_2\text{O}_3$ is most commonly used as gate dielectric in planar or Multi-gate
- HfO$_2$-only stacks have high $D_{it}$ (combination of $\text{Al}_2\text{O}_3$ or Al or Si is used)

<table>
<thead>
<tr>
<th>ALD-$\text{Al}_2\text{O}_3$</th>
<th>Si-HfO$_2$</th>
<th>$\text{Al}_2\text{O}_3$+HfO$_2$</th>
<th>HfAlO$_x$</th>
<th>TaSiO$_x$</th>
</tr>
</thead>
</table>

- By controlling the formation of GeO$_x$ at the interface, HfO$_2$ and $\text{Al}_2\text{O}_3$ show good results.

---

**Ge**
- By controlling the formation of GeO$_x$ at the interface, HfO$_2$ and $\text{Al}_2\text{O}_3$ show good results.

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**References**
- E. Kim, et al., APL96, 012906
- L. Chu, et al., APL99, 042908
- Hokkaido Uni, IEDM 2011
- Intel, IEDM 2010
- R. Zhang et al., VLSI2012, p161
5. Emerging devices
Emerging devices (future scaling trends)

**Carbon-based FET**

Carbon nanotube

Graphene

GaAs mHEMT

SiMOSFET (29nm)

GaAs pHEMT (100nm)

CNT

Graphene

Junctionless Transistor

All-spin logic device

Tunnel FET

Low $I_{OFF}$, Low $V_{DD}$, SS<60mV/decade

Band to band tunneling
TFET vs. MOSFET at low $V_{DD}$

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

- **TFET**
  - $EOT = 1$ nm
  - $L_G = 20$ nm
  - $t_{InAs} = 5$ nm

- **MOSFET** vs. TFET at low $V_{DD}$

<table>
<thead>
<tr>
<th></th>
<th>TFET @0.35V</th>
<th>CMOS @0.3V</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Stage (ps)</td>
<td>Switching Energy (fJ)</td>
</tr>
<tr>
<td>INV (FO=3)</td>
<td>105</td>
<td>0.26</td>
</tr>
<tr>
<td>NAND (FO=3)</td>
<td>149</td>
<td>0.32</td>
</tr>
<tr>
<td>NOR (FO=3)</td>
<td>158</td>
<td>0.34</td>
</tr>
<tr>
<td>Combined</td>
<td>129</td>
<td>0.29</td>
</tr>
</tbody>
</table>

- $V_{DD}$ 0.3~0.35V
- TFET 8x faster at the same power
- “parameter variation is not a significant factor for differentiation between MOSFET and TFET”
X in Si$_{1-x}$Ge$_x$ is optimized to allow for efficient BTBT

$L_G = 200$nm

$I_{ON}/I_{OFF} \approx 10^5$

Reducing SiGe Body thickness improves Subthreshold swing.

130mV/dec

190mV/dec
SS of TFET is function of $V_G$ due to Zener tunnel current

Minimum SS = 21 mV/dec is reached due to optimized series resistance of contact, undoped InAs and InAs/Si

$I_{ON}/I_{OFF} \sim 10^6$ at $V_{DS} = 1.0V$ ($I_{ON} = 1\text{A}_{\mu}/\mu\text{m}$)
Device structure

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

- Tunneling // to the gate oblique to the gate field
- Tunneling ⊥ to the gate in-line with the gate field

Nanowire TFET gate-all-around - best electrostatics

K. Tomioka et al., pp.47, VLSI2012 (Hokkaido University)
measured III-V channel TFETs

<table>
<thead>
<tr>
<th>Reference</th>
<th>Source</th>
<th>Channel</th>
<th>Dielectric</th>
<th>EOT</th>
<th>$I_{ON}$</th>
<th>$V_{DS}$</th>
<th>$V_{GS} = V_{TH}$</th>
<th>$V_{ON} - V_{OFF}$</th>
<th>$I_{ON}/I_{OFF}$</th>
<th>$S_{MIN}$</th>
<th>$S_{EFF}$</th>
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</thead>
<tbody>
<tr>
<td>this work</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.6</td>
<td>78</td>
<td>0.5</td>
<td>0.5</td>
<td>1.5</td>
<td>2,000</td>
<td>125</td>
<td>230</td>
</tr>
<tr>
<td>Li [4]</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$</td>
<td>3.9</td>
<td>20</td>
<td>0.3</td>
<td>2</td>
<td>6</td>
<td>210</td>
<td>830</td>
<td>1300</td>
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<tr>
<td>Mookerjea [5]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>5.6</td>
<td>10</td>
<td>0.5</td>
<td>2.5</td>
<td>2.5</td>
<td>10,000</td>
<td>240</td>
<td>310</td>
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<tr>
<td>Mohata [6]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>2.8</td>
<td>10</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>400,000</td>
<td>200</td>
<td>180</td>
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<tr>
<td>Zhao [7]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>20</td>
<td>0.45</td>
<td>1</td>
<td>1.5</td>
<td>30,000</td>
<td>86</td>
<td>170</td>
</tr>
<tr>
<td>Zhao [8]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>40</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>200,000</td>
<td>84</td>
<td>190</td>
</tr>
<tr>
<td>Ford [9]</td>
<td>InAs</td>
<td>InAs</td>
<td>ZrO$_2$</td>
<td>2</td>
<td>0.4</td>
<td>0.5</td>
<td>1</td>
<td>1</td>
<td>200</td>
<td>190</td>
<td>220</td>
</tr>
<tr>
<td>Zhou [10]</td>
<td>In$<em>{0.53+}$Ga$</em>{0.47+}$As</td>
<td>In$<em>{0.53+}$Ga$</em>{0.47+}$As</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.3</td>
<td>20</td>
<td>0.5</td>
<td>1</td>
<td>1.75</td>
<td>450,000</td>
<td>93</td>
<td>150</td>
</tr>
</tbody>
</table>

- **$S_{MIN}$**: Most common SS which is the inverse of $I_D$-$V_{GS}$ slope at the steepest part
- **$S_{EFF}$**: Is the average swing when $V_{TH} = V_{DD}/2$, $V_{OFF} = 0$

**Average SS**: $\frac{V_{TH} - V_{OFF}}{\log(I_D/I_{OFF})}$

**Effective SS**: $\frac{V_{DD}}{2\log(I_D/I_{OFF})}$
$I_{ON}$ and $I_{OFF}$ of TFETs

[1] G. Zhou et al., pp. 782, vol. 33, no. 6, EDL 2012 (University of Notre Dame)

C. Auth et al., pp.131, VLSI2012 (Intel).

K. Mistry et al., pp.247, IEDM2007 (Intel).
MEMS relay

- $I_{ON}/I_{OFF}$ of $\sim 10^{10}$
- Ultra-low-power digital logic applications.

- Frequency of 1, 5, 25kHz under operation

T. K. Liu et al., pp. 43, VLSI2012 (UC Berkeley)
Junctionless Accumulation Mode

- **IM**: Conventional Inversion Mode
- **JAM LD**: Junctionless Accumulation Mode with low dope
- **JAM HD**: Junctionless Accumulation Mode with high dope

JAM devices have **reduced gate control** and **degraded short-channel** characteristics relative to IM.

- Not suitable for high-performance logic (high $I_{on}$ and moderate $I_{off}$)

R. Rios et al., EDL. 32(2011)1170

![Graph](https://example.com/graph.png)

- $V_t$ (V)
- $DIBL$ (mV/V)
- $I_{dsat}$ (mA/μm)

$L_g$ (nm)

20 30 40

20 30 40

20 30 40
Near-ideal subthreshold slope, close to 60 mV/dec at room temperature, and extremely low leakage currents

- Silicon nanowire is uniformly doped
- Gate material is opposite polarity polysilicon

\[
\frac{I_{ON}}{I_{OFF}} \approx 1 \times 10^6 \quad (-1 < V_g < 1)
\]

\[I_{OFF} \text{ is smaller than } 10^{-15} \text{ A} \]
SWCNT : single wall carbon nanotube
GNR : graphene nano ribbon

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>SWCNT</th>
<th>GNR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mobility cm²/V/s</td>
<td>1400</td>
<td>&gt;10000</td>
<td>&gt;10000 for large widths</td>
</tr>
<tr>
<td>Mean free path (nm) @ room temp</td>
<td>30</td>
<td>&gt;1,000</td>
<td>~1,000 for small widths</td>
</tr>
<tr>
<td>Thermal conductivity (W/mK)</td>
<td>150</td>
<td>5800</td>
<td>~5000</td>
</tr>
</tbody>
</table>

Carbon materials for FET applications
- an ultra-thin body for aggressive channel length scaling
- excellent intrinsic transport properties similar to carbon nanotubes
- pattern the desired device structures
Sub-10nm carbon nanotube transistor

A. D. Franklin et al., pp.525, IEDM2011 (IBM)

Transistor operation with $L_{\text{ch}}$ of 9nm
- Ambipolar Characteristics
- Bi-layer graphene and double gates can open the gap
2D material: single layer MoS$_2$

- Mobility of 190 cm$^2$/Vsec
- $I_{on}$ of 1 $\mu$A/$\mu$m at $V_{DD} = 1$V

Candidate: MoS$_2$, MoSe$_2$, WSe$_2$, MoTe$_2$, WTe$_2$
Magnetic tunnel junction on S/D

Read/write are enabled by using ferromagnetic electrodes and Spin-polarized current
## Summary of Emerging Technology pro/cons

<table>
<thead>
<tr>
<th>Technology</th>
<th>Advantage</th>
<th>Issues</th>
</tr>
</thead>
</table>
| TFET             | Lower $V_{dd}$  
Lower $I_{OFF}$                                         | Integration  
higher $I_{ON}$                               |
| CNT FET          | Higher transport velocity  
$L_g$ scaling                                 | High density and alignment, reproducibility, integration |
| Graphene FET     | RF application  
Large area manufacturing                                       | NOT a direct replacement for Silicon logic       |
| MEMS             | Extremely low leakage  
Ultra-low digital logic                                          | Endurance  
Slow speed, scalability                           |
| Junctionless FET | CMOS process compatibility                                                | Worse gate control in short-channel              |
| Spin FET         | Low power, suitable for memory (nonvolatile info storage)                 | Low efficiency of spin injection                 |
Conclusions
Conclusions

- New device structures (FinFET, Tri-gate) are replacing conventional Planar CMOS

  - Same performance at lower supply voltage

- HKMG: Continuous innovation has enabled EOT scaling to 9 Å, however, new material could be needed for further EOT scaling.

  - La-based high-k material

- Recent advances in new channel material shows promising device performances but still far to catch up Si-CMOS.

  - The combination of III-V channel materials with a multi-gate structure appears to be a promising direction.
    (Higher performance in lower operating voltage)

- Device demonstration on emerging technologies (such as Tunnel FET, Junctionless FET, Carbon-based FET..) is increasing, But more time is needed for implementation of these technologies in future generation devices as mature technologies.
Extreme scaling in MOSFET

Less abruptness of S/D Junction
- \( V_t \) and \( I_{ON} \) variation, - GIDL
- Punch-through of S/D

Metal Schottky S/D junctions
- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- $V_t$ and $I_{ON}$ variation
- GIDL

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET