1. Background for nano-electronics
1900 “Electronics” started.

Device: Vacuum tube

Device feature size: 10 cm

Major Appl.: Amplifier (Radio, TV, Wireless etc.)

→ Technology Revolution

1970 “Micro-Electronics” started.

Device: Si MOS integrated circuits

Device feature size: 10 µm

Major Appl.: Digital (Computer, PC, etc.)

→ Technology Revolution
2000 “Nano-Electronics” started.

Device: Still, Si CMOS integrated circuits
Device feature size: 100 nm
Major Appl.: Digital (μ-processor, cell phone, etc.)

→ Technology Revolution??
Maybe, just evolution or innovation!

But very important so many innovations!
Now, 2013 “Nano-Electronics” continued.

Device: Still, Si CMOS integrated circuits
Device feature size: near 10 nm
Major Appl.: Still Digital (μ-processor, cell phone, etc.)

Still evolution and innovation..

But, so many important emerging applications for smart society.
Questions for future

Future, “Nano-Electronics” still continued?

Device: Still, Si CMOS integrated circuits?
Device feature size: ? nm, what is the limit?

Application: New application?

→ Any Technology Revolution?
What is special or new for Nano-Electronics?

In 1990’s, people expected completely new mechanism or operational principle due the nano size, like quantum mechanical effects.

However, no fancy new operational principle was found.

At least for logic application, there is no success story for “Beyond CMOS devices” to replace Si-CMOS.

Of course, I do not deny the importance of Beyond CMOS technology development. It is becoming very important as CMOS approach its limit.
Ballistic conduction will not happen even decreasing channel length.

\[ L \gg \lambda \]

**Diffusive transport**

\[ L \sim \lambda \]

**Quasi-Ballistic transport**

\[ L < \lambda \]

**Ballistic transport**

Ballistic transport will never happen for MOSFET because of back scattering at drain

With decreasing channel length, Drain current increase continue.

Also, 1D quantum conduction, or ballistic conduction will not happen.

(1D quantum conduction: 77.8\(\mu\)S regardless of the length and material)
2. Importance of nano-electronics as integrated circuits
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power consumption
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

Al Gate

Drain

Si

Si/SiO₂ Interface is extraordinarily good
1970,71: 1st generation of LSIs

DRAM Intel 1103

MPU Intel 4004
In 2012

Most Recent SD Card

128GB (Bite)
= 128G X 8bit
= 1T(Tera)bit

1T = 10^{12} = 1 Trillion

World Population: 7 Billion
Brain Cell: 10\text{~}100 Billion
Stars in Galaxy: 100 Billion
128 GB = 1Tbit
2.4cm X 3.2cm X 0.21cm
Volume: 1.6cm³  Weight: 2g
Voltage: 2.7 - 3.6V

Old Vacuum Tube:
5cm X 5cm X 10cm, 100g, 50W
What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube:
5cm X 5cm X 10cm

Volume = (5cm X 10,000) X (5cm X 10,000) X (10cm X 10,000)
= 0.5km X 0.5km X 1km

1Tbit = 10,000 X 10,000 X 10,000 bit

Pingan Intenational Finance Center
Shanghai, China (Year 2016)

Indian Tower
Mumbai, India (Year 2016)

Burji Khalifa
Dubai, UAE (Year 2010)

500 m
Old Vacuum Tube: 100W

Nuclear Power Generator

1Tbit = 10^{12}bit

Power = 0.05kW \times 10^{12} = 50 \text{ TW}

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving
Brain: Integrated Circuits
Ear, Eye: Sensor
Mouth: RF/Opto device
Stomach: PV device
Hands, Legs: Power device
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years, even though, it is very matured market!!

2011 300B USD      2025 1,500B USD

Gartner: By K. Kim, CSTIC 2012
2. Current status of Si-CMOS device technologies
Downsizing

Important for

Decreasing cost, power

Increasing performance
Feature Size / Technology Node

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm
0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm
90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm (2012)

From 1970 to 2013 (This year)

43 years 1 generation
18 generations 2.5 years
Line width: 1/450 Line width: 1/1.43 = 0.70
Area: 1/200,000 Area: 1/2 = 0.5
Problem for downsizing

$0V < V_{dep} < 1V$

$V_{dd}$ thinning

$t_{ox}$ and $V_{dd}$ have to be decreased for better channel potential control $\rightarrow I_{OFF}$ Suppression

Region governed by gate bias

Gate metal

Gate oxide

Region governed by drain bias

Substrate

Source

Channel

Drain

Depletion Region (DL) by Drain Bias

DL touch with S Region (DL)

Large $I_{OFF}$

$0V < V_{dep} < 1V$

Large $I_{OFF}$ (Electron current)

$V_{dd}$ thinning

$24$
$L_{\text{gate}} \text{ and } t_{ox}(EOT)$ scaling trend

A. Toriumi (Tokyo Univ), IEDM 2006, Short Course
EOT = 0.40 nm
What would be the limit of downsizing!

Energy or Potential for Electron

Source

Channel

Drain

3 nm Tunneling distance

Direct-tunnel current
Subthreshold leakage current of MOSFET

Subthreshold leakage current is OK at single transistor level but not OK for billions of transistors.

Vg = 0V

Vth (Threshold Voltage)
Subthreshold leakage current will limit the downsizing

Electron Energy
Boltzmann statics
Exp (qV/kT)
The limit is different depending on application.
How far can we go for production?

**Past**
0.7 times per 2.5 years

\[10 \mu m \rightarrow 8 \mu m \rightarrow 6 \mu m \rightarrow 4 \mu m \rightarrow 3 \mu m \rightarrow 2 \mu m \rightarrow 1.2 \mu m \rightarrow 0.8 \mu m \rightarrow 0.5 \mu m \rightarrow 0.35 \mu m \rightarrow 0.25 \mu m \rightarrow 180 \text{nm} \rightarrow 130 \text{nm} \rightarrow 90 \text{nm} \rightarrow 65 \text{nm} \rightarrow 45 \text{nm} \rightarrow 32 \text{nm}\]

**Now**

**Future**

- Limit depending on applications
- Fundamental limit
- Subthreshold
- Drain bias induc
- Direct-tunnel

(28nm) \rightarrow 22nm \rightarrow 16nm \rightarrow 11.5 \text{nm} \rightarrow 8\text{nm} \rightarrow 5.5\text{nm?} \rightarrow 4\text{nm?} \rightarrow 2.9 \text{nm?} \rightarrow...

Intermediate node

- At least 4,5 generations to 8 ~ 5 nm
Extremely Thin SOI

Planar

Extremely Thin SOI

 Drain bias induced depletion
Extremely thin Si

SiO₂

Si
Suppression of subthreshold leakage by surrounding gate structure

Planar

Multi gate

Drain bias induced depletion

Si fin or nanowire

0V

0V

1V
Because of off-leakage control,

Planar $\rightarrow$ Fin $\rightarrow$ Nanowire

Leakage current

Planar FET

Fin FET

Nanowire FET

Double-Gate FinFET

Omega FinFET

Nanowire FinFET

$T_{si} = \frac{2}{3} L_2$

$T_{si} = L_2$

$T_{si} = 2L_2$
Nanowire structures in a wide meaning

- Fin
- Tri-gate
- Tri-gate (Variation)
- Ω-gate
- All-around
Our work at TIT: Ω-gate Si Nanowire

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  - 1.32 mA/µm @ $I_{OFF}=117$ nA/µm
- DIBL of 62mV/V and SS of 70mV/dec for nFET
More Moore to More More Moore

Technology node

<table>
<thead>
<tr>
<th>65nm</th>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>(L_g) 35nm</td>
<td>(L_g) 30nm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Now

Future

15nm, 11nm, 8nm, 5nm, 3nm

(Fin,Tri, Nanowire)

Planar

Tri-Gate

Si channel

Si is still main stream for future !

Si

28nm

ET: Extremely Thin

Si is still main stream for future !

Others

Alternative (III-V/Ge) Channel FinFET

Emerging Devices

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)
High-k gate dielectrics

Hf-based oxides

<table>
<thead>
<tr>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
<th>15nm, 11nm, 8nm, 5nm, 3nm,</th>
</tr>
</thead>
<tbody>
<tr>
<td>EOT:1nm</td>
<td>EOT:0.95nm</td>
<td>EOT:0.9nm</td>
<td></td>
</tr>
</tbody>
</table>

SiO$_2$ IL (Interfacial Layer) is used at Si interface to realize good mobility

Technology for direct contact of high-k and Si is necessary

EOT=0.52 nm
Remote SiO$_2$-IL scavenging HfO$_2$ (IBM)

EOT=0.9nm
HfO$_2$/SiO$_2$ (IBM)

Continued research and development

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM2009, (IBM)

Direct contact with La-silicate (Tokyo Tech.)
I\textsubscript{ON} and I\textsubscript{OFF} benchmark

**NMOS**

- Intel [a] Bulk 32nm Tri-Gate 22nm $V_{DD}=0.8\,\text{V}$
- Intel [a] $V_{DD}=0.8\,\text{V}$
- Intel [b] Bulk 45nm $V_{DD}=1\,\text{V}$
- Samsung [c] Bulk 20nm $V_{DD}=0.9\,\text{V}$
- IBM [j] ETSOI $V_{DD}=1\,\text{V}$
- IBM [g] FinFET 25nm $V_{DD}=1\,\text{V}$
- Tokyo Tech. [i] Ω-gate NW $V_{DD}=1\,\text{V}$

**PMOS**

- Intel [a] Bulk 32nm Tri-Gate 22nm $V_{DD}=0.8\,\text{V}$
- Intel [b] Bulk 45nm $V_{DD}=1\,\text{V}$
- IBM [a] $V_{DD}=1\,\text{V}$
- Samsung [c] Bulk 20nm $V_{DD}=0.9\,\text{V}$
- IBM [g] ETSOI $V_{DD}=1\,\text{V}$
- IBM [f] FinFET 25nm $V_{DD}=1\,\text{V}$
- STMicro. [h] GAA NW $V_{DD}=1.1\,\text{V}$
- IBM [j] ETSOI $V_{DD}=0.9\,\text{V}$

\[I_{ON} \text{ [mA/µm]} \quad I_{OFF} \text{ [nA/µm]}\]

References:

[a] C. Auth et al., pp.131, VLSI2012 (Intel).
[d] S. Saitoh et al., pp.11, VLSI2012 (Toshiba).
[g] A. Khakifirooz et al., pp.117, VLSI2012 (IBM).
[i] S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)
### Benchmark of device characteristics

<table>
<thead>
<tr>
<th></th>
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<th></th>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Lg (nm)</strong></td>
<td>35</td>
<td>30</td>
<td>30</td>
<td>14</td>
<td>22</td>
<td>20</td>
<td>35/25 (nFET/pFET)</td>
<td>22/30</td>
</tr>
<tr>
<td><strong>Gate Dielectrics</strong></td>
<td>Hf-based</td>
<td>Hf-based</td>
<td>SiO₂</td>
<td>HfO₂</td>
<td>HfO₂</td>
<td>Hf-based</td>
<td>HfZrO₂</td>
<td>SiO₂</td>
</tr>
<tr>
<td><strong>EOT (nm)</strong></td>
<td>1</td>
<td>0.95</td>
<td>0.9</td>
<td>3</td>
<td>~1</td>
<td>-</td>
<td>1.5</td>
<td>-</td>
</tr>
<tr>
<td><strong>Vth (V)</strong></td>
<td>~0.4</td>
<td>~0.3</td>
<td>~0.2</td>
<td>-0.15 (nFET)</td>
<td>0.3~0.4</td>
<td>~0.3</td>
<td>0.3~0.4</td>
<td>~0.5</td>
</tr>
<tr>
<td><strong>VDD (V)</strong></td>
<td>1</td>
<td>1</td>
<td>0.8</td>
<td>1</td>
<td>0.9</td>
<td>0.9</td>
<td>1</td>
<td>1.1</td>
</tr>
<tr>
<td><strong>I ON (mA/um)</strong></td>
<td>1.36/1.07</td>
<td>1.53/1.23</td>
<td>1.26/1.1</td>
<td>0.83 (nFET)</td>
<td>0.59/0.62 (I eff)</td>
<td>1.2/1.05</td>
<td>0.83/0.95</td>
<td>2.05/1.5</td>
</tr>
<tr>
<td><strong>DIBL (mV/V)</strong></td>
<td>~150</td>
<td>~200</td>
<td>46/50</td>
<td>&lt;50</td>
<td>-</td>
<td>104/115</td>
<td>65/105</td>
<td>56/9</td>
</tr>
<tr>
<td><strong>SS (mV/dec)</strong></td>
<td>-</td>
<td>~100</td>
<td>~70</td>
<td>&lt;80</td>
<td>-</td>
<td>87</td>
<td>85</td>
<td>&lt;80</td>
</tr>
</tbody>
</table>

| Lg (nm) | 35 | 30 | 30 | 22 | 20 | 35/25 (nFET/pFET) | 22/30 | 65 |
| EOT (nm) | 1 | 0.95 | 0.9 | 3 | ~1 | - | 1.5 | - | 3 |
| Vth (V) | ~0.4 | ~0.3 | ~0.2 | -0.15 (nFET) | 0.3~0.4 | ~0.3 | 0.3~0.4 | ~0.5 | -0.2 (nFET) |
| VDD (V) | 1 | 1 | 0.8 | 1 | 0.9 | 0.9 | 1 | 1.1 | 1 |
| I ON (mA/um) | 1.36/1.07 | 1.53/1.23 | 1.26/1.1 | 0.83 (nFET) | 0.59/0.62 (I eff) | 1.2/1.05 | 0.83/0.95 | 2.05/1.5 | 1.32 (nFET) |
| DIBL (mV/V) | ~150 | ~200 | 46/50 | <50 | - | 104/115 | 65/105 | 56/9 | 62 |
| SS (mV/dec) | - | ~100 | ~70 | <80 | - | 87 | 85 | <80 | 70 |
**Ω-gate Si Nanowire**

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  
  \( (1.32 \text{ mA/µm} @ I_{OFF}=117 \text{ nA/µm}) \)
- DIBL of 62mV/V and SS of 70mV/dec for nFET
Effective Electron Mobility (cm²/Vs)

Inversion Carrier Density (cm⁻²)

A₁ (12x19) \( h_{NW} \times w_{NW} \) (nm²)

A₂ (12x28)

B (20x10)

SOI Planar

\( T_{SOI} = 28 \) nm

SOI planar

\( h_{NW} : 12 \) nm

\( w_{NW} : 19 \) nm

\( h_{NW} : 20 \) nm

\( w_{NW} : 10 \) nm

\( W = 1 \) μm

\( T_{SOI} = 28 \) nm

BOX
Electron Density (x10^{19} cm^{-3})

- **Edge portion**
- **Flat portion**

Distance from SiNW Surface (nm)
Tri-gate implementation for transistors

C. Auth et al., pp.131, VLSI2012 (Intel)

<table>
<thead>
<tr>
<th></th>
<th>HP</th>
<th>MP</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{OX,E}$ (nm)</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>$L_{GATE}$ (nm)</td>
<td>30</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>$I_{OFF}$ (nA/µm)</td>
<td>20-100</td>
<td>5-20</td>
<td>1-5</td>
</tr>
</tbody>
</table>

Tri-gate has been implemented since 22nm node, enabling further scaling
Lg and EOT are larger than ITRS requirements

Implementation of Tri-gate and lower Vth/Vdd since 22nm

K. Mistry et al., pp.247, IEDM2007 (Intel).
P. Packan et al., pp.659, IEDM2009 (Intel).
C. Auth et al., pp.131, VLSI2012 (Intel).
Tri-gate width/height optimization

C. Auth et al., pp.131, VLSI2012 (Intel)

Intel’s fin is triangle shape!

PMOS channel under the gate

S/D region showing the SiGe epitaxy

A fin width of 8nm to balance SCE and $R_{ext}$

A fin height of 34nm to balance drive current vs. capacitance
**Tri-gate $I_d-V_g$ characteristics and $V_{th}$**

C.-H. Jan et al., pp.44, IEDM2012 (Intel)

- SS of 71 and 72 mV/dec for HP NMOS and PMOS, respectively
- DIBL of 30 and 35 mV/V for NMOS and PMOS, respectively
- $V_{th}$ of 22 nm is about 0.1 ~0.2 V lower than that of 32nm

Very good Vth control!
Extremely Thin SOI (ETSOI)

Also, ET-SOI works very good!

- Hybrid CMOS
  - Si Channel nFET
  - Strained SiGe Channel pFET
- RO delay improvement over FinFET with $FO = 2$

K. Cheng et al., pp. 419, IEDM2012 (IBM)
· $L_g = 25\sim35\text{nm}$ GAA NW
· Hydrogen anneal provide smooth channel surface
· Competitive with conventional CMOS technologies
· Scaling the dimensions of NW leads to suppressed SCE
3. Problems
Short-channel effect

T. Skotnicki, IEDM 2009 Short Course (STMicroelectronics)

\[
SCE = 0.64 \frac{\varepsilon_s}{\varepsilon_{ox}} \times EI \times \Phi_d
\]

\[
DIBL = 0.8 \frac{\varepsilon_s}{\varepsilon_{ox}} \times EI \times V_{ds}
\]

\[
EI = 1 \times \left(1 + \frac{X_j^2}{L_{el}^2} \right) \times \frac{T_{ox}}{L_{el}} \times T_{dep}
\]

\[
EI = 1 \times \left(1 + \frac{T_{si}^2}{L_{el}^2} \right) \times \frac{T_{ox}}{L_{el}} \times \frac{T_{si} + \lambda T_{box}}{L_{el}}
\]

\[
EI = 1 \times \left(1 + \frac{T_{si}^2}{L_{el}^2} \right) \times \frac{T_{ox}}{L_{el}} \times \frac{T_{si} + \lambda T_{box}}{L_{el}}
\]

\[
EI = 1 \times \left(1 + \frac{T_{si}^2}{L_{el}^2} \right) \times \frac{T_{ox}}{L_{el}} \times \frac{T_{si} / 4}{L_{el}}
\]

if max ch. doping is $10^{16}$ cm$^{-3}$, $T_{ep} \approx 12$ nm

if max ch. doping is $10^{20}$ cm$^{-3}$, $T_{ep} \approx 12$ nm

$T_{box} = 145$ nm

$\lambda T_{box} = 18$ nm

If $T_{si}$ min $= 3$ nm then:

$T_{box} = 10$ nm

$\lambda T_{box} = 3$ nm

Approximately $0$ nm

If $T_{si}$ min $= 3$ nm then:

$T_{box} = 10$ nm

$\lambda T_{box} = 0.46$ nm

$T_{si}$/2 plays role of $X_j$, and that of $T_{dep}$, if minimum feasible $T_{si}$ is supposed $3$ nm, then:

$L_{el,min}$ (DIBL=100mV/V)

$= 34$ nm

$L_{el,min}$ (DIBL=100mV/V)

$= 34$ nm

$L_{el,min}$ (DIBL=100mV/V)

$\approx 30$ nm

$L_{el,min}$ (DIBL=100mV/V)

$\approx 10$ nm

$L_{el,min}$ (DIBL=100mV/V)

$\approx 6$ nm

$L_{el,min}$ (DIBL=100mV/V)

$\approx 2.7$ nm
Drain-induced barrier lowering

\[ DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} T_{dep} V_{DS} \]

**BULK**

- \( T_{dep} = \frac{3}{4} L_{el} \)
- \( X_j = \frac{3}{4} L_{el} \)
- 140 mV/V

**III-V**

- \( T_{ox} + 2A \)
- \( \varepsilon_{Si} + 15\% \)
- 210 mV/V

**FDSOI**

- \( T_{dep} = T_{si} + \lambda T_{box} \)
- \( X_j = T_{si} \geq 6 \text{nm} \)
- 110 mV/V

**ETSOI**

- 80 mV/V

**UTBB**

- 70 mV/V

**FinFET**

- \( T_{dep} = \frac{T_{si}}{2} \)
- \( X_j = \frac{T_{si}}{2} \)
- \( T_{si} \geq 10 \text{nm} \)

T. Skotnicki, IEDM 2010 Short Course (STMicroelectronics)
Sub-threshold Slope

\[ S = \frac{kT}{q} \ln \left( 1 + \frac{C_{\text{dep}}}{C_{\text{ox}}} \frac{\varepsilon_{\text{Si}}}{\varepsilon_{\text{ox}}} \frac{T_{\text{ox}}}{L_{\text{el}}} \frac{X_j}{L_{\text{el}}} \left( 1 + \frac{3 T_{\text{dep}}}{4 L_{\text{el}}} \right) \right) \]

- 110 mV/dec
- 85 mV/dec
- 75 mV/dec
- 65 mV/dec
- 95 mV/dec

**BULK**
- \( T_{\text{dep}} = 3/4 L_{\text{el}} \)
- \( X_j = 3/4 L_{\text{el}} \)

**III-V**

**FDSOI**
- \( T_{\text{dep}} = T_{\text{si}} \)
- \( X_j = T_{\text{si}} \)

**FinFET**
- \( T_{\text{dep}} = T_{\text{si}} / 2 \)
- \( X_j = T_{\text{si}} / 2 \)

**ETSOI**

**UTBB**

**RBB \Rightarrow Pstat**
Problems in Multi-gate

S. Bangsaruntip et al., pp.297, IEDM2009 (IBM),
K. Tachi et al., pp.313, IEDM2009 (CEA-LETI)

Need to decrease diameter for SCH

Significant $\mu$ degradation at diameter < 10 nm

Decreasing the diameter of NW

Improved short-channel control

Severe mobility degradation
Impact of Si thickness in FinFET

- Replacement Gate process
- TaN/HfO$_2$ gate stack
- Reduced $g_m$ and higher $V_{th}$ with decreasing Fin width
Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

< 10 nm

1. Mobility degradation

Extremely small distance between the electron and all around Si surface.

Strong scattering of electrons by interaction with all around Si surface.

2. Electron density decrease

Decrease of DOS in extremely narrow wire.

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-k is necessary.
Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Wire cross section dependence.
What cross section gives best solution for SCE suppression and drive current?
Significant increase in $V_{th}$ variability with decreasing Fin width
Smaller wire/fin width is necessary for SCE suppression

But mobility and $I_{ON}$ severely degrade with wire/fin width reduction

Therefore even in multi-gate structures, **EOT scaling should be accelerated** to provide SCE immunity
High-k beyond 0.5 nm
Gate oxide should be thicker than mono atomic layer

0.8 nm gate oxide thickness MOSFETs operate

0.8 nm $\rightarrow$ Distance of 3 Si atoms $\rightarrow$ 2 mono layers

R. Chau, et al., (Intel) IWGI 2003
Gate Leakage Power Density becomes significantly large with $L_g$ reduction, and thus, with $t_{ox}$ thinning!!
To use high-k dielectrics

K: Dielectric Constant

Thin SiO₂

K=4

Almost the same electric characteristics

Thick high-k dielectrics

K=20

5 times thicker

Small leakage Current

However, very difficult and big challenge!
Equivalent Oxide Thickness (EOT)

Combination of high-k and metal gate is important

K. Natori, et al., (Tsukuba Univ) SSDM 2005, p.286

Combination of high-k and metal gate is important

- **Poly-Si(10²⁰ cm⁻³)**
  - Depletion
  - (EOT: 0.3 nm)
  - Metal
  - High-k
  - Metal (EOT: 0.1 nm)

**Equivalent Oxide Thickness (EOT):** gate dielectrics itself, $C_{OX}$

**Capacitance Equivalent Thickness (CET):** entire gate stack,

- **Metal gate can eliminate the poly-Si depletion.**

  \[
  \text{Inversion CET} = T_{inv} \approx EOT + 0.4\text{nm}
  \]

with metal gate electrode

$C_{metal}$ is finite because of quantum effect. In other words, electron is not a point charge located at the interface but distributed charge.
Choice of High-k elements for oxide

Candidates

Unstable at Si interface

1. Si + MO<sub>x</sub> M + SiO<sub>2</sub>
2. Si + MO<sub>x</sub> MSi<sub>x</sub> + SiO<sub>2</sub>
3. Si + MO<sub>x</sub> M + MSi<sub>x</sub>O<sub>y</sub>

Gas or liquid at 1000 K

Radio active

Gas or liquid at 1000 K


HfO<sub>2</sub> based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La<sub>2</sub>O<sub>3</sub> based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Flat metal/high-k interface for better mobility
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Interface dipole control for $V_{th}$ tuning
- Suppression of FLP
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
- Reliability: PBTI, NBTI, TDDB
- Suppression of metal diffusion
- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Interface dipole control for $V_{th}$ tuning
- Suppression of FLP
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
- Reliability: PBTI, NBTI, TDDB
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band discontinuity [eV]

Si Band Gap

Dielectric Constant $\varepsilon(0)$

XPS measurement by Prof. T. Hattori, INFOS 2003
Direct high-k/Si by silicate reaction

HfO$_2$ case

La$_2$O$_3$ case

Our approach

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface
Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
Direct high-k/Si by silicate reaction

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface. Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ → HfO$_2$ + Si + 2O* → HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode
D.J. Lichtenwalner, Tans. ECS 11, 319

SiO$_x$-IL is formed after annealing
Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ can achieve direct contact of high-k/Si

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.
Cluster tool for HKMG Stack

- EB Deposition for HK
- Flash Lamp
- Sputter for MG
- Robot
- ALD
- RTA
- Entrance

5m
Cluster Chambers for HKMG Gate Stack

EB Deposition: HK
Sputter: MG
Flash Lamp Anneal
ALD: HK
Robot
RTA
Entrance
Deposited thin film

Substrate

Moving Mask

Electron Beam

Source

Flux
L = 0.5~100 µm (8 kinds)
W = 10, 20, 50, 100 µm (4 kinds)

26 chips

1 cm × 1 cm
Gate Leakage vs EOT, (Vg=|1|V)

- Al2O3
- HfAlO(N)
- HfO2
- HfSiO(N)
- HfTaO
- La2O3
- Nd2O3
- Pr2O3
- PrSiO
- PrTiO
- SiON/SiN
- Sm2O3
- SrTiO3
- Ta2O5
- TiO2
- ZrO2(N)
- ZrSiO
- ZrAlO(N)
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small Dit

① silicate-reaction-formed fresh interface

② stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress


No interfacial layer can be confirmed with Si/TiN/W
La$_2$O$_3$/silicate/$n$-Si CV

![Graph showing capacitance density vs. gate voltage for W/La$_2$O$_3$(4nm)/$n$-Si 600°C, 30min.]

- Capacitance density (µF/cm$^2$)
- Gate voltage (V)
- 1kHz and 1MHz markers
- $\Delta V_{fb}$ and $C_{fb}$ annotations
It is important to change the La2O3 to La-silicate completely.
Annealing temperature (°C)

EOT (nm)

Annealed for 2 s
La₂O₃(3.5 nm)

W(60 nm)

TiN/W(6 nm)

As depo

EOT=0.55 nm

TaN/(45nm)/W(3nm)

900°C, 30min

EOT=0.55nm
Flat-band voltage (V)

EOT (nm)

TaN(45nm)/W(3nm)

900°C, 30min

Fixed Charge density: $1 \times 10^{11}$ cm$^{-2}$

$Q_{fix} = 1 \times 10^{11}$ cm$^{-2}$
EOT = 0.53nm

Drain Current (μA)

Drain Voltage (V)

Electron Mobility [cm²/Vsec]

Vg = 0.2V
Vg = 0.4V
Vg = 0.6V
Vg = 0.8V
Vg = 1.0V

L/W = 20/20μm
T = 300K
Nsub = 3 x 10¹⁶cm⁻³

Eeff = 1MV/cm

151cm²/Vs

150cm²/Vs
Gate current (A/cm²) vs. Gate voltage (V) for a TaN/W/LaSiOₓ/nFET with Wᵍ/Lᵍ = 20/20 µm and EOT = 0.55 nm. The graph shows a comparison with ITRS standards, scaled by x1/100.
**Benchmark of La-silicate dielectrics**

**Gate Leakage current**

- ITRS requirement
- Our data: La-silicate gate oxide

**Effective Mobility**

- Solid circle: Our data
- Open square: Hf-based oxides


*T. Ando, et al., (IBM) IEDM 2009, p.423*
# Si benchmark (nMOSFET)

<table>
<thead>
<tr>
<th>Gate stack</th>
<th>EOT</th>
<th>Mobility</th>
<th>V&lt;sub&gt;th&lt;/sub&gt;</th>
<th>SS</th>
<th>DIBL</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN/Cap/HfO&lt;sub&gt;2&lt;/sub&gt;</td>
<td>0.52nm</td>
<td>110cm&lt;sup&gt;2&lt;/sup&gt;/Vs (at 1x10&lt;sup&gt;13&lt;/sup&gt;cm&lt;sup&gt;-2&lt;/sup&gt;)</td>
<td>~0.4V (L&lt;sub&gt;g&lt;/sub&gt;=24nm)</td>
<td>90mV/dec</td>
<td>147mV/V</td>
<td>IBM VLSI2011</td>
</tr>
<tr>
<td>TiN/Cap/HfO&lt;sub&gt;2&lt;/sub&gt;</td>
<td>0.55nm</td>
<td>140cm&lt;sup&gt;2&lt;/sup&gt;/Vs (at 1MV/cm)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IBM VLSI2009</td>
</tr>
<tr>
<td>TiN/Cap/HfO&lt;sub&gt;2&lt;/sub&gt;</td>
<td>0.45nm</td>
<td>115cm&lt;sup&gt;2&lt;/sup&gt;/Vs (at 1x10&lt;sup&gt;13&lt;/sup&gt;cm&lt;sup&gt;-2&lt;/sup&gt;)</td>
<td>0.3V (L&lt;sub&gt;g&lt;/sub&gt;=10um)</td>
<td>—</td>
<td>—</td>
<td>IMEC MEE2011</td>
</tr>
<tr>
<td>Metal/HfO&lt;sub&gt;2&lt;/sub&gt;</td>
<td>0.59nm</td>
<td>130cm&lt;sup&gt;2&lt;/sup&gt;/Vs (at 1MV/cm)</td>
<td>0.45V (L&lt;sub&gt;g&lt;/sub&gt;=1um)</td>
<td>75mV/dec</td>
<td>—</td>
<td>Sematech VLSI2009</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.65nm</td>
<td>—</td>
<td>0.3~0.4V (L&lt;sub&gt;g&lt;/sub&gt;=~30nm)</td>
<td>90mV/dec</td>
<td>100mV/V</td>
<td>Samsung VLSI2011</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.95nm</td>
<td>—</td>
<td>~0.3V (L&lt;sub&gt;g&lt;/sub&gt;=30nm)</td>
<td>100mV/dec</td>
<td>~200mV/V</td>
<td>Intel IEDM2009</td>
</tr>
<tr>
<td>W/La-silicate 93</td>
<td>0.62nm</td>
<td>155cm&lt;sup&gt;2&lt;/sup&gt;/Vs (at 1MV/cm)</td>
<td>~0.08V (L&lt;sub&gt;g&lt;/sub&gt;=10um)</td>
<td>~70mV/dec</td>
<td>—</td>
<td>Tokyo Tech. T-ED2012</td>
</tr>
</tbody>
</table>
ALD of La2O3


Precursor (ligand)

La(iPrCp)3

La(FAMD)3

ALD is indispensable from the manufacturing viewpoint
- precise control of film thickness and good uniformity
**Advantages of metal S/D**
- atomically abrupt junction
- low parasitic resistance
- reduced channel dopant concentration

**Issues in metal S/D**
- two different $\phi_B$ for $p/n$-ch FETs
- underlap/overlap to the gate
- narrow process temperature window

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S.-H. Kim, IEDM (2010) 596

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Ni is used both on InGaAs and Ge to form alloy.

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K. Ikeda, VLSI (2012) 165

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Metal S/D is considered for alternative channel material such as InGaAs and Ge

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L. Hutin, pp.45, IEDM2009 (CEA-LETI)
4. Alternative channel devices
### Ge, III-V Bulk Properties

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Electron Mobility (cm²/Vs)</strong></td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
</tr>
<tr>
<td><strong>Electron Effective Mass (mₑ/m₀)</strong></td>
<td>(m_t: 0.19) (m_l: 0.916)</td>
<td>(m_t: 0.082) (m_l: 1.467)</td>
<td>0.067</td>
<td>0.08</td>
<td>0.026</td>
<td>0.0135</td>
</tr>
<tr>
<td><strong>Hole Mobility (cm²/Vs)</strong></td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td><strong>Hole Effective Mass (mₓ/m₀)</strong></td>
<td>(m_{HH}: 0.49) (m_{LH}: 0.16)</td>
<td>(m_{HH}: 0.28) (m_{LH}: 0.044)</td>
<td>(m_{HH}: 0.45) (m_{LH}: 0.082)</td>
<td>(m_{HH}: 0.45) (m_{LH}: 0.12)</td>
<td>(m_{HH}: 0.57) (m_{LH}: 0.35)</td>
<td>(m_{HH}: 0.44) (m_{LH}: 0.016)</td>
</tr>
<tr>
<td><strong>Band Gap (eV)</strong></td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.14</td>
</tr>
<tr>
<td><strong>Permittivity</strong></td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

- Ge ⇒ lightest hole \(m^*\) (light electron \(m^*\)) ⇒ pMOS (CMOS)
- III-V ⇒ light electron \(m^*\) ⇒ nMOS
- GaAs·InP ⇒ \(E_g\) higher than that in Si ⇒ low power

*S. Takagi., IEDM2011, Short course (Tokyo Uni)*
InGaAs GAA
$L_{ch}=50\text{ nm}, \text{Dielectric: } 10\text{ nm } Al_{2}O_{3}$
$V_{DS}=0.5\text{V (Purdue Uni.)}[a]$

InGaAs FinFET
$L_{ch}=130\text{ nm}$
$EOT 3.8\text{nm}$
$V_{DS}=0.5\text{V (NUS)}[c]$

InGaAs Nanowire
$L_g=200\text{nm, } T_{ox} 14.8\text{nm}$
$V_{DS}=0.5\text{V (Hokkaido Uni.)}[d]$

Si-FinFET 32nm
$\text{Intel } V_{DD}=0.8\text{V [10]}$

InGaAs Tri-gate
$L_{g}=60\text{ nm}, \text{EOT 12A}$
$V_{DS}=0.5\text{V (Intel) [b]}$

Si-FinFET 22nm
$\text{Intel } V_{DD}=0.8\text{V [j]}$

Si-bulk 45nm
$\text{Intel } V_{DD}=1\text{V [k]}$

Metal S/D InGaAs-OI
$L_{ch}=55\text{nm, EOT 3.5nm}$
$V_{DS}=0.5\text{V (Tokyo Uni.)}[e]$

Si-FinFET 32nm
$\text{Intel } V_{DD}=0.8\text{V [j]}$

Ge FinFET
$L_{g}=4.5\text{ mm,}$
$\text{Dielectric: SiON, } V_{DS}=-1\text{V (Stanford Uni.)}[g]$

Ge GAA
$L_{g}=300\text{mm,}$
$\text{dielectric: } GeO_{2}(7\text{nm})-HfO_{2}(10\text{nm})$
$V_{DS}=-0.8\text{V (ASTAR Singapore)[h]}$

Si-FinFET 22nm
$\text{Intel } V_{DD}=0.8\text{V [j]}$

Si-bulk 45nm
$\text{Intel } V_{DD}=1\text{V}$

Ge Tri-gate
$L_{g}=183\text{nm, } EOT 5.5\text{nm}$
$V_{DS}=-1\text{V (NNDL Taiwan)[i]}$

Si-FinFET 22nm
$\text{Intel } V_{DD}=0.8\text{V [j]}$

Si-bulk 45nm
$\text{Intel } V_{DD}=1\text{V}$

[h] J. Peng et al., pp.931, IEDM2009 (ASTAR Singapore)
[i] S. Hsu et al., pp.825, IEDM2011 (NNDL Taiwan)
[j] C. Auth et al., pp.131, VLSI2012 (Intel)
[k] K. Mistry et al., pp.247, IEDM2007 (Intel)
In this slide, we see a graph comparing the On-Current ($I_{ON}$) to the Off-Current ($I_{OFF}$) benchmark for Ge pMOSFETs. The graph includes data from various research papers from 2005 to 2009, as indicated by the labels on the graph. The optimization of short channel Ge p-MOSFETs is still under investigation.
## III-V/Ge benchmark for various structures

<table>
<thead>
<tr>
<th>Planar (metal S/D, Strain, Buffer...)</th>
<th>FinFET</th>
<th>Tri-gate</th>
<th>Gate-all-around MOSFET</th>
<th>Nanowire</th>
</tr>
</thead>
<tbody>
<tr>
<td>material</td>
<td>InGaAs</td>
<td>Ge</td>
<td>InGaSn</td>
<td>InGaAs</td>
</tr>
<tr>
<td>Dielectric /EOT</td>
<td>Al₂O₃/3.5 nm</td>
<td>7.6 Å/HfO₂⁺/Al₂O₃+GeO₂</td>
<td>5nm ALD Al₂O₃</td>
<td>5nm ALD Al₂O₃</td>
</tr>
<tr>
<td>Mobility</td>
<td>-</td>
<td>~600 (cm²/Vs)</td>
<td>N₆⁺: 5e12 e⁻: 200 h⁻:400 (μS/μm)</td>
<td>~700 (μS/μm)</td>
</tr>
<tr>
<td>L₉ (nm)</td>
<td>55</td>
<td>W/L=30/5 μm</td>
<td>50 μm</td>
<td>100</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>84</td>
<td>-</td>
<td>180</td>
<td>-</td>
</tr>
<tr>
<td>SS (mV/dec)</td>
<td>105</td>
<td>-</td>
<td>150K 61pMOS 33nMOS 120K</td>
<td>145</td>
</tr>
<tr>
<td>Iₙ (µA/µm) (V₀=0.5V)</td>
<td>278</td>
<td>3</td>
<td>4 (n,p)</td>
<td>-</td>
</tr>
</tbody>
</table>
InGaSb as channel material (stanford)

Z. Yuan et al., pp.185, VLSI2012 (Stanford Uni)

**Achieving both N- and P-type MOSFET on a single channel is possible**

**In-content of 20-40% improves performance**

**electron/hole mobility > 4000/900 cm²/Vs** was gained in a single channel material

$I_{ON}$ at $L_G = 50 \, \mu$m

- $\mu_{pMOS}: 4 \, \mu A/\mu m$
- $\mu_{nMOS}: 3.8 \, \mu A/\mu m$

**AlGaSb creates barrier for both electrons and holes**
Metal S/D and InAs buffer layer are used as performance boosters.

- **DIBL=84 mV/V** and **SS=105 mV/V** was shown for $L_{ch} = 55$ nm when In-content was higher.

_S. H. Kim et al., pp.177, VLSI2012 (Tokyo Uni)_
Common InGaAs-GeSn gate stack (NUS)

- Common gate stack (gate metal and dielectric) were used for both p- and n-type.
- Si$_2$H$_6$ plasma passivation is employed which creates Si layer at interface.

\[
\text{SS: nMOS: 90 (mV/decade)} \\
\text{pMOS: 190 (mV/decade)}
\]

- High intrinsic peak $G_{M,\text{Sat}}$ of ~465 $\mu$S/\mu m at $V_{DS}$=-1.1 V was achieved for $L_G=250$ nm.

\[
V_{GS}-V_{TH} = 0 \sim 2.0 \text{V} \\
L_G = 5 \mu \text{m}
\]
Core-multishell InGaAs nanowires grown without buffer layer on Si substrate (bottom up approach)

At $V_d = 1$ V peak transconductance of 500 mS/mm is achieved (roughly x3 InGaAs nanowire)
Tri-gate InGaAs QW-FET (Intel)


- Tri-gate structure has superiority electrostatic controllability compared to ultra-thin body planar structure
- Steepest SS and smallest DIBL ever reported ($W_{\text{fin}} = 30\text{nm}$)
Inversion mode $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFET with ALD $\text{Al}_2\text{O}_3$/WN with well electrostatic properties

DIBL was suppressed down to $L_{\text{ch}} = 50\text{nm}$ and $G_{m,\text{max}} = 701\text{mS/mm}$ at $V_{\text{ds}} = 1\text{V}$
DIBL = 135 mV/V and drive current over 840 µA/µm at $L_{ch} = 130$nm and $V_{ds} = 1.5$V was achieved.
Ge-nanowire pMOSFET (AIST, Tsukuba)


Using Ni-Ge alloy as metal S/D
Significantly reduces contact resistance

High saturation current and high mobility

\[ \mu_{\text{eff}} = 855 \text{ cm}^2/\text{Vs} \text{ at } N_s = 5 \times 10^{12} \text{cm}^{-2} \]
and saturation drain current of

\[ 731 \mu A/ \mu \text{m} \text{ at } V_d = -1V \]
Selective etching of high defect Ge near Ge/Si interface is used which improves gate controllability.

- $I_{ON}/I_{OFF} = 10^5$ and SS = 130 mV/dec
- And $I_{ON} = 235 \mu m/\mu m$ at $V_D = -1V$
Implementing high-k material to III-V, Ge

**III-V (InGaAs, InAs, InGaSb, …)**
- ALD-Al$_2$O$_3$ is most commonly used as gate dielectric in planar or Multi-gate
- HfO$_2$-only stacks have high $D_{it}$ (combination of Al$_2$O$_3$ or Al or Si is used)

![Graph and images showing capacitance vs gate bias for different materials]

**Ge**
- By controlling the formation of GeO$_x$ at the interface, HfO$_2$ and Al$_2$O$_3$ show good results.

![Graph showing capacitance vs voltage for different materials with EOT=0.76 nm]
5. Emerging devices
Emerging devices (future scaling trends)

**Carbon-based FET**

- Carbon nanotube
- Graphene

**GaAs mHEMT**

- CNT
- Graphene

**SiMOSFET**

- (20nm)

**GaAs pHEMT**

- (100nm)

**Junctionless Transistor**

**All-spin logic device**

Input and output related via Spin-coherent channel

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J. P. Colinge et al., Nature Nano. 5(2010)225

A. D. Franklin et al., pp.525, IEDM2011 (IBM)

J. P. Colinge et al., Nature Nano. 5(2010)266

Tunnel FET

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

Low $I_{OFF}$, Low $V_{DD}$, SS<60mV/decade
TFET vs. MOSFET at low $V_{DD}$

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

$EOT = 1\ \text{nm}$

$LG = 20\ \text{nm}$

$tInAs = 5\ \text{nm}$

<table>
<thead>
<tr>
<th>TFET @0.35V</th>
<th>Stage Delay (ps)</th>
<th>Switching Energy (fJ)</th>
<th>Leakage Power (nW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV (FO=3)</td>
<td>105</td>
<td>0.26</td>
<td>0.37</td>
</tr>
<tr>
<td>NAND (FO=3)</td>
<td>149</td>
<td>0.32</td>
<td>0.57</td>
</tr>
<tr>
<td>NOR (FO=3)</td>
<td>158</td>
<td>0.34</td>
<td>0.54</td>
</tr>
<tr>
<td>Combined</td>
<td>129</td>
<td>0.29</td>
<td>0.46</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CMOS @0.3V</th>
<th>Stage Delay (ps)</th>
<th>Switching Energy (fJ)</th>
<th>Leakage Power (nW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV (FO=3)</td>
<td>830</td>
<td>0.25</td>
<td>0.37</td>
</tr>
<tr>
<td>NAND (FO=3)</td>
<td>1364</td>
<td>0.32</td>
<td>0.56</td>
</tr>
<tr>
<td>NOR (FO=3)</td>
<td>1389</td>
<td>0.33</td>
<td>0.53</td>
</tr>
<tr>
<td>Combined</td>
<td>1103</td>
<td>0.29</td>
<td>0.46</td>
</tr>
</tbody>
</table>

$V_{DD} 0.3\sim0.35V$

TFET 8x faster at the same power

“parameter variation is not a significant factor for differentiation between MOSFET and TFET”
X in Si$_{1-x}$Ge$_x$ is optimized to allow for efficient BTBT

$L_G = 200$nm

$I_{ON}/I_{OFF} \approx 10^5$

Reducing SiGe Body thickness improves Subthreshold swing.

130mV/dec

190mV/dec
SS of TFET is function of $V_G$ due to Zener tunnel current

- Minimum SS= 21 mV/dec is reached due to optimized series resistance of contact, undoped InAs and InAs/Si

- $I_{ON}/I_{OFF} \sim 10^6$ at $V_{DS} = 1.0V$ ($I_{ON} = 1A/\mu m$)
Device structure

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

Device structure

- p+ AlGaSb 40 nm
- p+ GaSb 30 nm
- Al2O3 6 nm
- n+ InAs 30 nm
- Au
- Ti

AIAs/AlSb SL buffer on GaSb

tunneling // to the gate oblique to the gate field

tunneling ⊥ to the gate in-line with the gate field

nanowire TFET
gate-all-around - best electrostatics

K. Tomioka et al., pp.47, VLSI2012 (Hokkaido University)
## Tunnel FET performance comparison

**measured III-V channel TFETs**

<table>
<thead>
<tr>
<th>Reference</th>
<th>Source</th>
<th>Channel</th>
<th>Dielectric</th>
<th>EOT (nm)</th>
<th>$I_{ON}$ (μA/μm)</th>
<th>$V_{DS}$ (V)</th>
<th>$V_{GS} = V_{ON}$</th>
<th>$V_{ON} - V_{OFF}$</th>
<th>$I_{ON}/I_{OFF}$</th>
<th>$S_{MIN}$ (mV/dec)</th>
<th>$S_{EFF}$ (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>this work</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.6</td>
<td>78</td>
<td>0.5</td>
<td>0.5</td>
<td>1.5</td>
<td>2,000</td>
<td>125</td>
<td>1,230</td>
</tr>
<tr>
<td>Li [4]</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$</td>
<td>3.9</td>
<td>20</td>
<td>0.3</td>
<td>2</td>
<td>6</td>
<td>210</td>
<td>830</td>
<td>1,300</td>
</tr>
<tr>
<td>Moukerjea [5]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>5.6</td>
<td>10</td>
<td>0.5</td>
<td>2.5</td>
<td>2.5</td>
<td>10,000</td>
<td>240</td>
<td>310</td>
</tr>
<tr>
<td>Mohata [6]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>2.8</td>
<td>10</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>400,000</td>
<td>200</td>
<td>180</td>
</tr>
<tr>
<td>Zhao [7]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>20</td>
<td>0.45</td>
<td>1</td>
<td>1.5</td>
<td>30,000</td>
<td>86</td>
<td>170</td>
</tr>
<tr>
<td>Zhao [8]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>40</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>200,000</td>
<td>84</td>
<td>190</td>
</tr>
<tr>
<td>Ford [9]</td>
<td>InAs</td>
<td>InAs</td>
<td>ZrO$_2$</td>
<td>2</td>
<td>0.4</td>
<td>0.5</td>
<td>1</td>
<td>1</td>
<td>200</td>
<td>190</td>
<td>220</td>
</tr>
<tr>
<td>Zhou [10]</td>
<td>InP</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.3</td>
<td>20</td>
<td>0.5</td>
<td>1</td>
<td>1.75</td>
<td>450,000</td>
<td>93</td>
<td>150</td>
</tr>
</tbody>
</table>

- **$S_{MIN}$**: Most common SS which is the inverse of $I_D$-$V_{GS}$ slope at the steepest part
- **$S_{EFF}$**: Is the average swing when $V_{TH} = V_{DD}/2$, $V_{OFF} = 0$

**Average SS**: $\frac{V_{TH} - V_{OFF}}{\log(I_D/I_{OFF})}$

**Effective SS**: $\frac{V_{DD}}{2\log(I_D/I_{OFF})}$
I\textsubscript{ON} and I\textsubscript{OFF} of TFETs

[1] G. Zhou et al., pp. 782, vol. 33, no. 6, EDL 2012 (University of Notre Dame)

C. Auth et al., pp.131, VLSI2012 (Intel).

K. Mistry et al., pp.247, IEDM2007 (Intel).
MEMS relay

- Frequency of 1, 5, 25kHz under operation
- $I_{ON}/I_{OFF}$ of $\sim 10^{10}$
- Ultra-low-power digital logic applications.

T. K. Liu et al., pp. 43, VLSI2012 (UC Berkeley)
Conventional Inversion Mode

**JAM LD**: Junctionless Accumulation Mode with low dope

**JAM HD**: Junctionless Accumulation Mode with high dope

JAM devices have **reduced gate control** and **degraded short-channel** characteristics relative to IM.

Not suitable for high-performance logic (high $I_{on}$ and moderate $I_{off}$)
Near-ideal subthreshold slope, close to 60 mV/dec at room temperature, and extremely low leakage currents $I_{ON}/I_{OFF} \approx 1 \times 10^6 \quad (-1 < V_g < 1)$

$I_{OFF}$ is smaller than $10^{-15}$ A

- Silicon nanowire is uniformly doped
- Gate material is opposite polarity polysilicon

$\text{Lg} = 1 \mu\text{m} \quad W_{wire} = 30\text{nm}$
Carbon materials for FET applications
- an ultra-thin body for aggressive channel length scaling
- excellent intrinsic transport properties similar to carbon nanotubes
- pattern the desired device structures
Transistor operation with $L_{ch}$ of 9nm
• Ambipolar Characteristics

• Bi-layer graphene and double gates can open the gap
2D material: single layer MoS$_2$

- Mobility of 190 cm$^2$/V·sec
- $I_{on}$ of 1 μA/μm at $V_{DD} = 1$V

Candidate: MoS$_2$, MoSe$_2$, WS$_2$, WSe$_2$, MoTe$_2$, WTe$_2$
Spin transfer Torque Switching MOSFET

Magnetic tunnel junction on S/D

Read/write are enabled by using ferromagnetic electrodes and Spin-polarized current
## Summary of Emerging Technology pro/cons

<table>
<thead>
<tr>
<th>Technology</th>
<th>Advantage</th>
<th>Issues</th>
</tr>
</thead>
<tbody>
<tr>
<td>TFET</td>
<td>Lower $V_{dd}$</td>
<td>Integration higher $I_{ON}$</td>
</tr>
<tr>
<td></td>
<td>Lower $I_{OFF}$</td>
<td></td>
</tr>
<tr>
<td>CNT FET</td>
<td>Higher transport velocity</td>
<td>High density and alignment, reproducibility, integration</td>
</tr>
<tr>
<td></td>
<td>$L_g$ scaling</td>
<td></td>
</tr>
<tr>
<td>Graphene FET</td>
<td>RF application</td>
<td>NOT a direct replacement for Silicon logic</td>
</tr>
<tr>
<td></td>
<td>Large area manufacturing</td>
<td></td>
</tr>
<tr>
<td>MEMS</td>
<td>Extremely low leakage</td>
<td>Endurance</td>
</tr>
<tr>
<td></td>
<td>Ultra-low digital logic</td>
<td>Slow speed, scalability</td>
</tr>
<tr>
<td>Junctionless FET</td>
<td>CMOS process compatibility</td>
<td>Worse gate control in short-channel</td>
</tr>
<tr>
<td>Spin FET</td>
<td>Low power, suitable for memory (nonvolatile info storage)</td>
<td>Low efficiency of spin injection</td>
</tr>
</tbody>
</table>
Conclusions
Conclusions

- New device structures (FinFET, Tri-gate) are replacing conventional Planar CMOS
  - Same performance at lower supply voltage

- HKMG: Continuous innovation has enabled EOT scaling to 9 \( A^0 \), however, new material could be needed for further EOT scaling.
  - La-based high-k material

- Recent advances in new channel material shows promising device performances but still far to catch up Si-CMOS.
  - The combination of III-V channel materials with a multi-gate structure appears to be a promising direction.
    (Higher performance in lower operating voltage)

- Device demonstration on emerging technologies (such as Tunnel FET, Junctionless FET, Carbon-based FET..) is increasing, But more time is needed for implementation of these technologies in future generation devices as mature technologies.
### Extreme scaling in MOSFET

Less abruptness of S/D Junction
- $V_t$ and $I_{ON}$ variation, - GIDL
- Punch-through of S/D

### Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- \( V_t \) and \( I_{ON} \) variation
- GIDL

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET