Future of Nano CMOS Technology

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Tokyo Institute of Technology
1. Background for nano-electronics
1900 “Electronics” started.

Device: Vacuum tube
Device feature size: 10 cm
Major Appl.: Amplifier (Radio, TV, Wireless etc.)

→ Technology Revolution

1970 “Micro-Electronics” started.

Device: Si MOS integrated circuits
Device feature size: 10 µm
Major Appl.: Digital (Computer, PC, etc.)

→ Technology Revolution
2000 “Nano-Electronics” started.

Device: Still, Si CMOS integrated circuits
Device feature size: 100 nm
Major Appl.: Digital (µ-processor, cell phone, etc.)

→ Technology Revolution??

Maybe, just evolution or innovation!

But very important so many innovations!
Now, 2013 “Nano-Electronics” continued.

Device: Still, Si CMOS integrated circuits
Device feature size: near 10 nm
Major Appl.: Still Digital (μ-processor, cell phone, etc.)

Still evolution and innovation..

But, so many important emerging applications for smart society.
Questions for future

Future, “Nano-Electronics” still continued?

Device: Still, Si CMOS integrated circuits?

Device feature size: ? nm, what is the limit?

Application: New application?

→ Any Technology Revolution?
What is special or new for Nano-Electronics?

In 1990’s, people expected completely new mechanism or operational principle due the nano size, like quantum mechanical effects.

However, no fancy new operational principle was found.

At least for logic application, there is no success story for “Beyond CMOS devices” to replace Si-CMOS.

Of course, I do not deny the importance of Beyond CMOS technology development. It is becoming very important as CMOS approach its limit.
Ballistic conduction will not happen even decreasing channel length.

Ballistic transport will never happen for MOSFET because of back scattering at drain

With decreasing channel length, Drain current increase continue.

Also, 1D quantum conduction, or ballistic conduction will not happen.

(1D quantum conduction: 77.8μS regardless of the length and material).
2. Importance of nano-electronics as integrated circuits
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si

Source

Al Gate

Drain

Si

Si/\text{SiO}_2\text{ Interface is extraordinarily good}

Al

\text{SiO}_2

\text{Si}
1970, 71: 1st generation of LSIs

DRAM  Intel 1103

MPU   Intel 4004
Most Recent SD Card

In 2012

128GB (Bite)
= 128G X 8bit
= 1T(Tera)bit

1T = 10^{12} = 1 Trillion

World Population: 7 Billion
Brain Cell: 10~100 Billion
Stars in Galaxy: 100 Billion
128 GB = 1Tbit

2.4cm X 3.2cm X 0.21cm

Volume: 1.6 cm³   Weight: 2g

Voltage: 2.7 - 3.6V

Old Vacuum Tube:
5cm X 5cm X 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube: 5cm X 5cm X 10cm

Volume = (5cm X 10,000) X (5cm X 10,000) X (10cm X 10,000)

= 0.5km X 0.5km X 1km

1Tbit = 10,000 X 10,000 X 10,000 bit

Pingan International Finance Center
Shanghai, China (Year 2016)

Indian Tower
Mumbai, India (Year 2016)

Burj Khalifa
Dubai, UAE (Year 2010)

500 m

828 m

700 m
Old Vacuum Tube: 100W

1Tbit = 10^{12} bit
Power = 0.05kWX10^{12}=50 TW

Nuclear Power Generator

1MkW=1BW

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving
Brain: Integrated Circuits

Ear, Eye: Sensor

Mouth: RF/Opto device

Stomach: PV device

Hands, Legs: Power device
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years, even though, it is very matured market!!

2011
300B USD

2025
1,500B USD

Gartner: By K. Kim, CSTIC 2012
2. Current status of Si-CMOS device technologies
Downsizing

Important for

Decreasing cost, power

Increasing performance
Feature Size / Technology Node

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm →
0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm →
90 nm → 65 nm → 45 nm → 32 nm → (28 nm →) 22 nm(2012)

From 1970 to 2013 (This year)

43 years 1 generation
18 generations 2.5 years
Line width: 1/450 Line width: 1/1.43 = 0.70
Area: 1/200,000 Area: 1/2 = 0.5
Problem for downsizing

Region governed by gate bias
Region governed by drain bias

Gate oxide
Gate metal

Source
0V

Gate oxide

Drain
0V

Channel

Substrate
0V

0V < \(V_{dep}\) < 1V

Large \(I_{OFF}\)
Region (DL)

No \(t_{ox}\), \(V_{dd}\) thinning

Large \(I_{OFF}\)
(Electron current)

\(t_{ox}\), \(V_{dd}\) thinning

0V

\(V_{dd}\) 0V

\(V_{dd}\) 1V

\(V_{dd}\)

0V 0.5V

\(V_{dd}\)

0V

\(V_{dd}\)

0V

\(t_{ox}\) and \(V_{dd}\) have to be decreased for better channel potential control \(\rightarrow I_{OFF}\) Suppression
$L_{gate}$ and $t_{ox}(EOT)$ scaling trend

A. Toriumi (Tokyo Univ), IEDM 2006, Short Course
EOT=0.40nm

Drain Voltage (V) vs. Drain Current (mA)

- L/W = 5/20μm
- Vg = 1.0V
- Vg = 0.8V
- Vg = 0.6V
- Vg = 0.4V
- Vg = 0.2V
- Vg = 0 V

Electron Mobility [cm²/Vsec] vs. Effective Field [MV/cm]

- EOT = 0.40nm
- L/W = 5/20μm
- T = 300K
- N_sub = 3 × 10¹⁶cm⁻³
What would be the limit of downsizing!

Tunneling distance: 3 nm

Source | Channel | Drain

Energy or Potential for Electron

Direct-tunnel current
Subthreshold leakage current of MOSFET

- Subthreshold leakage current of MOSFET
- Subthreshold Current
- Ion
- Ioff
- Subthreshold region
- Vg=0V
- Vth (Threshold Voltage)

Subthreshold Current Is OK at Single Tr. level

But not OK For Billions of Trs.
Subthreshold leakage current will limit the downsizing.
The limit is different depending on application.

- **HP CMOS** (High Performance)
  - Highest Ion, Lowest CV/I
  - High leakage
  - Medium Vdd

- **LOP CMOS** (Low Operation Power)
  - Lowest Vdd
  - Medium Ion, medium CV/I
  - Medium leakage

- **LSTP CMOS** (Low Standby Power)
  - Lowest leakage
  - Low Ion, high CV/I
  - High Vdd

Source: 2007 ITRS Winter Public Conf.
How far can we go for production?

**Past**
0.7 times per 2.5 years

10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm →
0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

**Future**

- At least 4-5 generations to 8 ~ 5 nm

**Intermediate node**

- Drain bias induc ő
- Limit depending on applications

**Fundamental limit**

- Direct-tunnel
- Subthreshold
Extremely Thin SOI

Planar

Extremely Thin SOI

Drain bias induced depletion

Extremely thin Si

SiO₂

Si
Suppression of subthreshold leakage by surrounding gate structure

Planar

Multi gate

Drain bias induced depletion

Si fin or nanowire
Because of off-leakage control, Planar $\rightarrow$ Fin $\rightarrow$ Nanowire

Planar FET

Fin FET

Nanowire FET
Nanowire structures in a wide meaning

Fin

Tri-gate

Tri-gate (Variation)

Ω-gate

All-around
Our work at TIT: Ω-gate Si Nanowire

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
- DIBL of 62mV/V and SS of 70mV/dec for nFET
More Moore to More More Moore

Technology node
65nm  45nm  32nm  22nm
Lg 35nm  Lg 30nm

Now

Future
15nm, 11nm, 8nm, 5nm, 3nm
(Fin,Tri, Nanowire)

28nm

Si is still main stream for future!!

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)
High-k gate dielectrics

Continued research and development

Hf-based oxides

| 45nm | 32nm | 22nm | 15nm, 11nm, 8nm, 5nm, 3nm,
| EOT:1nm | EOT:0.95nm | EOT:0.9nm |

SiO$_2$ IL (Interfacial Layer) is used at Si interface to realize good mobility

Technology for direct contact of high-k and Si is necessary

EOT=0.52 nm
Remote SiO$_2$-IL scavenging HfO$_2$ (IBM)

EOT=0.37nm EOT=0.40nm EOT=0.48nm

0.48 → 0.37nm Increase of $I_d$ at 30%

Direct contact with La-silicate (Tokyo Tech.)

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K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM2009, (IBM)
$I_{ON}$ and $I_{OFF}$ benchmark

**NMOS**

- **Intel [a]**
  - Bulk 32nm Tri-Gate 22nm
  - $V_{DD}=0.8V$
  - $V_{DD}=1V$

- **Intel [b]**
  - Bulk 45nm
  - $V_{DD}=1V$

- **Samsung [c]**
  - Bulk 20nm
  - $V_{DD}=0.9V$

- **Tokyo Tech. [i]**
  - Ω-gate NW
  - $V_{DD}=1V$

- **IBM [g]**
  - ETSOI
  - $V_{DD}=0.9V$
  - $V_{DD}=1V$

- **STMicro. [h]**
  - GAA NW
  - $V_{DD}=1.1V$

**PMOS**

- **Intel [a]**
  - Bulk 32nm Tri-Gate 22nm
  - $V_{DD}=0.8V$

- **Intel [b]**
  - Bulk 45nm
  - $V_{DD}=1V$

- **IBM [g]**
  - ETSOI
  - $V_{DD}=0.9V$
  - $V_{DD}=1V$

- **Samsung [c]**
  - Bulk 20nm
  - $V_{DD}=0.9V$

- **IBM [f]**
  - FinFET 25nm
  - $V_{DD}=1V$

- **IBM [g]**
  - ETSOI
  - $V_{DD}=0.9V$

- **STMicro. [h]**
  - GAA NW
  - $V_{DD}=1.1V$

**References**

[a] C. Auth et al., pp.131, VLSI2012 (Intel).
[d] S. Saitoh et al., pp.11, VLSI2012 (Toshiba).
[g] A. Khakifirooz et al., pp.117, VLSI2012 (IBM).
[i] S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)
## Benchmark of device characteristics

<table>
<thead>
<tr>
<th>Structure</th>
<th>Bulk Planar</th>
<th>Tri-Gate NW</th>
<th>ETSOI</th>
<th>Bulk Planar</th>
<th>GAA NW</th>
<th>GAA NW</th>
<th>Ω-gate NW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lg (nm)</td>
<td>35</td>
<td>30</td>
<td>14</td>
<td>22</td>
<td>20</td>
<td>35/25</td>
<td>22/30</td>
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<tr>
<td>(nFET/pFET)</td>
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<tr>
<td>EOT (nm)</td>
<td>1</td>
<td>0.95</td>
<td>0.9</td>
<td>3</td>
<td>~1</td>
<td>-</td>
<td>1.5</td>
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<tr>
<td>(nFET/pFET)</td>
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<tr>
<td>Vth (V)</td>
<td>~0.4</td>
<td>~0.3</td>
<td>~0.2</td>
<td>~0.15 (nFET)</td>
<td>~0.3</td>
<td>0.3~0.4</td>
<td>~0.5</td>
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<tr>
<td>VDD (V)</td>
<td>1</td>
<td>1</td>
<td>0.8</td>
<td>1</td>
<td>0.9</td>
<td>0.9</td>
<td>1</td>
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<td>(nFET/pFET)</td>
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<tr>
<td>I_on (mA/um) nFET/pFET</td>
<td>1.36/1.07</td>
<td>1.53/1.23</td>
<td>1.26/1.1</td>
<td>0.83 (nFET)</td>
<td>0.59/0.62 (I_eff)</td>
<td>1.2/1.05</td>
<td>0.83/0.95</td>
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<td>DIBL (mV/V) nFET/pFET</td>
<td>~150</td>
<td>~200</td>
<td>46/50</td>
<td>&lt;50</td>
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<td>SS (mV/dec)</td>
<td>-</td>
<td>~100</td>
<td>~70</td>
<td>&lt;80</td>
<td>-</td>
<td>87</td>
<td>85</td>
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<tbody>
<tr>
<td>Gate Dielectrics</td>
<td>Hf-based</td>
<td>Hf-based</td>
<td>SiO₂</td>
<td>HfO₂</td>
<td>HfO₂</td>
<td>Hf-based</td>
<td>HfZrO₂</td>
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<td>0.8</td>
<td>1</td>
<td>0.9</td>
<td>0.9</td>
<td>1</td>
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<td>2.05/1.5</td>
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<td>~200</td>
<td>46/50</td>
<td>&lt;50</td>
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<td>104/115</td>
<td>65/105</td>
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<td>&lt;80</td>
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</tbody>
</table>

40
**Ω-gate Si Nanowire**

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  - (1.32 mA/µm @ $I_{OFF}=117$ nA/µm)
- DIBL of 62mV/V and SS of 70mV/dec for nFET
Electron Density
\((x10^{19} \text{cm}^{-3})\)

Distance from SiNW Surface (nm)

- Edge portion
- Flat portion

Inversion areal ratio: 29 %
Tri-gate implementation for transistors

C. Auth et al., pp.131, VLSI2012 (Intel)

<table>
<thead>
<tr>
<th></th>
<th>HP</th>
<th>MP</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{OX,E}$ (nm)</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>$L_{GATE}$ (nm)</td>
<td>30</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>$I_{OFF}$ (nA/um)</td>
<td>20-100</td>
<td>5-20</td>
<td>1-5</td>
</tr>
</tbody>
</table>

Tri-gate has been implemented since 22nm node, enabling further scaling
Comparison with ITRS

- $L_g$ and EOT are larger than ITRS requirements
- Implementation of Tri-gate and lower $V_{th}/V_{dd}$ since 22nm

K. Mistry et al., pp.247, IEDM2007 (Intel).
P. Packan et al., pp.659, IEDM2009 (Intel).
C. Auth et al., pp.131, VLSI2012 (Intel).
Tri-gate width/height optimization

C. Auth et al., pp.131, VLSI2012 (Intel)

Intel’s fin is triangle shape!

PMOS channel under the gate

S/D region showing the SiGe epitaxy

A fin width of 8nm to balance SCE and $R_{\text{ext}}$

A fin height of 34nm to balance drive current vs. capacitance
- SS of 71 and 72 mV/dec for HP NMOS and PMOS, respectively
- DIBL of 30 and 35 mV/V for NMOS and PMOS, respectively
- $V_{th}$ of 22 nm is about 0.1 ~0.2 V lower than that of 32nm
Extremely Thin SOI (ETSOI)

Also, ET-SOI works very good!

- Hybrid CMOS
  - Si Channel nFET
  - Strained SiGe Channel pFET
- RO delay improvement over FinFET with FO = 2

K. Cheng et al., pp.419, IEDM2012 (IBM)
• $L_g = 25$~35nm GAA NW

• Hydrogen anneal provide smooth channel surface

• Competitive with conventional CMOS technologies

• Scaling the dimensions of NW leads to suppressed SCE
3. Problems
Short-channel effect

T. Skotnicki, IEDM 2009 Short Course (STMicroelectronics)

\[ SCE = 0.64 \frac{q_S}{\varepsilon_{ox}} \times EI \times \Phi_d \]
\[ DIBL = 0.8 \frac{q_S}{\varepsilon_{ox}} \times EI \times V_{ds} \]

\[
\begin{align*}
EI_{\text{Bulk}} &= 1 \times \\
& \times \left(1 + \frac{X_j^2}{L_{el}^2} \right) \\
& \times \frac{1 + \frac{X_j}{L_{el}}}{L_{el}} \\
& \times \frac{\tau_{ox}}{L_{el}} \\
& \times T_{dep} \\
& \times L_{el}
\end{align*}
\]

\[
\begin{align*}
EI_{\text{PD SOI}} &= 1 \times \\
& \times \left(1 + \frac{X_j^2}{L_{el}^2} \right) \\
& \times \frac{1 + \frac{X_j}{L_{el}}}{L_{el}} \\
& \times \frac{\tau_{ox}}{L_{el}} \\
& \times T_{dep} \\
& \times L_{el}
\end{align*}
\]

\[
\begin{align*}
EI_{\text{Thick BOX FD SOI}} &= 1 \times \\
& \times \left(1 + \frac{T_{si}^2}{L_{el}^2} \right) \\
& \times \frac{1 + \frac{T_{si}}{L_{el}}}{L_{el}} \\
& \times \frac{\tau_{ox}}{L_{el}} \\
& \times T_{si} + \lambda T_{box} \\
& \times L_{el}
\end{align*}
\]

\[
\begin{align*}
EI_{\text{UTBB (FD SOI or SON)}} &= 1 \times \\
& \times \left(1 + \frac{T_{si}^2}{L_{el}^2} \right) \\
& \times \frac{1 + \frac{T_{si}}{L_{el}}}{L_{el}} \\
& \times \frac{\tau_{ox}}{L_{el}} \\
& \times T_{si} + \lambda T_{box} \\
& \times L_{el}
\end{align*}
\]

\[
\begin{align*}
EI_{\text{FinFET (independent gates)}} &= 1 \times \\
& \times \left(1 + \frac{T_{si}^2}{L_{el}^2} \right) \\
& \times \frac{1 + \frac{T_{si}}{L_{el}}}{L_{el}} \\
& \times \frac{\tau_{ox}}{L_{el}} \\
& \times T_{si} \\
& \times L_{el}
\end{align*}
\]

\[
\begin{align*}
EI_{\text{FinFET (common gates)}} &= 1 \times \\
& \times \left(1 + \frac{T_{si}^2}{L_{el}^2} \right) \\
& \times \frac{1 + \frac{T_{si}}{L_{el}}}{L_{el}} \\
& \times \frac{\tau_{ox}}{L_{el}} \\
& \times T_{si} \\
& \times L_{el}
\end{align*}
\]

If max ch. doping is \(10^{20} \text{cm}^{-3} \Rightarrow T_{ep} \approx 12 \text{nm}\) then :

\(\lambda T_{box} = 18 \text{nm}\)

If Tsi min \(\approx 3 \text{nm}\) then :

\(\lambda T_{box} = 3 \text{nm}\)

If Tsi min \(\approx 3 \text{nm}\) then :

\(\lambda T_{box} = 0.46 \text{nm}\)

\(\approx 0 \text{nm}\)

If Tsi/min feasible Tsi is supposed 3nm; then :

\(\lambda T_{box} = 2.7 \text{nm}\)

<table>
<thead>
<tr>
<th>(L_{el,min})</th>
<th>(L_{el,min})</th>
<th>(L_{el,min})</th>
<th>(L_{el,min})</th>
<th>(L_{el,min})</th>
<th>(L_{el,min})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\approx 34 \text{nm})</td>
<td>(= 34 \text{nm})</td>
<td>(\approx 30 \text{nm})</td>
<td>(\approx 10 \text{nm})</td>
<td>(\approx 6 \text{nm})</td>
<td>(\approx 2.7 \text{nm})</td>
</tr>
</tbody>
</table>
Drain-induced barrier lowering

\[ DIBL = 0.80 \frac{\varepsilon_Si}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{DS} \]

**BULK**
- \( X_j = 3/4 L_{el} \)
- \( T_{dep} = 3/4 L_{el} \)
- 140 mV/V

**III-V**
- 210 mV/V

**FDSOI**
- \( T_{dep} = T_{si} / 2 \)
- \( X_j = T_{si} \geq 6 \text{nm} \)
- \( T_{si} \geq 10 \text{nm} \)

**ETSOI**
- 110 mV/V

**UTBB**
- 80 mV/V

**FinFET**
- 70 mV/V

T. Skotnicki, IEDM 2010 Short Course (STMicroelectronics)
Sub-threshold Slope

T. Skotnicki, IEDM 2010 Short Course (STMicroelectronics)

\[
S = \frac{kT}{q} \ln\left(1 + \frac{C_{\text{dep}}}{C_{\text{ox}}} + \frac{\varepsilon_{\text{si}} T_{\text{ox}} X_j}{\varepsilon_{\text{ox}} L_{\text{el}} L_{\text{el}}} \left(1 + \frac{3 T_{\text{dep}}}{4 L_{\text{el}}} \right) \sqrt{1 + 2 \frac{V_{ds}}{\Phi_d}} \right)
\]

- **BULK**
  - \( T_{\text{dep}} = 3/4 L_{\text{el}} \)
  - \( X_j = 3/4 L_{\text{el}} \)
  - Slope: 95 mV/dec

- **III-V**
  - \( T_{\text{ox}} + 2A \)
  - \( \varepsilon_{\text{si}} + 15\% \)
  - Slope: 110 mV/dec

- **FDSOI**
  - \( T_{\text{dep}} = T_{\text{si}}/2 \)
  - \( X_j = T_{\text{si}}/2 \)
  - Slope: 85 mV/dec

- **UTBB**
  - \( T_{\text{dep}} = T_{\text{si}} \)
  - \( X_j = T_{\text{si}} \)
  - Slope: 75 mV/dec

- **FinFET**
  - \( T_{\text{dep}} = T_{\text{si}}/2 \)
  - \( X_j = T_{\text{si}}/2 \)
  - Slope: 65 mV/dec

- **ETSOI**
  - RBB ⇒ Pstat

- **RBB**

- **Pstat**
Decreasing the diameter of NW

Improved short-channel control

Severe mobility degradation

Need to decrease diameter for SCH

Significant $\mu$ degradation at diameter < 10 nm

Problems in Multi-gate

S. Bangsaruntip et al., pp.297, IEDM2009 (IBM), K. Tachi et al., pp.313, IEDM2009 (CEA-LETI)
Impact of Si thickness in FinFET

- Replacement Gate process
- TaN/HfO₂ gate stack
- Reduced $g_m$ and higher $V_{th}$ with decreasing Fin width
Problems in SOI

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.

K. Uchida et al., pp.47, IEDM2002 (Toshiba)
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

- **1. Mobility degradation**
  - Extremely small distance between the electron and all around Si surface.
  - Strong scattering of electrons by interaction with all around Si surface.

- **2. Electron density decrease**
  - Decrease of DOS in extremely narrow wire.

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-$k$ is necessary.
Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Wire cross section dependence. What cross section gives best solution for SCE suppression and drive current?

By Profs. Oshiyama and Iwata, U. of Tokyo
Significant increase in $V_{th}$ variability with decreasing Fin width
Smaller wire/fin width is necessary for SCE suppression

But mobility and $I_{ON}$ severely degrade with wire/fin width reduction

Therefore even in multi-gate structures, **EOT scaling should be accelerated** to provide SCE immunity
High-k beyond 0.5 nm
Gate oxide should be thicker than mono atomic layer

0.8 nm gate oxide thickness MOSFETs operate

0.8 nm $\rightarrow$ Distance of 3 Si atoms $\rightarrow$ 2 mono layers

R.Chau, et al., (Intel) IWGI 2003
Gate Leakage Power Density becomes significantly large with $L_g$ reduction, and thus, with $t_{ox}$ thinning!!
To use high-k dielectrics

K: Dielectric Constant

Thin SiO₂

K=4

Almost the same electric characteristics

K=20

Thick high-k dielectrics

5 times thicker

Small leakage Current

Solution

However, very difficult and big challenge!
Combination of high-k and metal gate is important

K. Natori, et al., (Tsukuba Univ) SSDM 2005, p.286

Equivalent Oxide Thickness (EOT): gate dielectrics itself, $C_{ox}$
Capacitance Equivalent Thickness (CET): entire gate stack,

Metal gate can eliminate the poly-Si depletion.

Inversion CET = $T_{inv} \approx EOT + 0.4\text{nm}$
with metal gate electrode

$C_{metal}$ is finite because of quantum effect. In other words electron is not a point charge located at the interface but distributed charge.
Choice of High-k elements for oxide

### Candidates

- **Unstable at Si interface**
  - 1. Si + MO\text{X} \rightarrow M + SiO\text{2}
  - 2. Si + MO\text{X} \rightarrow MSi\text{X} + SiO\text{2}
  - 3. Si + MO\text{X} \rightarrow M + MSi\text{X}O\text{Y}

- **Gas or liquid at 1000 K**
  - Radio active
  - He
  - B, C, N, O, F, Ne

- **Al Si P S Cl Ar**

- **Si + MO\text{X} \rightarrow M + SiO\text{2}
- Si + MO\text{X} \rightarrow MSi\text{X} + SiO\text{2}
- Si + MO\text{X} \rightarrow M + MSi\text{X}O\text{Y}

### Choice of High-k elements for oxide

- **HfO\text{2} based dielectrics** are selected as the first generation materials, because of their merit in
  1) band-offset
  2) dielectric constant
  3) thermal stability

- **La\text{2}O\text{3} based dielectrics** are thought to be the next generation materials, which may not need a thicker interfacial layer

---

R. Hauser, IEDM Short Course, 1999
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Flat metal/high-k interface for better mobility
- Workfunction engineering for $V_{th}$ control
- Suppression of $V_{th}$ tuning
- Suppression of oxygen vacancy formation
- Suppression of metal diffusion
- Interface dipole control for $V_{th}$ tuning
- Suppression of FLP
- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Control of interface reaction and Si diffusion to high-k
- Thinning or removal of SiO$_2$-IL for small EOT
- Reliability: PBTI, NBTI, TDDB
- Remove contamination introduced by CVD
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band Discontinuity [eV]

Dielectric Constant $\varepsilon(0)$

XPS measurement by Prof. T. Hattori, INFOS 2003
Direct high-k/Si by silicate reaction

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface.
Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
Direct high-k/Si by silicate reaction

HfO$_2$ case

La$_2$O$_3$ case

Our approach

Low $P_{O_2}$ → High $P_{O_2}$

Si substrate

SiO$_2$-IL formation

SiO$_2$-IL formation

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface

Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
**SiO$_x$-IL growth at HfO$_2$/Si Interface**

XPS Si1s spectrum

TEM image 500 °C 30 min

Phase separator

HfO$_2$ + Si + O$_2$ → HfO$_2$ + Si + 2O* $\rightarrow$ HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Tans. ECS 11, 319

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Cluster tool for HKMG Stack

EB Deposition for HK

Flash Lamp

Sputter for MG

Robot

ALD

RTA

Entrance
Cluster Chambers for HKMG Gate Stack

EB Deposition: HK
Sputter: MG
Flash Lamp Anneal
ALD: HK

Entrance
Robot
RTA
Deposited thin film

Substrate

Moving Mask

Flux

Source

Electron Beam
L = 0.5~100 µm (8 kinds)
W = 10, 20, 50, 100 µm (4 kinds)

1 cm × 1 cm
Gate Leakage vs EOT, \( (V_g = |1|V) \)

- **Current density** (A/cm²) vs **EOT** (nm)

- Materials: Al₂O₃, HfAlO(N), HfO₂, HfSiO(N), HfTaO, La₂O₃, Nd₂O₃, Pr₂O₃, PrSiO, PrTiO, SiON/SiN, Sm₂O₃, SrTiO₃, Ta₂O₅, TiO₂, ZrO₂(N), ZrSiO, ZrAlO(N)

- Key: Al₂O₃, HfAlO(N), HfO₂, HfSiO(N), HfTaO, La₂O₃, Nd₂O₃, Pr₂O₃, PrSiO, PrTiO, SiON/SiN, Sm₂O₃, SrTiO₃, Ta₂O₅, TiO₂, ZrO₂(N), ZrSiO, ZrAlO(N)

- Data points for HfO₂ and La₂O₃ highlighted.
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small Dit

1. Silicate-reaction-formed fresh interface
2. Stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress

---


No interfacial layer can be confirmed with Si/TiN/W.
La$_2$O$_3$/silicate/$n$-Si CV

W/La$_2$O$_3$(4nm)/$n$-Si
600$^\circ$C, 30min

Capacitance density ($\mu$F/cm$^2$)

Gate voltage (V)

$\Delta$V$_{fb}$
$C_{fb}$
\[ D_{it}, D_{slow} \]

\[ G_{p}/\omega \ \text{[F/cm}^2\text{]} \]

\[ \omega \ \text{[rad/s]} \]

\[ \times 10^{-6} \]

\[ D_{it} \]

\[ D_{slow} \]

(FG anneal)

\[ 400^\circ \text{C} \]

\[ 500^\circ \text{C} \]

\[ 600^\circ \text{C} \]

\[ 200 \ 400 \ 600 \ 800 \ 1000 \]

\[ D_{it}, D_{slow} \ \text{[cm}^{-2}\text{eV]} \]

\[ 10^{14} \ 10^{13} \ 10^{12} \ 10^{11} \]

\[ \text{Annealing temperature } \ (^\circ \text{C}) \]
It is important to change the La$_2$O$_3$ to La-silicate completely.
Annealing temperature (°C)

EOT (nm)

Annealed for 2 s
La$_2$O$_3$(3.5 nm)

W(60 nm)

TiN/W(6 nm)

As depo

W(60 nm)

TiN(45nm)/W(6nm)

EOT=0.55nm

Experiment

Cvc fitting

Theory

TaN/(45nm)/W(3nm)
900°C, 30min
EOT=0.55nm

Cg (µF/cm$^2$)

Vg (V)

0 -1 -0.5 0 0.5 4.5 4 3.5 3 2.5 2 1.5 1 0.5 0
TaN(45nm)/W(3nm)

$Q_{\text{fix}} = 1 \times 10^{11} \text{ cm}^{-2}$

900°C, 30min

Fixed Charge density: $1 \times 10^{11} \text{ cm}^{-2}$
EOT = 0.53 nm

- L/W = 20/20 μm
- T = 300 K
- \( N_{\text{sub}} = 3 \times 10^{16} \text{cm}^{-3} \)
- \( V_g = 1.0 \text{V} \)
- \( V_g = 0.8 \text{V} \)
- \( V_g = 0.6 \text{V} \)
- \( V_g = 0.4 \text{V} \)
- \( V_g = 0.2 \text{V} \)
- \( V_g = 0 \text{V} \)

Electron Mobility [cm²/V·sec]

- \( E_{\text{eff}} = 1 \text{MV/cm} \)
- \( 151 \text{cm}²/\text{Vs} \)
- \( 150 \text{cm}²/\text{Vs} \)

Drain Voltage (V)

Drain Current (µA)

Si-sub

EOT = 0.53 nm

Si-sub

L/W = 20/20 μm

T = 300 K

\( N_{\text{sub}} = 3 \times 10^{16} \text{cm}^{-3} \)

\( E_{\text{eff}} = 1 \text{MV/cm} \)

\( 151 \text{cm}²/\text{Vs} \)

\( 150 \text{cm}²/\text{Vs} \)
TaN/W/LaSiOₓ/nFET

\[ W_g/L_g = 20/20 \mu m \]

\[ \text{EOT}=0.55 \text{nm} \]
Benchmark of La-silicate dielectrics

Gate Leakage current

Effective Mobility


T. Ando, et al., (IBM) IEDM 2009, p.423
## Si benchmark (nMOSFET)

<table>
<thead>
<tr>
<th>Gate stack</th>
<th>EOT</th>
<th>Mobility</th>
<th>$V_{th}$</th>
<th>SS</th>
<th>DIBL</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.52nm</td>
<td>110cm$^2$/Vs (at 1x10$^{13}$cm$^{-2}$)</td>
<td>~0.4V (L$_g$=24nm)</td>
<td>90mV/dec</td>
<td>147mV/V</td>
<td>IBM VLSI2011</td>
</tr>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.55nm</td>
<td>140cm$^2$/Vs (at 1MV/cm)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IBM VLSI2009</td>
</tr>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.45nm</td>
<td>115cm$^2$/Vs (at 1x10$^{13}$cm$^{-2}$)</td>
<td>0.3V (L$_g$=10um)</td>
<td>—</td>
<td>—</td>
<td>IMEC MEE2011</td>
</tr>
<tr>
<td>Metal/HfO$_2$</td>
<td>0.59nm</td>
<td>130cm$^2$/Vs (at 1MV/cm)</td>
<td>0.45V (L$_g$=1um)</td>
<td>75mV/dec</td>
<td>—</td>
<td>Sematech VLSI2009</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.65nm</td>
<td>—</td>
<td>0.3~0.4V (L$_g$=~30nm)</td>
<td>90mV/dec</td>
<td>100mV/V</td>
<td>Samsung VLSI2011</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.95nm</td>
<td>—</td>
<td>~0.3V (L$_g$=30nm)</td>
<td>100mV/dec</td>
<td>~200mV/V</td>
<td>Intel IEDM2009</td>
</tr>
<tr>
<td>W/La-silicate 93</td>
<td>0.62nm</td>
<td>155cm$^2$/Vs (at 1MV/cm)</td>
<td>~0.08V (L$_g$=10um)</td>
<td>~70mV/dec</td>
<td>—</td>
<td>Tokyo Tech. T-ED2012</td>
</tr>
</tbody>
</table>
ALD of La2O3


ALD is indispensable from the manufacturing viewpoint - precise control of film thickness and good uniformity
Advantages of metal S/D
- atomically abrupt junction
- low parasitic resistance
- reduced channel dopant concentration

Issues in metal S/D
- two different $\phi_B$ for $p/n$-ch FETs
- underlap/overlap to the gate
- narrow process temperature window

Metal S/D is considered for alternative channel material such as InGaAs and Ge

Ni is used both on InGaAs and Ge to form alloy.

S.-H. Kim, IEDM (2010) 596
K. Ikeda, VLSI (2012) 165
4. Alternative channel devices
# Ge, III-V bulk properties

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>electron mob. (cm²/Vs)</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
</tr>
<tr>
<td>electron effective mass (/m₀)</td>
<td>m₁: 0.19</td>
<td>m₁: 0.082</td>
<td>0.067</td>
<td>0.08</td>
<td>0.026</td>
<td>0.0135</td>
</tr>
<tr>
<td>hole mob. (cm²/Vs)</td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td>hole effective mass (/m₀)</td>
<td>m₁: 0.49</td>
<td>m₁: 0.45</td>
<td>m₁: 0.45</td>
<td>m₁: 0.57</td>
<td>m₁: 0.44</td>
<td>m₁: 0.016</td>
</tr>
<tr>
<td>band gap (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.14</td>
</tr>
<tr>
<td>permittivity</td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

- **Ge** ⇒ lightest hole $m^*$ (light electron $m^*$) ⇒ pMOS (CMOS)
- **III-V** ⇒ light electron $m^*$ ⇒ nMOS
- **GaAs** · **InP** ⇒ $E_g$ higher than that in **Si** ⇒ low power
InGaAs GAA
$L_{ch}=50$nm, EOT 3.5nm, $V_{DS}=0.5V$ (Purdue Uni.) [a]

Si-FinFET 32nm
Intel $V_{DD}=0.8V$ [10]

InGaAs Tri-gate
$L_{g}=60$nm, EOT 12A, $V_{DS}=0.5V$ (Intel) [b]

Si-FinFET 22nm
Intel $V_{DD}=0.8V$ [j]

Si-FinFET 22nm
Intel $V_{DD}=0.8V$ [j]

InGaAs FinFET
$L_{ch}=130$nm, EOT 3.8nm, $V_{DS}=0.5V$ (NUS) [c]

Si-bulk 45nm
Intel $V_{DD}=1V$ [k]

InGaAs Nanowire
$L_{g}=200$nm, $T_{ox}$ 14.8nm, $V_{DS}=0.5V$ (Hokkaido Uni.) [d]

Ge GAA $L_{g}=300$nm, $V_{DS}=-0.8V$ (ASTAR Singapore) [h]

Metal S/D InGaAs-OI
$L_{ch}=55$nm, EOT 3.5nm, $V_{DS}=0.5V$ (Tokyo Uni.) [e]

Ge Tri-gate
$L_{g}=183$nm, EOT 5.5nm, $V_{DS}=-1V$ (NNDL Taiwan) [i]

[g] J. Feng et al., IEEE EDL 28(2007)637 (Stanford Uni)
[h] J. Peng et al., pp.931, IEDM2009 (ASTAR Singapore)
[i] S. Hsu et al., pp.825, IEDM2011 (NNDL Taiwan)
[j] C. Auth et al., pp.131, VLSI2012 (Intel)
ION/I\textsubscript{OFF} Benchmark of Ge pMOSFET

K. J. Kuhn, ECS Transactions, 33 (6) 3-17 (2010)

Optimization of short channel Ge p-MOSFETs is still under investigation
<table>
<thead>
<tr>
<th>Planar (metal S/D, Strain, Buffer...)</th>
<th>FinFET</th>
<th>Tri-gate</th>
<th>Gate-all-around MOSFET</th>
<th>Nanowire</th>
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<tr>
<td><strong>material</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielectric/EOT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Al₂O₃ / 3.5 nm</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Mobility</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>~600 (cm²/Vs)</td>
<td>~700 (μS/µm)</td>
<td>701 (μS/µm)</td>
<td>~500 (cm²/Vs)</td>
</tr>
<tr>
<td><strong>L_ch (nm)</strong></td>
<td>50 µm</td>
<td>60 μm</td>
<td>50 µm</td>
<td>65 µm</td>
</tr>
<tr>
<td><strong>DIBL (mV/V)</strong></td>
<td>84</td>
<td>-</td>
<td>180</td>
<td>-</td>
</tr>
<tr>
<td><strong>SS (mV/dec)</strong></td>
<td>105</td>
<td>-</td>
<td>145</td>
<td>-</td>
</tr>
<tr>
<td><strong>ION (µA/µm)</strong></td>
<td>278 (V₉=0.5V)</td>
<td>4 (n,p) (V₉=0.5V)</td>
<td>10 (V₉=0.5V)</td>
<td>180 (V₉=0.5V)</td>
</tr>
</tbody>
</table>

III-V/Ge benchmark for various structures

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<td><strong>Al₂O₃ / 3.5 nm</strong></td>
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<td><strong>Mobility</strong></td>
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<td></td>
</tr>
<tr>
<td>-</td>
<td>~600 (cm²/Vs)</td>
<td>~700 (μS/µm)</td>
<td>701 (μS/µm)</td>
<td>~500 (cm²/Vs)</td>
</tr>
<tr>
<td><strong>L_ch (nm)</strong></td>
<td>50 µm</td>
<td>60 μm</td>
<td>50 µm</td>
<td>65 µm</td>
</tr>
<tr>
<td><strong>DIBL (mV/V)</strong></td>
<td>84</td>
<td>-</td>
<td>180</td>
<td>-</td>
</tr>
<tr>
<td><strong>SS (mV/dec)</strong></td>
<td>105</td>
<td>-</td>
<td>145</td>
<td>-</td>
</tr>
<tr>
<td><strong>ION (µA/µm)</strong></td>
<td>278 (V₉=0.5V)</td>
<td>4 (n,p) (V₉=0.5V)</td>
<td>10 (V₉=0.5V)</td>
<td>180 (V₉=0.5V)</td>
</tr>
</tbody>
</table>
InGaSb as channel material (stanford)

Z. Yuan et al., pp.185, VLSI2012 (Stanford Uni)

AlGaSb creates barrier for both electrons and holes

- Achieving both N- and P-type MOSFET on a single channel is possible
- In-content of 20-40% improves performance
- electron/hole mobility > 4000/900 cm²/Vs was gained in a single channel material

I_{ON} at L_G = 50 µm
pMOS: 4 µA/µm
nMOS: 3.8 µA/µm
Metal S/D and InAs buffer layer are used as performance boosters.

- DIBL=84 mV/V and SS=105 mV/V was shown for $L_{\text{ch}} = 55$ nm when In-content was higher.

S. H. Kim et al., pp.177, VLSI2012 (Tokyo Uni)
Common InGaAs-GeSn gate stack (NUS)

- Common gate stack (gate metal and dielectric) were used for both p- and n-type.
- Si$_2$H$_6$ plasma passivation is employed which creates Si layer at interface.

\[ SS: nMOS: 90 \text{ (mV/decade)} \]
\[ pMOS: 190 \text{ (mV/decade)} \]

- High intrinsic peak \( G_{M,Sat} \) of ~465 \( \mu \text{S/} \mu \text{m} \) at \( V_{DS} = -1.1 \text{ V} \) was achieved for \( L_G = 250 \text{ nm} \).
Core-multishell InGaAs nanowires grown without buffer layer on Si substrate (bottom up approach)

At $V_d = 1$ V peak transconductance of 500 mS/mm is achieved (roughly x3 InGaAs nanowire)
Tri-gate InGaAs QW-FET (Intel)


- Tri-gate structure has superiority electrostatic controllability compared to ultra-thin body planar structure
- Steepest SS and smallest DIBL ever reported ($W_{\text{fin}} = 30$nm)
Inversion mode $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFET with ALD $\text{Al}_2\text{O}_3$/WN with well electrostatic properties

- DIBL was suppressed down to $L_{ch} = 50\text{nm}$ and
- $G_{m,\text{max}} = 701\text{mS/mm}$ at $V_{ds} = 1\text{V}$
DIBL = 135 mV/V and drive current over 840 µA/µm at $L_{ch} = 130$nm and $V_{ds} = 1.5$V was achieved.
Ge-nanowire pMOSFET (AIST, Tsukuba)


Using Ni-Ge alloy as metal S/D

Significantly reduces contact resistance

High saturation current and high mobility

\[ \mu_{\text{eff}} = 855 \text{ cm}^2/\text{Vs} \] at \( N_s = 5 \times 10^{12}\text{cm}^{-2} \)

and saturation drain current of

\[ 731 \mu\text{A/} \mu\text{m} \text{ at } V_d = -1\text{V} \]
Selective etching of high defect Ge near Ge/Si interface is used which improves gate controllability.

\[ \frac{I_{ON}}{I_{OFF}} = 10^5 \text{ and } SS = 130 \text{ mV/dec} \]

And \( I_{ON} = 235 \mu\text{m/\mu m} \) at \( V_D = -1V \)
Implementing high-k material to III-V, Ge

III-V (InGaAs, InAs, InGaSb,...)
- ALD-Al₂O₃ is most commonly used as gate dielectric in planar or Multi-gate
- HfO₂-only stacks have high D_{it} (combination of Al₂O₃ or Al or Si is used)

By controlling the formation of GeOₓ at the interface, HfO₂ and Al₂O₃ show good results.
5. Emerging devices
Emerging devices (future scaling trends)

**Carbon-based FET**

- Carbon nanotube
- Graphene

**Junctionless Transistor**

- GaAs mHEMT (20nm)
- SiMOSFET (29nm)
- GaAs pHEMT (100nm)
- CNT
- Graphene

**All-spin logic device**

- Input and output related via Spin-coherent channel

---

Tunnel FET

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

Low $I_{\text{OFF}}$, Low $V_{\text{DD}}$, $SS<60\text{mV/decade}$
TFET vs. MOSFET at low V_{DD}

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

EOT = 1 nm, LG = 20 nm, tlnAs = 5 nm

**TFET**

<table>
<thead>
<tr>
<th>Stage Delay (ps)</th>
<th>Switching Energy (fJ)</th>
<th>Leakage Power (nW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV (FO=3)</td>
<td>105</td>
<td>0.26</td>
</tr>
<tr>
<td>NAND (FO=3)</td>
<td>149</td>
<td>0.32</td>
</tr>
<tr>
<td>NOR (FO=3)</td>
<td>158</td>
<td>0.34</td>
</tr>
<tr>
<td>Combined</td>
<td>129</td>
<td>0.29</td>
</tr>
</tbody>
</table>

**CMOS @0.3V**

<table>
<thead>
<tr>
<th>Stage Delay (ps)</th>
<th>Switching Energy (fJ)</th>
<th>Leakage Power (nW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV (FO=3)</td>
<td>830</td>
<td>0.25</td>
</tr>
<tr>
<td>NAND (FO=3)</td>
<td>1364</td>
<td>0.32</td>
</tr>
<tr>
<td>NOR (FO=3)</td>
<td>1389</td>
<td>0.33</td>
</tr>
<tr>
<td>Combined</td>
<td>1103</td>
<td>0.29</td>
</tr>
</tbody>
</table>

V_{DD} 0.3~0.35V
TFET 8x faster at the same power
“parameter variation is not a significant factor for differentiation between MOSFET and TFET”
**Tunnel FET (Si)**

A. Villalon, pp.49, VLSI 2012 (CEA-LETI)

- X in Si$_{1-x}$Ge$_x$ is optimized to allow for efficient BTBT
  
  - $L_G = 200\text{nm}$
  - $I_{ON}/I_{OFF} \approx 10^5$

Reducing SiGe

Body thickness improves Subthreshold swing.

- 130mV/dec
- 190mV/dec
SS of TFET is function of $V_G$ due to Zener tunnel current

Minimum SS = 21 mV/dec is reached due to optimized series resistance of contact, undoped InAs and InAs/Si

$I_{ON}/I_{OFF} \sim 10^6$ at $V_{DS} = 1.0V$ ($I_{ON} = 1A/\mu m$)
Device structure

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

Device structure

- Tunneling // to the gate oblique to the gate field
- Tunneling ⊥ to the gate in-line with the gate field

Nanowire TFET gate-all-around - best electrostatics

K. Tomioka et al., pp.47, VLSI2012 (Hokkaido University)
## Tunnel FET performance comparison

 measured III-V channel TFETs

<table>
<thead>
<tr>
<th>Reference</th>
<th>Source</th>
<th>Channel</th>
<th>Dielectric</th>
<th>EOT (nm)</th>
<th>$I_{ON}$ (μA/μm)</th>
<th>$V_{DS}$ (V)</th>
<th>$V_{GS}=V_{ON}$</th>
<th>$V_{ON}-V_{OFF}$</th>
<th>$I_{ON}/I_{OFF}$</th>
<th>$S_{MIN}$ (mV/dec)</th>
<th>$S_{EFF}$ (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>this work</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.6</td>
<td>78</td>
<td>0.5</td>
<td>0.5</td>
<td>1.5</td>
<td>2,000</td>
<td>125</td>
<td>230</td>
</tr>
<tr>
<td>Li [4]</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$</td>
<td>3.9</td>
<td>20</td>
<td>0.3</td>
<td>2</td>
<td>6</td>
<td>210</td>
<td>830</td>
<td>1300</td>
</tr>
<tr>
<td>Mookerjea [5]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>5.6</td>
<td>10</td>
<td>0.5</td>
<td>2.5</td>
<td>2.5</td>
<td>10,000</td>
<td>240</td>
<td>310</td>
</tr>
<tr>
<td>Mohata [6]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>2.8</td>
<td>10</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>400,000</td>
<td>200</td>
<td>180</td>
</tr>
<tr>
<td>Zhao [7]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>20</td>
<td>0.45</td>
<td>1</td>
<td>1.5</td>
<td>30,000</td>
<td>86</td>
<td>170</td>
</tr>
<tr>
<td>Zhao [8]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>40</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>200,000</td>
<td>84</td>
<td>190</td>
</tr>
<tr>
<td>Ford [9]</td>
<td>InAs</td>
<td>InAs</td>
<td>ZrO$_2$</td>
<td>2</td>
<td>0.4</td>
<td>0.5</td>
<td>1</td>
<td>1</td>
<td>200</td>
<td>190</td>
<td>220</td>
</tr>
<tr>
<td>Zhou [10]</td>
<td>InP</td>
<td>In$<em>{0.53-0.47}$Ga$</em>{0.47-0.3}$</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.3</td>
<td>20</td>
<td>0.5</td>
<td>1</td>
<td>1.75</td>
<td>450,000</td>
<td>93</td>
<td>150</td>
</tr>
</tbody>
</table>

- $S_{MIN}$: Most common SS which is the inverse of $I_D$-$V_{GS}$ slope at the steepest part
- $S_{EFF}$: Is the average swing when $V_{TH}=V_{DD}/2, V_{OFF}=0$

**Effective SS:**

$$V_{DD} \cdot \frac{2 \log(I_D/I_{OFF})}{118}$$

**Average SS:**

$$\frac{V_{TH} - V_{OFF}}{\log(I_D/I_{OFF})}$$
$I_{ON}$ and $I_{OFF}$ of TFETs

[1] G. Zhou et al., pp. 782, vol. 33, no. 6, EDL 2012 (University of Notre Dame)

C. Auth et al., pp. 131, VLSI2012 (Intel).
K. Mistry et al., pp. 247, IEDM2007 (Intel).
MEMS relay

ON-state resistance [Ohm]

Number of Operation Cycles

Frequency of 1, 5, 25kHz under operation

\( I_{\text{ON}} / I_{\text{OFF}} \) of \( \sim 10^{10} \)

Ultra-low-power digital logic applications.

T. K. Liu et al., pp. 43, VLSI2012 (UC Berkeley)
IM: Conventional Inversion Mode
JAM LD: Junctionless Accumulation Mode with low dope
JAM HD: Junctionless Accumulation Mode with high dope

- JAM devices have **reduced gate control** and **degraded short-channel** characteristics relative to IM
- Not suitable for high-performance logic (high $I_{on}$ and moderate $I_{off}$)
A near-ideal subthreshold slope, close to 60 mV/dec at room temperature, and extremely low leakage currents $I_{ON}/I_{OFF} \sim 1 \times 10^6$ (-1 < $V_g$ < 1)

- Silicon nanowire is uniformly doped
- Gate material is opposite polarity polysilicon

$L_g = 1 \mu m$

$W_{wire} = 30 nm$

- $I_{OFF}$ is smaller than $10^{-15} A$

J. P. Colinge et al., Nature Nano. 5(2010)225
Carbon nanotube and Graphene

SWCNT : single wall carbon nanotube

GNR : graphene nano ribbon

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>SWCNT</th>
<th>GNR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mobility cm²/V/s</td>
<td>1400</td>
<td>&gt;10000</td>
<td>&gt;10000 for large widths</td>
</tr>
<tr>
<td>Mean free path (nm) @ room temp</td>
<td>30</td>
<td>&gt;1,000</td>
<td>~1,000 Bolotin, et al., Phys. Rev. Let., 2008</td>
</tr>
<tr>
<td></td>
<td></td>
<td>McEuen, et al., Trans. Nano., 2002</td>
<td>~10nm for W&lt;10nm</td>
</tr>
<tr>
<td>Thermal conductivity (W/mK)</td>
<td>150</td>
<td>5800</td>
<td>~5000 Balandin, et al., Nano Let., 2008</td>
</tr>
</tbody>
</table>

Carbon materials for FET applications
- an ultra-thin body for aggressive channel length scaling
- excellent intrinsic transport properties similar to carbon nanotubes
- pattern the desired device structures
Sub-10nm carbon nanotube transistor

Transistor operation with $L_{ch}$ of 9nm
Graphene Field-effect Transistor

- Ambipolar Characteristics
- Bi-layer graphene and double gates can open the gap
2D material: single layer MoS$_2$

- Mobility of 190 cm$^2$/Vsec
- $I_{on}$ of 1 $\mu$A/$\mu$m at $V_{DD} = 1$V

Candidate: MoS$_2$, MoSe$_2$, WS$_2$, WSe$_2$, MoTe$_2$, WTe$_2$
Magnetic tunnel junction on S/D

Read/write are enabled by using ferromagnetic electrodes and Spin-polarized current
<table>
<thead>
<tr>
<th>Technology</th>
<th>Advantage</th>
<th>Issues</th>
</tr>
</thead>
<tbody>
<tr>
<td>TFET</td>
<td>Lower $V_{dd}$</td>
<td>Integration higher $I_{ON}$</td>
</tr>
<tr>
<td></td>
<td>Lower $I_{OFF}$</td>
<td></td>
</tr>
<tr>
<td>CNT FET</td>
<td>Higher transport velocity</td>
<td>High density and alignment, reproducibility, integration</td>
</tr>
<tr>
<td></td>
<td>$L_g$ scaling</td>
<td></td>
</tr>
<tr>
<td>Graphene FET</td>
<td>RF application</td>
<td>NOT a direct replacement for Silicon logic</td>
</tr>
<tr>
<td></td>
<td>Large area manufacturing</td>
<td></td>
</tr>
<tr>
<td>MEMS</td>
<td>Extremely low leakage</td>
<td>Endurance</td>
</tr>
<tr>
<td></td>
<td>Ultra-low digital logic</td>
<td>Slow speed, scalability</td>
</tr>
<tr>
<td>Junctionless FET</td>
<td>CMOS process compatibility</td>
<td>Worse gate control in short-channel</td>
</tr>
<tr>
<td>Spin FET</td>
<td>Low power, suitable for memory (nonvolatile info storage)</td>
<td>Low efficiency of spin injection</td>
</tr>
</tbody>
</table>
Conclusions
Conclusions

- New device structures (FinFET, Tri-gate) are replacing conventional Planar CMOS
  
  ![Same performance at lower supply voltage]
  
- HKMG: Continuous innovation has enabled EOT scaling to 9 Å, however, new material could be needed for further EOT scaling.

![La-based high-k material]

- Recent advances in new channel material shows promising device performances but still far to catch up Si-CMOS.

  ![The combination of III-V channel materials with a multi-gate structure appears to be a promising direction. (Higher performance in lower operating voltage)]

- Device demonstration on emerging technologies (such as Tunnel FET, Junctionless FET, Carbon-based FET..) is increasing, But more time is needed for implementation of these technologies in future generation devices as mature technologies.
Extreme scaling in MOSFET

Less abruptness of S/D Junction
- $V_t$ and $I_{ON}$ variation, - GIDL
- Punch-through of S/D

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- $V_t$ and $I_{ON}$ variation
- GIDL

**Metal Schottky S/D junctions**

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Nanowire

Substrate (Bulk Si or SOI)

Ni-silicide Source → Si Channel ← Ni-silicide Drain

Gate Electrode

Side wall

Side wall