InGaAs can provide superior transfer characteristics due to high electron mobility and injection velocity.
The formation of unstable oxides at high-k/InGaAs interface must be controlled.

Due to As dangling bonds, Ga antisites: Ga$_2$O$_3$, As$_2$O$_3$, As$_3$O$_5$ form acceptor-like traps which increase interface state density.


Oxide specimens lead to inferior C-V characteristics.

Ref. Han Zhao et. al, Appl. Phys. Lett. 95, 253501(2009)
Present High-k/InGaAs Approaches

Realization of emergence of new structure devices (FinFET, Gate all-around, strained-channel, common gate-stack...) (VLSI 2011~

Almost all the reported devices employ ALD-\(\text{Al}_2\text{O}_3\)

- Better interface quality (Low \(D_{it} \sim 10^{12} \text{eV}^{-1}\text{cm}^{-2}\))
- Small thermal processing window (\(<400^\circ\text{C}\))
- No EOT scaling

Most tried high-k show common problems (HfO\(_2\) center of attention)

- Degraded interface quality upon annealing (High \(D_{it} \sim 10^{13} \text{eV}^{-1}\text{cm}^{-2}\)) (non-ideal CV...)

**III-V MOSFET**

**InGaAs-based gate stack**

**Issues:**
- High interface state density
- Capacitance dispersion in accumulation
- Thermal stability of gate stack

**Approach:**
- Preserving the atomic ratio of the substrate at dielectric interface (Using covalent dielectrics)
- Controlling diffusion of oxygen from gate metal high-k/InGaAs interface (gate metal selection)

**Issues:**
- Low dopant solubility
- High contact resistance
- Low thermal window for metal contacts

**Approach:**
- non-alloyed NiSi₂ structure with wide thermal window
Unlike HfO$_2$, La$_2$O$_3$ leads to bonding states with InGaAs substrate.

An interfacial LaInGaO layer is formed.
C-V response of W/La₂O₃/InGaAs gate stack is far from ideal

However the interface state density remained above $10^{13} \text{ eV}^{-1}\text{cm}^{-2}$

Formation of LaInGaO which is triggered by radical oxygen atoms must be controlled.
Effect of gate metal on La$_2$O$_3$/InGaAs interface

- Capping by TiN in an in-situ process drastically improves C-V characteristics
- Lowest ever reported $D_{it}$=4.6x10$^{11}$ eV$^{-1}$cm$^{-2}$ was obtained.
Annealing sample without metal gate does not show any reaction at the interface.

TiN capping of the sample reduces the oxide states of all elements by 80%.
Comparison of $D_{it}$ between various oxides

Through proper gate metal selection, La$_2$O$_3$/InGaAs interface showed the lowest $D_{it}$ at temperature up to 620 °C
Comparison of gate leakage current

- Incease of gate leakage current at higher temperature can be suppressed by TiN capping
PMA temperature effect on La$_2$O$_3$/InGaAs CET

- Increase of CET at higher annealing temperatures points to La$_2$O$_3$ and InGaAs reaction at the interface
- TiN capping improves CET tolerance to annealing temperature
### Metal SD/InGaAs purpose

**Purpose**

- high $I_{\text{ON}}/I_{\text{OFF}}$ ratio ($>10^4$)
- small barrier height for electrons ($\phi_{Bn} < 0.2$ eV)
- Thermally stable ($400^\circ C$) metal/InGaAs contact (invariability of schottky barrier height ($\phi_{Bn}$ or $\phi_{Bp}$))
- Inhibit surface roughness caused by thermal treatment

### Fabrication process

1. Substrate cleaning
2. Metal deposition by sputtering
3. Anneal in $N_2$ for 1min
4. Measurement

### Metal selection

- **Si(1.9nm)**
- **Ni(0.5nm)**
- **Ni (10nm)**

$x$ desired sets
Ni and NiSi cross-section TEM image

- Ni deposition leads to Ni-InGaAs alloy formation
- Ga component is reduced

A flat and abrupt interface is obtained for NiSi₂/InGaAs

Tezuka, Tsukuba, SSDM E-8-6 (2011)
Ni-InGaAs alloy composition

Ni-InGaAs alloy starts to form even without thermal annealing.

The structure of the alloy changes by increasing the annealing temperature.

At annealing temperature above 300 °C, stable phases of Ga-oxide dominate the Ga component of the alloy.
NiSi₂/InGaAs interface composition

Substrate stoichiometry is preserved even at 600 °C annealing temperature

No oxide or alloy species were detected at NiSi₂/InGaAs interface
NiSi surface roughness

Si(1.9nm) Ni(0.5nm) p-InGaAs

8 sets (~10nm) Annealed in N₂ ambient – 1min

As-depo 300 ºC 400 ºC 500 ºC

NiSi surface roughness

- Not only the interface but also the surface of NiSi₂ remains smooth after annealing

RMS (nm)

0 0.2 0.4 0.6 0.8 1 1.2

As-depo 300 400 500 Temperature (ºC)

1μm 3μm
NiSi barrier height

\[ J = J_{ST} \exp \left( \frac{qV}{nkT} - 1 \right) \]

\[ J_{ST} = A^* T^2 \exp \left( -\frac{q\phi_{Bn}}{kT} \right) \]

\( \phi_{Bp} = 0.588 \text{ eV} \)  
(less than 0.2 eV  
barrier for electrons)

\( n = 1.06 \) (at -0.2V)  
at room temperature
Conclusions

- Interface passivation, improvement
  - Applying $\text{La}_2\text{O}_3$ for gate dielectric
    1. $\text{La}_2\text{O}_3$ can react with InGaAs, forming interfacial layer
    2. Controlling the quality and amount of this layer is the key for improving interface properties
    3. Oxygen supplied from the gate metal is the trigger for IL formation. Choosing proper gate metal is imperative.

- Metal source-drain implementation
  - Apply $\text{NiSi}_2$ for contact
    1. Minimized reaction with substrate
    2. Smooth interface and surface
    3. Larger thermal stability
    4. Possible SBH controllability
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