Future of Nano CMOS Technology

Hiroshi Iwai

Frontier Research Center
Tokyo Institute of Technology
1. Background for nano-electronics
1900 “Electronics” started.

- Device: Vacuum tube
- Device feature size: 10 cm
- Major Appl.: Amplifier (Radio, TV, Wireless etc.)

→ Technology Revolution

1970 “Micro-Electronics” started.

- Device: Si MOS integrated circuits
- Device feature size: 10 \( \mu \text{m} \)
- Major Appl.: Digital (Computer, PC, etc.)

→ Technology Revolution
2000 “Nano-Electronics” started.

Device: Still, Si CMOS integrated circuits
Device feature size: 100 nm
Major Appl.: Digital (µ-processor, cell phone, etc.)

→Technology Revolution??

Maybe, just evolution or innovation!

But very important so many innovations!
Now, 2013 “Nano-Electronics” continued.

Device: Still, Si CMOS integrated circuits
Device feature size: near 10 nm
Major Appl.: Still Digital (μ-processor, cell phone, etc.)

Still evolution and innovation..

But, so many important emerging applications for smart society.
Questions for future

Future, “Nano-Electronics” still continued?

Device: Still, Si CMOS integrated circuits?
Device feature size: ? nm, what is the limit?

Application: New application?

Any Technology Revolution?
What is special or new for Nano-Electronics?

In 1990’s, people expected completely new mechanism or operational principle due the nano size, like quantum mechanical effects.

However, no fancy new operational principle was found.

At least for logic application, there is no success story for “Beyond CMOS devices” to replace Si-CMOS.

Of course, I do not deny the importance of Beyond CMOS technology development. It is becoming very important as CMOS approach its limit.
Ballistic conduction will not happen even decreasing channel length.

\[ L \gg \lambda \]

**Diffusive transport**

\[ L \sim \lambda \]

**Quasi-Ballistic transport**

\[ L < \lambda \]

**Ballistic transport**

Ballistic transport will never happen for MOSFET because of back scattering at drain.

With decreasing channel length, Drain current increase continue.

Ballistic conduction will not happen even decreasing channel length.

(1D quantum conduction: 77.8\(\mu\)S regardless of the length and material).

Also, 1D quantum conduction, or ballistic conduction will not happen.
2. Importance of nano-electronics as integrated circuits
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power
consumption
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

Al Gate

Si

SiO₂

Si

Si/SiO₂ Interface is extraordinarily good
1970,71: 1st generation of LSIs

DRAM    Intel 1103

MPU    Intel 4004
In 2012

Most Recent SD Card

128GB (Bite)

= 128G X 8bit

= 1T(Tera)bit

1T = 10^{12} = 1 Trillion

World Population: 7 Billion

Brain Cell: 10~100 Billion

Stars in Galaxy: 100 Billion
128 GB = 1Tbit

2.4cm × 3.2cm × 0.21cm

Volume: 1.6 cm³  Weight: 2g

Voltage: 2.7 - 3.6V

Old Vacuum Tube:
5cm × 5cm × 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube: 
5cm X 5cm X 10cm

Volume = (5cm X 10,000) X (5cm X 10,000) 
X (10cm X 10,000) 
= 0.5km X 0.5km X 1km

1Tbit = 10,000 X 10,000 X 10,000 bit

Pingan International Finance Center
Shanghai, China (Year 2016)

Indian Tower
Mumbai, India (Year 2016)

Burji Khalifa
Dubai, UAE (Year 2010)

500 m

1,000 m

1Tbit
**Old Vacuum Tube:**

- **100W**

**Nuclear Power Generator**

- **1MkW = 1BW**

\[
1Tbit = 10^{12} \text{bit}
\]

\[
\text{Power} = 0.05 \text{kW} \times 10^{12} = 50 \text{ TW}
\]

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving
Brain: Integrated Circuits

Ear, Eye: Sensor

Mouth: RF/Opto device

Stomach: PV device

Hands, Legs: Power device
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years, even though, it is very matured market!!

313 billion dollar (US) in 2011

1,528 billion dollar (US) in 2025

Gartner: By K. Kim, CSTIC 2012
2. Current status of Si-CMOS device technologies
Downsizing

Important for

Decreasing cost, power

Increasing performance
Feature Size/Technology Node

(1970) 10 μm → 8 μm → 6 μm → 4 μm → 3 μm → 2μm → 1.2 μm → 0.8 μm → 0.5 μm → 0.35 μm → 0.25 μm → 180 nm → 130 nm → 90 nm → 65 nm → 45 nm → 32 nm → 22 nm (2012)

Averaged downsizing rate (in the past 42 years): ~ 0.7X every 3 years

Total reduction in 19 generations: Gate Length ~ 1/500, Area ~ 1/250,000
Problem for downsizing

- Region governed by gate bias
- Region governed by drain bias

Gate oxide
Gate metal
Source Drain

1V 0V 0V
Substrate

0V < V_{dep} < 1V

Large I_{OFF}

No tox thinning

Depletion Region (DL)

V_{dd}

0V

t_{ox} and V_{dd} have to be decreased for better channel potential control → I_{OFF} Suppression
$L_{\text{gate}}$ and $t_{ox}$ (EOT) scaling trend

A. Toriumi (Tokyo Univ), IEDM 2006, Short Course
Our Work at TIT: High-k

EOT = 0.40nm
What would be the limit of downsizing!

Tunneling distance

3 nm

Source

Channel

Drain
Subthreshold leakage current of MOSFET

- **Vg** (Threshold Voltage)
- **Vg=0V**
- **Subthreshold region**
- **Subthreshold Leakage Current**
- **Ion**
- **loff**
- **Vth** (Threshold Voltage)
- **Subthreshold Current**
  - Is OK at Single Tr. level
  - But not OK For Billions of Trs.
Subthreshold leakage current will limit the downsizing

\[ I_d (A/\mu m) \]

\[ I_{on} \]

\[ I_{off} \]

\[ V_d \]

\[ V_{th} \]

\[ 0.15 \text{ V} \quad 0.3 \text{ V} \]

\[ 0 \quad 0.5 \quad 1 \text{ V} \]

\[ 0 \quad 5 \quad 10^{-5} \quad 10^{-7} \quad 10^{-9} \quad 10^{-11} \]

Electron Energy
Boltzmann statics
\[ \exp \left( \frac{-qV}{kT} \right) \]

Injection
The limit is different depending on application.

HP CMOS (High Performance)
- Highest Ion, Lowest CV/I
- High leakage
- Medium Vdd

LOP CMOS (Low Operation Power)
- Lowest Vdd
- Medium Ion, medium CV/I
- Medium leakage

LSTP CMOS (Low Standby Power)
- Lowest leakage
- Low Ion, high CV/I
- High Vdd

Source: 2007 ITRS Winter Public Conf.
How far can we go for production?

<table>
<thead>
<tr>
<th>Past</th>
<th>0.7 times per 3 years</th>
<th>In 40 years: 18 generations, Size 1/500, Area 1/250,000</th>
</tr>
</thead>
<tbody>
<tr>
<td>1970年</td>
<td>10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm → 0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Now</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td>22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?</td>
<td></td>
</tr>
</tbody>
</table>

- At least 4,5 generations to 8 ~ 5 nm
Suppression of subthreshold leakage by surrounding gate structure
Because of off-leakage control,

Planar $\rightarrow$ Fin $\rightarrow$ Nanowire

Planar FET

Fin FET

Nanowire FET
Nanowire structures in a wide meaning

Fin
Tri-gate
Ω-gate
All-around
Our work at TIT: Ω-gate Si Nanowire

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  (1.32 mA/µm @ I\text{OFF}=117 nA/µm)
- DIBL of 62mV/V and SS of 70mV/dec for nFET
More Moore to More More Moore

Technology node

<table>
<thead>
<tr>
<th>65nm</th>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>L_g 35nm</td>
<td>L_g 30nm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Now

Future

15nm, 11nm, 8nm, 5nm, 3nm

Main stream (Fin, Tri, Nanowire)

Alternative (III-V/Ge)

Si is still main stream for future!!

Si channel

ET: Extremely Thin

Emerging Devices

Si

Planar

Tri-Gate

Alternative (ETSOI)

Others

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)
High-k gate dielectrics

Hf-based oxides

<table>
<thead>
<tr>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
<th>15nm, 11nm, 8nm, 5nm, 3nm,</th>
</tr>
</thead>
</table>

- EOT: 1nm
- EOT: 0.95nm
- EOT: 0.9nm

SiO$_2$ IL (Interfacial Layer) is used at Si interface to realize good mobility.

Continued research and development

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM2009, (IBM)

Remote SiO$_2$-IL scavenging
HfO$_2$ (IBM)

EOT=0.52 nm

Direct contact with La-silicate (Tokyo.Tech)

0.48 → 0.37nm Increase of I$_d$ at 30%

EOT=0.37nm

EOT=0.40nm

EOT=0.48nm
Supply voltage affects very much!
## Benchmark of device characteristics

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Lg (nm)</td>
<td>35</td>
<td>30</td>
<td>30</td>
<td>14</td>
<td>22</td>
<td>20</td>
<td>35/25</td>
<td>22/30</td>
</tr>
<tr>
<td>Gate Dielectrics</td>
<td>Hf-based</td>
<td>Hf-based</td>
<td>SiO₂</td>
<td>HfO₂</td>
<td>HfO₂ ?</td>
<td>Hf-based</td>
<td>HfZrO₂</td>
<td>SiO₂</td>
</tr>
<tr>
<td>EOT (nm)</td>
<td>1</td>
<td>0.95</td>
<td>0.9</td>
<td>3</td>
<td>~1</td>
<td>-</td>
<td>1.5</td>
<td>-</td>
</tr>
<tr>
<td>Vth (V)</td>
<td>~0.4</td>
<td>~0.3</td>
<td>~0.2</td>
<td>-0.15 (nFET)</td>
<td>0.3~0.4</td>
<td>~0.3</td>
<td>0.3~0.4</td>
<td>~0.5</td>
</tr>
<tr>
<td>VDD (V)</td>
<td>1</td>
<td>1</td>
<td>0.8</td>
<td>1</td>
<td>0.9</td>
<td>0.9</td>
<td>1</td>
<td>1.1</td>
</tr>
<tr>
<td>ION (mA/um) nFET/pFET</td>
<td>1.36/1.07</td>
<td>1.53/1.23</td>
<td>1.26/1.1</td>
<td>0.83 (nFET)</td>
<td>0.59/0.62 (I&lt;sub&gt;eff&lt;/sub&gt;)</td>
<td>1.2/1.05</td>
<td>0.83/0.95</td>
<td>2.05/1.5</td>
</tr>
<tr>
<td>DIBL (mV/V) nFET/pFET</td>
<td>~150</td>
<td>~200</td>
<td>46/50</td>
<td>&lt;50</td>
<td>-</td>
<td>104/115</td>
<td>65/105</td>
<td>56/9</td>
</tr>
<tr>
<td>SS (mV/dec)</td>
<td>-</td>
<td>~100</td>
<td>~70</td>
<td>&lt;80</td>
<td>-</td>
<td>87</td>
<td>85</td>
<td>&lt;80</td>
</tr>
</tbody>
</table>
Ω-gate Si Nanowire

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  (1.32 mA/μm @ I_{OFF}=117 nA/μm)
- DIBL of 62mV/V and SS of 70mV/dec for nFET
Tri-gate implementation for transistors

C. Auth et al., pp.131, VLSI2012 (Intel)

<table>
<thead>
<tr>
<th></th>
<th>HP</th>
<th>MP</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{OX,E}$ (nm)</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>$L_{GATE}$ (nm)</td>
<td>30</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>$I_{OFF}$ (nA/um)</td>
<td>20-100</td>
<td>5-20</td>
<td>1-5</td>
</tr>
</tbody>
</table>

Tri-gate has been implemented since 22nm node, enabling further scaling
L_g and EOT are larger than ITRS requirements

Implementation of Tri-gate and lower V_{th}/V_{dd} since 22nm

K. Mistry et al., pp.247, IEDM2007 (Intel).
P. Packan et al., pp.659, IEDM2009 (Intel).
C. Auth et al., pp.131, VLSI2012 (Intel).
Tri-gate width/height optimization

Intel’s fin is triangle shape!

C. Auth et al., pp.131, VLSI2012 (Intel)

PMOS channel under the gate
S/D region showing the SiGe epitaxy

A fin width of 8nm to balance SCE and $R_{ext}$
A fin height of 34nm to balance drive current vs. capacitance
SS of 71 and 72 mV/dec for HP NMOS and PMOS, respectively

DIBL of 30 and 35 mV/V for NMOS and PMOS, respectively

V_{th} of 22 nm is about 0.1 ~0.2 V lower than that of 32nm

Very good V_{th} control!
Extremely Thin SOI (ETSOI)

K. Cheng et al., pp.419, IEDM2012 (IBM)

Also, ET-SOI works very good!

- Hybrid CMOS
  Si Channel nFET
  Strained SiGe Channel pFET
- RO delay improvement over FinFET with FO = 2

![Diagram showing comparison between Si CMOS and Hybrid CMOS]

![Graphs showing current measurements for Si and SiGe]

![Graph showing RO delay improvement with ETSOI FO = 3 vs FinFET FO = 2]
- $L_g = 25\sim35\text{nm}$ GAA NW

- Hydrogen anneal provide smooth channel surface

- Competitive with conventional CMOS technologies

- Scaling the dimensions of NW leads to suppressed SCE
3. Problems
Short-channel effect

T. Skotnicki, IEDM 2009 Short Course (STMicroelectronics)

\[
\begin{align*}
SCE &= 0.64 \frac{\varepsilon_s}{\varepsilon_{ox}} \times E_1 \times \Phi_d \\
DIBL &= 0.8 \frac{\varepsilon_s}{\varepsilon_{ox}} \times E_1 \times V_{ds}
\end{align*}
\]

\[
\begin{align*}
E_1 &= 1 \times \\
&\times \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \\
&\times \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}}
\end{align*}
\]

\[
\begin{align*}
E_1 &= 1 \times \\
&\times \left( 1 + \frac{T^2_{si}}{L_{el}^2} \right) \\
&\times \frac{T_{ox}}{L_{el}} \frac{T_{si} + \lambda T_{box}}{L_{el}}
\end{align*}
\]

\[
\begin{align*}
E_1 &= 1 \times \\
&\times \left( 1 + \frac{T^2_{si}}{L_{el}^2} \right) \\
&\times \frac{T_{ox}}{L_{el}} \frac{T_{si} + T_{box}}{L_{el}}
\end{align*}
\]

\[
\begin{align*}
E_1 &= 1 \times \\
&\times \left( 1 + \frac{T^2_{si}}{L_{el}^2} \right) \\
&\times \frac{T_{ox}}{L_{el}} \frac{T_{si} / 2}{L_{el}}
\end{align*}
\]

\[
\begin{align*}
E_1 &= 1 \times \\
&\times \left( 1 + \frac{T^2_{si} / 4}{L_{el}^2} \right) \\
&\times \frac{T_{ox}}{L_{el}} \frac{T_{si} / 2}{L_{el}}
\end{align*}
\]

- If max. ch. doping is $10^{20} \text{ cm}^{-3}$ => T_{ep} ~ 12 nm then:
  - $T_{box} = 145 \text{ nm}$
  - $\lambda T_{box} = 18 \text{ nm}$

- If T_{si} min ~ 3 nm then:
  - $T_{box} = 10 \text{ nm}$
  - $\lambda T_{box} = 3 \text{ nm}$

- If T_{si} min ~ 3 nm then:
  - $T_{box} = 10 \text{ nm}$
  - $\lambda T_{box} = 0.46 \text{ nm}$

- T_{si} / 2 plays role of X_{j}, and that of T_{dep}, if minimum feasible T_{si} is supposed 3 nm, then:

<table>
<thead>
<tr>
<th>$L_{el,\text{min}}$ (DIBL=100mV/V)</th>
<th>$L_{el,\text{min}}$ (DIBL=100mV/V)</th>
<th>$L_{el,\text{min}}$ (DIBL=100mV/V)</th>
<th>$L_{el,\text{min}}$ (DIBL=100mV/V)</th>
<th>$L_{el,\text{min}}$ (DIBL=100mV/V)</th>
<th>$L_{el,\text{min}}$ (DIBL=100mV/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$= 34 \text{ nm}$</td>
<td>$= 34 \text{ nm}$</td>
<td>$\approx 30 \text{ nm}$</td>
<td>$\approx 10 \text{ nm}$</td>
<td>$\approx 6 \text{ nm}$</td>
<td>$\approx 2.7 \text{ nm}$</td>
</tr>
</tbody>
</table>
Drain-induced barrier lowering

\[ DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left(1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{DS} \]

\[ T_{dep} = T_{si} + \lambda T_{box} \]
\[ X_j = T_{si} \geq 6 \text{nm} \]
\[ T_{dep} = T_{si}/2 \]
\[ X_j = T_{si}/2 \]
\[ T_{si} \geq 10 \text{nm} \]

BULK: 140mV/V
BULK: \( T_{dep} = 3/4 L_{el} \)

III-V: 210mV/V

ETSOI: 110mV/V

FDSOI: 80mV/V

UTBB: 70mV/V

FinFET: 70mV/V

\( T_{ox} + 2A \quad \varepsilon_{Si} + 15\% \)
Sub-threshold Slope

\[ S = \frac{kT}{q} \ln \left( 1 + \frac{C_{dep}}{C_{ox}} + \frac{\varepsilon_{Si} T_{ox} X_j}{\varepsilon_{ox} L_{el} L_{el}} \left( 1 + \frac{3 T_{dep}}{4 L_{el}} \right) \right) \]

- BULK: \( T_{dep} = \frac{3}{4} L_{el} \)
  - \( X_j = \frac{3}{4} L_{el} \)
  - \( 95 \text{ mV/dec} \)

- III-V
  - \( T_{ox} + 2A \)
  - \( \varepsilon_{Si} + 15\% \)
  - \( 110 \text{ mV/dec} \)

- FDSOI
  - \( T_{dep} = T_{si}/2 \)
  - \( X_j = T_{si}/2 \)

- UTBB
  - \( 75 \text{ mV/dec} \)

- ETSOI
  - \( 85 \text{ mV/dec} \)

- FinFET
  - \( T_{dep} = T_{si}/2 \)
  - \( X_j = T_{si}/2 \)
  - RBB => Pstat
  - \( 65 \text{ mV/dec} \)

T. Skotnicki, IEDM 2010 Short Course (STMicroelectronics)
Problems in Multi-gate

S. Bangsaruntip et al., pp.297, IEDM2009 (IBM), K. Tachi et al., pp.313, IEDM2009 (CEA-LETI)

Need to decrease diameter for SCH

Significant $\mu$ degradation at diameter < 10 nm

Decreasing the diameter of NW

Improved short-channel control $\leftrightarrow$ Severe mobility degradation

Effective mobility [cm$^2$/Vs] versus $N_{inv}$ [$10^{13}$ cm$^{-2}$]

PFET legend
- $W$ (nm) / $H$ (nm)
  - $\sim 5 / \sim 6$
  - 6.8 / 9.5
  - 9.0 / 13.9
  - 11.2 / 20.0

NFET legend
- $W$ (nm) / $H$ (nm)
  - 6.8 / 9.5
  - 12.3 / 15.1
  - 16.5 / 22.1
  - 21.6 / 23.8

DIBL (mV/V) versus $L_G$ (nm)

PFETs

NFETs
Impact of Si thickness in FinFET

- Replacement Gate process
- TaN/HfO₂ gate stack
- Reduced $g_m$ and higher $V_{th}$ with decreasing Fin width
Problems in SOI

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of \( I_d \)

1. Electron Scattering of every surface
2. Decrease of DOS

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-\( k \) is necessary.
Increase the Number of quantum channels

Energy band of Bulk Si

By Prof. Shiraishi of Tsukuba univ.

4 channels can be used

Energy band of 3 x 3 Si wire
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Wire cross section dependence.

What cross section gives best solution for SCE suppression and drive current?

By Profs. Oshiyama and Iwata, U. of Tokyo
Significant increase in $V_{th}$ variability with decreasing Fin width
Smaller wire/fin width is necessary for SCE suppression

- But mobility and $I_{ON}$ severely degrade with wire/fin width reduction

- Therefore even in multi-gate structures, **EOT scaling should be accelerated** to provide SCE immunity
High-k beyond 0.5 nm
Gate oxide should be thicker than mono atomic layer

0.8 nm gate oxide thickness MOSFETs operate

0.8 nm → Distance of 3 Si atoms → 2 mono layers

R.Chau, et al., (Intel) IWGI 2003
Gate Leakage Power Density becomes significantly large with $L_g$ reduction, and thus, with $t_{ox}$ thinning!!
To use high-k dielectrics

K: Dielectric Constant

Thin SiO$_2$

$K=4$

Almost the same electric characteristics

Thick high-k dielectrics

$K=20$

5 times thicker

Small leakage Current

However, very difficult and big challenge!
Combination of high-k and metal gate is important

K. Natori, et al., (Tsukuba Univ) SSDM 2005, p.286

Equivalent Oxide Thickness (EOT): gate dielectrics itself, $C_{OX}$

Capacitance Equivalent Thickness (CET): entire gate stack,

$C_{metal}$ is finite because of quantum effect. In other words electron is not a point charge located at the interface but distributed charge.

Inversion CET = $T_{inv}$ ≈ EOT + 0.4nm with metal gate electrode
### Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>[ \bullet ]</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
<th>He</th>
<th>B</th>
<th>C</th>
<th>N</th>
<th>O</th>
<th>F</th>
<th>Ne</th>
</tr>
</thead>
<tbody>
<tr>
<td>Li</td>
<td>Be</td>
<td>Mg</td>
<td>Ca</td>
<td>Sc</td>
<td>Ti</td>
<td>V</td>
<td>Cr</td>
<td>Mn</td>
<td>Fe</td>
<td>Co</td>
</tr>
<tr>
<td>Na</td>
<td>K</td>
<td>Rb</td>
<td>Sr</td>
<td>Y</td>
<td>Zr</td>
<td>Nb</td>
<td>Mo</td>
<td>Tc</td>
<td>Ru</td>
<td>Rh</td>
</tr>
</tbody>
</table>

Unstable at Si interface:

1. Si + MO\(_X\) → M + SiO\(_2\)
2. Si + MO\(_X\) → MSi\(_X\) + SiO\(_2\)
3. Si + MO\(_X\) → M + MSi\(_X\)O\(_Y\)

Choice of High-k elements for oxide are selected as the first generation materials, because of their merit in:
1. band-offset, 2. dielectric constant, 3. thermal stability.

HfO\(_2\) based dielectrics are selected as the first generation materials, because of their merit in:
1. band-offset, 2. dielectric constant, 3. thermal stability.

La\(_2\)O\(_3\) based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

R. Hauser, IEDM Short Course, 1999

Issues in high-k/metal gate stack

Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k

Suppression of metal diffusion

Suppression of oxygen vacancy formation

Small interfacial state density at high-k/Si

Control of interface reaction and Si diffusion to high-k

Suppression of gate leakage current

Endurance for high temperature process

Reliability: PBTI, NBTI, TDDB

Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k

Workfunction engineering for $V_{th}$ control

Suppression of FLP

Interface dipole control for $V_{th}$ tuning

Remove contamination introduced by CVD

Thinning or removal of SiO$_2$-IL for small EOT

Endurance for high temperature process

Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k

Flat metal/high-k interface for better mobility

Suppression of oxygen vacancy formation

Small interfacial state density at high-k/Si

Control of interface reaction and Si diffusion to high-k
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band Discontinuity [eV] vs. Dielectric Constant $\varepsilon(0)$

XPS measurement by Prof. T. Hattori, INFOS 2003
Direct high-k/Si by silicate reaction

HfO$_2$ case

La$_2$O$_3$ case

Our approach

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface. Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
**SiO$_x$-IL growth at HfO$_2$/Si Interface**

![XPS Si1s spectrum](image)

**Phase separator**

$$\text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2$$

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Tans. ECS 11, 319

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction
La-Silicate Reaction at $\text{La}_2\text{O}_3$/Si

Direct contact high-$k$/Si is possible

$\text{La}_2\text{O}_3 + \text{Si} + n\text{O}_2 \rightarrow \text{La}_2\text{SiO}_5, \text{La}_2\text{Si}_2\text{O}_7, \text{La}_{9.33}\text{Si}_6\text{O}_{26}, \text{La}_{10}(\text{SiO}_4)_6\text{O}_3,$ etc.

$\text{La}_2\text{O}_3$ can achieve direct contact of high-$k$/Si
Cluster tool for HKMG Stack

EB Deposition for HK

Flash Lamp

Sputter for MG

Robot

ALD

RTA

Entrance

5m

5m

5m
Cluster Chambers for HKMG Gate Stack

EB Deposition: HK
Sputter: MG
Flash Lamp
Anneal
ALD: HK
Entrance
Robot
RTA
Deposited thin film

Substrate

Moving Mask

Flux

Source

Electron Beam
L = 0.5~100µm (8 kinds)
W = 10, 20, 50, 100µm (4 kinds)

26 chips

1cm x 1cm

30 different Trs

n+ SiO₂
p-Si
n+
Gate Leakage vs EOT, \((V_g = |1| V)\)

Current density \((A/cm^2)\)

EOT (nm)

La\(_2\)O\(_3\)

HfO\(_2\)

Gate leakage vs EOT for various oxides and silicates.
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small $D_{it}$

1. Silicate-reaction-formed fresh interface

2. Stress relaxation at interface by glass type structure of La silicate.


No interfacial layer can be confirmed with Si/TiN/W.
La$_2$O$_3$/silicate/$n$-Si CV
A graph showing the dependence of \( G_p/\omega \) (in F/cm²) on \( \omega \) (in rad/s) for different annealing temperatures. The graph includes data points for annealing temperatures of 400°C, 500°C, and 600°C. The axes are labeled as follows:

- Y-axis: \( G_p/\omega \) (in F/cm²)
- X-axis: \( \omega \) (in rad/s)

A separate graph shows the relationship between the annealing temperature (in °C) and the Dit and Dslow values. The Dit values are shown in a log scale ranging from \( 10^{11} \) to \( 10^{14} \) cm⁻²/eV, while the Dslow values are shown in a log scale ranging from \( 10^{11} \) to \( 10^{14} \).
It is important to change the La2O3 to La-silicate completely.
Annealing temperature (°C) vs. EOT (nm)

- TiN(45nm)/W(6nm)
- Annealed for 2 s
- La₂O₃(3.5 nm)
- W(60 nm)
- TiN/W(6 nm)

Graph showing the relationship between annealing temperature and EOT for different layers.

EOT=0.55nm

- TaN/(45nm)/W(3nm)
- 900°C, 30min
- EOT=0.55nm

Graph showing the relationship between Vg (V) and Cg (µF/cm²) for experiment and theory.
Flat-band voltage (V)

EOT (nm)

TaN(45nm)/W(3nm)

\( Q_{fix} = 1 \times 10^{11} \text{ cm}^{-2} \)

900°C, 30min

Fixed Charge density: \( 1 \times 10^{11} \text{ cm}^{-2} \)
EOT = 0.53nm

L/W = 20/20 μm
T = 300K
N_{sub} = 3 \times 10^{16} \text{cm}^{-3}

E_{eff} = 1 \text{MV/cm}
151 \text{cm}^2/\text{Vs}

E_{eff} = 150 \text{cm}^2/\text{Vs}
Gate current (A/cm²) vs. Gate voltage (V) for a TaN/W/LaSiOₓ/nFET device with W_g/L_g = 20/20 μm and EOT = 0.55 nm. The graph shows the device performance compared to the ITRS standard.
Recent results by my group.
Benchmark of La-silicate dielectrics

Gate leakage is one order of magnitude lower than that of ITRS.

Electron mobility is comparable to record mobility with Hf-based oxides.


T. Ando, et al., (IBM) IEDM 2009, p.423
## Si benchmark (nMOSFET)

<table>
<thead>
<tr>
<th>Gate stack</th>
<th>EOT</th>
<th>Mobility</th>
<th>$V_{th}$</th>
<th>SS</th>
<th>DIBL</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.52nm</td>
<td>110cm$^2$/Vs</td>
<td>~0.4V</td>
<td>90mV/dec</td>
<td>147mV/V</td>
<td>IBM VLSI2011</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(at 1x10$^{13}$cm$^{-2}$)</td>
<td>(L$_g$=24nm)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.55nm</td>
<td>140cm$^2$/Vs</td>
<td>~</td>
<td>~</td>
<td>~</td>
<td>IBM VLSI2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(at 1MV/cm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.45nm</td>
<td>115cm$^2$/Vs</td>
<td>0.3V</td>
<td>~</td>
<td>~</td>
<td>IMEC MEE2011</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(at 1x10$^{13}$cm$^{-2}$)</td>
<td>(L$_g$=10um)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal/HfO$_2$</td>
<td>0.59nm</td>
<td>130cm$^2$/Vs</td>
<td>0.45V</td>
<td>75mV/dec</td>
<td>~</td>
<td>Sematech VLSI2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(at 1MV/cm)</td>
<td>(L$_g$=1um)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.65nm</td>
<td>~</td>
<td>0.3~0.4V</td>
<td>90mV/dec</td>
<td>100mV/V</td>
<td>Samsung VLSI2011</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(L$_g$=~30nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.95nm</td>
<td>~</td>
<td>~0.3V</td>
<td>100mV/dec</td>
<td>~200mV/V</td>
<td>Intel IEDM2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(L$_g$=30nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W/La-silicate 92</td>
<td>0.62nm</td>
<td>155cm$^2$/Vs</td>
<td>-0.08V</td>
<td>~70mV/dec</td>
<td>~</td>
<td>Tokyo Tech. T-ED2012</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(at 1MV/cm)</td>
<td>(L$_g$=10um)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
ALD of La2O3


Precursor (ligand)

La(iPrCp)3

La(FAMD)3

ALD is indispensable from the manufacturing viewpoint - precise control of film thickness and good uniformity.

1 cycle

1. La gas feed
2. Ar purge
3. H2O feed
4. Ar purge

ALD of La2O3
Advantages of metal S/D
- atomically abrupt junction
- low parasitic resistance
- reduced channel dopant concentration

Issues in metal S/D
- two different $\phi_B$ for $p/n$-ch FETs
- underlap/overlap to the gate
- narrow process temperature window

Metal S/D is considered for alternative channel material such as InGaAs and Ge

Ni is used both on InGaAs and Ge to form alloy.

S.-H. Kim, IEDM (2010) 596
K. Ikeda, VLSI (2012) 165
4. Alternative channel devices
## Ge, III-V bulk properties

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron mob.</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
</tr>
<tr>
<td>(cm²/Vs)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electron eff. mass (m₀)</td>
<td>m₁: 0.19</td>
<td>m₁: 0.916</td>
<td>m₁: 0.082</td>
<td>m₁: 1.467</td>
<td>0.067</td>
<td>0.08</td>
</tr>
<tr>
<td>Hole mob.</td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td>(cm²/Vs)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hole eff. mass</td>
<td>mₕ: 0.49</td>
<td>mₕ: 0.16</td>
<td>mₕ: 0.28</td>
<td>mₕ: 0.45</td>
<td>mₕ: 0.45</td>
<td>mₕ: 0.57</td>
</tr>
<tr>
<td>(m₀)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Band gap (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.14</td>
</tr>
<tr>
<td>Permittivity</td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

- Ge ⇒ lightest hole $m^*$ (light electron $m^*$) ⇒ pMOS (CMOS)
- III-V ⇒ light electron $m^*$ ⇒ nMOS
- GaAs·InP ⇒ $E_g$ higher than that in Si ⇒ low power

*S. Takagi., IEDM2011, Short course (Tokyo Uni)*
Multi-gate III-V and Si benchmark

**nMOS**
- **InGaAs GAA**
  - $L_g = 50$ nm, Dielectric: $10$ nm Al$_2$O$_3$
  - $V_{DS} = 0.5$ V (Purdue) [1]
- **Si-FinFET 32nm**
  - $V_{DS} = 0.5$ V (Intel) [10]
- **InGaAs Tri-gate**
  - $L_g = 60$ nm, EOT $12$ A
  - $V_{DS} = 0.5$ V (Intel) [2]
- **InGaAs FinFET**
  - $L_{ch} = 130$ nm
  - EOT 3.8 nm
  - $V_{DS} = 0.5$ V (NUS) [3]
- **Si-FinFET 22nm**
  - $V_{DS} = 0.8$ V [10]
- **Si-bulk 45nm**
  - $V_{DD} = 0.8$ V [10]
- **InGaAs Nanowire**
  - $L_g = 200$ nm, $T_{ox} = 14.8$ nm
  - $V_{DS} = 0.5V$ (Hokkaido Uni.) [4]
- **Metal S/D InGaAs-OI**
  - $L_{ch} = 55$ nm
  - EOT 3.5 nm
  - $V_{DS} = 0.5$ V (Tokyo Uni.) [5]

**pMOS**
- **GOI Tri-gate**
  - $L_g = 65$ nm, EOT 3.0 nm
  - $V_D = -1$ V (AIST Tsukuba) [6]
- **Si-FinFET 32nm**
  - $V_{DS} = 0.8$ V [10]
- **Si-FinFET 22nm**
  - $V_{DS} = 0.8$ V [10]
- **Si-bulk 45nm**
  - $V_{DD} = 1$ V
- **Ge FinFET**
  - $L_g = 4.5$ mm
  - Dielectric: SiON, $V_{DS} = -1$ V (Stanford Uni.) [7]
- **Ge GAA**
  - $L_g = 300$ nm
  - Dielectric: GeO$_2$ (7nm)-HfO$_2$ (10nm)
  - $V_D = -0.8$ V (ASTAR Singapore) [8]
- **Ge Tri-gate**
  - $L_g = 183$ nm, EOT 5.5 nm
  - $V_D = -1$ V (NNDL Taiwan) [9]

**References**
Optimization of short channel Ge p-MOSFETs is still under investigation.
### III-V/Ge benchmark for various structures

<table>
<thead>
<tr>
<th>Material</th>
<th>Planar  (metal S/D, Strain, Buffer...)</th>
<th>FinFET</th>
<th>Tri-gate</th>
<th>Gate-all-around MOSFET</th>
<th>Nanowire</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric/EOT</td>
<td>Al₂O₃/3.5 nm</td>
<td>5nm ALD Al₂O₃</td>
<td>SiON</td>
<td>1.2 nm</td>
<td>5.5 nm (Al₂O₃ + GeO₂)</td>
</tr>
<tr>
<td>Mobility</td>
<td>~600 (cm²/Vs)</td>
<td>~700 (µS/µm)</td>
<td>-</td>
<td>-</td>
<td>701 (µS/µm)</td>
</tr>
<tr>
<td>Lch (nm)</td>
<td>55</td>
<td>100</td>
<td>60</td>
<td>50</td>
<td>200</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>84</td>
<td>180</td>
<td>-</td>
<td>210</td>
<td>-</td>
</tr>
<tr>
<td>SS (mV/dec)</td>
<td>105</td>
<td>145</td>
<td>90</td>
<td>150</td>
<td>160</td>
</tr>
<tr>
<td>Ion (µA/µm)</td>
<td>278</td>
<td>10</td>
<td>235</td>
<td>180</td>
<td>604</td>
</tr>
</tbody>
</table>
InGaSb as channel material (stanford)

Z. Yuan et al., pp.185, VLSI2012 (Stanford Uni)

AlGaSb creates barrier for both electrons and holes

- Achieving both N- and P-type MOSFET on a single channel is possible
- In-content of 20-40% improves performance
- electron/hole mobility > 4000/900 cm²/Vs was gained in a single channel material

I_{ON} at L_G = 50 µm
pMOS: 4 µA/µm
nMOS: 3.8 µA/µm
Metal S/D and InAs buffer layer are used as performance boosters.

- DIBL=84 mV/V and SS=105 mV/V was shown for $L_{ch} = 55$ nm when In-content was higher.

*S. H. Kim et al., pp.177, VLSI2012 (Tokyo Uni)*
Common InGaAs-GeSn gate stack (NUS)

- Common gate stack (gate metal and dielectric) were used for both p- and n-type.
- Si$_2$H$_6$ plasma passivation is employed which creates Si layer at interface.
  
  \[
  \begin{align*}
  SS: \quad & nMOS: \quad 90 \text{ (mV/decade)} \\
  pMOS: \quad & 190 \text{ (mV/decade)}
  \end{align*}
  \]

- High intrinsic peak $G_{M,\text{Sat}}$ of \( \approx 465 \mu \text{S/}\mu \text{m} \) at $V_{DS}=-1.1 \text{ V}$ was achieved for $L_G=250 \text{ nm}$.

Core-multishell InGaAs nanowires grown without buffer layer on Si substrate (bottom up approach)

At $V_d = 1$ V peak transconductance of 500 mS/mm is achieved (roughly x3 InGaAs nanowire)
Tri-gate structure has superiority electrostatic controllability compared to ultra-thin body planar structure

- Steepest SS and smallest DIBL ever reported ($W_{\text{fin}} = 30\text{nm}$)

Inversion mode $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFET with ALD $\text{Al}_2\text{O}_3$/WN with well electrostatic properties

- DIBL was suppressed down to $L_{\text{ch}} = 50\text{nm}$ and $G_{\text{m, max}} = 701\text{mS/mm}$ at $V_{\text{ds}} = 1\text{V}$
DIBL = 135 mV/V and drive current over 840 µA/µm at $L_{ch} = 130$nm and $V_{ds} = 1.5$V was achieved.
Ge-nanowire pMOSFET (AIST, Tsukuba)


- Using Ni-Ge alloy as metal S/D
  - Significantly reduces contact resistance
  - High saturation current and high mobility
    - $\mu_{\text{eff}} = 855 \text{ cm}^2/\text{Vs}$ at $N_s = 5 \times 10^{12} \text{cm}^{-2}$
    - and saturation drain current of $731 \mu\text{A}/\mu\text{m}$ at $V_d = -1\text{V}$

$L_g = 65\text{nm}$, $W_{\text{wire}} = 20\text{nm}$
Selective etching of high defect Ge near Ge/Si interface is used which improves gate controllability.

- $I_{ON}/I_{OFF} = 10^5$ and $SS = 130 \text{ mV/dec}$
- $I_{ON} = 235 \mu\text{m/\mu m}$ at $V_D = -1\text{V}$
Implementing high-k material to III-V, Ge

III-V (InGaAs, InAs, InGaSb, …)
- ALD-Al$_2$O$_3$ is most commonly used as gate dielectric in planar or Multi-gate
- HfO$_2$-only stacks have high $D_{it}$ (combination of Al$_2$O$_3$ or Al or Si is used)

Ge
- By controlling the formation of GeO$_x$ at the interface, HfO$_2$ and Al$_2$O$_3$ show good results.

E. Kim, et al., APL96, 012906
L. Chu, et al., APL99, 042908
Hokkaido Uni, IEDM 2011
Intel, IEDM 2010
R. Zhang et al., VLSI2012, p161
5. Emerging devices
Emerging devices (future scaling trends)

Carbon-based FET

Junctionless Transistor

All-spin logic device

Carbon nanotube

Graphene

GaAs mHEMT

SiMOSFET

GaAs pHEMT

CNT

Graphene

Cut-off frequency (GHz)

Gate length (nm)

A. D. Franklin et al., pp.525, IEDM2011 (IBM)


J. P. Colinge et al., Nature Nano. 5(2010)225


M. Lemme, Nanotech workshop, 2012

J. P. Colinge et al., Nature Nano. 5(2010)266

Input and output related via Spin-coherent channel
Tunnel FET

Low $I_{OFF}$, Low $V_{DD}$, SS<60mV/decade
TFET vs. MOSFET at low $V_{DD}$

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

V$_{DD}$ 0.3~0.35V
TFET 8x faster at the same power
“parameter variation is not a significant factor for differentiation between MOSFET and TFET”
X in $Si_{1-x}Ge_x$ is optimized to allow for efficient BTBT

$\text{L}_G = 200\text{nm}$

$I_{ON}/I_{OFF} \sim 10^5$

Reducing SiGe
Body thickness improves Subthreshold swing.

130mV/dec

190mV/dec
SS of TFET is function of $V_G$ due to Zener tunnel current

Minimum SS = 21 mV/dec is reached due to optimized series resistance of contact, undoped InAs and InAs/Si

$I_{ON}/I_{OFF} \sim 10^6$ at $V_{DS} = 1.0V$ ($I_{ON} = 1A_\mu/\mu m$)
Device structure

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

- Tunneling // to the gate oblique to the gate field
- Tunneling ⊥ to the gate in-line with the gate field

Nanowire TFET gate-all-around - best electrostatics

K. Tomioka et al., pp.47, VLSI2012 (Hokkaido University)
**Tunnel FET performance comparison**

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

measured III-V channel TFETs

<table>
<thead>
<tr>
<th>Reference</th>
<th>Source</th>
<th>Channel</th>
<th>Dielectric</th>
<th>EOT (nm)</th>
<th>$I_{ON}$ (μA/μm)</th>
<th>$V_{DS}$ (V)</th>
<th>$V_{GS}=V_{ON}$ (V)</th>
<th>$V_{ON} - V_{OFF}$ (V)</th>
<th>$I_{ON}/I_{OFF}$</th>
<th>$S_{MIN}$ (mV/dec)</th>
<th>$S_{EFF}$ (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>this work</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.6</td>
<td>78</td>
<td>0.5</td>
<td>0.5</td>
<td>1.5</td>
<td>2,000</td>
<td>125</td>
<td>230</td>
</tr>
<tr>
<td>Li [4]</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$</td>
<td>3.9</td>
<td>20</td>
<td>0.3</td>
<td>2</td>
<td>6</td>
<td>210</td>
<td>830</td>
<td>1300</td>
</tr>
<tr>
<td>Mookerjea [5]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>5.6</td>
<td>10</td>
<td>0.5</td>
<td>2.5</td>
<td>2.5</td>
<td>10,000</td>
<td>240</td>
<td>310</td>
</tr>
<tr>
<td>Mohata [6]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>2.8</td>
<td>10</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>400,000</td>
<td>200</td>
<td>180</td>
</tr>
<tr>
<td>Zhao [7]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>20</td>
<td>0.45</td>
<td>1</td>
<td>1.5</td>
<td>30,000</td>
<td>86</td>
<td>170</td>
</tr>
<tr>
<td>Zhao [8]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>40</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>200,000</td>
<td>84</td>
<td>190</td>
</tr>
<tr>
<td>Ford [9]</td>
<td>InAs</td>
<td>InAs</td>
<td>ZrO$_2$</td>
<td>2</td>
<td>0.4</td>
<td>0.5</td>
<td>1</td>
<td>1</td>
<td>200</td>
<td>190</td>
<td>220</td>
</tr>
<tr>
<td>Zhou [10]</td>
<td>InP</td>
<td>In$<em>{0.53+4}$Ga$</em>{0.47+6}$As</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.3</td>
<td>20</td>
<td>0.5</td>
<td>1</td>
<td>1.75</td>
<td>450,000</td>
<td>93</td>
<td>150</td>
</tr>
</tbody>
</table>

**$S_{MIN}$**: Most common SS which is the inverse of $I_D$-$V_{GS}$ slope at the steepest part

**$S_{EFF}$**: Is the average swing when $V_{TH}=V_{DD}/2$ and $V_{OFF}=0$

**Average SS**: $\frac{V_{TH} - V_{OFF}}{\log(I_D/I_{OFF})}$

**Effective SS**: $\frac{V_{DD}}{2\log(I_D/I_{OFF})}$
**I\textsubscript{ON} and I\textsubscript{OFF} of TFETs**

[1] G. Zhou et al., pp. 782, vol. 33, no. 6, EDL 2012 (University of Notre Dame)

C. Auth et al., pp.131, VLSI2012 (Intel).

K. Mistry et al., pp.247, IEDM2007 (Intel).
ION/IOFF of ~10^10

Ultra-low-power digital logic applications.

Frequency of 1, 5, 25kHz under operation

T. K. Liu et al., pp. 43, VLSI2012 (UC Berkeley)
Junctionless Accumulation Mode (JAM) devices have reduced gate control and degraded short-channel characteristics relative to Conventional Inversion Mode (IM). JAM devices are not suitable for high-performance logic (high $I_{on}$ and moderate $I_{off}$).

- **IM**: Conventional Inversion Mode
- **JAM LD**: Junctionless Accumulation Mode with low dope
- **JAM HD**: Junctionless Accumulation Mode with high dope

---

*Images and diagrams are not transcribed.*

R. Rios et al., *EDL. 32(2011)1170* (Intel)
Near-ideal subthreshold slope, close to 60 mV/dec at room temperature, and extremely low leakage currents

- Silicon nanowire is uniformly doped
- Gate material is opposite polarity polysilicon

\[ \frac{I_{ON}}{I_{OFF}} \sim 1 \times 10^6 \quad (-1 < V_g < 1) \]

\[ I_{OFF} \text{ is smaller than } 10^{-15} \text{ A} \]
**Carbon nanotube and Graphene**

K. Banerjee, UC Santa Barbara, G-COE PICE International Symposium on Silicon Nano Devices in 2030

SWCNT : single wall carbon nanotube  
GNR : graphene nano ribbon

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>SWCNT</th>
<th>GNR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mobility cm²/V/s</td>
<td>1400</td>
<td>&gt;10000</td>
<td>&gt;10000 for large widths</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T. Dürkop, et al.,</td>
<td>200 for W&lt;10nm</td>
</tr>
<tr>
<td>Mean free path (nm) @ room temp</td>
<td>30</td>
<td>&gt;1,000</td>
<td>~1,000</td>
</tr>
<tr>
<td>Thermal conductivity (W/mK)</td>
<td>150</td>
<td>5800</td>
<td>~5000</td>
</tr>
</tbody>
</table>

Carbon materials for FET applications  
- an ultra-thin body for aggressive channel length scaling  
- excellent intrinsic transport properties similar to carbon nanotubes  
- pattern the desired device structures
Sub-10nm carbon nanotube transistor

A. D. Franklin et al., pp.525, IEDM2011 (IBM)

Transistor operation with $L_{ch}$ of 9nm
· Ambipolar Characteristics

· Bi-layer graphene and double gates can open the gap
2D material: single layer MoS$_2$

H. Wang et al., pp.88, IEDM2012 (MIT)

- Mobility of 190 cm$^2$/Vsec
- $I_{on}$ of 1 $\mu$A/$\mu$m at $V_{DD} = 1$V

Candidate: MoS$_2$, MoSe$_2$, WS$_2$, WSe$_2$, MoTe$_2$, WTe$_2$
Spin transfer Torque Switching MOSFET

Magnetic tunnel junction on S/D

Read/write are enabled by using ferromagnetic electrodes and Spin-polarized current
<table>
<thead>
<tr>
<th>Technology</th>
<th>Advantage</th>
<th>Issues</th>
</tr>
</thead>
<tbody>
<tr>
<td>TFET</td>
<td>Lower $V_{dd}$</td>
<td>Integration</td>
</tr>
<tr>
<td></td>
<td>Lower $I_{OFF}$</td>
<td>higher $I_{ON}$</td>
</tr>
<tr>
<td>CNT FET</td>
<td>Higher transport velocity</td>
<td>High density and</td>
</tr>
<tr>
<td></td>
<td>$L_g$ scaling</td>
<td>alignment, reproducibility, integration</td>
</tr>
<tr>
<td>Graphene FET</td>
<td>RF application</td>
<td>NOT a direct replacement</td>
</tr>
<tr>
<td></td>
<td>Large area manufacturing</td>
<td>for Silicon logic</td>
</tr>
<tr>
<td>MEMS</td>
<td>Extremely low leakage</td>
<td>Endurance</td>
</tr>
<tr>
<td></td>
<td>Ultra-low digital logic</td>
<td>Slow speed, scalability</td>
</tr>
<tr>
<td>Junctionless FET</td>
<td>CMOS process compatibility</td>
<td>Worse gate control in short-channel</td>
</tr>
<tr>
<td>Spin FET</td>
<td>Low power, suitable for memory (nonvolatile info storage)</td>
<td>Low efficiency of spin injection</td>
</tr>
</tbody>
</table>
Conclusions
Conclusions

- New device structures (FinFET, Tri-gate) are replacing conventional Planar CMOS.
  - Same performance at lower supply voltage
- HKMG: Continuous innovation has enabled EOT scaling to 9 Å, however, new material could be needed for further EOT scaling.
  - La-based high-k material
- Recent advances in new channel material shows promising device performances but still far to catch up Si-CMOS.
  - The combination of III-V channel materials with a multi-gate structure appears to be a promising direction.
    (Higher performance in lower operating voltage)
- Device demonstration on emerging technologies (such as Tunnel FET, Junctionless FET, Carbon-based FET..) is increasing, But more time is needed for implementation of these technologies in future generation devices as mature technologies.
- $L_g = 14\text{nm}$ Tri-Gate NW
- High SCE immunity at $L_g$ of 14nm
- $V_{th}$ tuning by applying $V_{sub}$ with thin BOX of 20nm

Vth control by back-gate bias
- $L_g = 20$nm bulk planar CMOS
- Gate last integration
- In-situ doped S/D for better SCE

Planar still works well at 20nm
Gate All Around Nanowire (GAA NW)

- Gate all around structure
- $L_g$ of 22~30nm
- Bulk wafer-based integration
- High drive currents by special stress and channel orientation design
Tri-gate $I_{ON}$ and $I_{OFF}$ characteristics

C.-H. Jan et al., pp.44, IEDM2012 (Intel)

<table>
<thead>
<tr>
<th>$I_{ON}$ (mA/um)</th>
<th>HP</th>
<th>SP</th>
<th>LP</th>
<th>ULP</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS/PMOS</td>
<td>1.08/0.91</td>
<td>0.71/0.59</td>
<td>0.41/0.37</td>
<td>0.35/0.33</td>
</tr>
<tr>
<td>$I_{OFF}$</td>
<td>100nA/um</td>
<td>1 nA/um</td>
<td>30 pA/um</td>
<td>15 pA/um</td>
</tr>
<tr>
<td>$I_{ON}/I_{OFF}$</td>
<td>$\approx 10^5$</td>
<td>$\approx 10^6$</td>
<td>$\approx 10^8$</td>
<td>$\approx 10^8$</td>
</tr>
</tbody>
</table>

$V_{dd} = 0.75$ V

$I_{ON}/I_{OFF} > 10^5$
For the past 45 years, SiO2 and SiON have been used as gate insulators. Today, EOT=1.0nm. The EOT limit is 0.7~0.8 nm.

The EOT can be reduced further beyond 0.5 nm by using direct contact to Si by choosing appropriate materials and processes. 

One order of magnitude can be achieved.

Introduction of High-k materials and processes.