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More Moore approach
- Technology benchmark
- Advance Si-based CMOS devices and technologies
- Challenges

Alternative channel material devices
- Technology benchmark
- III-V, Ge-based devices

Emerging technologies
(Tunnel FET, Junctionless FET, Carbon-based FET, MEMS, Spin-based Logic)

Conclusions
More Moore approach

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Conclusions
More Moore to More More Moore

Technology node

<table>
<thead>
<tr>
<th>Now</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td>65nm</td>
<td>15nm, 11nm, 8nm, 5nm, 3nm</td>
</tr>
<tr>
<td>45nm</td>
<td></td>
</tr>
<tr>
<td>32nm</td>
<td></td>
</tr>
<tr>
<td>22nm</td>
<td></td>
</tr>
</tbody>
</table>

Lg 35nm

Main stream
(Fin,Tri, Nanowire)

Si is still main stream for future !!

Si channel

ET: Extremely Thin

Planar

Tri-Gate

Alternative

Emerging Devices

Alternative (III-V/Ge)

Channel FinFET

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)
High-k gate dielectrics

Hf-based oxides

<table>
<thead>
<tr>
<th>Thickness</th>
<th>EOT</th>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
<th>15nm, 11nm, 8nm, 5nm, 3nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>EOT</td>
<td></td>
<td>1nm</td>
<td>0.95nm</td>
<td>0.9nm</td>
<td></td>
</tr>
</tbody>
</table>

SiO₂ IL (Interfacial Layer) is used at Si interface to realize good mobility.

Technology for direct contact of high-k and Si is necessary:
- EOT=0.52 nm
- Remote SiO₂-IL scavenging HfO₂ (IBM)

continued research and development

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM2009, (IBM)
**I_{ON} and I_{OFF} benchmark**

### NMOS

- **Intel [1]**
  - Bulk 32nm Tri-Gate 22nm
  - $V_{DD}=0.8V$
  - $V_{DD}=1V$
- **Samsung [3]**
  - Bulk 20nm
  - $V_{DD}=0.9V$
- **Tokyo Tech. [9]**
  - Ω-gate NW
  - $V_{DD}=1V$
- **IBM [5]**
  - ETSOI
  - $V_{DD}=0.9V$
- **IBM [6]**
  - FinFET 25nm
  - $V_{DD}=1V$
- **STMicro. [8]**
  - GAA NW
  - $V_{DD}=1.1V$
- **IBM [10]**
  - ETSOI
  - $V_{DD}=1V$

### PMOS

- **Intel [1]**
  - Bulk 32nm Tri-Gate 22nm
  - $V_{DD}=0.8V$
  - $V_{DD}=1V$
- **Samsung [3]**
  - Tri-Gate NW
  - $V_{DD}=1V$
- **IBM [7]**
  - ETSOI
  - $V_{DD}=0.9V$
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  - FinFET 25nm
  - $V_{DD}=1V$
- **STMicro. [8]**
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  - $V_{DD}=1.1V$
- **IBM [10]**
  - ETSOI
  - $V_{DD}=0.9V$

---

\( L_g \) and EOT are larger than ITRS requirements

Implementation of Tri-gate and lower \( V_{th}/V_{dd} \) since 22nm

*K. Mistry et al., pp.247, IEDM2007 (Intel).*

*P. Packan et al., pp.659, IEDM2009 (Intel).*

*C. Auth et al., pp.131, VLSI2012 (Intel).*
### Benchmark of device characteristics

<table>
<thead>
<tr>
<th>Structure</th>
<th>Bulk Planar</th>
<th>Tri-Gate</th>
<th>Tri-Gate NW</th>
<th>ETSOI</th>
<th>Bulk Planar</th>
<th>GAA NW</th>
<th>GAA NW</th>
<th>Ω-gate NW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lg (nm)</td>
<td>35</td>
<td>30</td>
<td>30</td>
<td>14</td>
<td>22</td>
<td>20</td>
<td>35/25</td>
<td>22/30</td>
</tr>
<tr>
<td>Gate Dielectrics</td>
<td>Hf-based</td>
<td>Hf-based</td>
<td>SiO₂</td>
<td>HfO₂</td>
<td>HfO₂</td>
<td>Hf-based</td>
<td>HfZrO₂</td>
<td>SiO₂</td>
</tr>
<tr>
<td>EOT (nm)</td>
<td>1</td>
<td>0.95</td>
<td>0.9</td>
<td>3</td>
<td>~1</td>
<td>-</td>
<td>1.5</td>
<td>-</td>
</tr>
<tr>
<td>Vth (V)</td>
<td>~0.4</td>
<td>~0.3</td>
<td>~0.2</td>
<td>-0.15 (nFET)</td>
<td>0.3~0.4</td>
<td>~0.3</td>
<td>0.3~0.4</td>
<td>~0.5</td>
</tr>
<tr>
<td>VDD (V)</td>
<td>1</td>
<td>1</td>
<td>0.8</td>
<td>1</td>
<td>0.9</td>
<td>0.9</td>
<td>1</td>
<td>1.1</td>
</tr>
<tr>
<td>ION (mA/um) (nFET/pFET)</td>
<td>1.36/1.07</td>
<td>1.53/1.23</td>
<td>1.26/1.1</td>
<td>0.83 (nFET)</td>
<td>0.59/0.62 (I_eff)</td>
<td>1.2/1.05</td>
<td>0.83/0.95</td>
<td>2.05/1.5</td>
</tr>
<tr>
<td>DIBL (mV/V) (nFET/pFET)</td>
<td>~150</td>
<td>~200</td>
<td>46/50</td>
<td>&lt;50</td>
<td>-</td>
<td>104/115</td>
<td>65/105</td>
<td>56/9</td>
</tr>
<tr>
<td>SS (mV/dec)</td>
<td>-</td>
<td>~100</td>
<td>~70</td>
<td>&lt;80</td>
<td>-</td>
<td>87</td>
<td>85</td>
<td>&lt;80</td>
</tr>
</tbody>
</table>
Short-channel effect

\[ \text{SCE} = 0.64 \frac{\varepsilon_s}{\varepsilon_{ox}} \times EI \times \Phi_d \]

\[ \text{DIBL} = 0.8 \frac{\varepsilon_s}{\varepsilon_{ox}} \times EI \times V_{ds} \]

\[
\begin{align*}
E_I &= 1 \times \\
&\left(1 + \frac{X_j^2}{L_{el}^2}\right) \\
&\times \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} \\
E_I &= 1 \times \\
&\left(1 + \frac{T_{si}^2}{L_{el}^2}\right) \\
&\times \frac{T_{ox}}{L_{el}} \frac{T_{si} + \lambda T_{box}}{L_{el}} \\
E_I &= 1 \times \\
&\left(1 + \frac{T_{si}^2}{L_{el}^2}\right) \\
&\times \frac{T_{ox}}{L_{el}} \frac{T_{si}}{L_{el}} \\
E_I &= 1 \times \\
&\left(1 + \frac{T_{si}^2}{4 L_{el}^2}\right) \\
&\times \frac{T_{ox}}{L_{el}} \frac{T_{si}}{L_{el}} \\
E_I &= 1 \times \\
&\left(1 + \frac{T_{si}^2}{2 L_{el}^2}\right) \\
&\times \frac{T_{ox}}{L_{el}} \frac{T_{si}}{L_{el}}
\end{align*}
\]

if max ch. doping is 10^{19} \text{cm}^{-3} \Rightarrow T_{ep} \approx 12 \text{nm} then:

\[ X_j = 145 \text{nm} \]
\[ \lambda T_{box} = 18 \text{nm} \]

if Tsi min \approx 3 \text{nm} then:

\[ T_{box} = 10 \text{nm} \]
\[ \lambda T_{box} = 3 \text{nm} \]

if Tsi min \approx 3 \text{nm} then:

\[ T_{box} = 10 \text{nm} \]
\[ \lambda T_{box} = 0.46 \text{nm} \]

\[ \approx 0 \text{nm} \]

Tsi/2 plays role of Xj, and that of Tdep, if minimum feasible Tsi is supposed 3nm, then:

\[ T_{box} = 10 \text{nm} \]
\[ \lambda T_{box} = 3 \text{nm} \]

\[ \approx 0 \text{nm} \]

LeL,min

(DIBL=100mV/V)

=34nm

LeL,min

(DIBL=100mV/V)

= 34nm

LeL,min

(DIBL=100mV/V)

≈ 30nm

LeL,min

(DIBL=100mV/V)

≈ 10nm

LeL,min

(DIBL=100mV/V)

≈ 6nm

LeL,min

(DIBL=100mV/V)

≈ 2.7nm
Drain-induced barrier lowering

\[ DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{DS} \]

T. Skotnicki, IEDM 2010 Short Course (STMicroelectronics)

- BULK: 140mV/V
- III-V: 210mV/V
- ETSOI: 110mV/V
- UTBB: 80mV/V
- FinFET: 70mV/V

- \( T_{dep} = T_{si} + \lambda T_{box} \)
- \( X_j = T_{si} \geq 6\text{nm} \)
- \( T_{dep} = T_{si}/2 \)
- \( X_j = T_{si}/2 \)
- \( T_{si} \geq 10\text{nm} \)

- \( \varepsilon_{si} + 15\% \)
- \( T_{ox} + 2\% \)
Sub-threshold Slope

\[ S = \frac{kT}{q} \ln \left( 1 + \frac{C_{\text{dep}}}{C_{\text{ox}}} + \frac{\varepsilon_{\text{Si}} T_{\text{ox}} X_j}{\varepsilon_{\text{ox}} L_{\text{el}} L_{\text{el}}} \left( 1 + \frac{3T_{\text{dep}}}{4 L_{\text{el}}} \right) \sqrt{1 + 2 \frac{V_{ds}}{\Phi_d}} \right) \]

- **BULK**
  - \( X_j = 3/4L_{\text{el}} \)
  - \( T_{\text{dep}} = 3/4L_{\text{el}} \)
  - 95 mV/dec

- **III-V**
  - \( T_{\text{ox}} + 2\varepsilon_{\text{Si}} + 15\% \)
  - 110 mV/dec

- **FDSOI**
  - \( T_{\text{dep}} = T_{\text{si}}/2 \)
  - \( X_j = T_{\text{si}}/2 \)

- **ETSOI**
  - 85 mV/dec

- **UTBB**
  - 75 mV/dec

- **FinFET**
  - 65 mV/dec

**Notes:**
- Sub-threshold Slope
- Log(\( I_d \)) vs. \( V_g \)
- \( \Delta S \): Subthreshold Slope
- \( T_{\text{dep}} = T_{\text{si}} + \Lambda T_{\text{box}} \)
- \( X_j = T_{\text{si}} \)
- \( T_{\text{dep}} = T_{\text{si}}/2 \)
- \( X_j = T_{\text{si}}/2 \)
- RBB => Pstat
Outline

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- Conclusions
Tri-gate implementation for transistors

C. Auth et al., pp.131, VLSI2012 (Intel)

<table>
<thead>
<tr>
<th></th>
<th>HP</th>
<th>MP</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{OX,E}$ (nm)</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>$L_{GATE}$ (nm)</td>
<td>30</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>$I_{OFF}$ (nA/um)</td>
<td>20-100</td>
<td>5-20</td>
<td>1-5</td>
</tr>
</tbody>
</table>

Tri-gate has been implemented since 22nm node, enabling further scaling
A fin width of 8nm to balance SCE and $R_{\text{ext}}$
A fin height of 34nm to balance drive current vs. capacitance
- SS of 71 and 72 mV/dec for HP NMOS and PMOS, respectively
- DIBL of 30 and 35 mV/V for NMOS and PMOS, respectively
- \(V_{th}\) of 22 nm is about 0.1 ~0.2 V lower than that of 32nm
Tri-gate $I_{ON}$ and $I_{OFF}$ characteristics

C.-H. Jan et al., pp.44, IEDM2012 (Intel)

<table>
<thead>
<tr>
<th>NMOS/PMOS</th>
<th>HP</th>
<th>SP</th>
<th>LP</th>
<th>ULP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ON}$ (mA/um)</td>
<td>1.08/0.91</td>
<td>0.71/0.59</td>
<td>0.41/0.37</td>
<td>0.35/0.33</td>
</tr>
<tr>
<td>$I_{OFF}$</td>
<td>100nA/um</td>
<td>1 nA/um</td>
<td>30 pA/um</td>
<td>15 pA/um</td>
</tr>
<tr>
<td>$I_{ON}/I_{OFF}$</td>
<td>$\sim 10^5$</td>
<td>$\sim 10^6$</td>
<td>$\sim 10^8$</td>
<td>$\sim 10^8$</td>
</tr>
</tbody>
</table>

$V_{dd} = 0.75$ V

$I_{ON}/I_{OFF} > 10^5$
- $L_g = 14\text{nm}$ Tri-Gate NW
- High SCE immunity at $L_g$ of $14\text{nm}$
- $V_{th}$ tuning by applying $V_{sub}$ with thin BOX of $20\text{nm}$
\( L_g = 20\text{nm} \) bulk planar CMOS

- Gate last integration
- In-situ doped S/D for better SCE
Extremely Thin SOI (ETSOI)

K. Cheng et al., pp.419, IEDM2012 (IBM)

- Hybrid CMOS
- Si Channel nFET
- Strained SiGe Channel pFET
- RO delay improvement over FinFET with FO = 2
\[ L_g = 25\text{~to~}35\text{nm} \text{ GAA NW} \]

- Hydrogen anneal provide smooth channel surface
- Competitive with conventional CMOS technologies
- Scaling the dimensions of NW leads to suppressed SCE
Gate All Around Nanowire (GAA NW)

- Gate all around structure
- $L_g$ of 22~30nm
- Bulk wafer-based integration
- High drive currents by special stress and channel orientation design
Ω-gate Si Nanowire

S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.)

- Conventional CMOS process
- High drive current
  (1.32 mA/µm @ I_{OFF}=117 nA/µm)
- DIBL of 62mV/V and SS of 70mV/dec for nFET
• **More Moore approach**
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• **Challenges**
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    - III-V, Ge-based devices
  - **Emerging technologies**
    (Tunnel FET, Junctionless FET, Carbon-based FET, MEMS, Spin-based Logic)

• Conclusions
Decreasing the diameter of NW

- Improved short-channel control
- Severe mobility degradation
Problems in SOI

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.

![Graph showing Mobility vs. SOI thickness for nMOS and pMOS transistors.](image)
Impact of Si thickness in FinFET

- Replacement Gate process
- TaN/HfO₂ gate stack
- Reduced $g_m$ and higher $V_{th}$ with decreasing Fin width
Significant increase in $V_{th}$ variability with decreasing Fin width.
Smaller wire/fin width is necessary for SCE suppression

But mobility and $I_{ON}$ severely degrade with wire/fin width reduction

Therefore even in multi-gate structures EOT scaling could be accelerated to provide SCE immunity
Advantages of metal S/D
- atomically abrupt junction
- low parasitic resistance
- reduced channel dopant concentration

Issues in metal S/D
- two different $\phi_B$ for p/n-ch FETs
- underlap/overlap to the gate
- narrow process temperature window

Metal S/D is considered for alternative channel material such as InGaAs and Ge

Ni is used both on InGaAs and Ge to form alloy.

S.-H. Kim, IEDM (2010) 596
K. Ikeda, VLSI (2012) 165
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- Conclusions
### Ge, III-V bulk properties

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>electron mob. (cm²/Vs)</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
</tr>
<tr>
<td>electron effective mass (/m₀)</td>
<td>mₑ: 0.19</td>
<td>mₑ: 0.082</td>
<td>mₑ: 0.067</td>
<td>0.08</td>
<td>0.026</td>
<td>0.0135</td>
</tr>
<tr>
<td>hole mob. (cm²/Vs)</td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td>hole effective mass (/m₀)</td>
<td>m_HH: 0.49</td>
<td>m_HH: 0.28</td>
<td>m_HH: 0.45</td>
<td>m_HH: 0.45</td>
<td>m_HH: 0.57</td>
<td>m_HH: 0.44</td>
</tr>
<tr>
<td>band gap (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.14</td>
</tr>
<tr>
<td>permittivity</td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

- Ge ⇒ lightest hole $m^*$ (light electron $m^*$) ⇒ pMOS (CMOS)
- III-V ⇒ light electron $m^*$ ⇒ nMOS
- GaAs·InP ⇒ $E_g$ higher than that in Si ⇒ low power

*S. Takagi, IEDM2011, Short course (Tokyo Uni)*
**Multi-gate III-V and Si benchmark**

**nMOS**

- InGaAs GAA
  - \(L_g=50\) nm, Dielectric: 10nm \(\text{Al}_2\text{O}_3\)
  - \(V_{DS}=0.5\) V (Purdue Uni.) [1]

- Si-FinFET 32nm
  - \(V_{DD}=0.8\) V [10]

- InGaAs Tri-gate
  - \(L_g=60\) nm, EOT 12A
  - \(V_{DS}=0.5\) V (Intel) [2]

- Si-FinFET 22nm
  - \(V_{DD}=0.8\) V [10]

- Si-bulk 45nm
  - \(V_{DD}=1\) V [11]

- InGaAs FinFET
  - \(L_{ch}=130\) nm
  - EOT 3.8nm
  - \(V_{DS}=0.5\) V (NUS) [3]

- InGaAs Nanowire
  - \(L_g=200\) nm, \(T_{ox} 14.8\) nm
  - \(V_{DS}=0.5\) V (Hokkaido Uni.) [4]

- Metal S/D InGaAs-OI
  - \(L_{ch}=55\) nm, EOT 3.5nm
  - \(V_{DS}=0.5\) V (Tokyo Uni.) [5]

**pMOS**

- GOI Tri-gate
  - \(L_g=65\) nm, EOT 3.0nm
  - \(V_{DS}=-1\) V (AIST Tsukuba) [6]

- Si-FinFET 32nm
  - \(V_{DD}=0.8\) V [10]

- Ge FinFET
  - \(L_g=4.5\) mm
  - Dielectric: SiON, \(V_{DS}=-1\) V (Stanford Uni.) [7]

- Si-FinFET 22nm
  - \(V_{DD}=0.8\) V [10]

- Si-bulk 45nm
  - \(V_{DD}=1\) V

- Ge GAA \(L_g=300\) nm,
  - Dielectric: GeO\(_2\)(7nm)-HfO\(_2\)(10nm)
  - \(V_{DS}=-0.8\) V (ASTAR Singapore) [8]

- Ge Tri-gate
  - \(L_g=183\) nm, EOT 5.5nm
  - \(V_{DS}=-1\) V (NNDL Taiwan) [9]

- Si-bulk 45nm
  - \(V_{DD}=1\) V

**References**

$I_{ON}/I_{OFF}$ Benchmark of Ge pMOSFET

K. J. Kuhn, ECS Transactions, 33 (6) 3-17 (2010)

Optimization of short channel Ge p-MOSFETs is still under investigation
### III-V/Ge benchmark for various structures

<table>
<thead>
<tr>
<th>Material</th>
<th>Planar (metal S/D, Strain, Buffer...)</th>
<th>FinFET</th>
<th>Tri-gate</th>
<th>Gate-all-around MOSFET</th>
<th>Nanowire</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric/EOT</td>
<td>$\text{Al}_2\text{O}_3/3.5\text{ nm}$</td>
<td>$7.6\text{ A}^0_{\text{HfO}_2+\text{Al}_2\text{O}_3+\text{GeO}_2}$</td>
<td>$5\text{ nm ALD }\text{Al}_2\text{O}_3$</td>
<td>$5\text{ nm ALD }\text{Al}_2\text{O}_3$</td>
<td>$1.2\text{ nm }\text{SiON}$</td>
</tr>
<tr>
<td>Mobility</td>
<td>-</td>
<td>$\sim600\text{ (cm}^2/\text{Vs})$</td>
<td>$N_e:5\times10^{12}$</td>
<td>$e:200$</td>
<td>$h:400$</td>
</tr>
<tr>
<td>$L_{ch}\text{ (nm)}$</td>
<td>55</td>
<td>$W/L=30/5\mu\text{m}$</td>
<td>50 $\mu\text{m}$</td>
<td>100</td>
<td>4.5 $\mu\text{m}$</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>84</td>
<td>-</td>
<td>-</td>
<td>180</td>
<td>-</td>
</tr>
<tr>
<td>SS (mV/dec)</td>
<td>105</td>
<td>-</td>
<td>-</td>
<td>$150\text{K}$</td>
<td>$61\text{pMOS}$</td>
</tr>
<tr>
<td>$I_{ON}\text{ (}\mu\text{A}/\mu\text{m)}$</td>
<td>278</td>
<td>3</td>
<td>$4\text{ (n,p)}$</td>
<td>$4\text{ (n,p)}$</td>
<td>$10\text{ (V}_{0}\approx0.5\text{V)}$</td>
</tr>
</tbody>
</table>
• More Moore approach
  • Technology benchmark
  • Advance Si-based CMOS devices and technologies
  • Challenges

• **Alternative channel material devices**
  • Technology benchmark

• **III-V, Ge-based devices**

• Emerging technologies
  (Tunnel FET, Junctionless FET, Carbon-based FET, MEMS, Spin-based Logic)

• Conclusions
Achieving both N- and P-type MOSFET on a single channel is possible

- In-content of 20-40% improves performance
- Electron/hole mobility > 4000/900 cm²/Vs was gained in a single channel material

\[ I_{ON} \text{ at } L_G = 50 \ \mu m \]
- pMOS: 4 \( \mu A/\mu m \)
- nMOS: 3.8 \( \mu A/\mu m \)
Metal S/D and InAs buffer layer are used as performance boosters.

- DIBL=84 mV/V and SS=105 mV/V was shown for $L_{ch} = 55$ nm when In-content was higher.

S. H. Kim et al., pp.177, VLSI2012 (Tokyo Uni)
Common InGaAs-GeSn gate stack (NUS)

- Common gate stack (gate metal and dielectric) were used for both p- and n-type

- Si$_2$H$_6$ plasma passivation is employed which creates Si layer at interface.

  \[ SS: \text{nMOS:} \ 90 \ (mV/\text{decade}) \]

  \[ p\text{MOS:} \ 190 \ (mV/\text{decade}) \]

- High intrinsic peak \( G_{M,Sat} \) of \(~465\) \( S/\mu m \) at \( V_{DS}=-1.1 \) V was achieved for \( L_G=250 \) nm.
Core-multishell InGaAs nanowires grown without buffer layer on Si substrate (bottom up approach)

At $V_d = 1$ V peak transconductance of 500 mS/mm is achieved (roughly $x3$ InGaAs nanowire)
Tri-gate structure has superiority in electrostatic controllability compared to ultra-thin body planar structure.

Steepest SS and smallest DIBL ever reported ($W_{\text{fin}} = 30\text{nm}$)

Inversion mode $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFET with ALD $\text{Al}_2\text{O}_3$/WN with well electrostatic properties

DIBL was suppressed down to $L_{\text{ch}} = 50\text{nm}$ and $G_{m,\text{max}} = 701\text{mS/mm}$ at $V_{ds} = 1\text{V}$
DIBL = 135 mV/V and drive current over 840 μA/μm at \( L_{\text{ch}} = 130\text{nm} \) and \( V_{ds} = 1.5\text{V} \) was achieved.
Ge-nanowire pMOSFET (AIST, Tsukuba)


Using Ni-Ge alloy as metal S/D

Significantly reduces contact resistance

High saturation current and high mobility

\( \mu_{\text{eff}} = 855 \text{ cm}^2/\text{Vs} \) at \( N_s = 5 \times 10^{12} \text{cm}^{-2} \)
and saturation drain current of

731 \( \mu \text{A/\mu m} \) at \( V_d = -1 \text{V} \)

\( L_g = 65 \text{nm} \)
\( W_{\text{wire}} = 20 \text{nm} \)
Selective etching of high defect Ge near Ge/Si interface is used which improves gate controllability.

$I_{ON}/I_{OFF} = 10^5$ and SS= 130 mV/dec
And $I_{ON}= 235 \mu m/\mu m$ at $V_D= -1V$
III-V (InGaAs, InAs, InGaSb, …)

- ALD-Al$_2$O$_3$ is most commonly used as gate dielectric in planar or Multi-gate
- HfO$_2$-only stacks have high $D_{it}$ (combination of Al$_2$O$_3$ or Al or Si is used)

Implementing high-$k$ material to III-V, Ge

- By controlling the formation of GeO$_x$ at the interface, HfO$_2$ and Al$_2$O$_3$ show good results.

E. Kim, et al., APL 96, 012906

L. Chu, et al., APL 99, 042908

Hokkaido Uni, IEDM 2011

Intel, IEDM 2010

R. Zhang et al., VLSI 2012, p161
Outline

- More Moore approach
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- Alternative channel material devices
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- Emerging technologies
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- Conclusions
Emerging devices (future scaling trends)

Carbon-based FET

Carbon nanotube

Graphene

GaAs mHEMT

SiMOSFET (29nm)

GaAs pHEMT (100nm)

CNT

Graphene

Junctionless Transistor

All-spin logic device

Input and output related via Spin-coherent channel

M. Lemme, Nanotech workshop, 2012

A. D. Franklin et al., pp.525, IEDM2011 (IBM)

J. P. Colinge et al., Nature Nano. 5(2010)225

J. P. Colinge et al., Nature Nano. 5(2010)266
Tunnel FET

Low $I_{OFF}$, Low $V_{DD}$, SS<60mV/decade
TFET vs. MOSFET at low $V_{DD}$

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

- **EOT = 1 nm**
- **$LG = 20$ nm**
- **$tlnAs = 5$ nm**

<table>
<thead>
<tr>
<th>TFET @0.35V</th>
<th>Stage Delay (ps)</th>
<th>Switching Energy (fJ)</th>
<th>Leakage Power (nW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV (FO=3)</td>
<td>105</td>
<td>0.26</td>
<td>0.37</td>
</tr>
<tr>
<td>NAND (FO=3)</td>
<td>149</td>
<td>0.32</td>
<td>0.57</td>
</tr>
<tr>
<td>NOR (FO=3)</td>
<td>158</td>
<td>0.34</td>
<td>0.54</td>
</tr>
<tr>
<td>Combined</td>
<td>129</td>
<td>0.29</td>
<td>0.46</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CMOS @0.3V</th>
<th>Stage Delay (ps)</th>
<th>Switching Energy (fJ)</th>
<th>Leakage Power (nW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV (FO=3)</td>
<td>830</td>
<td>0.25</td>
<td>0.37</td>
</tr>
<tr>
<td>NAND (FO=3)</td>
<td>1364</td>
<td>0.32</td>
<td>0.56</td>
</tr>
<tr>
<td>NOR (FO=3)</td>
<td>1389</td>
<td>0.33</td>
<td>0.53</td>
</tr>
<tr>
<td>Combined</td>
<td>1103</td>
<td>0.29</td>
<td>0.46</td>
</tr>
</tbody>
</table>

- $V_{DD}$ 0.3~0.35V
- TFET 8x faster at the same power
- "parameter variation is not a significant factor for differentiation between MOSFET and TFET"
X in Si$_{1-x}$Ge$_x$ is optimized to allow for efficient BTBT

$L_G = 200$nm

$I_{ON}/I_{OFF} \approx 10^5$

Reducing SiGe Body thickness improves Subthreshold swing.

130mV/dec

190mV/dec
SS of TFET is function of $V_G$ due to Zener tunnel current

Minimum SS = 21 mV/dec is reached due to optimized series resistance of contact, undoped InAs and InAs/Si

$I_{ON}/I_{OFF} \sim 10^6$ at $V_{DS} = 1.0V$ ($I_{ON} = 1A_{\mu A/\mu m}$)
Device structure

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

Device structure

tunneling // to the gate
oblique to the gate field

tunneling ⊥ to the gate
in-line with the gate field

nanowire TFET
gate-all-around - best electrostatics

K. Tomioka et al., pp.47, VLSI2012 (Hokkaido University)
### Tunnel FET performance comparison

**measured III-V channel TFETs**

<table>
<thead>
<tr>
<th>Reference</th>
<th>Source</th>
<th>Channel</th>
<th>Dielectric</th>
<th>EOT (nm)</th>
<th>$I_{ON}$ ($\mu A/\mu m$)</th>
<th>$V_{DS}$ (V)</th>
<th>$V_{GS} = V_{ON}$ (V)</th>
<th>$V_{ON} - V_{OFF}$ (V)</th>
<th>$I_{ON}/I_{OFF}$</th>
<th>$S_{MIN}$ (mV/dec)</th>
<th>$S_{EFF}$ (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>this work</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.6</td>
<td>78</td>
<td>0.5</td>
<td>0.5</td>
<td>1.5</td>
<td>2,000</td>
<td>125</td>
<td>230</td>
</tr>
<tr>
<td>Li [4]</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$</td>
<td>3.9</td>
<td>20</td>
<td>0.3</td>
<td>2</td>
<td>6</td>
<td>210</td>
<td>830</td>
<td>1300</td>
</tr>
<tr>
<td>Mookerjea [5]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>5.6</td>
<td>10</td>
<td>0.5</td>
<td>2.5</td>
<td>2.5</td>
<td>10,000</td>
<td>240</td>
<td>310</td>
</tr>
<tr>
<td>Mohata [6]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>2.8</td>
<td>10</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>400,000</td>
<td>200</td>
<td>180</td>
</tr>
<tr>
<td>Zhao [7]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>20</td>
<td>0.45</td>
<td>1</td>
<td>1.5</td>
<td>30,000</td>
<td>86</td>
<td>170</td>
</tr>
<tr>
<td>Zhao [8]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>40</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>200,000</td>
<td>84</td>
<td>190</td>
</tr>
<tr>
<td>Ford [9]</td>
<td>InAs</td>
<td>InAs</td>
<td>ZrO$_2$</td>
<td>2</td>
<td>0.4</td>
<td>0.5</td>
<td>1</td>
<td>1</td>
<td>200</td>
<td>190</td>
<td>220</td>
</tr>
<tr>
<td>Zhou [10]</td>
<td>InP</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$,As</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.3</td>
<td>20</td>
<td>0.5</td>
<td>1</td>
<td>1.75</td>
<td>450,000</td>
<td>93</td>
<td>150</td>
</tr>
</tbody>
</table>

- **$S_{MIN}$**: Most common SS which is the inverse of $I_D$-$V_{GS}$ slope at the steepest part
- **$S_{EFF}$**: Is the average swing when $V_{TH}=V_{DD}/2$, $V_{OFF}=0$

**Average SS**: 

$$V_{TH} - V_{OFF}$$ 

$$\log(I_D/I_{OFF})$$

**Effective SS**: 

$$V_{DD}$$ 

$$2 \log(I_D/I_{OFF})$$
I\textsubscript{ON} and I\textsubscript{OFF} of TFETs

[1] G. Zhou et al., pp. 782, vol. 33, no. 6, EDL 2012 (University of Notre Dame)

C. Auth et al., pp.131, VLSI2012 (Intel).
K. Mistry et al., pp.247, IEDM2007 (Intel).
MEMS relay

- ON-state resistance (Ohm)
- Number of Operation Cycles
- I_{ON}/I_{OFF} of \sim 10^{10}
- Ultra-low-power digital logic applications.
- Frequency of 1, 5, 25kHz under operation

T. K. Liu et al., pp. 43, VLSI2012 (UC Berkeley)
Si Junctionless Transistor (Intel)

R. Rios et al., EDL. 32(2011)1170

- **IM**: Conventional Inversion Mode
- **JAM LD**: Junctionless Accumulation Mode with low dope
- **JAM HD**: Junctionless Accumulation Mode with high dope

- JAM devices have **reduced gate control** and **degraded short-channel** characteristics relative to IM

- Not suitable for high-performance logic (high $I_{on}$ and moderate $I_{off}$)
Near-ideal subthreshold slope, close to 60 mV/dec at room temperature, and extremely low leakage currents

- Silicon nanowire is uniformly doped
- Gate material is opposite polarity polysilicon

\[ I_{ON}/I_{OFF} \approx 1 \times 10^6 \quad (-1 < V_g < 1) \]

\[ I_{OFF} \text{ is smaller than } 10^{-15} \text{ A} \]
SWCNT : single wall carbon nanotube  
GNR : graphene nano ribbon

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>SWCNT</th>
<th>GNR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mobility cm²/V/s</td>
<td>1400</td>
<td>&gt;10000</td>
<td>&gt;10000 for large widths</td>
</tr>
<tr>
<td></td>
<td></td>
<td>J. Of Physics, Cond. Matter, 2004</td>
<td>200 for W&lt;10nm</td>
</tr>
<tr>
<td>Mean free path (nm) @ room temp</td>
<td>30</td>
<td>&gt;1,000</td>
<td>~1,000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>~10nm for W&lt;10nm</td>
</tr>
<tr>
<td>Thermal conductivity (W/mK)</td>
<td>150</td>
<td>5800</td>
<td>~5000</td>
</tr>
</tbody>
</table>

Carbon materials for FET applications  
• an ultra-thin body for aggressive channel length scaling  
• excellent intrinsic transport properties similar to carbon nanotubes  
• pattern the desired device structures
Transistor operation with $L_{ch}$ of 9nm
Graphene Field-effect Transistor

- Ambipolar Characteristics
- Bi-layer graphene and double gates can open the gap
2D material: single layer MoS$_2$

- Mobility of $190 \text{ cm}^2/\text{Vsec}$
- $I_{on}$ of $1 \mu\text{A}/\mu\text{m}$ at $V_{DD} = 1\text{V}$
- Candidate: MoS$_2$, MoSe$_2$, WS$_2$, WSe$_2$, MoTe$_2$, WTe$_2$
Magnetic tunnel junction on S/D

Read/write are enabled by using ferromagnetic electrodes and Spin-polarized current
## Summary of Emerging Technology pros/cons

<table>
<thead>
<tr>
<th>Technology</th>
<th>Advantage</th>
<th>Issues</th>
</tr>
</thead>
</table>
| TFET             | Lower $V_{dd}$  
                 Lower $I_{OFF}$                        | Integration  
                 higher $I_{ON}$                        |
| CNT FET          | Higher transport velocity  
                  $L_g$ scaling                            | High density and  
                  alignment, reproducibility,  
                  integration                                |
| Graphene FET     | RF application  
                  Large area manufacturing                  | NOT a direct replacement  
                  for Silicon logic                           |
| MEMS             | Extremely low leakage  
                  Ultra-low digital logic                  | Endurance  
                  Slow speed, scalability                    |
| Junctionless FET | CMOS process compatibility                    | Worse gate control in  
                  short-channel                                |
| Spin FET         | Low power, suitable for memory (nonvolatile info storage) | Low efficiency of spin injection |
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• Conclusions
Conclusions

- New device structures (FinFET, Tri-gate) are replacing conventional Planar CMOS
  - Same performance at lower supply voltage

- HKMG: Continuous innovation has enabled EOT scaling to 9 Å, however, new material could be needed for further EOT scaling.
  - La-based high-k material

- Recent advances in new channel material shows promising device performances comparable to state of the art Si-based MOSFETs.
  - The combination of III-V channel materials with a multi-gate structure appears to be a promising direction. (Higher performance in lower operating voltage)

- Device demonstration on emerging technologies (such as Tunnel FET, Junctionless FET, Carbon-based FET..) is increasing, But more time is needed for implementation of these technologies in future generation devices as mature technologies.