High-k/Metal Gate and New Channel Material Technologies

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Introduction

High-k/metal gate on Si channel
  - Gate first/last processes
  - Threshold voltage
  - Mobility
  - Reliability
  - EOT reduction toward 0.5 nm
  - Atomic layer deposition (ALD)
  - Benchmark

New channel materials

Some conclusions
Outline

- **Introduction**
  - High-k/metal gate on Si channel
    - Gate first/last processes
    - Threshold voltage
    - Mobility
    - Reliability
    - EOT reduction toward 0.5 nm
    - Atomic layer deposition (ALD)
    - Benchmark
  - New channel materials
  - Some conclusions
Downscaling of MOSFET

$L_g$: Gate length, $W_g$: Gate width, $t_{ox}$: Gate oxide thickness, $V_{dd}$: Supply voltage

$L_g$, $W_g$, $t_{ox}$, $V$ shrink with same factor $k \approx 0.7$ about every 3 years

Drain current: $I_d = \nu_{inj} W_g C_o (V_g-V_{th}) = W_g t_{ox}^{-1} (V_g-V_{th}) = KK^{-1}K = K$

Gate Capacitance: $C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox} = KK/K = K$

Switching time: $\tau = C_g V_{dd} / I_d = KK/K = K$

Clock frequency: $f = 1/\tau = 1/K$

Power for MOSFET: $P = f CV^2/2 = K^{-1}K (K^1)^2 = K^2$

$(P \text{ per cycle } = CV^2/2 = K^3)$

Every 6 years

$k = 0.7^2 = 0.5$

Ideally:

$V_{dd} \rightarrow 0.5$

$t_{ox} \rightarrow 0.5$

$I_d \rightarrow 0.5$

$C_g \rightarrow 0.5$

$\tau \rightarrow 0.5$

$f \rightarrow 2$

$P \rightarrow 0.5^2 = 0.25$

$(P \text{ per cycle } \rightarrow 0.5^3 = 0.125)$

Downscaling decrease the power consumption and increase the performance of MOSFET
$L_{\text{gate}}$ and $t_{\text{ox}}(\text{EOT})$ scaling trend

A. Toriumi (Tokyo Univ), IEDM 2006, Short Course
Why $t_{ox}$ thinning

$t_{ox}$ and $V_{dd}$ have to be decreased for better channel potential control $\rightarrow I_{OFF}$ Suppression
Why $t_{ox}$ thinning

K. Henson, et al., (IBM) IEDM 2008, p.645  
K. J. Kuhn (Intel), IEDM 2007, p.471

DIBL (Drain Induced Barrier Lowering)

Vth (Threshold Voltage) variation

Better control of channel potential

Suppression of SCE & $V_{th}$ variability

$\sigma V_{th} = \frac{1}{2} \frac{4q^2 \epsilon_0 \phi_0}{\epsilon_{ox}} \frac{T_{ox}}{1 \sqrt{Leff \cdot Weff}} \left( \frac{4N}{\sqrt{Leff \cdot Weff}} \right) = \frac{1}{2} \frac{c_3}{\sqrt{Leff \cdot Weff}}$
Why $t_{ox}$ thinning

- Small $C_{ox}$ → Low inversion electron density → Small $I_{ON}$
- Large $C_{ox}$ → High inversion electron density → Large $I_{ON}$

$t_{ox}$ thinning
Gate oxide should be thicker than mono atomic layer
0.8 nm gate oxide thickness MOSFETs operate
0.8 nm → Distance of 3 Si atoms → 2 mono layers

R.Chau, et al., (Intel) IWGI 2003
Gate Leakage Power Density becomes significantly large with $L_g$ reduction, and thus, with $t_{ox}$ thinning!!
To use high-k dielectrics

K: Dielectric Constant

Thin SiO$_2$

K=4

SiO$_2$

Almost the same electric characteristics

Thick high-k dielectrics

High-k

K=20

5 times thicker

Small leakage Current

However, very difficult and big challenge!
“SiO₂ is at the very heart of the transistor, and replacing it is like performing a heart transplant,” said Robin Degraeve, a researcher at the IMEC in Leuven, Belgium. *EE Times. 4/8/03, “High-k insulators line up at the gate”*

“High-k is a very tough problem,” he [Bijan Davari, vice president of tech development at IBM Microelectronics] said. “People have started working on it, but not enough attention has been paid to it. Silicon dioxide is this amazing material, the interface with silicon is so good, it will take more time to develop alternatives.”

*EE Times. 6/11/02, “Technologist sketches IBM’s silicon road map”*
Combination of high-k and metal gate is important

K. Natori, et al., (Tsukuba Univ) SSDM 2005, p.286

Equivalent Oxide Thickness (EOT): gate dielectrics itself, $C_{ox}$

Capacitance Equivalent Thickness (CET): entire gate stack,

Metal gate can eliminate the poly-Si depletion.

\[ \text{Inversion CET} = T_{inv} \approx \text{EOT} + 0.4\text{nm} \]

with metal gate electrode

$C_{metal}$ is finite because of quantum effect. In other words electron is not a point charge located at the interface but distributed charge.
Band gap of high-k materials are inversely proportional to the k-value.

\[ J_g \propto \exp\left( -A \sqrt{m \Phi_B} \cdot \frac{k}{k_{SiO_2}} \cdot EOT \right) \]
Too Large k enhances SCE

Comparison of High-k and SiO₂ MOSFETs

**SiO₂**

- Gate: εᵣ = 3.9
- Source
- Drain
- Substrate

**Too large high-k**

- Gate: εᵣ = 390
- Source
- Drain
- Substrate

Penetration of lateral field from Drain through high-k causes significant short channel effects

### Choice of high-k

**High-k film: amorphous and flat → not like perovskite-type compound**

**Candidates**

<table>
<thead>
<tr>
<th>Unstable at Si interface</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
</tr>
</thead>
<tbody>
<tr>
<td>Li Be Mg Na</td>
<td>He</td>
<td>B C N O F Ne</td>
</tr>
<tr>
<td>Al Si P S Cl Ar</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>Si + MO(_x) M + SiO(_2)</td>
<td></td>
</tr>
<tr>
<td>Be</td>
<td>Si + MO(_x) MSi(_x) + SiO(_2)</td>
<td></td>
</tr>
<tr>
<td>Mg</td>
<td>Si + MO(_x) M + MSi(_x)O(_y)</td>
<td></td>
</tr>
</tbody>
</table>

**Unstable at Si interface**

- Si + MO\(_x\) M + SiO\(_2\)
- Si + MO\(_x\) MSi\(_x\) + SiO\(_2\)
- Si + MO\(_x\) M + MSi\(_x\)O\(_y\)

**Candidates**

- Li Be Mg Na
- Al Si P S Cl Ar
- Sn Sb Te I Xe Cs Ba Hf Ta W Re Os Ir Pt Au Hg Tl Pb Bi Po At Rn Fr Ra Rf Ha Sg Ns Hs Os Mt

- La Ce Pr Nd Pm Sm Eu Gd Tb Dy Ho Er Tm Yb Lu

**R. Hauser, IEDM Short Course, 1999**

Band Offset is desirable as high as possible to suppress the tunneling leakage.

Comparison of calculated various high-k oxide band offset against Si.
Conduction band offset vs. Dielectric constant

Leakage Current by Tunneling

Band offset

Si

Oxide

Dielectric Constant

Band Discontinuity [eV]

0 10 20 30 40 50

Si Band Gap

Best

2nd Best

Gd₂O₃

La₂O₃

ZrO₂

HfO₂

Lu₂O₃

T. Hattori, (Musashi Inst. Tech.),
Choice of high-k

Candidates

Unstable at Si interface

1. H
2. Li, Be
3. Na

Gas or liquid at 1000 K

1. He
2. Ne
3. Ar

Radio active


HfO$_2$ based dielectrics are selected as the first generation materials, because of their merit in 1) band-offset, 2) dielectric constant, 3) thermal stability.

La$_2$O$_3$ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

Some difficulty was ygyroscopicity or moisture absorbency → Solved by in-situ process and also by La silicate formation.

R. Hauser, IEDM Short Course, 1999
EOT can be larger for MG (Multiple gate) (Fin, Tri-gate Ω-gate, nanowire)

Better control of channel potential by double gate.
Choice of metal for gate

Gate metal information is not published so much; Metal names are hidden in some papers by naming the metals such as M1, M2

Metal properties

- Low workfunction (~4.1eV)  
  - Small electronegativity  
  - High reactivity  
  - Thermally unstable
- High workfunction (~5.1eV)  
  - Large electronegativity  
  - Low reactivity  
  - Poor contact (easily removed)

High-k gate dielectrics

Hf-based oxides

<table>
<thead>
<tr>
<th>Thickness (nm)</th>
<th>EOT</th>
<th>Technology Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>45</td>
<td>1</td>
<td>Remote SiO₂-IL scavenging HfO₂ (IBM)</td>
</tr>
<tr>
<td>32</td>
<td>0.95</td>
<td>EOT=0.52 nm</td>
</tr>
<tr>
<td>22</td>
<td>0.9</td>
<td>Technology for direct contact of high-k and Si is necessary</td>
</tr>
<tr>
<td>15</td>
<td></td>
<td>EOT=0.9nm</td>
</tr>
<tr>
<td>11</td>
<td></td>
<td>HfO₂/SiO₂ (IBM)</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>EOT=0.9nm</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SiO₂ IL (Interfacial Layer) is used at Si interface to realize good mobility.

Continued research and development

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM 2009, (IBM)

Direct contact with La-silicate (TokyoTech)
Smaller wire/fin width is necessary for SCE suppression

But mobility and $I_{ON}$ severely degrade with wire/fin width reduction

Therefore even in multi-gate structures EOT scaling could be accelerated to provide SCE immunity
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Flat metal/high-k interface for better mobility
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Interface dipole control for $V_{th}$ tuning
- Suppression of FLP
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
- Reliability: PBTI, NBTI, TDDB
- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Control of interface reaction and Si diffusion to high-k
- Suppression of FLP
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT

Suppression of gate leakage current
Endurance for high temperature process

Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
Workfunction engineering for $V_{th}$ control
Interface dipole control for $V_{th}$ tuning
Suppression of FLP
Remove contamination introduced by CVD
Thinning or removal of SiO$_2$-IL for small EOT
Poly-Si/HfO$_2$

Difficulty in controlling $V_{th}$
Mechanisms of Fermi Level Pinning

Because of FLP, $V_{th}$ of pMOSFET becomes too high

By using a new material combination of high-k gate dielectrics and metal gates, Intel's 45nm transistors significantly improve performance. Intel is on track for 45nm production in the second half of 2007.
"The implementation of high-k and metal materials marks the biggest change in transistor technology since the introduction of polysilicon transistors in the late 1960s," said Intel's co-founder Gordon Moore.
45nm High-k needs IL (Interfacial Layer)

**Power per MOSFET (P)**

- **EOT=1.0nm**
- **EOT Limit ~0.7 nm**
- **EOT=0.5nm**

**Year**

- **45nm node**
- **Lₜₐₓ=22nm**

- Introduction of High-k
- Still SiO₂ IL (Interfacial Layer) is used at Si interface to realize good mobility

- Technology for direct Contact of high-k and Si is necessary

**Material Layers**

- **Si**
- **SiO₂**
- **SiON**
- **HfO₂**
- **Metal**
- **High-k**

**EOT Limit**

- **~0.7 nm**
Why high mobility channel materials?

Arming higher performance at lower supply voltage

Both 1) and 2) are important

1) High injection velocity of carriers
2) High mobility of carriers

Problems: Technologies and Cost

- Interfacial properties at the gate insulator/semiconductor
- Contact resistance at Source/Drain and semiconductor
- Different semiconductors for n- and p-channel FETs
- Integration on Si wafer
## High mobility channel materials


<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>electron mob. (cm²/Vs)</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
</tr>
<tr>
<td>electron effective mass (/m₀)</td>
<td>mᵣ: 0.19</td>
<td>mᵣ: 0.082</td>
<td>0.067</td>
<td>0.082</td>
<td>0.023</td>
<td>0.014</td>
</tr>
<tr>
<td></td>
<td>mᵢ: 0.916</td>
<td>mᵢ: 1.467</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>hole mob. (cm²/Vs)</td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td>hole effective mass (/m₀)</td>
<td>m_HH: 0.49</td>
<td>m_HH: 0.28</td>
<td>m_HH: 0.45</td>
<td>m_HH: 0.45</td>
<td>m_HH: 0.57</td>
<td>m_HH: 0.44</td>
</tr>
<tr>
<td></td>
<td>m_LH: 0.16</td>
<td>m_LH: 0.044</td>
<td>m_LH: 0.082</td>
<td>m_LH: 0.12</td>
<td>m_LH: 0.35</td>
<td>m_LH: 0.016</td>
</tr>
<tr>
<td>band gap (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.17</td>
</tr>
<tr>
<td>permittivity</td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

Better carrier transport

Higher drive current at low power supply
What ITRS 2011 says?

2016 (4 years from now)

**Si Multi gate MOSFET** (Tri-gate etc.)
Manufacturing solutions are known

\[ L_g = 15.3 \text{ nm}, \ EOT = 0.76 \text{ nm} \]

2018 (6 years from now)

**Si Multi gate MOSFET**
Manufacturing solutions are *almost* known

\[ L_g = 12.8 \text{ nm}, \ EOT = 0.68 \text{ nm}, \ V_{dd} = 0.73 \text{V}, \ I_{dsat} = 1.80 \text{mA/\mu m} \]
\[ v_{inj} = 18.2 \text{Mcm/s}, \ CV/I = 0.24 \text{ps}, \ CV^2 = 0.31 \text{fV/\mu m} \]

**III-V MOSFET** (Only 6 years from now!!)
Manufacturing solutions are not known

\[ L_g = 14 \text{nm}, \ EOT = 0.68 \text{ nm}, \ V_{dd} = 0.63 \text{V}, \ I_{dsat} = 2.2 \text{mA/\mu m} \]
\[ v_{inj} = 42.9 \text{Mcm/s}, \ CV/I = 0.13 \text{ps}, \ CV^2 = 0.18 \text{fV/\mu m} \]
What ITRS 2011 says?

2026 (14 years from now)

**Si Multi gate MOSFET**
Manufacturing solutions are not known

\[ L_g=5.9\text{nm}, \quad E\text{OT}=0.45\text{nm}, \quad V_{dd}=0.57\text{V}, \quad I_{dsat}=1.80\text{mA}/\mu\text{m} \]
\[ v_{inj}=26.7\text{Mcm/s}, \quad CV/I=0.10\text{ps}, \quad CV^2=0.14\text{fV}/\mu\text{m} \]

**III-V MOSFET**
Manufacturing solutions are not known

\[ L_g=5.8\text{nm}, \quad E\text{OT}=0.45\text{nm}, \quad V_{dd}=0.54\text{V}, \quad I_{dsat}=2.51\text{mA}/\mu\text{m} \]
\[ v_{inj}=66.4\text{Mcm/s}, \quad CV/I=0.06\text{ps}, \quad CV^2=0.09\text{fV}/\mu\text{m} \]
## ITRS 2011 for Si (HP: High Performance Logic)

*1: Thicker EOT for MG (Multiple gate: Fin/Tri gate, nanowire)

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2012</th>
<th>2014</th>
<th>2016</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
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<th>2026</th>
</tr>
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<tbody>
<tr>
<td>( L_g ) (nm)</td>
<td>22</td>
<td>18</td>
<td>15.3</td>
<td>12.8</td>
<td>10.6</td>
<td>8.9</td>
<td>7.4</td>
<td>5.9</td>
</tr>
<tr>
<td>( V_{dd} ) (V)</td>
<td>0.87</td>
<td>0.82</td>
<td>0.77</td>
<td>0.73</td>
<td>0.68</td>
<td>0.64</td>
<td>0.61</td>
<td>0.57</td>
</tr>
<tr>
<td>( EOT ) (nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bulk</td>
<td>0.84</td>
<td>0.73</td>
<td>0.61</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD SOI</td>
<td>0.8</td>
<td>0.72</td>
<td>0.63</td>
<td>0.54</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>*1: MG</td>
<td>0.76</td>
<td>0.68</td>
<td>0.62</td>
<td>0.56</td>
<td>0.50</td>
<td>0.45</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mobility enhancement factor due to strain</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
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</tr>
<tr>
<td>( C_g ) Ideal (fF/( \mu )m)</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bulk</td>
<td>0.658</td>
<td>0.611</td>
<td>0.576</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD SOI</td>
<td>0.529</td>
<td></td>
<td></td>
<td>0.429</td>
<td>0.393</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MG</td>
<td>0.455</td>
<td>0.409</td>
<td>0.362</td>
<td>0.320</td>
<td>0.284</td>
<td>0.238</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{t,sat} ) (mV)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bulk</td>
<td>289</td>
<td>302</td>
<td>310</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD SOI</td>
<td>222</td>
<td>227</td>
<td>234</td>
<td>242</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MG</td>
<td>217</td>
<td>223</td>
<td>225</td>
<td>228</td>
<td>231</td>
<td>237</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( CV/I ) (ps)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NMOS</td>
<td>0.57</td>
<td>0.47</td>
<td>0.38</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD SOI</td>
<td>0.38</td>
<td>0.30</td>
<td>0.24</td>
<td>0.20</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MG</td>
<td>0.29</td>
<td>0.24</td>
<td>0.19</td>
<td>0.16</td>
<td>0.13</td>
<td>0.10</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Manufacturing solutions exist or is being optimized

Manufacturing solutions are known

Manufacturing solutions are **NOT** known
### ITRS 2011 for Si (HP), contd

<table>
<thead>
<tr>
<th>Year of Production</th>
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<td>8.9</td>
<td>7.4</td>
<td>5.9</td>
</tr>
<tr>
<td>Equivalent Injection velocity ( V_{\text{inj}} ) ((10^7 \text{ cm/s}))</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bulk</td>
<td>1.09</td>
<td>1.18</td>
<td>1.33</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD SOI</td>
<td>1.37</td>
<td>1.51</td>
<td>1.63</td>
<td>1.83</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MG</td>
<td>1.68</td>
<td>1.82</td>
<td>2.05</td>
<td>2.26</td>
<td>2.38</td>
<td>2.67</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{d,\text{sat}} ) (mA/µm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bulk</td>
<td>1.367</td>
<td>1.496</td>
<td>1.670</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD SOI</td>
<td>1.530</td>
<td>1.654</td>
<td>1.791</td>
<td>1.942</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MG</td>
<td>1.685</td>
<td>1.805</td>
<td>1.916</td>
<td>2.030</td>
<td>2.152</td>
<td>2.308</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{sd,leak}} ) (nA/µm)</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>( R_{sd} ) ((\Omega·\mu\text{m}))</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bulk</td>
<td>232</td>
<td>183</td>
<td>149</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD SOI</td>
<td>274</td>
<td>228</td>
<td>187</td>
<td>153</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MG</td>
<td>257</td>
<td>218</td>
<td>186</td>
<td>160</td>
<td>133</td>
<td>104</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( CV^2 ) ((\text{fJ}/\mu\text{m}))</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bulk</td>
<td>0.68</td>
<td>0.57</td>
<td>0.49</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD SOI</td>
<td>0.47</td>
<td>0.38</td>
<td>0.32</td>
<td>0.26</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MG</td>
<td>0.38</td>
<td>0.31</td>
<td>0.25</td>
<td>0.21</td>
<td>0.17</td>
<td>0.14</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Manufacturing solutions exist or is being optimized

Manufacturing solutions are known

Manufacturing solutions are *NOT* known
## ITRS 2011 for III-V/Ge

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$ (nm)</td>
<td>14</td>
<td>11.7</td>
<td>9.3</td>
<td>7.4</td>
<td>5.8</td>
</tr>
<tr>
<td>$V_{dd}$ (V)</td>
<td>0.63</td>
<td>0.61</td>
<td>0.58</td>
<td>0.56</td>
<td>0.54</td>
</tr>
<tr>
<td>$EOT$ (nm)</td>
<td>0.68</td>
<td>0.62</td>
<td>0.56</td>
<td>0.50</td>
<td>0.45</td>
</tr>
<tr>
<td>$C_g$ Ideal (fF/µm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>III-V</td>
<td>0.28</td>
<td>0.24</td>
<td>0.20</td>
<td>0.16</td>
<td>0.13</td>
</tr>
<tr>
<td>Ge</td>
<td>0.41</td>
<td>0.36</td>
<td>0.30</td>
<td>0.25</td>
<td>0.21</td>
</tr>
<tr>
<td>$V_{t,sat}$ (mV)</td>
<td>229</td>
<td>230</td>
<td>238</td>
<td>245</td>
<td>251</td>
</tr>
<tr>
<td>III-V</td>
<td>230</td>
<td>231</td>
<td>241</td>
<td>249</td>
<td>254</td>
</tr>
<tr>
<td>Ge</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CV/I (ps)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>III-V</td>
<td>0.13</td>
<td>0.11</td>
<td>0.09</td>
<td>0.07</td>
<td>0.06</td>
</tr>
<tr>
<td>Ge</td>
<td>0.21</td>
<td>0.17</td>
<td>0.13</td>
<td>0.10</td>
<td>0.08</td>
</tr>
</tbody>
</table>

Manufacturing solutions are *NOT* known.
<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$ (nm)</td>
<td>14</td>
<td>11.7</td>
<td>9.3</td>
<td>7.4</td>
<td>5.8</td>
</tr>
<tr>
<td>Equivalent Injection velocity $V_{inj}$ (10^7 cm/s)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>III-V</td>
<td>4.29</td>
<td>4.58</td>
<td>5.32</td>
<td>5.93</td>
<td>6.64</td>
</tr>
<tr>
<td>Ge</td>
<td>2.26</td>
<td>2.44</td>
<td>2.86</td>
<td>3.19</td>
<td>3.63</td>
</tr>
<tr>
<td>$I_{d,sat}$ (mA/µm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>III-V</td>
<td>2.200</td>
<td>2.343</td>
<td>2.523</td>
<td>2.703</td>
<td>2.884</td>
</tr>
<tr>
<td>Ge</td>
<td>1.769</td>
<td>1.932</td>
<td>2.121</td>
<td>2.330</td>
<td>2.555</td>
</tr>
<tr>
<td>$I_{sd,leak}$ (nA/µm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>$R_{sd}$ (Ω-µm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>III-V</td>
<td>131</td>
<td>113</td>
<td>96</td>
<td>82</td>
<td>70</td>
</tr>
<tr>
<td>Ge</td>
<td>149</td>
<td>126</td>
<td>105</td>
<td>85</td>
<td>72</td>
</tr>
<tr>
<td>$CV^2$ (fJ/µm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>III-V</td>
<td>0.18</td>
<td>0.15</td>
<td>0.13</td>
<td>0.11</td>
<td>0.09</td>
</tr>
<tr>
<td>Ge</td>
<td>0.23</td>
<td>0.20</td>
<td>0.16</td>
<td>0.14</td>
<td>0.11</td>
</tr>
</tbody>
</table>

Manufacturing solutions are NOT known
Outline

- Introduction
- **High-k/metal gate on Si channel**
  - **Gate first/last processes**
    - Threshold voltage
    - Mobility
    - Reliability
    - EOT reduction toward 0.5 nm
    - Atomic layer deposition (ALD)
    - Benchmark
- New channel materials
- Some conclusions
Process order for High-k, Metal Gate & S/D

**Conventional SiO₂/Poly Gate**
Gate first, S/D last

- SiO₂
- Si
- Poly Si
- Gate Patterning
- Ion implantation (S/D)
- High temp anneal
- Dopant activation
- Self-alignment of S/D with Gate Electrode

**High-k/Metal Gate**

**Problem**
Poor endurance of High-k & MG at high-temp S/D anneal such at 1000~1050°C

**Solution 1 Gate first process (S/D Last)**

- High-k first
- Metal middle
- Self-aligned S/D
- S/D last
- High temp anneal
- Dopant activation

Improve the high-temp endurance of high-k & MG to keep the process order.
Process order for High-k, Metal Gate & S/D

High-k/Metal Gate

Solution 2 Gate last process
(S/D first)

Dummy gate

Self-aligned S/D high temp anneal

SiO₂ coverage

S/D first

CMP

High-k/Metal Gate

High-k gate removal

High-k middle

Metal

Replacement gate (damascene)
Process order for High-k, Metal Gate & S/D

**High-k/Metal Gate**

1. **High-k first**
2. **S/D middle**
3. **SiO₂ coverage**
4. **CMP**

**Solution 3**

Another Gate first process (S/D middle)

- Dummy gate removal
- Metal last
- Replacement gate (damascene)
High-k/metal gate integration schemes

R. Arghavani, (Applied Materials)
IEDM 2007, Short Course

**Replacement Metal Gate (Damascene)**
- Advantages:
  - Low thermal budget (metal gate deposition after S/D anneals)
  - Known metal work function
- Challenges:
  - Cost
  - Extendibility to narrower CDs

**Gate-First Process**
- Advantages:
  - Compatible with high thermal budget process
  - Follows standard CMOS flow
- Challenges:
  - NMOS and PMOS cap layer integration is challenging
Continued scaling in EOT has been reported.
Outline

- Introduction
- High-k/metal gate on Si channel
  - Gate first/last processes
  - Threshold voltage
    - Mobility
    - Reliability
    - EOT reduction toward 0.5 nm
    - Atomic layer deposition (ALD)
    - Benchmark
- New channel materials
- Some conclusions
Other issue: Usually, different metals or high-k’s are necessary to obtain good Vth values for n- and p-MOSFETs.
Threshold voltage control

Dual metal gate

Gate-last

→ EWF ~ Band edge

Capping layer with TiN

La for NMOS

Al for PMOS

Gate-first

→ EWF ~ Mid gap


T. Ando, et al., (IBM) IEDM 2009, p.423
Two different metals

R. Arghavani, (Applied Materials)
IEDM 2007, Short Course

One Dielectric Stack, Two $\Phi_m$ Metals

<table>
<thead>
<tr>
<th>Layer</th>
<th>Toolset Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal Fill</td>
<td>PVD TTN Liner, Al fill OR</td>
</tr>
<tr>
<td></td>
<td>eSIP Ta/TaN, Cu fill OR</td>
</tr>
<tr>
<td></td>
<td>MO-TiN, W fill</td>
</tr>
<tr>
<td>Metal Gate</td>
<td>ALD, PVD</td>
</tr>
<tr>
<td>High-$k$</td>
<td>ALD</td>
</tr>
<tr>
<td>Oxynitride</td>
<td>Radiance, DPN</td>
</tr>
</tbody>
</table>

General Process Flow *

- Gate Preclean
- RTO
- DPN/PNA [Option]
- ALD HfO$_2$
- DPN/PNA [Option]
- Deposit buffer layer
- Gate Poly, Litho/etch (incl. high-$k$)
- Std Flow (incl. stress liner) to PMD Dep
- PMD CMP
- Poly silicide/poly etch
- Remove buffer layer
- Deposit N-metal
- PMOS patterning (Resist dep, litho, etch N-metal off of PMOS side)
- Deposit P-metal
- Metal Fill: Liner + Seed + Fill
- Metal CMP
Process flow of dual metal gate CMOS. (a) ALD-HfO₂ deposition. (b) n-metal (PVD-HfSiₓ) deposition and pMOS region open. (c) HfSiₓ wet etching. (d) p-metal (PVD-Ru) deposition. (e) CVD-W deposition. (f) Dual metal CMP.

Gate last: S/D first, High-k middle, metal last
Two different dielectric cap layers

R. Arghavani, (Applied Materials)
IEDM 2007, Short Course

Two Dielectric Stacks, One $\Phi_m$ Metal

Dielectric cap layer at high-k/metal interface adjusts the dipole for $V_t$ tuning

<table>
<thead>
<tr>
<th>Layer</th>
<th>Toolset Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal</td>
<td>ALPVD</td>
</tr>
<tr>
<td>Cap Layer *</td>
<td>RF-PVD</td>
</tr>
<tr>
<td></td>
<td>(nFET LaO$_x$, pFET Al-based)*</td>
</tr>
<tr>
<td>High-k</td>
<td>ALD</td>
</tr>
<tr>
<td>Oxynitride</td>
<td>Radiance, DPN</td>
</tr>
</tbody>
</table>

General Process Flow
- Gate Preclean
- RTO
- DPN/PNA [Option]
- ALD HfO$_2$
- DPN/PNA [Option]
- Deposit nFET cap layer
- PMOS patterning (Resist dep, litho, etch N-cap layer off of PMOS side)
- Deposit pFET cap layer
- NMOS patterning (Resist dep, litho, etch P-metal off of NMOS side)
- Deposit metal gate
- Poly-Si dep
- Gate stack litho
- Etch poly-Si
- Etch Metal Gate & Gate dielectric stacks [Assumption: Need two different etches to remove dielectric cap layers before HfO$_2$]
- Implants $\rightarrow$ PMD Dep (std flow)
High-k/SiO$_2$ interface on $V_{FB}$ shift

Y. Kamimuta, et al., (MIRAI) IEDM 2007, p.341

$V_{FB}$ is determined by high-k/SiO$_2$ interface structure.
$V_{FB}$ modulation by capping materials


M. Niwa, (Tsukuba Uni) SSDM 2009, Short Course

Oxygen density ($\sigma$) is different from each material

$\sigma$: oxygen density

$\sigma/\sigma_{SiO_2}$
Capping layer technique


Capping elements diffuse to the bottom interfacial SiO₂ layer.

Dipole formation at the interface due to diffusion of capping material.
A simple interfacial dipole model

\[ \mu = \Delta \chi d \]

\[ \mu_{all} = \frac{2}{3} \mu_{La-O} - \frac{1}{2} \mu_{Si-O} + \Delta \mu \]

<table>
<thead>
<tr>
<th></th>
<th>( \chi )</th>
<th>( \Delta \chi )</th>
<th>( d ) (nm)</th>
<th>( \mu = \Delta \chi d )</th>
</tr>
</thead>
<tbody>
<tr>
<td>La</td>
<td>1.10</td>
<td>2.34</td>
<td>0.258</td>
<td>0.604</td>
</tr>
<tr>
<td>Si</td>
<td>1.90</td>
<td>1.54</td>
<td>0.160</td>
<td>0.246</td>
</tr>
<tr>
<td>(SiO)</td>
<td>(2.56)</td>
<td>0.88</td>
<td>(0.160)</td>
<td>0.141</td>
</tr>
</tbody>
</table>

\( \chi \): electronegativity

\( d \): distance between atoms

\( \Delta \chi \): \( \chi_{\text{atom}} - \chi_{O_2} \)

\( \chi_{O_2} \): 3.44
Dipole formation at high-k/SiO₂

K. Kakushima et al., (Tokyo Tech.) ECS, 2008

\[ \text{V}_{FB} = \eta \mu_{\text{all}} + \phi_{ms} \]
\[ \eta = -1.87 \]
\[ \text{0.36V} \]

Coefficient to convert dipole moment to voltage can be obtained

<table>
<thead>
<tr>
<th></th>
<th>calculation</th>
<th>( \mu_{\text{all}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂/Si</td>
<td>( 1/2 \mu_{\text{Si-O}} - 1/2 \mu_{\text{Si-O}} )</td>
<td>0</td>
</tr>
<tr>
<td>La₂O₃/SiO₂</td>
<td>( 2/3 \mu_{\text{La-O}} - 1/2 \mu_{\text{Si-O}} + \Delta \mu )</td>
<td>0.169</td>
</tr>
<tr>
<td>HfO₂/SiO₂</td>
<td>( 1/2 \mu_{\text{Hf-O}} - 1/2 \mu_{\text{Si-O}} + \Delta \mu )</td>
<td>-0.023</td>
</tr>
</tbody>
</table>
VFB estimation with simple dipole model

K. Kakushima et al., (Tokyo Tech.) ECS, 2008

<table>
<thead>
<tr>
<th>Calculation</th>
<th>( \mu_{all} )</th>
<th>VFB (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) SiO(_2)/Si</td>
<td>( 1/2\mu_{Si-O} - 1/2\mu_{Si-O} )</td>
<td>0</td>
</tr>
<tr>
<td>(b) La(_2)O(_3)/Si</td>
<td>( 2/3\mu_{La-O} - 1/2\mu_{Si-O} )</td>
<td>0.279</td>
</tr>
<tr>
<td>(c) HfO(_2)/Si</td>
<td>( 1/2\mu_{Hf-O} - 1/2\mu_{Si-O} )</td>
<td>0.087</td>
</tr>
<tr>
<td>(d) La(_2)O(_3)/SiO(_2)</td>
<td>( 2/3\mu_{La-O} - 1/2\mu_{Si-O} + \Delta\mu )</td>
<td>0.169</td>
</tr>
<tr>
<td>(e) HfO(_2)/SiO(_2)</td>
<td>( 1/2\mu_{Hf-O} - 1/2\mu_{Si-O} + \Delta\mu )</td>
<td>-0.023</td>
</tr>
</tbody>
</table>
Device architecture

High impurity in channel.

Low impurity (or non-dope) in channel.

F. Andrieu, et al., (LETI) VLSI 2010, p.57

Single mid gap metal/high-k with UTB SOI structure

Planar FET

UTB SOI

Multi Gate
After the activation anneal and sidewall removal, oxygen is introduced into high-k to annihilate the charged oxygen vacancy, resulting in positive $V_{th}$ shift.

E. Cartier, et al., (IBM) VLSI 2009, p.42
Outline

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  - Gate first/last processes
  - Threshold voltage
- Mobility
  - Reliability
  - EOT reduction toward 0.5 nm
  - Atomic layer deposition (ALD)
  - Benchmark
- New channel materials
- Some conclusions
Possible sources for reduced mobility in high-k/metal gate stacks
Insertion of SiO$_2$-IL can recover the mobility.

Scattering centers separate from inversion channel.
Remote phonon scattering

M. V. Fischetti et al., (IBM) J. Appl. Phys, vol.90, no.9, p.4587
Z. Ren et al., (IBM) IEDM 2003, p.793

Intrinsic mechanisms for high-k gate dielectrics?

Silicate (weaker ionicity) have weaker soft optical phonon scattering.

Calculation

SiO₂

HfO₂

Strong electron-phonon interaction

RPS (Remote Phonon scattering)


Origin of high-κ:
large ionic polarizability

Electron effective mobility [cm²/Vs]
Experiment: Remote phonon scattering

Z. Ren et al., (IBM) IEDM 2003, p.793

Electron effective mobility [cm²/Vs]

$N_{inv} = 5 \times 10^{12} \text{cm}^{-2}$
Remote Coulomb scattering


Fixed charges at HfO₂/SiO₂ interface

\[ \mu_{\text{add}} \approx \exp(2k_{\text{th}}t_{\text{IL}}) \]

\[ k_{\text{th}} = 0.65 \text{ nm}^{-1} \]

300K

interfacial SiO₂ thickness \( t_{\text{IL}} \) (Å)

\[ \mu_{\text{add}} \text{ (cm}^2/\text{Vs)} \]

1.4 MV/cm

0.8 MV/cm

0.5 MV/cm

Gate

High-k

SiO₂-IL

Source

\( e^- \)

Drain
Grain boundary acts as trap states.

HfO₂ Physical thickness

Amorphous Poly-crystalline

Point A Point B
Nitrogen-induced interface traps


Nitrogen diffusion from TiN degrades interfacial properties.

Interface state density is increased with increasing TiN thickness.
Cap-material dependence of mobility

T. Ando, et al., (IBM) IEDM 2009, p.423

La-cap doesn’t degrade mobility

Al-cap degrades the mobility due to RCS
EOT versus Mobility

Universal and Fundamental limits?
(RCS? or RSRS(remote-surface roughness scattering(?))
Metal/high-k interface

RCS caused by metal or oxygen defects in high-k near the metal gate

Spatial distribution of metal gate induced defects approaches to high-k/Si interface with small EOT

Some of the defects generates interfacial states

Even mobility degrades with decrease in EOT ($T_{inv}$), $I_{on}$ increases by choosing the conditions.
Even mobility degrades with decrease in EOT ($T_{\text{inv}}$), $I_{\text{on}}$ increases by choosing the conditions

\[ I_{\text{sat}} \propto N_{\text{inv}} \times \mu^\alpha \propto EOT^{-1} \times \mu^\alpha \]
HfO$_2$ gate stack with EOT=0.45 nm


ISSG : in-situ steam grown

EOT = 0.45 nm

EOT is decreased with decreasing metal thickness
High-k/metal gate on Si channel

- Gate first/last processes
- Threshold voltage
- Mobility

Reliability

- EOT reduction toward 0.5 nm
- Atomic layer deposition (ALD)
- Benchmark

New channel materials

Some conclusions
Gate stack and band diagrams

E. Cartier, et al., (IBM) IEDM 2011, p. 441
Gate tunneling current


nMOS: Electron current from the gate is dominant

pMOS: Electron current from the gate and hole current from the substrate are comparable
Bias temperature instability

vol. 9, no. 2, p. 147, 2009

Strong electron trapping at HfO₂ because of large electron current for PBTI (nFET)

HfO₂ has high density of oxygen vacancies which captures electrons

NBTI : comparable to conventional poly-Si/SiON stacks

PBTI : reliability challenge for MG HK nFET devices
HfO₂ thickness vs. trapped charge

Reducing the trap density by thinning the HfO₂ layer, however, inevitably leading to enhanced gate leakage.

The BTI lifetimes is predicted to decrease by 50-100x for every 0.1nm of IL-scaling. Drastic lifetime reduction also occurs for TDDB.
Introduction

High-k/metal gate on Si channel
- Gate first/last processes
- Threshold voltage
- Mobility
- Reliability

EOT reduction toward 0.5 nm
- Atomic layer deposition (ALD)
- Benchmark

New channel materials

Some conclusions
No. 1: Increase the k-value of the high-k

No. 2: Direct contact of high-k/Si structure
Physics of higher-k

Clausius – Mosotti equation

\[ \varepsilon = 1 + \frac{8\pi \alpha_m}{3V_m} \]

- \( \varepsilon \): dielectric constant
- \( \alpha_m \): polarizability
- \( V_m \): molar volume

Increasing polarizability (\( \alpha_m \)) – Doped high-k system

Ti-doped HfO\(_2\) : \( k \sim 36 \)

M. Khare (IBM), IEDM 2010 Short Course

R. D. Shannon (Central Research and Development,)
J. Appl. Phys, vol. 73, p.348, 1993

S. Rhee, et al., (Texas Uni) IEDM 2004, p.837

R. D. Shannon (Central Research and Development,)
J. Appl. Phys, vol. 73, p.348, 1993

Increasing polarizability (\( \alpha_m \)) – Doped high-k system

Ti-doped HfO\(_2\) : \( k \sim 36 \)
Y-doping in HfO₂ provides structural transformation and hence permittivity engineering.
**Scaling limit in EOT**


- **Scaling in EOT**
  - Hf based oxide
  - Limit

- **SiO\textsubscript{x} interfacial layer (typ.0.5~0.7nm)**

- **Si**

- **SiO\textsubscript{2}** interfacial layer inserted or re-grown for
  - Recovery of degraded mobility
  - Interface state, reliability (TDDB, BTI), etc.

- **SiO\textsubscript{2}-IL free structure (direct contact of high-k/Si)**
  - Is required for EOT=0.5nm
IL scavenging

Oxygen is transferred from SiO₂-IL to metal through the intermediary of oxygen vacancy (V₀) in HfO₂.

Content of oxygen vacancy in HfO₂ remains constant, enabling the removal of SiO₂ IL without Vₚh shift.
SiO\textsubscript{x}-IL growth at HfO\textsubscript{2}/Si Interface

\[ \text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2 \]

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Trans. ECS 11, 319

SiO\textsubscript{x}-IL is formed after annealing

Oxygen control is required for optimizing the reaction

K. Kakushima et al., (Tokyo Tech.), IWDTF2008, p. 9
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_9.33$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface. Control of oxygen partial pressure is the key for processing.
(1) Interface property improvement by optimized annealing

(2) Reduction of oxygen defects by oxygen partial pressure control

(3) Selection of gate metal and structure for scaled EOT
Issue in high-k/Si structure

(1) Interface property improvement by optimized annealing

(2) Reduction of oxygen defects by oxygen partial pressure control

(3) Selection of gate metal and structure for scaled EOT
Approach for small $D_{it}$

$\sigma/\sigma_0$: Normalized average stress

$P_b/P_{b0}$: Normalized density of $P_b$ centers

High temperature anneal decreases stress ($\sigma$) and $P_b$ center density

High temperature anneal decreases interfacial state density ($D_{it}$)
A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Impact of annealing temperature

T. Kawanago, et al., (Tokyo Tech.)

A small $D_{it}$ of $1.6 \times 10^{11}$ cm$^{-2}$/eV, results in better electron mobility.
FTIR analysis

K. Kakushima, et al., (Tokyo Tech.) the 17th Workshop on Gate Stack Technology and Physics., 2012


Red-shift of LO phonon regarding Si-O-Si with increasing annealing temperature

At above 700°C, network structure close to the thermally-grown SiO₂
① silicate-reaction-formed fresh interface

Fresh interface with silicate reaction

② stress relaxation at interface

FGA800°C is necessary to reduce the interfacial stress.

Issue in high-k/Si structure

(1) Interface property improvement by optimized annealing

(2) Reduction of oxygen defects by oxygen partial pressure control

(3) Selection of gate metal and structure for scaled EOT
Oxygen vacancy in high-k

Oxygen vacancy is suppressed by elemental addition (Mg, Sr, Ba) into HfO$_2$ (theoretical study).


N. Mise, et al., (selecte) IEDM2007, p. 527

Mg, Sr, Ba Capping layer

MgO incorporation into Hf-based oxide

Improvement of mobility
T. Koyanagi, et al., (Tokyo Tech.)
Jpn. J. Appl. Phys., 48, 05DC02, 2009

Remote Coulomb scattering is suppressed with Mg incorporation.

Mobility dependence on $E_{\text{eff}}^{0.5-0.6}$
Indicates remote coulomb scattering.

$\frac{1}{\mu_{\text{add}}} = \frac{1}{\mu_{\text{without Mg}}} - \frac{1}{\mu_{\text{with Mg}}}$
Charged defect in dielectrics

Oxygen concentration in film depend on external ambient

Charged defects generated

Oxygen chemical potential fluctuates by process condition.

La$_2$O$_3$ → La$_2$O$_3$ + V$_O^{2+}$

Estimation of charged defects density

$\text{Density of charged defect [cm}^{-3}\text{]}$

$10^{23}$ $10^{20}$ $10^{17}$ $10^{14}$ $10^{11}$ $10^{8}$ $10^{5}$

$-7$ $-6$ $-5$ $-4$ $-3$ $-2$ $-1$ $0$

$\text{O}_2 \text{ molecule}$

V$_{O}^{2+}$ rich

L$_{O}^{-2}$ rich

La$_2$O$_3$ monolayer

La$_2$O$_3$

Ce-oxide capping for $\mu_o$ fixation


Oxygen chemical potential

Reducing process:
- $\text{CeO}_2 \rightarrow \text{Ce}_2\text{O}_3 + O$
- $V_o^{2+}$ absorb
- $I_o^{2-}$ absorb

Oxidizing process:
- $\text{Ce}_2\text{O}_3 + O \rightarrow \text{CeO}_2$
- $I_o^{2-} - 2e^- \rightarrow O$
- $V_o^{2+}$ release

$\mu_o$ is kept constant with Ce-oxide capping.

Stable flat and voltage
Co-existence of Ce\(^{3+}\) and Ce\(^{4+}\)

binding energy difference of Ce \(3d_{5/2}\) and Si \(2s\) is constant

Oxygen concentration is fixed
Ce-oxide capped on La$_2$O$_3$ is useful for charged defects reduction.

Charged defect density ~experiment~

\[
\begin{align*}
\text{EuOx} / \text{La}_2\text{O}_3 \\
\text{CeOx} / \text{La}_2\text{O}_3 \\
\text{PrOx} / \text{La}_2\text{O}_3
\end{align*}
\]

Estimated from EOT-V$_{FB}$ slope

Oxygen defects in high-k affect on MOSFET characteristics. (ionic nature)


Oxygen incorporation into high-k

Oxygen vacancy is $V_{o}^{2+}$

Positive $V_{FB}$ shift
Oxygen incorporation method


n-Si Substrate → LOCOS isolated Si wafer (S/D pre-formed)

SPM and HF cleaning

La$_2$O$_3$ deposition (300°C)

Gate metal (W) deposition by RF sputtering

Gate patterning

FGA (3% H$_2$) at 800°C for 30min

Contact hole and Al wiring

Backside Al contact

Annealing in 5% O$_2$ for 30min (Oxy)

FGA (3% H$_2$) at 420°C for 30min

Measurement

Oxygen ambient annealing

La-silicate

Si sub.

W

W : 5nm
Effect of oxygen annealing


Positive \( V_{FB} \) Shift
Turn up in inversion

Excess oxygen leads to EOT increase.
Improved C-V curve while maintained the $V_{FB}$ at positive value
Reversible $V_{FB}$ shift has been reported with HfO$_2$ by oxidation and reduction annealing.
Experimental procedure


- Initial C-V measurement
- Diluted oxygen annealing (Oxy)
  - 400°C or 340°C, 30min
  - C-V measurement
- Forming gas annealing (FGA)
  - 420°C, 30min
  - C-V measurement
- Forming gas annealing (FGA)
  - 500°C, 30min
  - C-V measurement

Identical MOS devices were measured.
Additional oxygen atom supply recovers the oxygen defects.

Complete recovery of defects with La-silicate, owing to strong bonding of covalent nature in silicate.
Subsequent FGA can completely recover the interfacial state density.
Improvement in mobility was confirmed by combining the two processes.

Preserving oxygen after FGA

Recover of interfacial property
Issue in high-k/Si structure

(1) Interface property improvement by optimized annealing

(2) Reduction of oxygen defects by oxygen partial pressure control

(3) Selection of gate metal and structure for scaled EOT
Annealing temperature on EOT


EOT increase with increasing annealing temperature.

Excess La-silicate formation
Metal (TiN) thickness on EOT

Gate-last:

Gate-first: Standard

With oxygen control

Air exposure

Metal (TiN) oxidation & Oxygen down-diffusion

Decreasing metal thickness

Low content of oxygen in metal results in suppressing SiOₓ IL formation.
Thinner W metal can provide small EOT with La$_2$O$_3$.

D. Kitayama, et al., (Tokyo Tech.)
Si (100nm) W (5nm) TiN (10nm) La-silicate Si sub.

- Suppression of oxygen diffusion
- Barrier for reaction between Si and W
- Oxygen supply to gate dielectrics

LOCOS isolated p-Si wafer (S/D pre-formed)

- SPM and HF cleaning
- La$_2$O$_3$ deposition (300°C)
- W deposition (5nm) by RF sputtering
- TiN deposition (10nm) by RF sputtering (Ar:N$_2$=9:1)
- Si deposition (100nm) by RF sputtering

Gate patterning

- Post metallization annealing (PMA) in FG (H$_2$:N$_2$=3:97%) at 800°C for 30min
- Si removal by TMAH for electrical measurement

S/D & Backside Al contact

- FGA (H$_2$:N$_2$=3:97%) at 420°C for 30min
Increasing EOT caused by high temperature annealing can be dramatically suppressed by MIPS stacks.

Impact of MIPS structure

Cross-sectional TEM images

No interfacial layer can be confirmed in Si/TiN/W stacks

$K_{av} \sim 8$

$K_{av} \sim 12$

$K_{av} \sim 16$

EOT of 0.62nm and 155 cm²/Vsec at 1MV/cm can be achieved.

nMOSFET with EOT of 0.40nm

T = 300 K
L / W = 5 / 20 μm

EOT=0.40nm

Gate Voltage (V)

C_{gc} (μF/cm²)

0 0.1 0.2 0.3 0.4 0.5
-0.5 -0.4 -0.3 -0.2 -0.1 0 0.1 0.2 0.3 0.4 0.5

Mobility (cm²/Vsec)

0 20 40 60 80 100
0 0.5 1 1.5 2 2.5

E_{eff} (MV/cm)

T = 300 K
L / W = 5 / 20 μm
N_{sub} = 3 \times 10^{16} \text{ cm}^{-3}
nMOSFET with EOT of 0.44nm

EOT of 0.44nm

Mobility of 115 cm$^2$/Vsec at 1 MV/cm
EOT = 0.66 nm

PMA in F.G. (30 min)

Higher PMA temp

Gate voltage (V)

Capacitance (µF/cm²)

600 °C

800 °C

900 °C

1000 °C

10 µm x 10 µm

10 µm x 10 µm

10 µm x 10 µm

20 µm x 20 µm
EOT = 0.65 nm
PMA in F.G. (30 min)

Gate voltage (V)

Capacitance ($\mu$F/cm$^2$)

- 600 °C
- 800 °C
- 900 °C
- 1000 °C

$10 \, \mu$m x $10 \, \mu$m
EOT = 0.65 nm in F.G. (30 min)

- Hysteresis vs. PMA temperature (°C)
- Flat band Voltage vs. PMA temperature (°C)

10 µm x 10 µm
Transfer characteristics (EOT = 0.40 nm)

EOT = 0.40 nm

Drain Voltage (V)

Drain Current (A)

L/W = 5/20 µm

N_a = 3 \times 10^{16}
Transfer characteristics (EOT= 0.44 nm)

EOT=0.44 nm

\[ \text{L/W} = 5/10 \ \mu m \]
\[ N_a = 3 \times 10^{16} \]
Transfer characteristics (EOT= 0.53nm)

EOT=0.53 nm

L/W = 20/20 µm

N_a = 3x10^{16}

Drain Voltage (V)

Drain Current (A)
Transfer characteristics (EOT= 0.57nm)

EOT=0.57 nm

L/W = 10/10 µm
N_a = 3x10^{16}

Drain Voltage (V)

Drain Current (A)
Gate leakage at EOT of 0.44nm

![Graph showing gate leakage current vs. gate voltage]

Gate leakage at 1 V is an order of magnitude lower than that of ITRS.
Gate leakage at EOT of 0.40nm

Gate leakage at 1 V is an order of magnitude lower than that of ITRS.
Gate leakage is two orders of magnitude lower than that of ITRS.

Electron mobility is comparable to record mobility with Hf-based oxides.
Gate leakage is one order of magnitude lower than that of ITRS.

Electron mobility is comparable to record mobility with Hf-based oxides.

**Benchmark of La-silicate dielectrics**


*T. Ando, et al., (IBM) IEDM 2009, p.423*
Introduction

High-k/metal gate on Si channel
- Gate first/last processes
- Threshold voltage
- Mobility
- Reliability
- EOT reduction toward 0.5 nm

Atomic layer deposition (ALD)
- Benchmark

New channel materials
Some conclusions
The main trick of atomic layer deposition (ALD) is the use of a self-limiting chemical reaction to control the thickness of the film deposited in a very accurate way.

http://rdweb.adm.nctu.edu.tw/modules/mod_table/files/2011011710065875-3-0.pdf
“Introduction to Atomic Layer Deposition (ALD)”
Fabrication method: HfO$_2$

Example: Overall reaction

HfCl$_4$ + 2H$_2$O $\rightarrow$ HfO$_2$ + 4HCl

1. HfCl$_4$ (gas)
2. HfCl$_4$ (Surface Monolayer) $\rightarrow$ purge

3. HfCl$_4$ (Surface Monolayer) + H$_2$O (gas)
4. HfO$_2$ (Surface Film) $\rightarrow$ purge

J. Robertson (Cambridge Univ), Rep. Prog. Phys. 69, 327, 2006
Residual carbon

Layer-by-Layer Deposition & Annealing (LL-D&A) can reduce carbon in the film through decomposition of precursors.

C<sub>m</sub>H<sub>n</sub> desorption

T. Nabatame, et al., (MIRAI) VLSI 2003, p.25
Multi chamber ALD/CVD system

- Hot-wall reactor with minimum dead volume.
- Capable of in-situ metal deposition and RTA.
  (La$_2$O$_3$ is hygroscopic)

**ALD of La$_2$O$_3$**


**Precursor (ligand)**

La(iPrCp)$_3$  
La(FAMD)$_3$

**ALD is indispensable from the manufacturing viewpoint**
- precise control of film thickness and good uniformity

1 cycle

1. La gas feed
2. Ar purge
3. H$_2$O feed
4. Ar purge
Self-limiting growth of $\text{La}_2\text{O}_3$

- $T_s < 175\,^\circ\text{C}$: Self-limiting (ALD)
- $T_s > 200\,^\circ\text{C}$: none self-limiting (ALD+CVD)

Properties of La$_2$O$_3$-ALD MOSFET


MOSFET operation
Mobility is decreased with decreasing the EOT regardless of high-k/metal gate structures.
EBEvaporation vs. CVD/ALD

**Mobility**

- Peak mobility (Vs)
- EOT (nm)

**Leakage current**

- Leakage current density (A/cm²)
- EOT (nm)

- Open : EB 蒸着
- Solid : ALD/CVD

- La₂O₃ (EB)
- CeOₓ/La₂O₃ (EB)
- CeOₓ/La₂O₃ (CVD/ALD)
- MgO/La₂O₃ (ALD)
- La₂O₃/La₂O₃ (CVD/ALD)
- La₂O₃/CeO₂ (CVD/ALD)

- Vₙ - Vₜₙb = 1V

- La₂O₃ + H₂ plasma
800 °C spike
EOT : 0.7nm
V_FB : -0.76V

500 °C 1min
EOT:1.38nm
V_FB : -0.17V

Spike PDA

1min PDA

※PMA(F.G) 500°C 30min

EOT=0.7nm:

 capacitance density (μF/cm²)

Gate Voltage (V)

3.5
3
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5

2  3  4

k ~ 17

k ~ 10

3nm

0.5nm
Low-temperature (>200°C): self-limiting was confirmed
Properties of La$_2$O$_3$-ALD layer

Silicate layer was formed due to react with Si

Low-permittivity silicate was formed in ALD process film

The dielectric constant in ALD film is lower than EB

CV curve is good agreement with ideal curve
Properties of La$_2$O$_3$-ALD layered MOSFET

175°C
EOT: 1.78 nm

W/L = 20/20 μm

Normal operation was confirmed
Outline

- Introduction
- **High-k/metal gate on Si channel**
  - Gate first/last processes
  - Threshold voltage
  - Mobility
  - Reliability
  - EOT reduction toward 0.5 nm
  - Atomic layer deposition (ALD)
- **Benchmark**
  - New channel materials
  - Some conclusions
## Si benchmark (nMOSFET)

<table>
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<tr>
<th>Gate stack</th>
<th>EOT</th>
<th>Mobility</th>
<th>$V_{th}$</th>
<th>SS</th>
<th>DIBL</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.52nm</td>
<td>110cm$^2$/Vs (at 1x10$^{13}$cm$^{-2}$)</td>
<td>~0.4V (L$_g$=24nm)</td>
<td>90mV/dec</td>
<td>147mV/V</td>
<td>IBM VLSI2011</td>
</tr>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.55nm</td>
<td>140cm$^2$/Vs (at 1MV/cm)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IBM VLSI2009</td>
</tr>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.45nm</td>
<td>115cm$^2$/Vs (at 1x10$^{13}$cm$^{-2}$)</td>
<td>0.3V (L$_g$=10um)</td>
<td>—</td>
<td>—</td>
<td>IMEC MEE2011</td>
</tr>
<tr>
<td>Metal/HfO$_2$</td>
<td>0.59nm</td>
<td>130cm$^2$/Vs (at 1MV/cm)</td>
<td>0.45V (L$_g$=1um)</td>
<td>75mV/dec</td>
<td>—</td>
<td>Sematech VLSI2009</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.65nm</td>
<td>—</td>
<td>0.3~0.4V (L$_g$=~30nm)</td>
<td>90mV/dec</td>
<td>100mV/V</td>
<td>Samsung VLSI2011</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.95nm</td>
<td>—</td>
<td>~0.3V (L$_g$=30nm)</td>
<td>100mV/dec</td>
<td>~200mV/V</td>
<td>Intel IEDM2009</td>
</tr>
<tr>
<td>W/La-silicate</td>
<td>0.62nm</td>
<td>155cm$^2$/Vs (at 1MV/cm)</td>
<td>-0.08V (L$_g$=10um)</td>
<td>~70mV/dec</td>
<td>—</td>
<td>Tokyo Tech. T-ED2012</td>
</tr>
</tbody>
</table>
• Introduction
• High-k/metal gate on Si channel
  • Gate first/last processes
  • Threshold voltage
  • Mobility
  • Reliability
  • EOT reduction toward 0.5 nm
  • Atomic layer deposition (ALD)
  • Benchmark

• New channel materials
• Some conclusions
High mobility channel materials


<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>electron mob. (cm²/Vs)</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
</tr>
<tr>
<td>electron effective mass (/m₀)</td>
<td>mᵣ: 0.19</td>
<td>mᵣ: 0.082</td>
<td>0.067</td>
<td>0.082</td>
<td>0.023</td>
<td>0.014</td>
</tr>
<tr>
<td></td>
<td>mₗ: 0.916</td>
<td>mₗ: 1.467</td>
<td>1.1</td>
<td>0.12</td>
<td>0.57</td>
<td>0.44</td>
</tr>
<tr>
<td>hole mob. (cm²/Vs)</td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td>hole effective mass (/m₀)</td>
<td>m_HH: 0.49</td>
<td>m_HH: 0.28</td>
<td>m_HH: 0.45</td>
<td>m_HH: 0.45</td>
<td>m_HH: 0.57</td>
<td>m_HH: 0.44</td>
</tr>
<tr>
<td></td>
<td>m_LH: 0.16</td>
<td>m_LH: 0.044</td>
<td>0.082</td>
<td>m_LH: 0.12</td>
<td>m_LH: 0.35</td>
<td>m_LH: 0.016</td>
</tr>
<tr>
<td>band gap (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.17</td>
</tr>
<tr>
<td>permittivity</td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

Better carrier transport

Higher drive current at low power supply
Issue in high mobility channel

A. Toriumi (Tokyo Uni), 7th Annual SEMATECH Symposium.

K. C. Saraswat, et al., (Stanford Univ)  
IEDM 2006, p.659

\[ SS = 2.3 \frac{k_B T}{q} \left( 1 + \frac{q^2 D_{it} + C_{dep}}{C_{ox}} \right) \]

Large \( D_{it} \): SS degradation  
(\( D_{it} \): Interface State Density)

\[ DIBL = 0.80 \varepsilon_{\text{semicon}} \varepsilon_{\text{ox}} \left( 1 + \frac{x_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{ds} \]

Large \( \varepsilon_{\text{semicon}} \): Strong short-channel effect  
(\( \varepsilon_{\text{semicon}} \): Semiconductor permittivity)

\[ \text{GIDL} \propto \frac{E^2}{\sqrt{E_G}} \exp \left( -\alpha \frac{E_G^{2/3}}{E} \right) \]

Small \( E_G \) value: Large \( I_{off} \) due to BTBT  
(\( E_G \): Semiconductor bandgap)
## Challenges for III-V CMOS technology

<table>
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<th>Issues</th>
<th>Approaches</th>
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<td>Integration With Si</td>
<td>Large lattice and thermal expansion mismatch</td>
<td>Direct growth on Si with thick buffer, wafer bonding</td>
</tr>
<tr>
<td>Interface State Density ($D_{it}$)</td>
<td>Fermi level pinning, large SS</td>
<td>Interface passivation, $D_{it}$ below $10^{11}$ cm$^2$eV$^{-1}$</td>
</tr>
<tr>
<td>Thermal stability of gate stack</td>
<td>Stability during 800°C S/D implant activation</td>
<td>Diffusion prevention by Interlayer (Al$_2$O$_3$~)</td>
</tr>
<tr>
<td>Source/Drain Resistance</td>
<td>Low dopant solubility and low activation</td>
<td>Highly doped technique, metal Schottky S/D</td>
</tr>
<tr>
<td>Mobility of PFET</td>
<td>Low hole mobility</td>
<td>Strained channel, Sb channels</td>
</tr>
</tbody>
</table>
Channel material growth on Si

Direct growth on Si with thick buffer

N. Mukherjee, et.al., (Intel) IEDM 2011

Si/GaAs lattice dislocation is close to Si sub interface, thus defects are confined at the interface.

Large buffer layer still needed for growth.

Plan view of QW from substrate side shows no defects for lattice matched InP substrate.
III-V material growth on Si

Wafer bonding

S. Takagi, et.al., (Tokyo Univ) IEDM 2010

Bond and anneal

<table>
<thead>
<tr>
<th>Al₂O₃</th>
<th>InGaAs</th>
<th>InP</th>
</tr>
</thead>
</table>

InP removal

<table>
<thead>
<tr>
<th>InGaAs</th>
<th>Al₂O₃</th>
<th>Si</th>
</tr>
</thead>
</table>

Selective growth

M. Deura, et.al., (Tokyo Univ) IEEE International conference on Indium Phosphide & Related material 2009

Lateral growth of InGaAs from nucleated InAs initially planted on Si

InGaAs-on-insulator on Si
With InGaAs thickness down to 3 nm
Oxide/III-V interface issues

Volatile and unstable native oxides of III-V material makes it imperative to remove them.

Removal of Ga and As oxides by sulfur passivation and annealing in F.G.

(AlD)Al\textsubscript{2}O\textsubscript{3}/InGaAs CV characteristics were improved.

H.D. Trinh et al., (NCTU)
Appl. Phys. Lett 2010, 97, 042903
Various surface passivation technique has been reported.
The asymmetry of the two C–V plots in accumulation hints that the $D_{it}$ distribution at TaSiO$_x$–InGaAs interface is non-parabolic.
Source Starvation in high-mobility FETs

Optimization of the source, channel and source/channel region can improve performance.

Scattering is needed in order to replenish carriers entering channel.

High doping density, raised S/D, thicker channel

Sufficiently large doping density in source and/or momentum relaxation are necessary to sustain carrier flow from the source.
InP capping layer act as a spacer between InGaAs channel and oxide/III-V interface.

1750 µS/µm at V_{DS}=0.5V
Gate all around InGaAs MOSFET


Inversion mode In$_{0.53}$Ga$_{0.47}$As MOSFET with ALD Al$_2$O$_3$/WN with well electrostatic properties

DIBL was suppressed down to $L_{ch} = 50$nm

$G_{m,max} = 701 \mu S/\mu m$ at $V_{ds} = 1V$
Tri-gate InGaAs QW-FET


Tri-gate structure has electrostatic superiority compared to ultra-thin body planar structure

Steepest SS and smallest DIBL ever reported ($W_{\text{fin}} = 30\text{nm}$)
Core-multishell InGaAs nanowires grown without buffer layer on Si substrate (bottom up approach)

At $V_d = 1$ V peak transconductance of 500 $\mu$S/$\mu$m is achieved (roughly x3 InGaAs nanowire)
Ni-InGaAs alloy can be formed at low temperatures with good rectifying characteristics.

Schottky barrier for electrons is lowered by increasing In content, high peak mobility of 2000 cm²V⁻¹s⁻¹ is reached.

InₓGa₁₋ₓAs

\[ X=\ln \]

<table>
<thead>
<tr>
<th>In</th>
<th>Mobility [cm²/Vs]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7</td>
<td>3000</td>
</tr>
<tr>
<td>0.8</td>
<td>3000</td>
</tr>
<tr>
<td>0.6</td>
<td>1000</td>
</tr>
<tr>
<td>0.53</td>
<td>1000</td>
</tr>
</tbody>
</table>

RTA 250°C 1min

Si MOSFETs

\[ N_A = 2 \times 10^{16} \text{ cm}^{-3} \]
Strain technology on InGaAs

S. Takagi, et al. (Tokyo Univ), IEDM2011, p.311.

Both uni- and bi-axial tensile strain result in significant carrier transport improvement.

Introduction of high In content buffer layer further improves the carrier mobility.

Channel engineering:
- High Indium content $\rightarrow$ enhance $\mu_{ph}$
- MOS interface buffer $\rightarrow$ enhance $\mu_{or}$

Physical understanding of carrier scattering
<table>
<thead>
<tr>
<th>Structure</th>
<th>Planar</th>
<th>FinFET</th>
<th>Tri-gate</th>
<th>GAA MOSFET</th>
<th>Metal S/D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric/EOT</td>
<td>8nm ALD Al$_2$O$_3$</td>
<td>5nm ALD Al$_2$O$_3$</td>
<td>not-reported</td>
<td>10nm ALD Al$_2$O$_3$</td>
<td>10nm ALD Al$_2$O$_3$</td>
</tr>
<tr>
<td>Mobility/g$_m$</td>
<td>1200 (cm$^2$/Vs)</td>
<td>~700 ($\mu$S/$\mu$m)</td>
<td>not-reported</td>
<td>701 ($\mu$S/$\mu$m)</td>
<td>2810 (cm$^2$/Vs)</td>
</tr>
<tr>
<td>L$_{ch}$ (nm)</td>
<td>500nm</td>
<td>100nm</td>
<td>50nm (W$_{fin}$=30 nm)</td>
<td>50nm (W$_{fin}$=30 nm)</td>
<td>Long channel</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>350</td>
<td>180</td>
<td>~50</td>
<td>210</td>
<td>-</td>
</tr>
<tr>
<td>SS (mV/dec)</td>
<td>240</td>
<td>145</td>
<td>~90 (66 mV/dec at L$_g$=20$\mu$m)</td>
<td>150</td>
<td>103</td>
</tr>
</tbody>
</table>
III-V devices have been out performing Si in high frequency region for a long time.
Ge surface passivation

- GeOS formation

- $D_{it}$ is decreased, however, further improvement is needed.

Ge surface passivation – cont’d


Si passivation

Sr passivation

![Diagram showing Ge surface passivation using Si and Sr as passivation layers.](image)
Soft GeO₂ network can provide a better stress relaxation at/near the interface compared to SiO₂, resulting in low interface state density.
The sharp increase of $k$ at $\sim 6$ eV is corresponding to the bandgap of GeO$_2$. The increase of $k$ around 5 ~ 6 eV suggests the sub-gap photo absorption.

$$k = \frac{\alpha \lambda}{4\pi}$$

$\alpha$: absorption coefficient
$\lambda$: wavelength
High pressure thermal oxidation is quite effective because of suppressing Ge diffusion.
By combined High pressure thermal oxidation and low temperature oxygen annealing, small \( D_{it} \) and higher channel mobility has been demonstrated.
Scalability of Ge MOS devices

High channel mobility has been demonstrated with $\text{Al}_2\text{O}_3/\text{GeO}_x$ gate stacks in 1nm EOT region fabricated by plasma post oxidation through $\text{Al}_2\text{O}_3$.

$R. \text{ Zhang, et al., (Tokyo Univ) IEDM2011, p.642.}$
Outline

- Introduction
- High-k/metal gate on Si channel
  - Gate first/last processes
  - Threshold voltage
  - Mobility
  - Reliability
  - EOT reduction toward 0.5 nm
  - Atomic layer deposition (ALD)
  - Benchmark
- New channel materials
- Some conclusions
Some Conclusions

Still many issues to be solved in high-k/metal gate stacks

- Gate first/last process strongly affect on threshold voltage.

- Mobility degradation is one of the critical issues.
  - Further understanding is necessary.

- BTI and TDDB lifetime is reduced by IL-scaling.
  - Reliability challenge for high-k/metal gate stack

- Direct contact high-k/Si structure is indispensable for continued EOT scaling.

- Interface & oxygen defect control must be accomplished for state-of-the-art MOSFET.

- Rapid progress has been made in gate stacks for III-V/Ge high mobility channel devices.
I would like to express deep appreciation to the following people:

Dr. Takamasa Kawanago and Mr. Darius Zade for the material preparation and useful discussion.

Prof. Kuniyuki Kakushima, Prof. Parhat Ahmet and other members of Iwai Laboratory for the research results used in the material.

Our research activities regarding high-k gate dielectrics was supported by New Energy and Industrial Technology Development Organization (NEDO)

Additional references:
• T. Kawanago, ‘A Study on High-k/Metal Gate Stack MOSFETs with Rare Earth Oxides’
• M. Kouda, ‘A Systematic Study of Rare-Earth Oxide for Charged Defect Reduction and EOT scaling in Gate Dielectrics’
Thank you very much for your kind attention!