Past and Future of Micro/Nano Electronic Devices

December 27, 2012

@Mahabalipuram, India

Hiroshi Iwai,
Tokyo Institute of Technology
• There were many inventions in the 20th century: Airplane, Nuclear Power generation, Computer, Space aircraft, etc

• However, everything has to be controlled by electronics

• Electronics

  Most important invention in the 20th century

• What is Electronics: To use electrons, Electronic Circuits
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Cathode (heated)  Grid  Anode (Positive bias)

Same mechanism as that of transistor
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
J. E. LILIENTHAL

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928

J.E.LILIENFELD

J.E.LILIENFELD
Capacitor structure with notch

Negative bias

- Gate Electrode
- Gate Insulator
- Semiconductor
- Electron

No current

Positive bias

- Electric field

Current flows
Surface Potential (Negative direction)

- **0V**
- **N⁺-Si**
- **Negative**
- **P-Si**
- **1V**
- **N-Si**

**Source Channel Drain**

**0 bias for gate**

**Positive bias for gate**

Electron flow
MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Use Gate Field Effect for switching

N-MOS (N-type MOSFET)
N-MOS (N-type MOSFET)

Source: n-Si

Gate

Drain: n-Si

Electron flow

Current flow

P-MOS (P-type MOSFET)

Source: p-Si

Gate

Drain: p-Si

Hole flow

Current flow
When NMOS is ON, PMOS is OFF
When PMOS is ON, NMOS is OFF
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator

Even Shockley!

Drain Current was several orders of magnitude smaller than expected
However, they found amplification phenomenon when investigating Ge surface when putting needles. This is the 1st Transistor: **Not MOSFET!** But Bipolar Transistor (another mechanism)

**1947: 1st transistor**

Bipolar using Ge

J. Bardeen

W. Bratten,

W. Shockley
1958: 1st Integrated Circuit

Connect 2 bipolar transistors in the Same substrate by bonding wire.

Jack S. Kilby
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si

Source

Drain

Al Gate

Si

SiO₂

Al

Si

Si/SiO₂ Interface is extraordinarily good
1970,71: 1st generation of LSIs

DRAM    Intel 1103

MPU      Intel 4004
2011
Most recent SD Card

Lexar Professional

128GB
133x Speed
Most Recent SD Card

128GB (Bite)
= 128G X 8bit = 1024Gbit
= 1.024T(Tera)bit

1T = 10^{12} = 1Trillion

World Population : 7 Billion
Brain Cell : 10~100 Billion
Stars in Galaxy : 100 Billion
Most Recent SD Card

Lexar Professional
128GB
133x Speed

Galaxy Image
128 GB = 1Tbit

2.4cm X 3.2cm X 0.21cm

Volume : 1.6cm³  Weight 2g

Voltage 2.7 - 3.6V

Old Vacuum Tube :
5cm X 5cm X 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit
**Old Vacuum Tube:**
5cm X 5cm X 10cm

1Tbit = 10,000 X 10,000 X 10,000 bit

Volume = (5cm X 10,000) X (5cm X 10,000) X (10cm X 10,000)
= 0.5km X 0.5km X 1km

- **Pingan International Finance Center**
  - Shanghai, China
  - (Year 2016)
  - Height: 700 m

- **Indian Tower**
  - Mumbai, India
  - (Year 2016)
  - Height: 700 m

- **Burj Khalifa**
  - Dubai, UAE
  - (Year 2010)
  - Height: 828 m

- **1Tbit**
  - 1,000 m X 500 m
Old Vacuum Tube: 100W

1Tbit = $10^{12}$bit

Power = $0.05\text{kW} \times 10^{12} = 50\text{ TW}$

Nuclear Power Generator

1MkW = 1BW

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving.
Brain: Integrated Circuits

Ear, Eye : Sensor

Mouth : RF/Opto device

Stomach : PV device

Hands, Legs : Power device
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years!!

313 billion dollar (US) in 2011

1,528 billion dollar (US) in 2025

By K. Kim, CSTIC 2012
MOS LSI experienced continuous progress for many years

<table>
<thead>
<tr>
<th>Name of Integrated Circuits</th>
<th>Number of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>1960s IC (Integrated Circuits)</td>
<td>~10</td>
</tr>
<tr>
<td>1970s LSI (Large Scale Integrated Circuit)</td>
<td>~1,000</td>
</tr>
<tr>
<td>1980s VLSI (Very Large Scale IC)</td>
<td>~10,000</td>
</tr>
<tr>
<td>1990s ULSI (Ultra Large Scale IC)</td>
<td>~1,000,000</td>
</tr>
<tr>
<td>2000s ?LSI (? Large Scale IC)</td>
<td>~1,000,000,000</td>
</tr>
</tbody>
</table>
CMOS Technology:
Indispensible for our human society

All the human activities are controlled by CMOS:
living, production, financing, telecommunication,
transportation, medical care, education,
entertainment, etc.

Without CMOS:
There is no computer in banks, and
world economical activities immediately stop.

Cellarer phone dose not exists
Downsizing of the components has been the driving force for circuit evolution.

<table>
<thead>
<tr>
<th>Year</th>
<th>Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>1900</td>
<td>Vacuum Tube</td>
</tr>
<tr>
<td>1950</td>
<td>Transistor</td>
</tr>
<tr>
<td>1960</td>
<td>IC</td>
</tr>
<tr>
<td>1970</td>
<td>LSI</td>
</tr>
<tr>
<td>2000</td>
<td>ULSI</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 cm</td>
</tr>
<tr>
<td>cm</td>
</tr>
<tr>
<td>mm</td>
</tr>
<tr>
<td>10 µm</td>
</tr>
<tr>
<td>100 nm</td>
</tr>
<tr>
<td>10^{-1}m</td>
</tr>
<tr>
<td>10^{-2}m</td>
</tr>
<tr>
<td>10^{-3}m</td>
</tr>
<tr>
<td>10^{-5}m</td>
</tr>
<tr>
<td>10^{-7}m</td>
</tr>
</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
<table>
<thead>
<tr>
<th>Feature Size/Technology Node</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1970) 10 µm → 8 µm → 6 µm → 4 µm → 3 µm → 2 µm → 1.2 µm → 0.8 µm → 0.5 µm → 0.35 µm → 0.25 µm → 180 nm → 130 nm → 90 nm → 65 nm → 45 nm → 32 nm → 22 nm (2012)</td>
</tr>
</tbody>
</table>

Averaged downsizing rate (in the past 42 years): $\sim 0.7X$ every 3 years

Total reduction in 19 generations: Gate Length $\sim 1/500$, Area $\sim 1/250,000$
Downsizing

1. Reduce Capacitance
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. Increase number of Transistors
   - Parallel processing
     - Increase circuit operation speed

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.
Why $t_{\text{ox}}$ thinning

$0V \text{ to } V_{\text{dd}}$ have to be decreased for better channel potential control $\rightarrow I_{\text{OFF}}$ Suppression

- Region governed by gate bias
- Region governed by drain bias
- DL touch with S Region (DL)

$0V < V_{\text{dep}} < 1V$

No $t_{\text{ox}}$ thinning

Large $I_{\text{OFF}}$
Scaling Method: by R. Dennard in 1974

W_{dep}: Space Charge Region (or Depletion Region) Width

W_{dep} has to be suppressed
Otherwise, large leakage between S and D

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

For example

$K = 0.7$

$X, Y, Z: K, V: K, Na: 1/K$

By the scaling, W_{dep} is suppressed in proportion, and thus, leakage can be suppressed.

$W_{dep} \propto \sqrt{V/Na}$

$I: K$

Good scaled I-V characteristics
### Downscaling merit: Beautiful!

<table>
<thead>
<tr>
<th>Geometry &amp; Supply voltage</th>
<th>$L_g$, $W_g$, $T_{ox}$, $V_{dd}$</th>
<th>$K$</th>
<th>Scaling ( K : K=0.7 ) for example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive current in saturation</td>
<td>$I_d$</td>
<td>$K$</td>
<td>$I_d = v_{sat} W_g C_o \left(V_g - V_{th}\right)$ ( C_o ) : gate $C$ per unit area ( \rightarrow W_g \left(t_{ox}^{-1}\right)\left(V_g - V_{th}\right) = W_g t_{ox}^{-1}\left(V_g - V_{th}\right) = K K^{-1} = K )</td>
</tr>
<tr>
<td>$I_d$ per unit $W_g$</td>
<td>$I_d/\mu m$</td>
<td>1</td>
<td>$I_d$ per unit $W_g = I_d / \mu m = 1$</td>
</tr>
<tr>
<td>Gate capacitance</td>
<td>$C_g$</td>
<td>$K$</td>
<td>$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox}$ ( \rightarrow ) $K K/K = K$</td>
</tr>
<tr>
<td>Switching speed</td>
<td>$\tau$</td>
<td>$K$</td>
<td>$\tau = C_g V_{dd}/I_d$ ( \rightarrow ) $K K/K = K$</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>$f$</td>
<td>$1/K$</td>
<td>$f = 1/\tau = 1/K$</td>
</tr>
<tr>
<td>Chip area</td>
<td>$A_{chip}$</td>
<td>$\alpha$</td>
<td>$\alpha$: Scaling factor ( \rightarrow ) In the past, $\alpha &gt; 1$ for most cases</td>
</tr>
<tr>
<td>Integration (# of Tr)</td>
<td>$N$</td>
<td>$\alpha/K^2$</td>
<td>$N \rightarrow \alpha/K^2 = 1/K^2$, when $\alpha=1$</td>
</tr>
<tr>
<td>Power per chip</td>
<td>$P$</td>
<td>$\alpha$</td>
<td>$fN C V^2/2 \rightarrow K^{-1}(\alpha K^{-2}) K (K^{-1})^2 = \alpha = 1$, when $\alpha=1$</td>
</tr>
<tr>
<td></td>
<td>$k = 0.7$ and $\alpha = 1$</td>
<td>$k = 0.7^2 = 0.5$ and $\alpha = 1$</td>
<td></td>
</tr>
<tr>
<td>-------------------------</td>
<td>-----------------------------</td>
<td>-------------------------------------</td>
<td></td>
</tr>
<tr>
<td><strong>Single MOFET</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vdd</td>
<td>$0.7$</td>
<td>Vdd</td>
<td></td>
</tr>
<tr>
<td>Lg</td>
<td>$0.7$</td>
<td>Lg</td>
<td></td>
</tr>
<tr>
<td>Id</td>
<td>$0.7$</td>
<td>Id</td>
<td></td>
</tr>
<tr>
<td>Cg</td>
<td>$0.7$</td>
<td>Cg</td>
<td></td>
</tr>
<tr>
<td>$P ,(\text{Power})/\text{Clock}$</td>
<td>$0.7^3 = 0.34$</td>
<td>$P ,(\text{Power})/\text{Clock}$</td>
<td></td>
</tr>
<tr>
<td>$\tau , (\text{Switching time})$</td>
<td>$0.7$</td>
<td>$\tau , (\text{Switching time})$</td>
<td></td>
</tr>
<tr>
<td><strong>Chip</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N ($# \text{ of Tr}$)</td>
<td>$1/0.7^2 = 2$</td>
<td>N ($# \text{ of Tr}$)</td>
<td></td>
</tr>
<tr>
<td>f ($\text{Clock}$)</td>
<td>$1/0.7 = 1.4$</td>
<td>f ($\text{Clock}$)</td>
<td></td>
</tr>
<tr>
<td>P ($\text{Power}$)</td>
<td>$1$</td>
<td>P ($\text{Power}$)</td>
<td></td>
</tr>
</tbody>
</table>
Actual past downscaling trend until year 2000

Change in 30 years

<table>
<thead>
<tr>
<th></th>
<th>Ideal scaling</th>
<th>Real Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-2}$</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-2}$</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-1}$</td>
</tr>
<tr>
<td>$A_{chip}$</td>
<td>$\alpha$</td>
<td>$10^1$</td>
</tr>
</tbody>
</table>

| $I_d/\mu m$             | $1$           | $10^1$      |
| $\alpha$                | $\alpha/K^2(10^5)$ | $10^4$      |

Past 30 years scaling

Merit: $N$, $f$ increase

Demerit: $P$ increase

$V_{dd}$ scaling insufficient

Additional significant increase in $I_d$, $f$, $P$

Vd scaling insufficient, $\alpha$ increased  →  $N$, $I_d$, $f$, $P$ increased significantly

Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1µm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5µm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25µm:</td>
<td>Direct-tunneling of gate SiO$_2$</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1µm:</td>
<td>‘0.1µm brick wall’(various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
Historically, many predictions of the limit of downsizing. VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.
C. Mead    L. Conway
Finally, there appears to be a fundamental limit of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide .... begin to make the devices of smaller dimension unworkable.
Direct-tunneling effect

Direct tunneling leakage current start to flow when the thickness is 3 nm.
Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide

- $V_g = 2.0\text{V}$
- $V_d$ (V)
- $I_d$ (mA/μm)
Gate leakage: \( I_g \propto \text{Gate Area} \propto \text{Gate length (Lg)} \)

Drain current: \( I_d \propto \frac{1}{\text{Gate length (Lg)}} \)

\( L_g \rightarrow \text{small}, \)

Then, \( I_g \rightarrow \text{small}, \) \( I_d \rightarrow \text{large}, \)

Thus, \( \frac{I_g}{I_d} \rightarrow \text{very small} \)
Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!

Some one will think for you
Transistor Scaling Continues

Qi Xinag, ECS 2004, AMD
Downsizing limit?

Channel length?

10 nm

Electron wave length

Gate Oxidation

Channel
5 nm gate length CMOS
Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC

IEDM, 2003
Electron wave length

10 nm

Tunneling distance

3 nm

Downsizing limit!

Channel length
Gate oxide thickness
Electron wave length

10 nm

Tunneling distance

3 nm

Atom distance

0.3 nm

MOSFET operation

$L_g = 2 \sim 1.5$ nm?

Below this, no one knows future!
Subthreshold leakage current of MOSFET

Subthreshold leakage current of MOSFET

Subthreshold leakage current is OK at Single Tr. level

But not OK For Billions of Trs.

Vg=0V

Subthreshold region

Vth (Threshold Voltage)
Subthreshold leakage current will limit the downsizing
The limit is different depending on application.
However, Gate oxide thickness 2 orders magnitude smaller Close to limitation!!

Lg: Gate length downsizing will continue to another 10-15 years
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
So, we are now in the limitation of downsizing?

Do you believe this or do not?
To use high-k dielectrics

K: Dielectric Constant

Thin \( \text{SiO}_2 \)

- \( K=4 \)
- Almost the same electric characteristics

Thick high-k dielectrics

- \( K=20 \)
- 5 times thicker
- Small leakage Current

However, very difficult and big challenge!
Subthreshold leakage current of MOSFET

Subthreshold leakage current of MOSFET is OK at Single Tr. level but not OK for Billions of Trs.

Vg=0V

Subthreshold leakage current

Ion

loff

Vth (Threshold Voltage)

OFF

ON

Subthreshold region
Subthreshold leakage current will limit the downsizing
The limit is different depending on application.
How far can we go for production?

<table>
<thead>
<tr>
<th>Past</th>
<th>0.7 times per 3 years</th>
<th>In 40 years: 18 generations, Size 1/300, Area 1/100,000</th>
</tr>
</thead>
</table>

1970年
10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm → 0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

<table>
<thead>
<tr>
<th>Now</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td>→ (28nm)</td>
<td>→ 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?</td>
</tr>
</tbody>
</table>

• At least 4,5 generations to 8 ~ 5 nm
Suppression of subthreshold leakage by surrounding gate structure

Planar

Surrounding gate
Because of off-leakage control,

Planar $\rightarrow$ Fin $\rightarrow$ Nanowire
Nanowire structures in a wide meaning

Fin

Tri-gate

Ω-gate

All-around
More Moore to More More Moore

Technology node

<table>
<thead>
<tr>
<th>65nm</th>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$ 35nm</td>
<td>$L_g$ 30nm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Now

Future

15nm, 11nm, 8nm, 5nm, 3nm

Main stream (Fin, Tri, Nanowire)

Planar

Si

Tri-Gate

Si is still main stream for future!!

Si channel

ET: Extremely Thin

Alternative (III-V/Ge)

Emerging Devices

Others

Alternative (ETSOI)

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)
High-k gate dielectrics

Hf-based oxides

<table>
<thead>
<tr>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
<th>15nm, 11nm, 8nm, 5nm, 3nm,</th>
</tr>
</thead>
<tbody>
<tr>
<td>EOT:1.0 nm</td>
<td>EOT:0.95 nm</td>
<td>EOT:0.9 nm</td>
<td></td>
</tr>
</tbody>
</table>

SiO₂ IL (Interfacial Layer) is used at Si interface to realize good mobility.

Continued research and development

SiO₂ IL (Interfacial Layer)

EOT=0.52 nm
Remote SiO₂-IL scavenging HfO₂ (IBM)

SiO₂ IL (Interfacial Layer) is used at Si interface to realize good mobility.

Technology for direct contact of high-k and Si is necessary.

HfO₂/SiO₂ (IBM)

EOT=0.9 nm

HfO₂/SiO₂ (IBM)

HfO₂/SiO₂ (IBM)

HfO₂/SiO₂ (IBM)

HfO₂/SiO₂ (IBM)

EOT=0.37 nm

EOT=0.40 nm

EOT=0.48 nm

0.48 nm - 0.37 nm Increase of I_d at 30%

Direct contact with La-silicate (Tokyo.Tech)

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM2009, (IBM)
I_{ON} and I_{OFF} benchmark

**NMOS**

- **Intel [1]**
  - Bulk 32nm Tri-Gate 22nm
  - $V_{DD}=0.8V$
  - $V_{DD}=0.8V$

- **Intel [2]**
  - Bulk 45nm
  - $V_{DD}=1V$

- **Samsung [3]**
  - Bulk 20nm
  - $V_{DD}=0.9V$

- **IBM [5]**
  - GAA NW
  - $V_{DD}=1V$

- **IBM [6]**
  - FinFET 25nm
  - $V_{DD}=1V$

- **IBM [7]**
  - ETSOI
  - $V_{DD}=1V$

- **STMicro. [8]**
  - GAA NW
  - $V_{DD}=1.1V$

**PMOS**

- **Intel [1]**
  - Bulk 32nm Tri-Gate 22nm
  - $V_{DD}=0.8V$

- **Intel [2]**
  - Bulk 45nm
  - $V_{DD}=1V$

- **IBM [10]**
  - ETSOI
  - $V_{DD}=0.9V$

- **IBM [7]**
  - ETSOI
  - $V_{DD}=1V$

- **Samsung [3]**
  - Ω-gate NW
  - $V_{DD}=1V$

- **IBM [6]**
  - FinFET 25nm
  - $I_{eff}=1V$

- **IBM [7]**
  - ETSOI
  - $V_{DD}=1V$

- **STMicro. [8]**
  - GAA NW
  - $V_{DD}=1.1V$

References:

1. C. Auth et al., pp.131, VLSI2012 (Intel).
4. S. Saitoh et al., pp.11, VLSI2012 (Toshiba).
5. S. Bangsaruntip et al., pp.297, IEDM2009 (IBM).
7. A. Khakifirooz et al., pp.117, VLSI2012 (IBM).
9. S. Sato et al., pp.361, ESSDERC2010 (Tokyo Tech.).
10. K. Cheng et al., pp.419, IEDM2012 (IBM).
\( L_g \) and EOT are larger than ITRS requirements

Implementation of Tri-gate and lower \( V_{th}/V_{dd} \) since 22nm

K. Mistry et al., pp.247, IEDM2007 (Intel).
P. Packan et al., pp.659, IEDM2009 (Intel).
C. Auth et al., pp.131, VLSI2012 (Intel).
## Benchmark of device characteristics

<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Lg (nm)</td>
<td>35</td>
<td>30</td>
<td>30</td>
<td>14</td>
<td>22</td>
<td>20</td>
<td>35/25</td>
<td>22/30</td>
</tr>
<tr>
<td>Gate Dielectrics</td>
<td>Hf-based</td>
<td>Hf-based</td>
<td>SiO₂</td>
<td>HfO₂</td>
<td>HfO₂ ?</td>
<td>Hf-based</td>
<td>HfZrO₂</td>
<td>SiO₂</td>
</tr>
<tr>
<td>EOT (nm)</td>
<td>1</td>
<td>0.95</td>
<td>0.9</td>
<td>3</td>
<td>~1</td>
<td>-</td>
<td>1.5</td>
<td>-</td>
</tr>
<tr>
<td>Vth (V)</td>
<td>~0.4</td>
<td>~0.3</td>
<td>~0.2</td>
<td>~0.15 (nFET)</td>
<td>0.3~0.4</td>
<td>~0.3</td>
<td>0.3~0.4</td>
<td>~0.5</td>
</tr>
<tr>
<td>VDD (V)</td>
<td>1</td>
<td>1</td>
<td>0.8</td>
<td>1</td>
<td>0.9</td>
<td>0.9</td>
<td>1</td>
<td>1.1</td>
</tr>
<tr>
<td>ION (mA/um) nFET/pFET</td>
<td>1.36/1.07</td>
<td>1.53/1.23</td>
<td>1.26/1.1</td>
<td>0.83 (nFET)</td>
<td>0.59/0.62 (Ieff)</td>
<td>1.2/1.05</td>
<td>0.83/0.95</td>
<td>2.05/1.5</td>
</tr>
<tr>
<td>DIBL (mV/V) nFET/pFET</td>
<td>~150</td>
<td>~200</td>
<td>46/50</td>
<td>&lt;50</td>
<td>-</td>
<td>104/115</td>
<td>65/105</td>
<td>56/9</td>
</tr>
<tr>
<td>SS (mV/dec)</td>
<td>-</td>
<td>~100</td>
<td>~70</td>
<td>&lt;80</td>
<td>-</td>
<td>87</td>
<td>85</td>
<td>&lt;80</td>
</tr>
</tbody>
</table>
### Short-channel effect

T. Skotnicki, IEDM 2009 Short Course (STMicroelectronics)

\[
SCE = 0.64 \frac{\varepsilon_S}{\varepsilon_{ox}} \times E_l \times \Phi_d
\]

\[
DIBL = 0.8 \frac{\varepsilon_S}{\varepsilon_{ox}} \times E_l \times V_{ds}
\]

<table>
<thead>
<tr>
<th>Channel</th>
<th>Expression</th>
<th>Min. Length (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk</td>
<td>(E_l = 1 \times \left(1 + \frac{X_l^2}{L_{el}^2}\right) \times \frac{T_{ox}}{L_{el}} \times \frac{T_{dep}}{L_{el}})</td>
<td>34</td>
</tr>
<tr>
<td>PD SOI</td>
<td>(E_l = 1 \times \left(1 + \frac{X_l^2}{L_{el}^2}\right) \times \frac{T_{ox} T_{dep}}{L_{el}^2})</td>
<td>34</td>
</tr>
<tr>
<td>Thick BOX FD SOI</td>
<td>(E_l = 1 \times \left(1 + \frac{T_{ox}^2}{L_{el}^2}\right) \times \frac{T_{ox} T_{si}}{L_{el}} + \lambda T_{box})</td>
<td>≈ 30</td>
</tr>
<tr>
<td>UTBB (FD SOI or SON)</td>
<td>(E_l = 1 \times \left(1 + \frac{T_{ox}^2}{L_{el}^2}\right) \times \frac{T_{ox} T_{si} + \lambda T_{box}}{L_{el}})</td>
<td>≈ 10</td>
</tr>
<tr>
<td>FinFET (independent gates)</td>
<td>(E_l = 1 \times \left(1 + \frac{T_{ox}^2}{L_{el}^2}\right) \times \frac{T_{ox} T_{si}}{L_{el}^2})</td>
<td>≈ 6</td>
</tr>
<tr>
<td>FinFET (common gates)</td>
<td>(E_l = 1 \times \left(1 + \frac{T_{si}^2}{4 L_{el}^2}\right) \times \frac{T_{ox} T_{si}}{L_{el}^2})</td>
<td>≈ 2.7</td>
</tr>
</tbody>
</table>

- If max ch. doping is 10^{18} cm^{-3} \(\Rightarrow T_{ox} \approx 12\) nm then:
- If max ch. doping is 10^{20} cm^{-3} \(\Rightarrow T_{ox} \approx 12\) nm then:
- \(T_{box} = 145\) nm
- \(\lambda T_{box} = 18\) nm
- If \(T_{si} < 3\) nm then:
- \(T_{box} = 10\) nm
- \(\lambda T_{box} = 0.46\) nm
- \(\approx 0\) nm

Tsi/2 plays role of Xj, and that of Tdep, if minimum feasible Tsi is supposed 3 nm, then:

- \(L_{el, min} = 34\) nm
- \(L_{el, min} = 34\) nm
- \(L_{el, min} \approx 30\) nm
- \(L_{el, min} \approx 10\) nm
- \(L_{el, min} \approx 6\) nm
- \(L_{el, min} \approx 2.7\) nm
Drain-induced barrier lowering

\[ DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \left( \frac{T_{ox}}{L_{el}} \right) \left( \frac{T_{dep}}{L_{el}} \right) V_{DS} \]

- **Bulk**
  - \( T_{dep} = \frac{3}{4} L_{el} \)
  - 140 mV/V

- **III-V**
  - \( X_j = \frac{3}{4} L_{el} \)
  - 210 mV/V

- **FDSOI**
  - \( T_{dep} = T_{si} \)
  - \( T_{si} \geq 6 \text{ nm} \)
  - 110 mV/V

- **ETSOI**
  - \( X_j = T_{si} \)
  - 80 mV/V

- **FinFET**
  - \( T_{dep} = \frac{T_{si}}{2} \)
  - \( X_j = \frac{T_{si}}{2} \)
  - \( T_{si} \geq 10 \text{ nm} \)
  - 70 mV/V

- **UTBB**
Sub-threshold Slope

\[ S = \frac{kT}{q} \ln \left( 1 + \frac{C_{dep}}{C_{ox}} + \frac{\varepsilon_{Si} T_{ox} X_j}{\varepsilon_{ox} L_{el} L_{el} L_{el}} \sqrt{\frac{1 + 3T_{dep}}{4L_{el}}} \right) \left( 1 + 2 \frac{V_{ds}}{\Phi_d} \right) \]

BULK
- \( T_{dep} = 3/4L_{el} \)
- \( X_j = 3/4L_{el} \)
- 95 mV/dec

III-V
- \( T_{ox} + 2A \)
- \( \varepsilon_{Si} + 15\% \)
- 110 mV/dec

FDSOI
- \( T_{dep} = T_{si}/2 \)
- \( X_j = T_{si}/2 \)
- 85 mV/dec

FinFET
- \( T_{dep} = T_{si} + \lambda T_{box} \)
- \( X_j = T_{si} \)
- 75 mV/dec

ETSOI
- 65 mV/dec

UTBB
- RBB => Pstat
- 65 mV/dec
The down scaling of MOSFETs is still possible for at least another 10 years!

4 important technological items for down scaling.

New structures
1. Wire channel

New materials
2. Thinning of high-k gate oxide thickness beyond 0.5 nm
3. Metal(Silicide) S/D

4. III-V/Ge channel, for the moment, however, very difficult to replace Si
These technologies are very difficult and not every company can succeed in the development timely.

In the past, technology comes with the purchase of equipment, but any more.

Thus, some of the companies are in the threat of dropping off.

There are so many rooms for the universities to contribute to the development of Si world.
Wire channel
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of $I_{OFF}$
3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Compact modeling of nanowire MOSFETs is very difficult
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Wire cross section dependence.
What cross section gives best solution for SCE suppression and drive current?

By Profs. Oshiyama and Iwata, U. of Tokyo
Compact model for circuit designer is very important

- **Diffusive transport**
  - $L \gg \lambda$
  - Mobility
  - Theory

- **Quasi-Ballistic transport**
  - $L \sim \lambda$

- **Ballistic transport**
  - $L < \lambda$

Real nanoscale MOSFETs

Prof. K. Natori of TIT
Prof. K. Natori of TIT
チャネル内の電子散乱導入の考え方

透過確率

\[ T(\varepsilon) = \frac{(F(0) - G(0))}{F(0)} \]

ドレインからの入射 = 0

初期弹性散乱域

後方弹性散乱が支配

後方弹性散乱 + (光学フォノン放出)

光学フォノン放出可能域

Prof. K. Natori of TIT
散乱の導入に係る計算式

弾性散乱域

\[
\sqrt{\frac{2}{m}} (qE_x + \varepsilon) \frac{dF(x)}{dx} + \frac{B_0}{\sqrt{qE_x + \varepsilon}} \{F(x) - G(x)\} = 0
\]

\[
-\sqrt{\frac{2}{m}} (qE_x + \varepsilon) \frac{dG(x)}{dx} + \frac{B_0}{\sqrt{qE_x + \varepsilon}} \{G(x) - F(x)\} = 0
\]

光学フォノン放出域

\[
\sqrt{\frac{2}{m}} (qE_x + \varepsilon) \frac{dF(x)}{dx} + \frac{B_0}{\sqrt{qE_x + \varepsilon}} \{F(x) - G(x)\} + \frac{2D_0}{\sqrt{qE_x + \varepsilon - \varepsilon^*}} F(x) = 0
\]

\[
-\sqrt{\frac{2}{m}} (qE_x + \varepsilon) \frac{dG(x)}{dx} + \frac{B_0}{\sqrt{qE_x + \varepsilon}} \{G(x) - F(x)\} + \frac{2D_0}{\sqrt{qE_x + \varepsilon - \varepsilon^*}} G(x) = 0
\]

ソースからドレインへの透過確率 (エネルギー \( \varepsilon \) に対して)

\[
T(\varepsilon) = \frac{\sqrt{2D_0 qE}}{\left(\sqrt{B_0 + D_0} + \sqrt{D_0}\right) qE + \sqrt{2mD_0B_0} \ln\left(\frac{qE_x + \varepsilon}{\varepsilon}\right)}
\]

Prof. K. Natori of TIT

\(F(x)/h\) は、正速度フラックス

\(G(x)/h\) は、負速度フラックス

物理パラメータ\(B_0\)の値は移動度対応した値

物理パラメータ\(D_0\)の光学フォノンエネルギー緩和時間に対応した値

電子=+

\(qE_x + \varepsilon\)
Prof. K. Natori of TIT
Experiment
Quasi ballistic $V_g - V_{th} = 1V$
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off > 10^6, 60uA/wire

L_g = 65nm, T_ox = 3nm
Bench Mark

Gate Length (nm)

I\text{ON} (\mu\text{A} / \text{wire})

nMOS
pMOS

V_{\text{DD}}: 1.0\sim 1.5 \text{ V}

Our Work

102\mu\text{A} (10\times 20)

括弧内は寸法を示す

(10\times 20)
(13\times 20)
(9\times 14)
(12\times 19)
(10)
(30)
(19)
(13)
(10)
(8)
(12)
(5)
(3)
(3)
(10)
(8)
(10)
(10)
(12)
(5)
(3)
(30)
(19)

µ\text{A}

VDD: 1.0~1.5 V

Our Work

Gate Length (nm)
This work

Planer FET
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

Si nanowireFET
Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240

\( I_{ON} / I_{OFF} \) Bench mark

\[
\begin{align*}
L_g &= 500 \sim 65 \text{nm} \\
1.0 \sim 1.1 \text{V} \\
1.2 \sim 1.3 \text{V}
\end{align*}
\]
Electron Density (x10^{19} cm^{-3})

Distance from SiNW Surface (nm)

(a) Metal
12 nm
19 nm
SiO_2

(b) Inversion areal ratio: 29 %
12 nm
39 nm

Edge portion
Flat portion

Electron Density

V_g = 1 V
Tri-gate has been implemented at 22nm node, enabling further scaling

<table>
<thead>
<tr>
<th></th>
<th>HP</th>
<th>MP</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{OX,E}$ (nm)</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>$L_{GATE}$ (nm)</td>
<td>30</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>$I_{OFF}$ (nA/um)</td>
<td>20-100</td>
<td>5-20</td>
<td>1-5</td>
</tr>
</tbody>
</table>
PMOS channel under the gate

S/D region showing the SiGe epitaxy

A fin width of 8nm to balance SCE and $R_{\text{ext}}$

A fin height of 34nm to balance drive current vs. capacitance
SS of 69 and 72mV/dec for NMOS and PMOS, respectively
DIBL of 46 and 50mV/V for NMOS and PMOS, respectively
$V_{th}$ of 22nm is about 0.1V lower than that of 32nm
Extremely Thin SOI (ETSOI)

- $L_g = 22\text{nm}$ ETSOI
- Si channel thickness of 6 nm
- DIBL of 75 mV/V and 130 mV/V for NFET and PFET
GATE ALL AROUND NANOWIRE (GAA NW)

- $L_g = 25\sim35\text{nm}$ GAA NW
- Hydrogen anneal provides smooth channel surface
- Competitive with conventional CMOS technologies
- Scaling the dimensions of NW leads to suppressed SCE
Problems in Multi-gate

S. Bangsaruntip et al., pp.297, IEDM2009 (IBM),
K. Tachi et al., pp.313, IEDM2009 (CEA-LETI)

Decreasing the diameter of NW

Improved short-channel control ↔ Severe mobility degradation
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-k is necessary.
Problems in SOI

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.
Wire/fin mitigates EOT thinning trend (Trend 1 $\rightarrow$ Trend 2) Because of better SCE control.

However, $I_{ON}$ severely degrade with wire/fin width reduction

Therefore, EOT trend will become accelerated again (Trend 2 $\rightarrow$ Trend 3) $\rightarrow$ Thus, high-k becomes important again.
High-$k$

beyond 0.5 nm
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Flat metal/high-k interface for better mobility
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Interface dipole control for $V_{th}$ tuning
- Suppression of FLP
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
- Reliability: PBTI, NBTI, TDDB
- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Interface dipole control for $V_{th}$ tuning
- Suppression of FLP
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band offset

Oxide

Si

Dielectric Constant

Band Discontinuity [eV]

0 10 20 30 40 50

Dielectric Constant $\varepsilon(0)$

Lu$_2$O$_3$, Gd$_2$O$_3$, La$_2$O$_3$, ZrO$_2$, HfO$_2$

Si Band Gap

XPS measurement by Prof. T. Hattori, INFOS 2003
Choice of High-k elements for oxide

Candidates □

Unstable at Si interface
- Si + MOₓ M + SiO₂
- Si + MOₓ MSiₓ + SiO₂
- Si + MOₓ M + MSiₓOᵧ

Gas or liquid at 1000 K

Radio active □ He

B C N O F Ne

Al Si P S Cl Ar

K Ca Sc Ti V Cr Mn Fc Co Ni Cu Zn Ga Ge As Se Br Kr

Sr Y Zr Nb Mo Tc Ru Rb Pd Ag Cd In Sn Sb Te I Xe

Cs Ba Hf Ta W Re Os Ir Pt Au Hg Ti Pb Bi Po At Rn

Fr Ra Ac Th Pa U Np Pu Am Cm Bk Cf Es Fm Md No Lr

HfO₂ based dielectrics are selected as the first generation materials, because of their merit in:
1) band-offset, 2) dielectric constant, 3) thermal stability.

La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

Candidates □

Si + MOₓ M + SiO₂
- Si + MOₓ MSiₓ + SiO₂
- Si + MOₓ M + MSiₓOᵧ

Choice of High-k elements for oxide are selected as the first generation materials, because of their merit in:
1) band-offset, 2) dielectric constant, 3) thermal stability.

R. Hauser, IEDM Short Course, 1999
Direct high-k/Si by silicate reaction

Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface
Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O$^*$ $\rightarrow$ HfO$_2$ + SiO$_2$

Oxygen supplied from W gate electrode

H. Shimizu, JJAP, 44, pp. 6131

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction

D.J. Lichtenwalner, Trans. ECS 11, 319
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$

- La$_2$SiO$_5$, La$_2$Si$_2$O$_7$,
- La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
For the past 45 years, SiO₂ and SiON have been used as gate insulators. The EOT limit is 0.7~0.8 nm. Today, EOT=1.0 nm. One order of magnitude improvement is needed. The introduction of High-k materials can reduce EOT further beyond 0.5 nm, allowing direct contact to Si.

EOT can be reduced further beyond 0.5 nm by using direct contact to Si. This can be achieved by choosing appropriate materials and processes.
High-k/metal gate stack film deposition cluster tool
Gate Leakage vs EOT, (Vg=|1|V)

- Current density (A/cm²) vs EOT (nm)
- Materials: Al₂O₃, HfAlO(N), HfO₂, HfSiO(N), HfTaO, La₂O₃, Nd₂O₃, Pr₂O₃, PrSiO, PrTiO, SiON/SiN, Sm₂O₃, SrTiO₃, Ta₂O₅, TiO₂, ZrO₂(N), ZrSiO, ZrAlO(N)
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small $D_{it}$

- Silicate-reaction-formed fresh interface
- Stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress


No interfacial layer can be confirmed with Si/TiN/W
$D_{it}$, $D_{slow}$

(GP anneal)

$G_p/\omega$ (F/cm²)

$\omega$ (rad/s)

$D_{it}$, $D_{slow}$ (cm⁻²/eV)

Annealing temperature (°C)

$D_{it}$, $D_{slow}$
It is important to change the La$_2$O$_3$ to La-silicate completely.
As-depo

La₂O₃(3.5 nm)

W(60 nm)

Annealed for 2 s

TiN/W(6 nm)

Annealing temperature (°C)

EOT (nm)

TiN(45nm)/W(6nm)

EOT=0.55nm

TaN/(45nm)/W(3nm)

900°C, 30min

Experiment

Cᵥᵥ(Theory)

Cᵥᵥ(Experiment)

Vg (V)

Cᵥᵥ(Theory)

EOT=0.55nm
TaN(45nm)/W(3nm)

$Q_{fix} = 1 \times 10^{11} \text{ cm}^{-2}$

900°C, 30min

Fixed Charge density: $1 \times 10^{11} \text{ cm}^{-2}$
**EOT = 0.53nm**

- L/W = 20/20 µm
- T = 300K
- N_{sub} = 3 \times 10^{16} cm^{-3}

**Electron Mobility [cm^2/Vsec]**

- \( V_g = 1.0V \)
- \( V_g = 0.8V \)
- \( V_g = 0.6V \)
- \( V_g = 0.4V \)
- \( V_g = 0.2V \)

- \( V_g = 0V \)

\[
\begin{align*}
\text{Drain Voltage (V)} & \quad \text{Drain Current (µA)} \\
50 & \quad 150 & \quad 250 & \quad 300 \\
50 & \quad 100 & \quad 150 & \quad 200 & \quad 250 \\
\end{align*}
\]

**E_{eff} = 1 MV/cm**

- 150 cm^2/Vs

**Si-sub**

- Si-sub
- Si-sub
- TaN/Al
- La_{2}O_{3}

**Drain Current (µA)**

- Drain Voltage (V)
- Drain Current (µA)
- Electron Mobility [cm^2/Vsec]

\[
\begin{align*}
E_{eff} & = 1 MV/cm \\
150 & = 151 cm^2/Vs \\
150cm^2/Vs & \\
E_{O} & = 0.53nm \\
L/W & = 20/20µm \\
T & = 300K \\
N_{sub} & = 3 \times 10^{16} cm^{-3} \\
\end{align*}
\]
Gate current (A/cm²) vs. Gate voltage (V) for a TaN/W/LaSiOₓ/nFET with Wₙ/Lₙ = 20/20 µm and EOT = 0.55 nm. ITRS specification is also shown, with a zoom factor of x1/100.
EOT=0.40nm
Benchmark of La-silicate dielectrics

Gate leakage is two orders of magnitude lower than that of ITRS.

Electron mobility is comparable to record mobility with Hf-based oxides.


T. Ando, et al., (IBM) IEDM 2009, p.423
Gate leakage is one order of magnitude lower than that of ITRS.

Electron mobility is comparable to record mobility with Hf-based oxides.
## Si benchmark (nMOSFET)

<table>
<thead>
<tr>
<th>Gate stack</th>
<th>EOT</th>
<th>Mobility</th>
<th>$V_{th}$</th>
<th>SS</th>
<th>DIBL</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.52nm</td>
<td>110cm$^2$/Vs (at 1x10$^{13}$cm$^{-2}$)</td>
<td>~0.4V (L$_g$=24nm)</td>
<td>90mV/dec</td>
<td>147mV/V</td>
<td>IBM VLSI2011</td>
</tr>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.55nm</td>
<td>140cm$^2$/Vs (at 1MV/cm)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IBM VLSI2009</td>
</tr>
<tr>
<td>Metal$^{(A)}$/Cap/HfO$_2$</td>
<td>0.5nm</td>
<td>110cm$^2$/Vs (at 0.8MV/cm)</td>
<td>0.3V (L$_g$=1um)</td>
<td>—</td>
<td>—</td>
<td>IMEC IEDM2009</td>
</tr>
<tr>
<td>Metal/HfO$_2$</td>
<td>0.59nm</td>
<td>130cm$^2$/Vs (at 1MV/cm)</td>
<td>0.45V (L$_g$=1um)</td>
<td>75mV/dec</td>
<td>—</td>
<td>Sematech VLSI2009</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.65nm</td>
<td>—</td>
<td>0.3~0.4V (L$_g$=~30nm)</td>
<td>90mV/dec</td>
<td>100mV/V</td>
<td>Samsung VLSI2011</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.95nm</td>
<td>—</td>
<td>~0.3V (L$_g$=30nm)</td>
<td>100mV/dec</td>
<td>~200mV/V</td>
<td>Intel IEDM2009</td>
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<tr>
<td>W/La-silicate</td>
<td>0.62nm</td>
<td>155cm$^2$/Vs (at 1MV/cm)</td>
<td>-0.08V (L$_g$=10um)</td>
<td>~70mV/dec</td>
<td>—</td>
<td>Tokyo Tech. T-ED2012</td>
</tr>
</tbody>
</table>
Recent results by my group.
ALD of La$_2$O$_3$


ALD is indispensable from the manufacturing viewpoint
- precise control of film thickness and good uniformity
Why high mobility channel materials?
Arming higher performance at lower supply voltage

Both 1) and 2) are important

1) High injection Velocity of carriers
   \[ v_{\text{inj}} \]

2) High mobility of carriers

III-V (n-channel) or Ge (p-channel)

Problems: Technologies and Cost

- Interfacial properties at the gate insulator/semiconductor
- Contact resistance at Source/Drain and semiconductor
- Different semiconductors for n- and p- channel FETs
- Integration on Si wafer
## Ge, III-V bulk properties

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
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<tr>
<td><strong>electron mob.</strong></td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
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<tr>
<td>(cm²/Vs)</td>
<td></td>
<td></td>
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<tr>
<td><strong>electron effective mass (/m₀)</strong></td>
<td>m₁: 0.19</td>
<td>m₁: 0.916</td>
<td>m₁: 0.082</td>
<td>m₁: 1.467</td>
<td>0.067</td>
<td>0.08</td>
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<td>0.026</td>
<td>0.0135</td>
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<tr>
<td><strong>hole mob.</strong></td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
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<tr>
<td>(cm²/Vs)</td>
<td></td>
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<tr>
<td><strong>hole effective mass (/m₀)</strong></td>
<td>m₁: 0.49</td>
<td>m₈: 0.16</td>
<td>m₁: 0.28</td>
<td>m₈: 0.044</td>
<td>m₁: 0.45</td>
<td>m₈: 0.082</td>
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<td></td>
<td></td>
<td>m₁: 0.45</td>
<td>m₈: 0.12</td>
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<tr>
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<td></td>
<td>m₁: 0.57</td>
<td>m₈: 0.35</td>
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<td></td>
<td></td>
<td>m₁: 0.44</td>
<td>m₈: 0.016</td>
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<td><strong>band gap (eV)</strong></td>
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<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.14</td>
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<tr>
<td><strong>permittivity</strong></td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

- Ge \(\Rightarrow\) lightest hole \(m^*\) (light electron \(m^*\)) \(\Rightarrow\) pMOS (CMOS)
- III-V \(\Rightarrow\) light electron \(m^*\) \(\Rightarrow\) nMOS
- GaAs \cdot\) InP \(\Rightarrow\) \(E_g\) higher than that in Si \(\Rightarrow\) low power

S. Takagi., IEDM2011, Short course (Tokyo Uni)
Multi-gate III-V and Si benchmark

**nMOS**
- InGaAs GAA
  - \( L_{ch} = 50 \text{nm}, \) Dielectric: 10nm Al\(_2\)O\(_3\)
  - \( V_{DS} = 0.5V \) (Purdue Uni.) [1]
- InGaAs Tri-gate
  - \( L_g = 60 \text{nm}, \) EOT 12A
  - \( V_{DS} = 0.5V \) (Intel) [2]
- InGaAs FinFET
  - \( L_{ch} = 130 \text{nm}, \) EOT 3.8nm
  - \( V_{DS} = 0.5V \) (NUS)[3]
- InGaAs Nanowire
  - \( L_g = 200 \text{nm}, \) \( T_{ox} = 14.8 \text{nm} \)
  - \( V_{DS} = 0.5V \) (Hokkaido Uni.)[4]
- Metal S/D InGaAs-OI
  - \( L_{ch} = 55 \text{nm}, \) EOT 3.5nm
  - \( V_{DS} = 0.5V \) (Tokyo Uni.)[5]

**pMOS**
- GOI Tri-gate
  - \( L_g = 65 \text{nm}, \) EOT 3.0nm
  - \( V_D = -1V \) (AIST Tsukuba)[6]
- Si-FinFET 22nm
  - \( L_g = 4.5 \text{mm}, \) Dielectric: SiON, \( V_{DS} = -1V \)
  - (Stanford Uni.)[7]
- Si-FinFET 32nm
  - \( L_g = 183 \text{nm}, \) EOT 5.5nm
  - \( V_D = -1V \) (NNDL Taiwan)[9]
- Si-FinFET 22nm
  - \( L_g = 300 \text{nm}, \) dielectric: GeO\(_2\)(7nm)-HfO\(_2\)(10nm)
  - \( V_D = -0.8V \) (ASTAR Singapore)[8]
- Si-bulk 45nm
  - \( L_g = 300 \text{nm}, \) dielectric: GeO\(_2\)(7nm)-HfO\(_2\)(10nm)
  - \( V_D = -0.8V \) (ASTAR Singapore)[8]
- Si-FinFET 22nm
  - \( L_g = 4.5 \text{mm}, \) Dielectric: SiON, \( V_{DS} = -1V \)
  - (Stanford Uni.)[7]
- Si-FinFET 32nm
  - \( L_g = 183 \text{nm}, \) EOT 5.5nm
  - \( V_D = -1V \) (NNDL Taiwan)[9]
- Si-FinFET 22nm
  - \( L_g = 300 \text{nm}, \) dielectric: GeO\(_2\)(7nm)-HfO\(_2\)(10nm)
  - \( V_D = -0.8V \) (ASTAR Singapore)[8]
- Si-bulk 45nm
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  - \( V_D = -0.8V \) (ASTAR Singapore)[8]

---

Optimization of short channel Ge p-MOSFETs is still under investigation.
### III-V/Ge benchmark for various structures

<table>
<thead>
<tr>
<th>Material</th>
<th>Planar (metal S/D, Strain, Buffer...)</th>
<th>FinFET</th>
<th>Tri-gate</th>
<th>Gate-all-around MOSFET</th>
<th>Nanowire</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>InGaAs</td>
<td>Ge</td>
<td>InGaSn</td>
<td>InGaAs</td>
<td>Ge</td>
</tr>
<tr>
<td>Dielectric/EOT</td>
<td>Al₂O₃/3.5 nm</td>
<td>7.6 Å²</td>
<td>Al₂O₃</td>
<td>5nm ALD</td>
<td>5nm ALD</td>
</tr>
<tr>
<td>Mobility</td>
<td>~600 (cm²/Vs)</td>
<td>-</td>
<td>~700 (µS/µm)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Lch (nm)</td>
<td>55</td>
<td>W/L=30/5 µm</td>
<td>50 µm</td>
<td>100</td>
<td>4.5 µm</td>
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<tr>
<td>DIBL (mV/V)</td>
<td>150K</td>
<td>61pMOS</td>
<td>120K</td>
<td>145</td>
<td>750</td>
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<td>SS (mV/dec)</td>
<td>105</td>
<td>-</td>
<td>4 (n,p)</td>
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<td>4</td>
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<tr>
<td>Ion (µA/µm)</td>
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<td>(V_d=0.5V)</td>
<td>3</td>
<td>(V_d=0.2V)</td>
<td>-</td>
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</table>
## ITRS 2011 for Si (HP: High Performance Logic)

*1: Thicker EOT for MG (Multiple gate: Fin/Tri gate, nanowire)

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2012</th>
<th>2014</th>
<th>2016</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
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<tbody>
<tr>
<td>$L_g$ (nm)</td>
<td>22</td>
<td>18</td>
<td>15.3</td>
<td>12.8</td>
<td>10.6</td>
<td>8.9</td>
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<td>$V_{dd}$ (V)</td>
<td>0.87</td>
<td>0.82</td>
<td>0.77</td>
<td>0.73</td>
<td>0.68</td>
<td>0.64</td>
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<td>0.57</td>
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<td>0.54</td>
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<td>*1: MG</td>
<td>0.76</td>
<td>0.68</td>
<td>0.62</td>
<td>0.56</td>
<td>0.50</td>
<td>0.45</td>
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<tr>
<td>Mobility enhancement factor due to strain</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
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<td>1.8</td>
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<tr>
<td>$C_g$ Ideal (fF/µm)</td>
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<td>Bulk</td>
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<td>0.576</td>
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<td>$V_{t,sat}$ (mV)</td>
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<tr>
<td>MG</td>
<td>217</td>
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<td>225</td>
<td>228</td>
<td>231</td>
<td>237</td>
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<td>$CV/I$ (ps)</td>
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<td>0.30</td>
<td>0.24</td>
<td>0.20</td>
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<td>MG</td>
<td>0.29</td>
<td>0.24</td>
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<td>0.16</td>
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<td>0.10</td>
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Manufacturing solutions exist or is being optimized
Manufacturing solutions are known
Manufacturing solutions are **NOT** known
### ITRS 2011 for Si (HP), contd

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<th>2024</th>
<th>2026</th>
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<tbody>
<tr>
<td>$L_g$ (nm)</td>
<td>22</td>
<td>18</td>
<td>15.3</td>
<td>12.8</td>
<td>10.6</td>
<td>8.9</td>
<td>7.4</td>
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<tr>
<td><strong>Equivalent Injection velocity $V_{inj} (10^7 \text{ cm/s})$</strong></td>
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<td>$I_{d,\text{sat}}$ (mA/$\mu$m)</td>
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<td>1.670</td>
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<td>100</td>
<td>100</td>
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<td>100</td>
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<td>133</td>
<td>104</td>
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<td>$CV^2$ (fJ/$\mu$m)</td>
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<tr>
<td>Bulk</td>
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<td>0.57</td>
<td>0.49</td>
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<td>0.31</td>
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<td>0.21</td>
<td>0.17</td>
<td>0.14</td>
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Manufacturing solutions exist or are being optimized

Manufacturing solutions are known

Manufacturing solutions are **NOT** known
# ITRS 2011 for III-V/Ge

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
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<td>11.7</td>
<td>9.3</td>
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<tr>
<td>$V_{dd}$ (V)</td>
<td>0.63</td>
<td>0.61</td>
<td>0.58</td>
<td>0.56</td>
<td>0.54</td>
</tr>
<tr>
<td>$EOT$ (nm)</td>
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<td>0.62</td>
<td>0.56</td>
<td>0.50</td>
<td>0.45</td>
</tr>
<tr>
<td>Mobility enhancement factor due to channel material</td>
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<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>III-V</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Ge</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>$C_g$ Ideal (fF/µm)</td>
<td></td>
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</tr>
<tr>
<td>III-V</td>
<td>0.28</td>
<td>0.24</td>
<td>0.20</td>
<td>0.16</td>
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<tr>
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<td>0.30</td>
<td>0.25</td>
<td>0.21</td>
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<tr>
<td>$V_{t, sat}$ (mV)</td>
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<td>III-V</td>
<td>229</td>
<td>230</td>
<td>238</td>
<td>245</td>
<td>251</td>
</tr>
<tr>
<td>Ge</td>
<td>230</td>
<td>231</td>
<td>241</td>
<td>249</td>
<td>254</td>
</tr>
<tr>
<td>$CV/I$ (ps)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>III-V</td>
<td>0.13</td>
<td>0.11</td>
<td>0.09</td>
<td>0.07</td>
<td>0.06</td>
</tr>
<tr>
<td>Ge</td>
<td>0.21</td>
<td>0.17</td>
<td>0.13</td>
<td>0.10</td>
<td>0.08</td>
</tr>
</tbody>
</table>

Manufacturing solutions are **NOT** known.
## ITRS 2011 for III-V/Ge, Contd

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$ (nm)</td>
<td>14</td>
<td>11.7</td>
<td>9.3</td>
<td>7.4</td>
<td>5.8</td>
</tr>
<tr>
<td>Equivalent Injection velocity $V_{ini}$ ($10^7$ cm/s)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>III-V</td>
<td>4.29</td>
<td>4.58</td>
<td>5.32</td>
<td>5.93</td>
<td>6.64</td>
</tr>
<tr>
<td>Ge</td>
<td>2.26</td>
<td>2.44</td>
<td>2.86</td>
<td>3.19</td>
<td>3.63</td>
</tr>
<tr>
<td>$I_{d,sat}$ (mA/µm)</td>
<td>2.200</td>
<td>2.343</td>
<td>2.523</td>
<td>2.703</td>
<td>2.884</td>
</tr>
<tr>
<td>III-V</td>
<td>1.769</td>
<td>1.932</td>
<td>2.121</td>
<td>2.330</td>
<td>2.555</td>
</tr>
<tr>
<td>Ge</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{sd,leak}$ (nA/µm)</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>$R_{sd}$ ($\mu$m)</td>
<td>131</td>
<td>113</td>
<td>96</td>
<td>82</td>
<td>70</td>
</tr>
<tr>
<td>III-V</td>
<td>149</td>
<td>126</td>
<td>105</td>
<td>85</td>
<td>72</td>
</tr>
<tr>
<td>Ge</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$CV^2$ (fJ/µm)</td>
<td>0.18</td>
<td>0.15</td>
<td>0.13</td>
<td>0.11</td>
<td>0.09</td>
</tr>
<tr>
<td>III-V</td>
<td>0.23</td>
<td>0.20</td>
<td>0.16</td>
<td>0.14</td>
<td>0.11</td>
</tr>
<tr>
<td>Ge</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Manufacturing solutions are *NOT* known.
TFET vs. MOSFET at low $V_{\text{DD}}$

$V_{\text{DD}}$ 0.3~0.35V
TFET 8x faster at the same power
“parameter variation is not a significant factor for differentiation between MOSFET and TFET”
Tunnel FET (Si)

X in Si$_{1-x}$Ge$_x$ is optimized to allow for efficient BTBT

$L_G = 200$nm

$I_{ON}/I_{OFF} \approx 10^5$

Reducing SiGe

Body thickness improves Subthreshold swing.

130mV/dec

190mV/dec

A. Villalon, pp.49, VLSI 2012 (CEA-LETI)
SS of TFET is function of $V_G$ due to Zener tunnel current

Minimum SS = 21 mV/dec is reached due to optimized series resistance of contact, undoped InAs and InAs/Si

$I_{ON}/I_{OFF} \sim 10^6$ at $V_{DS} = 1.0V$ ($I_{ON} = 1A_{\mu}/\mu m$)
**Device structure**

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

- **tunneling // to the gate**
  - oblique to the gate field

- **tunneling ⊥ to the gate**
  - in-line with the gate field

- **nanowire TFET**
  - gate-all-around - best electrostatics

---

**References**

- K. Tomioka et al., pp.47, VLSI2012 (Hokkaido University)
## Tunnel FET performance comparison

**A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)**

Measured III-V channel TFETs

<table>
<thead>
<tr>
<th>Reference</th>
<th>Source</th>
<th>Channel</th>
<th>Dielectric</th>
<th>EOT (nm)</th>
<th>$I_{ON}$ (µA/µm)</th>
<th>$V_{DS}$ (V)</th>
<th>$V_{GS}=V_{ON}$</th>
<th>$V_{ON}-V_{OFF}$</th>
<th>$I_{ON}/I_{OFF}$</th>
<th>$S_{MIN}$ (mV/dec)</th>
<th>$S_{EFF}$ (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>this work</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.6</td>
<td>78</td>
<td>0.5</td>
<td>0.5</td>
<td>1.5</td>
<td>2,000</td>
<td>125</td>
<td>230</td>
</tr>
<tr>
<td>Li [4]</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$</td>
<td>3.9</td>
<td>20</td>
<td>0.3</td>
<td>2</td>
<td>6</td>
<td>210</td>
<td>830</td>
<td>1300</td>
</tr>
<tr>
<td>Mookerjea [5]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>5.6</td>
<td>10</td>
<td>0.5</td>
<td>2.5</td>
<td>2.5</td>
<td>10,000</td>
<td>240</td>
<td>310</td>
</tr>
<tr>
<td>Mohata [6]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
<td>2.8</td>
<td>10</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>400,000</td>
<td>200</td>
<td>180</td>
</tr>
<tr>
<td>Zhao [7]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>20</td>
<td>0.45</td>
<td>1</td>
<td>1.5</td>
<td>30,000</td>
<td>86</td>
<td>170</td>
</tr>
<tr>
<td>Zhao [8]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
<td>1.2</td>
<td>40</td>
<td>0.5</td>
<td>2</td>
<td>2</td>
<td>200,000</td>
<td>84</td>
<td>190</td>
</tr>
<tr>
<td>Ford [9]</td>
<td>InAs</td>
<td>InAs</td>
<td>ZrO$_2$</td>
<td>2</td>
<td>0.4</td>
<td>0.5</td>
<td>1</td>
<td>1</td>
<td>200</td>
<td>190</td>
<td>220</td>
</tr>
<tr>
<td>Zhou [10]</td>
<td>InP</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.3</td>
<td>20</td>
<td>0.5</td>
<td>1</td>
<td>1.75</td>
<td>450,000</td>
<td>93</td>
<td>150</td>
</tr>
</tbody>
</table>

- **$S_{MIN}$**: Most common SS which is the inverse of $I_D$-$V_{GS}$ slope at the steepest part
- **$S_{EFF}$**: Is the average swing when $V_{TH}=V_{DD}/2$, $V_{OFF}=0$

\[
V_{TH} - V_{OFF} = \frac{V_{DD}}{2} \frac{\log(I_D/I_{OFF})}{2\log(I_D/I_{OFF})}
\]

\[
V_{OFF}=0 \quad V_{TH}=V_{DD}/2
\]

**Effective SS:**

\[
V_{DD} \frac{\log(I_D/I_{OFF})}{2\log(I_D/I_{OFF})}
\]
$I_{ON}$ and $I_{OFF}$ of TFETs

[1] G. Zhou et al., pp. 782, vol. 33, no. 6, EDL 2012 (University of Notre Dame)

C. Auth et al., pp.131, VLSI 2012 (Intel).

K. Mistry et al., pp.247, IEDM 2007 (Intel).
Mechanical Switch: MEMS relay

- Frequency of 1, 5, 25 kHz under operation
- $\frac{I_{ON}}{I_{OFF}}$ of $\approx 10^{10}$

Ultra-low-power digital logic applications.
Metal (Silicide) S/D
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- \( V_t \) and \( I_{ON} \) variation
- GIDL

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
**Surface or interface control**

**Diffusion species:** *metal atom* (Ni, Co)
- Rough interface at silicide/Si
  - Excess silicide formation
  - Different $\phi_B$ presented at interface
  - Process temperature dependent composition

**Diffusion species:** *Si atom* (Ti)
- Surface roughness increases
  - Line dependent resistivity change

Annealing: 650 °C
Si(001) sub. Epitaxial NiSi$_2$


CoSi$_2$  NiSi  TiSi$_2$

Top view
Line width of 0.1 µm
Aglomeration

Deposition of Ni-Si mixed films from NiSi$_2$ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
SEM views of silicide/Si interfaces

Ni source (50nm)

- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

NiSi$_2$ source (50nm)

- Atomically flat interfaces
- No Si consumption
- Temperature-independent

Ni source

NiSi$_2$ source
Ideal characteristics ($n = 1.00$, suppressed leakage current)

- Flat interface and No Si substrate consumption
- No defects in Si substrate

Suppressed reverse leakage current

<table>
<thead>
<tr>
<th>Source</th>
<th>$\phi_Bn$ (eV)</th>
<th>$n$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>0.676</td>
<td>1.08</td>
</tr>
<tr>
<td>NiSi$_2$</td>
<td>0.659</td>
<td>1.00</td>
</tr>
</tbody>
</table>

Schottky diode structures

RTA: 500°C, 1 min
(a) Si Fin  Ni silicide  Ni  Growth length  200nm

(b) SiO₂  Ni silicide  Si NW  Growth length  200nm

Si Fin  Ni silicide  50nm  Fins width 20nm

SiO₂  Ni silicide  50nm  NWs width 20nm
Conclusions

Si-MOSFET is the most fundamental and smallest functional device available for manufacturing.

It is really amazing to keep the evolution for so many generations without being replaced by any other device.
The device downsizing of Si-MOSFET will be ended within 10 ~ 20 years because $I_{\text{off}}$ increase at the size of sub-5nm.

In order to reach the limit, R&D for nanowire, high-k for sub-5nm EOT, silicide S/D are necessary.

There are many rooms for the universities to contribute to the development.
Finally, even after the end of Si-MOSFET downsizing, Si-CMOS technology will still be the mainstream IC technology for a long period, as no other device technology seems to be developed into a comparable integration scale as the present CMOS technology in foreseeable future.

However, new device research other than Si-CMOS is also very important.
Difference of history

Bio device (brain, even insect): 4 Billion Years from single cell.

MOS IC: only 40 Years
Thank you for your attention!
High-k beyond 0.5 nm
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k

Metal

High-k

SiO₂-IL

Si-sub.

Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k

Suppression of gate leakage current

Endurance for high temperature process

Reliability: PBTI, NBTI, TDDB

Workfunction engineering for $V_{th}$ control

Suppression of FLP

Interface dipole control for $V_{th}$ tuning

Remove contamination introduced by CVD

Thinning or removal of SiO₂-IL for small EOT

160
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band offset

Oxide

Si

Band Discontinuity [eV]

Dielectric Constant $\varepsilon(0)$

XPS measurement by Prof. T. Hattori, INFOS 2003
## Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Elements</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si + MO\text{X} M + SiO\text{2}</td>
<td>Unstable at Si interface</td>
</tr>
<tr>
<td>Si + MO\text{X} MSi\text{X} + SiO\text{2}</td>
<td></td>
</tr>
<tr>
<td>Si + MO\text{X} M + MSi\text{X}O\text{Y}</td>
<td></td>
</tr>
<tr>
<td>Gas or liquid at 1000 K</td>
<td></td>
</tr>
<tr>
<td>Radio active He</td>
<td></td>
</tr>
<tr>
<td>B C N O F Ne</td>
<td></td>
</tr>
<tr>
<td>Al Si P S Cl Ar</td>
<td></td>
</tr>
<tr>
<td>Hf</td>
<td></td>
</tr>
<tr>
<td>La</td>
<td></td>
</tr>
<tr>
<td>Ce Pr Nd Sm Eu Gd Tb Dy Ho Er Tm Yb Lu</td>
<td></td>
</tr>
</tbody>
</table>

HfO\text{2} based dielectrics are selected as the first generation materials, because of their merit in 1) band-offset, 2) dielectric constant, 3) thermal stability.

La\text{2}O\text{3} based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

R. Hauser, IEDM Short Course, 1999
Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface. Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ ⇆ HfO$_2$ + Si + 2O* ⇆ HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 613

SiO$_x$-IL is formed after annealing

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Trans. ECS 11, 319

Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

XPS Si1s spectra

TEM image 500 °C, 30 min

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$Si$_6$O$_{30}$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
For the past 45 years, SiO2 and SiON have been used for gate insulator. Today, EOT=1.0nm.

EOT Limit: 0.7~0.8 nm

One order of Magnitude

EOT can be reduced further beyond 0.5 nm by using direct contact to Si.

By choosing appropriate materials and processes.

Introduction of High-k:
Still SiO2 or SiON is used at Si interface.

Direct Contact:
Of high-k and Si
High-k/metal gate stack film deposition cluster tool
La$_2$O$_3$ at 300° C process make sub-0.4 nm EOT MOSFET

**EOT=0.37nm**

- EOT=0.37nm
- EOT=0.40nm
- EOT=0.48nm

\[0.48 \rightarrow 0.37\text{nm Increase of } I_d \text{ at 30\%}\]
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small Dit

- silicate-reaction-formed fresh interface
- stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress

No interfacial layer can be confirmed with Si/TiN/W

La₂O₃
Gate leakage is two orders of magnitude lower than that of ITRS.

Electron mobility is comparable to record mobility with Hf-based oxides.
## Si benchmark (nMOSFET)

<table>
<thead>
<tr>
<th>Gate stack</th>
<th>EOT</th>
<th>Mobility</th>
<th>$V_{th}$</th>
<th>SS</th>
<th>DIBL</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.52nm</td>
<td>110cm$^2$/Vs (at 1x10$^{13}$cm$^{-2}$)</td>
<td>~0.4V (L$_g$=24nm)</td>
<td>90mV/dec</td>
<td>147mV/V</td>
<td>IBM VLSI2011</td>
</tr>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.55nm</td>
<td>140cm$^2$/Vs (at 1MV/cm)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IBM VLSI2009</td>
</tr>
<tr>
<td>Metal(A)/Cap/HfO$_2$</td>
<td>0.5nm</td>
<td>110cm$^2$/Vs (at 0.8MV/cm)</td>
<td>0.3V (L$_g$=1um)</td>
<td>—</td>
<td>—</td>
<td>IMEC IEDM2009</td>
</tr>
<tr>
<td>Metal/HfO$_2$</td>
<td>0.59nm</td>
<td>130cm$^2$/Vs (at 1MV/cm)</td>
<td>0.45V (L$_g$=1um)</td>
<td>75mV/dec</td>
<td>—</td>
<td>Sematech VLSI2009</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.65nm</td>
<td>—</td>
<td>0.3~0.4V (L$_g$=~30nm)</td>
<td>90mV/dec</td>
<td>100mV/V</td>
<td>Samsung VLSI2011</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.95nm</td>
<td>—</td>
<td>~0.3V (L$_g$=30nm)</td>
<td>100mV/dec</td>
<td>~200mV/V</td>
<td>Intel IEDM2009</td>
</tr>
<tr>
<td>W/La-silicate</td>
<td>0.62nm</td>
<td>155cm$^2$/Vs (at 1MV/cm)</td>
<td>-0.08V (L$_g$=10um)</td>
<td>~70mV/dec</td>
<td>—</td>
<td>Tokyo Tech. T-ED2012</td>
</tr>
</tbody>
</table>
Recent results by my group.
ALD is indispensable from the manufacturing viewpoint
- precise control of film thickness and good uniformity

How far can we go for production?

<table>
<thead>
<tr>
<th>Past</th>
<th>0.7 times per 3 years</th>
<th>In 40 years: 18 generations, Size 1/300, Area 1/100,000</th>
</tr>
</thead>
<tbody>
<tr>
<td>1970年</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm → 0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Now</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 3 nm?</td>
<td></td>
</tr>
</tbody>
</table>

• At least 4,5 generations to 8 ~ 5 nm
The down scaling of MOSFETs is still possible for at least another 10 years!

4 important technological items for down scaling.

New structures
1. Wire channel

New materials
1. Thinning of high-k gate oxide thickness beyond 0.5 nm
2. Metal(Silicide) S/D
3. III-V/Ge channel
These technologies are very difficult and not every company can succeed in the development timely.

In the past, technology comes with the purchase of equipment, but any more.

Thus, some of the companies are in the threat of dropping off.

There are so many rooms for the universities to contribute to the development of Si world.
Wire channel
Suppression of subthreshold leakage by surrounding gate structure

Planar

Surrounding gate
Because of off-leakage control, 

Planar $\rightarrow$ Fin $\rightarrow$ Nanowire
Nanowire structures in a wide meaning

- Fin
- Tri-gate
- Ω-gate
- All-around
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process

2. Good controllability of $I_{OFF}$

3. High drive current

**1D ballistic conduction**

**Multi quantum Channel**

**High integration of wires**
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Compact modeling of nanowire MOSFETs is very difficult
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Wire cross section dependence.
What cross section gives best solution for SCE suppression and drive current?
Compact model for circuit designer is very important

$\lambda > L$  Diffusive transport

$\lambda \sim L$  Quasi-Ballistic transport

$\lambda < L$  Ballistic transport

Prof. K. Natori of TIT
Prof. K. Natori of TIT
チャネル内の電子散乱導入の考え方

透過確率

\[ T(\varepsilon) = \frac{(F(0) - G(0))}{F(0)} \]

ドレインからの入射=0

\[ I_D = \frac{q}{\pi \hbar} \sum_i \int [f(E, \mu_S) - f(E, \mu_D)] T_i(E) dE \]

Prof. K. Natori of TIT
散乱の導入に係る計算式

弾性散乱域

\[
\sqrt{\frac{2}{m}} \left( qEx + \varepsilon \right) \frac{dF(x)}{dx} + \frac{B_0}{\sqrt{qEx + \varepsilon}} \left\{ F(x) - G(x) \right\} = 0
\]

\[
-\sqrt{\frac{2}{m}} \left( qEx + \varepsilon \right) \frac{dG(x)}{dx} + \frac{B_0}{\sqrt{qEx + \varepsilon}} \left\{ G(x) - F(x) \right\} = 0
\]

光学フォノン放出域

\[
\sqrt{\frac{2}{m}} \left( qEx + \varepsilon \right) \frac{dF(x)}{dx} + \frac{B_0}{\sqrt{qEx + \varepsilon}} \left\{ F(x) - G(x) \right\} + \frac{2D_0}{\sqrt{qEx + \varepsilon - \varepsilon^*}} F(x) = 0
\]

\[
-\sqrt{\frac{2}{m}} \left( qEx + \varepsilon \right) \frac{dG(x)}{dx} + \frac{B_0}{\sqrt{qEx + \varepsilon}} \left\{ G(x) - F(x) \right\} + \frac{2D_0}{\sqrt{qEx + \varepsilon - \varepsilon^*}} G(x) = 0
\]

ソースからドレインへの透過確率（エネルギー \( \varepsilon \) に対して）

\[
T(\varepsilon) = \frac{\sqrt{2D_0 qE}}{\left( \sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0 B_0} \ln \left( \frac{qEx_0 + \varepsilon}{\varepsilon} \right)}
\]
Prof. K. Natori of TIT
Experiment
Quasi ballistic
$V_g - V_{th} = 1V$

$V_d (V)$

$I_d (A)$
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off > 10^6, 60uA/wire

Lg = 65nm, Tōx = 3nm
Bench Mark

V_{DD}: 1.0~1.5 V

Gate Length (nm) vs. \( I_{ON} \) (\( \mu A \)/wire)

- nMOS
- pMOS

Our Work
\[ \frac{I_{ON}}{I_{OFF}} \text{ Bench mark} \]

![Graph showing \(I_{OFF}\) versus \(I_{ON}\) for Planar FET and Si nanowire FET.]

**Planar FET**
- S. Kamiyama, IEDM 2009, p. 431
- P. Packan, IEDM 2009, p.659

**Si nanowire FET**
- Y. Jiang, VLSI 2008, p.34
- H.-S. Wong, VLSI 2009, p.92
- S. Bangsaruntip, IEDM 2009, p.297
- C. Dupre, IEDM 2008, p. 749
- S.D. Suk, IEDM 2005, p.735
- G. Bidel, VLSI 2009, p.240

**Values**
- Planar FET: 1.0〜1.1V
- Si nanowire FET: 1.2〜1.3V

**Symbols**
- \(L_g = 500\sim 65\text{nm}\)
- This work

**Notes**
- Si nanowire FET: \(1.2\sim 1.3\text{V}\)
Effective Electron Mobility (cm²/Vs) vs Inversion Carrier Density (cm⁻²)

- A₁ (12x19) \( h_{NW} \times w_{NW} \) (nm²)
- A₂ (12x28)
- B (20x10)

SOI Planar \( T_{SOI} = 28 \text{ nm} \)

Dimensions:
- A₁: \( h_{NW} = 12 \text{ nm}, w_{NW} = 19 \text{ nm} \)
- B: \( h_{NW} = 20 \text{ nm}, w_{NW} = 10 \text{ nm} \)

SOI planar with BOX
The diagram illustrates the electron density distribution in a SiNW structure, comparing the edge portion with the flat portion.

(a) The image shows a cross-section of the SiNW with a metal contact on top. The electron density is color-coded, with the color bar indicating the density range from 16 to 20 (x10^19 cm^-3).

(b) The inset indicates the inversion areal ratio, which is 44% for the edge portion and 29% for the flat portion.

The graph on the right side of the image plots electron density (x10^19 cm^-3) against the distance from the SiNW surface (nm). The blue solid line represents the edge portion, while the red dashed line shows the flat portion.
Pr trials estimation!

$I_{ON} = \frac{\mu A}{\mu m}$

- Small EOT for high-k (33)
- P-MOS improvement (26)
- Low S/D resistance (20)
- $L_g^{-0.5} \cdot T_{ox}^{-1}$

Compact model

SiNW (12nm & 19nm)

Assumption

$# \text{ of wires } / 1 \mu m$

Bulk, FD, ITRS, MG

Year
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-$k$ is necessary.
III-V/Ge channel
Why high mobility channel materials?

Arming higher performance at lower supply voltage

Both 1) and 2) are important

1) High injection Velocity of carriers

2) High mobility of carriers

Problems: Technologies and Cost

Interfacial properties at the gate insulator/semiconductor

Contact resistance at Source/Drain and semiconductor

Different semiconductors for n- and p-channel FETs

Integration on Si wafer
# High mobility channel materials


<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>electron mob. (cm²/Vs)</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
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<tr>
<td>electron effective mass (/m₀)</td>
<td>mₑ: 0.19  mᵢ: 0.916</td>
<td>mₑ: 0.082 mᵢ: 1.467</td>
<td>0.067</td>
<td>0.082</td>
<td>0.023</td>
<td>0.014</td>
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<tr>
<td>hole mob. (cm²/Vs)</td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td>hole effective mass (/m₀)</td>
<td>m₉H: 0.49  m₈: 0.16</td>
<td>m₉H: 0.28  m₈: 0.044</td>
<td>m₉H: 0.45  m₈: 0.082</td>
<td>m₉H: 0.45  m₈: 0.12</td>
<td>m₉H: 0.57  m₈: 0.35</td>
<td>m₉H: 0.44  m₈: 0.016</td>
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<tr>
<td>band gap (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.17</td>
</tr>
<tr>
<td>permittivity</td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

Better carrier transport

Higher drive current at low power supply
## ITRS 2011 for Si (HP: High Performance Logic)

*1: Thicker EOT for MG (Multiple gate: Fin/Tri gate, nanowire)

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2012</th>
<th>2014</th>
<th>2016</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_g ) (nm)</td>
<td>22</td>
<td>18</td>
<td>15.3</td>
<td>12.8</td>
<td>10.6</td>
<td>8.9</td>
<td>7.4</td>
<td>5.9</td>
</tr>
<tr>
<td>( V_{dd} ) (V)</td>
<td>0.87</td>
<td>0.82</td>
<td>0.77</td>
<td>0.73</td>
<td>0.68</td>
<td>0.64</td>
<td>0.61</td>
<td>0.57</td>
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<tr>
<td>( EOT ) (nm)</td>
<td>( \text{Bulk} )</td>
<td>0.84</td>
<td>0.73</td>
<td>0.61</td>
<td>( \text{FD SOI} )</td>
<td>0.8</td>
<td>0.72</td>
<td>0.63</td>
</tr>
<tr>
<td>Mobility enhancement factor due to strain</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
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<tr>
<td>( C_g \text{ Ideal} ) (fF/( \mu )m)</td>
<td>( \text{Bulk} )</td>
<td>0.658</td>
<td>0.611</td>
<td>0.576</td>
<td>( \text{FD SOI} )</td>
<td>0.529</td>
<td>0.429</td>
<td>0.393</td>
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<tr>
<td>( V_{t,sat} ) (mV)</td>
<td>( \text{Bulk} )</td>
<td>289</td>
<td>302</td>
<td>310</td>
<td>( \text{FD SOI} )</td>
<td>222</td>
<td>227</td>
<td>234</td>
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<tr>
<td>( CV/I ) (ps)</td>
<td>( \text{NMOS} )</td>
<td>( \text{Bulk} )</td>
<td>0.57</td>
<td>0.47</td>
<td>0.38</td>
<td>( \text{FD SOI} )</td>
<td>0.38</td>
<td>0.30</td>
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</table>

<table>
<thead>
<tr>
<th>Manufacturing solutions exist or is being optimized</th>
<th>Manufacturing solutions are known</th>
<th>Manufacturing solutions are NOT known</th>
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</thead>
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<tr>
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<td>⬤</td>
<td>⬤</td>
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### ITRS 2011 for Si (HP), contd

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<th>Year of Production</th>
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<th>2022</th>
<th>2024</th>
<th>2026</th>
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</thead>
<tbody>
<tr>
<td>$L_g$ (nm)</td>
<td>22</td>
<td>18</td>
<td>15.3</td>
<td>12.8</td>
<td>10.6</td>
<td>8.9</td>
<td>7.4</td>
<td>5.9</td>
</tr>
</tbody>
</table>

#### Equivalent Injection velocity $V_{inj}$ ($10^7$ cm/s)

<table>
<thead>
<tr>
<th></th>
<th>Bulk</th>
<th>FD SOI</th>
<th>MG</th>
</tr>
</thead>
<tbody>
<tr>
<td>2014</td>
<td>1.09</td>
<td>1.37</td>
<td>1.68</td>
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<tr>
<td>2016</td>
<td>1.18</td>
<td>1.51</td>
<td>1.82</td>
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<tr>
<td>2018</td>
<td>1.33</td>
<td>1.63</td>
<td>2.05</td>
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<tr>
<td>2020</td>
<td>1.83</td>
<td>2.26</td>
<td>2.67</td>
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</table>

#### $I_{d,sat}$ (mA/µm)

<table>
<thead>
<tr>
<th></th>
<th>Bulk</th>
<th>FD SOI</th>
<th>MG</th>
</tr>
</thead>
<tbody>
<tr>
<td>2014</td>
<td>1.367</td>
<td>1.530</td>
<td>1.685</td>
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<tr>
<td>2016</td>
<td>1.496</td>
<td>1.654</td>
<td>1.805</td>
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<td>2018</td>
<td>1.670</td>
<td>1.791</td>
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<td>2020</td>
<td>1.942</td>
<td>2.030</td>
<td>2.308</td>
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#### $I_{sd,leak}$ (nA/µm)

<table>
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<tr>
<th></th>
<th>100</th>
<th>100</th>
<th>100</th>
<th>100</th>
<th>100</th>
<th>100</th>
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<th>100</th>
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</thead>
</table>

#### $R_{sd}$ (Ω·µm)

<table>
<thead>
<tr>
<th></th>
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<th>FD SOI</th>
<th>MG</th>
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</thead>
<tbody>
<tr>
<td>2014</td>
<td>232</td>
<td>274</td>
<td>257</td>
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<tr>
<td>2016</td>
<td>183</td>
<td>228</td>
<td>218</td>
</tr>
<tr>
<td>2018</td>
<td>149</td>
<td>187</td>
<td>186</td>
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<tr>
<td>2020</td>
<td>133</td>
<td>160</td>
<td>160</td>
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</table>

#### $CV^2$ (fJ/µm)

<table>
<thead>
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<th></th>
<th>Bulk</th>
<th>FD SOI</th>
<th>MG</th>
</tr>
</thead>
<tbody>
<tr>
<td>2014</td>
<td>0.68</td>
<td>0.47</td>
<td>0.38</td>
</tr>
<tr>
<td>2016</td>
<td>0.57</td>
<td>0.38</td>
<td>0.31</td>
</tr>
<tr>
<td>2018</td>
<td>0.49</td>
<td>0.32</td>
<td>0.25</td>
</tr>
<tr>
<td>2020</td>
<td>0.26</td>
<td>0.21</td>
<td>0.17</td>
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</table>

Manufacturing solutions exist or are being optimized

Manufacturing solutions are known

Manufacturing solutions are *NOT* known
### ITRS 2011 for III-V/Ge

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g \text{ (nm)}$</td>
<td>14</td>
<td>11.7</td>
<td>9.3</td>
<td>7.4</td>
<td>5.8</td>
</tr>
<tr>
<td>$V_{dd} \text{ (V)}$</td>
<td>0.63</td>
<td>0.61</td>
<td>0.58</td>
<td>0.56</td>
<td>0.54</td>
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<tr>
<td>$EOT \text{ (nm)}$</td>
<td>0.68</td>
<td>0.62</td>
<td>0.56</td>
<td>0.50</td>
<td>0.45</td>
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<tr>
<td>Mobility enhancement factor due to channel material</td>
<td>III-V</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
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<tr>
<td></td>
<td>Ge</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
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<tr>
<td>$C_g \text{ Ideal (fF/µm)}$</td>
<td>III-V</td>
<td>0.28</td>
<td>0.24</td>
<td>0.20</td>
<td>0.16</td>
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<tr>
<td></td>
<td>Ge</td>
<td>0.41</td>
<td>0.36</td>
<td>0.30</td>
<td>0.25</td>
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<tr>
<td>$V_{t,sat} \text{ (mV)}$</td>
<td>III-V</td>
<td>229</td>
<td>230</td>
<td>238</td>
<td>245</td>
</tr>
<tr>
<td></td>
<td>Ge</td>
<td>230</td>
<td>231</td>
<td>241</td>
<td>249</td>
</tr>
<tr>
<td>$CV/I \text{ (ps)}$</td>
<td>III-V</td>
<td>0.13</td>
<td>0.11</td>
<td>0.09</td>
<td>0.07</td>
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<tr>
<td></td>
<td>Ge</td>
<td>0.21</td>
<td>0.17</td>
<td>0.13</td>
<td>0.10</td>
</tr>
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</table>

Manufacturing solutions are **NOT** known.
### ITRS 2011 for III-V/Ge, Contd

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_g ) (nm)</td>
<td>14</td>
<td>11.7</td>
<td>9.3</td>
<td>7.4</td>
<td>5.8</td>
</tr>
<tr>
<td>( \text{Vinj} ) ( (10^7 \text{ cm/s}) )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{III-V} )</td>
<td>4.29</td>
<td>4.58</td>
<td>5.32</td>
<td>5.93</td>
<td>6.64</td>
</tr>
<tr>
<td>( \text{Ge} )</td>
<td>2.26</td>
<td>2.44</td>
<td>2.86</td>
<td>3.19</td>
<td>3.63</td>
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<tr>
<td>( \text{I}_{d,\text{sat}} ) ( (\text{mA/\mu m}) )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{III-V} )</td>
<td>2.200</td>
<td>2.343</td>
<td>2.523</td>
<td>2.703</td>
<td>2.884</td>
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<tr>
<td>( \text{Ge} )</td>
<td>1.769</td>
<td>1.932</td>
<td>2.121</td>
<td>2.330</td>
<td>2.555</td>
</tr>
<tr>
<td>( \text{I}_{sd,\text{leak}} ) ( (\text{nA/\mu m}) )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{III-V} )</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>( \text{Ge} )</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>( R_{sd} ) ( (\varnothing - \mu m) )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>( \text{III-V} )</td>
<td>131</td>
<td>113</td>
<td>96</td>
<td>82</td>
<td>70</td>
</tr>
<tr>
<td>( \text{Ge} )</td>
<td>149</td>
<td>126</td>
<td>105</td>
<td>85</td>
<td>72</td>
</tr>
<tr>
<td>( CV^2 ) ( (\text{fJ/\mu m}) )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{III-V} )</td>
<td>0.18</td>
<td>0.15</td>
<td>0.13</td>
<td>0.11</td>
<td>0.09</td>
</tr>
<tr>
<td>( \text{Ge} )</td>
<td>0.23</td>
<td>0.20</td>
<td>0.16</td>
<td>0.14</td>
<td>0.11</td>
</tr>
</tbody>
</table>

Manufacturing solutions are **NOT** known.
Metal (Silicide) S/D
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- $V_t$ and $I_{ON}$ variation
- GIDL

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
**Surface or interface control**

**Diffusion species:**
- **metal atom** (Ni, Co)

  Rough interface at silicide/Si
  - Excess silicide formation
  - Different $\phi_B$ presented at interface
  - Process temperature dependent composition

**Diffusion species:** **Si atom** (Ti)

  Surface roughness increases
  - Line dependent resistivity change

---

Annealing: 650 °C

Si(001) sub. Epitaxial NiSi$_2$


CoSi$_2$ NiSi TiSi$_2$

Top view

Line width of 0.1 µm

Aglomeration

Deposition of Ni film

- Si substrate
- Deposition of Ni film
- Annealing
- Ni-silicide
- Si substrate
- Rough interface

Deposition from NiSi₂ source

- Si substrate
- Deposition from NiSi₂ source
- Annealing
- Ni-silicide
- Si substrate
- Flat interface
- No consumption of Si substrate

Deposition of Ni-Si mixed films from NiSi₂ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
SEM views of silicide/Si interfaces

Ni source (50nm) + NiSi₂ source (50nm)

- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

Ni source

- Atomically flat interfaces
- No Si consumption
- Temperature-independent

NiSi₂ source
**Ideal characteristics** ($n = 1.00$, suppressed leakage current)

- Flat interface and No Si substrate consumption
- No defects in Si substrate

**Suppressed reverse leakage current**

- Schottky diode structures
  - Ni source
  - NiSi$_2$ source
  - Al contact
  - Si substrate

<table>
<thead>
<tr>
<th>Source</th>
<th>$\phi_B$ (eV)</th>
<th>n</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>0.676</td>
<td>1.08</td>
</tr>
<tr>
<td>NiSi$_2$</td>
<td>0.659</td>
<td>1.00</td>
</tr>
</tbody>
</table>

RTA: 500°C, 1min

Current density (A/cm$^2$) vs. Applied Voltage (V)
Conclusions

Si-MOSFET is the most fundamental and smallest functional device available for manufacturing.

It is really amazing to keep the evolution for so many generations without being replaced by any other device.
The device downsizing of Si-MOSFET will be ended within 10 \sim 20 years because $I_{off}$ increases at the size of sub-5nm.

In order to reach the limit, R&D for nanowire, high-k for sub-5nm EOT, silicide S/D, and maybe III/V channels are necessary.

There are many rooms for the universities to contribute to the development.
Finally, even after the end of Si-MOSFET downsizing, Si-CMOS technology will still be the mainstream IC technology for a long period, as no other device technology seems to be developed into a comparable integration scale as the present CMOS technology in foreseeable future.
Thank you for your attention!