Future of nano CMOS Technology to

December 3, 2012

EDSSC@Bankok, Thailand

Hiroshi Iwai,
Tokyo Institute of Technology
1900 “Electronics” started.
   Device: Vacuum tube
   Device feature size: 10 cm
   Major Appl.: Amplifier (Radio, TV, Wireless etc.)
   \rightarrow Technology Revolution

1970 “Micro-Electronics” started.
   Device: Si MOS integrated circuits
   Device feature size: 10 \mu m
   Major Appl.: Digital (Computer, PC, etc.)
   \rightarrow Technology Revolution
2000 “Nano-Electronics” started.

Device: Still, Si CMOS integrated circuits
Device feature size: 100 nm
Major Appl.: Digital (μ-processor, cell phone, etc.)

→ Technology Revolution??

Maybe, just evolution or innovation!


Device: Still, Si CMOS integrated circuits
Device feature size: 10 nm
Major Appl.: Digital (μ-processor, cell phone, etc.)
Future, “Nano-Electronics” still continued?

Device: Still, Si CMOS integrated circuits?
Device feature size: ? nm, what is the limit?

Application: New application?

→Technology Revolution?
Future, “Nano-Electronics” still continued?

Device: Still, Si CMOS integrated circuits?
Device feature size: ? nm, what is the limit?
Application: New application?

→ Technology Revolution?
What is special or new for Nano-Electronics?

In 1990’s, people expected completely new mechanism or operational principle due the nano size, like quantum mechanical effects.

However, no fancy new operational principle was found.

At least for logic application, there is no success story for “Beyond CMOS devices” to replace Si-CMOS.
Ballistic conduction will not happen even decreasing channel length.

\[ L \gg \lambda \]

**Diffusive transport**

\[ L \sim \lambda \]

**Quasi-Ballistic transport**

\[ L < \lambda \]

**Ballistic transport**

Ballistic transport will never happen for MOSFET because of back scattering.

With decreasing channel length, Drain current increase continue.

Also, 1D quantum conduction, or ballistic conduction will not happen.

(1D quantum conduction: 77.8\(\mu\)S regardless of the length and material).
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament
→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power consumption
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

Al Gate

Drain

Si

Si/SiO2 Interface is extraordinarily good

Al

SiO₂

Si
1970,71: 1st generation of LSIs

DRAM   Intel 1103

MPU    Intel 4004
In 2012

Most Recent SD Card

128GB (Bite)  
= 128G X 8bit  
= 1T(Tera)bit

1T = 10^{12} = 1Trillion

World Population : 7 Billion  
Brain Cell : 10\sim100 Billion  
Stars in Galaxy : 100 Billion
128 GB = 1Tbit

2.4cm X 3.2cm X 0.21cm

Volume: 1.6cm³  Weight: 2g

Voltage: 2.7 - 3.6V

Old Vacuum Tube:
5cm X 5cm X 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube: 5cm X 5cm X 10cm

Volume = (5cm X 10,000) X (5cm X 10,000) X (10cm X 10,000)
= 0.5km X 0.5km X 1km

1Tbit = 10,000 X 10,000 X 10,000 bit

Pingan International Finance Center, Shanghai, China (Year 2016)
Indian Tower, Mumbai, India (Year 2016)
Burj Khalifa, Dubai, UAE (Year 2010)
Old Vacuum Tube: 100W

Nuclear Power Generator: 1MkW=1BW

1Tbit = 10^{12} \text{bit}

Power = 0.05 \text{kW} \times 10^{12} = 50 \text{ TW}

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving.
Brain: Integrated Circuits

Ear, Eye : Sensor

Mouth : RF/Opto device

Stomach : PV device

Hands, Legs : Power device
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years!!

Gartner: By K. Kim, CSTIC 2012

313 billion dollar (US) in 2011

1,528 billion dollar (US) in 2025

Gartner
**Downsizing**

1. **Reduce Capacitance**
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. **Increase number of Transistors**
   - Parallel processing
     - Increase circuit operation speed

---

Downsizing contribute to the performance increase in double ways

**Thus, downsizing of Si devices is the most important and critical issue.**
Feature Size/Technology Node

(1970) 10 µm → 8 µm → 6 µm → 4 µm → 3 µm → 2 µm → 1.2 µm →
0.8 µm → 0.5 µm → 0.35 µm → 0.25 µm → 180 nm → 130 nm → 90 nm →
65 nm → 45 nm → 32 nm → 22 nm (2012)

Averaged downsizing rate (in the past 42 years): ~ 0.7X every 3 years

Total reduction in 19 generations: Gate Length ~ 1/500, Area ~ 1/250,000
$t_{ox}$ and $V_{dd}$ have to be decreased for better channel potential control $\rightarrow I_{OFF}$ Suppression
What would be the limit of downsizing!

Tunneling distance

3 nm

Source

Channel

Drain
Subthreshold leakage current of MOSFET

Subthreshold leakage current of MOSFET

Subthreshold Current Is OK at Single Tr. level
But not OK For Billions of Trs.

Subthreshold Leakage Current

Vg=0V

Vth (Threshold Voltage)
Subthreshold leakage current will limit the downsizing
The limit is deferent depending on application

HP CMOS (high Performance)
- Highest Ion, Lowest CV/I
- High leakage
- Medium Vdd

LOP CMOS
(Low Operation Power)
- Lowest Vdd
- Medium Ion, medium CV/I
- Medium leakage

LSTP CMOS
(Low Standby Power)
- Lowest leakage
- Low Ion, high CV/I
- High Vdd

Source: 2007 ITRS Winter Public Conf.
How far can we go for production?

**Past**
0.7 times per 3 years

1970年

10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm →
0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

**In 40 years:** 18 generations,
Size 1/300, Area 1/100,000

**Now**

→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

**Future**

• At least 4,5 generations to 8 ~ 5 nm
Suppression of subthreshold leakage by surrounding gate structure

Planar

Surrounding gate
Because of off-leakage control,

Planar $\rightarrow$ Fin $\rightarrow$ Nanowire

Planar FET

Fin FET

Nanowire FET

Double-Gate FinFET
($T_{si} = \frac{2}{3} L_2$)

Omega FinFET
($T_{si} = L_2$)

Nanowire FinFET
($T_{si} = 2L_2$)
Nanowire structures in a wide meaning

Fin
Tri-gate
Ω-gate
All-around
More Moore to More More Moore

Technology node

<table>
<thead>
<tr>
<th>Now</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td>65nm</td>
<td>15nm, 11nm, 8nm, 5nm, 3nm</td>
</tr>
<tr>
<td>L_g 35nm</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>45nm</td>
<td></td>
</tr>
<tr>
<td>L_g 30nm</td>
<td></td>
</tr>
<tr>
<td>32nm</td>
<td></td>
</tr>
<tr>
<td>22nm</td>
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</tr>
</tbody>
</table>

Main stream
( Fin, Tri, Nanowire)

Planar
Tri-Gate
Alternative

Alternative ( III-V/Ge)
Channel FinFET
Emerging Devices

Si is still main stream for future !!

M. Bohr, pp. 1, IEDM2011 (Intel)
P. Packan, pp. 659, IEDM2009 (Intel)
C. Auth et al., pp. 131, VLSI2012 (Intel)
T. B. Hook, pp. 115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp. 297, IEDM2009 (IBM)
High-k gate dielectrics

Hf-based oxides

<table>
<thead>
<tr>
<th>Thickness</th>
<th>EOT</th>
</tr>
</thead>
<tbody>
<tr>
<td>45nm</td>
<td>1nm</td>
</tr>
<tr>
<td>32nm</td>
<td>0.95nm</td>
</tr>
<tr>
<td>22nm</td>
<td>0.9nm</td>
</tr>
<tr>
<td>15nm, 11nm, 8nm, 5nm, 3nm,</td>
<td></td>
</tr>
</tbody>
</table>

SiO₂ IL (Interfacial Layer) is used at Si interface to obtain good mobility.

Remote SiO₂-IL scavenging HfO₂ (IBM)

EOT=0.52 nm

Direct contact with La-silicate (Tokyo Tech.)

K. Mistry, et al., p.247, IEDM 2007, (Intel)
T.C. Chen, et al., p.8, VLSI 2009, (IBM)
T. Ando, et al., p.423, IEDM 2009, (IBM)
**ION** and **IOFF** benchmark

### NMOS

- Intel [1] Bulk 32nm $V_{DD}=0.8\text{V}$
- Intel [1] Tri-Gate 22nm $V_{DD}=0.8\text{V}$
- Intel [2] Bulk 45nm $V_{DD}=1\text{V}$
- Samsung [3] Bulk 20nm $V_{DD}=0.9\text{V}$
- Toshiba [4] Tri-Gate NW $V_{DD}=1\text{V}$
- IBM [7] ETSOI $V_{DD}=1\text{V}$
- IBM [6] FinFET 25nm $V_{DD}=1\text{V}$
- STMicro. [8] GAA NW $V_{DD}=0.9\text{V}$
- STMicro. [8] GAA NW $V_{DD}=1.1\text{V}$

### PMOS

- Intel [1] Bulk 32nm $V_{DD}=0.8\text{V}$
- Intel [2] Bulk 45nm $V_{DD}=1\text{V}$
- Intel [1] Tri-Gate 22nm $V_{DD}=0.8\text{V}$
- IBM [7] ETSOI $V_{DD}=0.9\text{V}$
- IBM [6] FinFET 25nm $V_{DD}=1\text{V}$
- IBM [5] GAA NW $V_{DD}=1\text{V}$
- STMicro. [8] GAA NW $V_{DD}=1.1\text{V}$

Comparison with ITRS

K. Mistry et al., pp.247, IEDM2007 (Intel).
P. Packan et al., pp.659, IEDM2009 (Intel).
C. Auth et al., pp.131, VLSI2012 (Intel).
## Benchmark of device characteristics

<table>
<thead>
<tr>
<th>Structure</th>
<th>Bulk Planar</th>
<th>Tri-Gate 22nm</th>
<th>Tri-Gate NW</th>
<th>ETSOI</th>
<th>Bulk Planar</th>
<th>GAA NW</th>
<th>GAA NW</th>
<th>Ω-gate NW</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$ (nm)</td>
<td>35</td>
<td>30</td>
<td>30</td>
<td>14</td>
<td>22</td>
<td>35/25</td>
<td>22/30</td>
<td>65</td>
</tr>
<tr>
<td>Gate Dielectrics</td>
<td>Hf-based</td>
<td>Hf-based</td>
<td>SiO₂</td>
<td>HfO₂</td>
<td>HfO₂ ?</td>
<td>Hf-based</td>
<td>HfZrO₂</td>
<td>SiO₂</td>
</tr>
<tr>
<td>EOT (nm)</td>
<td>1</td>
<td>0.95</td>
<td>0.9</td>
<td>3</td>
<td>~1</td>
<td>-</td>
<td>1.5</td>
<td>-</td>
</tr>
<tr>
<td>$V_{th}$ (V)</td>
<td>~0.4</td>
<td>~0.3</td>
<td>~0.2</td>
<td>~0.15 (nFET)</td>
<td>0.3~0.4</td>
<td>~0.3</td>
<td>0.3~0.4</td>
<td>~0.5</td>
</tr>
<tr>
<td>$V_{DD}$ (V)</td>
<td>1</td>
<td>1</td>
<td>0.8</td>
<td>1</td>
<td>1</td>
<td>0.9</td>
<td>1</td>
<td>1.1</td>
</tr>
<tr>
<td>$I_{ON}$ (mA/um)</td>
<td>1.36/1.07</td>
<td>1.53/1.23</td>
<td>1.26/1.1</td>
<td>0.83 (nFET)</td>
<td>1.65/1.25</td>
<td>1.2/1.05</td>
<td>0.83/0.95</td>
<td>2.05/1.5</td>
</tr>
<tr>
<td>$DIBL$ (mV/V)</td>
<td>~150</td>
<td>~200</td>
<td>46/50</td>
<td>&lt;50</td>
<td>75/130</td>
<td>104/115</td>
<td>65/105</td>
<td>56/9</td>
</tr>
<tr>
<td>$SS$ (mV/dec)</td>
<td>-</td>
<td>~100</td>
<td>~70</td>
<td>&lt;80</td>
<td>&lt;90</td>
<td>87</td>
<td>85</td>
<td>&lt;80</td>
</tr>
</tbody>
</table>
The down scaling of MOSFETs is still possible for at least another 10 years!

4 important technological items for down scaling.

New structures
1. Wire channel

New materials
2. Thinning of high-k gate oxide thickness beyond 0.5 nm
3. Metal(Silicide) S/D
4. III-V/Ge channel, for the moment, however, very difficult to replace Si
These technologies are very difficult and not every company can succeed in the development timely.

In the past, technology comes with the purchase of equipment, but any more.

Thus, some of the companies are in the threat of dropping off.

There are so many rooms for the universities to contribute to the development of Si world.
Wire channel
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of $I_{OFF}$
3. High drive current

1D ballistic conduction

Multiquantum Channel

High integration of wires

Leakage current
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Compact modeling of nanowire MOSFETs is very difficult
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Wire cross section dependence.
What cross section gives best solution for SCE suppression and drive current?

By Profs. Oshiyama and Iwata, U. of Tokyo
Compact model for circuit designer is very important.

- **Diffusive transport**
  - \( \lambda \gg L \)
  - Mobility Theory

- **Quasi-Ballistic transport**
  - \( L \sim \lambda \)

- **Ballistic transport**
  - \( L < \lambda \)

Real nanoscale MOSFETs

Prof. K. Natori of TIT
Prof. K. Natori of TIT
チャネル内の電子散乱導入の考え方

透過確率

\[ T(\varepsilon) = \frac{(F(0) - G(0))}{F(0)} \]

ドレインからの入射=0

\[ I_D = \frac{q}{\pi \hbar} \sum_i \int \left[ f(E, \mu_S) - f(E, \mu_D) \right] T_i(E)dE \]

Prof. K. Natori of TIT
散乱の導入に係る計算式

弾性散乱域

\[ \sqrt{\frac{2}{m}} \left( qEx + \varepsilon \right) \frac{dF(x)}{dx} + \frac{B_0}{\sqrt{qEx + \varepsilon}} \{ F(x) - G(x) \} = 0 \]

\[ -\sqrt{\frac{2}{m}} \left( qEx + \varepsilon \right) \frac{dG(x)}{dx} + \frac{B_0}{\sqrt{qEx + \varepsilon}} \{ G(x) - F(x) \} = 0 \]

光学フォノン放出域

\[ \sqrt{\frac{2}{m}} \left( qEx + \varepsilon \right) \frac{dF(x)}{dx} + \frac{B_0}{\sqrt{qEx + \varepsilon}} \{ F(x) - G(x) \} + \frac{2D_0}{\sqrt{qEx + \varepsilon - \varepsilon^\star}} F(x) = 0 \]

\[ -\sqrt{\frac{2}{m}} \left( qEx + \varepsilon \right) \frac{dG(x)}{dx} + \frac{B_0}{\sqrt{qEx + \varepsilon}} \{ G(x) - F(x) \} + \frac{2D_0}{\sqrt{qEx + \varepsilon - \varepsilon^\star}} G(x) = 0 \]

ソースからドレインへの透過確率（エネルギー \( \varepsilon \) に対して）

\[ T(\varepsilon) = \frac{\sqrt{2D_0} qE}{\left( \sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0} B_0 \ln \left( \frac{qEx_0 + \varepsilon}{\varepsilon} \right)} \]
Prof. K. Natori of TIT
$V_g - V_{th} = 1\text{V}$

Experiment

Quasi ballistic

Vd (V)

Id (A)
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off > 10^6, 60 uA/wire

L_g = 65 nm, T_ox = 3 nm
Bench Mark

![Graph showing I_{ON} (µA/wire) vs. Gate Length (nm) with markers for nMOS and pMOS, and V_{DD} range of 1.0~1.5 V.]

- nMOS: 102 µA (10x20)
- pMOS: (12x19) (12x19) (10x20) (9x14) (13x20) (10x20) (12x19) (10x20) (30) (19)

- Our Work

V_{DD}: 1.0~1.5 V

- VDD: 1.0~1.5 V

- Gate Length (nm) vs. I_{ON} (µA/wire) graph
$I_{ON}/I_{OFF}$ Bench mark

This work

Planer FET ▲ ▶ 1.0～1.1V
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

Si nanowireFET ★ 1.2～1.3V
Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240
Electron Density

\( \times 10^{19} \text{cm}^{-3} \)

Distance from SiNW Surface (nm)

**Edge portion**

**Flat portion**

Inversion areal ratio: 29%
Primitive estimation!

- SiNW (12nm □ 19nm)
- Small EOT for high-k (33)
- P-MOS improvement (26)
- Low S/D resistance (20)
- # of wires /1µm (15)
- Compact model

**Compact model**

$I_{ON} \propto L_g^{-0.5} T_{ox}^{-1}$

**Assumption**

- P-MOS improvement (26)
- Low S/D resistance (20)
- # of wires /1µm (15)
- SiNW (12nm □ 19nm)
Tri-gate implementation for transistors

C. Auth et al., pp.131, VLSI2012 (Intel)

<table>
<thead>
<tr>
<th></th>
<th>HP</th>
<th>MP</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{OX,E}$ (nm)</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>$L_{GATE}$ (nm)</td>
<td>30</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>$I_{OFF}$ (nA/um)</td>
<td>20-100</td>
<td>5-20</td>
<td>1-5</td>
</tr>
</tbody>
</table>

Tri-gate has been implemented at 22nm node, enabling further scaling
Tri-gate width/height optimization

C. Auth et al., pp.131, VLSI2012 (Intel)

PMOS channel under the gate

S/D region showing the SiGe epitaxy

A fin width of 8nm to balance SCE and $R_{\text{ext}}$

A fin height of 34nm to balance drive current vs. capacitance
- SS of 69 and 72mV/dec for NMOS and PMOS, respectively
- DIBL of 46 and 50mV/V for NMOS and PMOS, respectively
- $V_{th}$ of 22nm is about 0.1V lower than that of 32nm
• $L_g = 22\text{nm ETSOI}$
• Si channel thickness of 6 nm
• DIBL of 75 mV/V and 130mV/V for NFET and PFET
Gate All Around Nanowire (GAA NW)

- \( L_g = 25\sim35\text{nm} \) GAA NW
- Hydrogen anneal provide smooth channel surface
- Competitive with conventional CMOS technologies
- Scaling the dimensions of NW leads to suppressed SCE
Problems in Multi-gate

S. Bangsaruntip et al., pp.297, IEDM2009 (IBM),
K. Tachi et al., pp.313, IEDM2009 (CEA-LETI)

Decreasing the diameter of NW

Improved short-channel control  Severe mobility degradation
Problems in SOI

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.
Wire/fin mitigates EOT thinning trend (Trend 1 $\rightarrow$ Trend 2) Because of better SCE control.

However, $I_{\text{ON}}$ severely degrade with wire/fin width reduction

Therefore, EOT trend will become accelerated again (Trend 2 $\rightarrow$ Trend 3) $\rightarrow$ Thus, high-k becomes important again.
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-k is necessary.
High-k beyond 0.5 nm
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Flat metal/high-k interface for better mobility
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Interface dipole control for $V_{th}$ tuning
- Suppression of FLP
- Remove contamination introduced by CVD
- Thinning or removal of $\text{SiO}_2$-IL for small EOT
- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Reliability: PBTI, NBTI, TDDB
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

![Diagram showing the relationship between conduction band offset and dielectric constant with data points for various oxides, including SiO$_2$, Gd$_2$O$_3$, La$_2$O$_3$, Lu$_2$O$_3$, ZrO$_2$, and HfO$_2$. The diagram includes a reference to XPS measurement by Prof. T. Hattori, INFOS 2003.]
 Candidates

Unstable at Si interface

- Si + MOx M + SiO2
- Si + MOx MSiX + SiO2
- Si + MOx M + MSiXOY

Gas or liquid at 1000 K

- Radio active
- He

<table>
<thead>
<tr>
<th>B</th>
<th>C</th>
<th>N</th>
<th>O</th>
<th>F</th>
<th>Ne</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Al</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>P</td>
<td>S</td>
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</table>

Candidates unstable at Si interface:

La2O3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

HfO2 based dielectrics are selected as the first generation materials, because of their merit in:
1) band-offset, 2) dielectric constant, 3) thermal stability.

Choice of High-k elements for oxide are selected as the first generation materials, because of their merit in:
1) band-offset, 2) dielectric constant, 3) thermal stability.

R. Hauser, IEDM Short Course, 1999
Direct high-k/Si by silicate reaction

HfO₂ case

Low Pₐₒ₂ → High Pₐₒ₂

HfSiₓ

Si substrate

(k~4)

HfO₂

SiO₂-IL

La₂O₃ case

Low Pₐₒ₂ → High Pₐₒ₂

LaSiₓ

Si substrate

(k~4)

La₂O₃

silicate

SiO₂-IL

Our approach

Direct contact can be achieved with La₂O₃ by forming silicate at interface
Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
SiO\textsubscript{x}-IL growth at HfO\textsubscript{2}/Si Interface

Phase separator

\[
\text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2
\]

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Trans. ECS 11, 319

\textbf{SiO}_{x}-\text{IL} is formed after annealing
Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-$k$/Si is possible

La$_2$O$_3$ can achieve direct contact of high-$k$/Si

La$_2$O$_3$ + Si + nO$_2$

- La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

W

1 nm

La$_2$O$_3$  k=23

La-silicate  k=8~14

TEM image 500 °C, 30 min

XPS Si1s spectra
For the past 45 years, SiO₂ and SiON have been used for gate insulators. Today, EOT=1.0nm. EOT can be reduced further to 0.5~0.7nm by using direct contact to Si and choosing appropriate materials and processes. This introduction of High-k materials allows for one order of magnitude reduction in EOT. The EOT limit for high-k materials is still SiO₂ or SiON, which is used at the Si interface. Direct contact of high-k and Si is achieved, leading to a significant reduction in EOT.
High-k/metal gate stack film deposition cluster tool
L = 0.5~100 µm (8 kinds)
W = 10, 20, 50, 100 µm (4 kinds)

30 different Trs
26 chips

1 cm × 1 cm
Shutter movement

Chip

high-k

Metal

Si

Metal

Si

Metal

Si

Thin

Thick

Id(V)

Vth=-0.04V

Vth=-0.05V

Vth=-0.06V

Vth=-0.07V

Vth=-0.08V

Vth=-0.09V

Vth=-0.10V

Vth=-0.11V

Vth=-0.12V

Vth=-0.13V

Vth=-0.14V

Vth=-0.15V

Vth=-0.16V

Vth=-0.17V

Vth=-0.18V

Vth=-0.19V

Vth=-0.20V

Vth=-0.21V

Vth=-0.22V

Vth=-0.23V

Vth=-0.24V

Vth=-0.25V

Vth=-0.26V

Vth=-0.27V

Vth=-0.28V

Vth=-0.29V

Vth=-0.30V

Vth=-0.31V

Vth=-0.32V

Vth=-0.33V

Vth=-0.34V

Vth=-0.35V

Vth=-0.36V

Vth=-0.37V

Vth=-0.38V

Vth=-0.39V

Vth=-0.40V

Vth=-0.41V

Vth=-0.42V

Vth=-0.43V

Vth=-0.44V

Vth=-0.45V

Vth=-0.46V

Vth=-0.47V

Vth=-0.48V

Vth=-0.49V

Vth=-0.50V

Vth=-0.51V

Vth=-0.52V

Vth=-0.53V

Vth=-0.54V

Vth=-0.55V

Vth=-0.56V

Vth=-0.57V

Vth=-0.58V

Vth=-0.59V

Vth=-0.60V

Vth=-0.61V

Vth=-0.62V

Vth=-0.63V

Vth=-0.64V

Vth=-0.65V

Vth=-0.66V

Vth=-0.67V

Vth=-0.68V

Vth=-0.69V

Vth=-0.70V

Vth=-0.71V

Vth=-0.72V

Vth=-0.73V

Vth=-0.74V

Vth=-0.75V

Vth=-0.76V

Vth=-0.77V

Vth=-0.78V

Vth=-0.79V

Vth=-0.80V

Vth=-0.81V

Vth=-0.82V

Vth=-0.83V

Vth=-0.84V

Vth=-0.85V

Vth=-0.86V

Vth=-0.87V

Vth=-0.88V

Vth=-0.89V

Vth=-0.90V

Vth=-0.91V

Vth=-0.92V

Vth=-0.93V

Vth=-0.94V

Vth=-0.95V

Vth=-0.96V

Vth=-0.97V

Vth=-0.98V

Vth=-0.99V

Vth=-1.00V
Gate Leakage vs EOT, ($V_g=|1|V$)

- **Al2O3**
- **HfAlO(N)**
- **HfO2**
- **HfSiO(N)**
- **HfTaO**
- **La2O3**
- **Nd2O3**
- **Pr2O3**
- **PrSiO**
- **PrTiO**
- **SiON/SiN**
- **Sm2O3**
- **SrTiO3**
- **Ta2O5**
- **TiO2**
- **ZrO2(N)**
- **ZrSiO**
- **ZrAlO(N)**

![Graph showing gate leakage vs EOT](image-url)
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small $D_{it}$

- Silicate-reaction-formed fresh interface
- Stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress

La$_2$O$_3$

$K_{av} \sim 8$

$K_{av} \sim 12$

$K_{av} \sim 16$

No interfacial layer can be confirmed with Si/TiN/W
La$_2$O$_3$/silicate/$n$-Si CV

![Graph showing capacitance density vs. gate voltage for W/La$_2$O$_3$(4nm)/$n$-Si at 600°C, 30min.](image)
$G_p/\omega$ (F/cm²)

$D_{it}, D_{slow}$

(10^-6)

(FG anneal)

$D_{it}$

$D_{slow}$

$D_{it}$

$D_{slow}$

Annealing temperature (°C)

$D_{it}$, $D_{slow}$ (cm²/eV)
Slow trap state

\[ \sigma_{\text{it}}, \sigma_{\text{slow}} (\text{cm}^2) \]

\[ \Delta V_{fb} (V) = 0.1, 0.2, 0.3 \]

\[ D_{\text{slow}} = 2.8 \times 10^{13} \text{cm}^{-2}/\text{eV} \]

\[ \Delta V_{fb} = C_{\text{La}_2\text{O}_3} / qD_{\text{slow}} \]

It is important to change the \( \text{La}_2\text{O}_3 \) to La-silicate completely.
As deposited

Annealed for 2 s

La$_2$O$_3$(3.5 nm)

W(60 nm)

TiN/W(6 nm)

TiN(45nm)/W(6nm)

Annealing temperature (°C)

EOT (nm)

EOT=0.55nm

Experiment

Cvc fitting

Theory

TaN/(45nm)/W(3nm)

900°C, 30min

EOT=0.55nm

Vg (V)

Cg (μF/cm²)
Flat-band voltage (V)

EOT (nm)

900°C, 30min

TaN(45nm)/W(3nm)

$Q_{\text{fix}} = 1 \times 10^{11} \text{ cm}^{-2}$

Fixed Charge density: $1 \times 10^{11} \text{ cm}^{-2}$
EOT = 0.53nm

- L/W = 20/20µm
- T = 300K
- N_{sub} = 3 \times 10^{16} cm^{-3}
- E_{eff} = 1 MV/cm
- 151 cm²/Vs

Drain Current (µA) vs. Drain Voltage (V)

- V_{g} = 1.0V
- V_{g} = 0.8V
- V_{g} = 0.6V
- V_{g} = 0.4V
- V_{g} = 0.2V
- V_{g} = 0 V

Electron Mobility [cm²/Vsec]

- E_{eff} = 150 cm²/Vs

- EOT = 0.53nm
- L/W = 20/20µm
- T = 300K
- N_{sub} = 3 \times 10^{16} cm^{-3}
Gate current (A/cm²) vs. Gate voltage (V)

- **TaN/W/LaSiOₓ/nFET**
  - $W_g/L_g = 20/20 \mu m$
  - EOT = 0.55 nm

**ITRS**

- Increased by a factor of 1/100
EOT = 0.40 nm

- Drain Voltage (V)
- Drain Current (mA)
- $V_g = 0.2 V$
- $V_g = 0.4 V$
- $V_g = 0.6 V$
- $V_g = 0.8 V$
- $V_g = 1.0 V$
- L/W = 5/20 μm
- $T = 300 K$
- $N_{sub} = 3 \times 10^{16} cm^{-3}$

Electron Mobility [cm²/Vsec]

- EOT = 0.40 nm
- L/W = 5/20 μm
- $T = 300 K$
- $N_{sub} = 3 \times 10^{16} cm^{-3}$
Benchmark of La-silicate dielectrics

Gate leakage is two orders of magnitude lower than that of ITRS.

Electron mobility is comparable to record mobility with Hf-based oxides.
Gate leakage current and mobility

[Graph showing gate leakage current ($J_g$) at $V_g = 1V$ as a function of EOT (n m) for different materials.]

- $J_g$ at $V_g = 1V$ [A/cm$^2$]
- EOT [nm]
- $A = 10 \times 10\mu m^2$

ITRS requirements:
- $10^{-3}$ [A/cm$^2$]
- $x1/100$

Electron Mobility [cm$^2$/Vsec]

- $EOT$ [nm]
- 0.5 to 0.8 [nm]

Materials:
- $\text{LaSi}_x\text{O}_y$
- $\text{HfO}_x$
- $\text{T = 300K}$

Other: Hf-based oxides
### Si benchmark (nMOSFET)

<table>
<thead>
<tr>
<th>Gate stack</th>
<th>EOT</th>
<th>Mobility</th>
<th>$V_{th}$</th>
<th>SS</th>
<th>DIBL</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.52nm</td>
<td>110cm$^2$/Vs (at 1x$10^{13}$cm$^{-2}$)</td>
<td>~0.4V (L$_g$=24nm)</td>
<td>90mV/dec</td>
<td>147mV/V</td>
<td>IBM VLSI2011</td>
</tr>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.55nm</td>
<td>140cm$^2$/Vs (at 1MV/cm)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IBM VLSI2009</td>
</tr>
<tr>
<td>Metal$^{(A)}$/Cap/HfO$_2$</td>
<td>0.5nm</td>
<td>110cm$^2$/Vs (at 0.8MV/cm)</td>
<td>0.3V (L$_g$=1um)</td>
<td>—</td>
<td>—</td>
<td>IMEC IEDM2009</td>
</tr>
<tr>
<td>Metal/HfO$_2$</td>
<td>0.59nm</td>
<td>130cm$^2$/Vs (at 1MV/cm)</td>
<td>0.45V (L$_g$=1um)</td>
<td>75mV/dec</td>
<td>—</td>
<td>Sematech VLSI2009</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.65nm</td>
<td>—</td>
<td>0.3~0.4V (L$_g$=~30nm)</td>
<td>90mV/dec</td>
<td>100mV/V</td>
<td>Samsung VLSI2011</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.95nm</td>
<td>—</td>
<td>~0.3V (L$_g$=30nm)</td>
<td>100mV/dec</td>
<td>~200mV/V</td>
<td>Intel IEDM2009</td>
</tr>
<tr>
<td>W/La-silicate</td>
<td>0.62nm</td>
<td>155cm$^2$/Vs (at 1MV/cm)</td>
<td>~0.08V (L$_g$=10um)</td>
<td>~70mV/dec</td>
<td>—</td>
<td>Tokyo Tech. T-ED2012</td>
</tr>
</tbody>
</table>
Recent results by my group.
ALD of La2O3


Precursor (ligand)

La(iPrCp)3

La(FAMD)3

ALD is indispensable from the manufacturing viewpoint
- precise control of film thickness and good uniformity
Why high mobility channel materials?
Arming higher performance at lower supply voltage

Both 1) and 2) are important

1) High injection Velocity of carriers $v_{\text{inj}}$

2) High mobility of carriers

Problems: Technologies and Cost

- Interfacial properties at the gate insulator/semiconductor
- Contact resistance at Source/Drain and semiconductor
- Different semiconductors for n- and p- channel FETs

Integration on Si wafer
# Ge, III-V bulk properties

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>electron mob. (cm²/Vs)</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
</tr>
<tr>
<td>electron effective mass (/m₀)</td>
<td>m₄: 0.19; m₁: 0.916</td>
<td>m₄: 0.082; m₁: 1.467</td>
<td>0.067</td>
<td>0.08</td>
<td>0.026</td>
<td>0.0135</td>
</tr>
<tr>
<td>hole mob. (cm²/Vs)</td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td>hole effective mass (/m₀)</td>
<td>m₄₉: 0.49; m₁₉: 0.16</td>
<td>m₄₉: 0.28; m₁₉: 0.044</td>
<td>m₄₉: 0.45; m₁₉: 0.082</td>
<td>m₄₉: 0.45; m₁₉: 0.12</td>
<td>m₄₉: 0.57; m₁₉: 0.35</td>
<td>m₄₉: 0.44; m₁₉: 0.016</td>
</tr>
<tr>
<td>band gap (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.14</td>
</tr>
<tr>
<td>permittivity</td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

- Ge ⇒ lightest hole $m^*$ (light electron $m^*$) ⇒ pMOS (CMOS)
- III-V ⇒ light electron $m^*$ ⇒ nMOS
- GaAs·InP ⇒ $E_g$ higher than that in Si ⇒ low power

S. Takagi., IEDM2011, Short course (Tokyo Uni)
Multi-gate III-V and Si benchmark

**nMOS**

- InGaAs GAA
  - $L_{ch}=50\text{nm}$, Dielectric: $10\text{nm}$ Al$_2$O$_3$
  - $V_{DS}=0.5\text{V}$ (Purdue Uni.) [1]

- Si-FinFET 32nm
  - $V_{DS}=0.5\text{V}$ (NUS) [3]

- InGaAs FinFET
  - $L_{ch}=130\text{nm}$, EOT 3.8nm
  - $V_{DS}=0.5\text{V}$ (Intel) [2]

- InGaAs Nanowire
  - $L_g=200\text{nm}$, $T_{ox}=14.8\text{nm}$
  - $V_{DS}=0.5\text{V}$ (Hokkaido Uni.) [4]

- Metal S/D InGaAs-OI
  - $L_{ch}=55\text{nm}$, EOT 3.5nm
  - $V_{DS}=0.5\text{V}$ (Tokyo Uni.) [5]

- InGaAs Tri-gate
  - $L_g=60\text{nm}$, EOT 12A
  - $V_{DS}=0.5\text{V}$ (Hokkaido Uni.) [4]

- Si-FinFET 22nm
  - $V_{DS}=0.5\text{V}$ (Intel) [2]

- Si-bulk 45nm
  - $V_{DS}=0.8\text{V}$ ( Intel) [10]

**pMOS**

- GOI Tri-gate
  - $L_g=65\text{nm}$, EOT 3.0nm
  - $V_D=-1\text{V}$ (AIST Tsukuba) [6]

- Si-FinFET 32nm
  - $V_{DS}=0.8\text{V}$ [10]

- Ge FinFET
  - $L_g=4.5\text{mm}$
  - Dielectric: SiON, $V_{DS}=-1\text{V}$ (Stanford Uni.) [7]

- Ge GAA
  - $L_g=300\text{nm}$, dielectric: GeO$_2$ (7nm)-HfO$_2$ (10nm)
  - $V_D=-0.8\text{V}$ (ASTAR Singapore) [8]

- Ge Tri-gate
  - $L_g=183\text{nm}$, EOT 5.5nm
  - $V_D=-1\text{V}$ (NNDL Taiwan) [9]

- Si-bulk 45nm
  - $V_{DS}=1\text{V}$

---

$I_{ON}/I_{OFF}$ Benchmark of Ge pMOSFET

K. J. Kuhn, ECS Transactions, 33 (6) 3-17 (2010)

Optimization of short channel Ge p-MOSFETs is still under investigation
### III-V/Ge benchmark for various structures

<table>
<thead>
<tr>
<th>Material</th>
<th>Planar (metal S/D, Strain, Buffer...)</th>
<th>FinFET</th>
<th>Tri-gate</th>
<th>Gate-all-around MOSFET</th>
<th>Nanowire</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric/EOT</td>
<td>Al₂O₃/3.5 nm</td>
<td>InGaAs</td>
<td>Ge</td>
<td>InGaSn</td>
<td>InGaAs</td>
</tr>
<tr>
<td>Mobility</td>
<td>-</td>
<td>~600 (cm²/Vs)</td>
<td>N₂: 5e12 e: 200 h: 400 (µS/µm)</td>
<td>~700 (µS/µm)</td>
<td>-</td>
</tr>
<tr>
<td>Lch (nm)</td>
<td>55</td>
<td>W/L=30/5 µm</td>
<td>50 µm</td>
<td>100</td>
<td>4.5 µm</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>84</td>
<td>-</td>
<td>-</td>
<td>180</td>
<td>-</td>
</tr>
<tr>
<td>SS (mV/dec)</td>
<td>105</td>
<td>-</td>
<td>-</td>
<td>145</td>
<td>750</td>
</tr>
<tr>
<td>ION (µA/µm)</td>
<td>278 (V₀=0.5V)</td>
<td>3 (V₀=0.2V)</td>
<td>4 (n,p) (V₀=0.5V)</td>
<td>-</td>
<td>10 (V₀=0.5V)</td>
</tr>
<tr>
<td>Year of Production</td>
<td>2012</td>
<td>2014</td>
<td>2016</td>
<td>2018</td>
<td>2020</td>
</tr>
<tr>
<td>-------------------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>$L_g$ (nm)</td>
<td>22</td>
<td>18</td>
<td>15.3</td>
<td>12.8</td>
<td>10.6</td>
</tr>
<tr>
<td>$V_{dd}$ (V)</td>
<td>0.87</td>
<td>0.82</td>
<td>0.77</td>
<td>0.73</td>
<td>0.68</td>
</tr>
<tr>
<td>$EOT$ (nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bulk</td>
<td>0.84</td>
<td>0.73</td>
<td>0.61</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD SOI</td>
<td>0.8</td>
<td>0.72</td>
<td>0.63</td>
<td>0.54</td>
<td></td>
</tr>
<tr>
<td>*1: MG</td>
<td>0.76</td>
<td>0.68</td>
<td>0.62</td>
<td>0.56</td>
<td>0.50</td>
</tr>
<tr>
<td>Mobility enhancement factor due to strain</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
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<tr>
<td>$C_g$ Ideal (fF/µm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Bulk</td>
<td>0.658</td>
<td>0.611</td>
<td>0.576</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD SOI</td>
<td>0.529</td>
<td></td>
<td></td>
<td>0.429</td>
<td>0.393</td>
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<tr>
<td>MG</td>
<td>0.455</td>
<td>0.409</td>
<td>0.362</td>
<td>0.320</td>
<td>0.284</td>
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<tr>
<td>$V_{t,sat}$ (mV)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bulk</td>
<td>289</td>
<td>302</td>
<td>310</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD SOI</td>
<td>222</td>
<td>227</td>
<td>234</td>
<td>242</td>
<td></td>
</tr>
<tr>
<td>MG</td>
<td>217</td>
<td>223</td>
<td>225</td>
<td>228</td>
<td>231</td>
</tr>
<tr>
<td>$CV/I$ (ps)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NMOS</td>
<td>0.57</td>
<td>0.47</td>
<td>0.38</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD SOI</td>
<td>0.38</td>
<td>0.30</td>
<td>0.24</td>
<td>0.20</td>
<td></td>
</tr>
<tr>
<td>MG</td>
<td>0.29</td>
<td>0.24</td>
<td>0.19</td>
<td>0.16</td>
<td>0.13</td>
</tr>
</tbody>
</table>

Manufacturing solutions exist or is being optimized
Manufacturing solutions are known
Manufacturing solutions are **NOT** known
# ITRS 2011 for Si (HP), contd

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2012</th>
<th>2014</th>
<th>2016</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$ (nm)</td>
<td>22</td>
<td>18</td>
<td>15.3</td>
<td>12.8</td>
<td>10.6</td>
<td>8.9</td>
<td>7.4</td>
<td>5.9</td>
</tr>
<tr>
<td>Equivalent Injection velocity $V_{inj}$ ($10^7$ cm/s)</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bulk</td>
<td>1.09</td>
<td>1.18</td>
<td>1.33</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>FD SOI</td>
<td>1.37</td>
<td>1.51</td>
<td>1.63</td>
<td>1.83</td>
<td></td>
<td></td>
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<tr>
<td>MG</td>
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<td>1.68</td>
<td>1.82</td>
<td>2.05</td>
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<tr>
<td>$I_{d,\text{sat}}$ (mA/µm)</td>
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<td>$R_{sd}$ (Ω-µm)</td>
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<td>Bulk</td>
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<td>0.21</td>
<td>0.17</td>
<td>0.14</td>
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**Manufacturing solutions exist or is being optimized**

**Manufacturing solutions are known**

**Manufacturing solutions are NOT known**
## ITRS 2011 for III-V/Ge

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
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<tr>
<td>( L_g ) (nm)</td>
<td>14</td>
<td>11.7</td>
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<td>Mobility enhancement factor due to channel material</td>
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<tr>
<td>III-V</td>
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<td>Ge</td>
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<td>( C_g ) Ideal ( (fF/\mu m) )</td>
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<td>( CV/I ) (ps)</td>
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Manufacturing solutions are **NOT** known
## ITRS 2011 for III-V/Ge, Contd

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<thead>
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<th>Year of Production</th>
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<th>2022</th>
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<tbody>
<tr>
<td>( L_g ) (nm)</td>
<td>14</td>
<td>11.7</td>
<td>9.3</td>
<td>7.4</td>
<td>5.8</td>
</tr>
<tr>
<td>( E_{\text{inj}} ) (10(^7) cm/s)</td>
<td>III-V</td>
<td>4.29</td>
<td>4.58</td>
<td>5.32</td>
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<td></td>
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<td>2.44</td>
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<td>( I_{d,\text{sat}} ) (mA/(\mu)m)</td>
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<td>2.200</td>
<td>2.343</td>
<td>2.523</td>
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<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>( R_{sd} ) ((\square)-(\mu)m)</td>
<td>III-V</td>
<td>131</td>
<td>113</td>
<td>96</td>
<td>82</td>
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<td>Ge</td>
<td>149</td>
<td>126</td>
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<td>85</td>
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<td>( CV^2 ) (fJ/(\mu)m)</td>
<td>III-V</td>
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<td>0.11</td>
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<td>0.23</td>
<td>0.20</td>
<td>0.16</td>
<td>0.14</td>
</tr>
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</table>

Manufacturing solutions are **NOT** known.
TFET vs. MOSFET at low $V_{DD}$

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

EOT = 1 nm  
LG = 20 nm  
$t_{lnAs} = 5$ nm

V$_{DD}$ 0.3~0.35V  
TFET 8x faster at the same power  
“parameter variation is not a significant factor for differentiation between MOSFET and TFET”
X in Si$_{1-x}$Ge$_x$ is optimized to allow for efficient BTBT

$L_G = 200$ nm

$I_{ON}/I_{OFF} \approx 10^5$

Reducing SiGe

Body thickness improves Subthreshold swing.

130mV/dec

190mV/dec
SS of TFET is function of $V_G$ due to Zener tunnel current

Minimum SS = 21 mV/dec is reached due to optimized series resistance of contact, undoped InAs and InAs/Si

$I_{ON}/I_{OFF} \sim 10^6$ at $V_{DS} = 1.0V$ ($I_{ON} = 1A \mu\mu m$)
Device structure

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

- Tunneling // to the gate oblique to the gate field
- Tunneling ⊥ to the gate in-line with the gate field

- Nanowire TFET gate-all-around - best electrostatics

K. Tomioka et al., pp.47, VLSI2012 (Hokkaido University)
Tunnel FET performance comparison

A. Seabaugh, IEDM 2011 Short Course (University of Notre Dame)

measured III-V channel TFETs

<table>
<thead>
<tr>
<th>Reference</th>
<th>Source</th>
<th>Channel</th>
<th>Dielectric</th>
<th>EOT (nm)</th>
<th>$I_{ON}$ (μA/μm)</th>
<th>$V_{DS}$ (V)</th>
<th>$V_{GS} = V_{ON}$ (V)</th>
<th>$V_{ON} - V_{OFF}$ (V)</th>
<th>$I_{ON}/I_{OFF}$</th>
<th>$S_{MIN}$ (mV/dec)</th>
<th>$S_{EFF}$ (mV/dec)</th>
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<tbody>
<tr>
<td>this work</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$/HfO$_2$</td>
<td>1.6</td>
<td>78</td>
<td>0.5</td>
<td>0.5</td>
<td>1.5</td>
<td>2,000</td>
<td>125</td>
<td>230</td>
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<tr>
<td>Li [4]</td>
<td>Al$<em>{0.45}$Ga$</em>{0.55}$Sb</td>
<td>InAs</td>
<td>Al$_2$O$_3$</td>
<td>3.9</td>
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<td>2</td>
<td>6</td>
<td>210</td>
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<td>Mookerjea [5]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>Al$_2$O$_3$</td>
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<td>2.5</td>
<td>2.5</td>
<td>10,000</td>
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<td>Mohata [6]</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
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<td>2</td>
<td>400,000</td>
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<td>Zhao [7]</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>HfO$_2$</td>
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<td>Ford [9]</td>
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<td>ZrO$_2$</td>
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<td>Zhou [10]</td>
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<td>1</td>
<td>1.75</td>
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- $S_{MIN}$: Most common SS which is the inverse of $I_D$-$V_{GS}$ slope at the steepest part
- $S_{EFF}$: Is the average swing when $V_{TH} = V_{DD}/2$, $V_{OFF} = 0$

Average SS: \[
\frac{V_{TH} - V_{OFF}}{\log(I_D/I_{OFF})}
\]

Effective SS: \[
\frac{V_{DD}}{2\log(I_D/I_{OFF})^{10^7}}
\]
$I_{ON}$ and $I_{OFF}$ of TFETs

[1] G. Zhou et al., pp. 782, vol. 33, no. 6, EDL 2012 (University of Notre Dame)

C. Auth et al., pp.131, VLSI2012 (Intel).

K. Mistry et al., pp.247, IEDM2007 (Intel).
Mechanical Switch: MEMS relay

- ON-state resistance [Ohm]
- Number of Operation Cycles

- Frequency of 1, 5, 25kHz under operation

- $I_{ON}/I_{OFF}$ of $\sim 10^{10}$

Ultra-low-power digital logic applications.

T. K. Liu et al., pp. 43, VLSI2012 (UC Berkeley)
Metal (Silicide) S/D
**Extreme scaling in MOSFET**

- Dopant abruptness at S/D
- $V_t$ and $I_{ON}$ variation
- GIDL

**Metal Schottky S/D junctions**

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Surface or interface control

**Diffusion species:** metal atom (Ni, Co)

- Rough interface at silicide/Si
  - Excess silicide formation
  - Different $\phi_{Bn}$ presented at interface
  - Process temperature dependent composition

**Diffusion species:** Si atom (Ti)

- Surface roughness increases
  - Line dependent resistivity change

Annealing: 650 °C

Si(001) sub. Epitaxial NiSi$_2$

CoSi$_2$ NiSi TiSi$_2$

Top view

Line width of 0.1 $\mu$m

Aglomeration

Deposition of Ni-Si mixed films from NiSi$_2$ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
SEM views of silicide/Si interfaces

Ni source (50nm)
- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

NiSi₂ source (50nm)
- Atomically flat interfaces
- No Si consumption
- Temperature-independent

Ni source
- 600°C, 1min

NiSi₂ source
- 700°C, 1min

Ni source
- 800°C, 1min
Ideal characteristics ($n = 1.00$, suppressed leakage current)

- Flat interface and No Si substrate consumption
- No defects in Si substrate

**NiSi$_2$ source**

**Suppressed reverse leakage current**

- Flat interface and No Si substrate consumption
- No defects in Si substrate
Ni silicide Ni
200nm Si Fin
Fins width 20nm

Growth length

Si Fin Ni silicide
50nm

Growth length

SiO₂ Ni silicide
200nm

Si NW Growth length

SiO₂ Ni silicide
50nm NWs width 20nm

(a) (b)
Conclusions

Si-MOSFET is the most fundamental and smallest functional device available for manufacturing.

It is really amazing to keep the evolution for so many generations without being replaced by any other device.
The device downsizing of Si-MOSFET will be ended within 10 ~ 20 years because $I_{\text{off}}$ increase at the size of sub-5nm.

In order to reach the limit, R&D for nanowire, high-k for sub-5nm EOT, silicide S/D are necessary.

There are many rooms for the universities to contribute to the development.
Finally, even after the end of Si-MOSFET downsizing, Si-CMOS technology will still be the mainstream IC technology for a long period, as no other device technology seems to be developed into a comparable integration scale as the present CMOS technology in foreseeable future.

However, new device research other than Si-CMOS is also very important.
Difference of history

Bio device (brain, even insect): 4 Billion Years from single cell.

MOS IC: only 40 Years
Thank you for your attention!