#2612  Si Nanowire Technology

ESC Symp on Dielectric Materials and Metals for Nanoelectronics and Photonics (E5)

10:00 – 10:30, October 10, 2012

@Rm 313A, Level 3, Hawaiian Convention Center, Honolulu, Hawaii

Hiroshi Iwai
Frontier Research Center, Tokyo Institute of Technology
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power
consumption
1970,71: 1st generation of LSIs

DRAM  Intel 1103

MPU    Intel 4004
Downsizing of the components has been the driving force for circuit evolution.

<table>
<thead>
<tr>
<th>Year</th>
<th>Device</th>
<th>1900</th>
<th>1950</th>
<th>1960</th>
<th>1970</th>
<th>2000</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Vacuum Tube</td>
<td>10 cm</td>
<td>cm</td>
<td>mm</td>
<td>10 µm</td>
<td>100 nm</td>
</tr>
<tr>
<td></td>
<td>Transistor</td>
<td>10⁻¹ m</td>
<td>10⁻² m</td>
<td>10⁻³ m</td>
<td>10⁻⁵ m</td>
<td>10⁻⁷ m</td>
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<td>IC</td>
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<td>LSI</td>
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<td>ULSI</td>
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</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. **We have never experienced such a tremendous reduction of devices in human history.**
In 2012

Most Recent SD Card

128GB (Bite)
= 128G X 8bit
= 1T(Tera)bit

1T = 10^{12} = 1 Trillion

World Population : 7 Billion
Brain Cell : 10~100 Billion
Stars in Galaxy : 100 Billion
128 GB = 1Tbit

2.4cm × 3.2cm × 0.21cm

Volume: 1.6 cm³
Weight: 2g

Voltage: 2.7 - 3.6V

Old Vacuum Tube:

5cm × 5cm × 10cm, 100g, 50W

What are volume and power consumption for 1Tbit
Old Vacuum Tube:
5cm X 5cm X 10cm

1Tbit = 10,000 X 10,000 X 10,000 bit

Volume = (5cm X 10,000) X (5cm X 10,000) X (10cm X 10,000)
= 0.5km X 0.5km X 1km

Pingan Intenational Finance Center
Shanghai, China (Year 2016)

Indian Tower
Mumbai, India (Year 2016)

Burji Khalifa
Dubai, UAE (Year 2010)

500 m
1,000 m

1Tbit
Old Vacuum Tube:

50 W

Nuclear Power Generator

1MkW = 1BW

1Tbit = $10^{12}$bit

Power = $0.1kWX10^{12}=50$ TW

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving.
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Gate oxide
Gate metal
Substrate
Source Drain
Region governed by gate bias
Region governed by drain bias
0V < V_{dep} < 1V
0V < V_{dep} < 1V
0V
0V
0V
0V
Depletion Region (DL)
S
Channel
DL touch with S Region (DL)
Large I_{OFF}
No t_{ox} thinning
Large I_{OFF}
Large I_{OFF}
No t_{ox} thinning
t_{ox} thinning
V_{dd} 0.5V
V_{dd} 1V
V_{dd}
0V
0V
0V
0V
0V
0V
0V
0V
0V
0V
0V
Large I_{OFF}
V_{dd}
V_{dd}
V_{dd}
V_{dd}
t_{ox} and V_{dd} have to be decreased for better channel potential control \( \rightarrow \) I_{OFF} Suppression
What would be the limit of downsizing!

Tunneling distance

Source

Channel

Drain

3 nm
Subthreshold leakage current of MOSFET

Subthreshold Leakage Current

Vg=0V

Subthreshold region

Vth (Threshold Voltage)

Id

Subthreshold Current Is OK at Single Tr. level

But not OK For Billions of Trs.
How far can we go for production?

![Past](0.7 times per 3 years)

In 40 years: 18 generations, Size 1/300, Area 1/100,000

1970年

10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm → 0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

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![Now](Future)

→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

- At least 4.5 generations to 8 ~ 5 nm
The down scaling of MOSFETs is still possible for at least another 10 years!

4 important technological items for down scaling.

**New structures**
1. Wire channel

**New materials**
2. Thinning of high-k gate oxide thickness beyond 0.5 nm
3. Metal(Silicide) S/D
4. III-V/Ge channel, for the moment, however, very difficult to replace Si
These technologies are very difficult and not every company can success in the development timely.

In the past, technology comes with the purchase of equipment, but any more.

Thus, some of the companies are in the threat of dropping off.

There are so many rooms for the universities to contribute to the development of Si world.
Wire channel
Suppression of subthreshold leakage by surrounding gate structure

Planar

Surrounding gate
Because of off-leakage control,

Planar $\rightarrow$ Fin $\rightarrow$ Nanowire

Leakage current
Nanowire structures in a wide meaning

- Fin
- Tri-gate
- Ω-gate
- All-around
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of $I_{OFF}$
3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires

Leakage current

Gate: OFF

Drain-source cut-off
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used

300 K

$E_g = 1.12 \text{ eV}$

$E_1 = 2.0 \text{ eV}$

$E_X = 1.2 \text{ eV}$

$E_\infty = 0.044 \text{ eV}$

$E_{T1} = 3.4 \text{ eV}$

$E_{T2} = 4.2 \text{ eV}$
High drive current
(1.32 mA/µm @ I_{OFF}=117 nA/µm)

DIBL of 62mV/V and SS of 70mV/dec for nFET
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off > 10^6, 60 uA/wire

L_g = 65 nm, T_{ox} = 3 nm
Our Work
Primitve estimation!

\[ I_{ON} \propto L_g^{-0.5} \times T_{ox}^{-1} \]

Compact model

Small EOT for high-k

P-MOS improvement

Low S/D resistance

SiNW (12nm \times 19nm)

Assumption

# of wires /1\mu m

ION \propto L_g^{-0.5} \times T_{ox}^{-1}

ITRS

Bulk

FD

ITRS

MG

Nanowire

Year

Distance from SiNW Surface (nm)

Electron Density ($x10^{19} \text{cm}^{-3}$)

- **Edge portion**
- **Flat portion**

**Electron Density**

**Distance from SiNW Surface (nm)**

- **Figure (a)**: Metal
  - 12 nm
  - 19 nm
  - $V_g = 1 \text{V}$
  - SiO$_2$
  - 44 %

- **Figure (b)**: Inversion areal ratio: 29 %
**ION and IOFF benchmark**

**NMOS**

- Intel [1] Bulk 32nm $V_{DD}=0.8V$
- Intel [1] Tri-Gate 22nm $V_{DD}=0.8V$
- Intel [2] Bulk 45nm $V_{DD}=1V$
- Samsung [3] Bulk 20nm $V_{DD}=0.9V$
- Toshiba [4] Tri-Gate NW $V_{DD}=1V$
- IBM [5] GAA NW $V_{DD}=1V$
- IBM [6] FinFET 25nm $V_{DD}=1V$
- STMicro. [8] GAA NW $V_{DD}=1.1V$
- Tokyo Tech. [9] Ω-gate NW $V_{DD}=1V$

**PMOS**

- Intel [1] Bulk 32nm $V_{DD}=0.8V$
- Intel [1] Tri-Gate 22nm $V_{DD}=0.8V$
- Intel [2] Bulk 45nm $V_{DD}=1V$
- IBM [7] ETSOI $V_{DD}=0.9V$
- Samsung [3] Bulk 20nm $V_{DD}=0.9V$
- IBM [6] FinFET 25nm $V_{DD}=1V$
- STMicro. [8] GAA NW $V_{DD}=1.1V$
- IBM [7] ETSOI $V_{DD}=1V$
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<tbody>
<tr>
<td>Lg (nm)</td>
<td>35 30 30 14 22 20 35/25 (nFET/pFET) 22/30 (nFET/pFET) 65</td>
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<tr>
<td>Lg (nm)</td>
<td>45nm 32nm 45nm 32nm 45nm 32nm 45nm 32nm 45nm 32nm 45nm 32nm</td>
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<td>Gate Dielectrics</td>
<td>Hf-based Hf-based SiO2 HfO2 HfO2 Hf-based HfZrO2 SiO2</td>
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<tr>
<td>EOT (nm)</td>
<td>1 0.95 0.9 3 ~1 - 1.5 - 3</td>
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<tr>
<td>Vth (V)</td>
<td>~0.4 ~0.3 <del>0.2 -0.15 (nFET) 0.3</del>0.4 <del>0.3 0.3</del>0.4 ~0.5 -0.2 (nFET)</td>
<td></td>
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<tr>
<td>VDD (V)</td>
<td>1 1 0.8 1 1 0.9 1 1.1 1</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>ION (mA/μm)</td>
<td>1.36/1.07 1.53/1.23 1.26/1.1 0.83 (nFET) 1.65/1.25 1.2/1.05 0.83/0.95 2.05/1.5 1.32 (nFET)</td>
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<tr>
<td>DIBL (mV/V)</td>
<td>~150 ~200 46/50 &lt;50 75/130 104/115 65/105 56/9 62</td>
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<tr>
<td>SS (mV/dec)</td>
<td>- ~100 ~70 &lt;80 &lt;90 87 85 &lt;80 70</td>
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</table>
Gate All Around Nanowire (GAA NW)

- Gate all around structure
- $L_g$ of 22~30nm
- High drive currents by special stress and channel orientation design
Gate All Around Nanowire (GAA NW)

- \( L_g = 25\sim35\text{nm} \) GAA NW
- Hydrogen anneal provide smooth channel surface
- Competitive with conventional CMOS technologies
- Scaling the dimensions of NW leads to suppressed SCE
More Moore to More More Moore

Technology node

<table>
<thead>
<tr>
<th>65nm</th>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
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</thead>
<tbody>
<tr>
<td>Lg 35nm</td>
<td>Lg 30nm</td>
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</table>

Now

Future

15nm, 11nm, 8nm, 5nm, 3nm

Main stream (Fin,Tri, Nanowire)

Si channel

Planar

Tri-Gate

Alternative (ETSOI)

ET: Extremely Thin

Si is still main stream for future!!

M. Bohr, pp.1, IEDM2011 (Intel)
P. Packan, pp.659, IEDM2009 (Intel)
C. Auth et al., pp.131, VLSI2012 (Intel)
T. B. Hook, pp.115, IEDM2011 (IBM)
S. Bangsaruntip et al., pp.297, IEDM2009 (IBM)
High-k gate dielectrics

Hf-based oxides

- 45nm EOT: 1nm
- 32nm EOT: 0.95nm
- 22nm EOT: 0.9nm
- 15nm, 11nm, 8nm, 5nm, 3nm,

SiO₂ IL (Interfacial Layer) is used at Si interface to obtain good mobility.

Remote SiO₂-IL scavenging

HfO₂ (IBM)

EOT=0.52 nm

HfO₂/SiO₂ (IBM)

EOT=0.9nm

T. Ando, et al., p.423, IEDM2009, (IBM)


K. Mistry, et al., p.247, IEDM 2007, (Intel)

T.C. Chen, et al., p.8, VLSI 2009, (IBM)

T. Ando, et al., p.423, IEDM2009, (IBM)


0.48 → 0.37nm Increase of Iₖ at 30%
Comparison with ITRS

K. Mistry et al., pp.247, IEDM2007 (Intel).
P. Packan et al., pp.659, IEDM2009 (Intel).
C. Auth et al., pp.131, VLSI2012 (Intel).
Tri-gate implementation for transistors

C. Auth et al., pp.131, VLSI2012 (Intel)

<table>
<thead>
<tr>
<th></th>
<th>HP</th>
<th>MP</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{OX,E}$ (nm)</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>$L_{GATE}$ (nm)</td>
<td>30</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>$I_{OFF}$ (nA/um)</td>
<td>20-100</td>
<td>5-20</td>
<td>1-5</td>
</tr>
</tbody>
</table>

Tri-gate has been implemented at 22nm node, enabling further scaling.
Tri-gate width/height optimization

C. Auth et al., pp.131, VLSI2012 (Intel)

PMOS channel under the gate

S/D region showing the SiGe epitaxy

A fin width of 8nm to balance SCE and $R_{\text{ext}}$

A fin height of 34nm to balance drive current vs. capacitance
SS of 69 and 72mV/dec for NMOS and PMOS, respectively
• DIBL of 46 and 50mV/V for NMOS and PMOS, respectively
• $V_{\text{th}}$ of 22nm is about 0.1V lower than that of 32nm
### Tri-gate $I_{ON}$ and $I_{OFF}$ characteristics

C. Auth et al., pp.131, VLSI2012 (Intel)

**NMOS**

<table>
<thead>
<tr>
<th></th>
<th>HP</th>
<th>MP</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ON}$ (mA/μm) NMOS/PMOS</td>
<td>1.26/1.1</td>
<td>1.07/0.95</td>
<td>0.88/0.78</td>
</tr>
<tr>
<td>$I_{OFF}$ (nA/μm)</td>
<td>20-100</td>
<td>5-20</td>
<td>1-5</td>
</tr>
<tr>
<td>$I_{ON}/I_{OFF}$</td>
<td>$\sim 10^5$</td>
<td>$\sim 10^6$</td>
<td>$\sim 10^6$</td>
</tr>
</tbody>
</table>

**PMOS**

**ION/IOFF of $10^5$~$10^6$**

![Graphs showing NMOS and PMOS characteristics](image)
• $L_g = 14$nm Tri-Gate NW
• High SCE immunity at $L_g$ of 14nm
• $V_{th}$ tuning by applying $V_{sub}$ at thin BOX of 20nm
**Bulk Planar**

H.-J. Cho et al., pp.350, IEDM2011 (Samsung)

- $L_g = 20$nm bulk planar CMOS
- Gate last integration
- In-situ doped S/D for better SCE
- $L_g = 22\text{nm} \text{ ETSOI}$
- Si channel thickness of 6 nm
- DIBL of 75 mV/V and 130mV/V for NFET and PFET
Problems in Multi-gate

Decreasing the diameter of NW

Improved short-channel control  Severe mobility degradation

S. Bangsaruntip et al., pp.297, IEDM2009 (IBM),
K. Tachi et al., pp.313, IEDM2009 (CEA-LETI)
Problems in SOI

Mobility is also decreased with decreasing the Si thickness of SOI transistor similar to the NW transistor.
Problem for nanowire

When wire diameter becomes less than 10 nm, sudden drop of $I_d$

1. Electron Scattering of every surface
2. Decrease of DOS

If diameter cannot be scaled, SCE cannot be suppressed.

Then, again aggressive EOT scaling of high-k is necessary.
Wire/fin mitigates EOT thinning trend (Trend 1 $\rightarrow$ Trend 2)
Because of better SCE control.

However, $I_{ON}$ severely degrade with wire/fin width reduction

Therefore, EOT trend will become accelerated again
(Trend 2 $\rightarrow$ Trend 3) $\rightarrow$ Thus, high-k becomes important again.
Diameter dependence

By Profs. Oshiyama and Iwata, U. of Tokyo
Wire cross section dependence.

What cross section gives best solution for SCE suppression and drive current?

By Profs. Oshiyama and Iwata, U. of Tokyo
Conclusions

Si nanowire will be the ultimate structure of scaled-down MOSFETs, with the introduction of new materials such as high-k.

There is a possibility that wire diameter cannot be decreased far from 10 nm due to the significant mobility degradation. In that case, aggressive thinning of EOT becomes necessary.
Thank you for the attention