#2653  Introduction of New Materials into CMOS Devices

ESC Symp on Purity Silicon(E6)

8:30 – 9:00 am, October, 10, 2012

@Rm 320, Level 3,
Hawaiian Convention Center, Honolulu, Hawaii

Hiroshi Iwai

Frontier Research Center, Tokyo Institute of Technology
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Cathode (heated) | Grid | Anode (Positive bias)

Same mechanism as that of transistor
J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928

J. E. LILIENFELD
Capacitor structure with notch

Negative bias

- Gate Electrode
- Gate Insulator
- Semiconductor
- Electron

No current

Positive bias

- Electric field
- Current flows
Surface Potential (Negative direction)

0 bias for gate

Positive bias for gate
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator

Interfacial Charges

Drain Current was several orders of magnitude smaller than expected

Even Shockley!
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

Drain

Al Gate

Si

Si/SiO₂ Interface is exceptionally good
Downsizing of the components has been the driving force for circuit evolution.

<table>
<thead>
<tr>
<th>Year</th>
<th>1900</th>
<th>1950</th>
<th>1960</th>
<th>1970</th>
<th>2000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Devices</td>
<td>Vacuum Tube</td>
<td>Transistor</td>
<td>IC</td>
<td>LSI</td>
<td>ULSI</td>
</tr>
<tr>
<td>Size</td>
<td>10 cm</td>
<td>cm</td>
<td>mm</td>
<td>10 μm</td>
<td>100 nm</td>
</tr>
<tr>
<td></td>
<td>$10^{-1}m$</td>
<td>$10^{-2}m$</td>
<td>$10^{-3}m$</td>
<td>$10^{-5}m$</td>
<td>$10^{-7}m$</td>
</tr>
</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. Reduce Capacitance
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed
2. Increase number of Transistors
   - Parallel processing
     - Increase circuit operation speed

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.
$t_{ox}$ and $V_{dd}$ have to be decreased for better channel potential control $\rightarrow I_{OFF}$ Suppression
Question:

How far we can go with downscaling?
What would be the limit of downsizing?

Tunneling distance

3 nm

Source

Channel

Drain
Subthreshold leakage current of MOSFET

Subthreshold leakage current is OK at Single Tr. level but not OK for billions of Trs.

\[ V_g = 0V \]

Subthreshold region

\[ V_{th} \] (Threshold Voltage)
Subthreshold leakage current will limit the downsizing
The limit is different depending on application.
How far can we go for production?

Past 0.7 times per 3 years  In 40 years: 18 generations, 
Size 1/300, Area 1/100,000

1970年
10μm → 8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm →
0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

Now  Future
→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

• At least 4,5 generations to 8 ~ 5 nm
The down scaling of MOSFETs is still possible for at least another 10 years!

4 important technological items for down scaling.

New structures
1. Wire channel

New materials
2. Thinning of high-k gate oxide thickness beyond 0.5 nm
3. Metal(Silicide) S/D
4. III-V/Ge channel,
   for the moment, however, very difficult to replace Si
MOSFET

Gate electrode

Gate Oxide

Channel

Source Drain

Source

Drain


Channel

Si

III-V/Ge

Gate Oxide

SiO2

SiON

HfO2

LaSiOy

Gate Electrode

Al

Poly Si

WSi2/

Poly Si

NiSi/

Poly Si

Metal

Source Drain

P/B-dope Si

As/B-dope Si

Silicide
High-k beyond 0.5 nm
Wire/fin mitigates EOT thinning trend (Trend 1 → Trend 2)
Because of better SCE control.

However, $I_{ON}$ severely degrade with wire/fin width reduction

Therefore, EOT trend will become accelerated again
(Trend 2 → Trend 3) → Thus, high-k becomes important again.
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Flat metal/high-k interface for better mobility
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k
- Suppression of gate leakage current
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Suppression of FLP
- Interface dipole control for $V_{th}$ tuning
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Reliability: PBTI, NBTI, TDDB
- Endurance for high temperature process
- Suppression of metal diffusion
- Control of interface reaction and Si diffusion to high-k
- Si-sub.
- Metal
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Oxide

Band offset

Si

Dielectric Constant $\varepsilon(0)$

Band Discontinuity [eV]

$\text{Si Band Gap}$

$\text{Lu}_2\text{O}_3$, $\text{Gd}_2\text{O}_3$, $\text{La}_2\text{O}_3$, $\text{ZrO}_2$, $\text{HfO}_2$

XPS measurement by Prof. T. Hattori, INFOS 2003
Choice of High-k elements for oxide

Candidates

Unstable at Si interface

1. Si + MO_x M + SiO_2
2. Si + MO_x MSi_x + SiO_2
3. Si + MO_x M + MSi_xO_y

Gas or liquid at 1000 K

Radio active

HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset, 2) dielectric constant 3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Direct contact can be achieved with La$_2$O$_3$ by forming silicate at interface. Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
SiO$_x$-IL growth at HfO$_2$/Si Interface

![XPS Si1s spectrum](image)  
**500 °C**  
**SiO$_2$**  
**Hf Silicate**  
**Si sub.**

---

**Phase separator**

\[
\text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2
\]

H. Shimizu, JJAP, 44, pp. 6131

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**SiO$_x$-IL** is formed after annealing  
Oxygen control is required for optimizing the reaction

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D.J. Lichtenwalner, Trans. ECS 11, 319
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ can achieve direct contact of high-k/Si
For the past 45 years, SiO2 and SiON have been used as gate insulators. Today, EOT=1.0nm. The EOT limit is 0.7~0.8nm.

One order of magnitude lower is possible by introducing High-k materials and choosing appropriate materials and processes. EOT can be reduced beyond 0.5nm by using direct contact to Si.
High-k/metal gate stack film deposition cluster tool
Gate Leakage vs EOT, (Vg=|1|V)

Current density (A/cm²) vs EOT (nm)

- Al₂O₃
- HfAlO(N)
- HfO₂
- HfSiO(N)
- HfTaO
- La₂O₃
- Nd₂O₃
- Pr₂O₃
- PrSiO
- PrTiO
- SiON/SiN
- Sm₂O₃
- SrTiO₃
- Ta₂O₅
- TiO₂
- ZrO₂(N)
- ZrSiO
- ZrAlO(N)
La$_2$O$_3$ at 300°C process make sub-0.4 nm EOT MOSFET

EOT=0.37nm

EOT=0.37nm

EOT=0.40nm

EOT=0.48nm

0.48 → 0.37nm Increase of $I_d$ at 30%
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small Dit

① silicate-reaction-formed fresh interface

② stress relaxation at interface by glass type structure of La silicate.


Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress
La$_2$O$_3$

No interfacial layer can be confirmed with Si/TiN/W
Electron mobility is comparable to record mobility with Hf-based oxides.

Gate leakage is two orders of magnitude lower than that of ITRS.
<table>
<thead>
<tr>
<th>Gate stack</th>
<th>EOT</th>
<th>Mobility</th>
<th>$V_{th}$</th>
<th>SS</th>
<th>DIBL</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.52</td>
<td>110cm$^2$/Vs (at 1x10$^{13}$cm$^{-2}$)</td>
<td>$\sim$0.4V (L$_g$=24nm)</td>
<td>90mV/dec</td>
<td>147mV/V</td>
<td>IBM VLSI2011</td>
</tr>
<tr>
<td>TiN/Cap/HfO$_2$</td>
<td>0.55</td>
<td>140cm$^2$/Vs (at 1MV/cm)</td>
<td>$\sim$</td>
<td></td>
<td></td>
<td>IBM VLSI2009</td>
</tr>
<tr>
<td>Metal(A)/Cap/HfO$_2$</td>
<td>0.5</td>
<td>110cm$^2$/Vs (at 0.8MV/cm)</td>
<td>0.3V (L$_g$=1um)</td>
<td></td>
<td></td>
<td>IMEC IEDM2009</td>
</tr>
<tr>
<td>Metal/HfO$_2$</td>
<td>0.59</td>
<td>130cm$^2$/Vs (at 1MV/cm)</td>
<td>0.45V (L$_g$=1um)</td>
<td>75mV/dec</td>
<td></td>
<td>Sematech VLSI2009</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.65</td>
<td>$\sim$</td>
<td>0.3$\sim$0.4V (L$_g$=30nm)</td>
<td>90mV/dec</td>
<td>100mV/V</td>
<td>Samsung VLSI2011</td>
</tr>
<tr>
<td>Metal/Hf-based</td>
<td>0.95</td>
<td>$\sim$</td>
<td>$\sim$0.3V (L$_g$=30nm)</td>
<td>100mV/dec</td>
<td>$\sim$200mV/V</td>
<td>Intel IEDM2009</td>
</tr>
<tr>
<td>W/La-silicate</td>
<td>0.62</td>
<td>155cm$^2$/Vs (at 1MV/cm)</td>
<td>$\sim$-0.08V (L$_g$=10um)</td>
<td>$\sim$70mV/dec</td>
<td></td>
<td>Tokyo Tech. T-ED2012</td>
</tr>
</tbody>
</table>
Recent results by my group.
ALD of La2O3


Precursor (ligand)

La(iPrCp)3
La(FAMD)3

1 cycle

ALD is indispensable from the manufacturing viewpoint
- precise control of film thickness and good uniformity
Metal (Silicide) S/D
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- \( V_t \) and \( I_{ON} \) variation
- GIDL

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Surface or interface control

Diffusion species: metal atom (Ni, Co)
- Rough interface at silicide/Si
  - Excess silicide formation
  - Different $\phi_Bn$ presented at interface
  - Process temperature dependent composition

Diffusion species: Si atom (Ti)
- Surface roughness increases
  - Line dependent resistivity change

Annealing: 650 °C
Si(001) sub.  Epitaxial NiSi$_2$


Deposition of Ni-Si mixed films from NiSi₂ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
SEM views of silicide/Si interfaces

Ni source (50nm) vs NiSi₂ source (50nm)

600°C, 1min
- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

700°C, 1min

800°C, 1min

Ni source
- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

NiSi₂ source
- Atomically flat interfaces
- No Si consumption
- Temperature-independent
Ideal characteristics ($n = 1.00$, suppressed leakage current)

Suppressed reverse leakage current

- Flat interface and No Si substrate consumption
- No defects in Si substrate
III-V/Ge Channel
Why high mobility channel materials?
Arming higher performance at lower supply voltage

Both 1) and 2) are important

1) High injection Velocity of carriers $v_{\text{inj}}$
2) High mobility of carriers

Problems: Technologies and Cost
Interfacial properties at the gate insulator/semiconductor
Contact resistance at Source/Drain and semiconductor
Different semiconductors for n- and p- channel FETs

$^47$Integration on Si wafer
## Ge, III-V bulk properties

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>electron mob. (cm^2/Vs)</strong></td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
</tr>
<tr>
<td><strong>electron effective mass (/m(_0))</strong></td>
<td>m(_i): 0.19</td>
<td>m(_i): 0.082</td>
<td>m(_i): 0.067</td>
<td>m(_i): 0.08</td>
<td>m(_i): 0.026</td>
<td>m(_i): 0.0135</td>
</tr>
<tr>
<td><strong>hole mob. (cm^2/Vs)</strong></td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td><strong>hole effective mass (/m(_0))</strong></td>
<td>m(_HH): 0.49</td>
<td>m(_HH): 0.28</td>
<td>m(_HH): 0.45</td>
<td>m(_HH): 0.45</td>
<td>m(_HH): 0.57</td>
<td>m(_HH): 0.44</td>
</tr>
<tr>
<td><strong>band gap (eV)</strong></td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.14</td>
</tr>
<tr>
<td><strong>permittivity</strong></td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

- Ge ⇒ lightest hole \( m^* \) (light electron \( m^* \)) ⇒ pMOS (CMOS)
- III-V ⇒ light electron \( m^* \) ⇒ nMOS
- GaAs·InP ⇒ \( E_g \) higher than that in Si ⇒ low power

*S. Takagi., IEDM2011, Short course (Tokyo Uni)*
Tri-gate structure has superiority electrostatic controllability compared to ultra-thin body planar structure

Steepest SS and smallest DIBL ever reported ($W_{\text{fin}} = 30\text{nm}$)

*M. Radosavljevic, et al. (Intel), IEDM2011, p.765.*
Ge-nanowire pMOSFET (AIST, Tsukuba)


Using Ni-Ge alloy as metal S/D

Significantly reduces contact resistance

High saturation current and high mobility

$\mu_{\text{eff}} = 855 \text{ cm}^2/\text{Vs}$ at $N_s = 5 \times 10^{12} \text{cm}^{-2}$

and saturation drain current of $731 \mu\text{A}/\mu\text{m}$ at $V_d = -1\text{V}$
### III-V/Ge benchmark for various structures

<table>
<thead>
<tr>
<th>Material</th>
<th>Planar (metal S/D, Strain, Buffer...)</th>
<th>FinFET</th>
<th>Tri-gate</th>
<th>Gate-all-around MOSFET</th>
<th>Nanowire</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dielectric/EOT</strong></td>
<td>InGaAs/Ge InGaSn/InGaAs/Ge</td>
<td>InGaAs/Ge</td>
<td>InGaAs/Ge</td>
<td>InGaAs/Ge</td>
<td>InGaAs/Ge</td>
</tr>
<tr>
<td><strong>Mobility</strong></td>
<td>~600 (cm²/Vs)</td>
<td>~700 (μS/μm³)</td>
<td>701 (μS/μm³)</td>
<td>~500 (μS/μm³)</td>
<td>~850 (cm²/Vs)</td>
</tr>
<tr>
<td><strong>Lch (nm)</strong></td>
<td>55</td>
<td>100</td>
<td>60</td>
<td>50</td>
<td>200</td>
</tr>
<tr>
<td><strong>DIBL (mV/V)</strong></td>
<td>84</td>
<td>180</td>
<td>~50</td>
<td>210</td>
<td>-</td>
</tr>
<tr>
<td><strong>SS (mV/dec)</strong></td>
<td>105</td>
<td>145</td>
<td>90</td>
<td>150</td>
<td>160</td>
</tr>
<tr>
<td><strong>ION (µA/µm)</strong></td>
<td>278 (Vd=0.5V)</td>
<td>10 (Vd=0.5V)</td>
<td>235 (Vd=-1V)</td>
<td>180 (Vd=0.5V)</td>
<td>604 (Vd=-0.5V)</td>
</tr>
</tbody>
</table>
Multi-gate III-V and Si benchmark

**nMOS**
- InGaAs GAA: $L_g=50$ nm, Dielectric: 10nm Al$_2$O$_3$, $V_{DS}=0.5$ V (Purdue Univ.) [1]
- Si-FinFET 32nm: Intel $V_{DD}=0.8$ V [10]
- InGaAs Tri-gate: $L_g=60$ nm, EOT 12A, $V_{DS}=0.5$ V (Intel) [2]
- Si-FinFET 22nm: Intel $V_{DD}=0.8$ V [10]
- Si-bulk 45nm: Intel $V_{DD}=1$ V [11]
- InGaAs Nanowire: $L_g=200$ nm, $T_{ox}=14.8$ nm, $V_{DS}=0.5$ V (Hokkaido Univ.) [4]
- Metal S/D InGaAs-OI: $L_{ch}=55$ nm, EOT 3.5nm, $V_{DS}=0.5$ V (Tokyo Uni.) [5]

**pMOS**
- GOI Tri-gate: $L_g=65$ nm, EOT 3.0nm, $V_D=-1$ V (AIST Tsukuba) [6]
- Si-FinFET 32nm: Intel $V_{DD}=0.8$ V [10]
- Si-FinFET 22nm: Intel $V_{DD}=0.8$ V [10]
- Si-bulk 45nm: Intel $V_{DD}=1$ V [11]
- Ge FinFET: $L_g=4.5$ mm, Dielectric: SiON, $V_{DS}=-1$ V (Stanford Univ.) [7]
- Ge GAA: $L_g=300$ nm, dielectric: GeO$_2$(7nm)-HfO$_2$(10nm), $V_D=-0.8$ V (ASTAR Singapore) [8]
- Si-FinFET 32nm: Intel $V_{DD}=0.8$ V [10]
- Ge Tri-gate: $L_g=183$ nm, EOT 5.5nm, $V_D=-1$ V (NNDL Taiwan) [9]

**References**

1. J. J. Gu et al., pp.769, IEDM2011 (Purdue).
4. K. Tomioka et al., pp.773, IEDM2011 (Hokkaido Univ.).
5. S. H. Kim et al., pp.177, VLSI2012 (Tokyo Uni).
8. J. Peng et al., pp.931, IEDM2009 (ASTAR Singapore)
9. S. Hsu et al., pp.825, IEDM2011 (NNDL Taiwan)
10. C. Auth et al., pp.131, VLSI2012 (Intel).
## ITRS 2011 for III-V/Ge

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$ (nm)</td>
<td>14</td>
<td>11.7</td>
<td>9.3</td>
<td>7.4</td>
<td>5.8</td>
</tr>
<tr>
<td>$V_{dd}$ (V)</td>
<td>0.63</td>
<td>0.61</td>
<td>0.58</td>
<td>0.56</td>
<td>0.54</td>
</tr>
<tr>
<td>$EOT$ (nm)</td>
<td>0.68</td>
<td>0.62</td>
<td>0.56</td>
<td>0.50</td>
<td>0.45</td>
</tr>
</tbody>
</table>

### Mobility enhancement factor due to channel material

<table>
<thead>
<tr>
<th>Material</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
</tr>
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<tbody>
<tr>
<td>III-V</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Ge</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$C_g$ Ideal ((fF/\mu m))</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>III-V</td>
<td>0.28</td>
<td>0.24</td>
<td>0.20</td>
<td>0.16</td>
<td>0.13</td>
</tr>
<tr>
<td>Ge</td>
<td>0.41</td>
<td>0.36</td>
<td>0.30</td>
<td>0.25</td>
<td>0.21</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$V_{t,sat}$ (mV)</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>III-V</td>
<td>229</td>
<td>230</td>
<td>238</td>
<td>245</td>
<td>251</td>
</tr>
<tr>
<td>Ge</td>
<td>230</td>
<td>231</td>
<td>241</td>
<td>249</td>
<td>254</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$CV/I$ (ps)</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>III-V</td>
<td>0.13</td>
<td>0.11</td>
<td>0.09</td>
<td>0.07</td>
<td>0.06</td>
</tr>
<tr>
<td>Ge</td>
<td>0.21</td>
<td>0.17</td>
<td>0.13</td>
<td>0.10</td>
<td>0.08</td>
</tr>
</tbody>
</table>

Manufacturing solutions are **NOT** known.
**ITRS 2011 for III-V/Ge, Contd**

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
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<td>$L_g$ (nm)</td>
<td>14</td>
<td>11.7</td>
<td>9.3</td>
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<tr>
<td>$V_{ini}$ ($10^7$ cm/s)</td>
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<tr>
<td>III-V</td>
<td>4.29</td>
<td>4.58</td>
<td>5.32</td>
<td>5.93</td>
<td>6.64</td>
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<tr>
<td>Ge</td>
<td>2.26</td>
<td>2.44</td>
<td>2.86</td>
<td>3.19</td>
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<tr>
<td>$I_{d,sat}$ (mA/µm)</td>
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<tr>
<td>III-V</td>
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<td>2.343</td>
<td>2.523</td>
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<td>Ge</td>
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<td>1.932</td>
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<td>$I_{sd,leak}$ (nA/µm)</td>
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<td>$R_{sd}$ ($Ω$-µm)</td>
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<td>131</td>
<td>113</td>
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<td>Ge</td>
<td>149</td>
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<td>85</td>
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<td>$CV^2$ (fJ/µm)</td>
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<td>0.20</td>
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Manufacturing solutions are **NOT** known
C based materials
Sub-10nm carbon nanotube transistor

A. D. Franklin et al., pp.525, IEDM2011 (IBM)

Transistor operation with $L_{ch}$ of 9nm
Graphene Field-effect Transistor

- Ambipolar Characteristics
- Bi-layer graphene and double gates can open the gap

- $I_{off}$ is very large  No bandgap
Conclusions

Si-MOSFET is the most fundamental and smallest functional device available for manufacturing.

In order to keep the scaling of MOSFETs, aggressive introduction of new materials is inevitable.
Thank you for your attention!