Evolution of Si CMOS Technologies to Sub-10 nm Generation

10:10-10:40, June 4, 2012

Electron Devices Colloquium
– Imec, Leuven, Belgium

Hiroshi Iwai,
Tokyo Institute of Technology
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

Drain
Al Gate

Si/SiO₂ Interface is extraordinarily good

Al
SiO₂
Si
1970,71: 1st generation of LSIs

DRAM   Intel 1103

MPU    Intel 4004
2012

Most recent SD Card

Lexar Professional

128 GB
133x Speed
Most Recent SD Card

128GB (Bite)
= 128G X 8bit = 1024Gbit
= 1.024T(Tera)bit

1T = 10^{12} = 1Trillion

World Population : 7 Billion
Brain Cell : 10〜100 Billion
Stars in Galaxy : 100 Billion
Most Recent SD Card

Lexar Professional

128GB
133x Speed

> 

Galaxy Image
128 GB = 1Tbit

2.4cm X 3.2cm X 0.21cm

Volume : 1.6cm³  Weight 2g

Voltage 2.7 - 3.6V

Old Vacuum Tube:
5cm X 5cm X 10cm, 100g, 100W

What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube: 5cm X 5cm X 10cm

1Tbit = 10,000 X 10,000 X 10,000 bit

Volume = (5cm X 10,000) X (5cm X 10,000) X (10cm X 10,000)
= 0.5km X 0.5km X 1km

Pingan International Finance Center
Shanghai, China (Year 2016)

Indian Tower
Mumbai, India (Year 2016)

Burj Khalifa
Dubai, UAE (Year 2010)
Old Vacuum Tube: 100W

1Tbit = $10^{12}$bit

Power = $0.1 \text{kW} \times 10^{12} = 50 \text{ TW}$

Nuclear Power Generator

1MkW = 1BW

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving.
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years!!

313 billion dollar (US) in 2011

1,528 billion dollar (US) in 2025

By K. Kim, CSTIC 2012
In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. **Reduce Capacitance**
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. **Increase number of Transistors**
   - Parallel processing
     - Increase circuit operation speed

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.
Feature Size/Technology Node

(1970) 10 µm → 8 µm → 6 µm → 4 µm → 3 µm → 2µm → 1.2 µm →

0.8 µm → 0.5 µm → 0.35 µm → 0.25 µm → 180 nm → 130 nm → 90 nm →

65 nm → 45 nm → 32 nm → 22 nm (2012)

Averaged downsizing rate (in the past 42 years): ~ 0.7X every 3 years

Total reduction in 19 generations: Gate Length ~ 1/500, Area ~ 1/250,000
$t_{ox}$ and $V_{dd}$ have to be decreased for better channel potential control $\rightarrow I_{OFF}$ Suppression
What would be the limit of downsizing!

Tunneling distance

Source

Channel

Drain

3 nm
Subthreshold leakage current will limit the downsizing
The limit is different depending on application.

HP CMOS (high Performance)
- Highest Ion, Lowest CV/I
- High leakage
- Medium Vdd

LOP CMOS (Low Operation Power)
- Lowest Vdd
- Medium Ion, medium CV/I
- Medium leakage

LSTP CMOS (Low Standby Power)
- Lowest leakage
- Low Ion, high CV/I
- High Vdd

Source: 2007 ITRS Winter Public Conf.
The down scaling of MOSFETs is still possible for at least another 10 years!

4 important technological items for down scaling.

New materials
1. Thinning of high-k gate oxide thickness beyond 0.5 nm
2. Metal(Silicide) S/D
3. III-V/Ge channel

New structures
4. Wire channel
1. High-k beyond 0.5 nm
Issues in high-k/metal gate stack

- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
- Suppression of metal diffusion
- Suppression of oxygen vacancy formation
- Small interfacial state density at high-k/Si
- Control of interface reaction and Si diffusion to high-k
- Flat metal/high-k interface for better mobility
- Suppression of gate leakage current
- Endurance for high temperature process
- Oxygen diffusion control for prevention of EOT increase and oxygen vacancy formation in high-k
- Workfunction engineering for $V_{th}$ control
- Interface dipole control for $V_{th}$ tuning
- Suppression of FLP
- Remove contamination introduced by CVD
- Thinning or removal of SiO$_2$-IL for small EOT
- Reliability: PBTI, NBTI, TDDB
- Oxygen concentration control for prevention of EOT increase and oxygen vacancy formation in high-k
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band offset

Oxide

Si

Band Discontinuity [eV]

Dielectric Constant $\varepsilon(0)$

XPS measurement by Prof. T. Hattori, INFOS 2003
### Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
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<td>La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer</td>
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</table>

### Unstable at Si interface
- Si + MOₓ M + SiO₂
- Si + MOₓ MSiₓ + SiO₂
- Si + MOₓ M + MSiₓOᵧ

### Choice of High-k elements for oxide

- HfO₂ based dielectrics are selected as the first generation materials, because of their merit in
  1) band-offset,
  2) dielectric constant
  3) thermal stability

- La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

---

R. Hauser, IEDM Short Course, 1999
Direct high-k/Si by silicate reaction

HfO₂ case

Low $P_{O2}$ → High $P_{O2}$

La₂O₃ case

Low $P_{O2}$ → High $P_{O2}$

Our approach

Direct contact can be achieved with La₂O₃ by forming silicate at interface. Control of oxygen partial pressure is the key for processing.

K. Kakushima, et al., VLSI2010, p.69
**SiO$_x$-IL growth at HfO$_2$/Si Interface**

**XPS Si1s spectrum**

- Binding energy (eV)
- Intensity (a.u)

- Si sub.
- Hf Silicate
- SiO$_2$

**Phase separator**

\[
\text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2
\]

H. Shimizu, JJAP, 44, pp. 6131

**TEM image 500 oC 30min**

- W
- HfO$_2$ $k=16$
- SiO$_x$-IL $k=4$
- 1 nm

SiO$_x$-IL is formed after annealing

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Trans. ECS 11, 319

Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La\textsubscript{2}O\textsubscript{3}/Si

Direct contact high-k/Si is possible

La\textsubscript{2}O\textsubscript{3} can achieve direct contact of high-k/Si
High-k gate insulator MOSFETs for Intel: EOT=1nm

HfO$_2$ based high-k
For the past 45 years, SiO\textsubscript{2} and SiON have been used as gate insulators. Today, EOT=1.0 nm. The EOT limit is 0.7~0.8 nm. One order of magnitude reduction is possible. EOT can be reduced further beyond 0.5 nm by using direct contact to Si. This is achieved by choosing appropriate materials and processes.
High-k/metal gate stack film deposition cluster tool

- Deposited thin film
- Substrate
- Moving Mask
- Flux
- Source
- Electron Beam
- Sputter
- EB Evaporation
- Flash Lamp
- Anneal
- ALD
- RTA
- Robot
- Entrance
Gate Leakage vs EOT, (Vg=|1|V)

- Al2O3
- HfAlO(N)
- HfO2
- HfSiO(N)
- HfTaO
- La2O3
- Nd2O3
- Pr2O3
- PrSiO
- PrTiO
- SiON/SiN
- Sm2O3
- SrTiO3
- Ta2O5
- TiO2
- ZrO2(N)
- ZrSiO
- ZrAlO(N)
La$_2$O$_3$ at 300° C process make sub-0.4 nm EOT MOSFET

EOT = 0.37 nm

EOT = 0.37 nm  EOT = 0.40 nm  EOT = 0.48 nm

0.48 → 0.37 nm Increase of Id at 30%
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small $D_{it}$

- silicate-reaction-formed fresh interface
- stress relaxation at interface by glass type structure of La silicate.

$\text{La}_2\text{O}_3$ La-silicate

La-O-Si bonding

SiO$_4$ tetrahedron network

Fresh interface with silicate reaction

FGA$800^\circ$C is necessary to reduce the interfacial stress

---


No interfacial layer can be confirmed with Si/TiN/W
Benchmark of La-silicate dielectrics


Gate leakage is two orders of magnitude lower than that of ITRS.

Electron mobility is comparable to record mobility with Hf-based oxides.

ALD of La$_2$O$_3$

Precursor (ligand)

La(iPrCp)$_3$

La(FAMD)$_3$

ALD is indispensable from the manufacturing viewpoint
- precise control of film thickness and good uniformity
Why high mobility channel materials?

Arming higher performance at lower supply voltage

Both 1) and 2) are important

1) High injection velocity of carriers

2) High mobility of carriers

Problems: Technologies and Cost

- Interfacial properties at the gate insulator/semiconductor
- Contact resistance at Source/Drain and semiconductor
- Different semiconductors for n- and p-channel FETs
- Integration on Si wafer
### High mobility channel materials


<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
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</thead>
<tbody>
<tr>
<td>electron mob. (cm²/Vs)</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
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<td>electron effective mass (/m₀)</td>
<td>mᵣ: 0.19</td>
<td>mᵣ: 0.082</td>
<td>0.067</td>
<td>0.082</td>
<td>0.023</td>
<td>0.014</td>
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<tr>
<td></td>
<td>mᵢ: 0.916</td>
<td>mᵢ: 1.467</td>
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<td></td>
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<tr>
<td>hole mob. (cm²/Vs)</td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
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<tr>
<td>hole effective mass (/m₀)</td>
<td>mₜH: 0.49</td>
<td>mₜH: 0.28</td>
<td>mₜH: 0.45</td>
<td>mₜH: 0.45</td>
<td>mₜH: 0.57</td>
<td>mₜH: 0.44</td>
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<td></td>
<td>mₜL: 0.16</td>
<td>mₜL: 0.044</td>
<td>mₜL: 0.082</td>
<td>mₜL: 0.12</td>
<td>mₜL: 0.35</td>
<td>mₜL: 0.016</td>
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<td>band gap (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.17</td>
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<tr>
<td>permittivity</td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
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</table>

Better carrier transport

Higher drive current at low power supply
### ITRS 2011 for Si (HP: High Performance Logic)

*1: Thicker EOT for MG (Multiple gate: Fin/Tri gate, nanowire)

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2012</th>
<th>2014</th>
<th>2016</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
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<tbody>
<tr>
<td>( L_g ) (nm)</td>
<td>22</td>
<td>18</td>
<td>15.3</td>
<td>12.8</td>
<td>10.6</td>
<td>8.9</td>
<td>7.4</td>
<td>5.9</td>
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<tr>
<td>( V_{dd} ) (V)</td>
<td>0.87</td>
<td>0.82</td>
<td>0.77</td>
<td>0.73</td>
<td>0.68</td>
<td>0.64</td>
<td>0.61</td>
<td>0.57</td>
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<td>( EOT ) (nm)</td>
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<td>( C_g ) Ideal ((fF/\mu m))</td>
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<td>( V_{t,sat} ) (mV)</td>
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<td>( CV/I ) (ps)</td>
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#### Mobile enhancement factor due to strain

- Bulk: 0.84
- FD SOI: 0.8
- MG: 0.76
- Thicker EOT for MG (Multiple gate: Fin/Tri gate, nanowire)

<table>
<thead>
<tr>
<th>( C_g ) Ideal ((fF/\mu m))</th>
<th>Bulk</th>
<th>FD SOI</th>
<th>MG</th>
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<td>( V_{t,sat} ) (mV)</td>
<td>Bulk</td>
<td>FD SOI</td>
<td>MG</td>
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<tr>
<td>( CV/I ) (ps)</td>
<td>Bulk</td>
<td>FD SOI</td>
<td>MG</td>
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- Manufacturing solutions exist or is being optimized
- Manufacturing solutions are known
- Manufacturing solutions are **NOT** known

<table>
<thead>
<tr>
<th>Year</th>
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- Thicker EOT for MG (Multiple gate: Fin/Tri gate, nanowire)
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<td>( \text{Equivalent Injection velocity} \ V_{\text{inj}} (10^7 \text{ cm/s}) )</td>
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<td>Bulk</td>
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<td>( I_{d,\text{sat}} ) (mA/( \mu )m)</td>
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<tr>
<td>Bulk</td>
<td>232</td>
<td>183</td>
<td>149</td>
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<tr>
<td>FD SOI</td>
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<td>228</td>
<td>187</td>
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<tr>
<td>MG</td>
<td>257</td>
<td>218</td>
<td>186</td>
<td>160</td>
<td>133</td>
<td>104</td>
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<tr>
<td>( CV^2 ) (fJ/( \mu )m)</td>
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<tr>
<td>MG</td>
<td>0.38</td>
<td>0.31</td>
<td>0.25</td>
<td>0.21</td>
<td>0.17</td>
<td>0.14</td>
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</tr>
</tbody>
</table>

**Manufacturing solutions exist or is being optimized**

**Manufacturing solutions are known**

**Manufacturing solutions are NOT known**
<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2024</th>
<th>2026</th>
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<tbody>
<tr>
<td>$L_g$ (nm)</td>
<td>14</td>
<td>11.7</td>
<td>9.3</td>
<td>7.4</td>
<td>5.8</td>
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<tr>
<td>$V_{dd}$ (V)</td>
<td>0.63</td>
<td>0.61</td>
<td>0.58</td>
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<tr>
<td>EOT (nm)</td>
<td>0.68</td>
<td>0.62</td>
<td>0.56</td>
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<td>Mobility enhancement factor due to channel material</td>
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<tr>
<td>III-V</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
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</tr>
<tr>
<td>Ge</td>
<td>4</td>
<td>4</td>
<td>4</td>
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<tr>
<td>$C_{g Ideal}$ (fF/µm)</td>
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<tr>
<td>III-V</td>
<td>0.28</td>
<td>0.24</td>
<td>0.20</td>
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<tr>
<td>Ge</td>
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<td>0.30</td>
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<tr>
<td>$V_{t, sat}$ (mV)</td>
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<td>230</td>
<td>238</td>
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</tr>
<tr>
<td>Ge</td>
<td>230</td>
<td>231</td>
<td>241</td>
<td>249</td>
<td>254</td>
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<tr>
<td>CV/I (ps)</td>
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<td>0.11</td>
<td>0.09</td>
<td>0.07</td>
<td>0.06</td>
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<td>Ge</td>
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<td>0.17</td>
<td>0.13</td>
<td>0.10</td>
<td>0.08</td>
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</table>

Manufacturing solutions are **NOT** known
### Year of Production

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2018</th>
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<td>$L_g \ (nm)$</td>
<td>14</td>
<td>11.7</td>
<td>9.3</td>
<td>7.4</td>
<td>5.8</td>
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<tr>
<td>Equivalent Injection velocity $V_{inj} \ (10^7 \ cm/s)$</td>
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<tr>
<td>III-V</td>
<td>4.29</td>
<td>4.58</td>
<td>5.32</td>
<td>5.93</td>
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<tr>
<td>$I_{d,\text{sat}} \ (mA/\mu m)$</td>
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<tr>
<td>III-V</td>
<td>2.200</td>
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<td>2.555</td>
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<td>$I_{sd,\text{leak}} \ (nA/\mu m)$</td>
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</tr>
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<td>100</td>
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<td>100</td>
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<td>100</td>
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<tr>
<td>$R_{sd} \ (\square \ - \mu m)$</td>
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<tr>
<td>III-V</td>
<td>131</td>
<td>113</td>
<td>96</td>
<td>82</td>
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<tr>
<td>Ge</td>
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<td>$CV^2 \ (fJ/\mu m)$</td>
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</tr>
</tbody>
</table>

Manufacturing solutions are **NOT** known.
However, high-temperature anneal is necessary for the good interfacial property

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Metal (Silicide) S/D
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- \(V_t\) and \(I_{ON}\) variation
- GIDL

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
**Surface or interface control**

**Diffusion species:**
- **metal atom** (Ni, Co)

Rough interface at silicide/Si
- Excess silicide formation
- Different $\phi_B$ presented at interface
- Process temperature dependent composition

**Diffusion species:** **Si atom** (Ti)

Surface roughness increases
- Line dependent resistivity change

Annealing: 650 °C
Si(001) sub.  Epitaxial NiSi$_2$

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CoSi$_2$  NiSi  TiSi$_2$

Top view

Line width of 0.1 µm

Aglomeration

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Deposition of Ni film

Deposition from NiSi$_2$ source

Deposition of Ni-Si mixed films from NiSi$_2$ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
SEM views of silicide/Si interfaces

Ni source (50nm) and NiSi$_2$ source (50nm) with different annealing temperatures:

- **600°C, 1min:**
  - Rough interfaces
  - Consumed Si substrate
  - Thickness increase ~100 nm

- **700°C, 1min:**

- **800°C, 1min:**

Ni source:
- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

NiSi$_2$ source:
- Atomically flat interfaces
- No Si consumption
- Temperature-independent
Ideal characteristics ($n = 1.00$, suppressed leakage current)

**Suppressed reverse leakage current**

- Flat interface and No Si substrate consumption
- No defects in Si substrate
Wire channel
Suppression of subthreshold leakage by surrounding gate structure
Because of off-leakage control, 
Planar $\rightarrow$ Fin $\rightarrow$ Nanowire
Nanowire structures in a wide meaning

Fin

Tri-gate

Ω-gate

All-around
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process

2. Good controllability of $I_{\text{OFF}}$

3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
By Profs. Oshiyama and Iwata, U. of Tokyo
Compact model for circuit designer is very important

Prof. K. Natori of TIT
チャネル内の電子散乱導入の考え方

\[ T(\varepsilon) = \frac{(F(0) - G(0))}{F(0)} \]

\[ I_D = \frac{q}{\pi \hbar} \sum_i \int [f(E, \mu_S) - f(E, \mu_D)] T_i(E) dE \]

Prof. K. Natori of TIT
散乱の導入に係る計算式

弾性散乱域

\[ \sqrt{\frac{2}{m}(qEx+\varepsilon)} \frac{dF(x)}{dx} + \frac{B_0}{\sqrt{qEx+\varepsilon}} \{F(x) - G(x)\} = 0 \]

\[ -\sqrt{\frac{2}{m}(qEx+\varepsilon)} \frac{dG(x)}{dx} + \frac{B_0}{\sqrt{qEx+\varepsilon}} \{G(x) - F(x)\} = 0 \]

光学フォノン放出域

\[ \sqrt{\frac{2}{m}(qEx+\varepsilon)} \frac{dF(x)}{dx} + \frac{B_0}{\sqrt{qEx+\varepsilon}} \{F(x) - G(x)\} + \frac{2D_0}{\sqrt{qEx+\varepsilon - \varepsilon^*}} F(x) = 0 \]

\[ -\sqrt{\frac{2}{m}(qEx+\varepsilon)} \frac{dG(x)}{dx} + \frac{B_0}{\sqrt{qEx+\varepsilon}} \{G(x) - F(x)\} + \frac{2D_0}{\sqrt{qEx+\varepsilon - \varepsilon^*}} G(x) = 0 \]

ソースからドレインへの透過確率 (エネルギー ε に対して)

\[ T(\varepsilon) = \frac{\sqrt{2D_0 qE}}{\left(\sqrt{B_0 + D_0} + \sqrt{D_0}\right) qE + \sqrt{2mD_0 B_0} \ln \left(\frac{qEx_0 + \varepsilon}{\varepsilon}\right)} \]
Prof. K. Natori of TIT
$V_g - V_{th} = 1V$

Experiment
Quasi ballistic

$V_g - V_{th} = 1V$

$0.2V$

$0.4V$

$0.6V$

$0.8V$
Device fabrication

Si/Si$_{0.8}$Ge$_{0.2}$ superlattice epitaxy on SOI

Anisotropic etching of these layers

Isotropic etching of SiGe

The NW diameter is controllable down to 5 nm by self limited oxidation.

Gate depositions

S/D implantation

Spacers formation

Activation anneal

Salicidation

Process Details:
C. Dupre et al., IEDM Tech. Dig., p.749, 2008
3D-stacked Si NWs with Hi-κ/MG

Wire direction : <110>
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT ~2.6 nm

C. Dupre et al.,
SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oxide etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

Standard recipe for gate stack formation
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off $>10^6$, 60 μA/wire

$L_g=65\text{nm}$, $T_{ox}=3\text{nm}$
Bench Mark

V_{DD}: 1.0~1.5 V

 Gate Length (nm) vs. I_{ON} (µA / wire)

- nMOS
- pMOS

Our Work
This work

Planer FET
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

Si nanowire FET
Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240
Electron Density (x10^{19}\text{cm}^{-3})

Distance from SiNW Surface (nm)

Edge portion

Flat portion

Electron density: Log |\psi| (cm^{-3})

(a) Metal

12 nm

19 nm

SiO_2

44 %

V_g = 1 V

(b) Inversion areal ratio: 29 %

12 nm

39 nm
Primitive estimation!

- Compact model
- Small EOT for high-k (33)
- P-MOS improvement (26)
- Low S/D resistance (20)
- # of wires /1μm (15)
- SiNW (12nm ⊕ 19nm)

Assumption:

\[ I_{ON} \propto L_g^{-0.5} T_{ox}^{-1} \]

Graph shows the evolution of \( I_{ON} \) (mA/μm) over the years.

- Bulk
- FD
- ITRS
- MG
Conclusions

MOSFET is the most fundamental and smallest functional device available for manufacturing.

It is really amazing to keep the evolution for so many generations without being replaced by any other device.
The device downsizing of MOSFET will be ended within 10 - 20 years because many of the device parameters are now approaching the physical and manufacturing limits.

Even after the end of MOSFET downsizing, CMOS technology will still be the mainstream IC technology for a long period, as no other device technology can be developed into a comparable integration scale as the present CMOS technology in foreseeable future.
Thank you for your attention!