Past and Future of Micro/Nano-Electronic Devices

April 30, 2012

IEEE EDS Distinguished Lecture

@NIT Manipur, Imphal, India

Hiroshi Iwai,
Tokyo Institute of Technology
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
Institute Overview

Established in 1881 → 130th anniversary in 2011
3 undergraduate schools
   School of Science, School of Engineering, School of Bioscience and Biotechnology
7 graduate schools
   Science and Engineering Science, Science and Engineering Technology,
   Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
   Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

<table>
<thead>
<tr>
<th></th>
<th>Undergraduate</th>
<th>Graduate</th>
<th>Master's</th>
<th>Doctoral</th>
<th>Teaching Staff</th>
<th>Student/Instructor</th>
<th>Staff</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tokyo Inst.</td>
<td>5,000</td>
<td>5,000</td>
<td>3,500</td>
<td>1,500</td>
<td>1,200</td>
<td>8.3</td>
<td>550</td>
</tr>
<tr>
<td>Per Year</td>
<td>1,200</td>
<td>1,800</td>
<td>500</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Asia 847
Europe 78
Africa 16
North America 12
South America 24
Oceania 5

Total 982
(As of May. 1, 2005)
东工大综合理工学研究科

先端ナノエレクトロニクス研究コアユニット

教育

教育

Research

Research

Producing world-leading scientists and engineers who contribute to manufacturing technology.

Industry

University

Industrial world

Universities/independent administrative institutions

海外大学（アジア諸国など）

Overseas universities (such as Asian countries)

連携

Collaboration

国際

International

ナノ電子デバイス

Education and research center

産業界

産業界

World-leading research in ultralow power consumption, ultralow voltage operation, and ultrahigh performance electronic devices.

Energy saving, prevention of global warming and realization of a safe and secure society.

学部生

Graduates

(3 persons)

修士学生

Graduate students

(26 persons)

博士研究員

Researchers

(19 persons)

技術員

Engineers

(1 persons)

教員

Faculties

(10 persons)
研究風景
Cluster tool for high-k thin film deposition

- Preparation Room
- Sputter for metal 5 different target
- E-Beam Evaporation 8 different target
- Robot room
- Flash Lamp
- Anneal
- Micro to mille-seconds
• There were many inventions in the 20th century: Airplane, Nuclear Power generation, Computer, Space aircraft, etc
• However, everything has to be controlled by electronics
• Electronics
  Most important invention in the 20th century
• What is Electronics: To use electrons, Electronic Circuits
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Cathode (heated)  Grid  Anode (Positive bias)

Same mechanism as that of transistor
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power consumption
J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928
Capacitor structure with notch

Negative bias

No current

Positive bias

Current flows

Gate Electrode

Gate Insulator

Semiconductor

Electron

Electric field
Source

Channel

Drain

Gate electrode

Gate Oxid

Surface Potential (Negative direction)

0V

N⁺-Si

P-Si

1V

N-Si

Source

Channel

Drain

0 bias for gate

Positive bias for gate

Electron flow
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator

Drain Current was several orders of magnitude smaller than expected

Even Shockley!
However, they found amplification phenomenon when investigating Ge surface when putting needles. This is the 1st Transistor: 

*Not Field Effect Transistor, But Bipolar Transistor (another mechanism)*

1947: 1st transistor

Bipolar using Ge

J. Bardeen  
W. Shockley  
W. Bratten,
1958: 1st Integrated Circuit

Connect 2 bipolar transistors in the Same substrate by bonding wire.
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

Drain

Al Gate

Si/SiO₂ Interface is extraordinarily good

Al
SiO₂
Si
1970, 71: 1st generation of LSIs

DRAM   Intel 1103

MPU    Intel 4004
2011
Most recent SD Card

Lexar Professional
128GB
133x Speed
Most Recent SD Card

128GB (Bite)  
= 128G X 8bit = 1024Gbit  
= 1.024T(Tera)bit

1T = 10^{12} = 1Trillion

World Population :7 Billion  
Brain Cell :10〜100 Billion  
Stars in Galaxy :100 Billion
Most Recent SD Card
128 GB = 1Tbit

2.4cm X 3.2cm X 0.21cm

Volume :1. 6cm³ Weight 2g

Voltage 2.7 - 3.6V

Old Vacuum Tube :
5cm X 5cm X 10cm, 100g, 100W

What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube:
5cm × 5cm × 10cm

1Tbit = 10,000 × 10,000 × 10,000 bit

Volume = (5cm × 10,000) × (5cm × 10,000) × (5cm × 10,000)
= 0.5km × 0.5km × 1km

Pingan International Finance Center
Shanghai, China (Year 2016)

Indian Tower
Mumbai, India (Year 2016)

Burj Khalifa
Dubai, UAE (Year 2010)

500 m

1,000 m
Old Vacuum Tube: 100W

1 Tbit = $10^{12}$ bit

Power = 0.1 kW x $10^{12}$ = 50 TW

Nuclear Power Generator: 1 MkW = 1 BW

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55 BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
MOS LSI experienced continuous progress for many years.

<table>
<thead>
<tr>
<th>Name of Integrated Circuits</th>
<th>Number of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>1960s IC (Integrated Circuits)</td>
<td>~10</td>
</tr>
<tr>
<td>1970s LSI (Large Scale Integrated Circuit)</td>
<td>~1,000</td>
</tr>
<tr>
<td>1980s VLSI (Very Large Scale IC)</td>
<td>~10,000</td>
</tr>
<tr>
<td>1990s ULSI (Ultra Large Scale IC)</td>
<td>~1,000,000</td>
</tr>
<tr>
<td>2000s ?LSI (? Large Scale IC)</td>
<td>~1,000,000,000</td>
</tr>
</tbody>
</table>
MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Use Gate Field Effect for switching

N-MOS (N-type MOSFET)
N-MOS (N-type MOSFET)

Source

p-Si

n-Si

Electron flow

Gate

n-Si

p-Si

Current flow

Drain

P-MOS (P-type MOSFET)

Source

p-Si

n-Si

Hole flow

Gate

p-Si

n-Si

Current flow

Drain
CMOS

Complimentary MOS

Inverter

PMOS

NMOS

When NMOS is ON, PMOS is OFF
When PMOS is ON, NMOS is OFF
CMOS Technology: Indispensable for our human society

All the human activities are controlled by CMOS

- living, production, financing, telecommunication,
- transportation, medical care, education,
- entertainment, etc.

Without CMOS:
- There is no computer in banks, and
- world economical activities immediately stop.

Cellarer phone dose not exists
Downsizing of the components has been the driving force for circuit evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Vacuum Tube</th>
<th>Transistor</th>
<th>IC</th>
<th>LSI</th>
<th>ULSI</th>
</tr>
</thead>
<tbody>
<tr>
<td>1900</td>
<td>10 cm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1950</td>
<td>cm</td>
<td>10 cm</td>
<td>mm</td>
<td>10 μm</td>
<td>100 nm</td>
</tr>
<tr>
<td>1960</td>
<td>mm</td>
<td>10-3m</td>
<td></td>
<td>10-5m</td>
<td>10-7m</td>
</tr>
<tr>
<td>1970</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. **Reduce Capacitance**
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. **Increase number of Transistors**
   - Parallel processing
     - Increase circuit operation speed

Thus, downsizing of Si devices is the most important and critical issue.
Why $t_{ox}$ thinning

$t_{ox}$ and $V_{dd}$ have to be decreased for better channel potential control $\rightarrow I_{OFF}$ Suppression

Region governed by gate bias

Region governed by drain bias

Gate oxide

Gate metal

Source

Drain

Channel

Substrate

$0V < V_{dep} < 1V$

$0V < V_{dep} < 1V$

No $t_{ox}$ thinning

Large $I_{OFF}$

Large $I_{OFF}$

DL touch with S Region (DL)

$V_{dd}$

$0.5V$
Scaling Method: by R. Dennard in 1974

**Wdep**: Space Charge Region (or Depletion Region) Width

- Wdep has to be suppressed
- Otherwise, large leakage between S and D

K = 0.7 for example

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

Good scaled I-V characteristics

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.
### Downscaling merit: Beautiful!

<table>
<thead>
<tr>
<th>Geometry &amp; Supply voltage</th>
<th>( L_g, W_g, T_{ox}, V_{dd} )</th>
<th>( K )</th>
<th>[ \text{Scaling} \quad K : \quad K=0.7 \text{ for example} ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive current in saturation</td>
<td>( I_d )</td>
<td>( K )</td>
<td>[ I_d = v_{sat} W_g C_o \left(V_g - V_{th}\right) ]</td>
</tr>
<tr>
<td></td>
<td>( I_d / \mu m )</td>
<td>1</td>
<td>[ C_o : \text{gate } C \text{ per unit area} ]</td>
</tr>
<tr>
<td></td>
<td>[ \rightarrow W_g \left(t_{ox}^{-1}(V_g - V_{th})\right) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K=K ]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_d ) per unit ( W_g )</td>
<td>( I_d / W_g )</td>
<td>( 1 )</td>
<td>[ I_d \text{ per unit } W_g = I_d / W_g = 1 ]</td>
</tr>
<tr>
<td>Gate capacitance</td>
<td>( C_g )</td>
<td>( K )</td>
<td>[ C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox} ]</td>
</tr>
<tr>
<td></td>
<td>[ \rightarrow KK/K = K ]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching speed</td>
<td>( \tau )</td>
<td>( K )</td>
<td>[ \tau = C_g V_{dd} / I_d ]</td>
</tr>
<tr>
<td></td>
<td>[ \rightarrow KK/K = K ]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock frequency</td>
<td>( f )</td>
<td>( 1/K )</td>
<td>[ f = 1/\tau = 1/K ]</td>
</tr>
<tr>
<td>Chip area</td>
<td>( A_{chip} )</td>
<td>( \alpha )</td>
<td>[ \alpha : \text{Scaling factor} ]</td>
</tr>
<tr>
<td></td>
<td>[ \rightarrow \text{In the past, } \alpha &gt; 1 \text{ for most cases} ]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integration (# of Tr)</td>
<td>( N )</td>
<td>( \alpha / K^2 )</td>
<td>[ N \rightarrow \alpha / K^2 = 1/K^2, \text{ when } \alpha=1 ]</td>
</tr>
<tr>
<td>Power per chip</td>
<td>( P )</td>
<td>( \alpha )</td>
<td>[ fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha = 1, \text{ when } \alpha=1 ]</td>
</tr>
<tr>
<td></td>
<td>$k = 0.7$ and $\alpha = 1$</td>
<td>$k = 0.7^2 = 0.5$ and $\alpha = 1$</td>
<td></td>
</tr>
<tr>
<td>--------------------------</td>
<td>-----------------------------</td>
<td>--------------------------------------</td>
<td></td>
</tr>
<tr>
<td><strong>Single MOFET</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>$0.7$</td>
<td>$0.5$</td>
<td></td>
</tr>
<tr>
<td>$L_g$</td>
<td>$0.7$</td>
<td>$0.5$</td>
<td></td>
</tr>
<tr>
<td>$I_d$</td>
<td>$0.7$</td>
<td>$0.5$</td>
<td></td>
</tr>
<tr>
<td>$C_g$</td>
<td>$0.7$</td>
<td>$0.5$</td>
<td></td>
</tr>
<tr>
<td>$P$ (Power)/Clock</td>
<td>$0.7^3 = 0.34$</td>
<td>$0.5^3 = 0.125$</td>
<td></td>
</tr>
<tr>
<td>$\tau$ (Switching time)</td>
<td>$0.7$</td>
<td>$0.5$</td>
<td></td>
</tr>
<tr>
<td><strong>Chip</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$N$ (# of Tr)</td>
<td>$1/0.7^2 = 2$</td>
<td>$1/0.5^2 = 4$</td>
<td></td>
</tr>
<tr>
<td>$f$ (Clock)</td>
<td>$1/0.7 = 1.4$</td>
<td>$1/0.5 = 2$</td>
<td></td>
</tr>
<tr>
<td>$P$ (Power)</td>
<td>$1$</td>
<td>$1$</td>
<td></td>
</tr>
</tbody>
</table>
Actual past downscaling trend until year 2000

Change in 30 years

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ideal scaling</th>
<th>Real Change</th>
<th>Ideal scaling</th>
<th>Real Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_g )</td>
<td>( K ) ( \times 10^{-2} )</td>
<td>( 10^{-2} )</td>
<td>( I_d/\mu m )</td>
<td>( K \times 10^{-2} )</td>
</tr>
<tr>
<td>( t_{ox} )</td>
<td>( K \times 10^{-2} )</td>
<td>( 10^{-2} )</td>
<td>( I_d/\mu m )</td>
<td>( 1 )</td>
</tr>
<tr>
<td>( V_{dd} )</td>
<td>( K \times 10^{-2} )</td>
<td>( 10^{-1} )</td>
<td>( N )</td>
<td>( \alpha/K^2 \times 10^5 )</td>
</tr>
<tr>
<td>( A_{chip} )</td>
<td>( \alpha )</td>
<td>( 10^1 )</td>
<td>( P )</td>
<td>( \alpha \times 10^1 )</td>
</tr>
</tbody>
</table>

Vd scaling insufficient, \( \alpha \) increased \( \implies \) N, \( I_d \), f, P increased significantly

Past 30 years scaling

Merit: N, f increase
Demerit: P increase

V\(_{dd}\) scaling insufficient
Additional significant increase in \( I_d, f, P \)

Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1μm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5μm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25μm:</td>
<td>Direct-tunneling of gate SiO₂</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1μm:</td>
<td>‘0.1μm brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
Historically, many predictions of the limit of downsizing. VLSI text book written 1979 predict that 0.25 micrometer would be the limit because of direct-tunneling current through the very thin-gate oxide.
Finally, there appears to be a fundamental limit of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide begin to make the devices of smaller dimension unworkable.
Direct-tunneling effect

Potential Barrier

Wave function

Direct tunneling current

Direct tunneling leakage current start to flow when the thickness is 3 nm.
Direct tunneling leakage was found to be OK! In 1994!
Gate leakage: $I_g \propto \text{Gate Area} \propto \text{Gate length (Lg)}$

Drain current: $I_d \propto 1/\text{Gate length (Lg)}$

$Lg \rightarrow$ small,

Then, $I_g \rightarrow$ small, $I_d \rightarrow$ large, Thus, $I_g/I_d \rightarrow$ very small
Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!

Some one will think for you
Transistor Scaling Continues

Qi Xinag, ECS 2004, AMD
Downsizing limit?

Channel length?

10 nm

Electron wave length

Gate Oxd

Channel
5 nm gate length CMOS
Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC
IEDM, 2003
Electron wave length: 10 nm

Tunneling distance: 3 nm

Downsizing limit:
Channel length
Gate oxide thickness

Diagram showing a simplified view of a transistor with dimensions and labels.
Prediction now!

Electron wave length
10 nm

Tunneling distance
3 nm

Atom distance
0.3 nm

MOSFET operation
Lg = 2 ~ 1.5 nm?

Below this, no one knows future!
However, Gate oxide thickness 2 orders magnitude smaller Close to limitation!!

Lg: Gate length downsizing will continue to another 10-15 years
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
So, we are now in the limitation of downsizing?

Do you believe this or do not?
To use high-k dielectrics

**K: Dielectric Constant**

<table>
<thead>
<tr>
<th>Thin $\text{SiO}_2$</th>
<th>Thick high-k dielectrics</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K=4$</td>
<td>$K=20$</td>
</tr>
<tr>
<td>Almost the same electric characteristics</td>
<td>5 times thicker</td>
</tr>
<tr>
<td>Small leakage Current</td>
<td></td>
</tr>
</tbody>
</table>

However, very difficult and big challenge!
### Choice of High-k elements for oxide

#### Candidates

- **Unstable at Si interface**
  - Si + MO\(_X\) M + SiO\(_2\)
  - Si + MO\(_X\) MSi\(_X\) + SiO\(_2\)
  - Si + MO\(_X\) M + MSi\(_X\)O\(_Y\)

- **Gas or liquid at 1000 K**

- **Radio active**

#### Elements

- **Gas or liquid at 1000 K**
  - He
  - B
  - C
  - N
  - O
  - F
  - Ne

- **Radio active**
  - He

- **Unstable at Si interface**
  - Si + MO\(_X\) M + SiO\(_2\)
  - Si + MO\(_X\) MSi\(_X\) + SiO\(_2\)
  - Si + MO\(_X\) M + MSi\(_X\)O\(_Y\)

- **La\(_2\)O\(_3\)** based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

- **HfO\(_2\)** based dielectrics are selected as the first generation materials, because of their merit in 1) band-offset, 2) dielectric constant, 3) thermal stability.

####Choice of High-k elements for oxide

- HfO\(_2\) based dielectrics are selected as the first generation materials, because of their merit in 1) band-offset, 2) dielectric constant, 3) thermal stability.

- **La\(_2\)O\(_3\)** based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band offset

Oxide

Si

Band Discontinuity [eV]

Dielectric Constant $\varepsilon(0)$

XPS measurement by Prof. T. Hattori, INFOS 2003
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness
For the past 45 years, SiO2 and SiON have been used as gate insulators. However, the EOT limit has been reached at 0.7~0.8 nm. Today, EOT is 1.0 nm, which is still above the EOT limit. To reduce the EOT further, high-k materials like HfO2 have been introduced, reducing EOT to 0.5~0.7 nm. To achieve an EOT of 0.5 nm, direct contact to Si is proposed. By choosing appropriate materials and processes, EOT can be reduced beyond 0.5 nm.
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O$^*$ $\rightarrow$ HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 6131

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction

D.J. Lichtenwalner, Trans. ECS 11, 319
### Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>Unstable at Si interface</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
<th>He</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Si + MO&lt;sub&gt;x&lt;/sub&gt; M + SiO&lt;sub&gt;2&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Li Be</td>
<td>Si + MO&lt;sub&gt;x&lt;/sub&gt; MSi&lt;sub&gt;x&lt;/sub&gt; + SiO&lt;sub&gt;2&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Na Mg</td>
<td>Si + MO&lt;sub&gt;x&lt;/sub&gt; M + MSi&lt;sub&gt;x&lt;/sub&gt;O&lt;sub&gt;y&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>K Ca Sc</td>
<td>Al Si P S Cl Ar</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rh Sr Y Zr</td>
<td>Unstable at Si interface</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cs Ba Hf</td>
<td>La&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;3&lt;/sub&gt; based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer</td>
<td></td>
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<tr>
<td>Fr Ra Rf</td>
<td>La Ce Pr Nd Pm Sm Eu Gd Tb Dy Ho Er Tm Yb Lu</td>
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</table>

R. Hauser, IEDM Short Course, 1999
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
EOT = 0.48 nm        Our results

Transistor with La2O3 gate insulator
EOT=0.37nm
La2O3

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

W/L = 50µm /2.5µm

Vg=0V  Vg=0.2V  Vg=0.4V  Vg=0.6V  Vg=0.8V  Vg=1.0V  Vg=1.2V
Vth=-0.06V  Vth=-0.05V  Vth=-0.04V

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

0.48 → 0.37nm Increase of $I_d$ at 30%
$\mu_{\text{eff}}$ of W/La$_2$O$_3$ and W/HfO$_2$ nFET on EOT

- W/La$_2$O$_3$ exhibits higher $\mu_{\text{eff}}$ than W/HfO$_2$
- $\mu_{\text{eff}}$ start degrades below EOT=1.4nm
FET characteristics of W/La$_2$O$_3$ on EOT

N$_{fix}$ = $7 \times 10^{12}$ cm$^{-2}$

Aggressive N$_{fix}$ generation at EOT < 1.2 nm

All characteristics start to degrade or shift below EOT = 1.4 nm
Gate Metal Induced Defects Compensation

Suppression of aggressive shift in $V_{fb}$

TEM
EDX

Metal Gate
- MgO
- La2O3
- Si

PMA 500°C

Gate Metal Induced Defects Compensation

Mobility Improvement with Mg Incorporation

Recovery of $\mu_{\text{eff}}$ mainly at low $E_{\text{eff}}$
6 µm NMOS LSI in 1974

**Layers**
1. Si substrate
2. Field oxide
3. Gate oxide
4. Poly Si
5. S/D
6. Interlayer
7. Aluminum
8. Passivation

**Materials**
1. Si
2. SiO₂
3. BPSG
4. Al
5. PSG

**Atoms**
1. Si
2. O
3. P
4. B
5. Al
(H, N, Cl)
New materials

Just examples!
Many other candidates

Al
Si
SiO₂
Poly Si
Si₃N₄
PtSi₂
WSi₂
CoSi₂
TiSi₂
MoSi₂
TaSi₂

NiSi silicide
SiGe Semiconductor
Low-k dielectrics
Air
HSQ
Polymer
TaN
Cu
W
Metals

La₂O₃
Ta₂O₅
HfO₂
ZrO₂
ZrSiₓOᵧ
RuO₂
Pt
IrO₂
Y₁
PZT
BST

High-k dielectrics
Electrode materials
Ferroelectrics
Semiconductors

Ge
III-V

PtSi₂
WSi₂
CoSi₂
TiSi₂
MoSi₂
TaSi₂

Silicides


Al
Al
SiO₂
SiO₂
Si
Si

Just examples!
Many other candidates

Y. Nishi, Si Nano Workshop, 2006,
(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)
What is a roadmap? What is ITRS?

Roadmap: Prediction of future technologies

ITRS: International Technology Roadmap for Semiconductors made by SIA (Semiconductor Industry Association with Collaboration with Japan, Europe, Korea and Taiwan)
1992 - 1997: NTRS (National Technology Roadmap)
1998 - : ITRS (International Technology Roadmap)
5 nm gate length CMOS
Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC
IEDM, 2003
Question:
How far we can go with downscaling?
How far can we go for production?

Past

0.7 times per 3 years

In 40 years: 18 generations,
Size 1/300, Area 1/100,000

1970

10μm → 8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm →
0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

Now

Future

→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

• At least 4,5 generations to 8nm

• Hopefully 8 generations to 3nm
Subthreshold leakage current of MOSFET

- $V_{g}=0V$
- Subthreshold leakage current of MOSFET
- $I_{on}$
- $I_{off}$
- $V_{th}$ (Threshold Voltage)
Subthreshold slope (SS)  
\[ SS = (\ln 10)(kT/q)(C_{ox}+C_D+C_{it})/C_{ox} \]  
> ~ 60 mV/decade at RT

SS value:  
Constant and does not become small with down-scaling

Vth cannot be decreased anymore  
Significant Ioff increase

Vth: 300mV → 100mV  
Ioff increases with 3.3 decades  
(300 – 100)mV/(60mV/dec)  
= 3.3 dec

Vg (V)  
Log scale Id plot  
Ion  
Ioff

Log Id per unit gate width (\(= 1\mu m\))

Vdd down-scaling  
Vdd=0.5V  
Vdd=1.5V

Voff increases with 3.3 decades (300 – 100)mV/(60mV/dec)  
= 3.3 dec

Vth: 300mV  
Æ 100mV

Vth cannot be decreased anymore
Subthreshold leakage current of MOSFET

- \( V_{g}=0 \text{V} \) Subtheshold Leakage Current
- \( I_{on} \) is OK at Single Tr. level
- But not OK For Billions of Trs.

Subthreshold region

\( V_{th} \) (Threshold Voltage)
The limit is different depending on application.
The down scaling of MOSFETs is still possible for at least another 10 years!

3 important technological items for down scaling.

New materials

1. Thinning of high-k gate oxide thickness beyond 0.5 nm

2. Metal S/D

New structures

3. Wire channel
1. High-k beyond 0.5 nm
Choice of High-k elements for oxide

| Candidates | Unstable at Si interface | Gas or liquid at 1000 K | Radio active | He
|------------|--------------------------|------------------------|-------------|
| H          | Si + MO\textsubscript{x} M + SiO\textsubscript{2} |            |             | B C N O F Ne
| Li Be      | Si + MO\textsubscript{x} MSi\textsubscript{x} + SiO\textsubscript{2} |            |             | Al Si P S Cl Ar
| Mg Na      | Si + MO\textsubscript{x} M + MSi\textsubscript{x}O\textsubscript{y} |            |             | K Ti V Cr Mn Fc Co Ni Cu Zn Ga Ge As Se Br Kr
| Ca Sc      |                            |            |             | Sr Y Zr Nb Mo Tc Ru Rb Pd Ag Cd In Sn Sb Te I Xe
| Cs Ba Hf   |                            |            |             | La2O\textsubscript{3} based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer
| Fr Ra Ac   |                            |            |             | La

R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

XPS measurement by Prof. T. Hattori, INFOS 2003
High-k gate insulator MOSFETs for Intel: EOT=1nm

HfO₂ based high-k
For the past 45 years SiO₂ and SiON For gate insulator

Today EOT=1.0nm

EOT Limit 0.7~0.8 nm

One order of Magnitude

EOT=0.5nm

EOT can be reduced further beyond 0.5 nm by using direct contact to Si By choosing appropriate materials and processes.

Introduction of High-k

Still SiO₂ or SiON Is used at Si interface

Direct Contact Of high-k and Si

Power per MOSFET (P)

Now Year
Preparation Room

E-Beam Evaporation
8 different target

Anneal
Micro to mille-seconds

Sputter for metal
5 different target

Robot room

Cluster tool for high-k thin film deposition
SiO$_x$-IL growth at HfO$_2$/Si Interface

XPS Si1s spectrum

Intensity (a.u)

1837 1840 1843 1846

Binding energy (eV)

Si sub.

Hf Silicate

SiO$_2$

Phase separator

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O$^*$ $\rightarrow$ HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 6131

SiO$_x$-IL is formed after annealing

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Trans. ECS 11, 319

Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ can achieve direct contact of high-k/Si
Gate Leakage vs EOT, (Vg=|1|V)

- Al2O3
- HfAlO(N)
- HfO2
- HfSiO(N)
- HfTaO
- La2O3
- Nd2O3
- Pr2O3
- PrSiO
- PrTiO
- SiON/SiN
- Sm2O3
- SrTiO3
- Ta2O5
- TiO2
- ZrO2(N)
- ZrSiO
- ZrAlO(N)
La$_2$O$_3$ at 300ºC process make sub-0.4 nm EOT MOSFET

EOT=0.37nm

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

0.48 $\rightarrow$ 0.37nm Increase of $I_d$ at 30%
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small Dit

- Silicate-reaction-formed fresh interface
- Stress relaxation at interface by glass type structure of La silicate.


Fresh interface with silicate reaction
FGA800°C is necessary to reduce the interfacial stress
A small $D_{it}$ of $1.6 \times 10^{11}$ cm$^{-2}$/eV, results in better electron mobility.
Increasing EOT caused by high temperature annealing can be dramatically suppressed by Silicon masked stacks.
No interfacial layer can be confirmed with Si/TiN/W.
nMOSFET with EOT of 0.62nm

EOT of 0.62nm and 155 cm$^2$/Vsec at 1MV/cm can be achieved
Benchmark of La-silicate dielectrics

Gate leakage is two orders of magnitude lower than that of ITRS

Electron mobility is comparable to record mobility with Hf-based oxides

This work (MIPS Stacks)

Open : Hf-based oxides

T. Ando et al., IEDM2009
Metal (Silicide) S/D
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- $V_t$ and $I_{ON}$ variation
- GIDL

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Surface or interface control

**Diffusion species:** metal atom (Ni, Co)
- Rough interface at silicide/Si
  - Excess silicide formation
  - Different $\phi_B$ presented at interface
  - Process temperature dependent composition

**Diffusion species:** Si atom (Ti)
- Surface roughness increases
  - Line dependent resistivity change

Annealing: 650 °C
Si(001) sub. Epitaxial NiSi$_2$


Unwanted leakage current

- Edge leakage current at periphery
- Generation current due to defects in substrate

Variable leakage current in smaller contact

Specification for metal silicide S/D

- Atomically flat interface with smooth surface
- Suppressed leakage current
- Stability of silicide phase and interface in a wide process temperature

Annealing: 500 °C

\[ V_{\text{app}} = -0.2V \]

\[ \phi_{Bn} = \sim 0.57 \text{ eV} \]
Deposition of Ni-Si mixed films from NiSi₂ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
**SEM views of silicide/Si interfaces**

Ni source (50nm)

- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

NiSi$_2$ source (50nm)

- Atomically flat interfaces
- No Si consumption
- Temperature-independent

Ni source

- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

NiSi$_2$ source

- Atomically flat interfaces
- No Si consumption
- Temperature-independent
Ideal characteristics ($n = 1.00$, suppressed leakage current)

- Flat interface and No Si substrate consumption
- No defects in Si substrate

NiSi$_2$ source

Suppressed reverse leakage current

<table>
<thead>
<tr>
<th>Source</th>
<th>$\phi_B$ (eV)</th>
<th>n</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>0.676</td>
<td>1.08</td>
</tr>
<tr>
<td>NiSi$_2$</td>
<td>0.659</td>
<td>1.00</td>
</tr>
</tbody>
</table>

RTA: 500°C, 1 min

Current density (A/cm$^2$) vs. Applied Voltage (V)
Wire channel
Suppression of subthreshold leakage by surrounding gate structure

Planar

Surrounding gate
Because of off-leakage control, 

Planar $\rightarrow$ Fin $\rightarrow$ Nanowire

Planar FET

Leakage current

Fin FET

Nanowire FET
Nanowire structures in a wide meaning

- Fin
- Tri-gate
- $\Omega$-gate
- All-around
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of $I_{OFF}$
3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires
Increase the Number of quantum channels

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

By Prof. Shiraishi of Tsukuba univ.

4 channels can be used
Device fabrication

Si/Si$_{0.8}$Ge$_{0.2}$ superlattice epitaxy on SOI

Anisotropic etching of these layers

Isotropic etching of SiGe

The NW diameter is controllable down to 5 nm by self limited oxidation.

Gate depositions
HfO$_2$ (3nm)
TiN (10nm)
Poly-Si (200nm)

Gate etching

S/D implantation
Spacer formation
Activation anneal
Salicidation

Standard Back-End of-Line Process

Process Details:
C. Dupre et al.,
3D-stacked Si NWs with Hi-\(k\)/MG

Wire direction : \(<110>\)
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT ~2.6 nm

C. Dupre \textit{et al.},
SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oxide etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

Standard recipe for gate stack formation
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off $> 10^6$, 60uA/wire

$L_g = 65\text{nm}$, $T_{ox} = 3\text{nm}$
Bench Mark

Our Work
\( I_{ON}/I_{OFF} \) Bench mark

Planer FET

<table>
<thead>
<tr>
<th>Name</th>
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<tbody>
<tr>
<td>S. Kamiyama</td>
<td>IEDM 2009</td>
<td>431</td>
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<td>P. Packan</td>
<td>IEDM 2009</td>
<td>659</td>
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Si nanowireFET

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<tr>
<td>Y. Jiang</td>
<td>VLSI 2008</td>
<td>34</td>
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<td>H.-S. Wong</td>
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<td>S.D. Suk</td>
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<tr>
<td>G. Bidel</td>
<td>VLSI 2009</td>
<td>240</td>
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</tbody>
</table>

\( L_g = 500 \sim 65 \text{nm} \)
Electron Density (x10^{19} cm^{-3})

Distance from SiNW Surface (nm)

Edge portion

Flat portion
Primitive estimation!

- Small EOT for high-k (33)
- P-MOS improvement (26)
- Low S/D resistance (20)
- Low S/D resistance (15)
- Compact model

SiNW (12nm × 19nm)

Assumption

\[ I_{ON} \propto L_g^{-0.5} T_{ox}^{-1} \]

- # of wires /1μm
- Assumption

- ITRS
- MG
- FD
- bulk
Our roadmap for R & D
Source: H. Iwai, IWJT 2008

Current Issues
Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Thank you for your attention!