Past and Future of Micro/Nano-Electronic Devices

April 28, 2012

IEEE EDS Distinguished Lecture

@Institute of Engineering & Management, Kolkata, India

Hiroshi Iwai,
Tokyo Institute of Technology
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
Institute Overview

Established in 1881 → 130th anniversary in 2011

3 undergraduate schools
School of Science, School of Engineering, School of Bioscience and Biotechnology

7 graduate schools
Science and Engineering Science, Science and Engineering Technology,
Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

<table>
<thead>
<tr>
<th></th>
<th>Undergraduate</th>
<th>Graduate</th>
<th>Master's</th>
<th>Doctoral</th>
<th>Teaching Staff</th>
<th>Student/Instructor</th>
<th>Staff</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tokyo Inst.</strong></td>
<td>5,000</td>
<td>5,000</td>
<td>3,500</td>
<td>1,500</td>
<td>1,200</td>
<td>8.3</td>
<td>550</td>
</tr>
<tr>
<td><strong>Per Year</strong></td>
<td>1,200</td>
<td>1,800</td>
<td>500</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Total 982
(As of May. 1, 2005)

<table>
<thead>
<tr>
<th>Region</th>
<th>Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>Asia</td>
<td>847</td>
</tr>
<tr>
<td>Europe</td>
<td>78</td>
</tr>
<tr>
<td>North America</td>
<td>12</td>
</tr>
<tr>
<td>South America</td>
<td>24</td>
</tr>
<tr>
<td>Oceania</td>
<td>5</td>
</tr>
<tr>
<td>Africa</td>
<td>16</td>
</tr>
</tbody>
</table>

### Map

- Asia 847
- Europe 78
- North America 12
- South America 24
- Oceania 5
東京工業大学大学院
総合理工学研究科
先端ナノエレクトロニクス研究コアユニット研究室メンバー

(2010年10月1日現在)

教育 Education

産業界
大學・独法
海外大学（アジア諸国など）
Industry
Universities/Independent administrative institutions
Overseas universities (such as Asian countries)

連携 Collaboration

国際
ナノ電子デバイス
教育研究拠点
International
Nanoelectronic devices
Education and research center

研究 Research

世界を先導する研究
超低消費電力、超低電圧動作、超高能率電子デバイス
World-leading research
Ultra low power consumption, ultra low voltage operation, and ultra high performance electronic devices

省エネ
地球温暖化防止、安心・安全
Energy saving, prevention of global warming and realization of a safe and secure society
研究風景
Cluster tool for high-k thin film deposition

Preparation Room

Sputter for metal
5 different target

Robot room

E-Beam Evaporation
8 different target

Flash Lamp
Anneal
Micro to milli-seconds
• There were many inventions in the 20th century: Airplane, Nuclear Power generation, Computer, Space aircraft, etc
• However, everything has to be controlled by electronics
• Electronics
  Most important invention in the 20th century
• What is Electronics: To use electrons, Electronic Circuits
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Cathode (heated) Grid Anode (Positive bias)

Same mechanism as that of transistor
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power consumption
J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928
Capacitor structure with notch

**Negative bias**

- Gate Electrode
- Gate Insulator
- Semiconductor
- Electron

No current

**Positive bias**

- Electric field

Current flows
Surface Potential (Negative direction)

- **0V**
  - **N⁺-Si**
  - **P-Si**

- **1V**
  - **N-Si**

**0 bias for gate**

**Positive bias for gate**

Electron flow

- **G**
  - **S**
  - **D**

Source Channel Drain

Gate electrode
Gate Oxid
Channel
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator. 

Interfacial Charges

Electric Shielding

Carrier Scattering

Drain Current was several orders of magnitude smaller than expected.

Even Shockley!
However, they found amplification phenomenon when investigating Ge surface when putting needles. This is the 1st Transistor: 

Not Field Effect Transistor, 
But Bipolar Transistor (another mechanism)

1947: 1st transistor

Bipolar using Ge

J. Bardeen  W. Bratten, W. Shockley
1958: 1st Integrated Circuit

Connect 2 bipolar transistors in the Same substrate by bonding wire.

Jack S. Kilby
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source
↓
Drain
↓
Al Gate

Al
SiO₂
Si

Si/SiO₂ Interface is extraordinarily good
1970,71: 1st generation of LSIs

DRAM   Intel 1103

MPU    Intel 4004
2011
Most recent SD Card

Lexar Professional

128GB
133x Speed
Most Recent SD Card

128GB (Bite)
= 128G X 8bit = 1024Gbit
= 1.024T(Tera)bit

1T = 10^{12} = 1Trillion

World Population : 7 Billion
Brain Cell : 10〜100 Billion
Stars in Galaxy : 100 Billion
Most Recent SD Card
128 GB = 1Tbit

2.4cm × 3.2cm × 0.21cm

Volume : 1.6cm³  Weight 2g

Voltage 2.7 - 3.6V

Old Vacuum Tube:

5cm × 5cm × 10cm, 100g, 100W

What are volume, weight, power consumption for 1Tbit
Old Vacuum Tube: 5cm X 5cm X 10cm

Volume = (5cm X 10,000) X (5cm X 10,000) X (5cm X 10,000)
= 0.5km X 0.5km X 1km

1Tbit = 10,000 X 10,000 X 10,000 bit

Pingan International Finance Center
Shanghai, China (Year 2016)
700 m

Indian Tower
Mumbai, India (Year 2016)
700 m

Burji Khalifa
Dubai, UAE (Year 2010)
828 m

500 m

1,000 m

1Tbit
Old Vacuum Tube: 100W

1Tbit = 10^{12}bit

Power = 0.1kWX10^{12}=50 \text{ TW}

Nuclear Power Generator: 1MkW=1BW

We need 50,000 Nuclear Power Plant for just one 128 GB memory

In Japan we have only 54 Nuclear Power Generator

Last summer Tokyo Electric Power Company (TEPCO) can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
MOS LSI experienced continuous progress for many years

<table>
<thead>
<tr>
<th>Name of Integrated Circuits</th>
<th>Number of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>1960s IC (Integrated Circuits)</td>
<td>~10</td>
</tr>
<tr>
<td>1970s LSI (Large Scale Integrated Circuit)</td>
<td>~1,000</td>
</tr>
<tr>
<td>1980s VLSI (Very Large Scale IC)</td>
<td>~10,000</td>
</tr>
<tr>
<td>1990s ULSI (Ultra Large Scale IC)</td>
<td>~1,000,000</td>
</tr>
<tr>
<td>2000s ?LSI (? Large Scale IC)</td>
<td>~1,000,000,000</td>
</tr>
</tbody>
</table>
MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Use Gate Field Effect for switching

N-MOS (N-type MOSFET)
N-MOS (N-type MOSFET)

Source

p-Si

n-Si

Electron flow

Gate

Current flow

Drain

n-Si

p-Si

P-MOS (P-type MOSFET)

Source

p-Si

n-Si

Hole flow

Gate

Current flow

Drain

p-Si

p-Si
CMOS

Complimentary MOS

Inverter

PMOS

NMOS

When NMOS is ON, PMOS is OFF

When PMOS is ON, NMOS is OFF
CMOS Technology:
Indispensable for our human society

All the human activities are controlled by CMOS
   living, production, financing, telecommunication,
   transportation, medical care, education,
   entertainment, etc.

Without CMOS:
   There is no computer in banks, and
   world economical activities immediately stop.

Cellarer phone dose not exists
# Downsizing of the components has been the driving force for circuit evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Technology</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>1900</td>
<td>Vacuum Tube</td>
<td>10 cm</td>
</tr>
<tr>
<td>1950</td>
<td>Transistor</td>
<td>cm</td>
</tr>
<tr>
<td>1960</td>
<td>IC</td>
<td>mm</td>
</tr>
<tr>
<td>1970</td>
<td>LSI</td>
<td>10 µm</td>
</tr>
<tr>
<td>2000</td>
<td>ULSI</td>
<td>100 nm</td>
</tr>
</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. 
**We have never experienced such a tremendous reduction of devices in human history.**
Downsizing

1. Reduce Capacitance
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. Increase number of Transistors
   - Parallel processing
     - Increase circuit operation speed

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.
Why $t_{\text{ox}}$ thinning

- $t_{\text{ox}}$ thinning affects channel potential control.
- $t_{\text{ox}}$ thinning and $V_{\text{dd}}$ must be decreased for better channel potential control → $I_{\text{OFF}}$ Suppression.

Region governed by gate bias

Region governed by drain bias

DL touch with $S$ Region (DL)

$t_{\text{ox}}$ thinning

$0V < V_{\text{dep}} < 1V$

No $t_{\text{ox}}$ thinning

Large $I_{\text{OFF}}$

$V_{\text{dd}}$

$0.5V$
Scaling Method: by R. Dennard in 1974

**Wdep**: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed. Otherwise, large leakage between S and D

Leakage current

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

**K=0.7 for example**

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

**Good scaled I-V characteristics**

\[
W_{\text{dep}} \propto \sqrt{V/Na} : K
\]

**X, Y, Z : K, V : K, Na : 1/K**

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.
## Downscaling merit: Beautiful!

<table>
<thead>
<tr>
<th>Geometry &amp; Supply voltage</th>
<th>$L_g, W_g$</th>
<th>$T_{ox}, V_{dd}$</th>
<th>$K$</th>
<th><strong>Scaling $K$: K=0.7 for example</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive current in saturation</td>
<td>$I_d$</td>
<td>$K$</td>
<td>$I_d = v_{sat} W_g C_o (V_g - V_{th})$</td>
<td>$C_o$: gate C per unit area</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1} (V_g - V_{th}) = K^{-1}K = K$</td>
<td></td>
</tr>
<tr>
<td>$I_d$ per unit $W_g$</td>
<td>$I_d / \mu m$</td>
<td>1</td>
<td>$I_d$ per unit $W_g = I_d / W_g = 1$</td>
<td></td>
</tr>
<tr>
<td>Gate capacitance</td>
<td>$C_g$</td>
<td>$K$</td>
<td>$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox}$</td>
<td>$KK/K = K$</td>
</tr>
<tr>
<td>Switching speed</td>
<td>$\tau$</td>
<td>$K$</td>
<td>$\tau = C_g V_{dd} / I_d$</td>
<td>$KK/K = K$</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>$f$</td>
<td>$1/K$</td>
<td>$f = 1/\tau = 1/K$</td>
<td></td>
</tr>
<tr>
<td>Chip area</td>
<td>$A_{chip}$</td>
<td>$\alpha$</td>
<td>$\alpha$: Scaling factor</td>
<td>In the past, $\alpha &gt; 1$ for most cases</td>
</tr>
<tr>
<td>Integration (# of Tr)</td>
<td>$N$</td>
<td>$\alpha/K^2$</td>
<td>$N$</td>
<td>$\alpha/K^2 = 1/K^2$, when $\alpha = 1$</td>
</tr>
<tr>
<td>Power per chip</td>
<td>$P$</td>
<td>$\alpha$</td>
<td>$fNCV^2/2$</td>
<td>$K^{-1}(\alpha K^{-2})K (K^1)^2 = \alpha = 1$, when $\alpha = 1$</td>
</tr>
<tr>
<td>k= 0.7 and $\alpha = 1$</td>
<td>k= 0.7$^2$ =0.5 and $\alpha = 1$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Single MOFET</strong></td>
<td><strong>Single MOFET</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vdd $\rightarrow$ 0.7</td>
<td>Vdd $\rightarrow$ 0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lg $\rightarrow$ 0.7</td>
<td>Lg $\rightarrow$ 0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Id $\rightarrow$ 0.7</td>
<td>Id $\rightarrow$ 0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cg $\rightarrow$ 0.7</td>
<td>Cg $\rightarrow$ 0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P$ (Power)/Clock $\rightarrow$ $0.7^3 = 0.34$</td>
<td>$P$ (Power)/Clock $\rightarrow$ $0.5^3 = 0.125$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\tau$ (Switching time) $\rightarrow$ 0.7</td>
<td>$\tau$ (Switching time) $\rightarrow$ 0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Chip</strong></td>
<td><strong>Chip</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N (# of Tr) $\rightarrow$ $1/0.7^2 = 2$</td>
<td>N (# of Tr) $\rightarrow$ $1/0.5^2 = 4$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>f (Clock) $\rightarrow$ $1/0.7 = 1.4$</td>
<td>f (Clock) $\rightarrow$ $1/0.5 = 2$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P (Power) $\rightarrow$ 1</td>
<td>P (Power) $\rightarrow$ 1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Change in 30 years

<table>
<thead>
<tr>
<th>Change in 30 years</th>
<th>Ideal scaling</th>
<th>Real Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_g )</td>
<td>( K )</td>
<td>( 10^{-2} )</td>
</tr>
<tr>
<td>( t_{ox} )</td>
<td>( K(10^{-2}) )</td>
<td>( 10^{-2} )</td>
</tr>
<tr>
<td>( V_{dd} )</td>
<td>( K(10^{-2}) )</td>
<td>( 10^{-1} )</td>
</tr>
<tr>
<td>( A_{chip} )</td>
<td>( \alpha )</td>
<td>( 10^1 )</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Ideal scaling</th>
<th>Real Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_d/\mu m )</td>
<td>( K(10^{-2}) )</td>
<td>( 10^{-1} )</td>
</tr>
<tr>
<td>( f )</td>
<td>( 1/K(10^2) )</td>
<td>( 10^3 )</td>
</tr>
<tr>
<td>( P )</td>
<td>( \alpha(10^1) )</td>
<td>( 10^5 )</td>
</tr>
</tbody>
</table>

**V_{dd} scaling insufficient, \( \alpha \) increased**

\[ V_{dd} \text{ scaling insufficient} \rightarrow N, I_d, f, P \text{ increased significantly} \]
Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1µm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5µm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25µm:</td>
<td>Direct-tunneling of gate SiO₂</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1µm:</td>
<td>‘0.1µm brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
Historically, many predictions of the limit of downsizing. VLSI textbook written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.
Finally, there appears to be a fundamental limit of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide begin to make the devices of smaller dimension unworkable.
Direct-tunneling effect

Gate Electrode  Gate Oxide  Si Substrate

Potential Barrier

Wave function  Direct tunneling current

Direct tunneling leakage current starts to flow when the thickness is 3 nm.
Direct tunneling leakage was found to be OK! In 1994!
Gate leakage: \( I_g \propto \text{Gate Area} \propto \text{Gate length (Lg)} \)

Drain current: \( I_d \propto 1/\text{Gate length (Lg)} \)

\( \text{Lg} \to \text{small}, \)  
Then, \( I_g \to \text{small}, I_d \to \text{large}, \) Thus, \( I_g/I_d \to \text{very small} \)
Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!

Some one will think for you
Transistor Scaling Continues

qi xinag, ecs 2004, amd
Downsizing limit?  
Electron wave length

Channel length?

10 nm
5 nm gate length CMOS Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC

IEDM, 2003
Gate Oxidation

Electron wave length
10 nm

Tunneling distance
3 nm

Downsizing limit!
Channel length
Gate oxide thickness
Prediction now!

Electron wave length

10 nm

Tunneling distance

3 nm

Atom distance

0.3 nm

MOSFET operation

Lg = 2 ~ 1.5 nm?

Below this, no one knows future!
However, Gate oxide thickness 2 orders magnitude smaller! Close to limitation!!

Lg: Gate length downsizing will continue to another 10-15 years
0.8 nm Gate Oxide Thickness MOSFETs operates!!

**0.8 nm: Distance of 3 Si atoms!!**

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
So, we are now in the limitation of downsizing?

Do you believe this or do not?
To use high-k dielectrics

**K**: Dielectric Constant

- Thin SiO₂: K=4
- Thick high-k dielectrics: K=20

- 5 times thicker
- Small leakage Current

Almost the same electric characteristics

However, very difficult and big challenge!
### Choice of High-k elements for oxide

#### Candidates

<table>
<thead>
<tr>
<th>Transuranics</th>
<th>Actinides</th>
<th>Elements</th>
<th>Radioactive</th>
<th>Unstable at Si interface</th>
<th>Gas or liquid at 1000 K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hf</td>
<td>Ti</td>
<td>K</td>
<td>He</td>
<td>Si + MOₓ M + SiO₂</td>
<td>Si + MOₓ MSiₓ + SiO₂</td>
</tr>
<tr>
<td>Be</td>
<td>V</td>
<td>Na</td>
<td>B</td>
<td>Si + MOₓ M + MSiₓOᵧ</td>
<td>Si + MOₓ M + SiO₂</td>
</tr>
<tr>
<td>Li</td>
<td>Cr</td>
<td>Mg</td>
<td>O</td>
<td>Si + MOₓ M + SiO₂</td>
<td>Si + MOₓ M + SiO₂</td>
</tr>
<tr>
<td>He</td>
<td>Mn</td>
<td>Ca</td>
<td>F</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fe</td>
<td>Sc</td>
<td>Ne</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Co</td>
<td>Ti</td>
<td>Ar</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ni</td>
<td>V</td>
<td>Al</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Cu</td>
<td>Cr</td>
<td>Si</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Zn</td>
<td>Mn</td>
<td>P</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ga</td>
<td>F</td>
<td>S</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ge</td>
<td>As</td>
<td>Cl</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>As</td>
<td>Se</td>
<td>Ar</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Br</td>
<td>Br</td>
<td>He</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Kr</td>
<td>He</td>
<td>Hf</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Sr</td>
<td>Y</td>
<td>Li</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Y</td>
<td>Zr</td>
<td>Na</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Zr</td>
<td>Cs</td>
<td>Al</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Cs</td>
<td>Ba</td>
<td>Si</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ba</td>
<td>Hf</td>
<td>P</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hf</td>
<td>La</td>
<td>Si</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>La</td>
<td>Ce</td>
<td>Pb</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ce</td>
<td>Pr</td>
<td>Sn</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pr</td>
<td>Nd</td>
<td>Re</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Nd</td>
<td>Pm</td>
<td>Mo</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pm</td>
<td>Sm</td>
<td>Nb</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Sm</td>
<td>Eu</td>
<td>Co</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Eu</td>
<td>Gd</td>
<td>Ti</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Gd</td>
<td>Tb</td>
<td>Hf</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Tb</td>
<td>Dy</td>
<td>Fe</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dy</td>
<td>Ho</td>
<td>Pt</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ho</td>
<td>Er</td>
<td>Au</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Er</td>
<td>Tm</td>
<td>Hg</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Tm</td>
<td>Y</td>
<td>Tl</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Y</td>
<td>Lu</td>
<td>Pb</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Lu</td>
<td>La</td>
<td>Bi</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>La</td>
<td>Ce</td>
<td>Po</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ce</td>
<td>Pr</td>
<td>At</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pr</td>
<td>Nd</td>
<td>Tl</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Nd</td>
<td>Pm</td>
<td>Pb</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pm</td>
<td>Sm</td>
<td>Sn</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Sm</td>
<td>Eu</td>
<td>Se</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Eu</td>
<td>Gd</td>
<td>Br</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Gd</td>
<td>Tb</td>
<td>Kr</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Tb</td>
<td>Dy</td>
<td>In</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dy</td>
<td>Ho</td>
<td>Sn</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ho</td>
<td>Er</td>
<td>Pb</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Er</td>
<td>Tm</td>
<td>Bi</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Tm</td>
<td>Y</td>
<td>Po</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Y</td>
<td>La</td>
<td>At</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

HfO₂ based dielectrics are selected as the first generation materials, because of their merit in 1) band-offset, 2) dielectric constant 3) thermal stability.

La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

---

R. Hauser, IEDM Short Course, 1999  
Conduction band offset vs. Dielectric Constant

![Diagram showing the conduction band offset vs. dielectric constant, with data points for various materials like Gd$_2$O$_3$, Lu$_2$O$_3$, and HfO$_2$. The diagram includes a band discontinuity vs. band offset graph, with a note that the data was measured by XPS and provided by Prof. T. Hattori, INFOS 2003.](image-url)
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness
For the past 45 years, SiO2 and SiON have been used as gate insulators. Today, the EOT is 1.0 nm. One order of magnitude can be achieved by using direct contact to Si, and EOT can be reduced further beyond 0.5 nm by using appropriate materials and processes.
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ $\sqsubset$ HfO$_2$ + Si + 2O* $\sqsubset$ HfO$_2$ + SiO$_2$

Oxygen supplied from W gate electrode

H. Shimizu, JJAP, 44, pp. 6131

D.J. Lichtenwalner, Trans. ECS 11, 319

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction

TEM image 500 °C 30min

SiO$_x$-IL growth at HfO$_2$/Si Interface
Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>Unstable at Si interface</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Si + MOₓ M + SiO₂</td>
<td>He</td>
<td></td>
</tr>
<tr>
<td>Li Be</td>
<td>Si + MOₓ MSiₓ + SiO₂</td>
<td>B C N O F Ne</td>
<td></td>
</tr>
<tr>
<td>Mg Na</td>
<td>Si + MOₓ M + MSiₓOᵧ</td>
<td>Al Si P S Cl Ar</td>
<td></td>
</tr>
</tbody>
</table>

- Si + MOₓ M + SiO₂
- Si + MOₓ MSiₓ + SiO₂
- Si + MOₓ M + MSiₓOᵧ
- Si + MOₓ M + MSiₓ

<table>
<thead>
<tr>
<th>K</th>
<th>Ca Sc</th>
<th>Ti V Cr Mn Fc Co Ni Cu Zn Ga Ge As Se Br Kr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ca Sc</td>
<td>Ti V</td>
<td>Cr Mn</td>
</tr>
<tr>
<td>Sr Y Zr</td>
<td>Nb Mo</td>
<td>Tc Ru</td>
</tr>
<tr>
<td>Cs Ba Hf</td>
<td>Ta W</td>
<td>Re Os</td>
</tr>
<tr>
<td>Fr Ra Rf</td>
<td>Ha Sg</td>
<td>Ns Hs</td>
</tr>
<tr>
<td>La Ce Pr Nd</td>
<td>Sm Eu</td>
<td>Gd Tb Dy Ho Er Tm Y b Lu</td>
</tr>
</tbody>
</table>

- HfO₂ based dielectrics are selected as the first generation materials, because of their merit in:
  1) band-offset
  2) dielectric constant
  3) thermal stability

- La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

Choice of High-k elements for oxide are selected as the first generation materials, because of their merit in:
1) band-offset
2) dielectric constant
3) thermal stability

R. Hauser, IEDM Short Course, 1999
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ can achieve direct contact of high-k/Si

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
EOT = 0.48 nm

Our results

Transistor with La2O3 gate insulator
EOT=0.37nm
La2O3

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

0.48 → 0.37nm Increase of Id at 30%
\( \mu_{\text{eff}} \) of W/La\(_2\)O\(_3\) and W/HfO\(_2\) nFET on EOT

- W/La\(_2\)O\(_3\) exhibits higher \( \mu_{\text{eff}} \) than W/HfO\(_2\)
- \( \mu_{\text{eff}} \) start degrades below EOT=1.4nm
FET characteristics of W/La$_2$O$_3$ on EOT

All characteristics start to degrade or shift below EOT=1.4nm

$N_{\text{fix}} = 7 \times 10^{12}$ cm$^{-2}$

Aggressive $N_{\text{fix}}$ generation at EOT < 1.2nm

$N_{\text{fix}}$ and $D_{it}$

All characteristics start to degrade or shift below EOT=1.4nm
Gate Metal Induced Defects Compensation

Suppression of aggressive shift in $V_{fb}$
Mobility Improvement with Mg Incorporation

Recovery of $\mu_{\text{eff}}$ mainly at low $E_{\text{eff}}$
6 µm NMOS LSI in 1974

Layers
1. Si substrate
2. Field oxide
3. Gate oxide
4. Poly Si
5. S/D
6. Interlayer
7. Aluminum
8. Passivation

Materials
1. Si
2. SiO$_2$
3. BPSG
4. Al
5. PSG

Atoms
1. Si
2. O
3. P
4. B
5. Al
(H, N, Cl)
New materials

Just examples!
Many other candidates

Semiconductors

Ge

III-V

La$_2$O$_3$

Ta$_2$O$_5$

HfO$_2$

ZrO$_2$

ZrSi$_x$O$_y$

RuO$_2$

Pt

IrO$_2$

Y1

PZT

BST

High-$k$ dielectrics

NiSi silicide

SiGe Semiconductor

Air

HSQ

Polymer

Low-$k$

dielectrics

Metals

TiN

TaN

Cu

W

Ferroelectrics

NiSi silicide

SiGe Semiconductor

Air

HSQ

Polymer

Low-$k$

dielectrics

Metals

TiN

TaN

Cu

W

High-$k$

dielectrics

NiSi silicide

SiGe Semiconductor

Air

HSQ

Polymer

Low-$k$

dielectrics

Metals

TiN

TaN

Cu

W

Ferroelectrics

New materials

Y. Nishi, Si Nano Workshop, 2006,
(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)
What is a roadmap? What is ITRS?

Roadmap: Prediction of future technologies

ITRS: International Technology Roadmap for Semiconductors made by SIA (Semiconductor Industry Association with Collaboration with Japan, Europe, Korea and Taiwan)
1992 - 1997: NTRS (National Technology Roadmap)
1998 - : ITRS (International Technology Roadmap)
5 nm gate length CMOS
Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et. al, NEC

IEDM, 2003
Question:
How far we can go with downscaling?
How far can we go for production?

**Past**
0.7 times per 3 years

1970年

10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm → 0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

**Now**

In 40 years: 18 generations,
Size 1/300, Area 1/100,000

**Future**

→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

- At least 4.5 generations to 8nm
- Hopefully 8 generations to 3nm
Subthreshold leakage current of MOSFET

Subthreshold Leakage Current

$V_{g}=0V$

Subthreshold region

$V_{th}$ (Threshold Voltage)
Vth cannot be decreased anymore

significantloff increase

Vth: 300mV → 100mV
loff increases with 3.3 decades
(300 – 100)mV/(60mv/dec)
= 3.3 dec

Subthreshold slope (SS)
= \((\text{Ln}10)(kT/q)(C_{ox} + C_D + C_{it})/C_{ox}\)
> ~ 60 mV/decade at RT

SS value:
Constant and does not become small with down-scaling
Subthreshold leakage current of MOSFET

Subthreshold leakage current is OK at single Tr. level but not OK for billions of Trs.

Subthreshold region

Vg=0V

Vth (Threshold Voltage)

Id

Ion

loff

OFF

ON

Subthreshold leakage current of MOSFET
The limit is different depending on application.
The down scaling of MOSFETs is still possible for at least another 10 years!

3 important technological items for down scaling.

New materials

1. Thinning of high-k gate oxide thickness beyond 0.5 nm
2. Metal S/D

New structures

3. Wire channel
1. High-k beyond 0.5 nm
## Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
<th>He</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Li</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Be</td>
<td>Si + MO_\textsubscript{X} M + SiO\textsubscript{2}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mg</td>
<td>Si + MO_\textsubscript{X} MSi_\textsubscript{X} + SiO\textsubscript{2}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Na</td>
<td>Si + MO_\textsubscript{X} M + MSi_\textsubscript{X}O_\textsubscript{Y}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ca</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sr</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Zr</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ba</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hf</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>La</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ce</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pr</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nd</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Eu</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gd</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tb</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dy</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ho</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Er</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yb</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lu</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

HfO\textsubscript{2} based dielectrics are selected as the first generation materials, because of their merit in:
1) band-offset,
2) dielectric constant,
3) thermal stability.

La\textsubscript{2}O\textsubscript{3} based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

Unstable at Si interface:
\[\text{Si} + \text{MO}_\text{X} \rightarrow \text{M} + \text{SiO}_2\]
\[\text{Si} + \text{MO}_\text{X} \rightarrow \text{MSi}_\text{X} + \text{SiO}_2\]
\[\text{Si} + \text{MO}_\text{X} \rightarrow \text{M} + \text{MSi}_\text{X}O_\text{Y}\]

Choice of High-k elements for oxide are selected as the first generation materials, because of their merit in:
1) band-offset,
2) dielectric constant,
3) thermal stability.

HfO\textsubscript{2} based dielectrics are selected as the first generation materials, because of their merit in:
1) band-offset,
2) dielectric constant,
3) thermal stability.

La\textsubscript{2}O\textsubscript{3} based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Oxide

Band offset

Si

\[ \text{Dielectric Constant} \]

\[ \begin{array}{cccc}
0 & 1 & 0 & 2 \\
0 & 3 & 0 & 4 \\
0 & 5 & 0 & 0
\end{array} \]

\[ \text{Band Discontinuity [eV]} \]

\[ \begin{array}{cccc}
4 & 2 & 0 & 0 \\
2 & 4 & 6 & 0 \\
0 & 2 & 4 & 0 \\
0 & 2 & 4 & 0
\end{array} \]

\[ \text{Si Band Gap} \]

\[ \begin{array}{cccc}
\text{Lu}_2\text{O}_3 & \text{Gd}_2\text{O}_3 & \text{La}_2\text{O}_3 \\
\text{Zr}_2\text{O}_2 & \text{Hf}_2\text{O}_2 \\
\end{array} \]

\[ XPS \text{ measurement by Prof. T. Hattori, INFOS 2003} \]
High-k gate insulator MOSFETs for Intel: EOT=1nm

HfO$_2$ based high-k
For the past 45 years, SiO₂ and SiON have been used as gate insulators. Today, EOT=1.0nm. The EOT limit is 0.7~0.8 nm. One order of magnitude improvement is achieved. EOT can be reduced further beyond 0.5 nm by using direct contact to Si. This can be achieved by choosing appropriate materials and processes.
Cluster tool for high-k thin film deposition

- Preparation Room
- E-Beam Evaporation
  - 8 different target
- Sputter for metal
  - 5 different target
- Flash Lamp
- Anneal
- Micro to mille-seconds
- Robot room
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O$^*$ $\rightarrow$ HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Trans. ECS 11, 319

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction

D.J. Lichtenwalner, Trans. ECS 11, 319
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$Si$_6$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Gate Leakage vs EOT, (Vg=|1|V)
La$_2$O$_3$ at 300°C process make sub-0.4 nm EOT MOSFET

EOT=0.37nm

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

0.48 $\rightarrow$ 0.37nm Increase of Id at 30%
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small $D_{it}$

- silicate-reaction-formed fresh interface
- stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA $800^\circ$C is necessary to reduce the interfacial stress

---

A small $D_{it}$ of $1.6 \times 10^{11}$ cm$^{-2}$/eV, results in better electron mobility.
Increasing EOT caused by high temperature annealing can be dramatically suppressed by Silicon masked stacks.
La$_2$O$_3$

W

TiN/W

Si/TiN/W

$K_{av} \sim 8$

$K_{av} \sim 12$

$K_{av} \sim 16$

No interfacial layer can be confirmed with Si/TiN/W
nMOSFET with EOT of 0.62nm

Gate-Channel Capacitance [µF/cm²]

FGA 800°C 30min
L / W = 10 / 10µm

- 10kHz
- 100kHz
- 1MHz

EOT=0.62nm

No frequency dispersion

Electron Mobility [cm²/Vsec]

EOT=0.62nm

T = 300K
N_{sub} = 3 \times 10^{16} \text{ cm}^{-3}
L / W = 10 / 10\mu m

EOT of 0.62nm and 155 cm²/Vsec at 1MV/cm can be achieved
Benchmark of La-silicate dielectrics

Gate leakage is two orders of magnitude lower than that of ITRS

Electron mobility is comparable to record mobility with Hf-based oxides

This work (MIPS Stacks)

Open : Hf-based oxides

T. Ando et al., IEDM2009

Electron Mobility [cm²/V·sec]
Metal (Silicide) S/D
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- $V_t$ and $I_{ON}$ variation
- GIDL

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
**Surface or interface control**

**Diffusion species:** **metal atom** (Ni, Co)
- Rough interface at silicide/Si
  - Excess silicide formation
  - Different $\phi_{Bn}$ presented at interface
  - Process temperature dependent composition

**Diffusion species:** **Si atom** (Ti)
- Surface roughness increases
  - Line dependent resistivity change

---

Annealing: 650 °C
Si(001) sub. Epitaxial NiSi$_2$


CoSi$_2$ NiSi TiSi$_2$

Top view
Line width of 0.1 µm

Unwanted leakage current

- Edge leakage current at periphery
- Generation current due to defects in substrate

Variable leakage current in smaller contact

Specification for metal silicide S/D

- Atomically flat interface with smooth surface
- Suppressed leakage current
- Stability of silicide phase and interface in a wide process temperature

Annealing: 500 °C

\[ V_{\text{app}} = 0.2V \]

\[ \phi_{Bn} = \sim 0.57 \text{ eV} \]
Deposition of Ni-Si mixed films from NiSi$_2$ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
SEM views of silicide/Si interfaces

- **Ni source**
  - Rough interfaces
  - Consumed Si substrate
  - Thickness increase ~100 nm

- **NiSi₂ source**
  - Atomically flat interfaces
  - No Si consumption
  - Temperature-independent
Ideal characteristics ($n = 1.00$, suppressed leakage current)

- Flat interface and No Si substrate consumption
- No defects in Si substrate

Schottky diode structures

Ni source

NiSi$_2$ source

Suppressed reverse leakage current

<table>
<thead>
<tr>
<th>Source</th>
<th>$\phi_B$ (eV)</th>
<th>$n$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>0.676</td>
<td>1.08</td>
</tr>
<tr>
<td>NiSi$_2$</td>
<td>0.659</td>
<td>1.00</td>
</tr>
</tbody>
</table>

RTA: 500°C, 1min
Wire channel
Suppression of subthreshold leakage by surrounding gate structure

Planar

Surrounding gate
Because of off-leakage control,

Planar $\rightarrow$ Fin $\rightarrow$ Nanowire

Planar FET

Fin FET

Nanowire FET
Nanowire structures in a wide meaning

- Fin
- Tri-gate
- Ω-gate
- All-around
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of $I_{OFF}$
3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3x3 Si wire

4 channels can be used
Device fabrication

Si/Si$_{0.8}$Ge$_{0.2}$ superlattice epitaxy on SOI

Anisotropic etching of these layers

Isotropic etching of SiGe

The NW diameter is controllable down to 5 nm by self limited oxidation.

Gate depositions
- HfO$_2$ (3nm)
- TiN (10nm)
- Poly-Si (200nm)

Gate etching

S/D implantation
Spacer formation
Activation anneal
Salicidation

Process Details:
C. Dupre et al.,
3D-stacked Si NWs with Hi-$k$/MG

- Wire direction: <110>
- 50 NWs in parallel
- 3 levels vertically-stacked
- Total array of 150 wires
- EOT $\sim$2.6 nm

C. Dupre et al., IEDM Tech. Dig., p.749, 2008
SiNW FET Fabrication

S/D & Fin Patterning

Sacrificial Oxidation

Oxide etch back

SiN sidewall support formation

Gate Oxidation & Poly-Si Deposition
Gate Lithography & RIE Etching
Gate Sidewall Formation
Ni SALISIDE Process (Ni 9nm / TiN 10nm)

Backend

Standard recipe for gate stack formation
Recent results to be presented by ESSDERC 2010 next week in Seville.

Wire cross-section: 20 nm X 10 nm

---

On/Off $>10^6$, 60uA/wire

$L_g = 65\text{nm}, \, T_{ox} = 3\text{nm}$
Bench Mark

- **Gate Length (nm)**
- **$I_{ON} (\mu A / wire)$**

- **nMOS**
- **pMOS**

VDD: 1.0~1.5 V

- **Our Work**

- 102µA (10x20)

- (16) (10)
- (34) (13)
- (8) (10)
- (9x14) (12)
- (13x20) (12)
- (12x19) (5)
- (10) (30)
- (3) (19)

括弧内は寸法を示す
$I_{ON}/I_{OFF}$ Bench mark

Planer FET
- S. Kamiyama, IEDM 2009, p. 431
- P. Packan, IEDM 2009, p. 659

Si nanowire FET
- Y. Jiang, VLSI 2008, p. 34
- H.-S. Wong, VLSI 2009, p. 92
- S. Bangsaruntip, IEDM 2009, p. 297
- C. Dupre, IEDM 2008, p. 749
- S.D. Suk, IEDM 2005, p. 735
- G. Bidel, VLSI 2009, p. 240

\[
\begin{align*}
I_{OFF} & \propto nA/\mu m \\
I_{ON} & \propto \mu A/\mu m
\end{align*}
\]

$L_g=500\sim65\text{nm}$
Electron Density
\((x10^{19} \text{cm}^{-3})\)

Distance from SiNW Surface (nm)

Edge portion

Flat portion

(a) Metal

12 nm

19 nm

SiO₂

44 %

(b) Inversion areal ratio: 29 %

12 nm

39 nm

\(V_g = 1 \text{V}\)
Primitive estimation!

- SiNW (12nm □ 19nm)
- Small EOT for high-k (33)
- P-MOS improvement (26)
- Low S/D resistance (20)
- (15)
- Compact model
- Assumption
  \[ I_{ON} = \frac{L}{1 \mu m} \cdot \frac{L}{0.5} \cdot \frac{T_{ox}}{-1} \]

- # of wires /1μm

- FD
- ITRS
- MG
Our roadmap for R & D
Source: H. Iwai, IWJT 2008

Current Issues
Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Thank you for your attention!