Materials and Structures for Future nano CMOS

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Hiroshi Iwai,
Tokyo Institute of Technology
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
Mechanism of MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

Surface Potential (Negative direction)

0 bias for gate

Positive bias for gate
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

SiO₂

Si

Al Gate

Drain

Si/SiO₂ Interface is exceptionally good
1970,71: 1st generation of LSIs

1kbit DRAM     Intel 1103     4bit MPU     Intel 4004
2011

Most recent SD Card

Lexar Professional

128GB

133x Speed
Most Recent SD Card

128GB (Bite)
= 128G X 8bit = 1024Gbit
= 1.024T(Tera)bit

1T = 10^{12} = 1Trillion

World Population : 6 Billion
Brain Cell : 10〜100 Billion
Stars in Galaxy : 100 Billion
Most Recent SD Card

Lexar Professional

128GB
133x Speed

Galaxy Image
2.4cm X 3.2cm X 0.21cm
Volume : 1.6cm³  Weight 2g
Voltage 2.7 - 3.6V

Old Vacuum Tube:
5cm X 5cm X 10cm, 100g, 100W

1Tbit = 10k X 10k X 10k bit

Volume = 0.5km X 0.5km X 1km
= 0.25 km³ = 0.25X10^{12}cm³

Weight = 0.1 kg X 10^{12} = 0.1X10^9 ton = 100 Mton
Power = 0.1 kW X 10^{12} = 50 TW

Supply Capability of Tokyo Electric Power Company: 55 BW
So, progress of IC technology is most important for the power saving!
Downsizing of the components has been the driving force for circuit evolution.

<table>
<thead>
<tr>
<th>Year</th>
<th>Device</th>
<th>1900</th>
<th>1950</th>
<th>1960</th>
<th>1970</th>
<th>2000</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Vacuum Tube</td>
<td>10 cm</td>
<td>cm</td>
<td>mm</td>
<td>10 µm</td>
<td>100 nm</td>
</tr>
<tr>
<td></td>
<td>Transistor</td>
<td>10^{-1}m</td>
<td>10^{-2}m</td>
<td>10^{-3}m</td>
<td>10^{-5}m</td>
<td>10^{-7}m</td>
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</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
5 nm gate length CMOS Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC

IEDM, 2003
Question:
How far we can go with downscaling?
Surface Potential (Negative direction)

0 bias for gate

Tunneling

@\( V_g = 0V \), Transistor cannot be switched off
Limitation for MOSFET operation

Prediction now!

Tunneling distance

3 nm

$L_g = \text{Sub-3 \, nm?}$

Below this, no one knows future!
How far can we go for production?

**Past**
- 0.7 times per 3 years
- In 40 years: 18 generations,
  Size 1/300, Area 1/100,000
- 1970年
- $10 \mu m \rightarrow 8 \mu m \rightarrow 6 \mu m \rightarrow 4 \mu m \rightarrow 3 \mu m \rightarrow 2 \mu m \rightarrow 1.2 \mu m \rightarrow 0.8 \mu m \rightarrow 0.5 \mu m \rightarrow 0.35 \mu m \rightarrow 0.25 \mu m \rightarrow 180 \text{nm} \rightarrow 130 \text{nm} \rightarrow 90 \text{nm} \rightarrow 65 \text{nm} \rightarrow 45 \text{nm} \rightarrow 32 \text{nm}$

**Future**
- At least 4,5 generations to 8nm
- Hopefully 8 generations to 3nm
Subthreshold leakage current of MOSFET

- $V_{g}=0V$
- Subthreshold leakage current of MOSFET
- $I_{on}$
- $I_{off}$
- ON
- OFF
- $V_{th}$ (Threshold Voltage)
Vth cannot be decreased anymore

significant I_{off} increase

Vth: 300mV → 100mV
I_{off} increases with 3.3 decades

(300 – 100)mV/(60mV/dec) = 3.3 dec

Subthreshold slope (SS)
= (Ln10)(kT/q)(C_{ox}+C_D+C_{it})/C_{ox}
> ~ 60 mV/decade at RT

SS value:
Constant and does not become small with down-scaling
Subthreshold leakage current of MOSFET

Subthreshold leakage current is OK at Single Tr. level but not OK for Billions of Trs.

Ion
loff

Vg=0V

Subthreshold region

Vth (Threshold Voltage)
The limit is different depending on application.
Scaling Method: by R. Dennard in 1974

W_{\text{dep}}: \text{Space Charge Region (or Depletion Region) Width}

W_{\text{dep}} \text{ has to be suppressed}

Otherwise, large leakage between S and D

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

By the scaling, W_{\text{dep}} is suppressed in proportion, and thus, leakage can be suppressed.

Good scaled I-V characteristics

K=0.7 for example

X, Y, Z: K, V: K, Na: 1/K

W_{\text{dep}} \propto \sqrt{V/Na}

I: K

Leakage current
Down scaling is the most effective way of Power saving.

The down scaling of MOSFETs is still possible for another 10 years!

3 important technological items for DS.

New materials
1. Thinning of high-k beyond 0.5 nm
2. Metal S/D

New structures
3. Wire channel
1. High-k beyond 0.5 nm
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
There is a solution! To use high-k dielectrics

Thin gate SiO$_2$

K=4  Almost the same electric characteristics

Thick gate high-k dielectrics

K=20  Thick Small leakage Current

However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO$_2$!
### Choice of High-k elements for oxide

| Candidates | Unstable at Si interface | Gas or liquid at 1000 K | Radio active | He | B | C | N | O | F | Ne |
|---|---|---|---|---|---|---|---|---|---|---|---|
| H | Li | Be | Mg | Na | Ca | Sc | Ti | V | Cr | Mn | Fe | Co | Ni | Cu | Zn | Ga | Ge | As | Se | Br | Kr |
| Si + MOₓ M + SiO₂ | Si + MOₓ MSiₓ + SiO₂ | Si + MOₓ M + MSiₓOᵧ |

- HfO₂ based dielectrics are selected as the first generation materials, because of their merit in:
  1) band-offset, 2) dielectric constant, 3) thermal stability.

- La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

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R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band Discontinuity [eV]

Dielectric Constant $\varepsilon(0)$

XPS measurement by Prof. T. Hattori, INFOS 2003
High-k gate insulator MOSFETs for Intel: EOT=1nm

HfO$_2$ based high-k
EOT can be reduced further beyond 0.5 nm by using direct contact to Si by choosing appropriate materials and processes.
Cluster tool for high-k thin film deposition

- **Preparation Room**
- **E-Beam Evaporation**: 8 different target
- **Flash Lamp**: Anneal
- **Robot Room**
- **Sputter for metal**: 5 different target
- **Micro to mille-seconds**
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

\[\text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2\]

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Trans. ECS 11, 319

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Gate Leakage vs EOT, (Vg=|1|V)

- Al2O3
- HfAlO(N)
- HfO2
- HfSiO(N)
- HfTaO
- La2O3
- Nd2O3
- Pr2O3
- PrSiO
- PrTiO
- SiON/SiN
- Sm2O3
- SrTiO3
- Ta2O5
- TiO2
- ZrO2(N)
- ZrSiO
- ZrAlO(N)
La$_2$O$_3$ at 300°C process make sub-0.4 nm EOT MOSFET

**EOT=0.37nm**

![](chart.png)

- EOT=0.37nm
- EOT=0.40nm
- EOT=0.48nm

W/L = 50µm / 2.5µm

Vth=-0.06V

Vth=-0.05V

Vth=-0.04V

0.48 → 0.37nm Increase of Id at 30%
However, high-temperature anneal is necessary for the good interfacial property

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
A small $D_{it}$ of $1.6 \times 10^{11}$ cm$^{-2}$/eV, results in better electron mobility.
Physical mechanisms for small Dit

- silicate-reaction-formed fresh interface
- stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress


Increasing EOT caused by high temperature annealing can be dramatically suppressed by Silicon masked stacks.
La$_2$O$_3$  

$W$  

Si/TiN/W  

TiN/W  

Kav $\sim$ 8  

Kav $\sim$ 12  

Kav $\sim$ 16  

No interfacial layer can be confirmed with Si/TiN/W
nMOSFET with EOT of 0.62nm

EOT of 0.62nm and 155 cm²/Vsec at 1MV/cm can be achieved
Benchmark of La-silicate dielectrics

Gate leakage is two orders of magnitude lower than that of ITRS

Electron mobility is comparable to record mobility with Hf-based oxides

T. Ando et al., IEDM2009
Metal (Silicid e) S/D
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- $V_t$ and $I_{ON}$ variation
- GIDL

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Surface or interface control

**Diffusion species:** metal atom (Ni, Co)
- Rough interface at silicide/Si
  - Excess silicide formation
  - Different $\phi_{Bn}$ presented at interface
- Process temperature dependent composition

**Diffusion species:** Si atom (Ti)
- Surface roughness increases
- Line dependent resistivity change

Annealing: 650 °C

Si(001) sub. Epitaxial NiSi$_2$

CoSi$_2$, NiSi, TiSi$_2$

Top view

Line width of 0.1 µm

Aglomerated


**Unwanted leakage current**

- Edge leakage current at periphery
- Generation current due to defects in substrate

**Variable leakage current in smaller contact**

**Specification for metal silicide S/D**

- Atomically flat interface with smooth surface
- Suppressed leakage current
- Stability of silicide phase and interface in a wide process temperature

Annealing: 500 °C

\[ V_{\text{app}} = -0.2 \text{V} \]

\[ \phi_{\text{Bn}} = \approx 0.57 \text{ eV} \]
Deposition of Ni-Si mixed films from NiSi$_2$ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
SEM views of silicide/Si interfaces

Ni source (50nm)

NiSi₂ source (50nm)

Ni source

- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

NiSi₂ source

- Atomically flat interfaces
- No Si consumption
- Temperature-independent
Ideal characteristics ($n = 1.00$, suppressed leakage current)

**Suppressed reverse leakage current**
- Flat interface and No Si substrate consumption
- No defects in Si substrate
Wire channel
Suppression of subthreshold leakage by surrounding gate structure

Planar

Surrounding gate
Because of off-leakage control, planar FETs evolve into FinFETs and eventually nanowire FETs.

Planar FET

Fin FET

Nanowire FET
Nanowire structures in a wide meaning

Fin

Tri-gate

Ω-gate

Nanowire
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of $I_{OFF}$
3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

By Prof. Shiraishi of Tsukuba univ.

4 channels can be used
Device fabrication

Si/Si<sub>0.8</sub>Ge<sub>0.2</sub>
superlattice epitaxy on SOI

Anisotropic etching of these layers

Isotropic etching of SiGe

The NW diameter is controllable down to 5 nm by self limited oxidation.

Gate depositions
HfO<sub>2</sub> (3nm)
TiN (10nm)
Poly-Si (200nm)

Gate etching

S/D implantation
Spacer formation
Activation anneal
Salicidation

Process Details:
C. Dupre et al.,
3D-stacked Si NWs with Hi-$k$/MG

Wire direction: $\langle 110 \rangle$
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT $\sim 2.6$ nm

C. Dupre et al.,
SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oxide etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)

Standard recipe for gate stack formation
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off > 10^6, 60uA/wire

L_g = 65nm, T_{ox} = 3nm
Bench Mark

$I_{ON} (\mu A / \text{wire})$

- nMOS
- pMOS

Gate Length (nm)

V$_{DD}$: 1.0~1.5 V

Our Work
This work
Effective Electron Mobility (cm²/Vs) vs. Inversion Carrier Density (cm⁻²)

- **A₁ (12x19) \( h_{NW} \times w_{NW} \) (nm²)**
  - **A₂ (12x28)**
  - **B (20x10)**

**SOI Planar**
- **\( T_{SOI} = 28 \text{ nm} \)**

**SOI planar**
- **W = 1 \text{ μm}**
- **\( T_{SOI} = 28 \text{ nm} \)**

**Dimensions**
- **A₁**: 20 nm × 19 nm
- **A₂**: 12 nm × 28 nm
- **B**: 20 nm × 10 nm

**Images**
- **A**: 20 nm scale bar
- **B**: 10 nm scale bar
(a) Metal
12 nm
19 nm SiO₂

(b) Inversion areal ratio: 29%
39 nm

Electron Density
(x\times10^{19}\text{cm}^{-3})

Edge portion
Flat portion

Distance from SiNW Surface (nm)
Primitive estimation!

- SiNW (12nm × 19nm)
- Small EOT for high-k (33)
- P-MOS improvement (26)
- Low S/D resistance (20)
- # of wires /1µm (15)
- Assumption: $I_{ON} \propto L_g^{-0.5} T_{ox}^{-1}$

Compact model

ITRS

Nanowire
Our roadmap for R & D

Source: H. Iwai, IWJT 2008

Current Issues

Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Thank you for your attention!