Miniaturization and future prospects of Si devices

G-COE PICE International Symposium and IEEE EDS Minicolloquium on Advanced Hybrid Nano Devices: Prospects by World’s Leading Scientists

October 4, 2011

Hiroshi Iwai,
Tokyo Institute of Technology
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power
consumption
Mechanism of MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

Surface Potential (Negative direction)

0 bias for gate

Positive bias for gate
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

SiO₂

Si

Si/SiO₂ Interface is exceptionally good

Al Gate
Drain
1970,71: 1st generation of LSIs

1kbit DRAM  Intel 1103  4bit MPU  Intel 4004
2011
Most recent SD Card
Most Recent SD Card

128GB (Bite)
= 128G X 8bit = 1024Gbit
= 1.024T(Tera)bit

1T = 10^{12} = 1Trillion

World Population : 6 Billion
Brain Cell : 10〜100 Billion
Stars in Galaxy : 100 Billion
Most Recent SD Card
2.4cm × 3.2cm × 0.21cm

Volume: 1.6 cm³  Weight: 2g

Voltage: 2.7 - 3.6V

Old Vacuum Tube:
5cm × 5cm × 10cm, 100g, 100W

1 Tbit = 10k × 10k × 10k bit

Volume = 0.5 km × 0.5 km × 1 km
= 0.25 km³ = 0.25 × 10¹² cm³

Weight = 0.1 kg × 10¹² = 0.1 × 10⁹ ton = 100 M ton

Power = 0.1 kW × 10¹² = 50 TW

Supply Capability of Tokyo Electric Power Company: 55 BW
So, progress of IC technology is most important for the power saving!
Downsizing of the components has been the driving force for circuit evolution.

<table>
<thead>
<tr>
<th>Year</th>
<th>Device</th>
<th>Size</th>
<th>Size (m)</th>
<th>Size (µm)</th>
<th>Size (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1900</td>
<td>Vacuum Tube</td>
<td>10 cm</td>
<td>10^-1 m</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1950</td>
<td>Transistor</td>
<td>cm</td>
<td>10^-2 m</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1960</td>
<td>IC</td>
<td>mm</td>
<td>10^-3 m</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1970</td>
<td>LSI</td>
<td>10 µm</td>
<td>10^-5 m</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2000</td>
<td>ULSI</td>
<td>100 nm</td>
<td>10^-7 m</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. **Reduce Capacitance**
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. **Increase number of Transistors**
   - Parallel processing
     - Increase circuit operation speed

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Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.
Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1µm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5µm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25µm:</td>
<td>Direct-tunneling of gate SiO₂</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1µm:</td>
<td>‘0.1µm brick wall’(various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
Transistor Scaling Continues

90nm node

65nm node

45nm node

32nm node

22nm node

Lg=10nm

Lg=50nm

Lg=35nm

Lg=25nm

Lg=15nm

~30% every two years

ITRS 2003 (HP)

Qi Xinag, ECS 2004, AMD
5 nm gate length CMOS
Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC
IEDM, 2003
@Vg=0V, Transistor cannot be switched off
Tunneling distance 3 nm

Limitation for MOSFET operation

Prediction now!

Lg = Sub-3 nm?

Below this, no one knows future!
Prediction now!

Limitation for MOSFET operation

Tunneling distance
3 nm

Lg = Sub-3 nm?

Below this, no one knows future!

Ultimate limitation

Atom distance
0.3 nm

No one can make a MOSET below this size!
Question:
How far we can go with downscaling?
How far can we go for production?

**Past** 0.7 times per 3 years

1970年

10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm → 0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

**Now**

In 40 years: 18 generations, Size 1/300, Area 1/100,000

**Future**

→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

- At least 4,5 generations to 8nm
- Hopefully 8 generations to 3nm
Subthreshold leakage current of MOSFET

$V_{th}$ (Threshold Voltage)

$V_{g}=0V$

Subthreshold region

$I_{on}$

$I_{off}$

Subthreshold Leakage Current

OFF

ON

21
Vth cannot be decreased anymore

significant Ioff increase

Vth: 300mV → 100mV
Ioff increases with 3.3 decades

(300 - 100)mV/(60mV/dec) = 3.3 dec

Subthreshold slope (SS)
= (Ln10)(kT/q)(Cox + CD + Cit)/Cox
> ~ 60 mV/decade at RT

SS value:
Constant and does not become small with down-scaling
Subthreshold leakage current of MOSFET

Subthreshold leakage current of MOSFET is OK at single transistor level but not OK for billions of transistors.
The limit is different depending on application.
Scaling Method: by R. Dennard in 1974

**W_{dep}:** Space Charge Region (or Depletion Region) Width

W_{dep} has to be suppressed. Otherwise, large leakage between S and D.

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

By the scaling, W_{dep} is suppressed in proportion, and thus, leakage can be suppressed.

Good scaled I-V characteristics

K=0.7 for example

\[ W_{dep} \propto \sqrt{V/Na} \]

\[ X, Y, Z : K, \quad V : K, \quad Na : 1/K \]
Down scaling is the most effective way of Power saving.

The down scaling of MOSFETs is still possible for another 10 years!

3 important technological items for DS.

New materials
1. Thinning of high-k beyond 0.5 nm
2. Metal S/D

New structures
3. Wire channel
1. High-k beyond 0.5 nm
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
There is a solution! To use high-k dielectrics

**K**: Dielectric Constant

- Thin gate SiO₂
  - \( K = 4 \)
  - Almost the same electric characteristics
- Thick gate high-k dielectrics
  - \( K = 20 \)
  - Thick
  - Small leakage Current

However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO₂!
Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
<th>He</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Li Be</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Na Mg</td>
<td>Si + MO\textsubscript{X} M + SiO\textsubscript{2}</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Si + MO\textsubscript{X} MSi\textsubscript{X} + SiO\textsubscript{2}</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Si + MO\textsubscript{X} M + MSi\textsubscript{X}O\textsubscript{Y}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>K Ca Sc</td>
<td></td>
<td>Al Si</td>
<td>P S Cl Ar</td>
</tr>
<tr>
<td>Rh Sr Y Zr</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cs Ba</td>
<td>Hf</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fr Ra</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Unstable at Si interface

- Si + MO\textsubscript{X} M + SiO\textsubscript{2}
- Si + MO\textsubscript{X} MSi\textsubscript{X} + SiO\textsubscript{2}
- Si + MO\textsubscript{X} M + MSi\textsubscript{X}O\textsubscript{Y}

La\textsubscript{2}O\textsubscript{3} based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

HfO\textsubscript{2} based dielectrics are selected as the first generation materials, because of their merit in:
1) band-offset,
2) dielectric constant,
3) thermal stability.

Choice of High-k elements for oxide

- R. Hauser, IEDM Short Course, 1999

- Sm Eu Gd Tb Dy Ho Er Tm Yb Lu
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band offset

Oxide

Si

Band Discontinuity [eV]

0 1 0 2 0 3 0 4 0 5 0

0 10 20 30 40 50

Dielectric Constant $\varepsilon(0)$

XPS measurement by Prof. T. Hattori, INFOS 2003
High-k gate insulator MOSFETs for Intel: EOT=1nm

HfO$_2$ based high-k
For the past 45 years SiO$_2$ and SiON for gate insulator.

- Today EOT=1.0nm
- EOT=0.7~0.8 nm (EOT Limit)
- One order of Magnitude
- Introduction of High-k
- Still SiO$_2$ or SiON is used at Si interface

EOT can be reduced further beyond 0.5 nm by using direct contact to Si by choosing appropriate materials and processes.
Cluster tool for high-k thin film deposition
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ ⇋ HfO$_2$ + Si + 2O* ⇋ HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Trans. ECS 11, 319

SiO$_x$-IL is formed after annealing
Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ can achieve direct contact of high-k/Si
La$_2$O$_3$ at 300$^\circ$C process make sub-0.4 nm EOT MOSFET

EOT=0.37nm

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

0.48 $\rightarrow$ 0.37nm Increase of $I_d$ at 30%
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
A small $D_{it}$ of $1.6 \times 10^{11}$ cm$^{-2}$/eV, results in better electron mobility.
Physical mechanisms for small $D_{it}$

- Silicate-reaction-formed fresh interface
- Stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA $800^\circ C$ is necessary to reduce the interfacial stress


Increasing EOT caused by high temperature annealing can be dramatically suppressed by Silicon masked stacks.
No interfacial layer can be confirmed with Si/TiN/W.
nMOSFET with EOT of 0.62nm

EOT of 0.62nm and 155 cm²/Vsec at 1MV/cm can be achieved
Benchmark of La-silicate dielectrics

Gate leakage is two orders of magnitude lower than that of ITRS

Electron mobility is comparable to record mobility with Hf-based oxides
Metal (Silicide) S/D
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- $V_t$ and $I_{ON}$ variation
- GIDL

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Surface or interface control

**Diffusion species:** metal atom (Ni, Co)

Rough interface at silicide/Si
- Excess silicide formation
- Different $\phi_B$ presented at interface
- Process temperature dependent composition

**Diffusion species:** Si atom (Ti)

Surface roughness increases
- Line dependent resistivity change

Annealing: 650 °C
Si(001) sub. Epitaxial NiSi$_2$

CoSi$_2$ NiSi TiSi$_2$

Top view
Line width of 0.1 μm
Aglomeration


Unwanted leakage current

- Edge leakage current at periphery
- Generation current due to defects in substrate

Variable leakage current in smaller contact

Specification for metal silicide S/D

- Atomically flat interface with smooth surface
- Suppressed leakage current
- Stability of silicide phase and interface in a wide process temperature

Annealing: 500 °C

$V_{\text{app}} = -0.2 \text{V}$

$\phi_{Bn} = \sim 0.57 \text{ eV}$

Current density (A/cm²)

Length of a contact side (µm)

Ni silicide/Si diodes
Deposition of Ni-Si mixed films from NiSi₂ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
- *n*-type Si substrate, Si(100) with 400 nm SiO₂ isolation
  Doping concentration: \(3 \times 10^{15} \text{ cm}^{-3}\)

- SPM and HF cleaning

- Diode patterning by photolithography and BHF etching of SiO₂

- Deposition of 10-nm-thick NiSi₂ and Ni sources by RF sputtering in Ar atmosphere

- Ni silicidation by Rapid Thermal Annealing (RTA) in N₂ atmosphere

- Al contact deposition on substrate backside by thermal evaporation

- Measurement of electrical characteristics
- SEM and TEM observation
- XRD and XPS analysis
SEM views of silicide/Si interfaces

**Ni source (50nm)**
- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

**NiSi₂ source (50nm)**
- Atomically flat interfaces
- No Si consumption
- Temperature-independent
Ideal characteristics \((n = 1.00, \text{ suppressed leakage current})\)

**Suppressed reverse leakage current**

- Flat interface and No Si substrate consumption
- No defects in Si substrate
- Ni-rich phases in the silicide layer are maintained with NiSi$_2$ source

- No distinct structure change at the interface

  - Stable $\phi_{Bn}$ and $n$-factor
  - No structural effect for silicidation
Wire channel
Suppression of subthreshold leakage by surrounding gate structure

Planar

Surrounding gate
Because of off-leakage control,

Planar $\rightarrow$ Fin $\rightarrow$ Nanowire

Leakage current

Planar FET

Fin FET

Nanowire FET
Nanowire structures in a wide meaning

- **Fin**
- **Tri-gate**
- **Ω-gate**
- **Nanowire**
Nanowire FET

ITRS 2009
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process

2. Good controllability of $I_{\text{OFF}}$

3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires

Leakage current

Gate: OFF
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Device fabrication

Si/Si$_{0.8}$Ge$_{0.2}$ superlattice epitaxy on SOI

Anisotropic etching of these layers

Isotropic etching of SiGe

The NW diameter is controllable down to 5 nm by self limited oxidation.

Gate depositions
HfO$_2$ (3nm)
TiN (10nm)
Poly-Si (200nm)

S/D implantation
Spacer formation
Activation anneal
Salicidation

Standard Back-End of-Line Process

Process Details:
C. Dupre et al.,
3D-stacked Si NWs with Hi-\(k\)/MG

Wire direction : <110>

50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT \(\sim\)2.6 nm

C. Dupre et al.,
SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oxide etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

Standard recipe for gate stack formation
(a) SEM image of Si NW FET (Lg = 200nm) 
(b) high magnification observation of gate and its sidewall.
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off $>10^6$, 60uA/wire

$L_g=65nm$, $T_{ox}=3nm$
Bench Mark

Our Work

Gate Length (nm)

$V_{DD}$: 1.0~1.5 V

$I_{ON}$ (µA / wire)

nMOS

pMOS
$I_{ON}/I_{OFF}$ Benchmark

- **Planer FET**
  - S. Kamiyama, IEDM 2009, p. 431
  - P. Packan, IEDM 2009, p. 659
  - Voltage range: 1.0 ~ 1.1V

- **Si Nano Wire FET**
  - Y. Jiang, VLSI 2008, p. 34
  - H.-S. Wong, VLSI 2009, p. 92
  - S. Bangsaruntip, IEDM 2009, p. 297
  - C. Dupre, IEDM 2008, p. 749
  - S.D. Suk, IEDM 2005, p. 735
  - G. Bidel, VLSI 2009, p. 240
  - Voltage range: 1.2 ~ 1.3V

- $L_g = 500 \sim 65$ nm
Distance from SiNW Surface (nm)

Electron Density
\( \times 10^{19} \text{cm}^{-3} \)

Edge portion
Flat portion

Inversion areal ratio: 29%
Primitive estimation!

- Small EOT for high-k (33)
- P-MOS improvement (26)
- Low S/D resistance (20)
- Low S/D resistance (15)
- # of wires /1µm

Compact model

SiNW (12nm □ 19nm)

Assumption

\[ I_{ON} \propto L_g^{-0.5} T_{ox}^{-1} \]

Year

S/D resistance

P-MOS improvement

Small EOT for high-k

Compact model

SiNW
Intel announcement

Transistor Innovations Enable Technology Cadence

- 2003: 90 nm (Invented SiGe Strained Silicon)
- 2005: 65 nm (2nd Gen. SiGe Strained Silicon)
- 2007: 45 nm (Invented Gate-Last High-k Metal Gate)
- 2009: 32 nm (2nd Gen. Gate-Last High-k Metal Gate)
- 2011: 22 nm (First to Implement Tri-Gate)

Strained Silicon

High k Metal gate

Tri-Gate
22nm Silicon Technology Breakthrough Benefits Broad Range of Intel Architecture Devices

New 22nm 3-D transistors deliver unprecedented performance improvement and power reduction for Intel’s product portfolio

- This benefits smallest handhelds to powerful cloud-based servers
- 37% performance increase at low voltage vs. 32nm planar transistors*
- Consumes only half the power at the same performance level as 2-D transistors on 32nm planar chips*
Our roadmap for R & D

Source: H. Iwai, IWJT 2008

Current Issues

Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Thank you for your attention!