Past and Future of Micro/Nano Electronics

Zhejiang Technology and Science University
Hangzhou, China

October 31, 2011

Hiroshi Iwai,
Tokyo Institute of Technology
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
Institute Overview

Established in 1881 → 130th anniversary in 2011
3 undergraduate schools
   School of Science, School of Engineering, School of Bioscience and Biotechnology
7 graduate schools
   Science and Engineering Science, Science and Engineering Technology,
   Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
   Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

<table>
<thead>
<tr>
<th></th>
<th>Undergraduate</th>
<th>Graduate</th>
<th>Master’s</th>
<th>Doctoral</th>
<th>Teaching Staff</th>
<th>Student/Instructor</th>
<th>Staff</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tokyo Inst.</td>
<td>5,000</td>
<td>5,000</td>
<td>3,500</td>
<td>1,500</td>
<td>1,200</td>
<td>8.3</td>
<td>550</td>
</tr>
<tr>
<td>Per Year</td>
<td>1,200</td>
<td>1,800</td>
<td>500</td>
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</tbody>
</table>
Asia 847
Europe 78
Africa 16
North America 12
South America 24
Oceania 5

Total 982
(As of May. 1, 2005)
研究風景
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906.

Thermal electrons from cathode controlled by grid bias.

Same mechanism as that of transistor.
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928
Capacitor structure with notch

Negative bias

No current

Positive bias

Current flows
Mechanism of MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

Surface Potential (Negative direction)

0 bias for gate

Positive bias for gate

Electron flow
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator.

Drain Current was several orders of magnitude smaller than expected.

Even Shockley!
However, they found amplification phenomenon when investigating Ge surface when putting needles. This is the 1st Transistor:

Not Field Effect Transistor, But Bipolar Transistor (another mechanism)

**1947: 1st transistor**

J. Bardeen  W. Bratten,

Bipolar using Ge

W. Shockley
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si

Source

Drain

Al Gate

Si

SiO₂

Al

Si/SiO₂ Interface is exceptionally good
1970,71: 1st generation of LSIs

1kbit DRAM   Intel 1103   4bit MPU   Intel 4004
2011
Most recent SD Card
Most Recent SD Card

128GB (Bite)
= 128G X 8bit = 1024Gbit
= 1.024T(Tera)bit

1T = 10^{12} = 1Trillion

World Population : 6 Billion
Brain Cell : 10〜100 Billion
Stars in Galaxy : 100 Billion
Most Recent SD Card
2.4cm X 3.2cm X 0.21cm
Volume : 1.6cm³  Weight: 2g
Voltage: 2.7 - 3.6V

Old Vacuum Tube:
5cm X 5cm X 10cm, 100g, 100W

1Tbit = 10k X 10k X 10k bit

Volume = 0.5km X 0.5km X 1km
= 0.25 km³ = 0.25 X 10¹² cm³

Weight = 0.1 kg X 10¹² = 0.1 X 10⁹ ton = 100 Mton
Power = 0.1 kW X 10¹² = 50 TW

Supply Capability of Tokyo Electric Power Company: 55 BW
So, progress of IC technology is most important for the power saving!
Downsizing of the components has been the driving force for circuit evolution.

<table>
<thead>
<tr>
<th>Year</th>
<th>Vacuum Tube</th>
<th>Transistor</th>
<th>IC</th>
<th>LSI</th>
<th>ULSI</th>
</tr>
</thead>
<tbody>
<tr>
<td>1900</td>
<td>10 cm</td>
<td>cm</td>
<td>mm</td>
<td>10 μm</td>
<td>100 nm</td>
</tr>
<tr>
<td>1950</td>
<td>10^{-1}m</td>
<td>10^{-2}m</td>
<td>10^{-3}m</td>
<td>10^{-5}m</td>
<td>10^{-7}m</td>
</tr>
<tr>
<td>1960</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1970</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2000</td>
<td></td>
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</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. Reduce Capacitance
   - Reduce switching time of MOSFETs
   - Increase circuit operation speed
   - Increase clock frequency
   - Increase circuit operation speed

2. Increase number of Transistors
   - Parallel processing
     - Increase circuit operation speed

Thus, downsizing contribute to the performance increase in double ways.

Thus, downsizing of Si devices is the most important and critical issue.
Question:
How far we can go with downscaling?
Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1µm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5µm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25µm:</td>
<td>Direct-tunneling of gate SiO₂</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1µm:</td>
<td>‘0.1µm brick wall’(various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
Historically, many predictions of the limit of downsizing. VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.
Finally, there appears to be a fundamental limit of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.
Direct-tunneling effect

Gate Electrode  |  Gate Oxide | Si Substrate
Potential Barrier

Wave function  \rightarrow  Direct tunneling current

Direct tunneling leakage current start to flow when the thickness is 3 nm.
Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide

\[ \text{Vg} = 2.0 \text{V} \]

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\[ \text{Vg} = 2.0 \text{V} \]

\[ \text{Lg} = 10 \mu\text{m} \]

\[ \text{Vd} (\text{V}) \]

\[ \text{Id} (\text{mA} / \mu\text{m}) \]

\[ \text{Lg} = 5 \mu\text{m} \]

\[ \text{Vd} (\text{V}) \]

\[ \text{Id} (\text{mA} / \mu\text{m}) \]

\[ \text{Lg} = 1.0 \mu\text{m} \]

\[ \text{Vd} (\text{V}) \]

\[ \text{Id} (\text{mA} / \mu\text{m}) \]

\[ \text{Lg} = 0.1 \mu\text{m} \]

\[ \text{Vd} (\text{V}) \]
Gate leakage: \( I_g \propto \text{Gate Area} \propto \text{Gate length (Lg)} \)

Drain current: \( I_d \propto 1/\text{Gate length (Lg)} \)

\( L_g \to \text{small,} \)

Then, \( I_g \to \text{small, } I_d \to \text{large, } \)

Thus, \( I_g/I_d \to \text{very small} \)

\[
\begin{array}{cccc}
\text{Lg} = 10 \, \mu\text{m} & \text{Lg} = 5 \, \mu\text{m} & \text{Lg} = 1.0 \, \mu\text{m} & \text{Lg} = 0.1 \, \mu\text{m} \\
\end{array}
\]
Transistor Scaling Continues

Qi Xinag, ECS 2004, AMD
Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!
Some one will think for you
So, what is the limitation for downsizing?
Prediction now!

Limitation for MOSFET operation

Tunneling distance

3 nm

Lg = Sub-3 nm?

Below this, no one knows future!
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

- 1.2 nm physical SiO₂ in production (90 nm logic node)
- 0.8 nm physical SiO₂ in research transistors

By Robert Chau, IWGI 2003
So, we are now facing the limit of downsizing?
There is a solution! To use high-k dielectrics

- Thin gate SiO$_2$: $K=4$
  - Almost the same electric characteristics

- Thick gate high-k dielectrics: $K=20$
  - Thick
  - Small leakage
  - Current

However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO$_2$!
5 nm gate length CMOS
Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC
IEDM, 2003
So, again, how far we can go with downscaling?
Source Channel Drain

Gate electrode
Gate Oxid

Surface

0V
N+ - Si
P - Si
1V
N - Si

3nm

Tunneling

Surface Potential (Negative direction)

0 bias for gate

@Vg=0V, Transistor cannot be switched off
How far can we go for production?

Past | 0.7 times per 3 years | In 40 years: 18 generations, Size 1/300, Area 1/100,000

1970年
10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm → 0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

Future
→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

- At least 4.5 generations to 8nm
- Hopefully 8 generations to 3nm
Subthreshold leakage current of MOSFET

- Subthreshold leakage current of MOSFET
- $Vg=0V$
- Subthreshold region
- $Vth$ (Threshold Voltage)
- $Id$ vs $Vg$
- $Ion$ and $Ioff$
Vth cannot be decreased anymore

significant Ioff increase

Vth: 300mV $\rightarrow$ 100mV
Ioff increases with 3.3 decades

(300 - 100)mV/(60mV/dec) = 3.3 dec

Subthreshold slope (SS) = $(\ln 10)(kT/q)(C_{ox} + C_D + C_{it})/C_{ox}$
$> \sim 60$ mV/decade at RT

Log scale Id plot

Vdd down-scaling

Vdd = 0.5V  Vdd = 1.5V

Vth = 300mV  Vth = 100mV

Log Id per unit gate width (= 1\,\mu m)

10^{-3}A  10^{-4}A  10^{-5}A  10^{-6}A  10^{-7}A  10^{-8}A  10^{-9}A  10^{-10}A

Vg (V)

Vg = 0V

SS value:
Constant and does not become small with down-scaling
Subthreshold leakage current of MOSFET

Subthreshold Leakage Current

$Vg=0V$

Subthreshold region

$Vth$ (Threshold Voltage)

$Id$

$Ion$

$loff$

OFF

ON

Subthreshold Current Is OK at Single Tr. level

But not OK For Billions of Trs.
The limit is deferent depending on application.
Scaling Method: by R. Dennard in 1974

**Wdep**: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage between S and D

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

\[ W_{dep} \propto \sqrt{V/N_a} \]

\[ I : K \]

\[ X, Y, Z : K, \quad V : K, \quad N_a : 1/K \]

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

Good scaled I-V characteristics

\[ K = 0.7 \] for example
Down scaling is the most effective way of Power saving.

The down scaling of MOSFETs is still possible for another 10 years!

3 important technological items for DS.

New materials

1. Thinning of high-k beyond 0.5 nm
2. Metal S/D

New structures

3. Wire channel
1. High-k beyond 0.5 nm
There is a solution! K: Dielectric Constant
To use high-k dielectrics

Thin gate SiO₂

K=4
Almost the same electric characteristics

K=20

Thick gate high-k dielectrics

However, very difficult and big challenge!
Remember MOSFET had not been realized without Si/SiO₂!
Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active He</th>
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</thead>
<tbody>
<tr>
<td>H</td>
<td>B</td>
<td>C</td>
</tr>
<tr>
<td>Li</td>
<td>Na</td>
<td>Mg</td>
</tr>
<tr>
<td>Be</td>
<td></td>
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<tr>
<td></td>
<td>Cs</td>
<td>Ba</td>
</tr>
<tr>
<td></td>
<td>Fr</td>
<td>Ra</td>
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</table>

Unstable at Si interface
- Si + MOₓ M + SiO₂
- Si + MOₓ MSiₓ + SiO₂
- Si + MOₓ M + MSiₓOᵧ

HfO₂ based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

Choice of High-k elements for oxide

- LaCePrNdPmSmEuGdTbDyHoErTmYbLu
- AcThPaUNpPuAmCmBkCfEsFmMdNoLr

R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

XPS measurement by Prof. T. Hattori, INFOS 2003
High-k gate insulator MOSFETs for Intel: EOT=1nm

HfO₂ based high-k
For the past 45 years, SiO₂ and SiON have been used as gate insulators. Today, EOT = 1.0 nm. EOT can be reduced further beyond 0.5 nm by using direct contact to Si by choosing appropriate materials and processes.

Introduction of High-k materials, such as HfO₂, can reduce EOT to 0.5~0.7 nm. Still, SiO₂ or SiON is used at the Si interface. Direct contact of high-k and Si will further reduce EOT.

One order of magnitude improvement in power per MOSFET (P) has been achieved with advances in technology.
Cluster tool for high-k thin film deposition
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O$^*$ $\rightarrow$ HfO$_2$ + SiO$_2$

Oxygen supplied from W gate electrode

SiO$_x$-IL is formed after annealing
Oxygen control is required for optimizing the reaction

H. Shimizu, JJAP, 44, pp. 6131
D.J. Lichtenwalner, Trans. ECS 11, 319
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ can achieve direct contact of high-k/Si

La$_2$O$_3$ + Si + nO$_2$

- La$_2$SiO$_5$, La$_2$Si$_2$O$_7$,
- La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

XPS Si1s spectra

TEM image 500 °C, 30 min

1 nm
Gate Leakage vs EOT, \( (V_g=\pm |1|V) \)

- Al2O3
- HfO2
- HfAlO(N)
- HfSiO(N)
- HfTaO
- La2O3
- Nd2O3
- Pr2O3
- PrSiO
- PrTiO
- SiON/SiN
- Sm2O3
- SrTiO3
- Ta2O5
- TiO2
- ZrO2(N)
- ZrSiO
- ZrAlO(N)
La$_2$O$_3$ at 300°C process make sub-0.4 nm EOT MOSFET

**EOT=0.37nm**

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

0.48 \rightarrow 0.37\text{nm} Increase of $I_d$ at 30%
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
Physical mechanisms for small Dit

- silicate-reaction-formed fresh interface
- stress relaxation at interface by glass type structure of La silicate.

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress

A small $D_{it}$ of $1.6 \times 10^{11}$ cm$^{-2}$/eV, results in better electron mobility.
EOT growth suppression by Si coverage

Increasing EOT caused by high temperature annealing can be dramatically suppressed by Silicon masked stacks.
No interfacial layer can be confirmed with Si/TiN/W.
EOT of 0.62nm and 155 cm$^2$/Vsec at 1MV/cm can be achieved
**Benchmark of La-silicate dielectrics**

Gate leakage is two orders of magnitude lower than that of ITRS.

Electron mobility is comparable to record mobility with Hf-based oxides.

**Figure:**
- **Left Diagram:**
  - $J_g$ at $V_g = 1V$ [$A/cm^2$]
  - EOT [nm]
  - $A = 10 \times 10\mu m^2$
- **Right Diagram:**
  - Electron Mobility [cm$^2$/Vsec]
  - EOT [nm]
  - T = 300K

**Legend:**
- MIPS Stacks
- Open: Hf-based oxides
- This work (MIPS Stacks)

**References:**
- T. Ando et al., IEDM2009
Metal (Silicide) S/D
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- $V_t$ and $I_{ON}$ variation
- GIDL

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Surface or interface control

Diffusion species: metal atom (Ni, Co)
Rough interface at silicide/Si
- Excess silicide formation
- Different $\phi_B$ presented at interface
- Process temperature dependent composition

Diffusion species: Si atom (Ti)
Surface roughness increases
- Line dependent resistivity change

Annealing: 650 °C
Si(001) sub.
Epitaxial NiSi$_2$


CoSi$_2$  NiSi  TiSi$_2$

Top view

Line width of 0.1 µm
Aglomeration

Unwanted leakage current
- Edge leakage current at periphery
- Generation current due to defects in substrate

Variable leakage current in smaller contact

Specification for metal silicide S/D
- Atomically flat interface with smooth surface
- Suppressed leakage current
- Stability of silicide phase and interface in a wide process temperature
Deposition of Ni-Si mixed films from NiSi$_2$ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
SEM views of silicide/Si interfaces

Ni source (50nm)

NiSi₂ source (50nm)

Ni source

- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

NiSi₂ source

- Atomically flat interfaces
- No Si consumption
- Temperature-independent
Ideal characteristics ($n = 1.00$, suppressed leakage current)

- Suppressed reverse leakage current
  - Flat interface and No Si substrate consumption
  - No defects in Si substrate

<table>
<thead>
<tr>
<th>Source</th>
<th>$\phi_B$ (eV)</th>
<th>n</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>0.676</td>
<td>1.08</td>
</tr>
<tr>
<td>NiSi$_2$</td>
<td>0.659</td>
<td>1.00</td>
</tr>
</tbody>
</table>

RTA : 500°C, 1min
Wire channel
Suppression of subthreshold leakage by surrounding gate structure

Planar

Surrounding gate
Because of off-leakage control, Planar $\rightarrow$ Fin $\rightarrow$ Nanowire
Nanowire structures in a wide meaning

- Fin
- Tri-gate
- Ω-gate
- All-around
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process

2. Good controllability of $I_{OFF}$

3. High drive current

1D ballistic conduction

Leakage current

Multi quantum Channel

High integration of wires
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

- Energy band of Bulk Si
- Split-off band
- Heavy holes
- Light holes
- Wave vect

Energy band of 3 x 3 Si wire

- 4 channels can be used
- 300 K
- $E_g = 1.12 \text{ eV}$
- $E_L = 2.0 \text{ eV}$
- $E_x = 1.2 \text{ eV}$
- $E_v = 0.044 \text{ eV}$
- $E_{T1} = 3.4 \text{ eV}$
- $E_{T2} = 4.2 \text{ eV}$
Device fabrication

Si/Si$_{0.8}$Ge$_{0.2}$ superlattice epitaxy on SOI

Anisotropic etching of these layers

Isotropic etching of SiGe

The NW diameter is controllable down to 5 nm by self limited oxidation.

Process Details:
C. Dupre et al., IEDM Tech. Dig., p.749, 2008
3D-stacked Si NWs with Hi-\(k\)/MG

Wire direction : \(<110>\)
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT \(~2.6\) nm

C. Dupre et al.,
SiNW FET Fabrication

1. S/D & Fin Patterning
2. Sacrificial Oxidation
3. Oxide etch back
4. SiN sidewall support formation
5. Gate Oxidation & Poly-Si Deposition
6. Gate Lithography & RIE Etching
7. Gate Sidewall Formation
8. Ni SALISIDE Process (Ni 9nm / TiN 10nm)
9. Backend

Standard recipe for gate stack formation
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off $> 10^6$, 60uA/wire

$L_g = 65\text{nm}$, $T_{ox} = 3\text{nm}$
Bench Mark

Gate Length (nm)

I_{ON} (μA / wire)

V_{DD}: 1.0~1.5 V

Our Work

Our Work
$I_{\text{ON}}/I_{\text{OFF}}$ Bench mark

- **Planer FET**: 1.0~1.1V
  - S. Kamiyama, IEDM 2009, p. 431
  - P. Packan, IEDM 2009, p.659

- **Si nanowireFET**: 1.2~1.3V
  - Y. Jiang, VLSI 2008, p.34
  - H.-S. Wong, VLSI 2009, p.92
  - S. Bangsaruntip, IEDM 2009, p.297
  - C. Dupre, IEDM 2008, p. 749
  - S.D.Suk, IEDM 2005, p.735
  - G.Bidel, VLSI 2009, p.240

Diagram:
- $L_g = 500\sim 65$ nm
- $I_{\text{ON}}$ (μA/μm)
- $I_{\text{OFF}}$ (nA/μm)

This work
(a) Metal
12 nm
19 nm
SiO₂

44 %

V₉ = 1V

(b) Inversion areal ratio: 29 %

Electron Density (x10¹⁹ cm⁻³)

Distance from SiNW Surface (nm)

Edge portion

Flat portion
Primitive estimation!

![Graph showing the relationship between ION (µA/µm) and the year with various technologies and assumptions.](image)

- **SiNW (12nm - 19nm)**
- **Small EOT for high-k**
- **P-MOS improvement**
- **Low S/D resistance**
- **Compact model**
- **Assumption**
  \[ I_{ON} \propto L_g^{-0.5} \times T_{ox}^{-1} \]

**Notes:**
- # of wires /1µm
- Assumption
- ITRS
- MG
**Our roadmap for R & D**

**Source:** H. Iwai, IWJT 2008

### Current Issues

**Si Nanowire**
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

**III-V & Ge Nanowire**
- High-k gate insulator
- Wire formation technique

**CNT:**
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

**Graphene:**
- Graphene formation technique
- Suppression of off-current
  - Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Thank you for your attention!