Past and Future of Micro/Nano Electronics

Yuquan (玉泉) Campus
Zhejiang University
Hangzhou, China

October 28, 2011

Hiroshi Iwai,
Tokyo Institute of Technology
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
Institute Overview

Established in 1881 → 130th anniversary in 2011
3 undergraduate schools
   School of Science, School of Engineering, School of Bioscience and Biotechnology
7 graduate schools
   Science and Engineering Science, Science and Engineering Technology,
   Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
   Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

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<tr>
<th></th>
<th>Undergraduate</th>
<th>Graduate</th>
<th>Master's</th>
<th>Doctoral</th>
<th>Teaching Staff</th>
<th>Student/Instructor</th>
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**Total 982**

(As of May. 1, 2005)
研究風景

Deposition  Lithography  Etching

Analysis  Measurement  Annealing

Office
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Same mechanism as that of transistor
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
Capacitor structure with notch

**Negative bias**
- Gate Electrode
- Gate Insulator
- Semiconductor
- Electron

No current

**Positive bias**
- Electric field

Current flows
Mechanism of MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

Surface Potential (Negative direction)

0 bias for gate

Positive bias for gate

Electron flow
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator.

Drain Current was several orders of magnitude smaller than expected

Even Shockley!
However, they found amplification phenomenon when investigating Ge surface when putting needles. This is the 1st Transistor:

Not Field Effect Transistor, But Bipolar Transistor (another mechanism)

1947: 1st transistor

J. Bardeen  W. Bratten,  W. Shockley

Bipolar using Ge
1960: First MOSFET
by D. Kahng and M. Atalla

Top View

Si
Source

Al Gate
Drain

Si

Si/SiO₂ Interface is exceptionally good
1970,71: 1st generation of LSIs

1kbit DRAM   Intel 1103   4bit MPU   Intel 4004
2011
Most recent SD Card
Most Recent SD Card

128GB (Bite)
= 128G X 8bit = 1024Gbit
= 1.024T(Tera)bit

1T = 10^{12} = 1Trillion

World Population : 6 Billion
Brain Cell : 10～100 Billion
Stars in Galaxy : 100 Billion
Most Recent SD Card

Lexar Professional

128 GB
133x Speed

Next Image: Galaxy
2.4cm X 3.2cm X 0.21cm
Volume :1.6 cm³  Weight 2g
Voltage 2.7 - 3.6V

Old Vacuum Tube:
5cm X 5cm X 10cm, 100g, 100W

1Tbit = 10k X10k X 10k bit

Volume = 0.5km X 0.5km X 1km
= 0.25 km³ = 0.25X10¹² cm³

Weight = 0.1 kgX10¹² = 0.1X10⁹ ton = 100 M ton
Power = 0.1kWX10¹² = 50 TW

Supply Capability of Tokyo Electric Power Company: 55 BW
So, progress of IC technology is most important for the power saving!
**Downsizing of the components has been the driving force for circuit evolution**

<table>
<thead>
<tr>
<th>Year</th>
<th>1900</th>
<th>1950</th>
<th>1960</th>
<th>1970</th>
<th>2000</th>
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<tr>
<td>Vacuum Tube</td>
<td>cm</td>
<td>cm</td>
<td>mm</td>
<td>10 μm</td>
<td>100 nm</td>
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<tr>
<td>10 cm</td>
<td>10^{-1}m</td>
<td>10^{-2}m</td>
<td>10^{-3}m</td>
<td>10^{-5}m</td>
<td>10^{-7}m</td>
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</table>

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
*We have never experienced such a tremendous reduction of devices in human history.*
Downsizing

1. **Reduce Capacitance**
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. **Increase number of Transistors**
   - Parallel processing
     - Increase circuit operation speed

Thus, downsizing of Si devices is the most important and critical issue.
5 nm gate length CMOS
Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC
IEDM, 2003
Question:
How far we can go with downscaling?
Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
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<tbody>
<tr>
<td>Late 1970’s</td>
<td>1µm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5µm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25µm:</td>
<td>Direct-tunneling of gate SiO₂</td>
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<tr>
<td>Late 1980’s</td>
<td>0.1µm:</td>
<td>‘0.1µm brick wall’(various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
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<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
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</table>
Historically, many predictions of the limit of downsizing. VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.
Finally, there appears to be a fundamental limit of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.
Direct-tunneling effect

Gate Electrode

Gate Oxide

Potential Barrier

Wave function

Direct tunneling current

Si Substrate

Direct tunneling leakage current start to flow when the thickness is 3 nm.
Direct tunneling leakage was found to be OK! In 1994!
Gate leakage: $I_g \propto \text{Gate Area} \propto \text{Gate length (Lg)}$

Drain current: $I_d \propto 1/\text{Gate length (Lg)}$

$Lg \rightarrow \text{small},$

Then, $I_g \rightarrow \text{small}, I_d \rightarrow \text{large},$ Thus, $I_g/I_d \rightarrow \text{very small}$
Transistor Scaling Continues

Qi Xinag, ECS 2004, AMD
Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!

Some one will think for you
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
So, we are now facing the limit of downsizing?
There is a solution!  
To use high-k dielectrics

Thin gate SiO\textsubscript{2}  
K=4  
Almost the same electric characteristics

Thick gate high-k dielectrics  
K=20  
Thick  
Small leakage Current

However, very difficult and big challenge!  
Remember MOSFET had not been realized without Si/SiO\textsubscript{2}!
So, again, how far we can go with downscaling?
Surface Potential (Negative direction)

0 bias for gate

@Vg=0V,
Transistor cannot be switched off
Limitation for MOSFET operation

Prediction now!

Tunneling distance

3 nm

Lg = Sub-3 nm?

Below this, no one knows future!
How far can we go for production?

**Past**

0.7 times per 3 years

1970年

10μm → 8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm → 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

**Now**

In 40 years: 18 generations,
Size 1/300, Area 1/100,000

**Future**

→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

- At least 4.5 generations to 8nm
- Hopefully 8 generations to 3nm
Subthreshold leakage current of MOSFET

\[ V_{th} \] (Threshold Voltage)

\[ V_{g} = 0 \text{V} \]

\[ I_{on} \] (ON)

\[ I_{off} \] (OFF)

Subthreshold leakage current of MOSFET
Vth cannot be decreased anymore

significant Ioff increase

Vth: 300mV → 100mV
Ioff increases with 3.3 decades

(300 - 100)mV/(60mV/dec) = 3.3 dec

Subthreshold slope (SS)
= (Ln10)(kT/q)(C_{ox} + C_D + C_{it})/C_{ox}
> ~ 60 mV/decade at RT

SS value:
Constant and does not become small with down-scaling
Subthreshold leakage current of MOSFET

- Subthreshold leakage current is OK at single transistor level.
- But not OK for billions of transistors.

Graph showing the relationship between drain current (Id) and gate voltage (Vg) with threshold voltage (Vth).
The limit is different depending on application

Source: 2007 ITRS Winter Public Conf.
Scaling Method: by R. Dennard in 1974

\( W_{\text{dep}} \): Space Charge Region (or Depletion Region) Width

- \( W_{\text{dep}} \) has to be suppressed
- Otherwise, large leakage between S and D

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

\[ \begin{align*}
X, Y, Z : & \quad K, \\
V : & \quad K, \\
Na : & \quad 1/K
\end{align*} \]

\( W_{\text{dep}} \propto \sqrt{V/Na} \) :

K = 0.7 for example

By the scaling, \( W_{\text{dep}} \) is suppressed in proportion, and thus, leakage can be suppressed.

Good scaled I-V characteristics
Down scaling is the most effective way of Power saving.

The down scaling of MOSFETs is still possible for another 10 years!

3 important technological items for DS.

New materials
   1. Thinning of high-k beyond 0.5 nm
   2. Metal S/D

New structures
   3. Wire channel
1. High-k beyond 0.5 nm
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

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By Robert Chau, IWGI 2003
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Choice of High-k elements for oxide

### Candidates

<table>
<thead>
<tr>
<th>H</th>
<th>Li</th>
<th>Be</th>
<th>Mg</th>
<th>Na</th>
<th>Ca</th>
<th>Sc</th>
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<tbody>
<tr>
<td>Si + MO&lt;sub&gt;x&lt;/sub&gt; M + SiO&lt;sub&gt;2&lt;/sub&gt;</td>
<td>Si + MO&lt;sub&gt;x&lt;/sub&gt; MSi&lt;sub&gt;x&lt;/sub&gt; + SiO&lt;sub&gt;2&lt;/sub&gt;</td>
<td>Si + MO&lt;sub&gt;x&lt;/sub&gt; M + MSi&lt;sub&gt;x&lt;/sub&gt;O&lt;sub&gt;y&lt;/sub&gt;</td>
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</tbody>
</table>

- Unstable at Si interface
- Gas or liquid at 1000 K
- Radio active
- He
- B  C  N  O  F  Ne
- Al  Si  P  S  Cl  Ar

La<sub>2</sub>O<sub>3</sub> based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

HfO<sub>2</sub> based dielectrics are selected as the first generation materials, because of their merit in:
1) band-offset,
2) dielectric constant,
3) thermal stability.

#### Choice of High-k elements for oxide

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R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

![Diagram showing conduction band offset vs. dielectric constant]

Band Discontinuity [eV] vs. Dielectric Constant $\varepsilon(0)$

XPS measurement by Prof. T. Hattori, INFOS 2003
High-k gate insulator MOSFETs for Intel: EOT=1nm

HfO$_2$ based high-k
For the past 45 years, SiO2 and SiON have been used as gate insulators. Today, EOT = 1.0 nm. EOT can be reduced further beyond 0.5 nm by using direct contact to Si and choosing appropriate materials and processes.

EOT Limit: 0.7~0.8 nm

One order of magnitude improvement:

- Today: EOT = 1.0 nm
- 45nm node: EOT = 0.7~0.8 nm
- Now: EOT = 0.5 nm

Introduction of High-k materials: High-k metal can be directly contacted to Si to reduce EOT below 0.5 nm.

Still SiO2 or SiON is used at Si interface.
Cluster tool for high-k thin film deposition
SiO$_x$-IL growth at HfO$_2$/Si Interface

SiO$_x$-IL is formed after annealing
Oxygen control is required for optimizing the reaction

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O$^*$ $\rightarrow$ HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 6131

D.J. Lichtenwalner, Trans. ECS 11, 319

Oxygen supplied from W gate electrode
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ can achieve direct contact of high-k/Si
Gate Leakage vs EOT, \((V_g=|1|V)\)

- Al2O3
- HfAlO(N)
- HfO2
- HfSiO(N)
- HfTaO
- La2O3
- Nd2O3
- Pr2O3
- PrSiO
- PrTiO
- SiON/SiN
- Sm2O3
- SrTiO3
- Ta2O5
- TiO2
- ZrO2(N)
- ZrSiO
- ZrAlO(N)
La$_2$O$_3$ at 300° C process make sub-0.4 nm EOT MOSFET

**EOT=0.37nm**

- EOT=0.37nm
- EOT=0.40nm
- EOT=0.48nm

0.48 → 0.37nm Increase of Id at 30%
However, high-temperature anneal is necessary for the good interfacial property.

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
A small $D_{it}$ of $1.6 \times 10^{11}$ cm$^{-2}$/eV, results in better electron mobility.
Physical mechanisms for small Dit

- Silicate-reaction-formed fresh interface
- Stress relaxation at interface by glass type structure of La silicate.


EOT growth suppression by Si coverage

Increasing EOT caused by high temperature annealing can be dramatically suppressed by Silicon masked stacks
La$_2$O$_3$

W

Si/TiN/W

Si/TiN/W

K$_{av}$ ~ 8

K$_{av}$ ~ 12

K$_{av}$ ~ 16

No interfacial layer can be confirmed with Si/TiN/W
nMOSFET with EOT of 0.62nm

EOT of 0.62nm and 155 cm$^2$/Vsec at 1MV/cm can be achieved
Benchmark of La-silicate dielectrics

Gate leakage is two orders of magnitude lower than that of ITRS

Electron mobility is comparable to record mobility with Hf-based oxides

This work (MIPS Stacks)

Open: Hf-based oxides

T. Ando et al., IEDM2009
Metal (Silicide) S/D
Extreme scaling in MOSFET

- Dopant abruptness at S/D
- \( V_t \) and \( I_{ON} \) variation
- GIDL

Metal Schottky S/D junctions

- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Surface or interface control

Diffusion species: metal atom (Ni, Co)
- Rough interface at silicide/Si
  - Excess silicide formation
  - Different $\phi_{Bn}$ presented at interface
  - Process temperature dependent composition

Diffusion species: Si atom (Ti)
- Surface roughness increases
  - Line dependent resistivity change

Annealing: 650 °C
Si(001) sub. Epitaxial NiSi$_2$


CoSi$_2$ NiSi TiSi$_2$

Top view
Line width of 0.1 $\mu$m

Aglomeration

**Unwanted leakage current**

- Edge leakage current at periphery
- Generation current due to defects in substrate

**Variable leakage current in smaller contact**

**Specification for metal silicide S/D**

- Atomically flat interface with smooth surface
- Suppressed leakage current
- Stability of silicide phase and interface in a wide process temperature

**Graph**

- Abbreviation: $V_{app} = -0.2V, \phi_B = \sim 0.57 \text{ eV}$
- Current density (A/cm$^2$) vs. Length of a contact side ($\mu$m)

**Note**

Annealing: 500 °C
Deposition of Ni-Si mixed films from NiSi$_2$ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
SEM views of silicide/Si interfaces

Ni source (50nm) vs. NiSi$_2$ source (50nm)

600°C, 1min
- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

700°C, 1min
- Atomically flat interfaces
- No Si consumption
- Temperature-independent

800°C, 1min
- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm
Ideal characteristics ($n = 1.00$, suppressed leakage current)

- Flat interface and No Si substrate consumption
- No defects in Si substrate

Suppressed reverse leakage current

Schottky diode structures

Ni source

NiSi$_2$ source

Ni contact

NiSi$_2$ contact

Si substrate

Al contact

Diode voltage (V)

Diode current (A/cm$^2$)

<table>
<thead>
<tr>
<th>Source</th>
<th>$\phi_B$ (eV)</th>
<th>$n$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>0.676</td>
<td>1.08</td>
</tr>
<tr>
<td>NiSi$_2$</td>
<td>0.659</td>
<td>1.00</td>
</tr>
</tbody>
</table>

RTA: 500$^\circ$C, 1min

Current density (A/cm$^2$)

Applied Voltage (V)
Wire channel
Suppression of subthreshold leakage by surrounding gate structure

Planar

Surrounding gate
Because of off-leakage control,

Planar $\rightarrow$ Fin $\rightarrow$ Nanowire
Nanowire structures in a wide meaning

Fin
Tri-gate
Ω-gate
Nanowire
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of $I_{OFF}$
3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires

Cut-off

Leakage current

Gate: OFF

Drain source

Cut-off

Gate: OFF

Drain source
Increase the Number of quantum channels

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

By Prof. Shiraishi of Tsukuba univ.
Device fabrication

Si/Si$_{0.8}$Ge$_{0.2}$ superlattice epitaxy on SOI

Anisotropic etching of these layers

Isotropic etching of SiGe

The NW diameter is controllable down to 5 nm by self limited oxidation.

Gate depositions

HfO$_2$ (3nm)

TiN (10nm)

Poly-Si (200nm)

Gate etching

S/D implantation

Spacer formation

Activation anneal

Salicidation

Standard Back-End of-Line Process

Process Details:

C. Dupre et al.,
3D-stacked Si NWs with Hi-\(k\)/MG

Wire direction: \(<110>\)
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT \(\sim\) 2.6 nm

C. Dupre et al.,
SiNW FET Fabrication

S/D & Fin Patterning

Sacrificial Oxidation

Oxide etch back

SiN sidewall support formation

Gate Oxidation & Poly-Si Deposition

Gate Lithography & RIE Etching

Gate Sidewall Formation

Ni SALISIDE Process (Ni 9nm / TiN 10nm)

Backend

Standard recipe for gate stack formation
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off > 10^6, 60uA/wire

L_g = 65nm, T_ox = 3nm
This work

Planer FET △  1.0~1.1V
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

Si ノワイヤFET ★  1.2~1.3V
Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240
Figure 1: (a) Schematic diagram of a SiNW device with a metal contact. The graph shows the electron density distribution as a function of distance from the SiNW surface. The color bar indicates electron density in units of $10^{19}\text{cm}^{-3}$. The figure highlights two regions: the edge portion and the flat portion. (b) Comparison of inversion areal ratios at different voltages, with $V_g = 1\text{V}$. The percentage of the edge portion is 44%, and the inversion areal ratio for the flat portion is 29%.
Primitive estimation!

- Small EOT for high-k (33)
- P-MOS improvement (26)
- Low S/D resistance (20)
- # of wires /1µm (15)
- SiNW (12nm & 19nm)

Compact model

Assumption

\[ I_{ON} \propto L_g^{-0.5} T_{ox}^{-1} \]

- Bulk
- FD
- ITRS
- MG
Our roadmap for R & D
Source: H. Iwai, IWJT 2008

Current Issues

Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Thank you for your attention!