Future of Nano CMOS Technology

September 29, 2011

2011 IEEE Regional Symposium on Micro and Nanoelectronics (IEEE-RSM2011)

Le Meridien Hotel, Kota Kinabalu, Malaysia

Hiroshi Iwai,
Tokyo Institute of Technology
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
Institute Overview

Established in 1881 → 130th anniversary in 2011
3 undergraduate schools
  School of Science, School of Engineering, School of Bioscience and Biotechnology
7 graduate schools

Total Number of Students

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<tr>
<th></th>
<th>Undergraduate</th>
<th>Graduate</th>
<th>Master’s</th>
<th>Doctoral</th>
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</table>

Total 982
(As of May. 1, 2005)
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Same mechanism as that of transistor
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928
Mechanism of MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

- **Surface Potential (Negative direction)**
  - 0V
  - N⁺-Si
  - P-Si
  - 1V
  - N-Si

- **Electron flow**
  - Positive bias for gate
  - Negative bias for gate

- **Diagram**
  - Source
  - Channel
  - Drain

- **Gate electrode**
  - Gate Oxid

- **Symbols**
  - G (Gate)
  - S (Source)
  - D (Drain)
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator.

Interfacial Charges

Electric Shielding

Carrier Scattering

Drain Current was several orders of magnitude smaller than expected.

Even Shockley!
However, they found amplification phenomenon when investigating Ge surface when putting needles. This is the 1\textsuperscript{st} Transistor:

Not MOSFET (Field Effect Transistor), But Bipolar Transistor (another mechanism)

1947: 1\textsuperscript{st} transistor

Bipolar using Ge

J. Bardeen  W. Bratten,  W. Shockley
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si/SiO₂ Interface is exceptionally good
1970, 71: 1st generation of LSIs

DRAM   Intel 1103

MPU     Intel 4004
2011
Most recent SD Card
Most Recent SD Card

128GB (Bite)
= 128G X 8bit = 1024Gbit
= 1.024T(Tera)bit

1T = 10^{12} = 1Trillion

World Population : 6 Billion
Brain Cell : 10〜100 Billion
Stars in Galaxy : 100 Billion
Most Recent SD Card
2.4cm X 3.2cm X 0.21cm

Volume : 1.6cm³  Weight 2g

Voltage 2.7 - 3.6V

Old Vacuum Tube :
5cm X 5cm X 10cm, 100g, 100W

1Tbit = 10k X 10k X 10k bit

Volume = 0.5km X 0.5km X 1km
= 0.25 km³ = 0.25 X 10¹² cm³

Weight = 0.1 kg X 10¹² = 0.1 X 10⁹ ton = 100 M ton

Power = 0.1 kW X 10¹² = 50 TW

Supply Capability of Tokyo Electric Power Company: 55 BW
Downsizing of the components has been the driving force for circuit evolution.

<table>
<thead>
<tr>
<th>Year</th>
<th>Vacuum Tube</th>
<th>Transistor</th>
<th>IC</th>
<th>LSI</th>
<th>ULSI</th>
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<tr>
<td>1900</td>
<td>10 cm</td>
<td>10 cm</td>
<td>mm</td>
<td>10 µm</td>
<td>100 nm</td>
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<td>1950</td>
<td>10^{-1}m</td>
<td>10^{-2}m</td>
<td>10^{-3}m</td>
<td>10^{-5}m</td>
<td>10^{-7}m</td>
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<tr>
<td>1960</td>
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<td>2000</td>
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In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. **Reduce Capacitance**
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. **Increase number of Transistors**
   - Parallel processing
     - Increase circuit operation speed

Thus, downsizing of Si devices is the most important and critical issue.
Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
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<tbody>
<tr>
<td>Late 1970’s</td>
<td>1μm:</td>
<td>SCE</td>
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<td>Early 1980’s</td>
<td>0.5μm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25μm:</td>
<td>Direct-tunneling of gate SiO₂</td>
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<tr>
<td>Late 1980’s</td>
<td>0.1μm:</td>
<td>‘0.1μm brick wall’ (various)</td>
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<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
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</tbody>
</table>
Transistor Scaling Continues

Qi Xinag, ECS 2004, AMD
5 nm gate length CMOS
Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC
IEDM, 2003
Electron wave length \( 10 \text{ nm} \)

Tunneling distance \( 3 \text{ nm} \)

MOSFET operation \( L_g = 3 \text{ nm} \)?
Electron wave length \(10\,\text{nm}\)

Tunneling distance \(3\,\text{nm}\)

Atom distance \(0.3\,\text{nm}\)

MOSFET operation 

\[L_g = \text{Sub-3 nm?}\]

Below this, no one knows future!
Question:
How far we can go with downscaling?
How far can we go for production?

**Past** 0.7 times per 3 years

1970年
10µm → 8µm → 6µm → 4µm → 3µm → 2µm → 1.2µm → 0.8µm → 0.5µm → 0.35µm → 0.25µm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

**Now**

In 40 years: 18 generations,
Size 1/300, Area 1/100,000

**Future**

→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

- At least 4,5 generations to 8nm
- Hopefully 8 generations
Subthreshold leakage current of MOSFET

- $V_{th}$ (Threshold Voltage)
- $I_{on}$
- $I_{off}$
- $V_g = 0V$
- Subthreshold region

Graph showing the relationship between $V_g$ and $I_g$ with $I_{on}$ and $I_{off}$ indicating the ON and OFF states respectively.
Vth cannot be decreased anymore

significant Ioff increase

Vth: 300mV → 100mV
Ioff increases with 3.3 decades

(300 – 100)mV/(60mV/dec) = 3.3 dec

Subthreshold slope (SS)
= \((\ln 10)(kT/q)(C_{ox}+C_D+C_{it})/C_{ox}\)
> ~ 60 mV/decade at RT

SS value:
Constant and does not become small with down-scaling
Subthreshold leakage current of MOSFET

Subthreshold leakage current is OK at single transistor level, but not OK for billions of transistors.
HP, LOP, LSTP for Logic CMOS

- **HP CMOS** (high Performance)
  - Highest Ion, Lowest CV/I
  - High leakage
  - Medium Vdd

- **LOP CMOS** (Low Operation Power)
  - Lowest Vdd
  - Medium Ion, medium CV/I
  - Medium leakage

- **LSTP CMOS** (Low Standby Power)
  - Lowest leakage
  - Low Ion, high CV/I
  - High Vdd

Source: 2007 ITRS Winter Public Conf.
Scaling Method: by R. Dennard in 1974

**W_{dep}:** Space Charge Region (or Depletion Region) Width

W_{dep} has to be suppressed. Otherwise, large leakage between S and D.

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

K=0.7 for example

By the scaling, W_{dep} is suppressed in proportion, and thus, leakage can be suppressed.

Good scaled I-V characteristics

\[ W_{dep} \propto \sqrt{V/Na} : K \]
Down scaling is the most effective way of Power saving.

It has been always discussed about the limit of downscaling, but the down scaling of MOSFETs is still possible for another 10 or 20 years!

3 important technological items for DS.

1. Thinning of high-k beyond 0.5 nm

2. Metal S/D

3. Si-Nanowire FET
High-k
0.8 nm Gate Oxide Thickness MOSFETs operates!!

**0.8 nm: Distance of 3 Si atoms!!**

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
There is a solution!  
To use high-k dielectrics

Thin gate SiO$_2$  
K=4  
Almost the same electric characteristics

Thick gate high-k dielectrics  
K=20  
Thick  
Small leakage Current

However, very difficult and big challenge!  
Remember MOSFET had not been realized without Si/SiO$_2$!
### Choice of High-k elements for oxide

### Candidates

<table>
<thead>
<tr>
<th>H</th>
<th>Li</th>
<th>Be</th>
<th>Mg</th>
<th>Na</th>
<th>Ca</th>
<th>Sc</th>
<th>Ti</th>
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</table>

#### Unstable at Si interface
- Si + MO\(_x\) \(\rightarrow\) M + SiO\(_2\)
- Si + MO\(_x\) \(\rightarrow\) MSi\(_x\) + SiO\(_2\)
- Si + MO\(_x\) \(\rightarrow\) M + MSi\(_x\)O\(_y\)

| K  | Ca | Sc | Ti | V  | Cr | Mn | Fe | Co | Ni | Cu | Zn | Ga | Ge | As | Se | Br | Kr |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Ra | Rf | Ha | Sg | Np | Pu | Am | Cm | Bk | Cf | Es | Fm | Md | No | Lr |    |    |    |    |
| Ac | Th | Pa | U  | Np | Pu | Am | Cm | Bk | Cf | Es | Fm | Md | No | Lr |    |    |    |    |

### Gas or liquid at 1000 K

### Radio active He

HfO\(_2\) based dielectrics are selected as the first generation materials, because of their merit in:
1) band-offset,
2) dielectric constant,
3) thermal stability.

La\(_2\)O\(_3\) based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

Unstable at Si interface: Si + MO\(_x\) \(\rightarrow\) M + SiO\(_2\) \(\rightarrow\) MSi\(_x\) + SiO\(_2\) \(\rightarrow\) M + MSi\(_x\)O\(_y\)

Choice of High-k elements for oxide are selected as the first generation materials, because of their merit in:
1) band-offset,
2) dielectric constant,
3) thermal stability.

R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band offset

Oxide

Si

XPS measurement by Prof. T. Hattori, INFOS 2003
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness
For the past 45 years, SiO2 and SiON have been used for gate insulator. Today, EOT=1.0nm.

EOT Limit: 0.7~0.8 nm

One order of Magnitude

EOT=0.5nm

45nm node: Lg=22nm

Introduction of High-k:
Still SiO2 or SiON is used at Si interface.

EOT can be reduced further beyond 0.5 nm by using direct contact to Si. By choosing appropriate materials and processes.
Cluster tool for high-k thin film deposition

- Preparation Room
- E-Beam Evaporation: 8 different target
- Flash Lamp
- Anneal: Micro to milli-seconds
- Robot Room
- Sputter for metal: 5 different target
SiO$_x$-IL growth at HfO$_2$/Si Interface

XPS Si1s spectrum

Phase separator

HfO$_2$ + Si + O$_2$ $\nRightarrow$ HfO$_2$ + Si + 2O* $\nRightarrow$ HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 6131

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction

D.J.Lichtenwalner, Tans. ECS 11, 319
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$
  □ La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Gate Leakage vs EOT, (Vg=|1|V)
EOT=0.37nm
La2O3

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

W/L = 50µm /2.5µm

Vth=-0.06V  Vth=-0.05V  Vth=-0.04V

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

0.48 → 0.37nm Increase of Id at 30%
A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
A small $D_{it}$ of $1.6 \times 10^{11}$ cm$^{-2}$/eV, results in better electron mobility.
Physical mechanisms for small Dit

- silicate-reaction-formed fresh interface
- stress relaxation at interface

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress


Increasing EOT caused by high temperature annealing can be dramatically suppressed by MIPS stacks.
La$_2$O$_3$

Cross sectional TEM images

W

TiN/W

MIPS

La$_2$O$_3$

$K_{av} \sim 8$

$K_{av} \sim 12$

$K_{av} \sim 16$

No interfacial layer can be confirmed in MIPS stacks
nMOSFET with EOT of 0.62nm

EOT of 0.62nm and 155 cm²/Vsec at 1MV/cm can be achieved
Gate leakage is two orders of magnitude lower than that of ITRS

Electron mobility is comparable to record mobility with Hf-based oxides
Metal (Silicide) S/D
**Introduction - Schottky Barrier FET**

**Extreme scaling in MOSFET**
- Dopant abruptness at S/D
- $V_t$ and $I_{ON}$ variation
- GIDL

**Metal Schottky S/D junctions**
- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Issues in metal silicide S/D

Surface or interface control

Diffusion species: metal atom (Ni, Co)
- Rough interface at silicide/Si
  - Excess silicide formation
  - Different $\phi_B$ presented at interface
  - Process temperature dependent composition

Diffusion species: Si atom (Ti)
- Surface roughness increases
  - Line dependent resistivity change

Annealing: 650 ºC
Si(001) sub. Epitaxial NiSi$_2$


CoSi$_2$ NiSi TiSi$_2$

Top view
Line width of 0.1 µm

Aglomeration

Unwanted leakage current
- Edge leakage current at periphery
- Generation current due to defects in substrate

Variable leakage current in smaller contact

Specification for metal silicide S/D
- Atomically flat interface with smooth surface
- Suppressed leakage current
- Stability of silicide phase and interface in a wide process temperature

Annealing: 500 °C

$V_{app} = -0.2V$

$\phi_Bn = \sim 0.57$ eV
Our approach for flat silicide/Si interface

Deposition of Ni film

- Deposition of Ni film
- Annealing
- Rough interface

Deposition from NiSi$_2$ source

- Deposition from NiSi$_2$ source
- No Si substrate consumption
- Flat interface

Deposition of Ni-Si mixed films from NiSi$_2$ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
Fabrication process of the Schottky diodes

- *n*-type Si substrate, Si(100) with 400 nm SiO$_2$ isolation
  Doping concentration: $3 \times 10^{15}$ cm$^{-3}$

- SPM and HF cleaning

- Diode patterning by photolithography and BHF etching of SiO$_2$

- Deposition of 10-nm-thick NiSi$_2$ and Ni sources by RF sputtering in Ar atmosphere

- Ni silicidation by Rapid Thermal Annealing (RTA) in N$_2$ atmosphere

- Al contact deposition on substrate backside by thermal evaporation

- Measurement of electrical characteristics
- SEM and TEM observation
- XRD and XPS analysis
SEM views of silicide/Si interfaces

- Ni source (50nm)
  - Rough interfaces
  - Consumed Si substrate
  - Thickness increase ~100 nm

- NiSi₂ source (50nm)
  - Atomically flat interfaces
  - No Si consumption
  - Temperature-independent

Ni source

NiSi₂ source

Ni-silicide

Si substrate

STI

600°C, 1min

700°C, 1min

800°C, 1min
J-V characteristics of the Schottky diodes

Ideal characteristics ($n = 1.00$, suppressed leakage current)

- Flat interface and No Si substrate consumption
- No defects in Si substrate

Suppressed reverse leakage current

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<th>Source</th>
<th>$\phi_B$ (eV)</th>
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<td>Ni</td>
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<tr>
<td>NiSi$_2$</td>
<td>0.659</td>
<td>1.00</td>
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</table>

Si substrate

Ni source

NiSi$_2$ source

RTA $500^\circ$C, 1min

Schottky diode structures
Summary of the silicide phases with NiSi₂ source

- Ni-rich phases in the silicide layer are maintained with NiSi₂ source

- No distinct structure change at the interface
  - Stable $\phi_Bn$ and n-factor
  - No structural effect for silicidation
Si nanowire
Because of off-leakage control,

Planar $\rightarrow$ Fin $\rightarrow$ Nanowire

Planar FET

Fin FET

Nanowire FET
Nanowire structures in a wide meaning
Nanowire FET

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<td>Multiple Gate</td>
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- 2015: 22 or 16nm node
- 2020: 11 or 8nm node

Multiple Gate (Fin) FET

Nanowire FET

ITRS 2009

Bulk  □ Fin  □ Nanowire

Scaling Pathways

- w and w/o 3rd gate?
- Bulk or SOI
- Fin

Si Nanowire
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of \( I_{\text{OFF}} \)
3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Device fabrication

Si/Si_{0.8}Ge_{0.2} superlattice epitaxy on SOI

Anisotropic etching of these layers

Isotropic etching of SiGe

The NW diameter is controllable down to 5 nm by self limited oxidation.

SiN HM

BOX

SiN
SiGe
Si
SiGe
Si
SiGe
Si
BOX

Gate depositions
- HfO_2 (3nm)
- TiN (10nm)
- Poly-Si (200nm)

Gate etching

S/D implantation
Spacer formation
Activation anneal
Salicidation

Standard Back-End of-Line Process

Process Details:
C. Dupre et al., IEDM Tech. Dig., p.749, 2008
3D-stacked Si NWs with Hi-κ/MG

Wire direction: <110>
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT ~2.6 nm
SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oxide etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)

Backend: Standard recipe for gate stack formation
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off $>10^6$, 60uA/wire

$L_g=65\text{nm}$, $T_{ox}=3\text{nm}$
Our Work
$I_{ON}/I_{OFF}$ Benchmark

Planer FET ▲ 1.0~1.1V
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

Si Nano Wire FET ★ 1.2~1.3V
Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240

$L_g=500~65nm$
Electron Density
(x×10^{19} cm^{-3})

Distance from SiNW Surface (nm)

(a) Metal

12 nm

19 nm

SiO₂

V_g = 1 V

44%

(b) Inversion areal ratio: 29%

12 nm

39 nm

Edge portion

Flat portion
Primitive estimation!

- **SiNW (12nm - 19nm)**
- **Small EOT for high-k**  
  $L_g^{-0.5}$ $T_{ox}^{-1}$
- **P-MOS improvement**
- **Low S/D resistance**
- **Compact model**
- **Assumption**
  $I_{ON} \propto L_g^{-0.5} \cdot T_{ox}^{-1}$
- **# of wires / 1\,\mu m**

![Graph showing trend of $I_{ON}$ vs. Year with various technologies and assumptions](image-url)
Transistor Innovations Enable Technology Cadence

- **2003**: 90 nm, Invented SiGe Strained Silicon
- **2005**: 65 nm, 2nd Gen. SiGe Strained Silicon
- **2007**: 45 nm, Invented Gate-Last High-k Metal Gate
- **2009**: 32 nm, 2nd Gen. Gate-Last High-k Metal Gate
- **2011**: 22 nm, First to Implement Tri-Gate

- Strained Silicon
- High k Metal gate
- Tri-Gate
22nm Silicon Technology Breakthrough Benefits Broad Range of Intel Architecture Devices

New 22nm 3-D transistors deliver unprecedented performance improvement and power reduction for Intel’s product portfolio

- This benefits smallest handhelds to powerful cloud-based servers
- 37% performance increase at low voltage vs. 32nm planar transistors*
- Consumes only half the power at the same performance level as 2-D transistors on 32nm planar chips*
Our roadmap for R & D
Source: H. Iwai, IWJT 2008

**Current Issues**

**Si Nanowire**
- Control of wire surface property
- Optimization of wire diameter
- Compact I-V model

**III-V & Ge Nanowire**
- High-k gate insulator
- Wire formation technique

**CNT:**
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

**Graphene:**
- Graphene formation technique
- Suppression of off-current
  - Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Thank you for your attention!