Future of Micro/Nano Electronics

September 19, 2011

@KTH

Kista, Sweden

Hiroshi Iwai,
Tokyo Institute of Technology
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
Institute Overview

Established in 1881 → 130th anniversary in 2011

3 undergraduate schools
School of Science, School of Engineering, School of Bioscience and Biotechnology

7 graduate schools
Science and Engineering Science, Science and Engineering Technology,
Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

<table>
<thead>
<tr>
<th></th>
<th>Undergraduate</th>
<th>Graduate</th>
<th>Master's</th>
<th>Doctoral</th>
<th>Teaching Staff</th>
<th>Student/Instructor</th>
<th>Staff</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tokyo Inst.</td>
<td>5,000</td>
<td>5,000</td>
<td>3,500</td>
<td>1,500</td>
<td>1,200</td>
<td>8.3</td>
<td>550</td>
</tr>
<tr>
<td>Per Year</td>
<td>1,200</td>
<td>1,800</td>
<td>500</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Einstein Visit
Asia 847
Europe 78
North America 12
Africa 16
South America 24
Oceania 5
Total 982
(As of May. 1, 2005)
先端ナノエレクトロニクス研究コアユニット研究室メンバー

（2010年10月1日現在）

博士
研究員 (1人)

修士
学生 (26人)

学部
生 (3人)

教員 (10人)

技術員 (1人)
研究風景

Deposition  Lithography  Etching
Analysis     Measurement  Annealing
Office
Cluster tool for high-k thin film deposition
Lee De Forest

Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Same mechanism as that of transistor
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
Devices for controlled electric current

Filed March 28, 1928
Capacitor structure with notch

Negative bias

- - - - -

No current

Positive bias

- - - - -

Current flows

Gate Electrode

Gate Insulator

Semiconductor

Electron

Electric field
Surface Potential (Negative direction)

- **0V**: Source
- **1V**: N-Si
- **N⁺-Si**: Negative
- **P-Si**: Channel
- **Drain**

**Gate electrode**

**Gate Oxid**

**Electron flow**

0 bias for gate

Positive bias for gate
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator.

Drain Current was several orders of magnitude smaller than expected.

Even Shockley!
However, they found amplification phenomenon when investigating Ge surface when putting needles. This is the 1st Transistor: 
**Not Field Effect Transistor,**  
**But Bipolar Transistor (another mechanism)**

1947: 1\textsuperscript{st} transistor

Bipolar using Ge

J. Bardeen  
W. Bratten

W. Shockley
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source
Drain
Si
Al Gate

Si/SiO₂ Interface is extraordinarily good
1970,71: 1st generation of LSIs

DRAM   Intel 1103

MPU    Intel 4004
Most recent SD Card
Most Recent SD Card

128GB = 128G Bite
= 128G X 8bit = 1024Gbit
= 1.024T(Tera)bit

1T = 10^{12} = 1Trillion

World Population : 6 Billion
Brain Cell : 10〜100 Billion
Stars in Galaxy : 100 Billion
Most Recent SD Card

Lexar Professional

128GB

133x Speed

Next Image
2.4cm X 3.2cm X 0.21cm
Volume : 1.6cm³  Weight : 2g
Voltage : 2.7 - 3.6V

Old Vacuum Tube:
5cm X 5cm X 10cm, 100g, 100W

1Tbit = 10k X 10k X 10k bit

Volume = 0.5km X 0.5km X 1km
= 0.25 km³ = 0.25 X 10¹² cm³

Weight = 0.1 kg X 10¹² = 0.1 X 10⁹ ton = 100 M ton

Power = 0.1 kW X 10¹² = 50 TW

Supply Capability of Tokyo Electric Power Company: 55 BW
Downsizing of the components has been the driving force for circuit evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Device</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>1900</td>
<td>Vacuum Tube</td>
<td>10 cm</td>
</tr>
<tr>
<td>1950</td>
<td>Transistor</td>
<td>cm</td>
</tr>
<tr>
<td>1960</td>
<td>IC</td>
<td>mm</td>
</tr>
<tr>
<td>1970</td>
<td>LSI</td>
<td>10 µm</td>
</tr>
<tr>
<td>2000</td>
<td>ULSI</td>
<td>100 nm</td>
</tr>
</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. Reduce Capacitance
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. Increase number of Transistors
   - Parallel processing
     - Increase circuit operation speed

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.
Scaling Method: by R. Dennard in 1974

**Wdep:** Space Charge Region (or Depletion Region) Width

- Wdep has to be suppressed
- Otherwise, large leakage between S and D

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

$K = 0.7$ for example

### Good scaled I-V characteristics

$$W_{dep} \propto \sqrt{V/Na}$$

$X, Y, Z: K, \quad V: K, \quad Na: 1/K$

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

$$I: K$$
### Downscaling merit: Beautiful!

<table>
<thead>
<tr>
<th>Geometry &amp; Supply voltage</th>
<th>( L_g, W_g, T_{ox}, V_{dd} )</th>
<th>( K )</th>
<th>Scaling  ( K : K=0.7 ) for example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive current in saturation</td>
<td>( I_d )</td>
<td>( K )</td>
<td>( I_d = v_{sat} W_g C_o (V_g - V_{th}) ) ( C_o ): gate C per unit area ( \rightarrow W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = K K^{-1} K = K )</td>
</tr>
<tr>
<td>( I_d ) per unit ( W_g )</td>
<td>( I_d / \mu m )</td>
<td>1</td>
<td>( I_d ) per unit ( W_g = I_d / W_g = 1 )</td>
</tr>
<tr>
<td>Gate capacitance</td>
<td>( C_g )</td>
<td>( K )</td>
<td>( C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox} ) ( \rightarrow KK/K = K )</td>
</tr>
<tr>
<td>Switching speed</td>
<td>( \tau )</td>
<td>( K )</td>
<td>( \tau = C_g V_{dd} / I_d ) ( \rightarrow KK/K = K )</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>( f )</td>
<td>( 1/K )</td>
<td>( f = 1/\tau = 1/K )</td>
</tr>
<tr>
<td>Chip area</td>
<td>( A_{chip} )</td>
<td>( \alpha )</td>
<td>( \alpha ): Scaling factor ( \rightarrow ) In the past, ( \alpha &gt; 1 ) for most cases</td>
</tr>
<tr>
<td>Integration (# of Tr)</td>
<td>( N )</td>
<td>( \alpha/K^2 )</td>
<td>( N \rightarrow \alpha/K^2 = 1/K^2 ), when ( \alpha = 1 )</td>
</tr>
<tr>
<td>Power per chip</td>
<td>( P )</td>
<td>( \alpha )</td>
<td>( fN C V^2 / 2 ) ( \rightarrow K^{-1}(\alpha K^{-2})K (K^1)^2 = \alpha = 1 ), when ( \alpha = 1 )</td>
</tr>
<tr>
<td></td>
<td>k= 0.7 and $\alpha = 1$</td>
<td>k= 0.7$^2$ =0.5 and $\alpha = 1$</td>
<td></td>
</tr>
<tr>
<td>--------------------------</td>
<td>-----------------------------------------------</td>
<td>----------------------------------</td>
<td></td>
</tr>
<tr>
<td><strong>Single MOFET</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vdd $\rightarrow$ 0.7</td>
<td></td>
<td>Vdd $\rightarrow$ 0.5</td>
<td></td>
</tr>
<tr>
<td>Lg $\rightarrow$ 0.7</td>
<td></td>
<td>Lg $\rightarrow$ 0.5</td>
<td></td>
</tr>
<tr>
<td>Id $\rightarrow$ 0.7</td>
<td></td>
<td>Id $\rightarrow$ 0.5</td>
<td></td>
</tr>
<tr>
<td>Cg $\rightarrow$ 0.7</td>
<td></td>
<td>Cg $\rightarrow$ 0.5</td>
<td></td>
</tr>
<tr>
<td>$P$ (Power)/Clock $\rightarrow 0.7^3 = 0.34$</td>
<td>$P$ (Power)/Clock $\rightarrow 0.5^3 = 0.125$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\tau$ (Switching time) $\rightarrow$ 0.7</td>
<td>$\tau$ (Switching time) $\rightarrow$ 0.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Chip</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N (# of Tr) $\rightarrow$ $1/0.7^2 = 2$</td>
<td>N (# of Tr) $\rightarrow$ $1/0.5^2 = 4$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f (Clock) $\rightarrow$ $1/0.7 = 1.4$</td>
<td>f (Clock) $\rightarrow$ $1/0.5 = 2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P (Power) $\rightarrow$ 1</td>
<td>P (Power) $\rightarrow$ 1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Actual past downscaling trend until year 2000

![Graph showing the trend of various parameters over time](image)

#### Change in 30 years

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ideal Scaling</th>
<th>Real Change</th>
<th>Ideal Scaling</th>
<th>Real Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$</td>
<td>$K$</td>
<td>$10^{-2}$</td>
<td>$K$</td>
<td>$10^{-2}$</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>$K(10^{-2})$</td>
<td></td>
<td>$K(10^{-2})$</td>
<td></td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-1}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$A_{chip}$</td>
<td>$\alpha$</td>
<td>$10^1$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_d/\mu m$</td>
<td>$1$</td>
<td>$10^1$</td>
<td>$\alpha/K^2(10^5)$</td>
<td>$10^4$</td>
</tr>
<tr>
<td>$N$</td>
<td>$\alpha/K^2(10^5)$</td>
<td>$10^4$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f$</td>
<td>$1/K(10^2)$</td>
<td>$10^3$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P$</td>
<td>$\alpha(10^1)$</td>
<td>$10^5$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$= f\alpha NCV^2$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Past 30 years scaling**

- **Merit**: $N$, $f$ increase
- **Demerit**: $P$ increase

**$V_{dd}$ scaling insufficient**

- Additional significant increase in $I_d$, $f$, $P$

**Vd scaling insufficient, $\alpha$ increased**

$\rightarrow$ $N$, $I_d$, $f$, $P$ increased significantly

Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1μm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5μm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25μm:</td>
<td>Direct-tunneling of gate SiO₂</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1μm:</td>
<td>‘0.1μm brick wall’(various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
Historically, many predictions of the limit of downsizing. VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.
Finally, there appears to be a fundamental limit of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.
Direct-tunneling effect

Gate Electrode

Gate Oxide

Potential Barrier

Si Substrate

Wave function

Direct tunneling current

Direct tunneling leakage current starts to flow when the thickness is 3 nm.
Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide

- $L_g = 10 \, \mu m$
- $L_g = 5 \, \mu m$
- $L_g = 1.0 \, \mu m$
- $L_g = 0.1 \, \mu m$
Gate leakage: $I_g \propto \text{Gate Area} \propto \text{Gate length (Lg)}$

Drain current: $I_d \propto \frac{1}{\text{Gate length (Lg)}}$

$Lg \rightarrow \text{small},$

Then, $I_g \rightarrow \text{small}, I_d \rightarrow \text{large},$  Thus, $I_g/I_d \rightarrow \text{very small}$

$Lg = 10 \, \mu m$  
$Lg = 5 \, \mu m$  
$Lg = 1.0 \, \mu m$  
$Lg = 0.1 \, \mu m$
Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!
Some one will think for you

Do not believe a text book statement, blindly!
Transistor Scaling Continues

Qi Xinag, ECS 2004, AMD
Downsizing limit?

Channel length?

10 nm

Electron wave length
5 nm gate length CMOS Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC

IEDM, 2003
Electron wave length

10 nm

Tunneling distance

3 nm

Downsizing limit!
Channel length
Gate oxide thickness
Prediction now!

Electron wave length: 10 nm

Tunneling distance: 3 nm

Atom distance: 0.3 nm

MOSFET operation: $L_g = 2 \sim 1.5$ nm?

Below this, no one knows future!
However, Gate oxide thickness 2 orders magnitude smaller Close to limitation!!

Lg: Gate length downsizing will continue to another 10-15 years
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
So, we are now in the limitation of downsizing.
High-k
There is a solution! To use high-k dielectrics

Thin gate SiO$_2$

Thick gate high-k dielectrics

K=4
Almost the same
electric characteristics

K=20
Thick
Small
leakage
Current

However, very difficult and big challenge!
Remember MOSFET had not been realized without Si/SiO$_2$!
Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>Unstable at Si interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Si + MOₓ M + SiO₂</td>
</tr>
<tr>
<td>Li, Be</td>
<td>Si + MOₓ MSiₓ + SiO₂</td>
</tr>
<tr>
<td>Na, Mg</td>
<td>Si + MOₓ M + MSiₓOᵧ</td>
</tr>
</tbody>
</table>

- Gas or liquid at 1000 K
- Radio active

<table>
<thead>
<tr>
<th>He</th>
<th>Ne</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>C</td>
</tr>
<tr>
<td>N</td>
<td>O</td>
</tr>
<tr>
<td>F</td>
<td>Al</td>
</tr>
<tr>
<td>Si</td>
<td></td>
</tr>
</tbody>
</table>

HfO₂ based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Band offset

Si

Oxide

Dielectric Constant

Conduction band offset vs. Dielectric Constant

Si Band Gap

SiO₂

Band Discontinuity [eV]

XPS measurement by Prof. T. Hattori, INFOS 2003
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness
For the past 45 years SiO₂ and SiON have been used as gate insulators. Today, EOT = 1.0 nm.

EOT Limit: 0.7 to 0.8 nm

EOT can be reduced further beyond 0.5 nm by using direct contact to Si. This is achieved by choosing appropriate materials and processes.

Introduction of High-k materials, such as HfO₂, allows for EOT to be reduced to 0.5~0.7 nm.

Direct Contact Of high-k and Si

Still SiO₂ or SiON is used at the Si interface.

One order of Magnitude
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O* $\rightarrow$ HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 6131

SiO$_x$-IL is formed after annealing
Oxygen control is required for optimizing the reaction

D.J. Lichtenwalner, Trans. ECS 11, 319
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$

La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Gate Leakage vs EOT, \((V_g=|1|V)\)
EOT=0.37nm
La2O3

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

0.48 → 0.37nm Increase of $I_d$ at 30%
$\mu_{\text{eff}}$ of W/La$_2$O$_3$ and W/HfO$_2$ nFET on EOT

- W/La$_2$O$_3$ exhibits higher $\mu_{\text{eff}}$ than W/HfO$_2$
- $\mu_{\text{eff}}$ start degrades below EOT=1.4nm
1. Precise control of high-k/Si interface
Scaling limit in EOT

SiO$_x$ interfacial layer (typ. 0.5~0.7nm)

Si

Hf based oxide

Scaling in EOT

Excess gate leakage

SiO$_2$ interfacial layer
- recovery of degraded mobility
- interface state, reliability (TDDB, BTI), etc.

SiO$_2$-IL free structure (direct contact of high-k/Si) is required for EOT=0.5nm
Benefit of EOT scaling

Poly-Si ($10^{20}$ cm$^{-3}$) depletion: $\Delta$EOT=0.3 nm

K. Henson et al., IEDM 2008, p.91

M. Khare IEDM 10 Short Course

EOT scaling with High-k/Metal Gate

Suppression of SCE & $V_{th}$ variability
Direct contact of high-k/Si

K. Kakushima, et al., ESSDERC2009

Our approach

Control of oxygen atoms

Direct HfO$_2$/Si structure

La$_2$O$_3$ can easily achieve direct contact of high-k/Si

La$_2$O$_3$ + Si + nO$_2$

- La$_2$SiO$_5$
- La$_{10}$(SiO$_4$)$_6$O$_3$
- La$_{9.33}$Si$_6$O$_{26}$
- La$_2$Si$_2$O$_7$

K. Kakushima, et al., ESSDERC2009

Precise control of interface is indispensable

- Small interface state density
  Reliability, Mobility
- Control of silicate reaction
  EOT scaling

Superior interfacial property and Scaled EOT
2. High temperature annealing for small interface state density
Experimental procedure

- LOCOS isolated Si wafer (S/D pre-formed)
- SPM and HF cleaning
- La$_2$O$_3$ deposition (300°C)
- Gate metal (W) deposition by RF sputtering
- Gate patterning
- Post metallization annealing in FG (H$_2$:N$_2$=3%:97%) for 30min
- Contact hole and Al wiring
- Backside Al contact
- Measurement

Frequency dispersion of C-V curves

A fairly nice La-silicate/Si interface can be obtained with high temperature annealing. (800°C)
A small $D_{it}$ of $1.6 \times 10^{11}$ cm$^{-2}$/eV, results in better electron mobility.
Physical mechanisms for small $D_{it}$

- silicate-reaction-formed fresh interface
- stress relaxation at interface

Fresh interface with silicate reaction

FGA800°C is necessary to reduce the interfacial stress


Annealing temperature on EOT

EOT increase with increasing annealing temperature

Excess La-silicate formation
3. Metal Inserted Poly-Si (MIPS) stacks with high temperature annealing

~ Solution ~
Si (100nm)
TiN (10nm)
W (5nm)
La-silicate
Si sub.

Si (100nm)
→ Suppression of oxygen diffusion
TiN (10nm)
→ Barrier for reaction between Si and W
W (5nm)
→ Oxygen supply to gate dielectrics

LOCOS isolated p-Si wafer (S/D pre-formed)

- SPM and HF cleaning
- La$_2$O$_3$ deposition (300ºC)
- W deposition (5nm)
  by RF sputtering
  - TiN deposition (10nm)
    by RF sputtering (Ar:N$_2$=9:1)
  - Si deposition (100nm)
    by RF sputtering
- Gate patterning
- Post metallization annealing (PMA) in FG (H$_2$:N$_2$=3:97% ) at 800ºC for 30min
  - Si removal by TMAH for electrical measurement
- S/D & Backside Al contact
- FGA (H$_2$:N$_2$=3:97% ) at 420ºC for 30min

MIPS with high temperature annealing
Increasing EOT caused by high temperature annealing can be dramatically suppressed by MIPS stacks.
Cross sectional TEM images

$W$

$\text{TiN/W}$

$\text{MIPS}$

$K_{av} \sim 8$

$K_{av} \sim 12$

$K_{av} \sim 16$

No interfacial layer can be confirmed in MIPS stacks
EOT of 0.62nm and 155 cm²/Vsec at 1MV/cm can be achieved.
Benchmark of La-silicate dielectrics

Gate leakage is two orders of magnitude lower than that of ITRS

Electron mobility is comparable to record mobility with Hf-based oxides
Metal (Silicide) S/D
**Introduction - Schottky Barrier FET**

**Extreme scaling in MOSFET**
- Dopant abruptness at S/D
- $V_t$ and $I_{ON}$ variation
- GIDL

---

**Metal Schottky S/D junctions**
- Atomically abrupt junction
- Lowering S/D resistances
- Low temperature process for S/D

Schottky Barrier FET is a strong candidate for extremely scaled MOSFET
Issues in metal silicide S/D

**Surface or interface control**

**Diffusion species:** metal atom (Ni, Co)
- Rough interface at silicide/Si
  - Excess silicide formation
  - Different $\phi_B$ presented at interface
  - Process temperature dependent composition

**Diffusion species:** Si atom (Ti)
- Surface roughness increases
  - Line dependent resistivity change

Annealing: 650 °C
Si(001) sub. Epitaxial NiSi$_2$


CoSi$_2$ NiSi TiSi$_2$

Line width of 0.1 µm

Aglomeration

Issues in metal silicide S/D

Unwanted leakage current
- Edge leakage current at periphery
- Generation current due to defects in substrate

Variable leakage current in smaller contact

Specification for metal silicide S/D
- Atomically flat interface with smooth surface
- Suppressed leakage current
- Stability of silicide phase and interface in a wide process temperature

Annealing: 500 °C

\( V_{\text{app}} = -0.2 \text{V} \)
\( \phi_{Bn} = \sim 0.57 \text{ eV} \)

Current density (A/cm²)

<table>
<thead>
<tr>
<th>Length of a contact side (µm)</th>
<th>Ni silicide/Si diodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>10⁻³</td>
</tr>
<tr>
<td>10²</td>
<td>10⁻²</td>
</tr>
</tbody>
</table>

Variable leakage current in smaller contact
Process technology to form NiSi$_2$ is the key to obtain atomically flat silicide/Si interface.

Reports on atomically flat silicide/Si


Silicidation with nitrogen-doped in Ni films

Annealing: 500 ºC

Silicidation with ultra-thin Ni films (< 3-nm)

Annealing: 500 ºC

Grain boundary diffusion

Lattice diffusion

Poly-crystalline NiSi

Epitaxial NiSi$_2$

Residual Ni

Epitaxial NiSi$_2$

w/o nitrogen

with nitrogen

NiSi$_2$

SSOI

NiSi$_2$

SOI

850 ºC

850 ºC
Stability and structure dependence on silicidation


Annealing time/temperature and structure of Si influence the silicidation
Our approach for flat silicide/Si interface

Deposition of Ni film

- Deposition of Ni film
- Annealing
- Ni-silicide
- Si substrate

Rough interface

Deposition from NiSi₂ source

- Deposition from NiSi₂ source
- Annealing
- Ni-silicide
- Si substrate

No Si substrate consumption
Flat interface

Deposition of Ni-Si mixed films from NiSi₂ source

- No consumption of Si atoms from substrate
- No structural size effect in silicidation process
- Stable in a wide process temperature range
Fabrication process of the Schottky diodes

- n-type Si substrate, Si(100) with 400 nm SiO$_2$ isolation
  Doping concentration : $3 \times 10^{15}$ cm$^{-3}$

- SPM and HF cleaning
- Diode patterning by photolithography and BHF etching of SiO$_2$
- Deposition of 10-nm-thick NiSi$_2$ and Ni sources by RF sputtering in Ar atmosphere
- Ni silicidation by Rapid Thermal Annealing (RTA) in N$_2$ atmosphere
- Al contact deposition on substrate backside by thermal evaporation

- Measurement of electrical characteristics
- SEM and TEM observation
- XRD and XPS analysis
SEM views of silicide/Si interfaces

Ni source (50nm) | NiSi₂ source (50nm)

- Rough interfaces
- Consumed Si substrate
- Thickness increase ~100 nm

Ni source

- Atomically flat interfaces
- No Si consumption
- Temperature-independent

NiSi₂ source
Silicidation with narrow Si Fins

Top views

20-nm-thick Ni and NiSi₂ sources

Diffusion of Ni atoms

Encroached Ni silicide

Annealing: 500 °C, Fins height: 30nm

Complete suppression of encroachment

No structural dependency with NiSi₂ source

- advantage for scaled MOSFET (Fin, SiNW, etc.)
J-V characteristics of the Schottky diodes

Ideal characteristics ($n = 1.00$, suppressed leakage current)

- Flat interface and No Si substrate consumption
- No defects in Si substrate

NiSi$_2$ source

Suppressed reverse leakage current

<table>
<thead>
<tr>
<th>Source</th>
<th>$\phi_B$ (eV)</th>
<th>n</th>
</tr>
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<tbody>
<tr>
<td>Ni</td>
<td>0.676</td>
<td>1.08</td>
</tr>
<tr>
<td>NiSi$_2$</td>
<td>0.659</td>
<td>1.00</td>
</tr>
</tbody>
</table>

RTA: 500$^\circ$C, 1min
Annealing temperature dependent Schottky diode characteristics

Annealing temperature (°C)

- At 400 °C
  \( n = 1.03, \phi_{Bn} = 0.655 \text{ eV} \)

- At 450 and 500 °C
  \( n = 1.00, \phi_{Bn} = 0.66 \text{ eV} \)

Around 500 °C is in order
Annealing time dependent Schottky diode characteristics

NiSi$_2$ source

Good stability of SBH ($\phi_{Bn}$) and $n$-factor

$\phi_{Bn} = \sim 0.66$ eV
$n = 1.00\sim 1.02$

Stable against annealing time
Sheet resistances of the Ni-silicide films

At thermally stable temperature range: $\rho_{sh} = 120\sim160 \, \mu\Omega\cdot\text{cm}$

Although the silicide film with NiSi$_2$ source showed relatively larger $\rho_{sh}$, the film is thermally stable up to 800 °C.
TEM observation of silicide film from NiSi$_2$ source

Si and NiSi$_2$ can be matched together with lattice mismatch $\sim 0.4\%$

Thin epitaxially grown layer ($\sim 1$nm) was formed on the substrate

This phase can be assumed NiSi$_2$

Atomically flat interface with smooth surface
XPS analysis of silicide film from NiSi$_2$ source

Ni$_{2p3/2}$ binding energy is 7938.57 eV.

NiSi$_2$ source mainly appeared and a little Ni-rich phases.
XRD analysis of silicide film from NiSi$_2$ source

After high temperature annealing (850 °C)

The peaks indicated NiSi$_2$

| Peak 2θ (deg.) | 28.63 | 47.62 |

Grazing angle XRD (2θ measurement)

850°C-annealing
Summary of the silicide phases with NiSi$_2$ source

- Ni-rich phases in the silicide layer are maintained with NiSi$_2$ source

- No distinct structure change at the interface
  - Stable $\phi_{Bn}$ and $n$-factor
  - No structural effect for silicidation
Question:
How far we can go with downscaling?
How far can we go?

**Past**
0.7 times per 3 years
1970年
10μm → 8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm → 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm → 32nm

**Now**
In 40 years: 18 generations,
Size 1/300, Area 1/100,000

**Future**
→ (28nm) → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

- At least 4.5 generations to 8nm
- Hopefully 8 generations
HP, LOP, LSTP for Logic CMOS

Subthreshold Leakage ($A/\mu m$) vs. Operation Frequency (a.u.)

- **HP CMOS** (high Performance)
  - Highest Ion, Lowest CV/I
  - High leakage
  - Medium Vdd

- **LOP CMOS** (Low Operation Power)
  - Lowest Vdd
  - Medium Ion, medium CV/I
  - Medium leakage

- **LSTP CMOS** (Low Standby Power)
  - Lowest leakage
  - Low Ion, high CV/I
  - High Vdd

Source: 2007 ITRS Winter Public Conf.
Scaling Method: by R. Dennard in 1974

$W_{dep}$: Space Charge Region (or Depletion Region) Width

- $W_{dep}$ has to be suppressed
- Otherwise, large leakage between S and D

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

K=0.7 for example

$W_{dep} \propto \sqrt{V/Na}$

Good scaled I-V characteristics
Scaling of high beyond 0.5 nm is important

Power of FET = \( CV^2/2 \cdot D^3 (=L^3) \)

Problems
→ SCE
→ Variation in Vth
→ Increase in Off-leakage current

Solution

Planar Bulk & Poly-Si/SiON
\( T_{inv}=2.5 \text{nm} \)
\( N_A=3E18 \)

Planar Bulk & Metal/High-k
\( T_{inv}=1.8 \text{nm} \)
\( N_A=1.5E18 \)

Normalized \( \sigma V_{th} \)

ITRS2007
Because of off-leakage control, Planar $\rightarrow$ Fin $\rightarrow$ Nanowire

Planar FET

Fin FET

Nanowire FET
Down scaling is the most effective way of Power saving.

It has been always discussed about the limit of downscaling, but the down scaling of MOSFETs is still possible for another 10 or 20 years!

3 important technological items for DS.

1. Thinning of high-k beyond 0.5 nm

2. Metal S/D

3. Si-Nanowire FET
Si nanowire
Nanowire structures in a wide meaning
Nanowire FET

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<td>Planar bulk</td>
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<td>FDSOI</td>
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<td>Multiple Gate</td>
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2015

22 or 16nm node

Multiple Gate (Fin) FET

2020

11 or 8nm node

Nanowire FET

ITRS 2009

Bulk □ Fin □ Nanowire

Scaling Pathways

Bulk or SOI → Fin

Si Nanowire
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of $I_{OFF}$
3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Maximum number of wires per 1 µm

Front gate type MOS 165 wires /µm

Surrounded gate type MOS 33 wires/µm

- Metal gate electrode (10nm)
- High-k gate insulator (4nm)
- Si Nano wire (Diameter 2nm)

6nm pitch
By nano-imprint method

30nm pitch:
EUV lithography

Surrounded gate MOS
Device fabrication

Si/Si$_{0.8}$Ge$_{0.2}$ superlattice epitaxy on SOI

Anisotropic etching of these layers

Isotropic etching of SiGe

The NW diameter is controllable down to 5 nm by self limited oxidation.

SiN HM

Box

Gate depositions
HfO$_2$ (3nm)
TiN (10nm)
Poly-Si (200nm)

Gate etching

S/D implantation
Spacer formation
Activation anneal
Salicidation

Standard Back-End of-Line Process

Process Details:
C. Dupre et al.,
3D-stacked Si NWs with Hi-\textit{k}/MG

Wire direction: \textit{<110>}
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT \sim 2.6 nm
SiNW Band structure calculation
Cross section of Si NW

First principal calculation,

D=1.96nm [001]  
D=1.94nm [011]  
D=1.93nm [111]
Si nanowire FET with 1D Transport

Orientation | [001] | [011] | [111]
Diameter (nm) | 0.86 | 0.94 | 0.89

(a)

Energy (eV)

Wave Number

Small mass with [011]

Large number of quantum channels with [001]
Atomic models of a Si quantum dot and Si nanowires

6.6 nm diameter SiQD
(8651 atoms)

10 nm diameter Si(100)NW
(2341 atoms)

20 nm diameter Si(100)NW
(8941 atoms)
Kohn-Sham eq. (finite-difference)

\[
\left( -\frac{1}{2} \nabla^2 + v_s[\rho](\mathbf{r}) + \hat{v}_{nloc}^{PP}(\mathbf{r}) \right) \phi_n(\mathbf{r}) = \varepsilon_n \phi_n(\mathbf{r})
\]

Higher-order finite difference

\[
\frac{\partial^2}{\partial x^2} \psi_n(x, y, z) \approx \sum_{m=-6}^{6} C_m \psi_n(x + m\Delta x, y, z)
\]

Integration

\[
\int \psi_m(\mathbf{r}) \psi_n(\mathbf{r}) d\mathbf{r} \approx \sum_{i=1}^{Mesh} \psi_m(\mathbf{r}_i) \psi_n(\mathbf{r}_i) \Delta x \Delta y \Delta z
\]
Massively Parallel Computing

with our recently developed code “RSDFT”

Iwata et al, J. Comp. Phys., to be published

Real-Space Density-Functional Theory code (RSDFT)

Based on the finite-difference pseudopotential method (J. R. Chelikowsky et al., PRB1994)

Highly tuned for massively parallel computers

Computations are done on a massively-parallel cluster PACS-CS at University of Tsukuba.
(Theoretical Peak Performance = 5.6GFLOPS/node)

e.g.) The system over 10,000 atoms $\text{Si}_{10701}\text{H}_{1996}$
(7.6 nm diameter Si dot)

Convergence behavior for $\text{Si}_{10701}\text{H}_{1996}$

Grid points = 3,402,059
Bands = 22,432

Computational Time (with 1024 nodes of PACS-CS)

6781 sec. $\cdot$ 60 iteration step = 113 hour
Band Structure and DOS of Si(100)NWs (D=1nm, 4nm, and 8nm)

D=1 nm
Si21H20 (41 atoms)
KS band gap=2.60eV

D = 4 nm
Si341H84 (425 atoms)
KS band gap = 0.81eV

D=8 nm
Si1361H164 (1525 atoms)
KS band gap=0.61eV

KS band gap of bulk (LDA) = 0.53eV
SiNW Band compact model
Landauer Formalism for Ballistic FET

\[ I_D = \frac{q}{\pi \hbar} \sum_i \int [f(E, \mu_S) - f(E, \mu_D)] T_i(E) dE \]

From \( x_{\text{max}} \) to \( x_{\text{min}} \) \( T_i(E) \approx 1 \)

\[ I_D = G_0 \left( \frac{k_B T}{q} \right) \sum_i g_i \ln \left\{ \frac{1 + \exp\left[ (\mu_S - E_{i0}) / k_B T \right]}{1 + \exp\left[ (\mu_D - E_{i0}) / k_B T \right]} \right\} \]
IV Characteristics of Ballistic SiNW FET

Small temperature dependency
35 \mu A/wire for 4 quantum channels
Model of Carrier Scattering

Linear Potential Approx. : Electric Field $E$

Transmission Probability to Drain

$$T(\varepsilon) = \frac{F(0) - G(0)}{F(0)}$$

Injection from Drain $= 0$
Résumé of the Compact Model

\[ I = \frac{q}{\pi \hbar} \sum_i g_i \int [f(\varepsilon, \mu_s) - f(\varepsilon, \mu_D)] T_i d\varepsilon \]

\[ (V_G - V_t) - \alpha \frac{\mu_s - \mu_0}{q} = \frac{Q_f + Q_b}{C_G}. \]

\[ \mu_s - \mu_D = qV_D \]

\[ C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left( \frac{\sqrt{2r + t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r + t_{ox}} - \sqrt{t_{ox}}} \right)}. \]

Planar Gate

\[ C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left( \frac{r + t_{ox}}{r} \right)}. \]

GAA

\[ |Q_f + Q_b| = \frac{q}{\pi} \sum_i g_i \left[ \int_{-\infty}^{\infty} \frac{dk}{1 + \exp \left( \frac{\varepsilon_i(k) - \mu_S}{k_B T} \right)} - \int_{-\infty}^{0} \frac{1}{1 + \exp \left( \frac{\varepsilon_i(k) - \mu_S}{k_B T} \right)} + \int_{0}^{1} \frac{1}{1 + \exp \left( \frac{\varepsilon_i(k) - \mu_D}{k_B T} \right)} \right] T_i(\varepsilon_i(k)) dk \]

Planar Gate

Planar Gate

(Carrier distribution in Subbands)

\[ T(\varepsilon) = \frac{\sqrt{2D_0} qE}{\left( \sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0} B_0 \ln \left( \frac{qE x_0 + \varepsilon}{\varepsilon} \right)} \]

Unknowns are \( I_D, (\mu_S - \mu_0), (\mu_D - \mu_0), (Q_f + Q_b) \)
Electric current 20~25 µA
No saturation at Large $V_D$
SiNW FET Fabrication
SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oxide etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

Standard recipe for gate stack formation
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

(a) $V_g-V_{th}=1.0 \text{ V}$

(b) $V_d=-1 \text{ V}$, $V_{th}=1 \text{ V}$

On/Off $>10^6$, 60uA/wire

$L_g=65\text{nm}$, $T_{ox}=3\text{nm}$
Bench Mark

- Gate Length (nm)
- $I_{ON} (\mu A / \text{wire})$
- VDD: 1.0~1.5 V

- Our Work
### Bench Mark

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<tbody>
<tr>
<td>NW Size (nm)</td>
<td>Rect.</td>
<td>Rect.</td>
<td>Rect.</td>
<td>Cir.</td>
<td>Cir.</td>
<td>Elliptical</td>
<td>Elliptical</td>
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<tr>
<td>Lg (nm)</td>
<td>65</td>
<td>25</td>
<td>100</td>
<td>30</td>
<td>8</td>
<td>65</td>
<td>35</td>
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<tr>
<td>EOT or Tox (nm)</td>
<td>3</td>
<td>1.8</td>
<td>1.8</td>
<td>2</td>
<td>4</td>
<td>3</td>
<td>1.5</td>
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<tr>
<td>Vdd (V)</td>
<td>1.0</td>
<td>1.1</td>
<td>1.2</td>
<td>1.0</td>
<td>1.2</td>
<td>1.2</td>
<td>1.0</td>
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<tr>
<td>Ion (μA) per wire</td>
<td>60.1</td>
<td>102</td>
<td>30.3</td>
<td>26.4</td>
<td>37.4</td>
<td>48.4</td>
<td>43.8</td>
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<td>Ion (μA/μm) by dia.</td>
<td>3117</td>
<td>5010</td>
<td>2170</td>
<td>2640</td>
<td>3740</td>
<td>4030</td>
<td>2592</td>
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<td>Ion (μA/μm) by cir.</td>
<td>1609</td>
<td>2054</td>
<td>430</td>
<td>841</td>
<td>1191</td>
<td>1283</td>
<td>825</td>
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<tr>
<td>SS (mV/dec.)</td>
<td>70</td>
<td>79</td>
<td>68</td>
<td>71</td>
<td>75</td>
<td>~75</td>
<td>85</td>
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<tr>
<td>DIBL (mV/V)</td>
<td>62</td>
<td>56</td>
<td>15</td>
<td>13</td>
<td>22</td>
<td>40-82</td>
<td>65</td>
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<tr>
<td>Ion/Ioff</td>
<td>~1E6</td>
<td>&gt;1E6</td>
<td>&gt;1E5</td>
<td>~1E6</td>
<td>&gt;1E7</td>
<td>&gt;1E7</td>
<td>~2E5</td>
</tr>
</tbody>
</table>

Ref[11] by Stmicro Lg=25nm, Tox=1.8nm
This work Lg=65nm, Tox=3nm
This work

$I_{ON}/I_{OFF}$ Bench mark

Planer FET ▲
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

SiナノワイヤFET ★
Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240

$V_{gs}$

This work

$L_g=500\sim65$nm

$0$ $500$ $1000$ $1500$ $2000$ $I_{ON}$ ($\mu$A/$\mu$m)

$10^{-3}$ $10^{-1}$ $1$ $10^1$ $10^2$ $10^3$ $I_{OFF}$ (nA/$\mu$m)
The graph shows the effective electron mobility (cm²/Vs) as a function of inversion carrier density (cm⁻²) for different configurations. The labels A₁ (12x19) and A₂ (12x28) indicate different sample configurations, with A₁ having a lower mobility due to reduced dimensions compared to A₂. The inset images illustrate the dimensions of the samples, with A₁ having a height (hNW) of 12 nm and width (wNW) of 19 nm, while A₂ has a height of 12 nm and width of 28 nm. The SOI Planar region with thickness (T_SOI) of 28 nm is also shown, indicating a 1 μm width (W) and a BOX layer thickness of 28 nm.
Primitive estimation!

- Small EOT for high-k (33)
- P-MOS improvement (26)
- Low S/D resistance (20)
- Assumption: $I_{ON} \propto L_g^{-0.5} \cdot T_{ox}^{-1}$

Graph showing $I_{ON}$ (µA/µm) vs Year with points for bulk, FD, ITRS, and MG.
Transistor Innovations Enable Technology Cadence

2003: 90 nm
Invented SiGe Strained Silicon

2005: 65 nm
2nd Gen. SiGe Strained Silicon

2007: 45 nm
Invented Gate-Last High-k Metal Gate

2009: 32 nm
2nd Gen. Gate-Last High-k Metal Gate

2011: 22 nm
First to Implement Tri-Gate

Strained Silicon
High-k Metal gate
Tri-Gate
22 nm 3-D Tri-Gate Transistor
Energy-Efficient Performance Built on Moore’s Law

Higher Transistor Performance (Switching Speed)

Lower Transistor Leakage

Lower Active Power

Active Power per Transistor (normalized)

Source: Intel

22 nm Tri-Gate transistors increase the benefit from a new technology generation

> 50% reduction
22nm Silicon Technology Breakthrough Benefits Broad Range of Intel Architecture Devices

New 22nm 3-D transistors deliver unprecedented performance improvement and power reduction for Intel’s product portfolio

- This benefits smallest handhelds to powerful cloud-based servers
- 37% performance increase at low voltage vs. 32nm planar transistors*
- Consumes only half the power at the same performance level as 2-D transistors on 32nm planar chips*
Our roadmap for R & D
Source: H. Iwai, IWJT 2008

Current Issues
Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Thank you for your attention!