Future of Si Nano-CMOS Technology

May 27, 2011

IEEE EDS: WIMNACT 29
@International Convention Hall,
Eng. Building 4,
National Chiao Tung University

Hiroshi Iwai,
Tokyo Institute of Technology

- There were many inventions in the 20th century:

  Airplane, Nuclear Power generation, Computer,

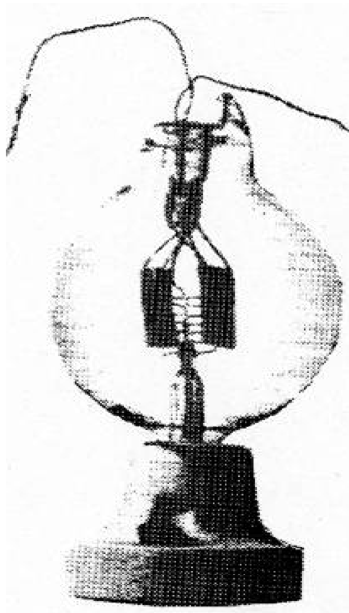
  Space aircraft, etc
- However, everything has to be controlled by electronics
- Electronics

  Most important invention in the 20th century
- What is Electronics: To use electrons,

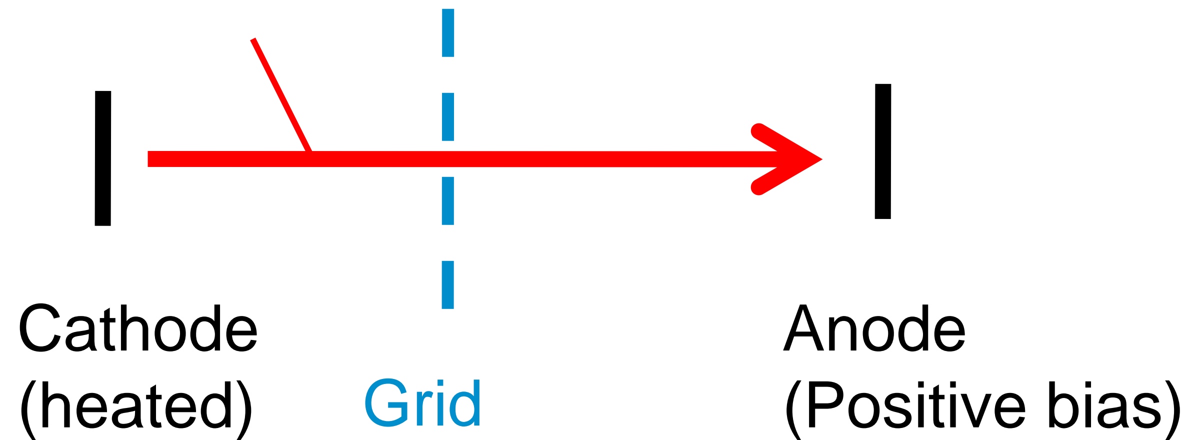
  Electronic Circuits

Lee De Forest

Electronic Circuits started by the invention of vacuum tube (Triode) in 1906



Thermal electrons from cathode controlled by grid bias



Same mechanism as that of transistor

First Computer Eniac: made of huge number of vacuum tubes 1946

Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

Needless to say, but….

CMOS Technology:

Indispensible for our human society

All the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:

There is no computer in banks, and

world economical activities immediately stop.

Cellarer phone dose not exists

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

→ **Increase clock frequency**

→ **Increase circuit operation speed**

2. **Increase number of Transistors**

→ **Parallel processing**

→ **Increase circuit operation speed**

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.

Question:

How far we can go with downscaling?

How far can we go?

Past

0.7 times per 3 years

In 40 years: 15 generations,
Size 1/200, Area 1/40,000

1973年

Now

8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm

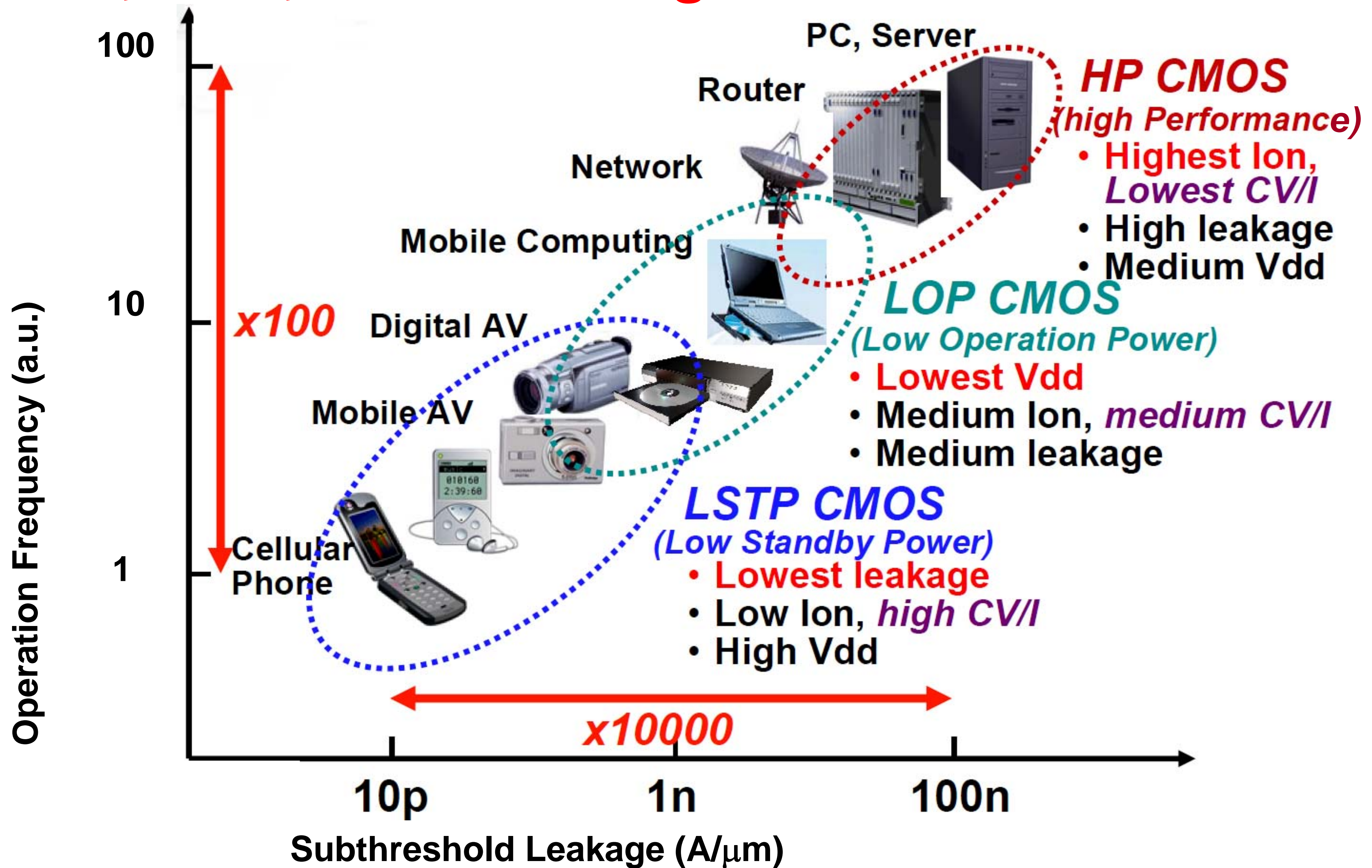
→ 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm

Future

→ 32nm → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

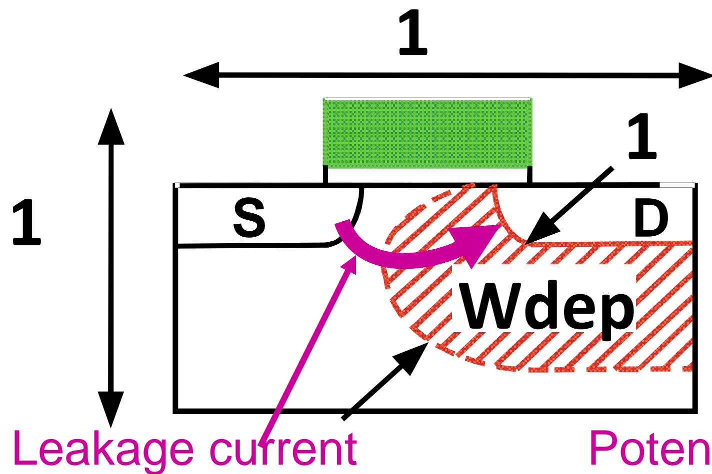
- **At least 5,6 generations, for 15 ~ 20 years**
- **Hopefully 8 generations, for 30 years**

HP, LOP, LSTP for Logic CMOS



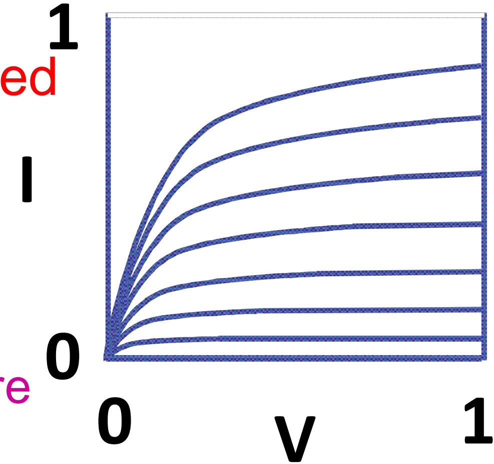
Source: 2007 ITRS Winter Public Conf.

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

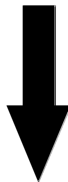
Wdep has to be suppressed
Otherwise, large leakage between S and D



Leakage current

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

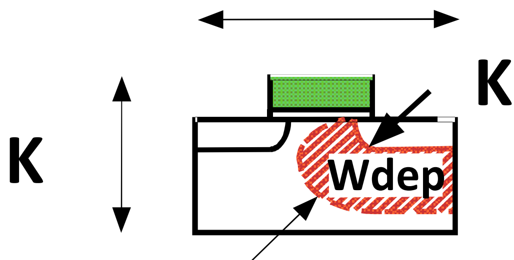
K=0.7 for example



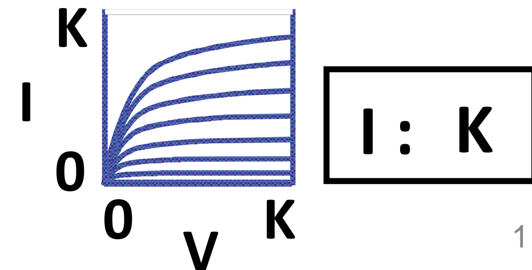
X , Y , Z : K, V : K, Na : 1/K

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$\text{Wdep} \propto \sqrt{V/Na}$$
: K

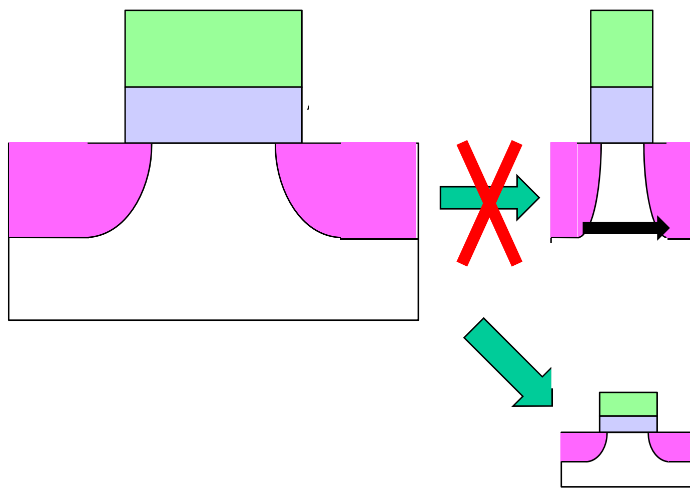


I : K

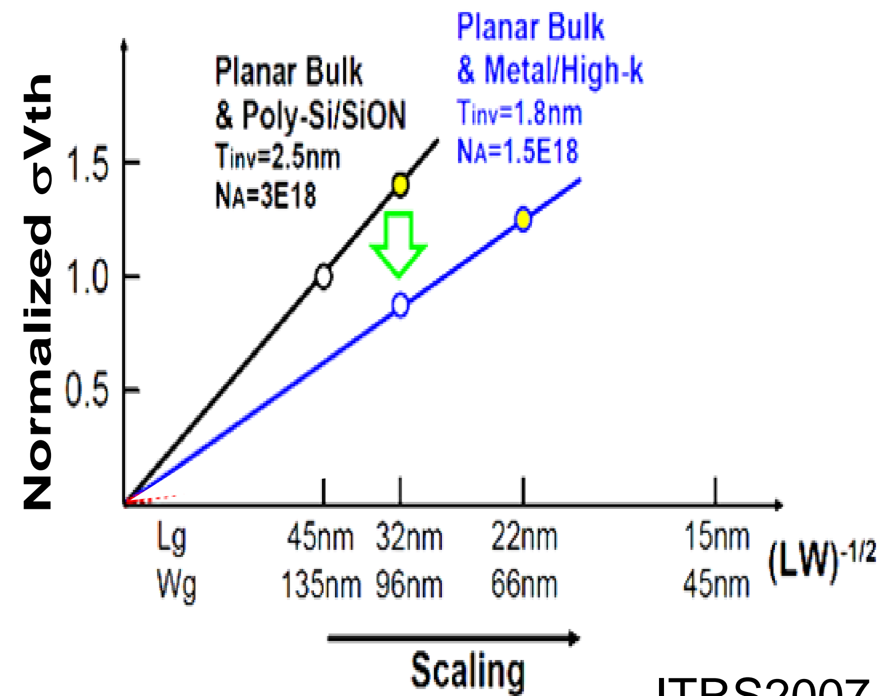
Scaling of high beyond 0.5 nm is important

Power of FET $= CV^2/2 \propto D^3$ $(=L^3)$

Problems
→SCE
→Variation in Vth
→Increase in Off-leakage current



Solution



ITRS2007

Down scaling is the most effective way of Power saving.

It has been always discussed about the limit of downscaling, but the down scaling of MOSFETs is still possible for another 10 or 20 years!

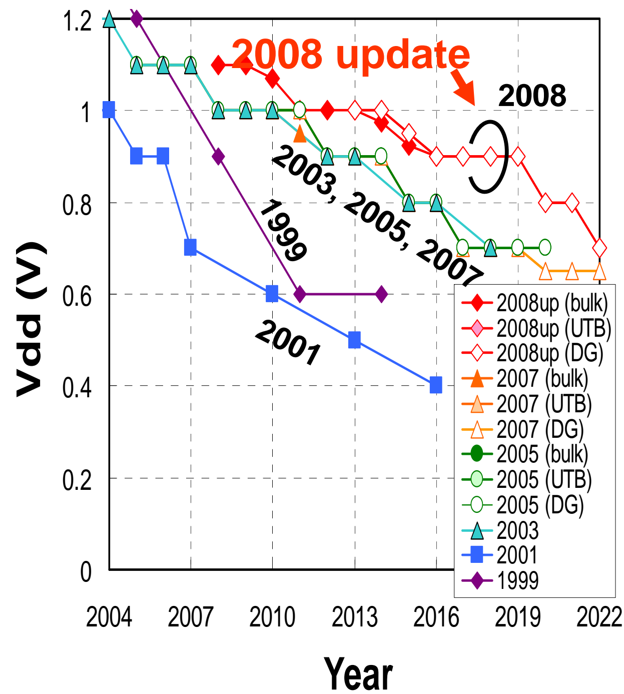
3 important technological items for DS.

1. Thinning of high-k beyond 0.5 nm
2. Metal S/D
3. Si-Nanowire FET

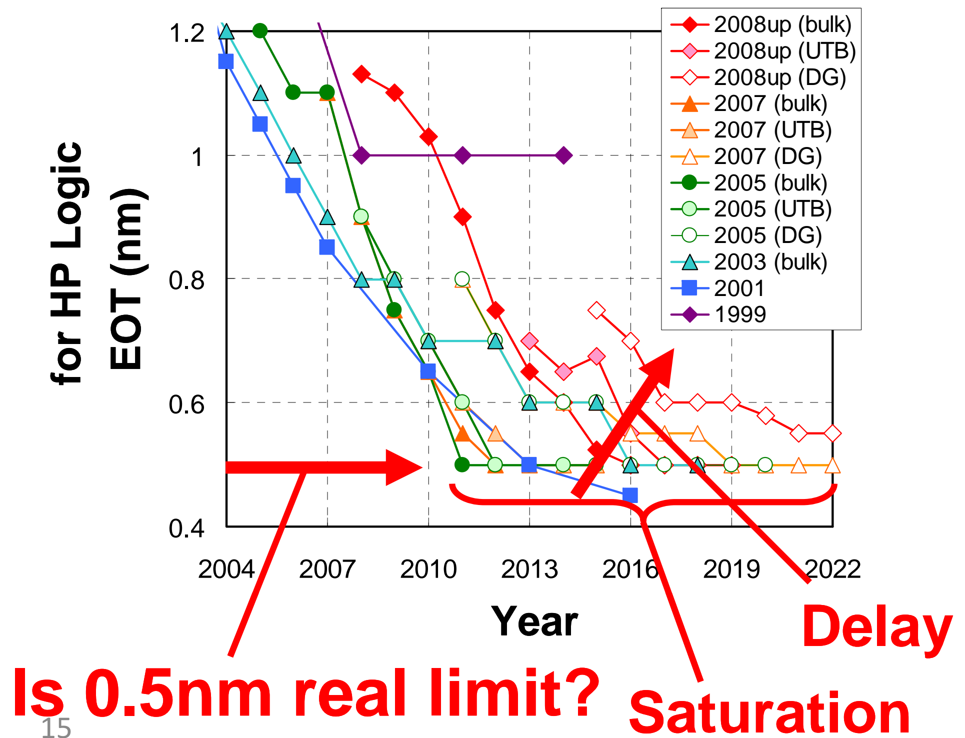
High k gate stack

ITRS

Vdd stay high



ITRS EOT limit = 0.5 nm?

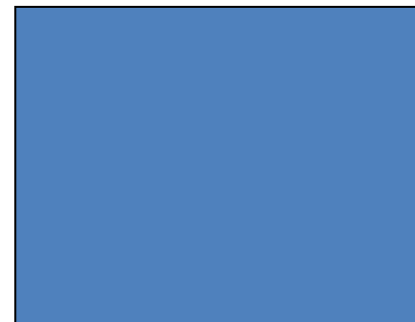


To use high-k dielectrics

K: Dielectric Constant

Thick gate high-k dielectrics

Thin gate SiO_2



Thick → Small leakage Current

Almost the same electric characteristics

However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO_2!

Choice of High-k elements for oxide

Candidates

● Gas or liquid at 1000 K

○ Radio active

Unstable at Si interface

① Si + MO_X M + SiO_2

② Si + MO_X MSi_X + SiO_2

③ Si + MO_X M + MSi_XO_Y

● H																	● He
Li	Be											● B	● C	● N	● O	● F	● Ne
① Na	Mg											Al	Si	● P	● S	● Cl	● Ar
K	Ca	Sc	② Ti	① V	① Cr	① Mn	① Fc	① Co	① Ni	① Cu	① Zn	① Ga	① Ge	● As	● Se	● Br	● Kr
● Rh	Sr	Y	Zr	① Nb	① Mo	Tc	① Ru	① Rb	① Pd	● Ag	① Cd	① In	① Sn	① Sb	① Te	● I	● Xe
● Cs	③ Ba	★	Hf	① Ta	① W	① Re	① Os	① Ir	● Pt	● Au	● Hg	● Tl	① Pb	① Bi	○ Po	○ At	○ Rn
○ Fr	○ Ra	☆	○ Rf	○ Ha	○ Sg	○ Ns	○ Hs	○ Mt									

★	La	Ce	Pr	Nd	○ Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
☆	○ Ac	○ Th	○ Pa	○ U	○ Np	○ Pu	○ Am	○ Cm	○ Bk	○ Cf	○ Es	○ Fm	○ Md	○ No	○ Lr

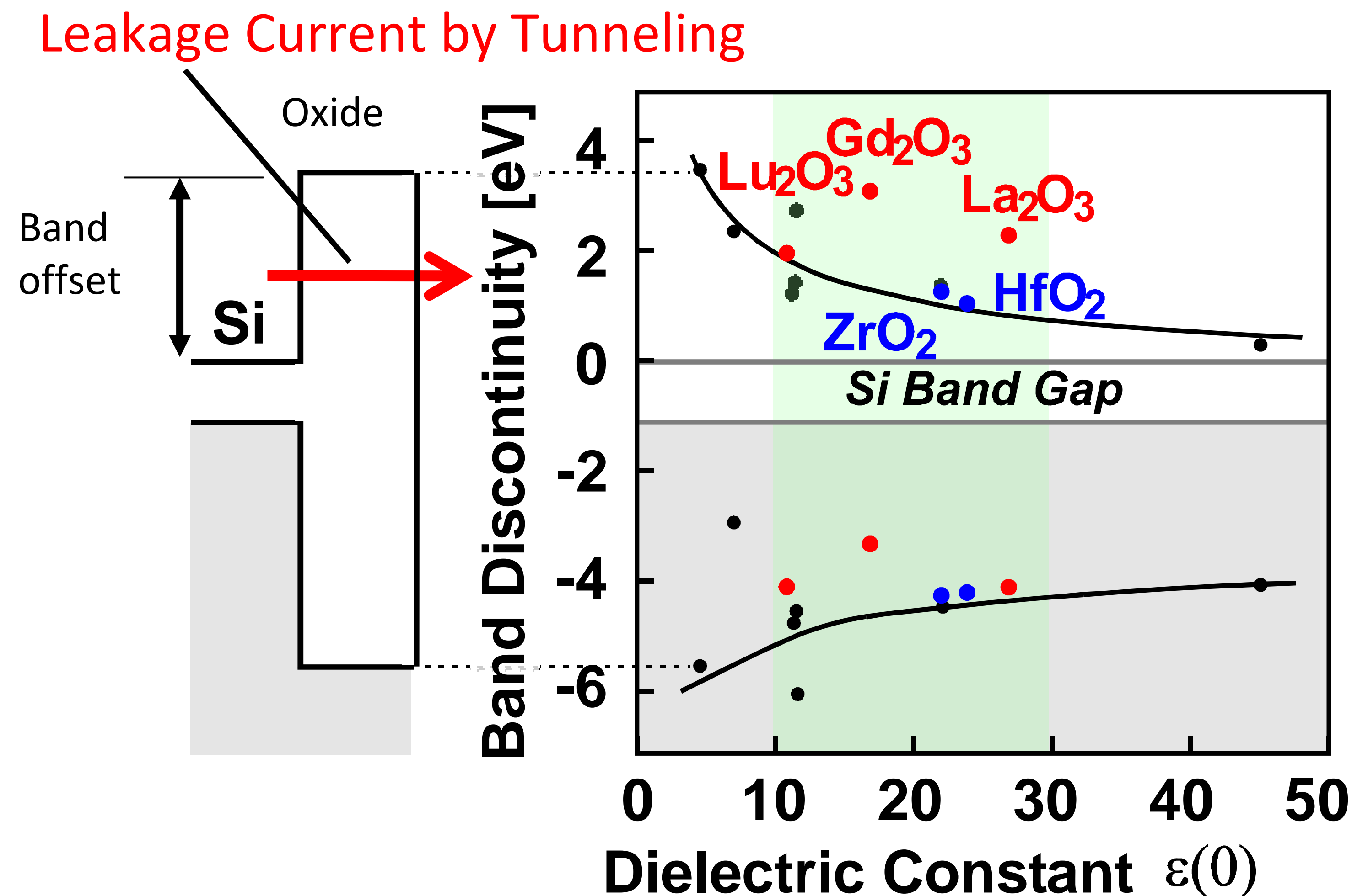
HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999

Hubbard and Schlom, J Mater Res 11 2757 (1996)

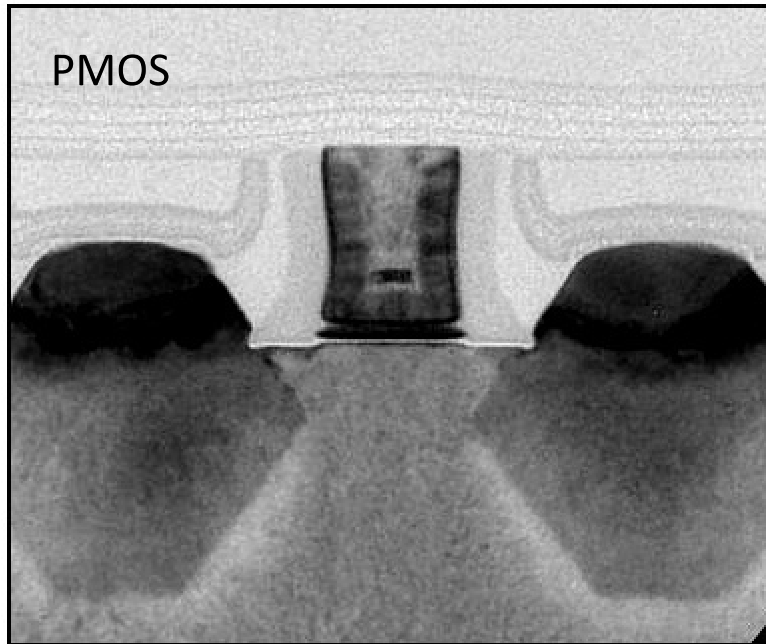
Conduction band offset vs. Dielectric Constant

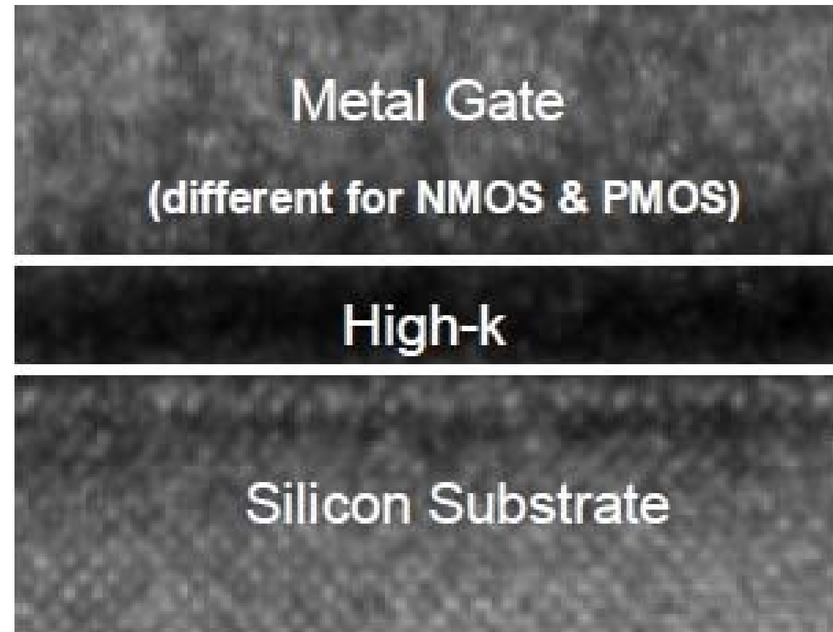


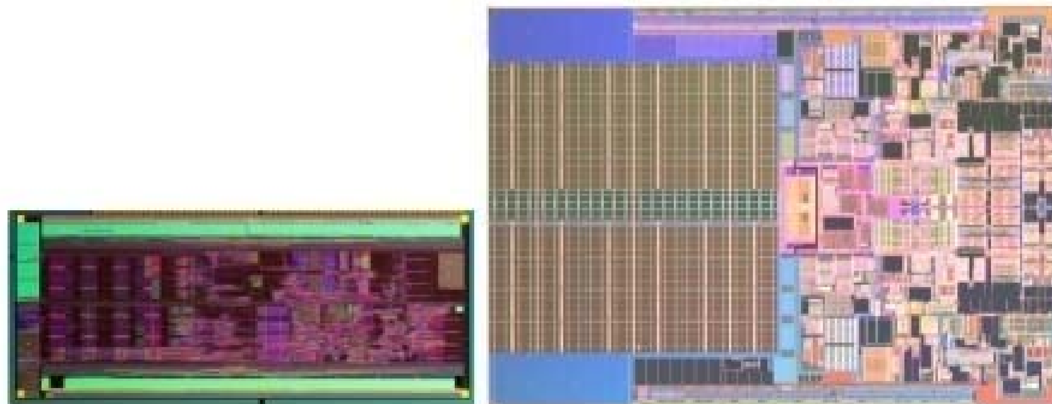
XPS measurement by Prof. T. Hattori, INFOS 2003

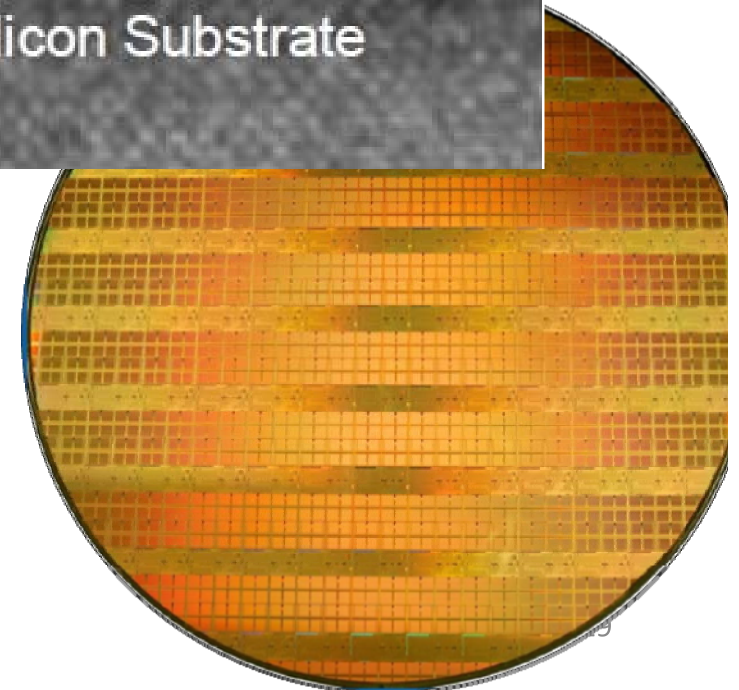
High-k gate insulator MOSFETs for Intel: EOT=1nm

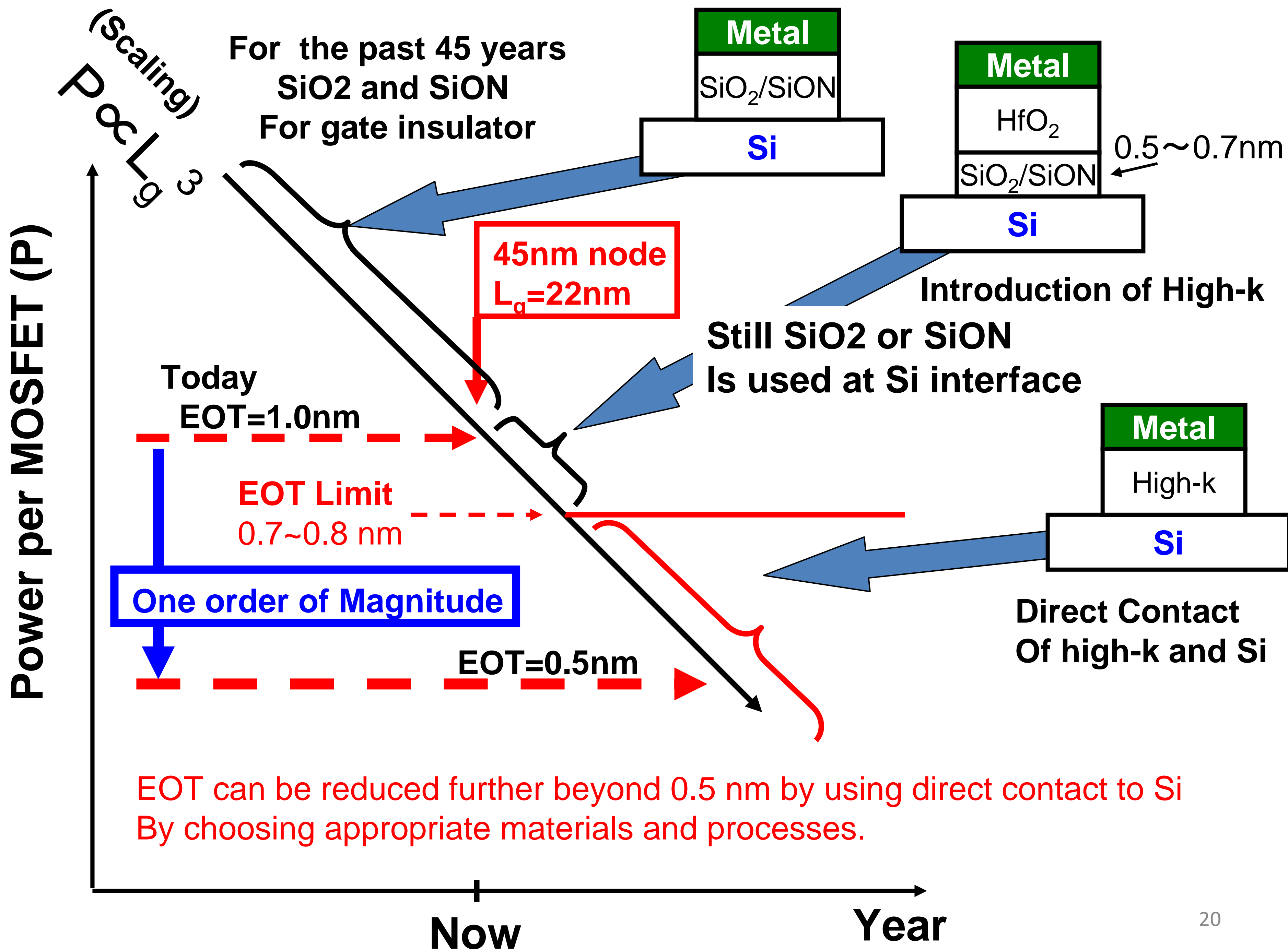
EOT: Equivalent Oxide Thickness







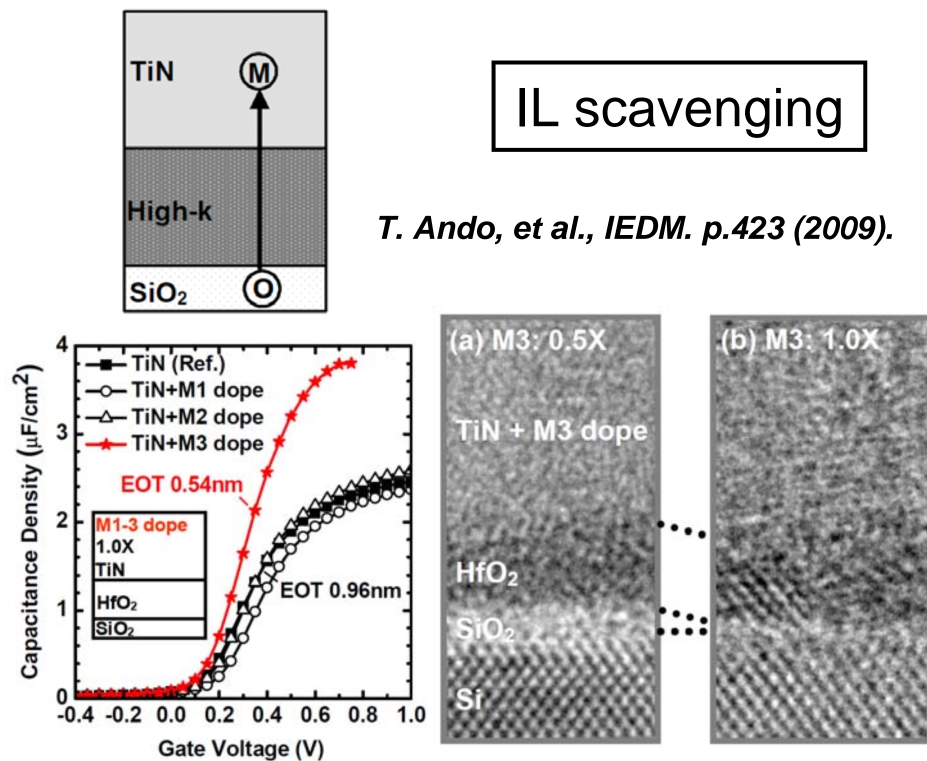



(Scaling)
P ∝ Lg3
Power per MOSFET (P)
For the past 45 years
SiO2 and SiON
For gate insulator
Metal
SiO2/SiON
Si
Metal
HfO2
0.5~0.7nm
SiO2/SiON
Si
Introduction of High-k
45nm node
Lg=22nm
Still SiO2 or SiON
Is used at Si interface
Today
EOT=1.0nm
EOT Limit
0.7~0.8 nm
Metal
High-k
Si
One order of Magnitude
Direct Contact
Of high-k and Si
EOT=0.5nm
EOT can be reduced further beyond 0.5 nm by using direct contact to Si
By choosing appropriate materials and processes.
Now
Year

Reports on direct contact of high-k/Si

IL scavenging

T. Ando, et al., IEDM. p.423 (2009).

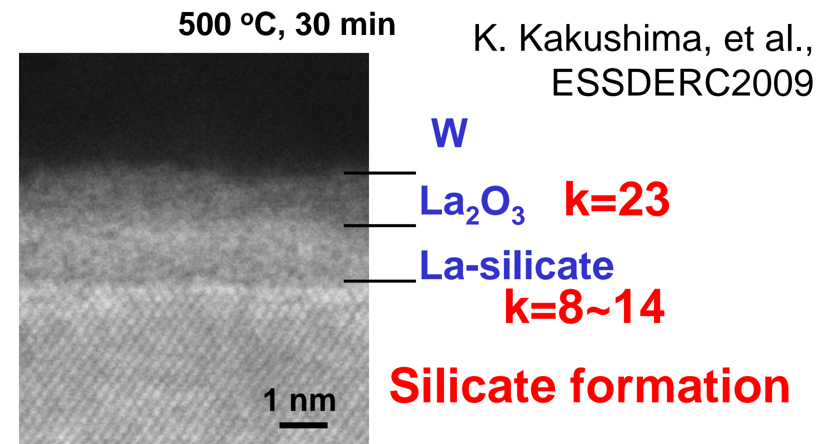


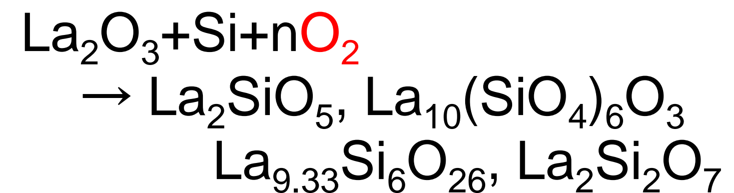
Control of oxygen atoms

Direct HfO_2/Si structure

Our approach

K. Kakushima, et al., ESSDERC2009

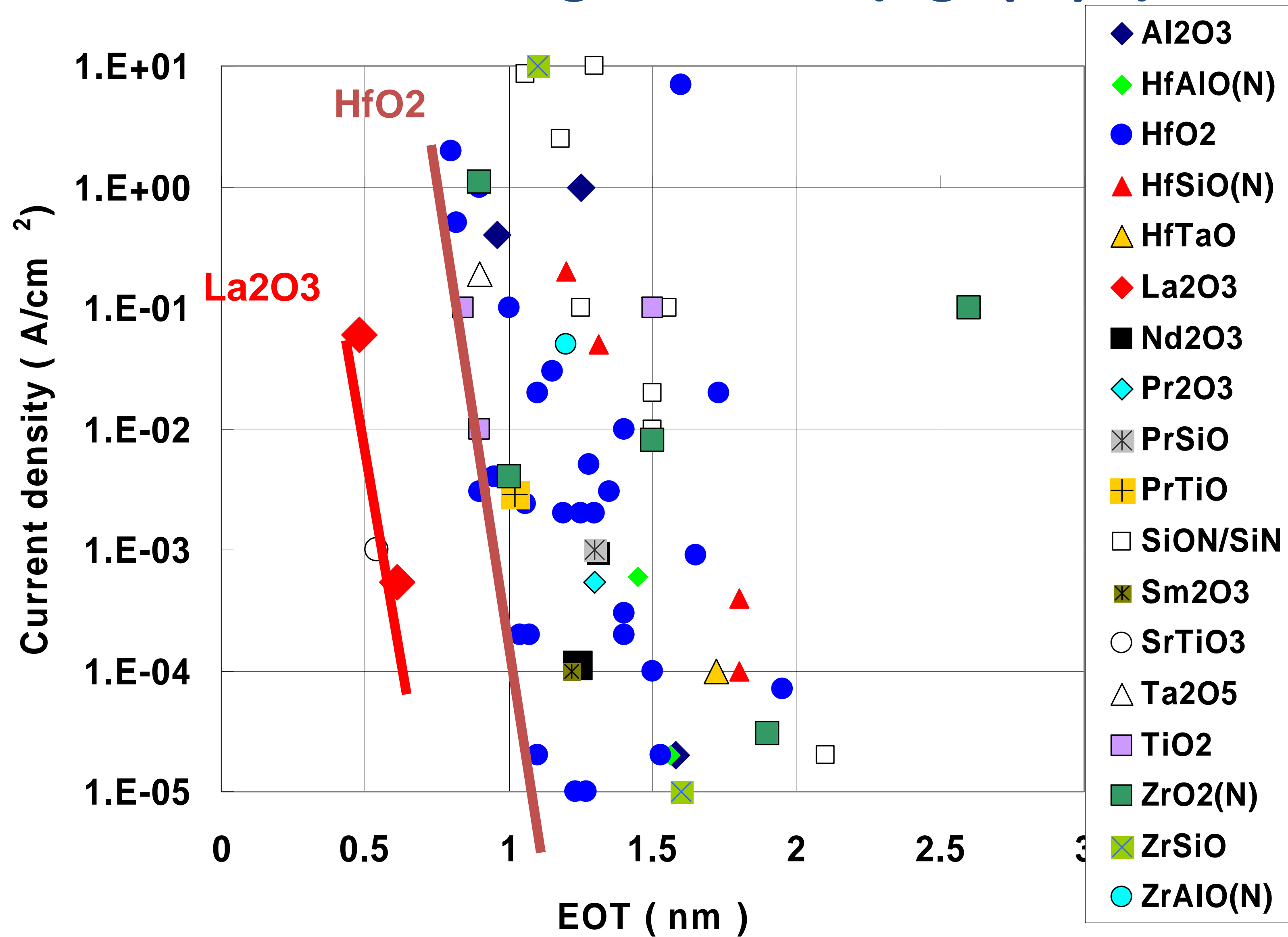




La_2O_3+Si+nO_2
→ La_2SiO_5, $La_{10}(SiO_4)_6O_3$
$La_{9.33}Si_6O_{26}$, $La_2Si_2O_7$

La_2O_3 can easily achieve direct contact of high-k/Si

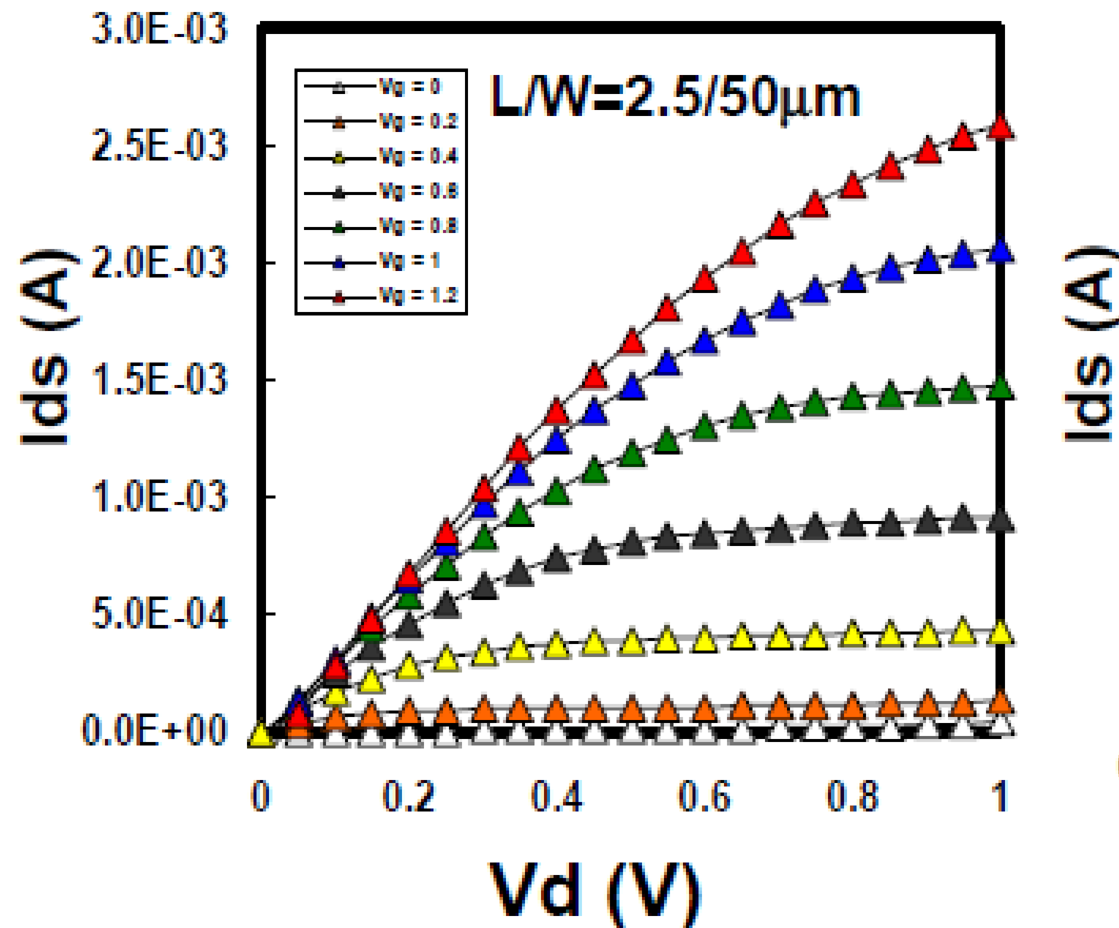
Gate Leakage vs EOT, (Vg=|1|V)



EOT = 0.48 nm

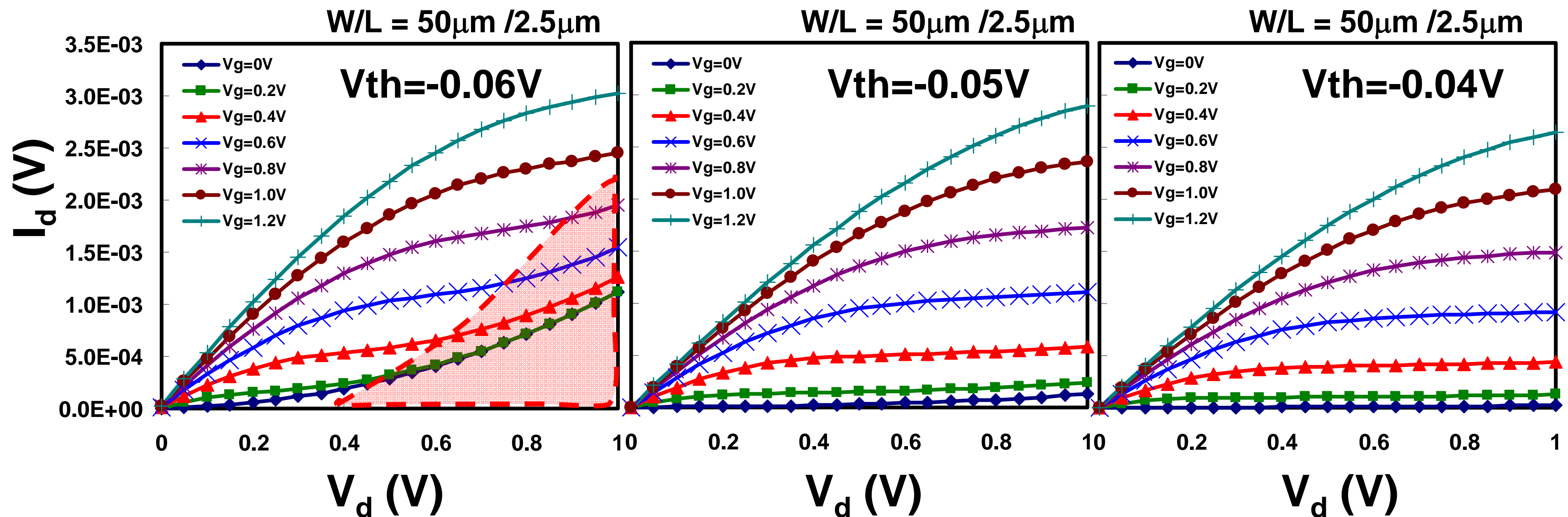
Our results

Transistor with La_2O_3 gate insulator



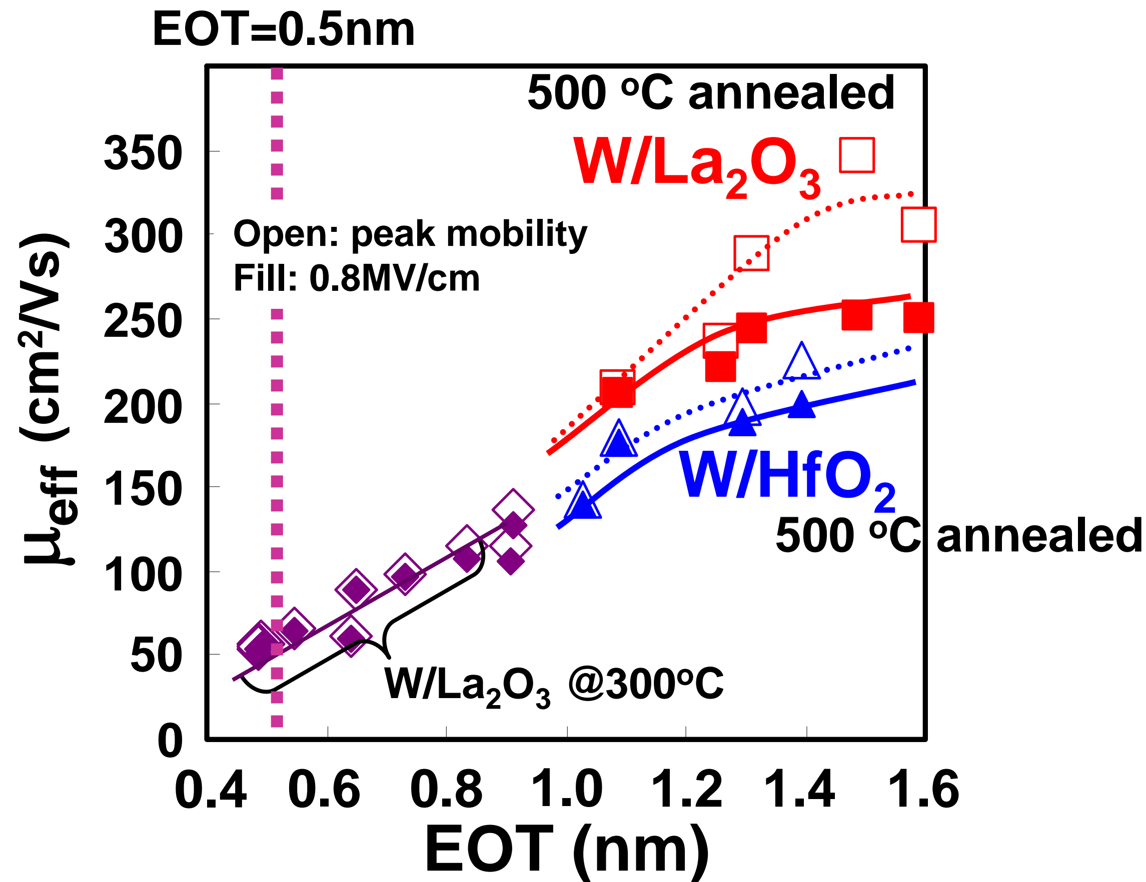
EOT=0.37nm

La2O3



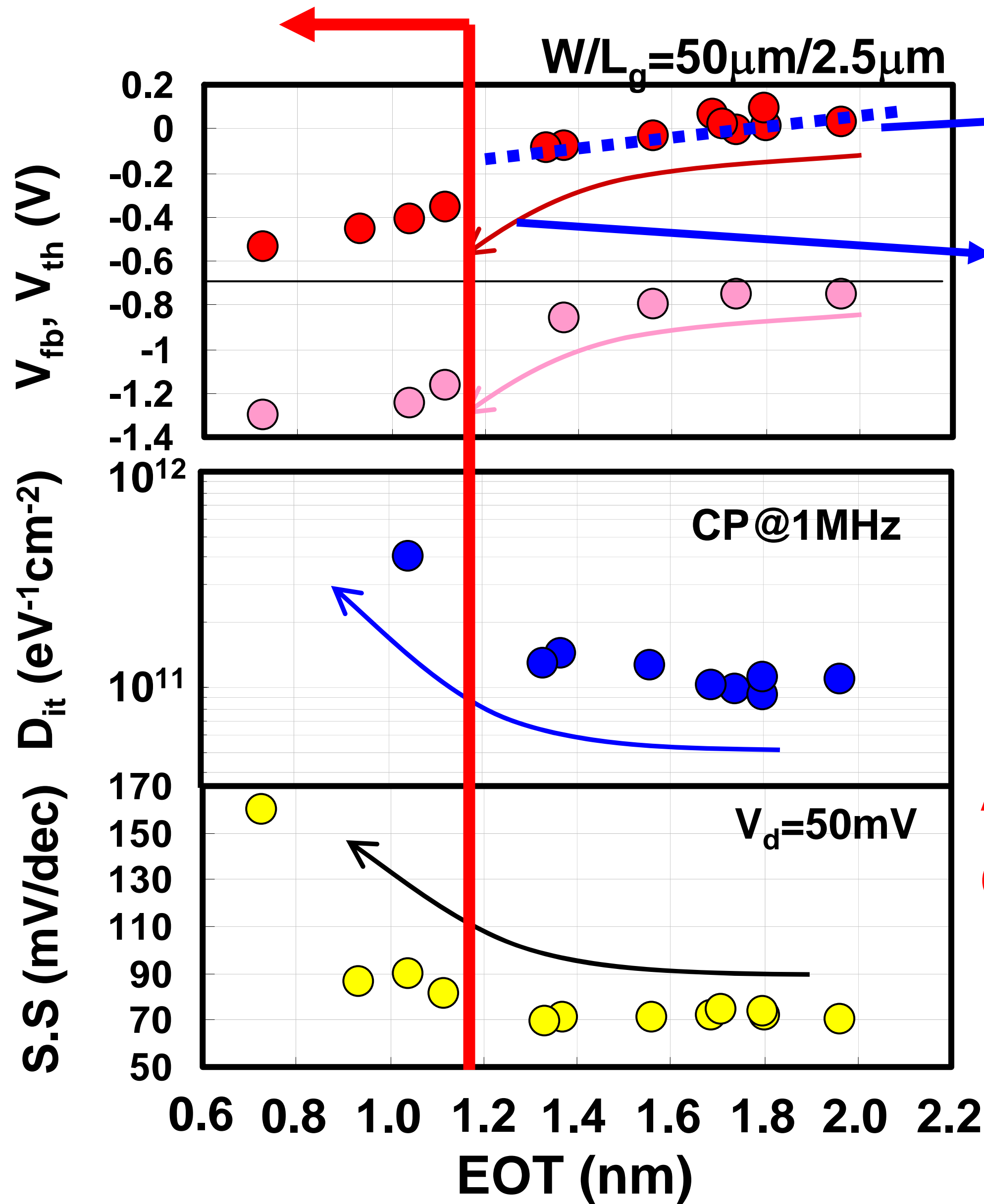
0.48 →0.37nm Increase of Id at 30%

μ_{eff} of W/La_2O_3 and W/HfO_2 nFET on EOT



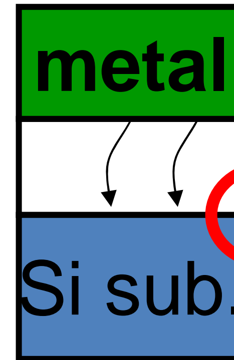
- W/La_2O_3 exhibits higher μ_{eff} than W/HfO_2
- μ_{eff} start degrades below EOT=1.4nm

FET characteristics of W/La_2O_3 on EOT



N_{fix}=7x10^{12} cm^{-2}

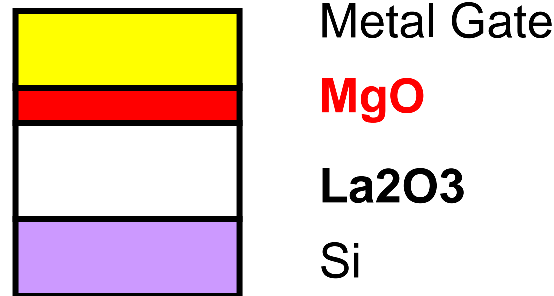
Aggressive N_{fix} generation at EOT<1.2nm

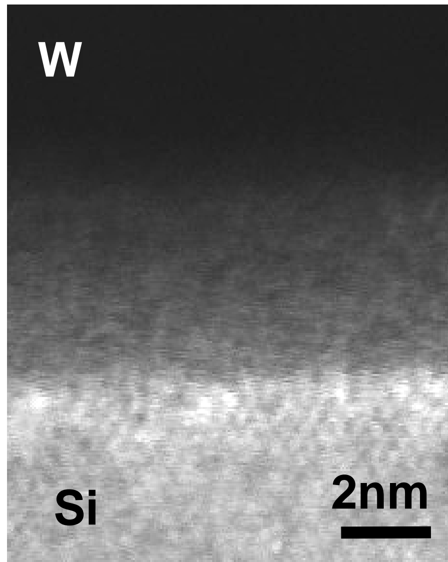


N_{fix} and D_{it}

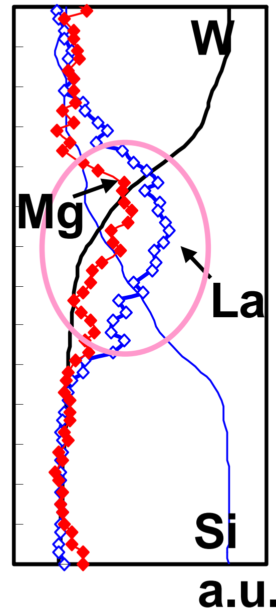
All characteristics start to degrade or shift below EOT=1.4nm

Gate Metal Induced Defects Compensation

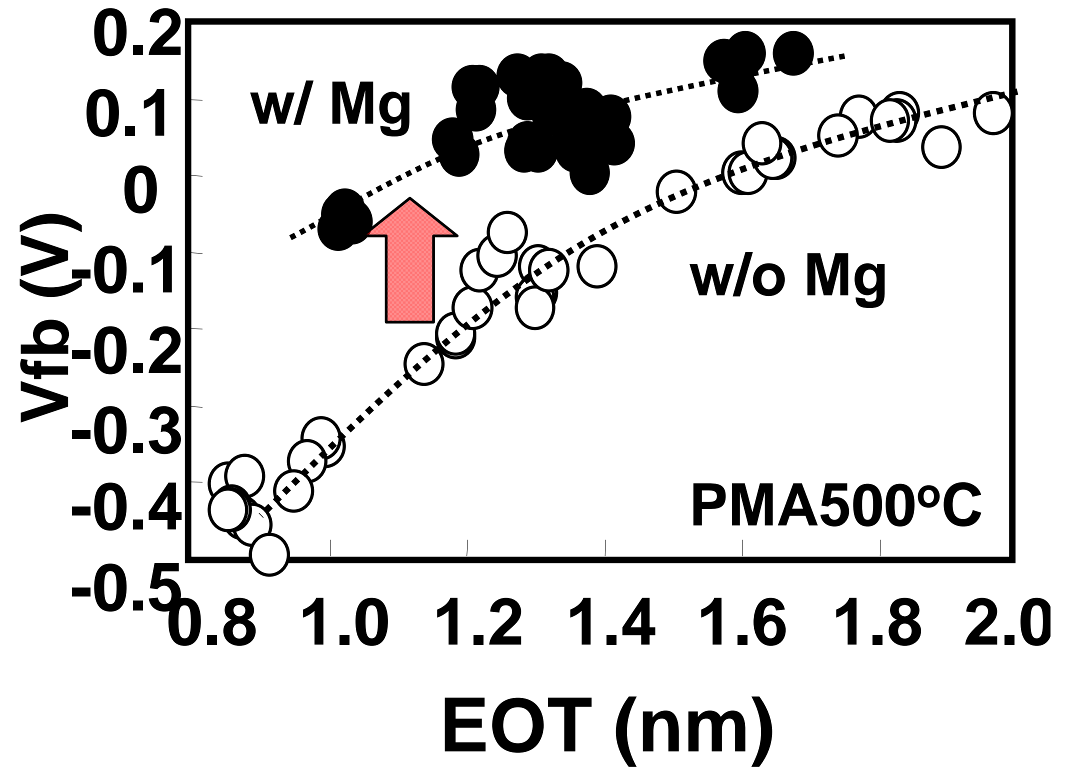




TEM

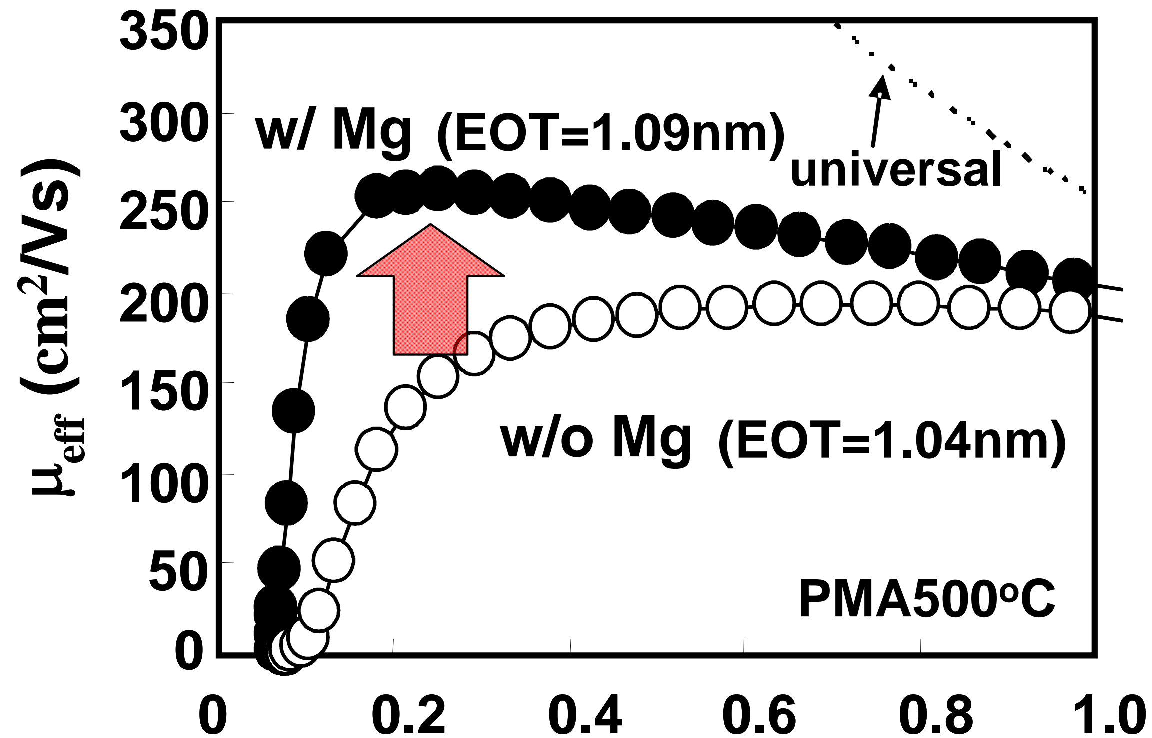


EDX



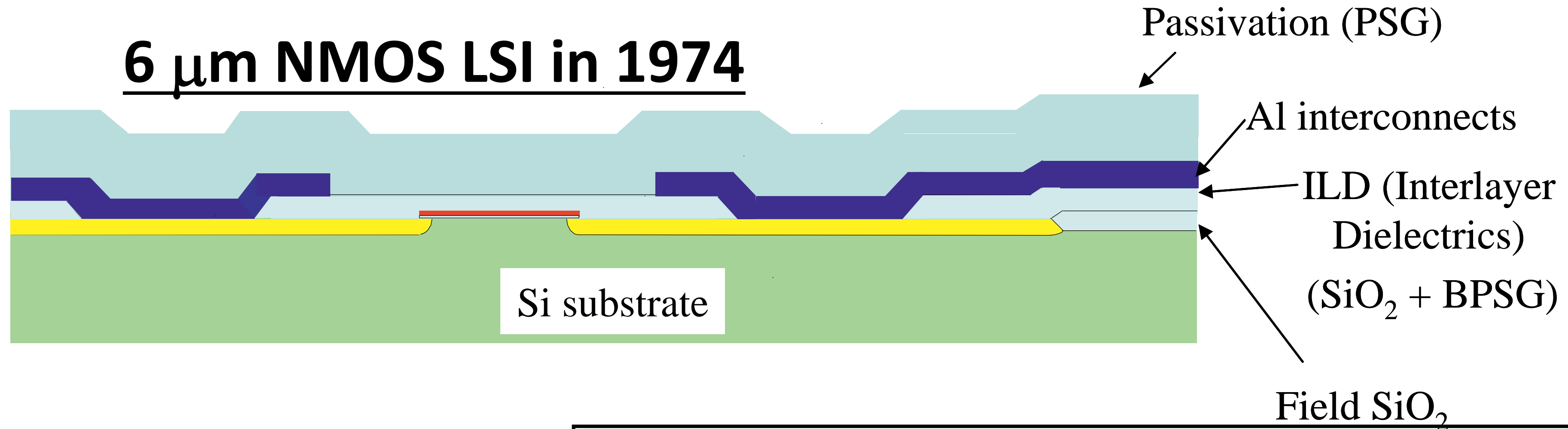
Suppression of aggressive shift in V_{fb}

Mobility Improvement with Mg Incorporation

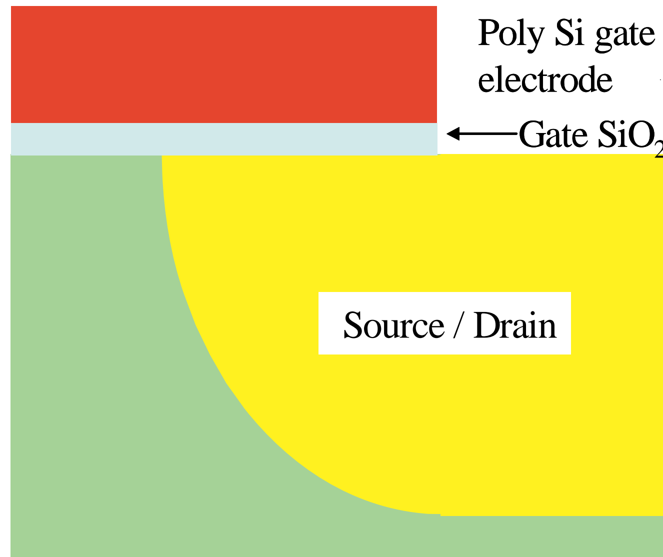


Recovery of μ_{eff} mainly at low E_{eff}

6 μm NMOS LSI in 1974



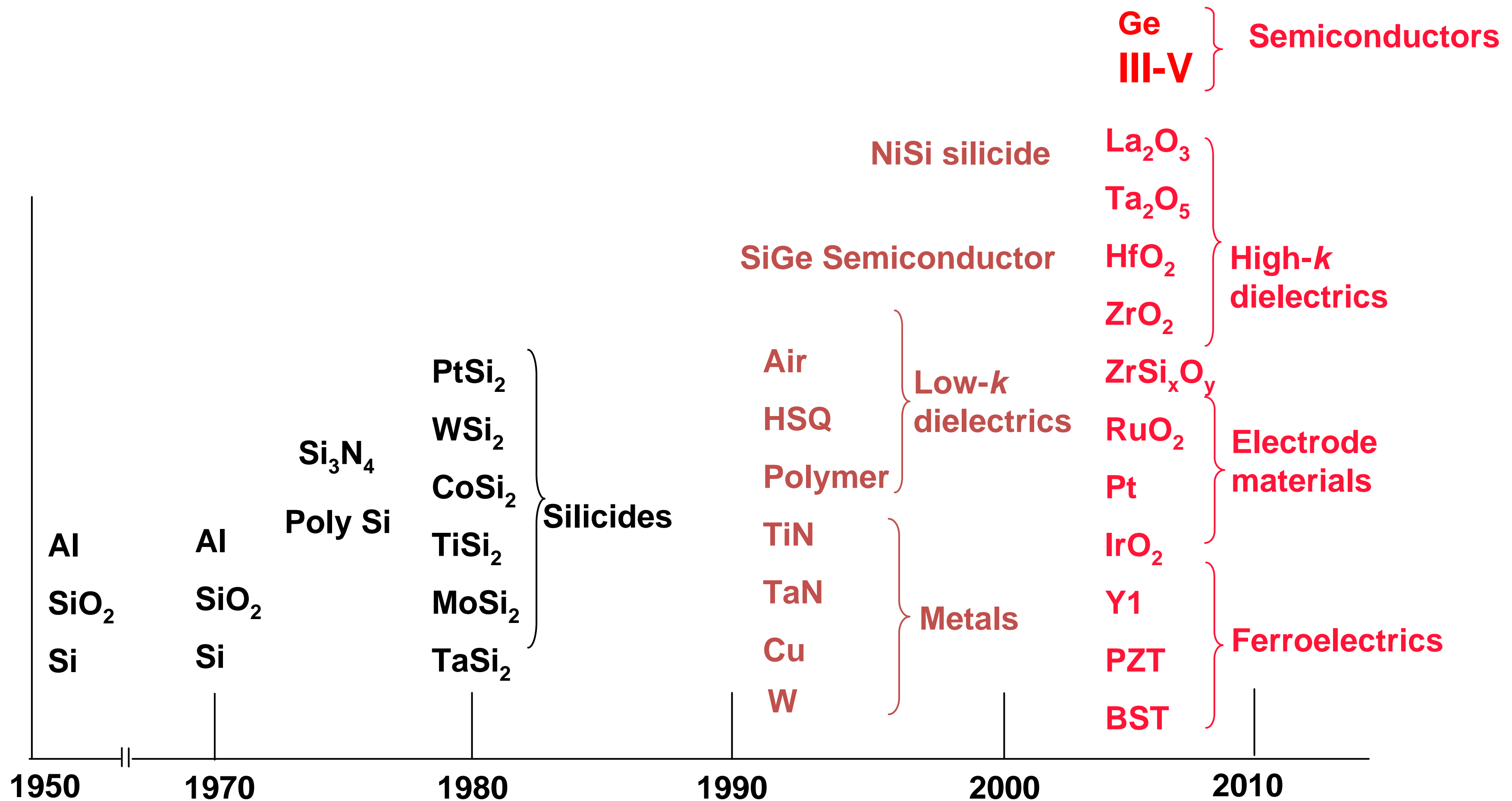
magnification



Layers	Materials	Atoms
1. Si substrate	1. Si	**1. Si**
2. Field oxide	2. SiO_2	**2. O**
3. Gate oxide	3. BPSG	**3. P**
4. Poly Si	4. Al	**4. B**
5. S/D	5. PSG	**5. Al**
6. Interlayer		**(H, N, Cl)**
7. Aluminum		
8. Passivation		

Just examples!
Many other candidates

New materials



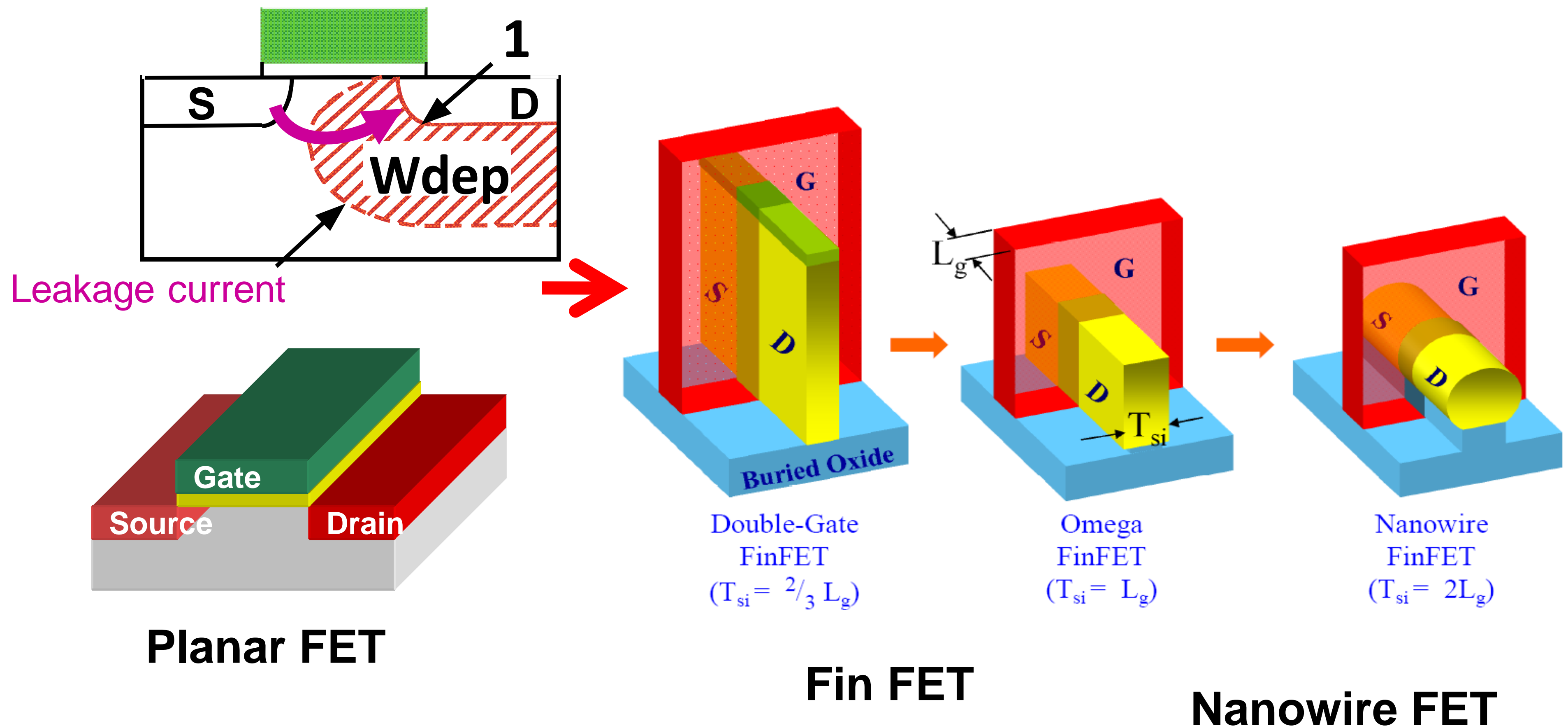
Y. Nishi, Si Nano Workshop, 2006,

(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)

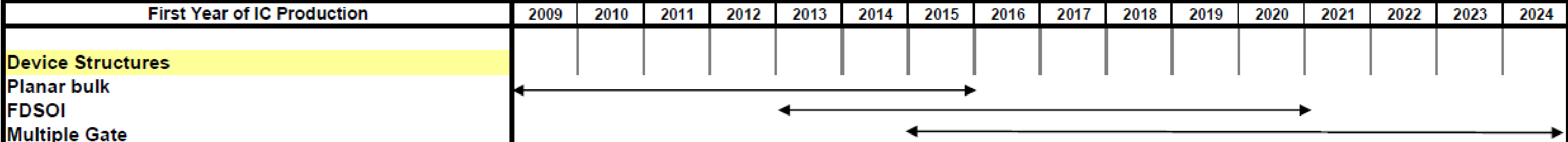
Si nanowire FET

Because of off-leakage control,

Planar → Fin → Nanowire



Nanowire FET



2015

22 or 16nm node

Multiple Gate (Fin) FET

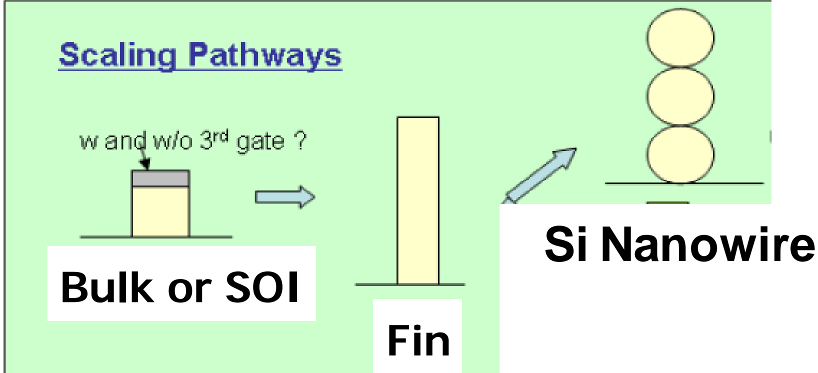
2020

11 or 8nm node

Nanowire FET

ITRS 2009

Bulk → Fin → Nanowire

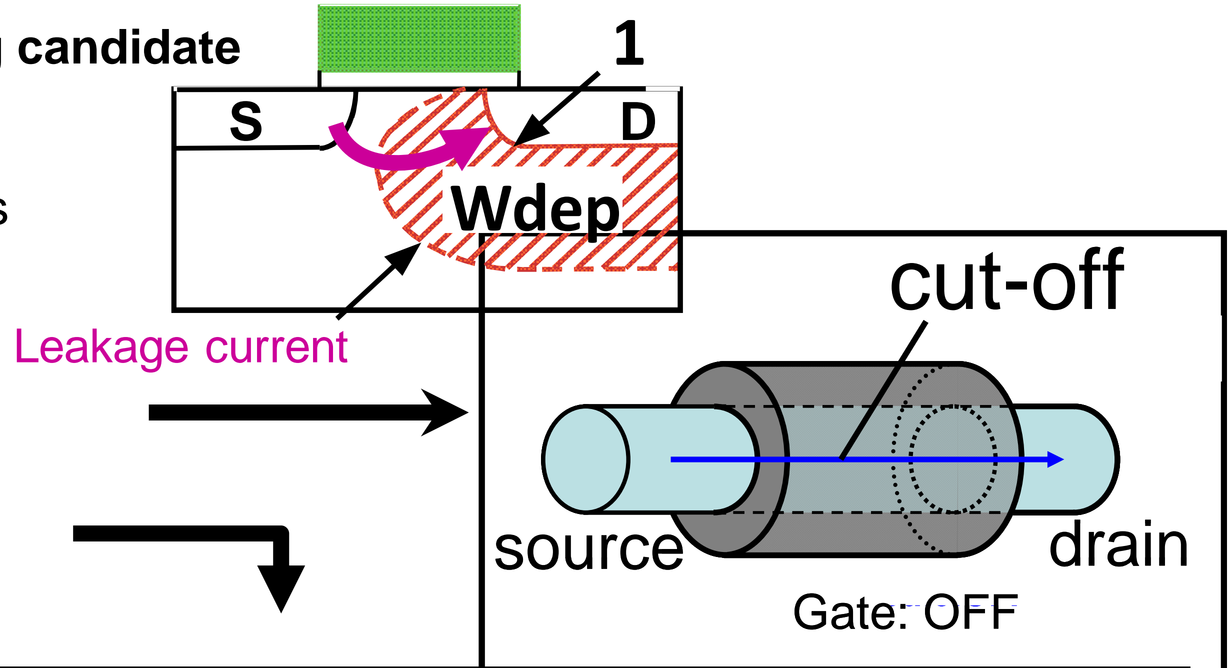


Si nanowire FET as a strong candidate

1. Compatibility with
   current CMOS process

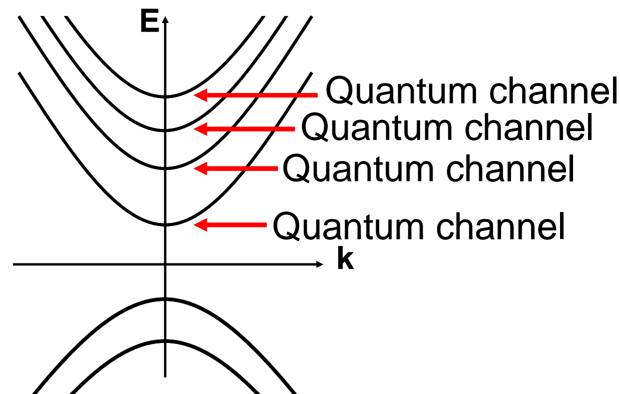
2. Good controllability of I_{OFF}

3. High drive current

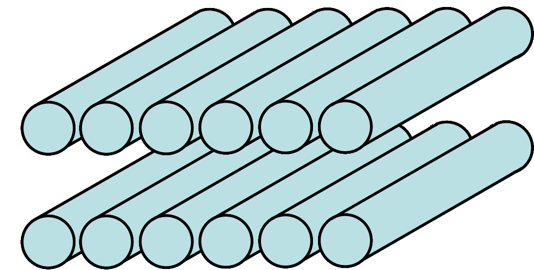


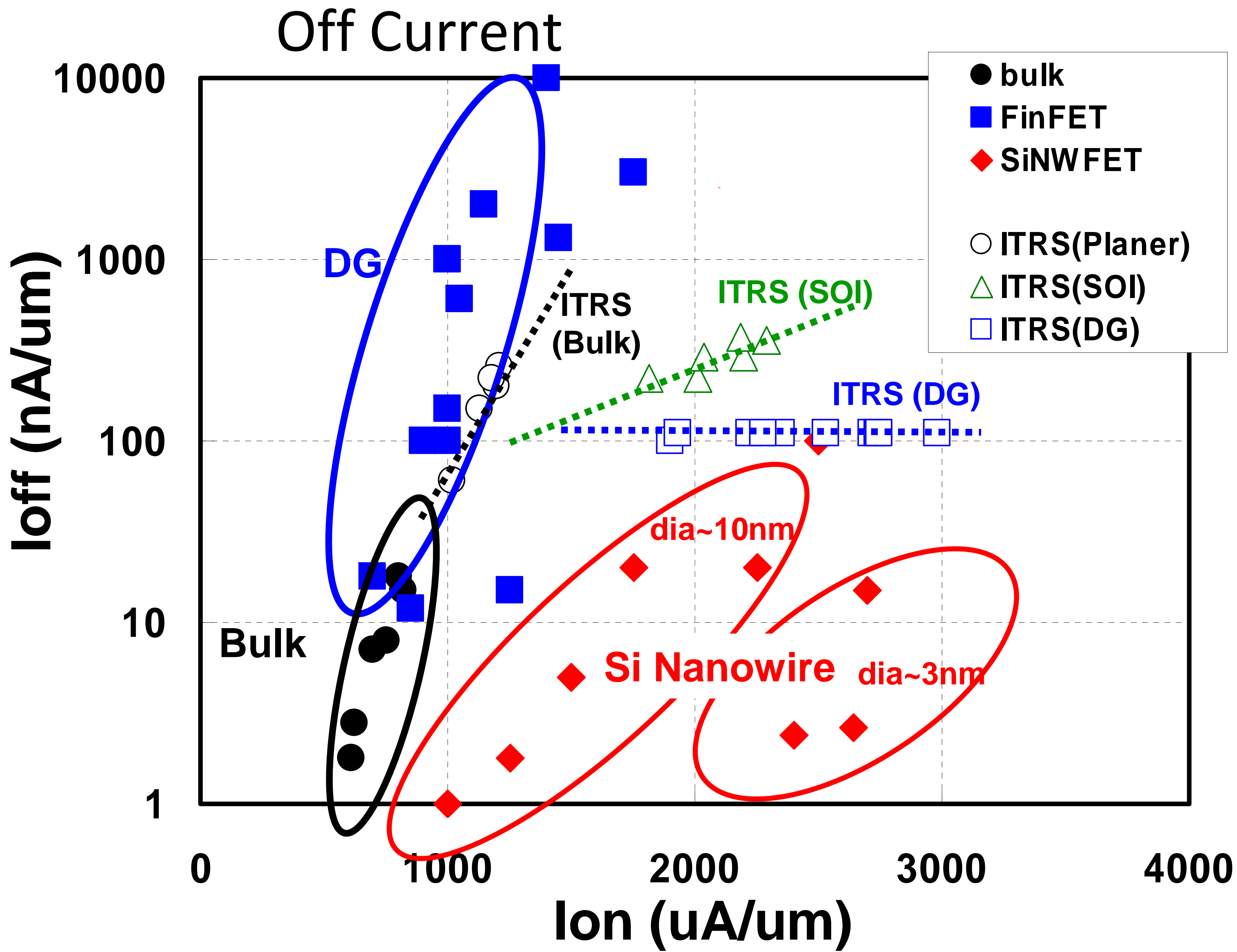
1D ballistic conduction

Multi quantum Channel



High integration of wires

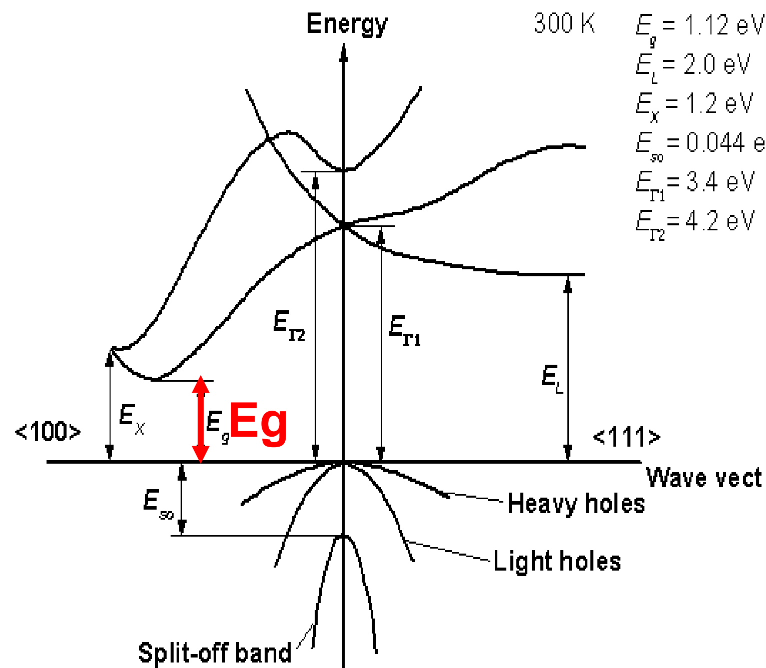




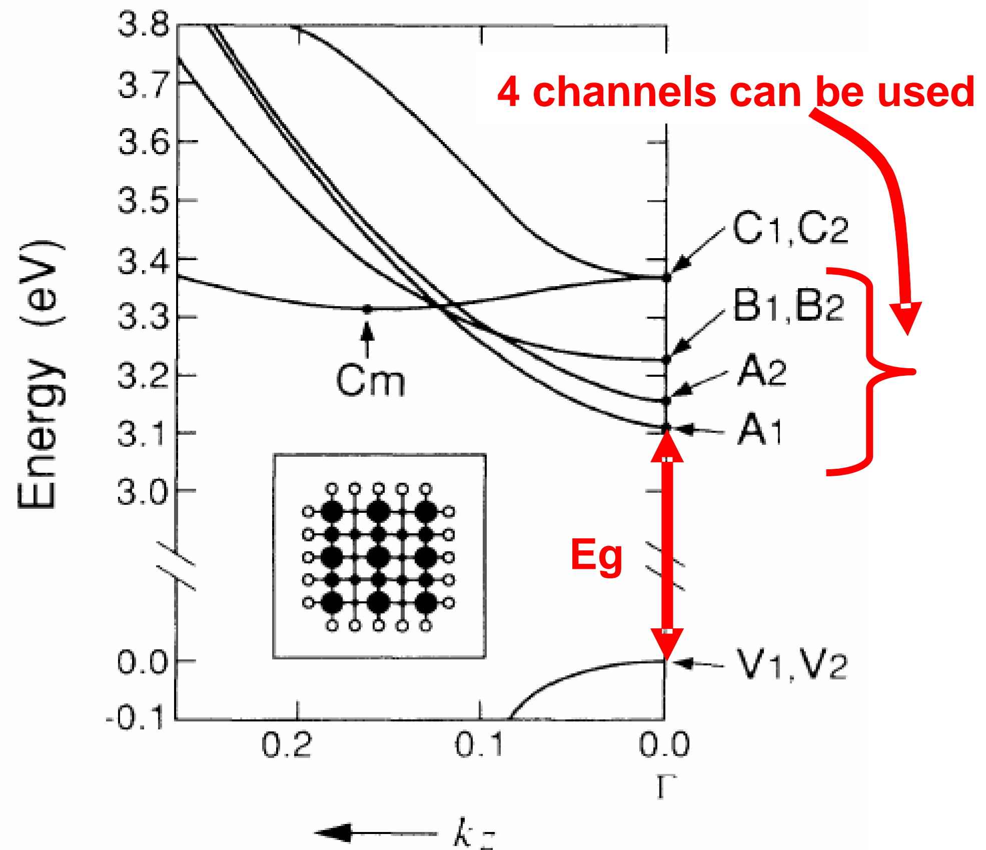
Off Current
Ioff (nA/um)
Ion (uA/um)
10000
1000
100
10
1
0
1000
2000
3000
4000
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
Bulk
dia~10nm
Si Nanowire
dia~3nm

Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



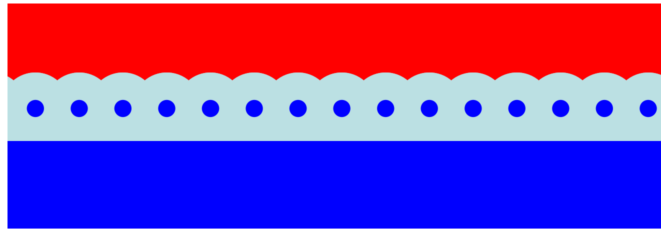
Energy band of Bulk Si



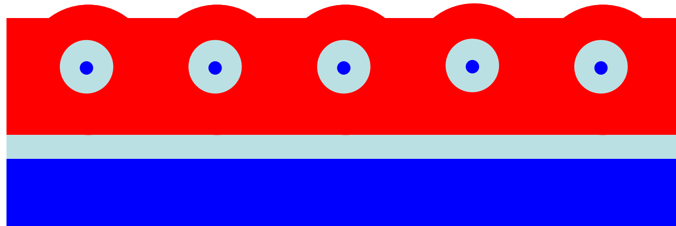
Energy band of 3 x 3 Si wire

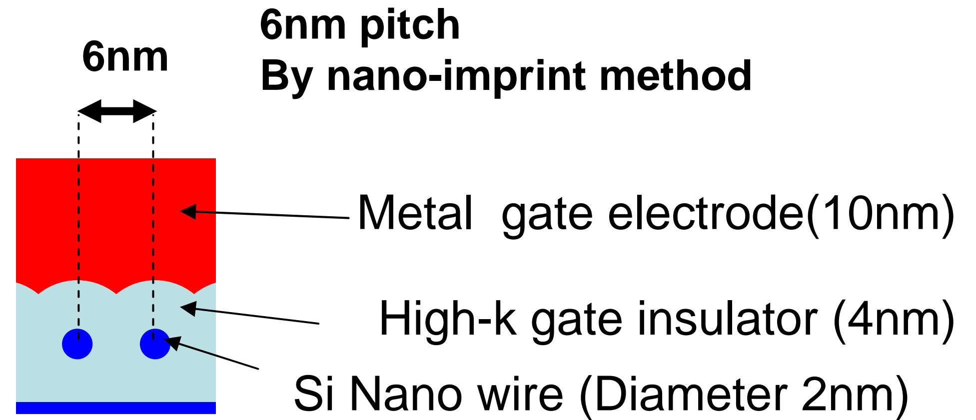
Maximum number of wires per 1 µm

Front gate type MOS 165 wires /µm

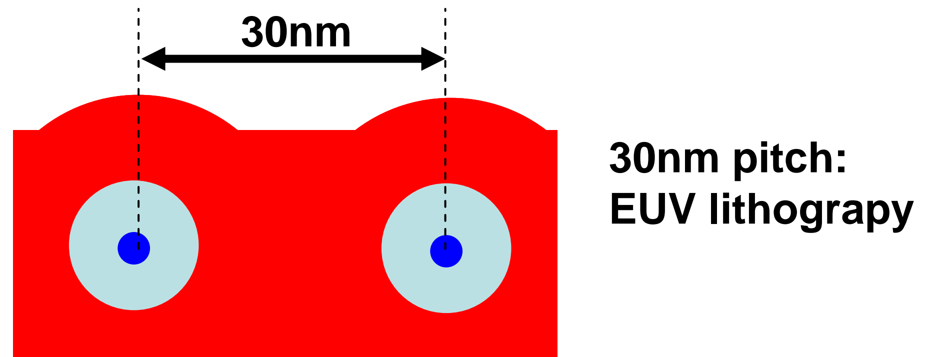


Surrounded gate type MOS 33 wires/µm

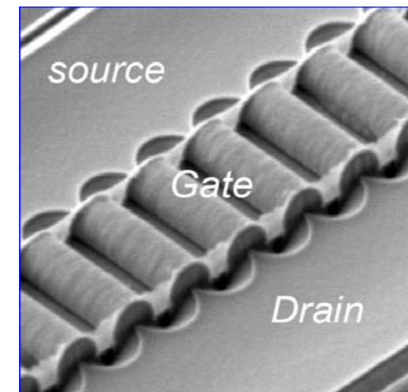




6nm pitch
By nano-imprint method

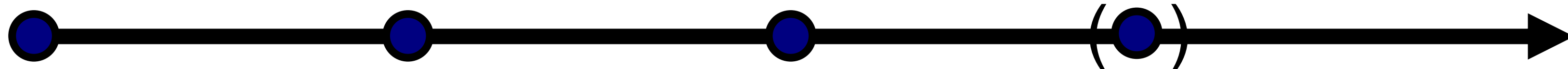


30nm pitch:
EUV lithograpy



Surrounded gate MOS

Device fabrication

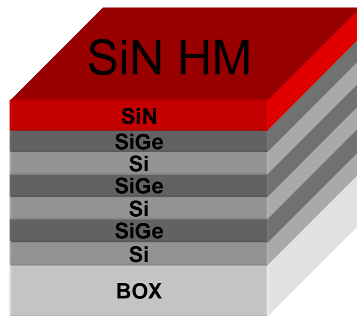


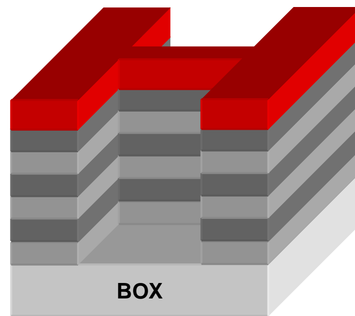
$Si/Si_{0.8}Ge_{0.2}$ superlattice epitaxy on SOI

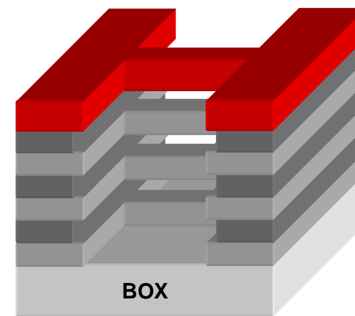
Anisotropic etching of these layers

Isotropic etching of SiGe

(The NW diameter is controllable down to 5 nm by self limited oxidation.)







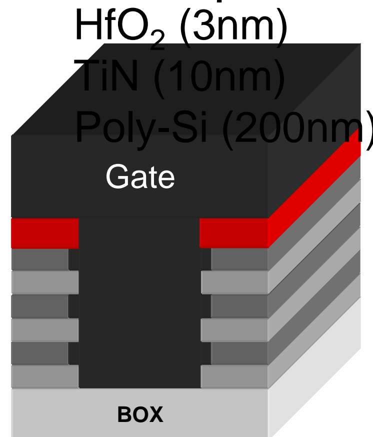
Gate depositions

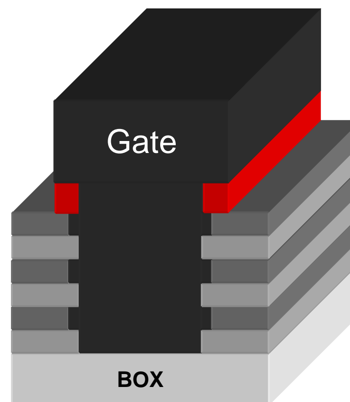
HfO_2 (3nm)
TiN (10nm)
Poly-Si (200nm)

Gate etching

S/D implantation
Spacer formation
Activation anneal
Salicidation

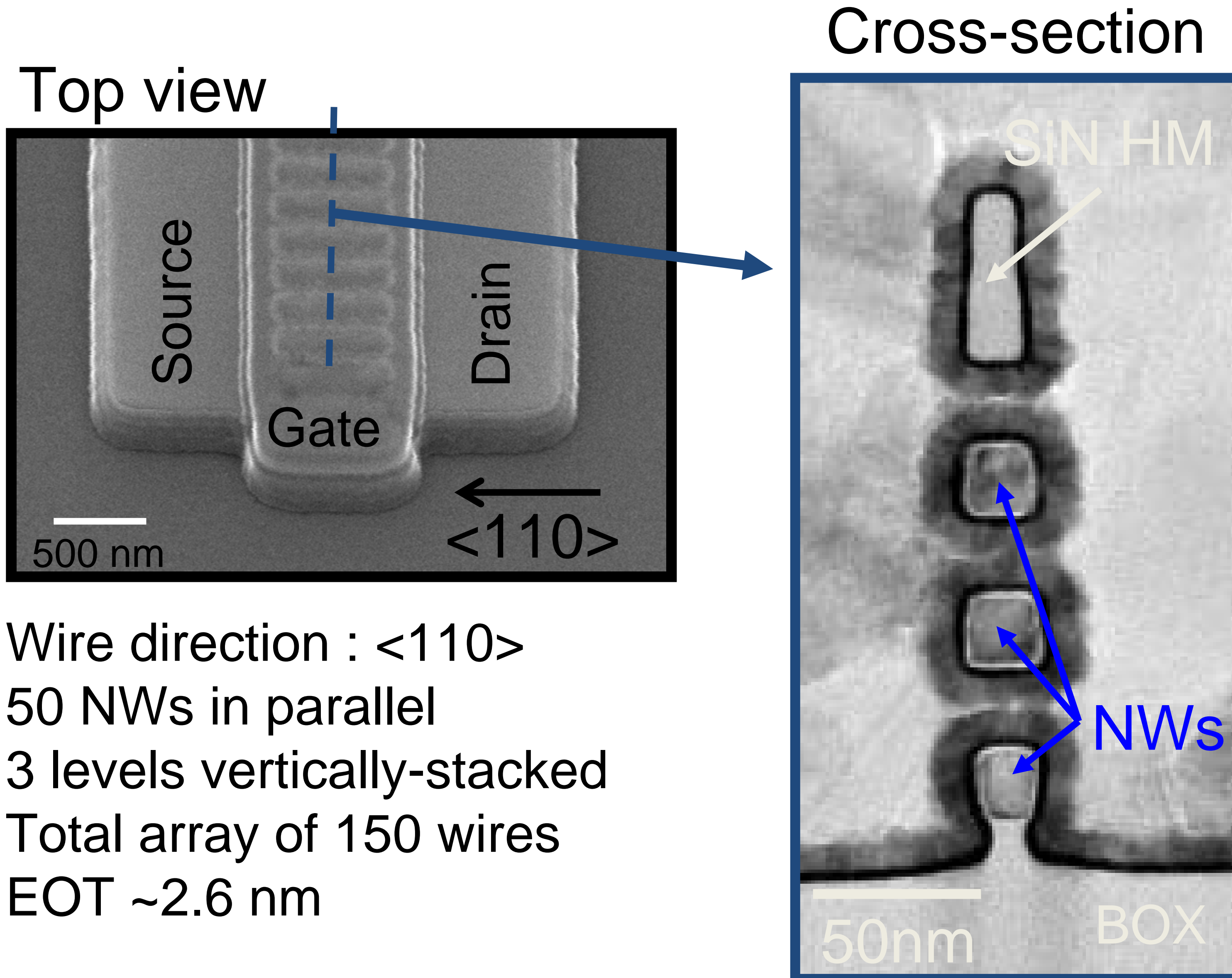
Standard Back-End of-Line Process





Process Details :
C. Dupre *et al.*,
IEDM Tech. Dig., p.749, 2008

3D-stacked Si NWs with Hi-*k*/MG

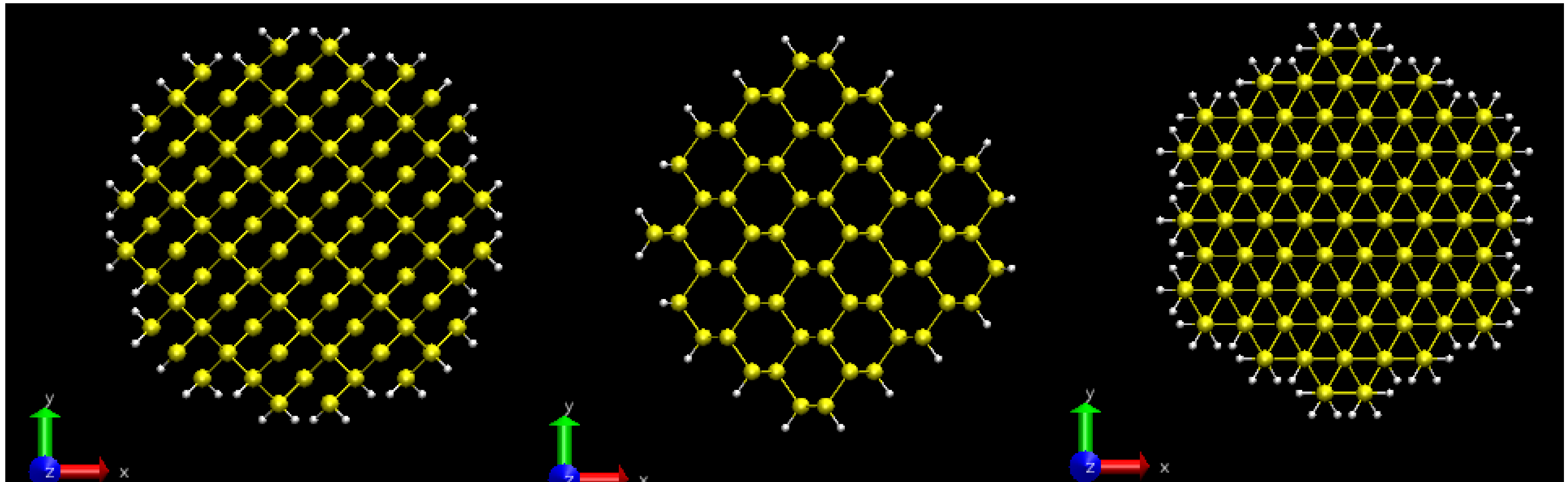


Wire direction : <110>
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT ~2.6 nm

SiNW Band structure calculation

Cross section of Si NW

First principal calculation,

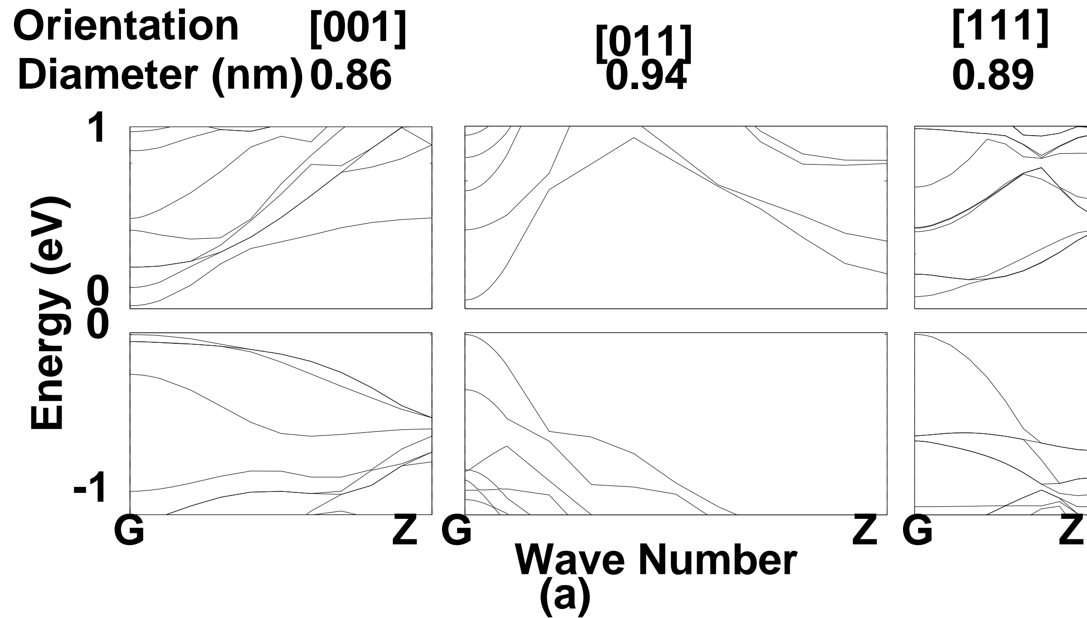


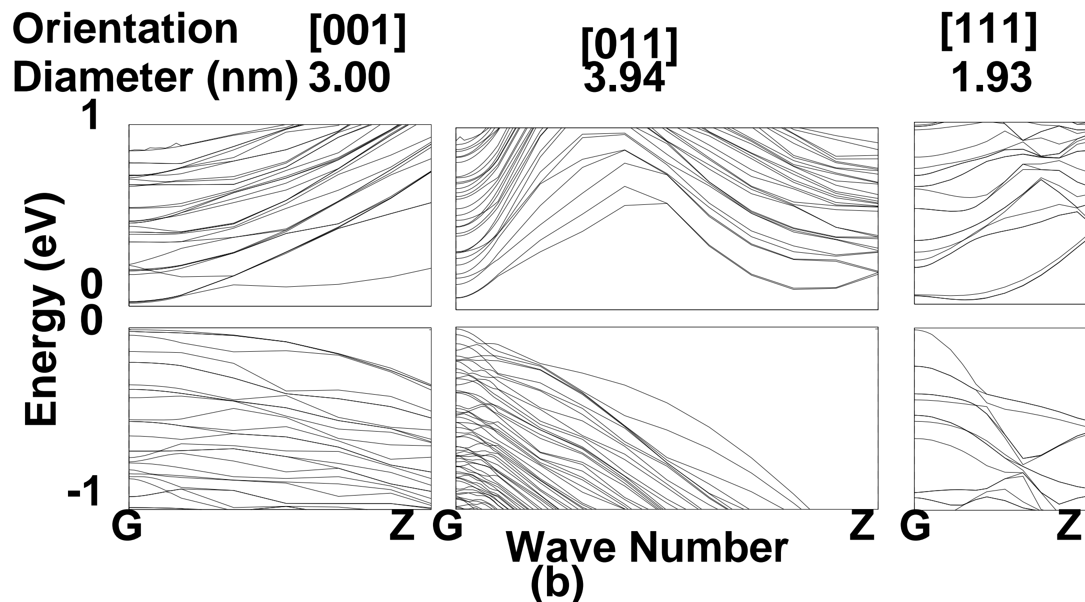
D=1.96nm [001]

D=1.94nm [011]

D=1.93nm [111]

Si nanowire FET with 1D Transport



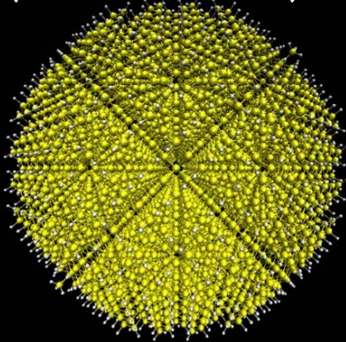


Small mass with [011]

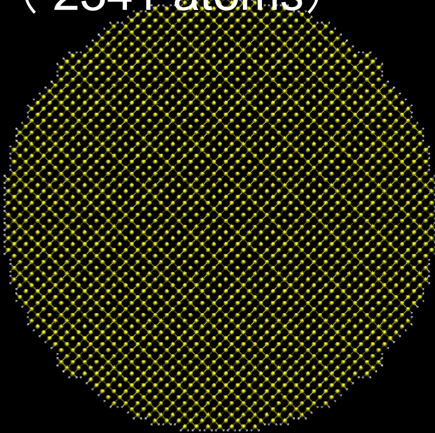
Large number of quantum channels with [001]

Atomic models of a Si quantum dot and Si nanowires

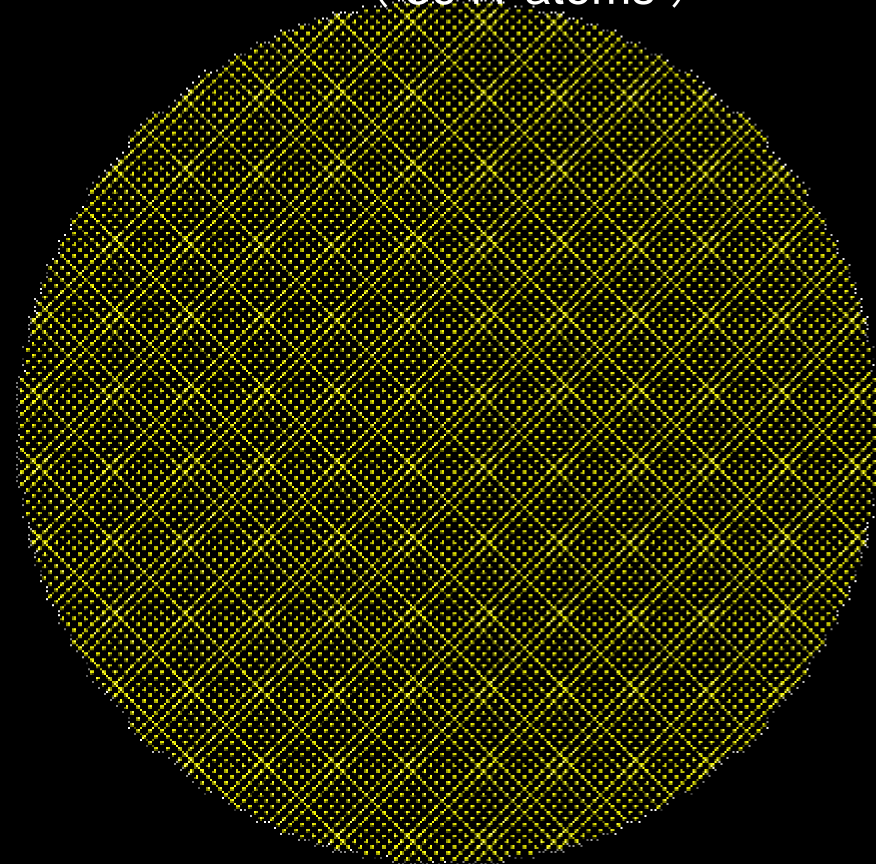
6.6 nm diameter SiQD
(8651 atoms)



10 nm diameter Si(100)NW
(2341 atoms)



20 nm diameter Si(100)NW
(8941 atoms)



RSDFT – suitable for parallel first-principles calculation -

- ✓Real-Space Finite-Difference
- ✓Sparse Matrix
- ✓FFT free (FFT is inevitable in the conventional plane-wave code)
- ✓MPI (Message Passing Interface) library

Higher-order finite difference pseudopotential method
J. R. Chelikowsky et al., Phys. Rev. B, (1994)

3D grid is divided by several regions for parallel computation.

Kohn-Sham eq. (finite-difference)

$$\left(-\frac{1}{2}\nabla^2 + v_s[\rho](\mathbf{r}) + \hat{v}_{nloc}^{PP}(\mathbf{r})\right)\phi_n(\mathbf{r}) = \varepsilon_n \phi_n(\mathbf{r})$$

Higher-order finite difference

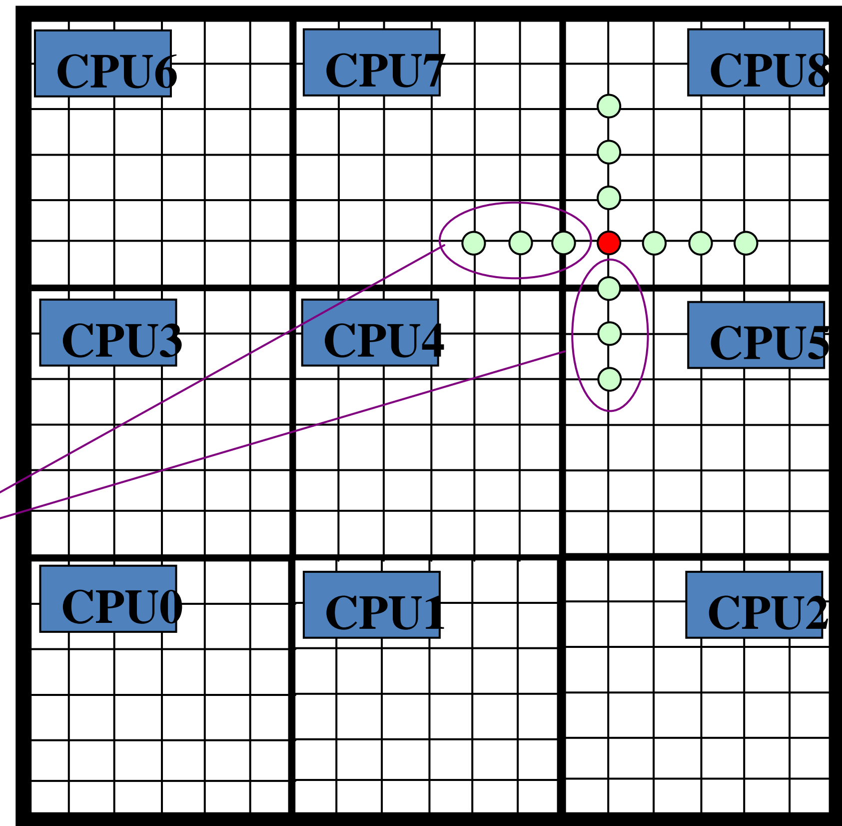
$$\frac{\partial^2}{\partial x^2}\psi_n(x,y,z) \approx \sum_{m=-6}^{6} C_m \psi_n(x + m\Delta x, y, z)$$

MPI_ISEND, MPI_IRECV

Integration

$$\int \psi_m(\mathbf{r})\psi_n(\mathbf{r})d\mathbf{r} \approx \sum_{i=1}^{Mesh} \psi_m(\mathbf{r}_i)\psi_n(\mathbf{r}_i)\Delta x \Delta y \Delta z$$

MPI_ALLREDUCE



Massively Parallel Computing

with our recently developed code "RSDFT"

Iwata et al, J. Comp. Phys., to be published

Real-Space Density-Functional Theory code (RSDFT)

Based on the finite-difference pseudopotential method (J. R. Chelikowsky et al., PRB1994)

Highly tuned for massively parallel computers

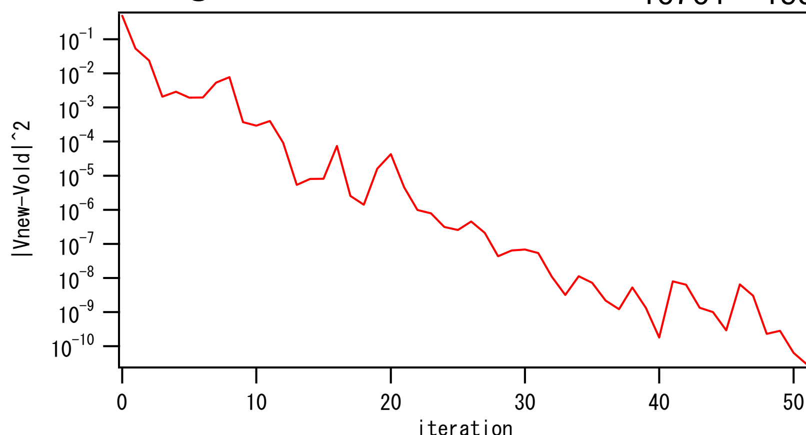
Computations are done on a massively-parallel cluster **PACS-CS** at University of Tsukuba.

(Theoretical Peak Performance = 5.6GFLOPS/node)

e.g.) The system over 10,000 atoms → $Si_{10701}H_{1996}$
(7.6 nm diameter Si dot)

Convergence behavior for $Si_{10701}H_{1996}$

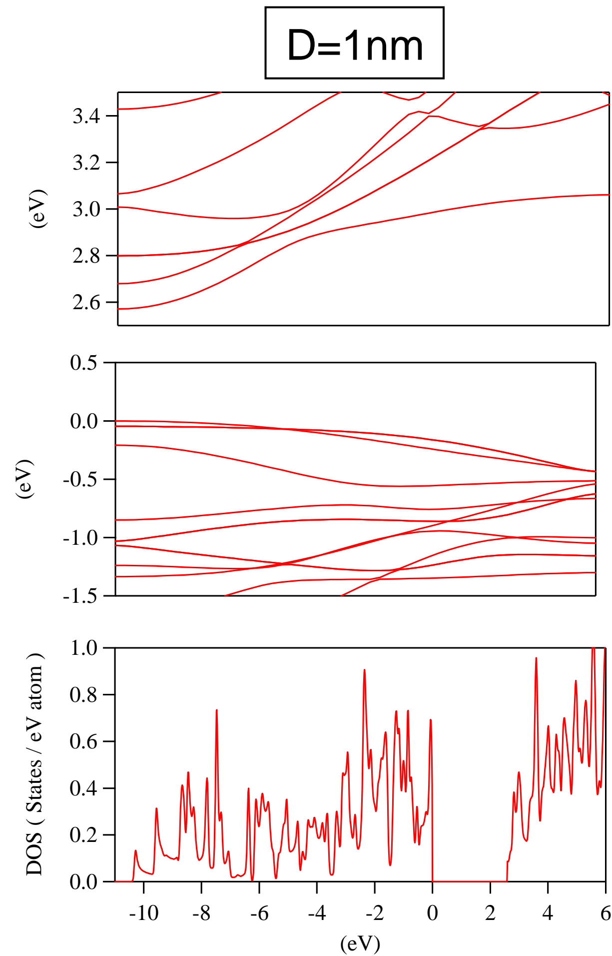
Grid points = 3,402,059
Bands = 22,432

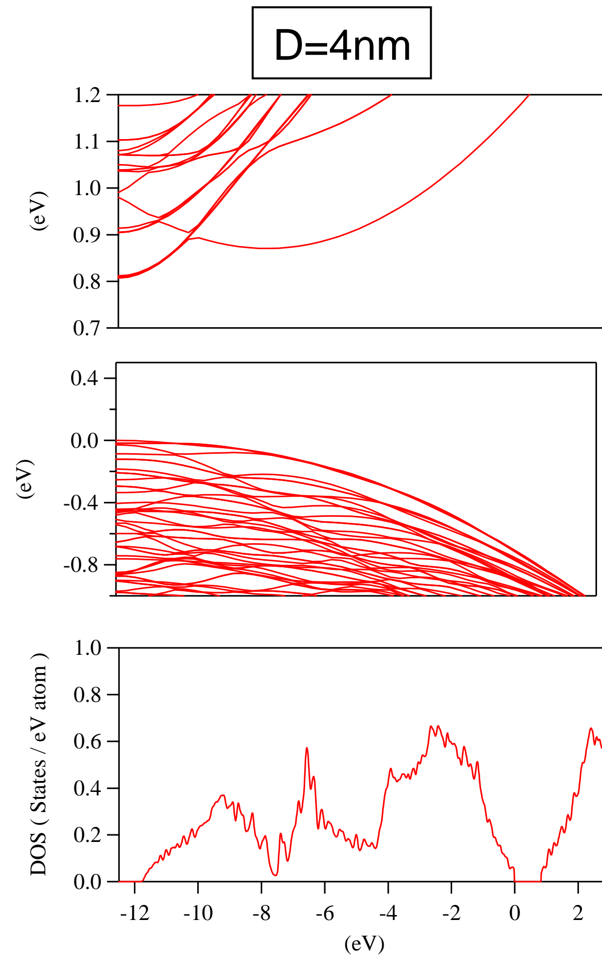


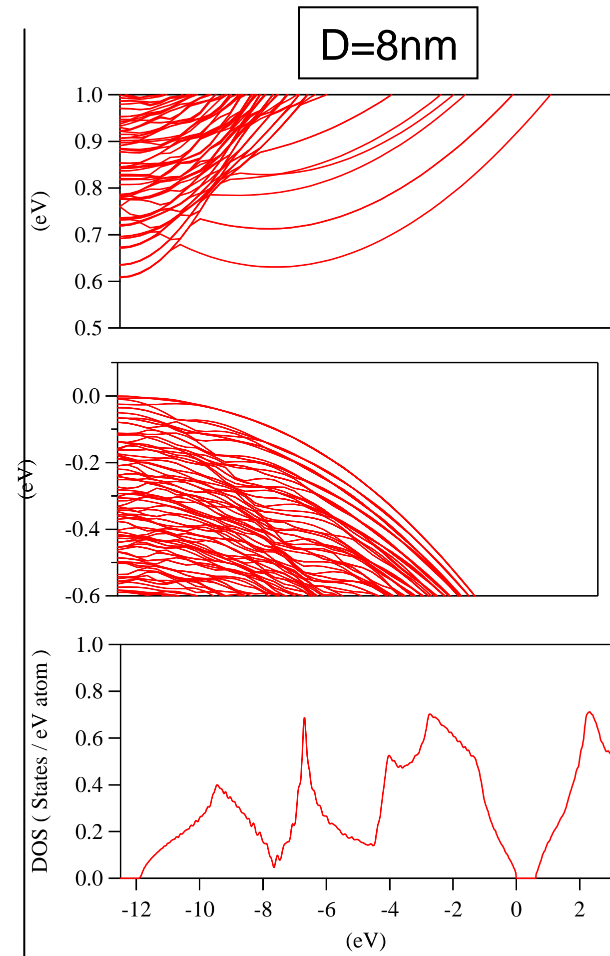
Computational Time (with 1024 nodes of PACS-CS

6781 sec. × 60 iteration step = 113 hour

Band Structure and DOS of Si(100)NWs (D=1nm, 4nm, and 8nm)







D=1 nm
Si21H20 (41 atoms)
KS band gap=2.60eV

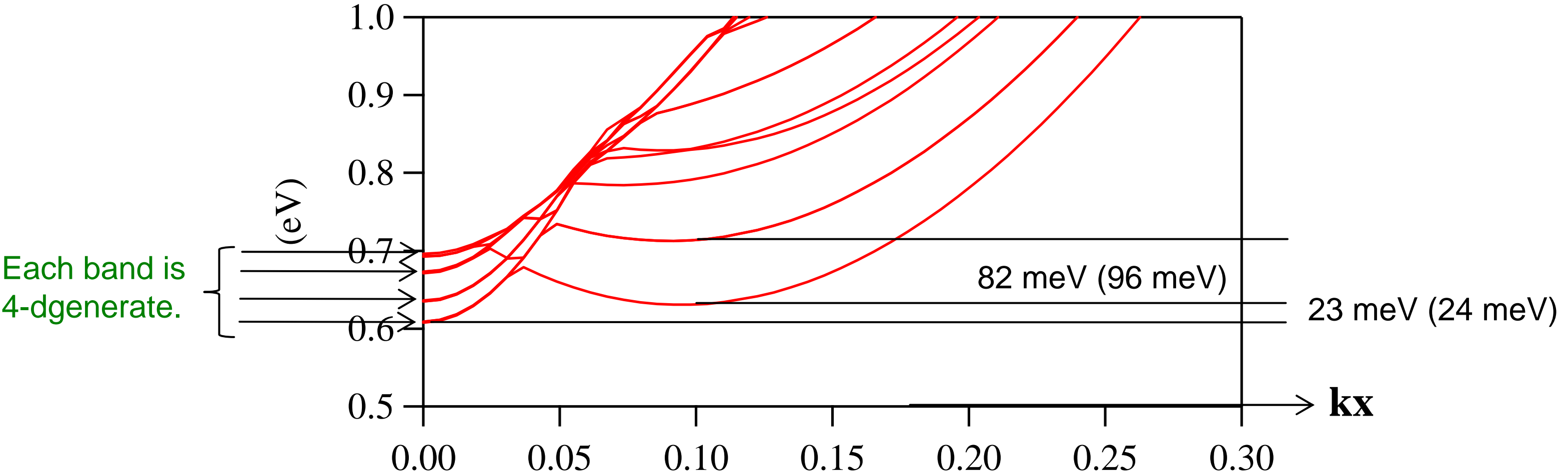
D = 4 nm
Si341H84 (425 atoms)
KS band gap = 0.81eV

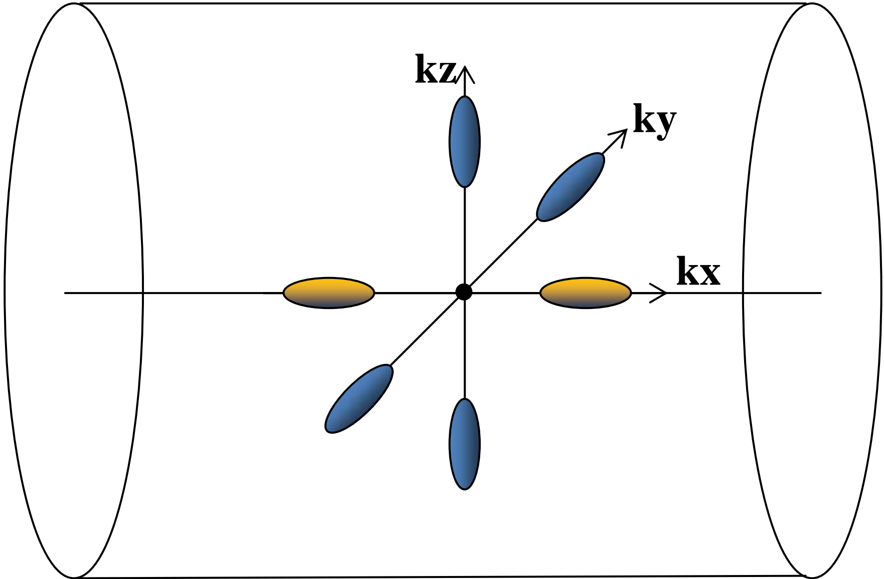
D=8 nm
Si1361H164 (1525 atoms)
KS band gap=0.61eV

KS band gap of bulk (LDA) = 0.53eV

Band structure of 8-nm-diameter Si nanowire near the CBM

- KS band gap = 0.608 eV (@Γ)



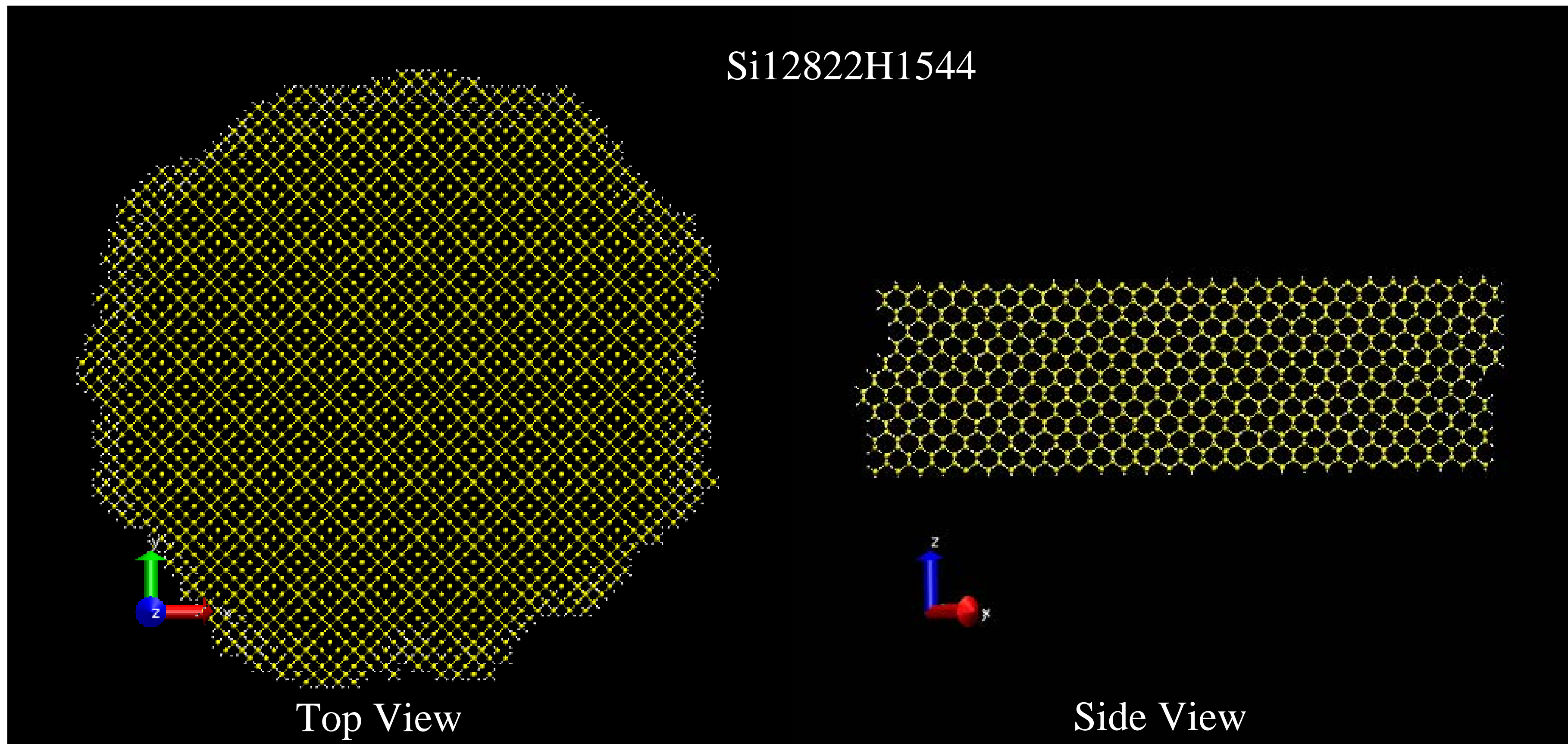


Effective mass equation

$$\left[-\frac{\hbar^2}{2m_t^*}\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}\right)-\frac{\hbar^2}{2m_l^*}\frac{\partial^2}{\partial z^2}\right]\Phi(\mathbf{r})=(\varepsilon-\varepsilon_{CBM})\Phi(\mathbf{r})$$

The band structure can be understood that electrons near the CBM in the bulk Si are Confined within a cylindrical geometry.

Si nano wire with surface roughness

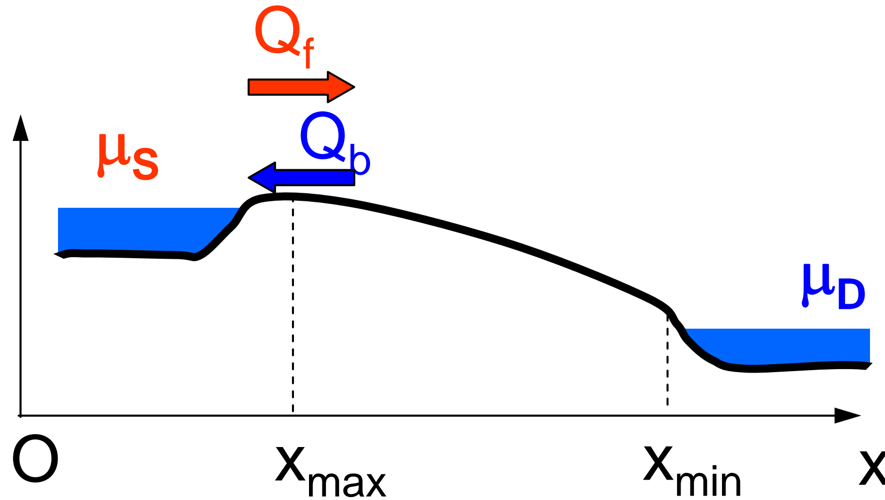


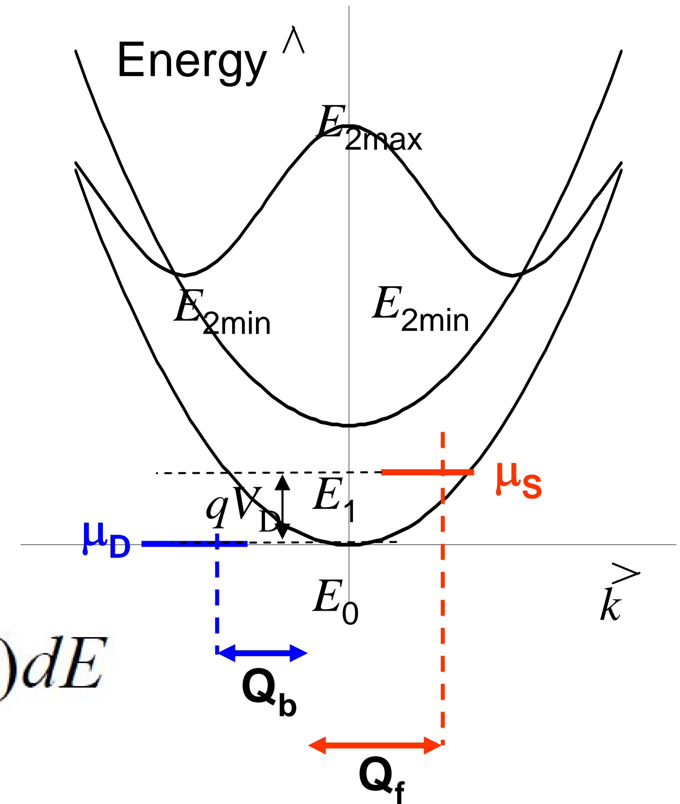
Si12822H1544（14,366 atoms）

- 10nm diameter、3.3nm height、(100)
- Grid spacing : 0.45Å (~14Ry)
- # of grid points : 4,718,592
- # of bands : 29,024
- Memory : 1,022GB～2,044GB

SiNW Band compact model

Landauer Formalism for Ballistic FET



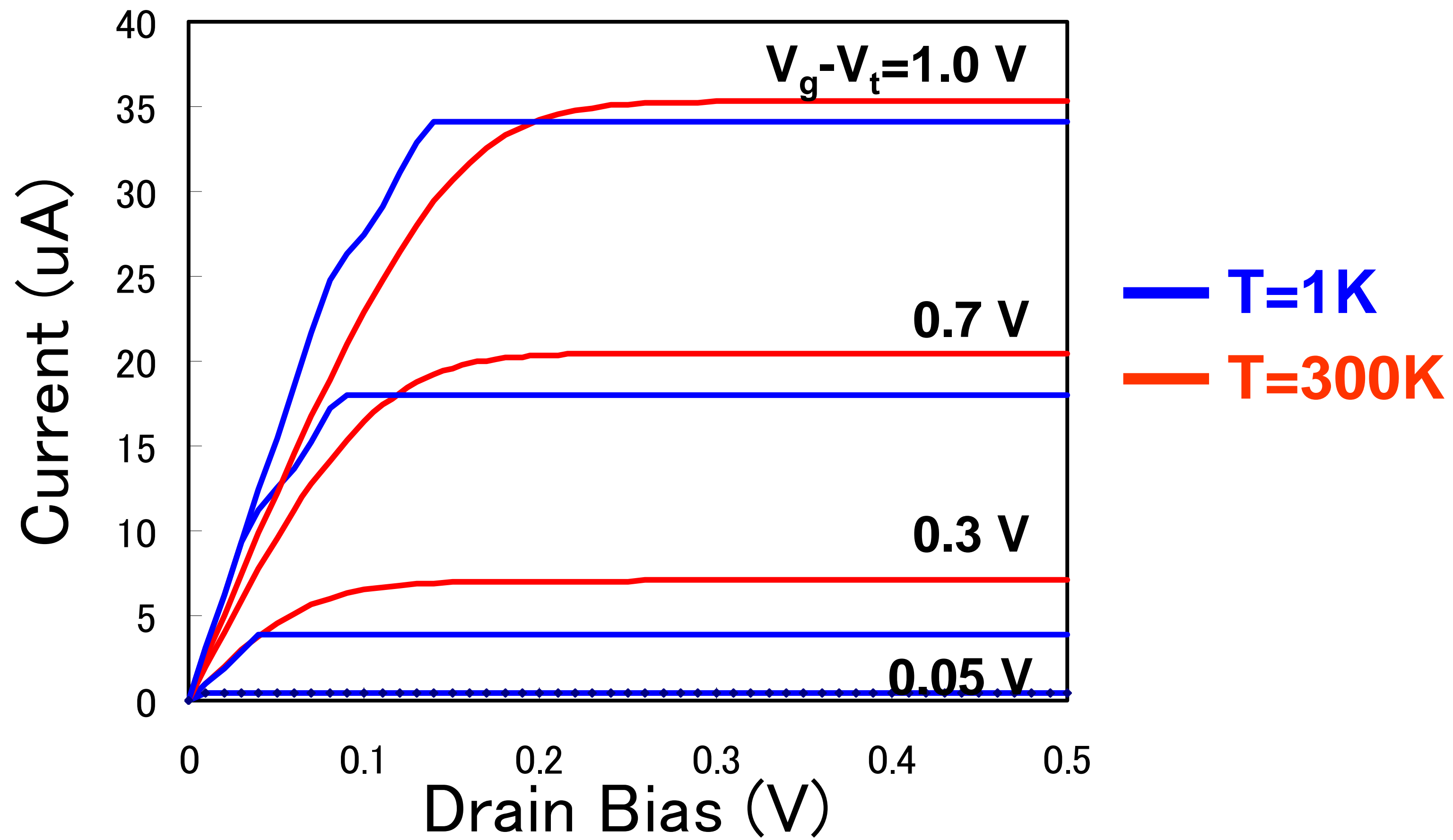


$$I_D = \frac{q}{\pi\hbar}\sum_i \int \left[f(E,\mu_S) - f(E,\mu_D) \right] T_i(E)\,dE$$

From x_{max} to x_{min} $\quad T_i(E) \approx 1$

$$I_D = G_0\left(\frac{k_B T}{q}\right)\sum_i g_i \ln\left\{\frac{1+\exp\left[(\mu_S - E_{i0})/k_B T\right]}{1+\exp\left[(\mu_D - E_{i0})/k_B T\right]}\right\}$$

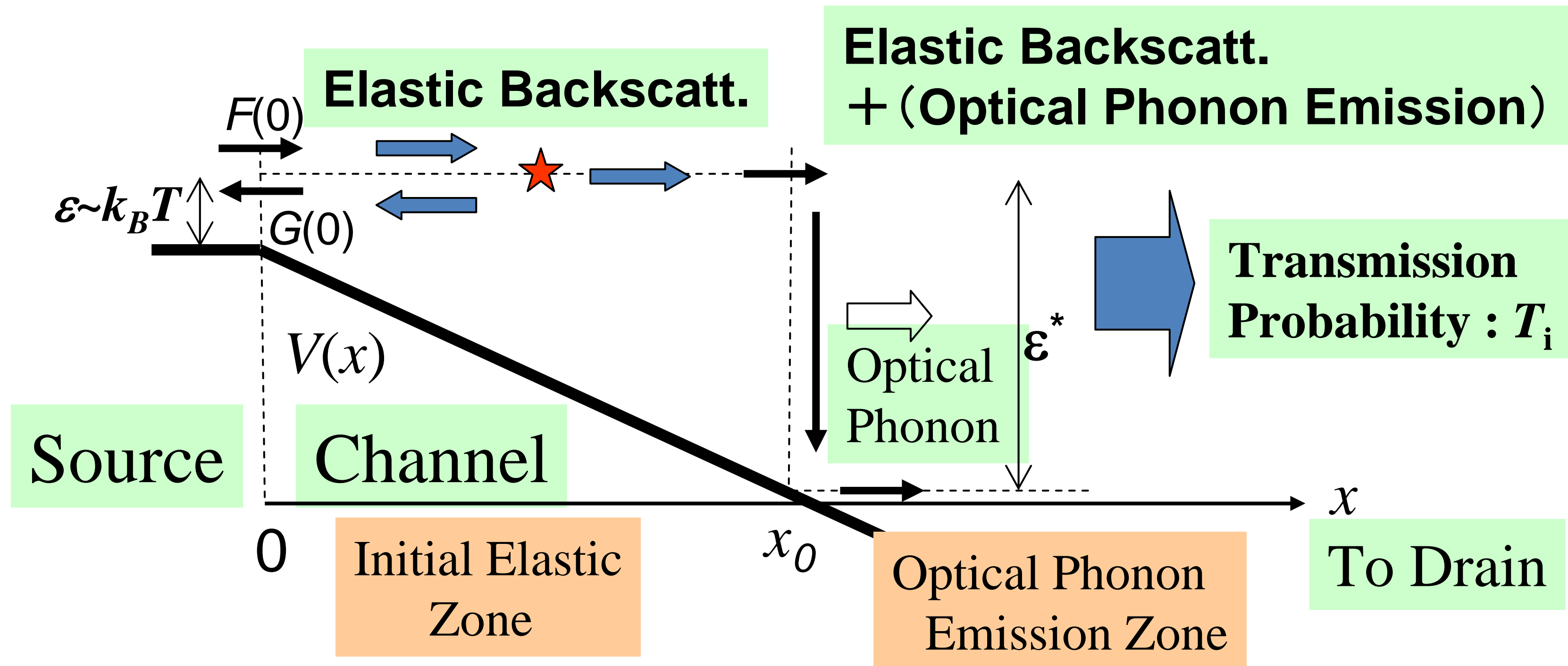
IV Characteristics of Ballistic SiNW FET



Small temperature dependency
35μA/wire for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx. :   Electric Field *E*



Transmission Probability to Drain

$$T(\varepsilon) = \left. \frac{F(0) - G(0)}{F(0)} \right)_{\text{Injection from Drain}=0}$$

Résumé of the Compact Model

$$I = \frac{q}{\pi\hbar}\sum_i g_i \int \left[f(\varepsilon,\mu_s) - f(\varepsilon,\mu_D) \right] T_i \, d\varepsilon$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left\{ \frac{\sqrt{2r+t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r+t_{ox}} - \sqrt{t_{ox}}} \right\}}.$$

Planar Gate

$$(V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{\left| Q_f + Q_b \right|}{C_G}.$$

$$\mu_S - \mu_D = qV_D$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left(\frac{r+t_{ox}}{r} \right)}.$$

GAA

(Electrostatics requirement)

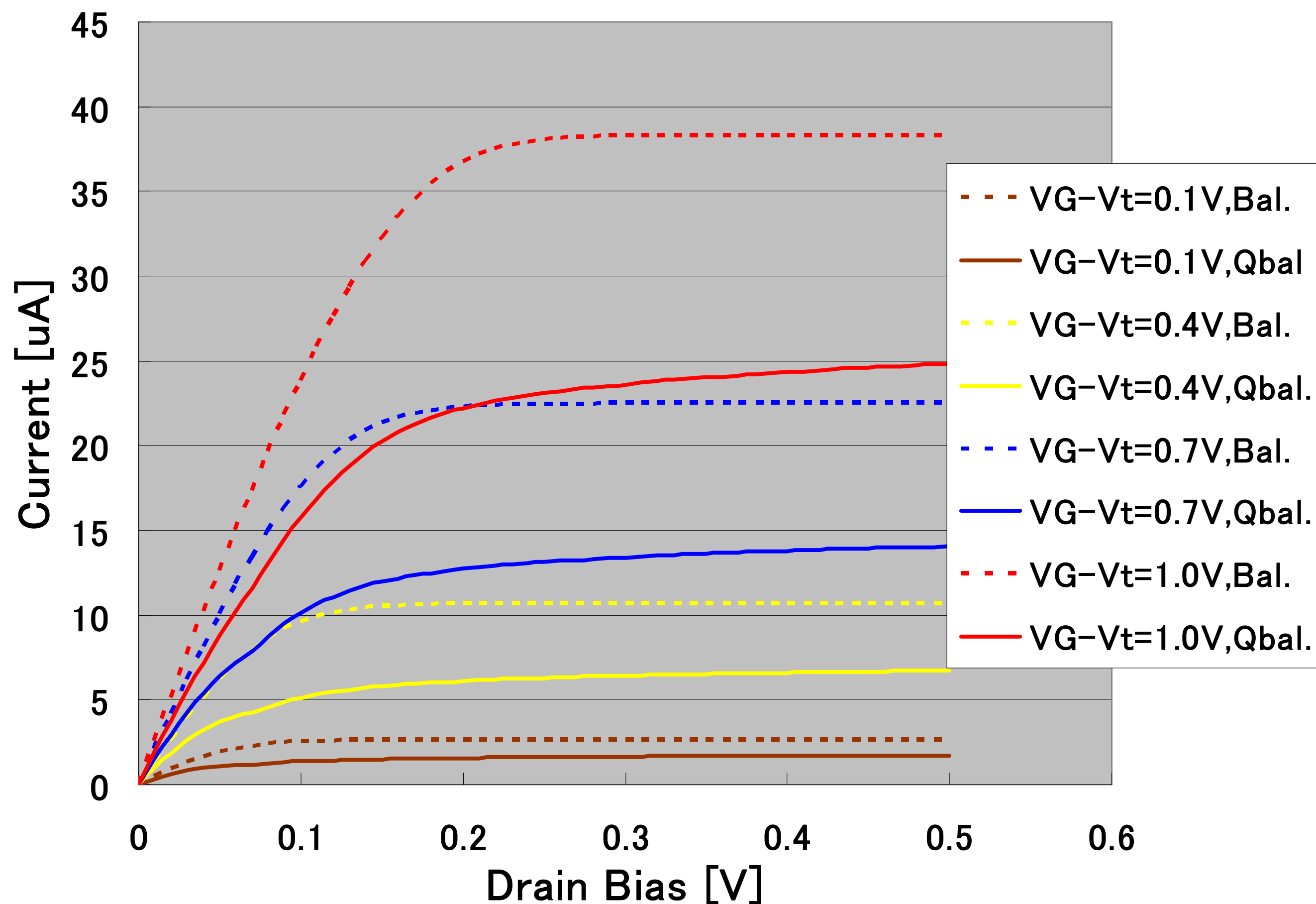
$$\left| Q_f + Q_b \right| = \frac{q}{\pi}\sum_i g_i \left[\int_{-\infty}^{\infty} \frac{dk}{1+\exp\left\{ \frac{\varepsilon_i(k)-\mu_S}{k_B T} \right\}} - \int_{-\infty}^{0} \left\{ \frac{1}{1+\exp\left\{ \frac{\varepsilon_i(k)-\mu_S}{k_B T} \right\}} - \frac{1}{1+\exp\left\{ \frac{\varepsilon_i(k)-\mu_D}{k_B T} \right\}} \right\} T_i(\varepsilon_i(k)) dk \right]$$

$$T(\varepsilon) = \frac{\sqrt{2D_0}\, qE}{\left(\sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0}\, B_0 \ln\left(\frac{qEx_0 + \varepsilon}{\varepsilon} \right)}$$

(Carrier distribution in Subbands)

Unknowns are I_D, $(\mu_S - \mu_0)$, $(\mu_D - \mu_0)$, $(Q_f + Q_b)$

I-V_D Characteritics (RT)



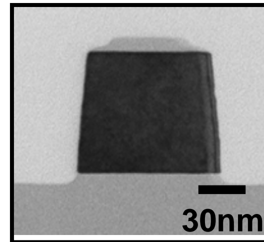
- Electric current 20～25 μA
- No satruration at Large V_D

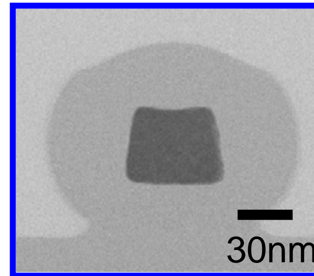
SiNW FET Fabrication

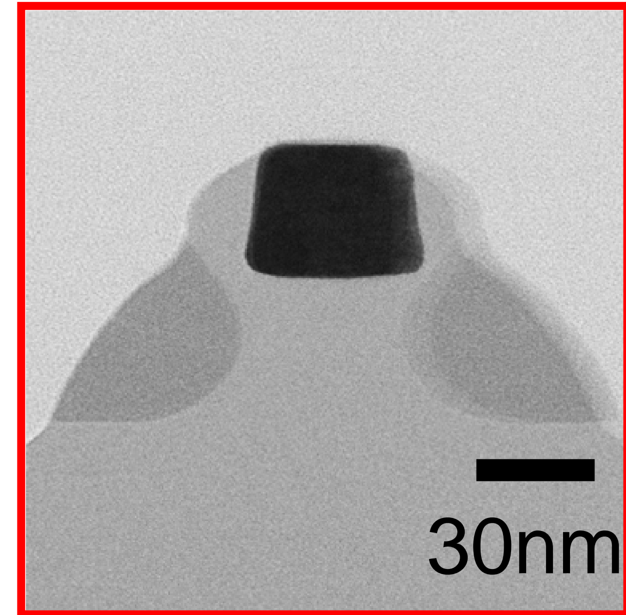
SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oixde etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

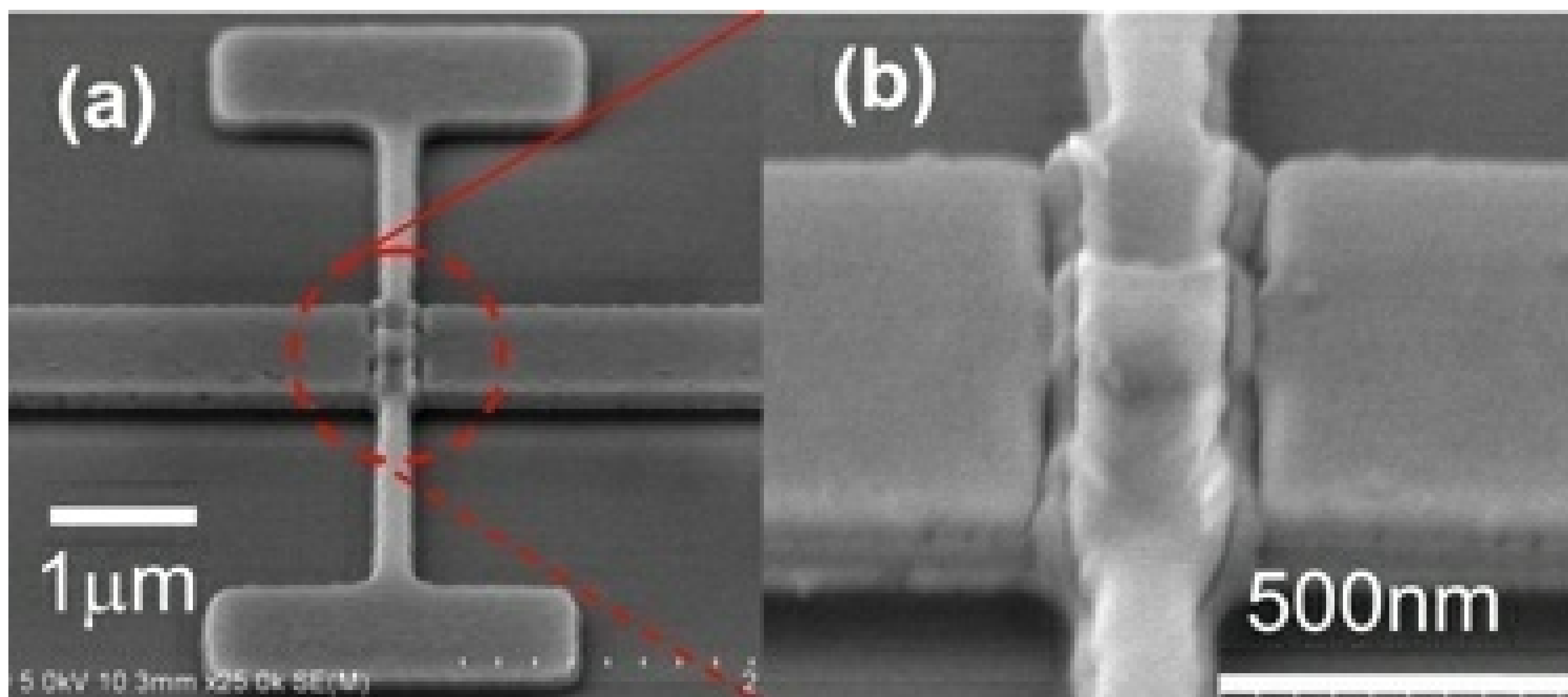
Standard recipe for gate stack formation



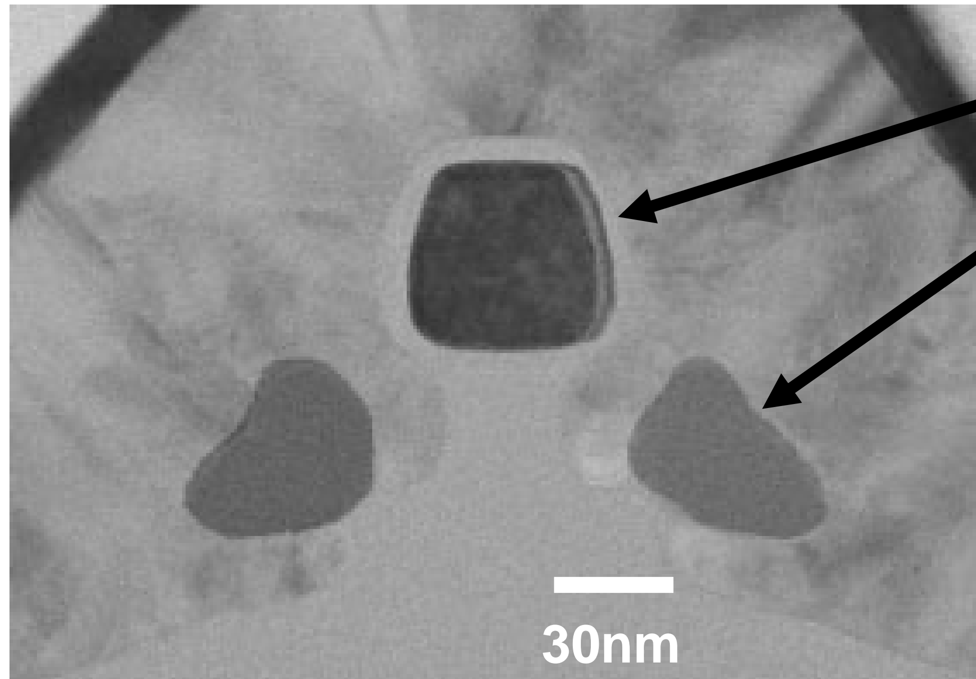




(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.

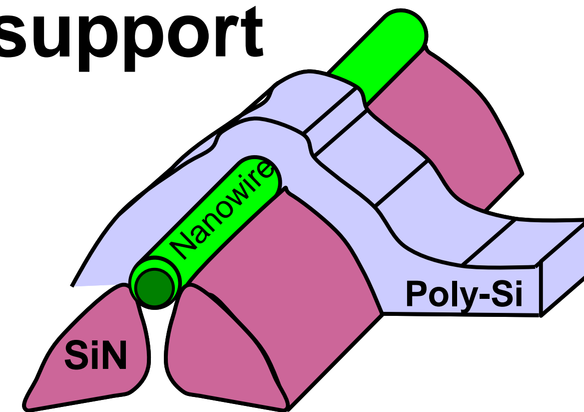


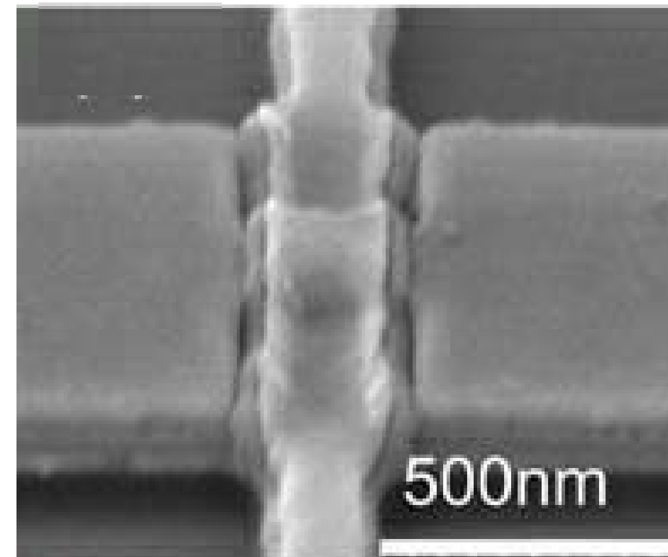
Fabricated SiNW FET



SiNW

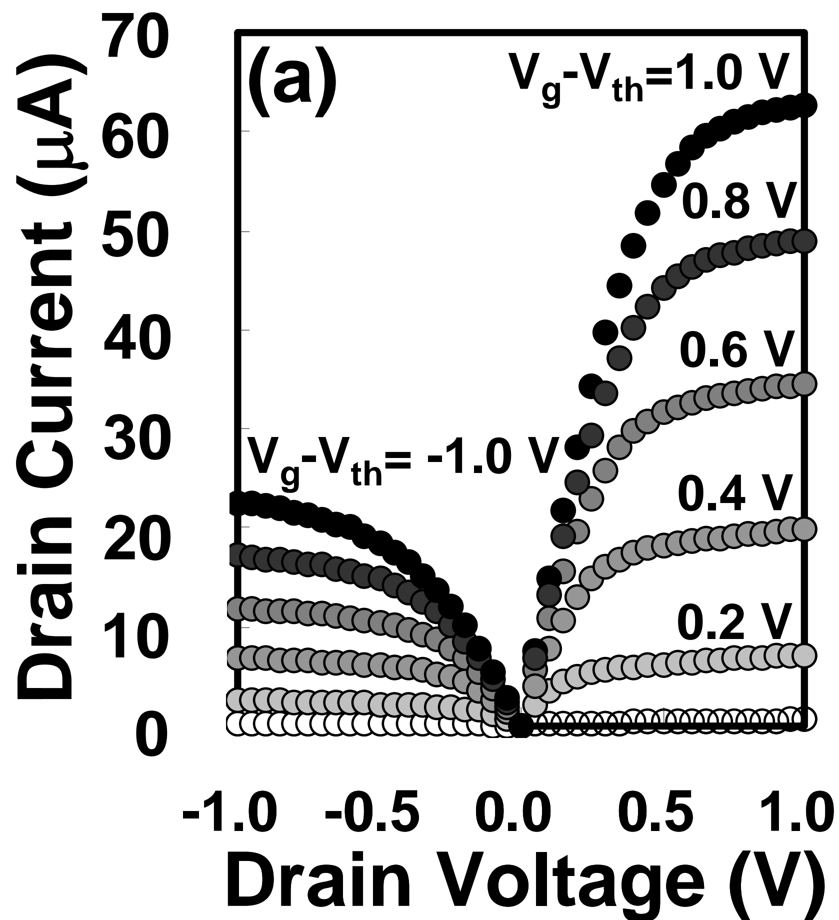
SiN support

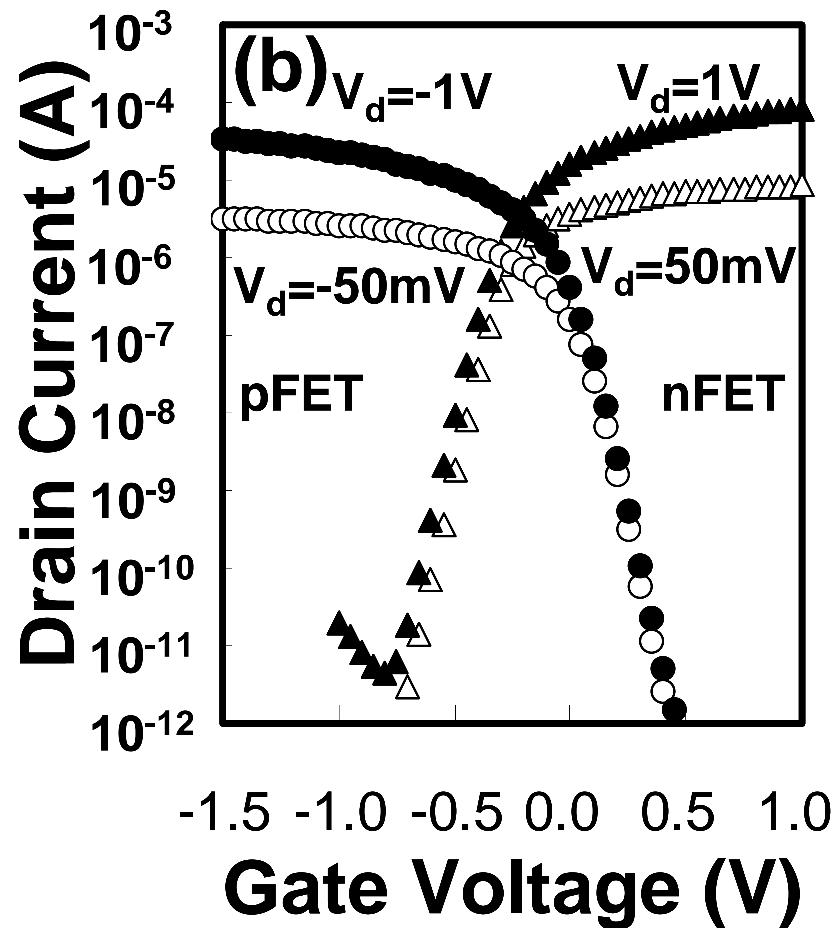




Recent results to be presented by ESSDERC 2010 next week in Sevile

Wire cross-section: 20 nm X 10 nm

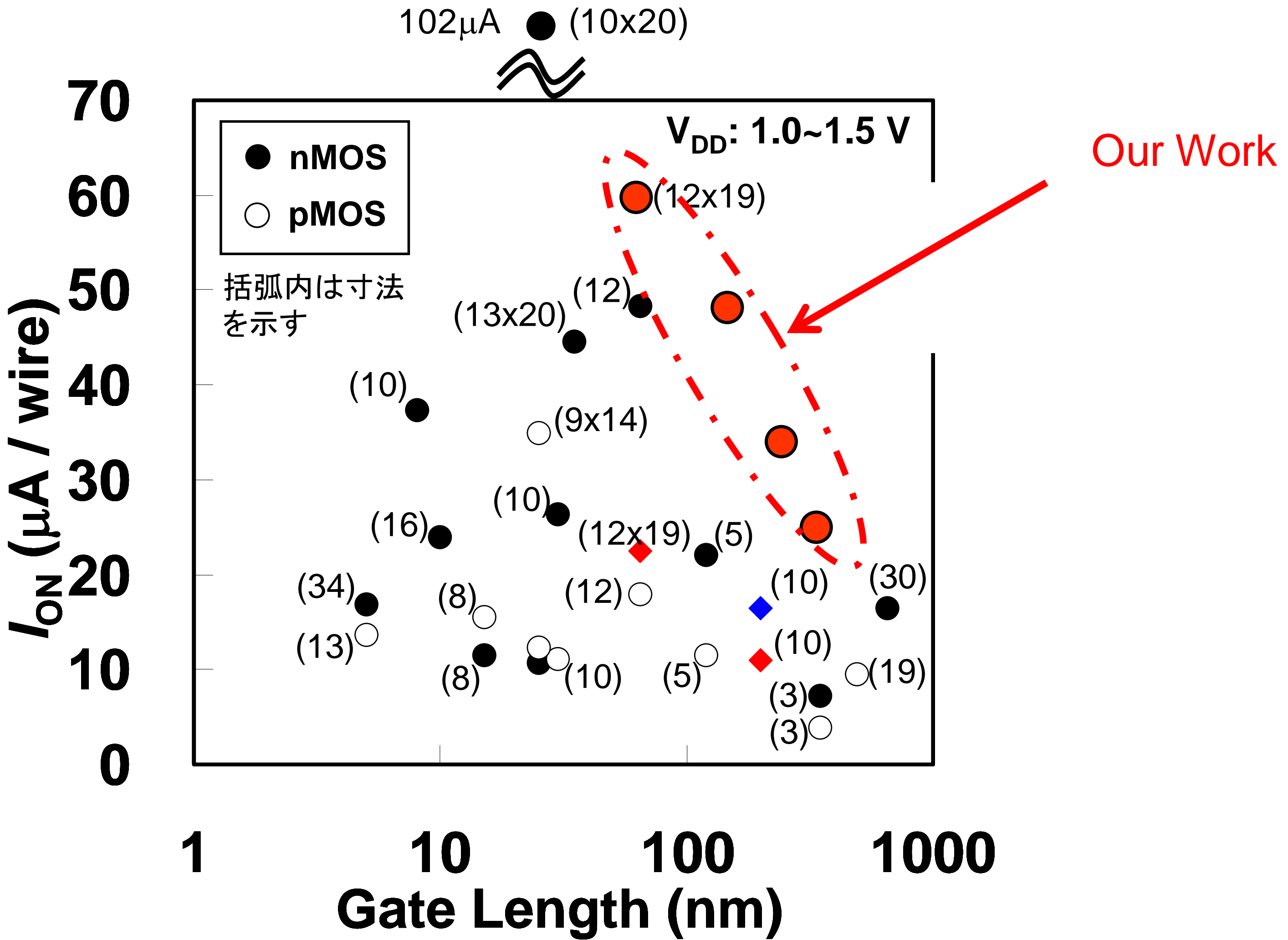




On/Off>10^6、60uA/wire

L_g=65nm, T_{ox}=3nm

Bench Mark



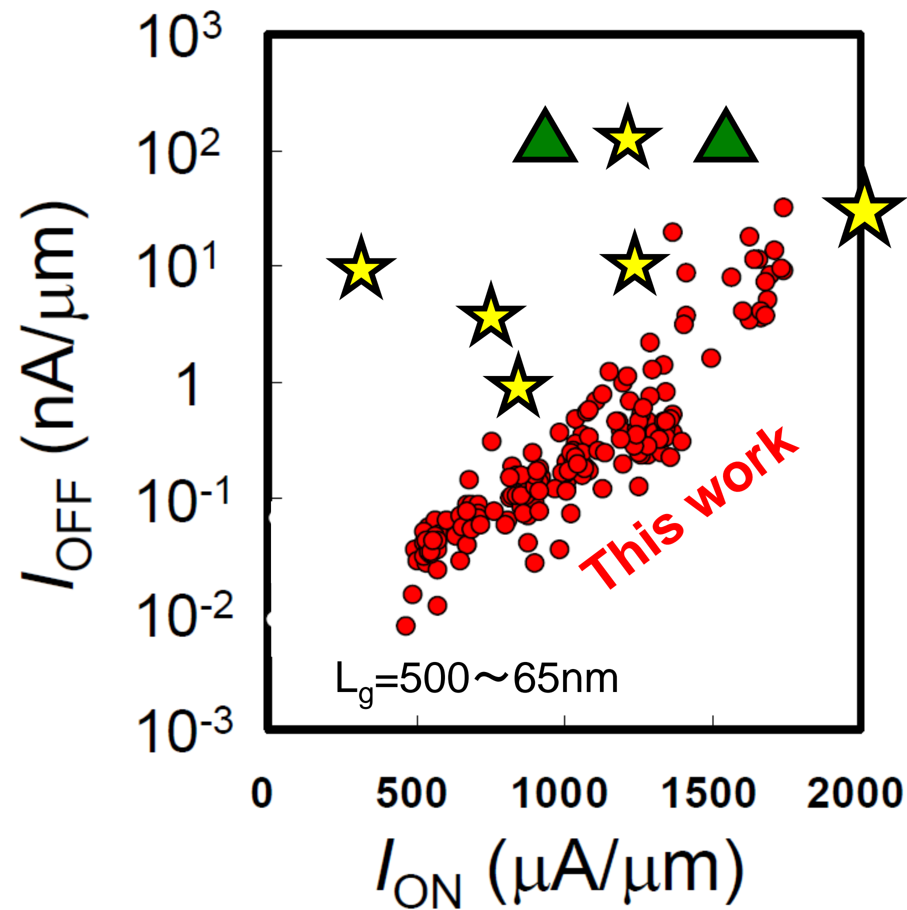
Bench Mark

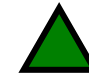
	This work	Ref[11]	Ref[12]	Ref[13]	Ref[14]	Ref[15]	Ref[4]
NW Cross-section (nm)	Rect.	Rect.	Rect.	Cir.	Cir.	Elliptical	Elliptical
NW Size (nm)	10x20	10x20	14	10	10	12	13x20
Lg (nm)	65	25	100	30	8	65	35
EOT or Tox (nm)	3	1.8	1.8	2	4	3	1.5
Vdd (V)	1.0	1.1	1.2	1.0	1.2	1.2	1.0
Ion(uA) per wire	60.1	102	30.3	26.4	37.4	48.4	43.8
Ion(uA/um) by dia.	3117	5010	2170	2640	3740	4030	2592
Ion(uA/um) by cir.	1609	2054	430	841	1191	1283	825
SS (mV/dec.)	70	79	68	71	75	~75	85
DIBL (mV/V)	62	56	15	13	22	40-82	65
Ion/Ioff	~1E6	>1E6	>1E5	~1E6	>1E7	>1E7	~2E5

Ref[11] by Stmicro Lg=25nm,Tox=1.8nm

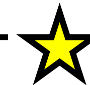
This work Lg=65nm,Tox=3nm

I_{ON}/I_{OFF} Bench mark

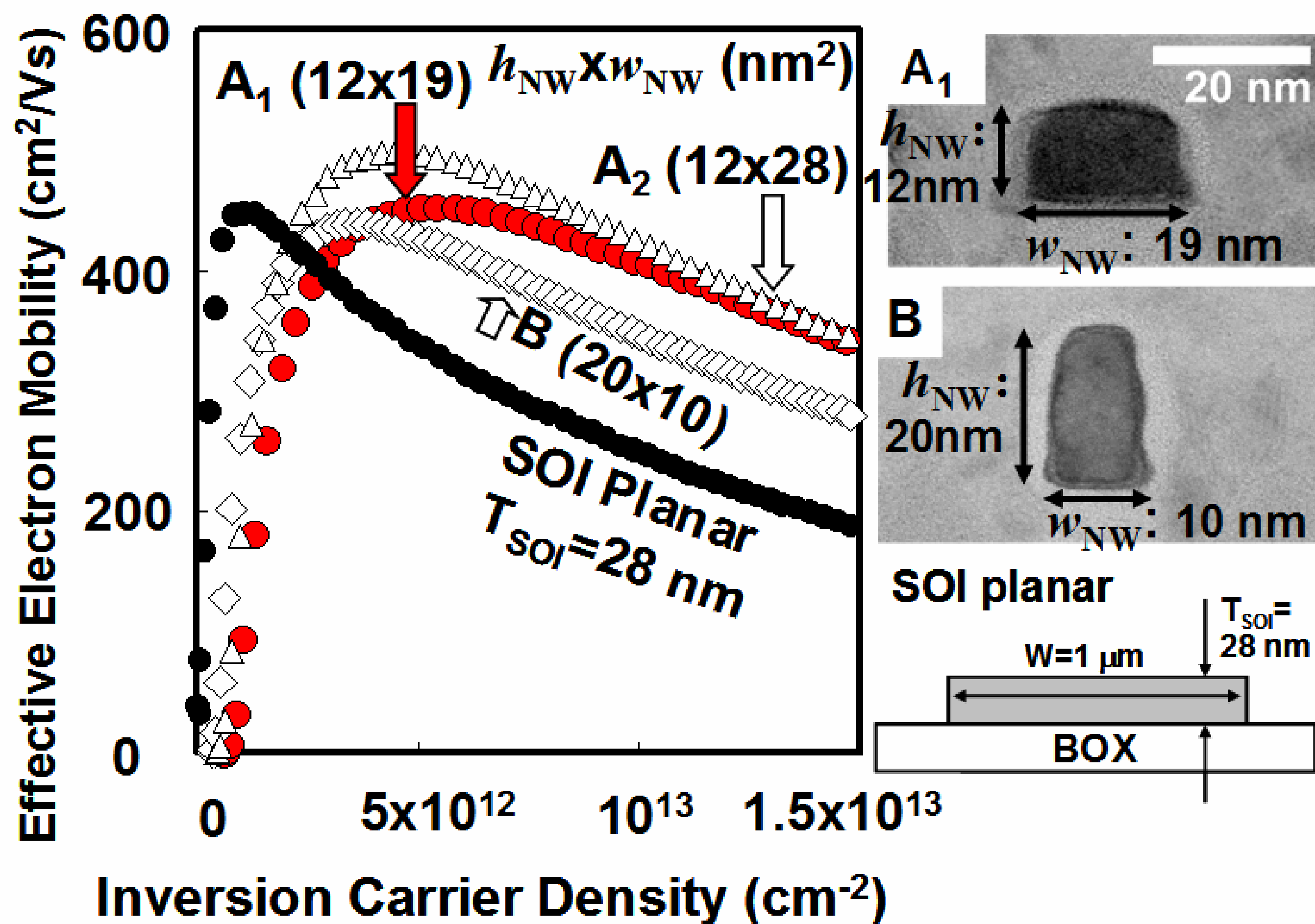


Planer FET  1.0〜1.1V

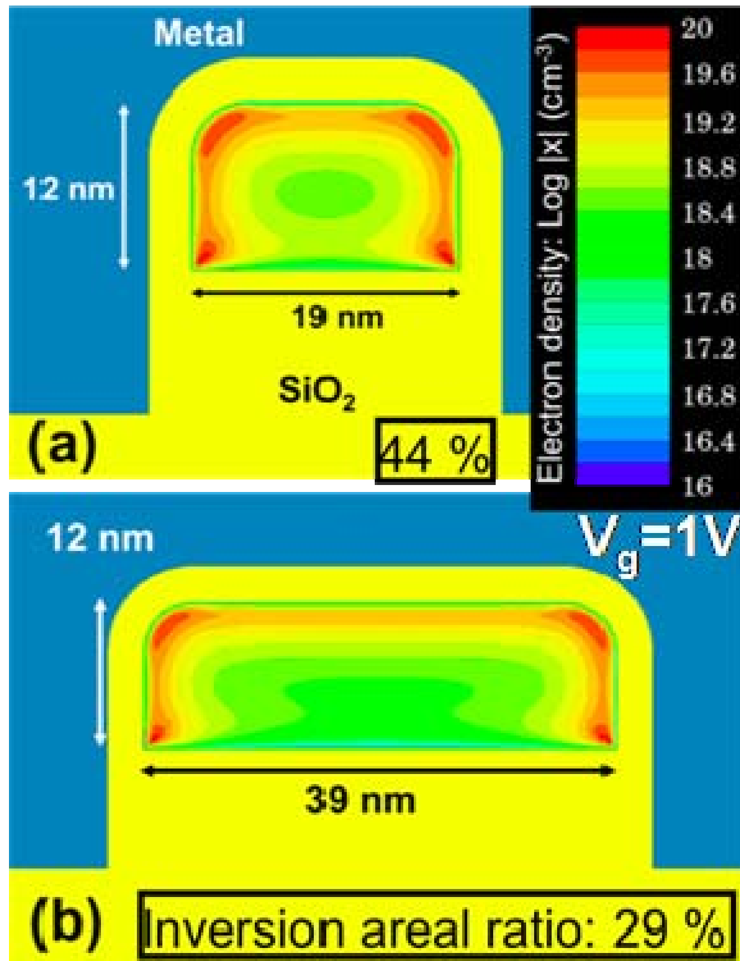
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

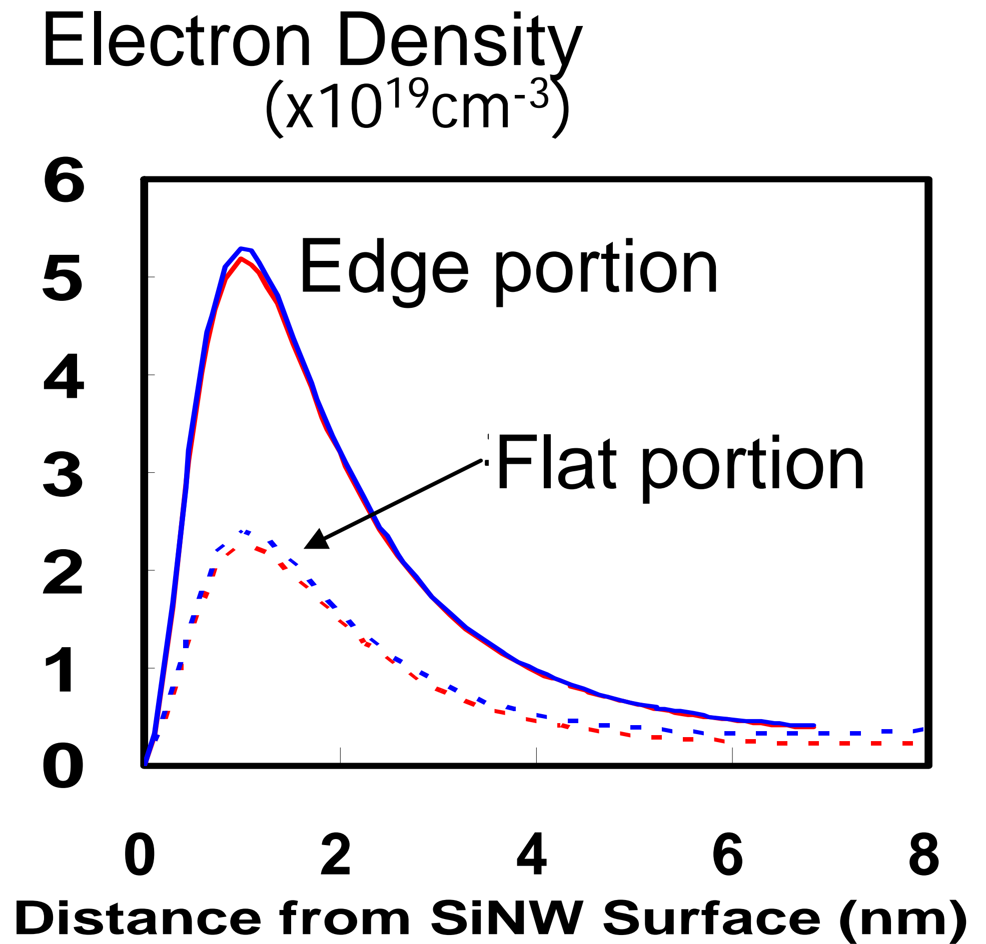
SiナノワイヤFET  1.2〜1.3V

Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240

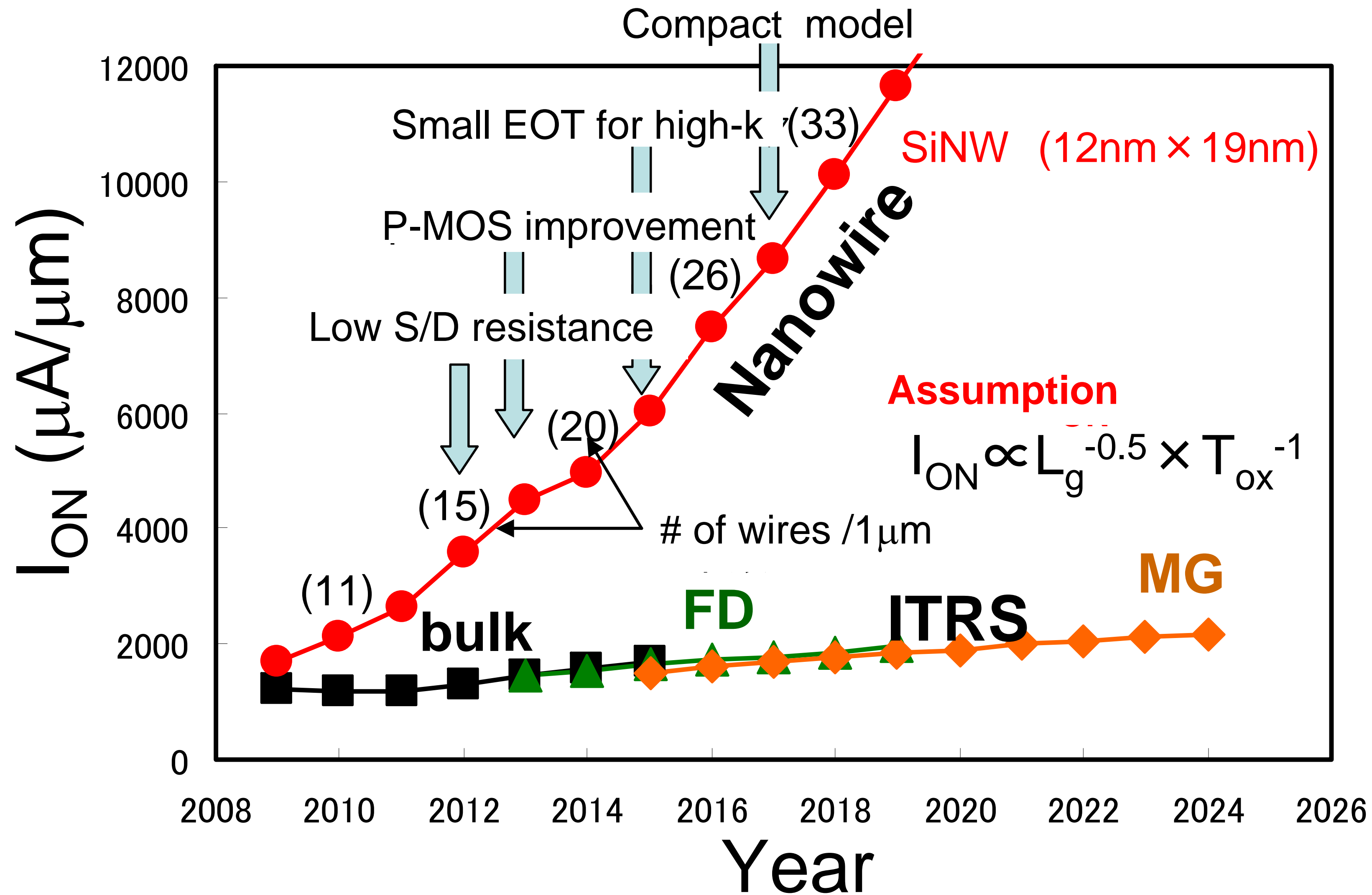


Effective Electron Mobility (cm²/Vs)
Inversion Carrier Density (cm⁻²)
600
400
200
0
0
5x10¹²
10¹³
1.5x10¹³
A1 (12x19)
hNW x wNW (nm²)
A2 (12x28)
B (20x10)
SOI Planar
TSOI=28 nm
A1
20 nm
hNW:
12nm
wNW: 19 nm
B
hNW:
20nm
wNW: 10 nm
SOI planar
TSOI=
28 nm
W=1 μm
BOX


Metal
12 nm
19 nm
SiO2
(a)
44 %
Electron density: Log |x| (cm-3)
20
19.6
19.2
18.8
18.4
18
17.6
17.2
16.8
16.4
16
Vg=1V
12 nm
39 nm
(b)
Inversion areal ratio: 29 %

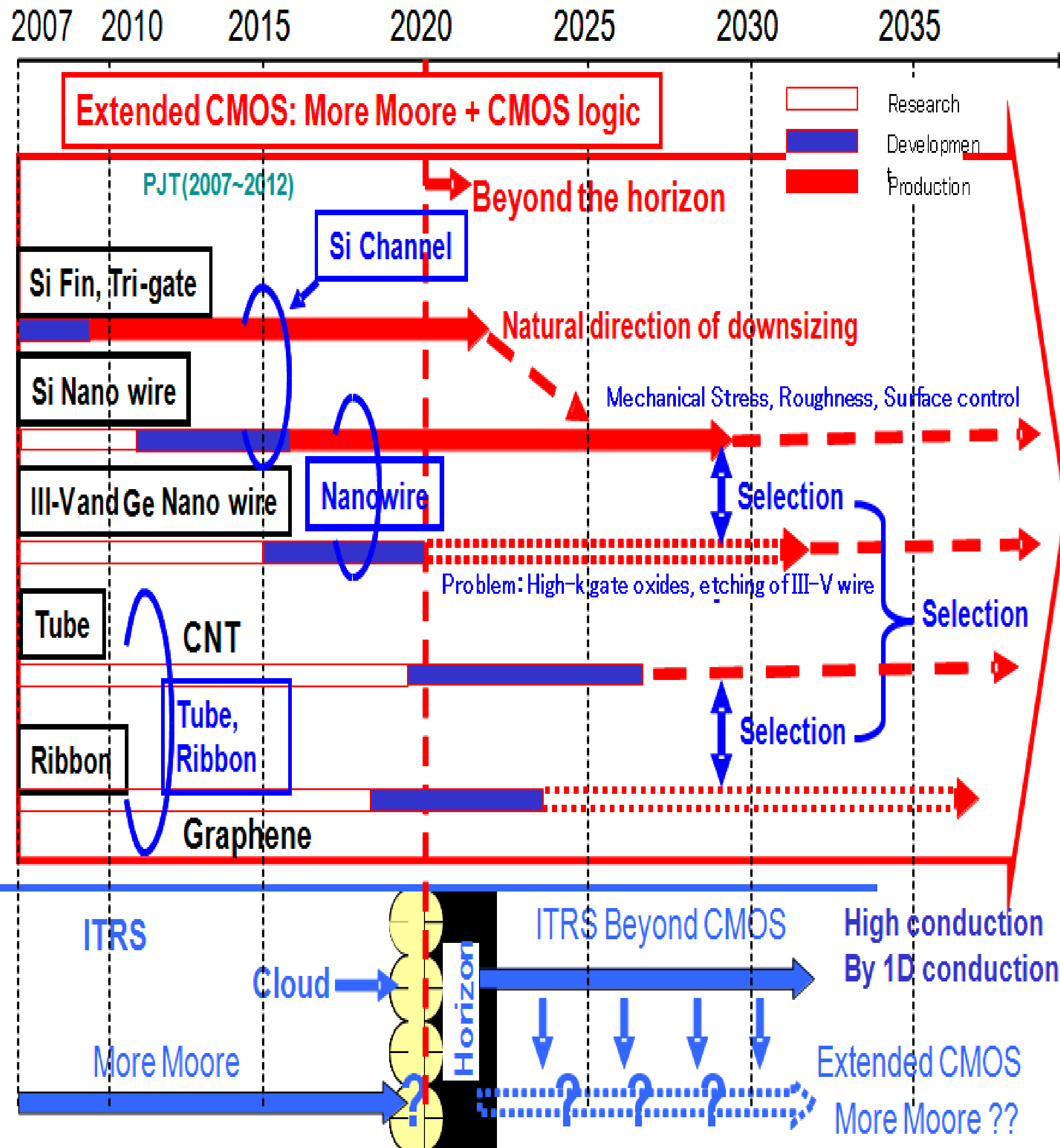

Electron Density
(x10^19cm^-3)
Edge portion
Flat portion
6
5
4
3
2
1
0
0
2
4
6
8
Distance from SiNW Surface (nm)

Primitive estimation !



Our roadmap for R &D

Source: H. Iwai, IWJT 2008



Current Issues

Si Nanowire

Control of wire surface property
Source Drain contact
Optimization of wire diameter
Compact I-V model

III-V & Ge Nanowire

High-k gate insulator
Wire formation technique

CNT:

Growth and integration of CNT
Width and Chirality control
Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique
Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

Thank you
for your attention!