Future of Si nano CMOS technology

April 14, 2011

Calcutta University
@Kolkata, India

Hiroshi Iwai,
Tokyo Institute of Technology
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
Institute Overview

Established in 1881 → 130th anniversary in 2011

3 undergraduate schools
- School of Science, School of Engineering, School of Bioscience and Biotechnology

7 graduate schools
- Science and Engineering Science, Science and Engineering Technology,
- Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
- Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

<table>
<thead>
<tr>
<th></th>
<th>Undergraduate</th>
<th>Graduate</th>
<th>Master's</th>
<th>Doctoral</th>
<th>Teaching Staff</th>
<th>Student/Instructor</th>
<th>Staff</th>
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<tr>
<td>Tokyo Inst.</td>
<td>5,000</td>
<td>5,000</td>
<td>3,500</td>
<td>1,500</td>
<td>1,200</td>
<td>8.3</td>
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<td>Per Year</td>
<td>1,200</td>
<td>1,800</td>
<td>500</td>
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</table>

Einstein Visit
Asia 847
Europe 78
Africa 16
North America 12
South America 24
Oceania 5

Total 982
(As of May. 1, 2005)
研究風景
Cluster tool for high-k thin film deposition
• There were many inventions in the 20\textsuperscript{th} century: Airplane, Nuclear Power generation, Computer, Space aircraft, etc
• However, everything has to be controlled by electronics

Electronics
  Most important invention in the 20\textsuperscript{th} century

• What is Electronics: To use electrons, Electronic Circuits
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Same mechanism as that of transistor
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
CMOS Technology: Indispensable for our human society

All the human activities are controlled by CMOS living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS: There is no computer in banks, and world economical activities immediately stop.

Cellarer phone dose not exists
Downsizing of the components has been the driving force for circuit evolution.

<table>
<thead>
<tr>
<th>Year</th>
<th>1900</th>
<th>1950</th>
<th>1960</th>
<th>1970</th>
<th>2000</th>
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<tr>
<td>Devices</td>
<td>Vacuum Tube</td>
<td>Transistor</td>
<td>IC</td>
<td>LSI</td>
<td>ULSI</td>
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<tr>
<td>Size</td>
<td>10 cm</td>
<td>cm</td>
<td>mm</td>
<td>10 µm</td>
<td>100 nm</td>
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<tr>
<td>Metric</td>
<td>10⁻¹m</td>
<td>10⁻²m</td>
<td>10⁻³m</td>
<td>10⁻⁵m</td>
<td>10⁻⁷m</td>
</tr>
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</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. **Reduce Capacitance**
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. **Increase number of Transistors**
   - Parallel processing
     - Increase circuit operation speed

---

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.
Question: How far we can go with downscaling?
How far can we go?

Past  0.7 times per 3 years  In 40 years: 15 generations,
    1973 年  Size 1/200, Area 1/40,000
     8 µm → 6 µm → 4 µm → 3 µm → 2 µm → 1.2 µm → 0.8 µm → 0.5 µm
     → 0.35 µm → 0.25 µm → 180 nm → 130 nm → 90 nm → 65 nm → 45 nm

Now

Future

→ 32 nm → 22 nm → 16 nm → 11.5 nm → 8 nm → 5.5 nm? → 4 nm? → 2.9 nm?

- At least 5,6 generations, for 15 ~ 20 years

- Hopefully 8 generations, for 30 years
HP, LOP, LSTP for Logic CMOS

- **HP CMOS** (High Performance)
  - Highest Ion, Lowest CV/I
  - High leakage
  - Medium Vdd

- **LOP CMOS** (Low Operation Power)
  - Lowest Vdd
  - Medium Ion, medium CV/I
  - Medium leakage

- **LSTP CMOS** (Low Standby Power)
  - Lowest leakage
  - Low Ion, high CV/I
  - High Vdd

Source: 2007 ITRS Winter Public Conf.
Scaling Method: by R. Dennard in 1974

$W_{\text{dep}}$: Space Charge Region (or Depletion Region) Width

$W_{\text{dep}}$ has to be suppressed
Otherwise, large leakage between S and D

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

$K=0.7$
for example

By the scaling, $W_{\text{dep}}$ is suppressed in proportion, and thus, leakage can be suppressed.

Good scaled I-V characteristics

$W_{\text{dep}} \propto \sqrt{V/Na}$

$I : K$
Scaling of high beyond 0.5 nm is important

Power of FET = $CV^2/2 \cdot D^3 (= L^3)$

Problems
- SCE
- Variation in Vth
- Increase in Off-leakage current

Solution
- Scaling of high beyond 0.5 nm is important
Down scaling is the most effective way of Power saving.

It has been always discussed about the limit of downscaling, but the down scaling of MOSFETs is still possible for another 10 or 20 years!

3 important technological items for DS.

1. Thinning of high-k beyond 0.5 nm

2. Metal S/D

3. Si-Nanowire FET
High k gate stack
To use high-k dielectrics

Thin gate SiO$_2$

Almost the same electric characteristics

Thick gate high-k dielectrics

K: Dielectric Constant

Thick
Small leakage Current

However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO$_2$!
Choice of High-k elements for oxide

<table>
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<tr>
<th>Candidates</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active He</th>
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<tr>
<td>H</td>
<td></td>
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<tr>
<td>Li, Be</td>
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<td>Mg, Na</td>
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<tr>
<td>K, Ca, Sc</td>
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<tr>
<td>Sr, Y, Zr</td>
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<tr>
<td>Cs, Ba</td>
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<tr>
<td>Cs, Ba</td>
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<tr>
<td>Fr, Ra, Rf</td>
<td>Ha, Sg, Ns, Hs, Mt</td>
<td></td>
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<tr>
<td>La, Ce, Pr, Nd, Pm</td>
<td>Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Y, Lu</td>
<td></td>
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</table>

Unstable at Si interface

- Si + MO\(_x\) \(\text{M} + \text{SiO}_2\)
- Si + MO\(_x\) \(\text{MSi}_x + \text{SiO}_2\)
- Si + MO\(_x\) \(\text{M} + \text{MSi}_x\text{O}_y\)

Hf\(_2\)O\(_2\) based dielectrics are selected as the first generation materials, because of their merit in 1) band-offset, 2) dielectric constant, 3) thermal stability.

La\(_2\)O\(_3\) based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

Choice of High-k elements for oxide are selected as the first generation materials, because of their merit in 1) band-offset, 2) dielectric constant, 3) thermal stability.

R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

XPS measurement by Prof. T. Hattori, INFOS 2003
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness
For the past 45 years, SiO2 and SiON have been used as gate insulators. However, the EOT (Equivalent Oxide Thickness) limit is approximately 0.7~0.8 nm. Today, EOT=1.0 nm for 45nm node with Lg=22nm.

One order of magnitude improvement is possible by introducing High-k materials.

EOT can be reduced further beyond 0.5 nm by using direct contact to Si by choosing appropriate materials and processes.
Reports on direct contact of high-k/Si

IL scavenging


Our approach

K. Kakushima, et al., ESSDERC2009

W

La$_2$O$_3$  $k=23$

La-silicate  $k=8$~$14$

Silicate formation

La$_2$O$_3$+Si+nO$_2$
  $\rightarrow$  La$_2$SiO$_5$  La$_{10}$(SiO$_4$)$_6$O$_3$
  La$_{9.33}$Si$_6$O$_{26}$  La$_2$Si$_2$O$_7$

La$_2$O$_3$ can easily achieve direct contact of high-k/Si

Control of oxygen atoms

Direct HfO$_2$/Si structure
EOT = 0.48 nm

Our results

Transistor with La2O3 gate insulator
EOT=0.37nm
La2O3

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

0.48 → 0.37nm Increase of $I_d$ at 30%
$\mu_{\text{eff}}$ of W/La$_2$O$_3$ and W/HfO$_2$ nFET on EOT

- W/La$_2$O$_3$ exhibits higher $\mu_{\text{eff}}$ than W/HfO$_2$
- $\mu_{\text{eff}}$ start degrades below EOT=1.4nm
FET characteristics of W/La$_2$O$_3$ on EOT

All characteristics start to degrade or shift below EOT=1.4nm

N$_{\text{fix}}$=7x10$^{12}$ cm$^{-2}$

Aggressive N$_{\text{fix}}$ generation at EOT<1.2nm

N$_{\text{fix}}$ and D$_{\text{it}}$

All characteristics start to degrade or shift below EOT=1.4nm
Gate Metal Induced Defects Compensation

Suppression of aggressive shift in $V_{fb}$

Metal Gate
- MgO
- La2O3
- Si

TEM
EDX

PMA500°C
Mobility Improvement with Mg Incorporation

Recovery of $\mu_{\text{eff}}$ mainly at low $E_{\text{eff}}$
Problems for scaled EOT with La$_2$O$_3$


W electrode supplies oxygen to La$_2$O$_3$

Excess oxygen
Excess silicate formation (EOT increase)

(2) C. S. Park et al., SSDM 2007, p.14

W is high oxygen diffusivity metal

Deficient oxygen
Oxygen vacancy (reduced mobility, gate leakage)

Control of oxygen
Strategy & Concept

Oxygen trigger the silicate reaction

Poly-Si prevent the oxygen diffusion

Oxygen in W metal is consuming during annealing process
Experimental procedure

n-Si Substrate

- SPM and HF cleaning
- La$_2$O$_3$ deposition (300°C)
- Gate metal (W) deposition by RF sputtering
- TiN deposition by RF sputtering (Ar:N$_2$=9:1)
- Si deposition (100nm) by RF sputtering
- Gate patterning
- FGA (3% H$_2$) at 800°C for 30min
- Si removal by TMAH
- Backside Al contact
- Annealing in 5% O$_2$ for 30min
- FGA (3% H$_2$) at 420°C for 30min
- Measurement

in-situ

- TiN : barrier layer
C-V characteristics ~TiN/W~

TiN layer is effective to suppress the increase in EOT

Barrier layer or Oxygen getter
C-V characteristics ~MIPS~

EOT increase is dramatically suppressed with MIPS

$V_{FB}$ is almost identical
Comparison of C-V characteristics

EOT of 0.69nm can be attained with a combination of MIPS structure and FGA 800 °C 30min

2011-4-25
Effect of gate metal structure on EOT

Si Cap layer can prevent the excess oxygen incorporation from atmospheric
Oxygen incorporation through TiN/W

T. Kawanago, et al., ESSDERC2010

Positive $V_{FB}$ shift increase with decreasing the TiN thickness
Oxygen incorporation after Si removal

Positive $V_{FB}$ shift by 490mV can be observed

EOT degradation is less than 1Å
6 µm NMOS LSI in 1974

Layers
1. Si substrate
2. Field oxide
3. Gate oxide
4. Poly Si
5. S/D
6. Interlayer
7. Aluminum
8. Passivation

Materials
1. Si
2. SiO₂
3. BPSG
4. Al
5. PSG

Atoms
1. Si
2. O
3. P
4. B
5. Al
(H, N, Cl)
New materials

Just examples!
Many other candidates

Semiconductors
- Ge
- III-V
- Si
- SiO₂
- Al
- Poly Si
- PtSi₂
- WSi₂
- CoSi₂
- TiSi₂
- MoSi₂
- TaSi₂
- NiSi silicide
- SiGe Semiconductor
- Air
- HSQ
- Polymer
- Low-k dielectrics
- TiN
- TaN
- Cu
- Metals
- W
- Electrode materials
- RuO₂
- Pt
- IrO₂
- Y₁
- PZT
- BST
- Ferroelectrics

High-k dielectrics
- La₂O₃
- Ta₂O₅
- HfO₂
- ZrO₂
- ZrSiₓOᵧ

Low-k dielectrics
- Air
- HSQ
- Polymer


Y. Nishi, Si Nano Workshop, 2006,
(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)
Si nanowire FET
Because of off-leakage control,

\[ \text{Planar} \rightarrow \text{Fin} \rightarrow \text{Nanowire} \]
Nanowire FET

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<td>Multiple Gate</td>
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2015
22 or 16nm node
Multiple Gate (Fin) FET

2020
11 or 8nm node
Nanowire FET

ITRS 2009
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of $I_{OFF}$
3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires

Leakage current

cut-off

Gate: OFF

Source: drain

$W_{dep}$
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

300 K
$E_g = 1.12 \text{ eV}$
$E_l = 2.0 \text{ eV}$
$E_x = 1.2 \text{ eV}$
$E_v = 0.044 \text{ eV}$
$E_{T1} = 3.4 \text{ eV}$
$E_{T2} = 4.2 \text{ eV}$

Energy band of 3 x 3 Si wire

4 channels can be used
Maximum number of wires per 1 µm

Front gate type MOS
- 165 wires /µm

Surrounded gate type MOS
- 33 wires/µm

6nm pitch
By nano-imprint method

- Metal gate electrode (10nm)
- High-k gate insulator (4nm)
- Si Nano wire (Diameter 2nm)

30nm pitch:
- EUV lithography

Surrounded gate MOS
Device fabrication

- **Si/Si$_{0.8}$Ge$_{0.2}$ superlattice epitaxy on SOI**
- **Anisotropic etching of these layers**
- **Isotropic etching of SiGe**
- **The NW diameter is controllable down to 5 nm by self limited oxidation.**

**Process Details:**
3D-stacked Si NWs with Hi-$k$/MG

Wire direction: $<110>$
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT $\sim$2.6 nm
SiNW Band structure calculation
Cross section of Si NW

First principal calculation,

D=1.96nm  [001]
D=1.94nm  [011]
D=1.93nm  [111]
Si nanowire FET with 1D Transport

Orientation [001] [011] [111]
Diameter (nm) 0.86 0.94 0.89

Energy (eV)
1
0
-1
G Z G

Wave Number
Z G Z

Small mass with [011]
Large number of quantum channels with [001]
Atomic models of a Si quantum dot and Si nanowires

6.6 nm diameter SiQD
(8651 atoms)

10 nm diameter Si(100)NW
(2341 atoms)

20 nm diameter Si(100)NW
(8941 atoms)
RSDFT – suitable for parallel first-principles calculation -

- Real-Space Finite-Difference
- Sparse Matrix
- FFT free (FFT is inevitable in the conventional plane-wave code)
- MPI (Message Passing Interface) library

Kohn-Sham eq. (finite-difference)

\[
\left(-\frac{1}{2} \nabla^2 + v_s[\rho](\mathbf{r}) + \hat{v}_{\text{PP}}^{\text{PP}}(\mathbf{r})\right)\psi_n(\mathbf{r}) = \varepsilon_n \psi_n(\mathbf{r})
\]

Higher-order finite difference

\[
\frac{\partial^2}{\partial x^2} \psi_n(x, y, z) \approx \sum_{m=-6}^{6} C_m \psi_n(x + m\Delta x, y, z)
\]

Integration

\[
\int \psi_m(\mathbf{r})\psi_n(\mathbf{r})d\mathbf{r} \approx \sum_{i=1}^{\text{Mesh}} \psi_m(\mathbf{r}_i)\psi_n(\mathbf{r}_i)\Delta x \Delta y \Delta z
\]
Massively Parallel Computing

Iwata et al, J. Comp. Phys., to be published

Real-Space Density-Functional Theory code (RSDFT)

Based on the finite-difference pseudopotential method (J. R. Chelikowsky et al., PRB1994)

Highly tuned for massively parallel computers

Computations are done on a massively-parallel cluster PACS-CS at University of Tsukuba.
(Theoretical Peak Performance = 5.6GFLOPS/node)

e.g.) The system over 10,000 atoms $\mathrm{Si}_{10701}\mathrm{H}_{1996}$
(7.6 nm diameter Si dot)

Convergence behavior for $\mathrm{Si}_{10701}\mathrm{H}_{1996}$

Grid points = 3,402,059
Bands = 22,432

Computational Time (with 1024 nodes of PACS-CS)
6781 sec. $\times$ 60 iteration step = 113 hour
Band Structure and DOS of Si(100)NWs (D=1nm, 4nm, and 8nm)

D=1nm
Si21H20 (41 atoms)
KS band gap=2.60eV

D = 4 nm
Si341H84 (425 atoms)
KS band gap = 0.81eV

D=8 nm
Si1361H164 (1525 atoms)
KS band gap=0.61eV

KS band gap of bulk (LDA) = 0.53eV
Band structure of 8-nm-diameter Si nanowire near the CBM

- KS band gap = 0.608 eV (@Γ)

![Band structure diagram]

Each band is 4-dgenerate.

Effective mass equation

\[
\left[-\frac{\hbar^2}{2m^*} \left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}\right) - \frac{\hbar^2}{2m^*} \frac{\partial^2}{\partial z^2}\right] \Phi(r) = (\varepsilon - \varepsilon_{CBM}) \Phi(r)
\]

The band structure can be understood that electrons near the CBM in the bulk Si are Confined within a cylindrical geometry.
Si12822H1544 (14,366 atoms)
- 10nm diameter, 3.3nm height, (100)
- Grid spacing 0.45Å (~14Ry)
- # of grid points 4,718,592
- # of bands 29,024
- Memory 1,022GB ～ 2,044GB
SiNW Band compact model
Landauer Formalism for Ballistic FET

\[ I_D = \frac{q}{\pi \hbar} \sum_i \int [f(E, \mu_S) - f(E, \mu_D)] T_i(E) dE \]

From \( x_{\text{max}} \) to \( x_{\text{min}} \) \( T_i(E) \approx 1 \)

\[ I_D = G_0 \left( \frac{k_B T}{q} \right) \sum_i g_i \ln \left\{ \frac{1 + \exp \left[ (\mu_S - E_{i0}) / k_B T \right]}{1 + \exp \left[ (\mu_D - E_{i0}) / k_B T \right]} \right\} \]
IV Characteristics of Ballistic SiNW FET

Small temperature dependency
35$\mu$A/wire for 4 quantum channels
Model of Carrier Scattering

Linear Potential Approx.  : Electric Field  \( E \)

Transmission Probability to Drain

\[
T(\varepsilon) = \frac{F(0) - G(0)}{F(0)}
\]

Injection from Drain = 0
Résumé of the Compact Model

\[ I = \frac{q}{\pi \hbar} \sum_i g_i \int [f(\varepsilon, \mu_s) - f(\varepsilon, \mu_D)] T_i d\varepsilon \]

\[ (V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{Q_f + Q_b}{C_G} \]

\[ \mu_S - \mu_D = qV_D \]

\[ C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left( \frac{\sqrt{2r + t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r + t_{ox}} - \sqrt{t_{ox}}} \right)} \]

\[ C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left( \frac{r + t_{ax}}{r} \right)} \]

\[ |Q_f + Q_b| = \frac{q}{\pi} \sum_i g_i \left[ \int_{-\infty}^{0} \frac{dk}{1 + \exp \left\{ \frac{\varepsilon_i(k) - \mu_S}{k_B T} \right\}} - \int_{-\infty}^{0} \frac{1}{1 + \exp \left\{ \frac{\varepsilon_i(k) - \mu_S}{k_B T} \right\}} - \int_{-\infty}^{0} \frac{1}{1 + \exp \left\{ \frac{\varepsilon_i(k) - \mu_D}{k_B T} \right\}} \right] T_i(\varepsilon_i(k))dk \]

\[ T(\varepsilon) = \frac{\sqrt{2D_0 qE}}{\left( \sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0 B_0} \ln \left( \frac{qEx_0 + \varepsilon}{\varepsilon} \right)} \]

Unknowns are \( I_D, (\mu_S-\mu_0), (\mu_D-\mu_0), (Q_f+Q_b) \)
I-V_D Characteristics (RT)

- Electric current: 20–25 µA
- No saturation at large V_D
SiNW FET Fabrication
SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oxide etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend
  - Standard recipe for gate stack formation
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.
Fabricated SiNW FET
Recent results to be presented by ESSDERC 2010 next week in Sevile

Wire cross-section: 20 nm X 10 nm

On/Off > 10^6, 60uA/wire

Lg=65nm, Tox=3nm
Bench Mark

Our Work
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<tbody>
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<td>NW Size (nm)</td>
<td>Rect.</td>
<td>Rect.</td>
<td>Rect.</td>
<td>Cir.</td>
<td>Cir.</td>
<td>Elliptical</td>
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<td>10x20</td>
<td>10x20</td>
<td>14</td>
<td>10</td>
<td>10</td>
<td>12</td>
<td>13x20</td>
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<tr>
<td>Lg (nm)</td>
<td>65</td>
<td>25</td>
<td>100</td>
<td>30</td>
<td>8</td>
<td>65</td>
<td>35</td>
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<tr>
<td>EOT or Tox (nm)</td>
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<td>1.8</td>
<td>2</td>
<td>4</td>
<td>3</td>
<td>1.5</td>
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<td>1.2</td>
<td>1.0</td>
<td>1.2</td>
<td>1.2</td>
<td>1.0</td>
</tr>
<tr>
<td>Ion(uA) per wire</td>
<td>60.1</td>
<td>102</td>
<td>30.3</td>
<td>26.4</td>
<td>37.4</td>
<td>48.4</td>
<td>43.8</td>
</tr>
<tr>
<td>Ion(uA/um) by dia.</td>
<td>3117</td>
<td>5010</td>
<td>2170</td>
<td>2640</td>
<td>3740</td>
<td>4030</td>
<td>2592</td>
</tr>
<tr>
<td>Ion(uA/um) by cir.</td>
<td>1609</td>
<td>2054</td>
<td>430</td>
<td>841</td>
<td>1191</td>
<td>1283</td>
<td>825</td>
</tr>
<tr>
<td>SS (mV/dec.)</td>
<td>70</td>
<td>79</td>
<td>68</td>
<td>71</td>
<td>75</td>
<td>~75</td>
<td>85</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>62</td>
<td>56</td>
<td>15</td>
<td>13</td>
<td>22</td>
<td>40-82</td>
<td>65</td>
</tr>
<tr>
<td>Ion/Ioff</td>
<td>~1E6</td>
<td>&gt;1E6</td>
<td>&gt;1E5</td>
<td>~1E6</td>
<td>&gt;1E7</td>
<td>&gt;1E7</td>
<td>~2E5</td>
</tr>
</tbody>
</table>

Ref[11] by Stmicro Lg=25nm, Tox=1.8nm
This work Lg=65nm, Tox=3nm
\( I_{ON}/I_{OFF} \) Benchmark

![Graph showing \( I_{ON}/I_{OFF} \) benchmarks](image)

**Planer FET**
- S. Kamiyama, IEDM 2009, p. 431
- P. Packan, IEDM 2009, p. 659

**Si Nanowire FET**
- Y. Jiang, VLSI 2008, p. 34
- H.-S. Wong, VLSI 2009, p. 92
- S. Bangsaruntip, IEDM 2009, p. 297
- C. Dupre, IEDM 2008, p. 749
- S.D. Suk, IEDM 2005, p. 735
- G. Bidel, VLSI 2009, p. 240

- \( L_g = 500 \sim 65 \text{nm} \)
- \( V_{gs} = 1.0 \sim 1.1 \text{V} \)
- \( V_{gs} = 1.2 \sim 1.3 \text{V} \)
The graph shows the effective electron mobility ($\mu_{\text{eff}}$) as a function of inversion carrier density ($n_i$) for different samples.

- **A$_1$ (12x19)**: $h_{\text{NW}} \times w_{\text{NW}} = (12 \times 19) \text{ nm}^2$
  - $h_{\text{NW}} = 12 \text{ nm}$
  - $w_{\text{NW}} = 19 \text{ nm}$

- **A$_2$ (12x28)**: $h_{\text{NW}} \times w_{\text{NW}} = (12 \times 28) \text{ nm}^2$
  - $h_{\text{NW}} = 12 \text{ nm}$
  - $w_{\text{NW}} = 28 \text{ nm}$

- **B (20x10)**: $h_{\text{NW}} \times w_{\text{NW}} = (20 \times 10) \text{ nm}^2$
  - $h_{\text{NW}} = 20 \text{ nm}$
  - $w_{\text{NW}} = 10 \text{ nm}$

The samples are n-type SOI (Silicon on Insulator) planar devices with $T_{\text{SOI}} = 28 \text{ nm}$.

The effective mobility is plotted on the y-axis, with units of cm$^2$/V's, and the inversion carrier density is shown on the x-axis, with units of cm$^{-2}$. The data points are indicated with markers, and the curves represent the trend with increasing carrier density.
Electron Density
\((x10^{19} \text{cm}^{-3})\)

Distance from SiNW Surface (nm)

- **Edge portion**
- **Flat portion**

(a) Metal
12 nm
19 nm
\(\text{SiO}_2\)
44%

(b) Inversion areal ratio: 29%
12 nm
39 nm

\(V_g = 1\text{V}\)
Primitive estimation!

- SiNW (12nm - 19nm)
- Small EOT for high-k (33)
- P-MOS improvement (26)
- Low S/D resistance (20)
- # of wires /1µm (15)
- Compact model (11)
- Assumption
  \[ I_{ON} \propto L_g^{-0.5} T_{ox}^{-1} \]

Year

I\textsubscript{ON} (µA/µm)
Our roadmap for R & D

Source: H. Iwai, IWJT 2008

Current Issues

Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Thank you for your attention!