Past and Future of Mirco/Nano-Electronic Devices

April 7, 2011

National Workshop on Electronic Devices

@Mizoram University
Aizawl, Mizoram, India

Hiroshi Iwai,
Tokyo Institute of Technology

Tokyo Institute of Technology

Founded in 1881, Promoted to Univ. 1929

Institute Overview

Einstein Visit

Established in 1881→ 130th anniversary in 2011

3 undergraduate schools

School of Science, School of Engineering, School of Bioscience and Biotechnology

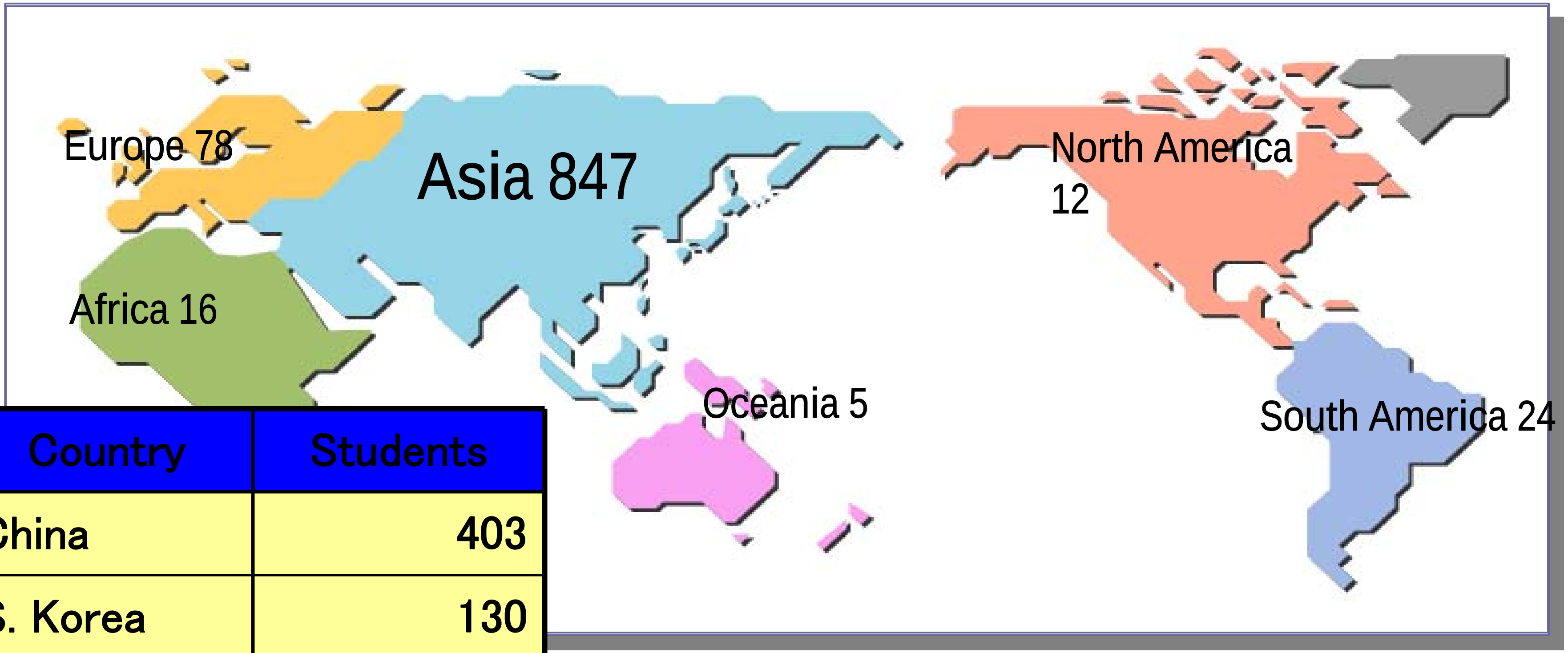
7 graduate schools

Science and Engineering Science, Science and Engineering Technology, Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering, Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

	Undergraduate	Graduate	Master's	Doctoral	Teaching Staff	Student/Instructor	Staff
Tokyo Inst.	**5,000**	**5,000**	**3,500**	**1,500**	**1,200**	**8.3**	**550**
Per Year	**1,200**		**1,800**	**500**			

International Students



Country	Students
China	403
S. Korea	130
Indonesia	64
Thailand	55
Vietnam	60
Malaysia	28

Total 982

(As of May. 1, 2005)

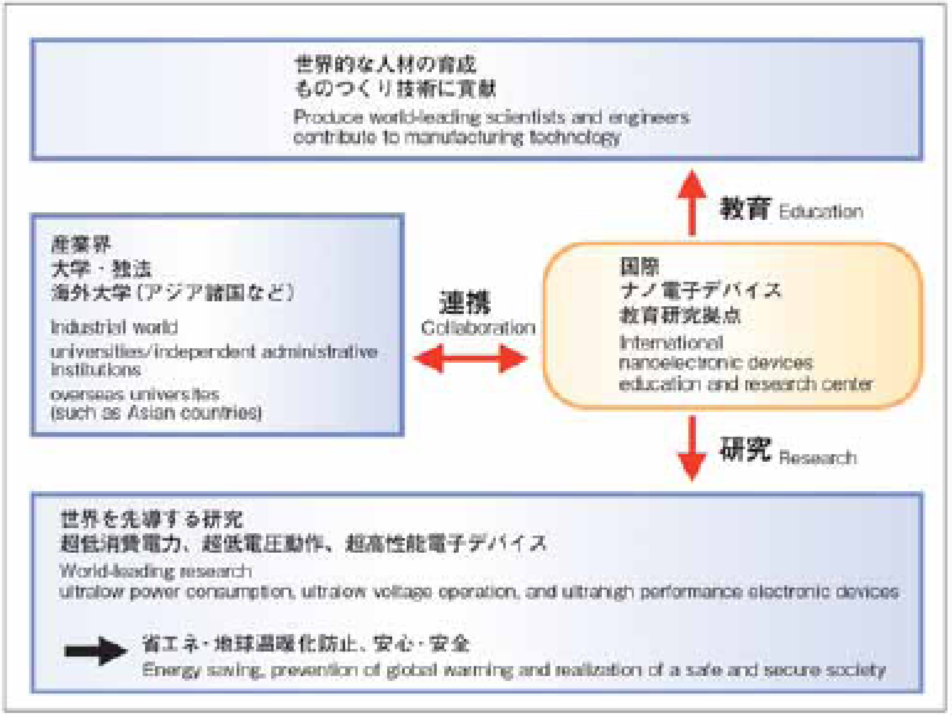
東京工業大学大学院
総合理工学研究科

複合創造領域
Innovative Platform for
Education and Research

先端ナノエレクトロニクス研究コアユニット研究室メンバー

Nanoelectronics Research Frontier Core Unit

（2010年10月1日現在）



世界的な人材の育成
ものつくり技術に貢献

Produce world-leading scientists and engineers
contribute to manufacturing technology

教育 Education

産業界
大学・独法
海外大学（アジア諸国など）

Industrial world
universities/independent administrative institutions
overseas universities
(such as Asian countries)

連携
Collaboration

国際
ナノ電子デバイス
教育研究拠点

International
nanoelectronic devices
education and research center

研究 Research

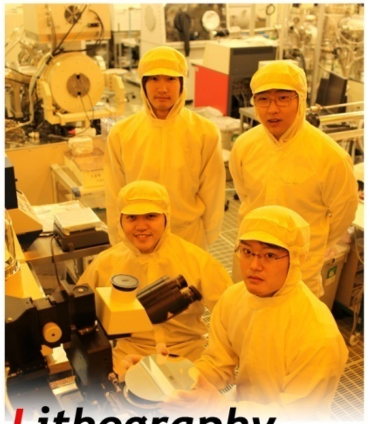
世界を先導する研究
超低消費電力、超低電圧動作、超高性能電子デバイス

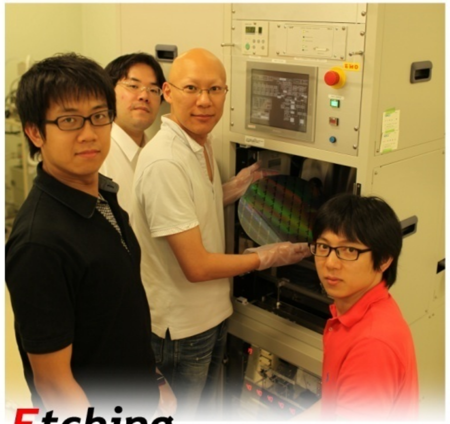
World-leading research
ultralow power consumption, ultralow voltage operation, and ultrahigh performance electronic devices

→ 省エネ・地球温暖化防止、安心・安全
Energy saving, prevention of global warming and realization of a safe and secure society

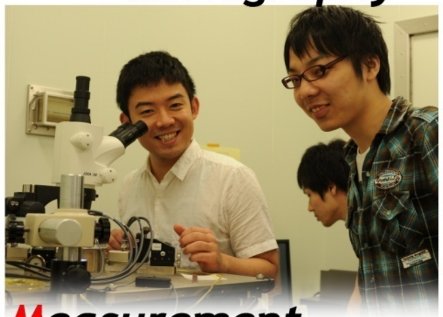
研究風景

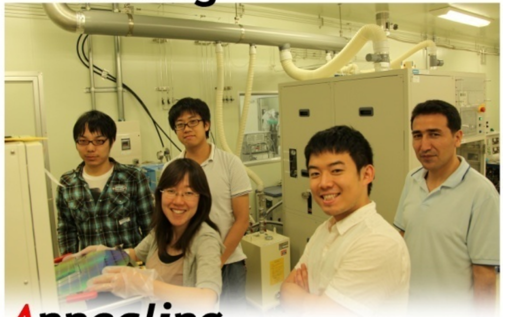

Deposition


Lithography


Etching


Analysis

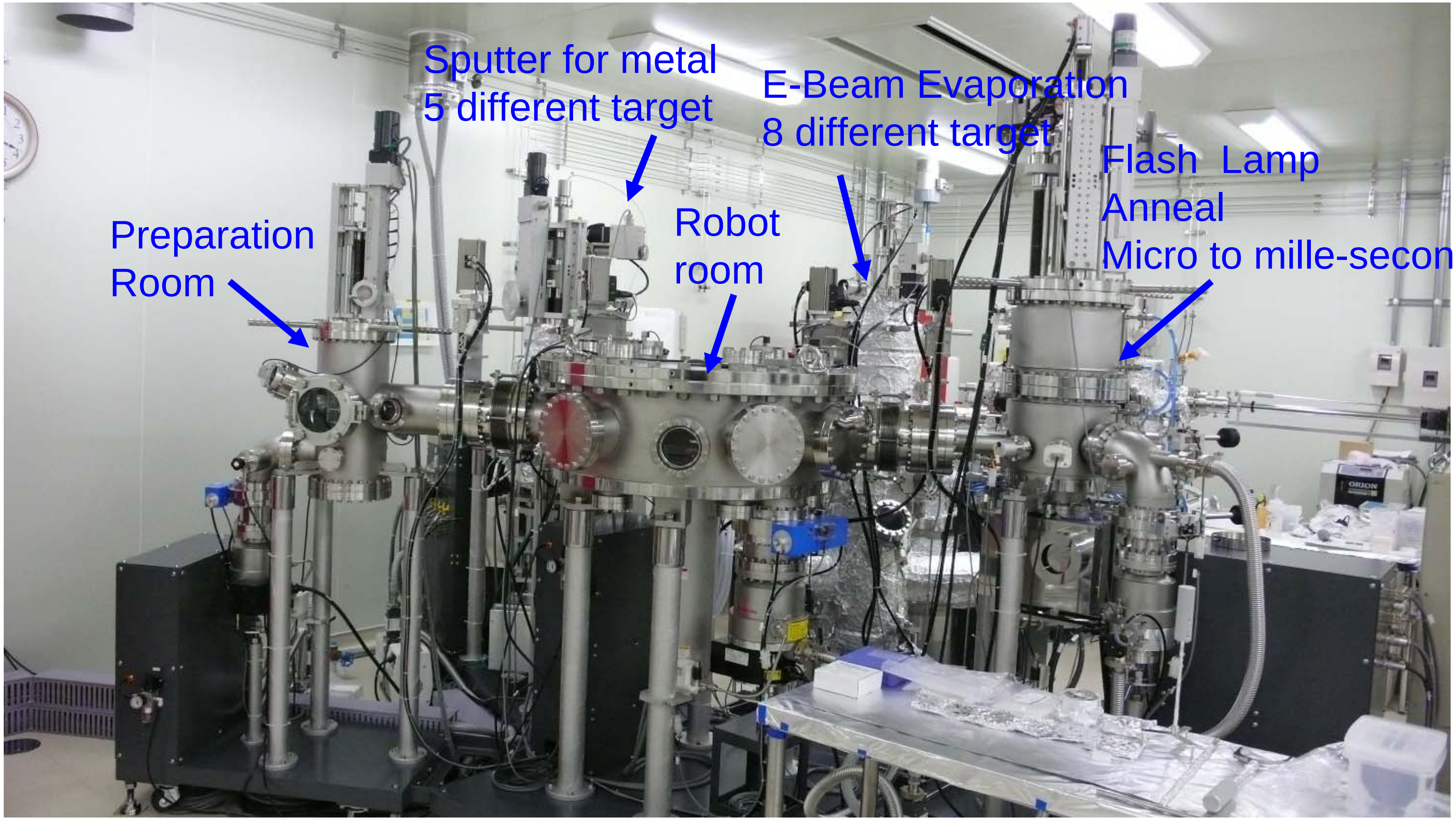

Measurement


Annealing


Office

Si MOSFET
IWAI LAB.®

Cluster tool for high-k thin film deposition



- There were many inventions in the 20th century:

  Airplane, Nuclear Power generation, Computer,

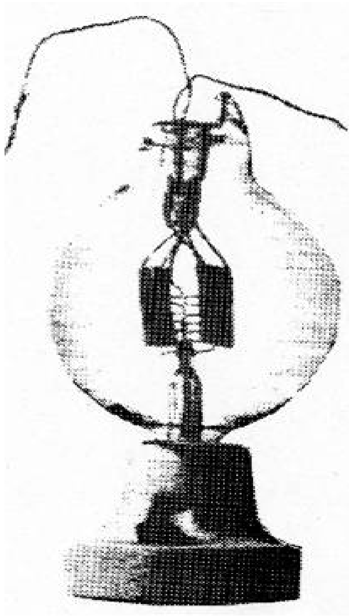
  Space aircraft, etc
- However, everything has to be controlled by electronics
- Electronics

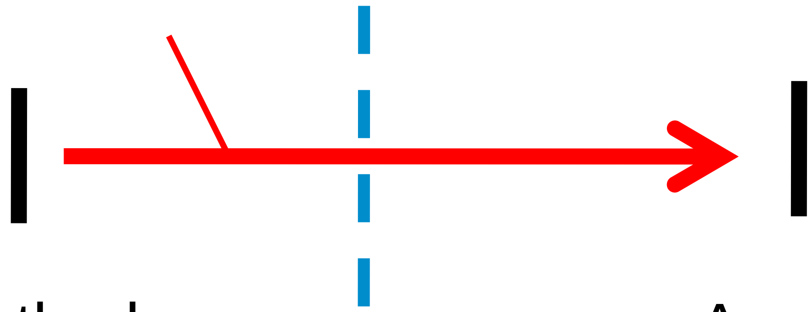
  Most important invention in the 20th century
- What is Electronics: To use electrons,

  Electronic Circuits

Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Lee De Forest





Thermal electrons from cathode
controlled by grid bias

Cathode
(heated)

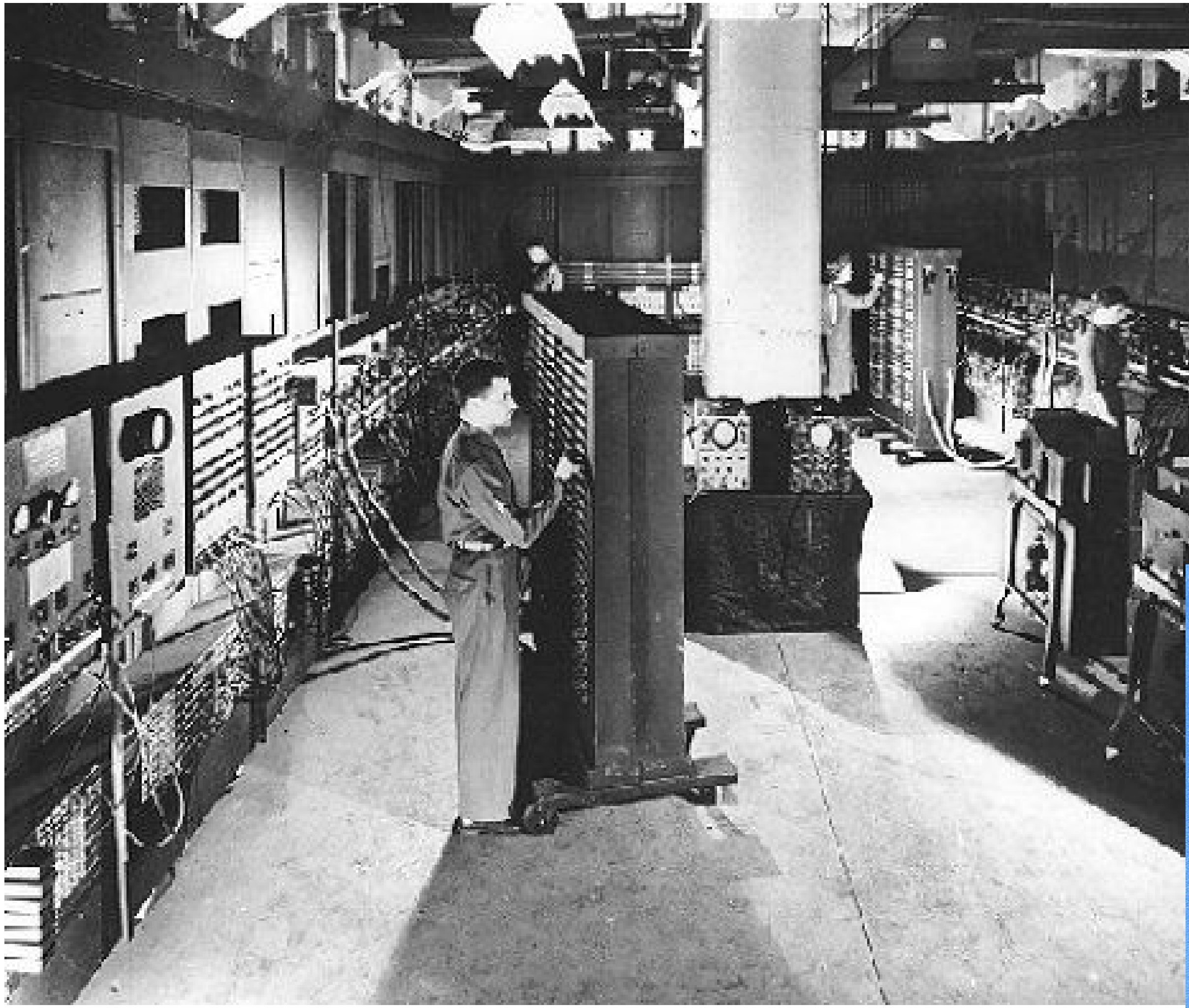
Grid

Anode
(Positive bias)

Same mechanism as that of transistor

First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

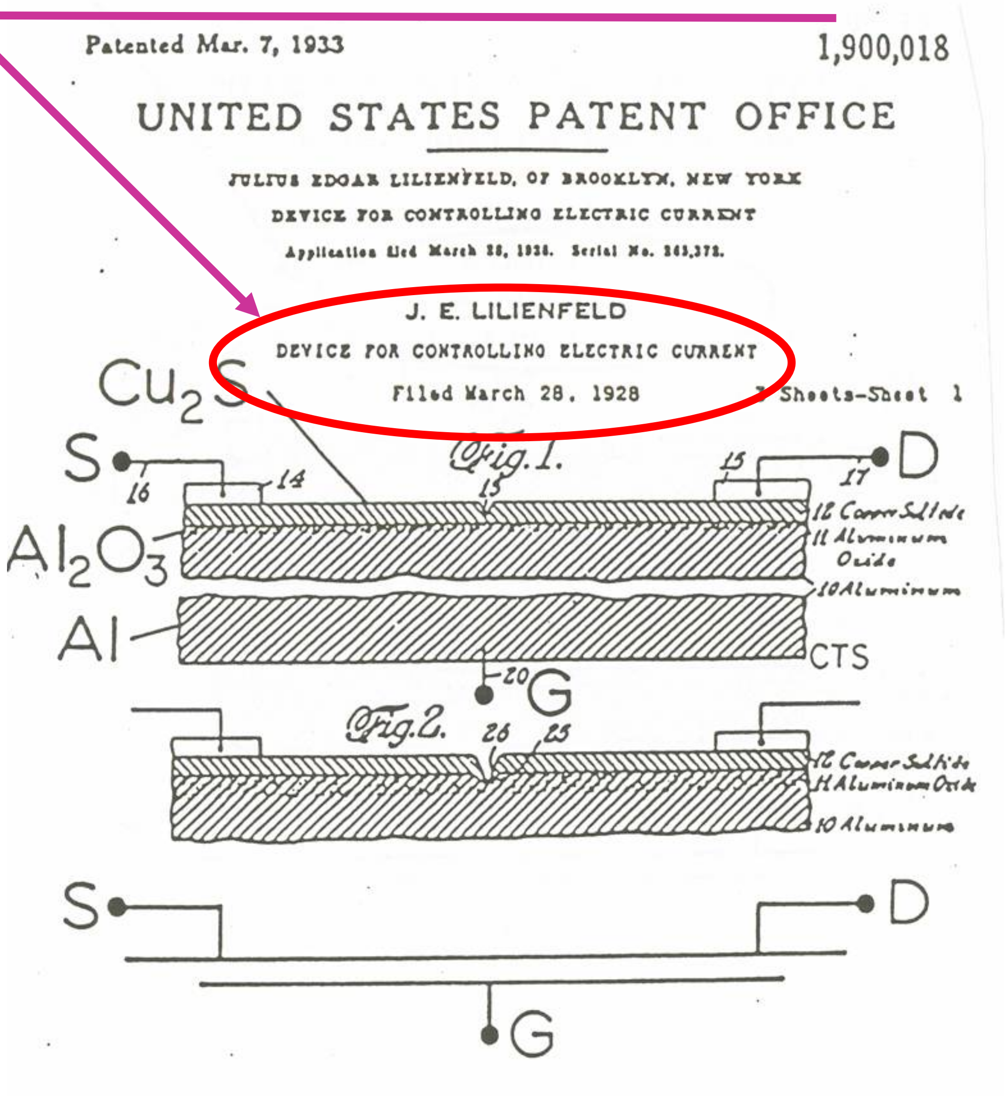


Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928



Patented Mar. 7, 1933 1,900,018

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Application filed March 28, 1928. Serial No. 265,372.

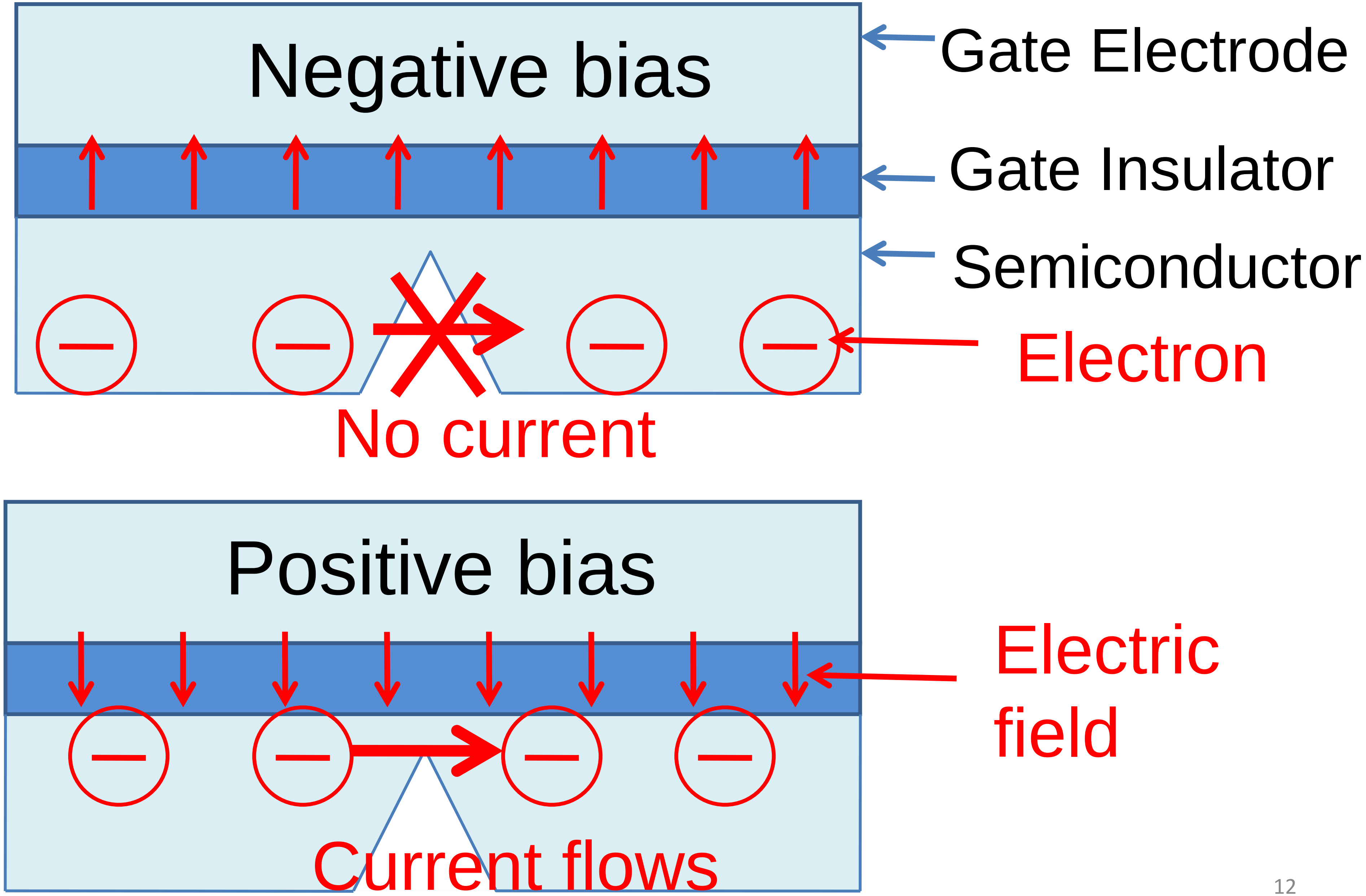
J. E. LILIENFELD

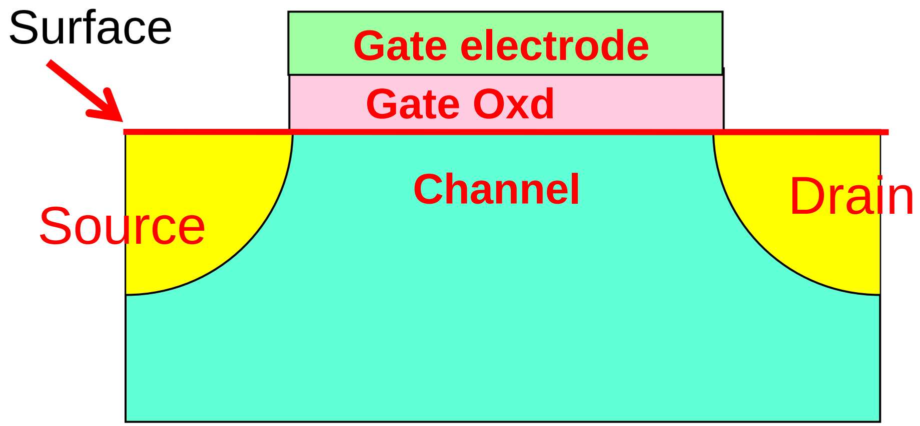
DEVICE FOR CONTROLLING ELECTRIC CURRENT

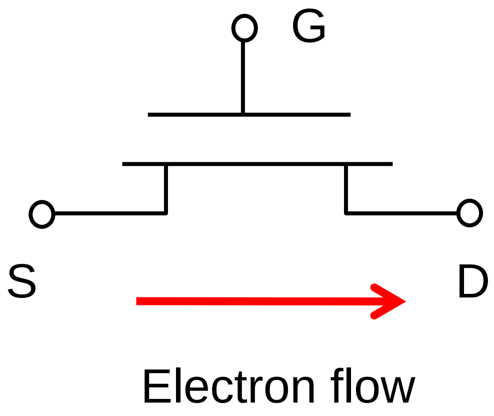
Filed March 28, 1928 3 Sheets-Sheet 1

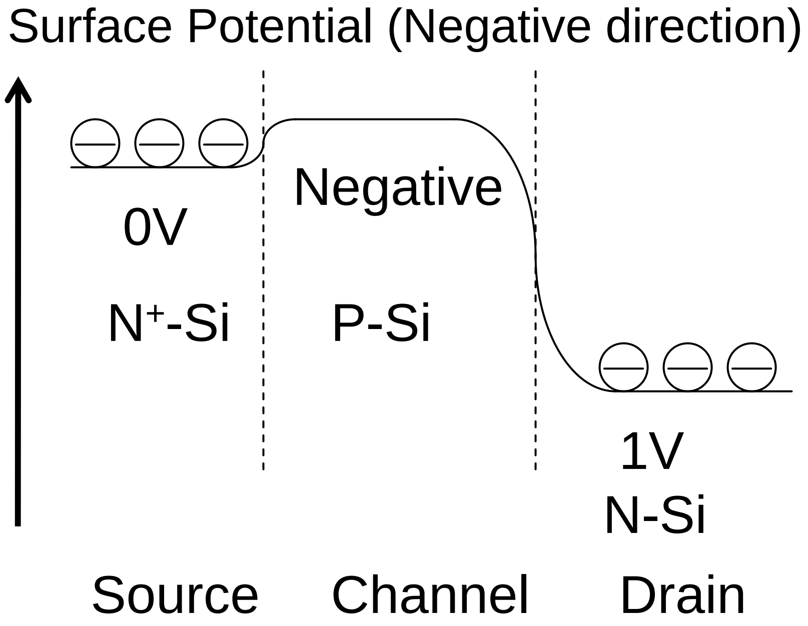
J.E.LILIENFELD

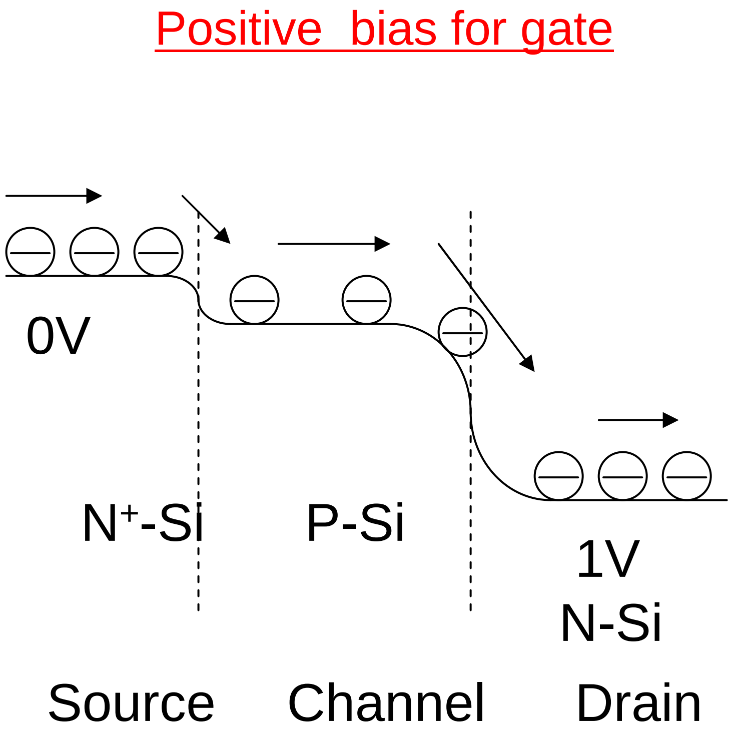
Capacitor structure with notch




Surface
Gate electrode
Gate Oxd
Channel
Source
Drain


G
S
D
Electron flow


0 bias for gate
Surface Potential (Negative direction)
Negative
0V
N^+-Si
P-Si
1V
N-Si
Source
Channel
Drain

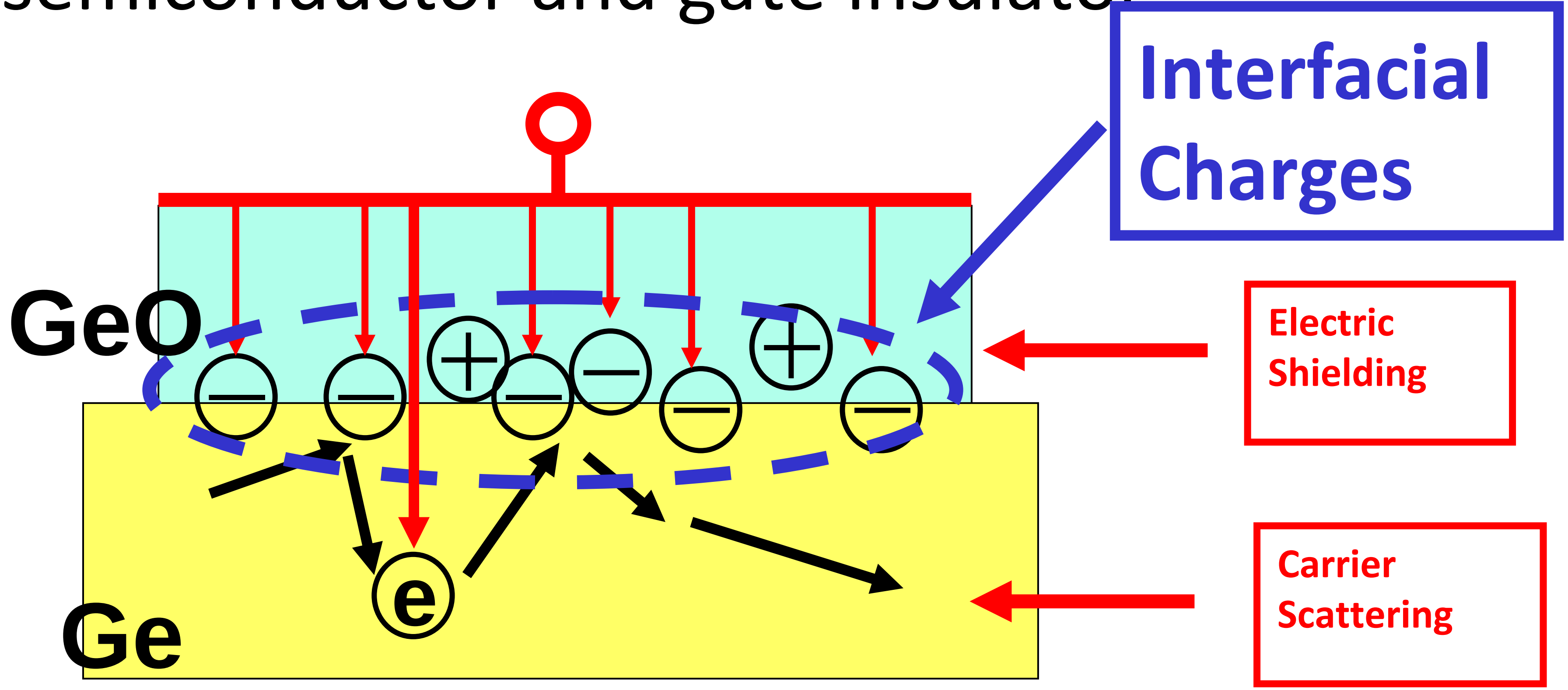

Positive bias for gate
0V
N^+-Si
P-Si
1V
N-Si
Source
Channel
Drain

However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!

Very bad interface property between the semiconductor and gate insulator



Interfacial Charges

Electric Shielding

Carrier Scattering

Drain Current was several orders of magnitude smaller than expected

Even Shockley!

However, they found amplification phenomenon when investigating Ge surface when putting needles.

This is the 1st Transistor:

Not Field Effect Transistor,

But Bipolar Transistor (another mechanism)

1947: 1st transistor

Bipolar using Ge

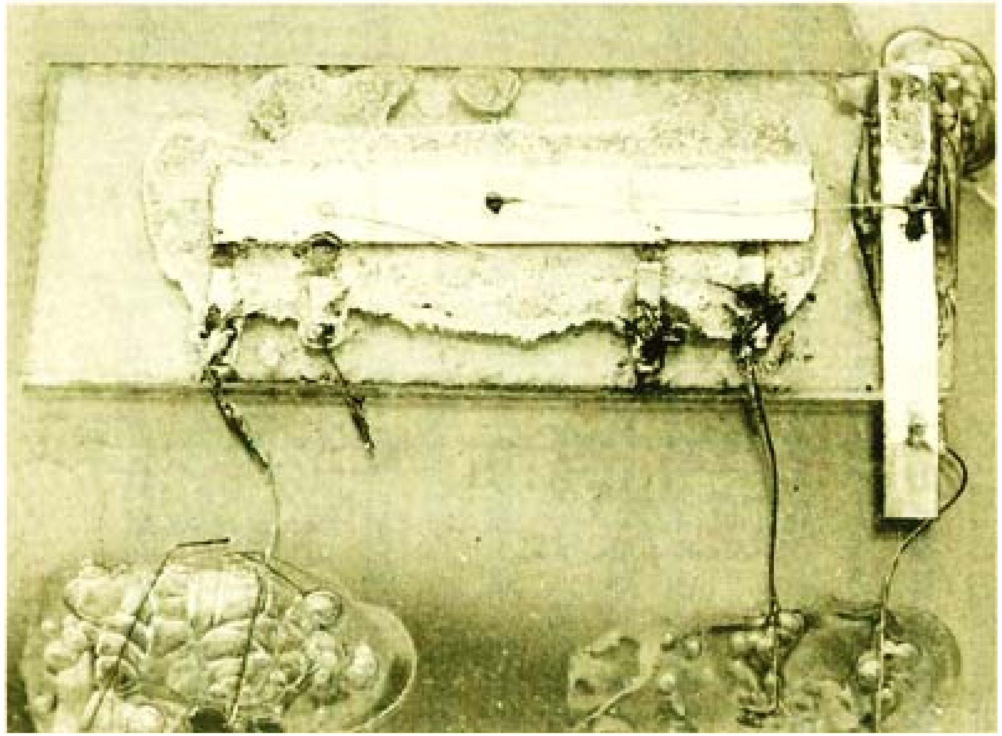
J. Bardeen W. Bratten,

W. Shockley

1958: 1st Integrated Circuit

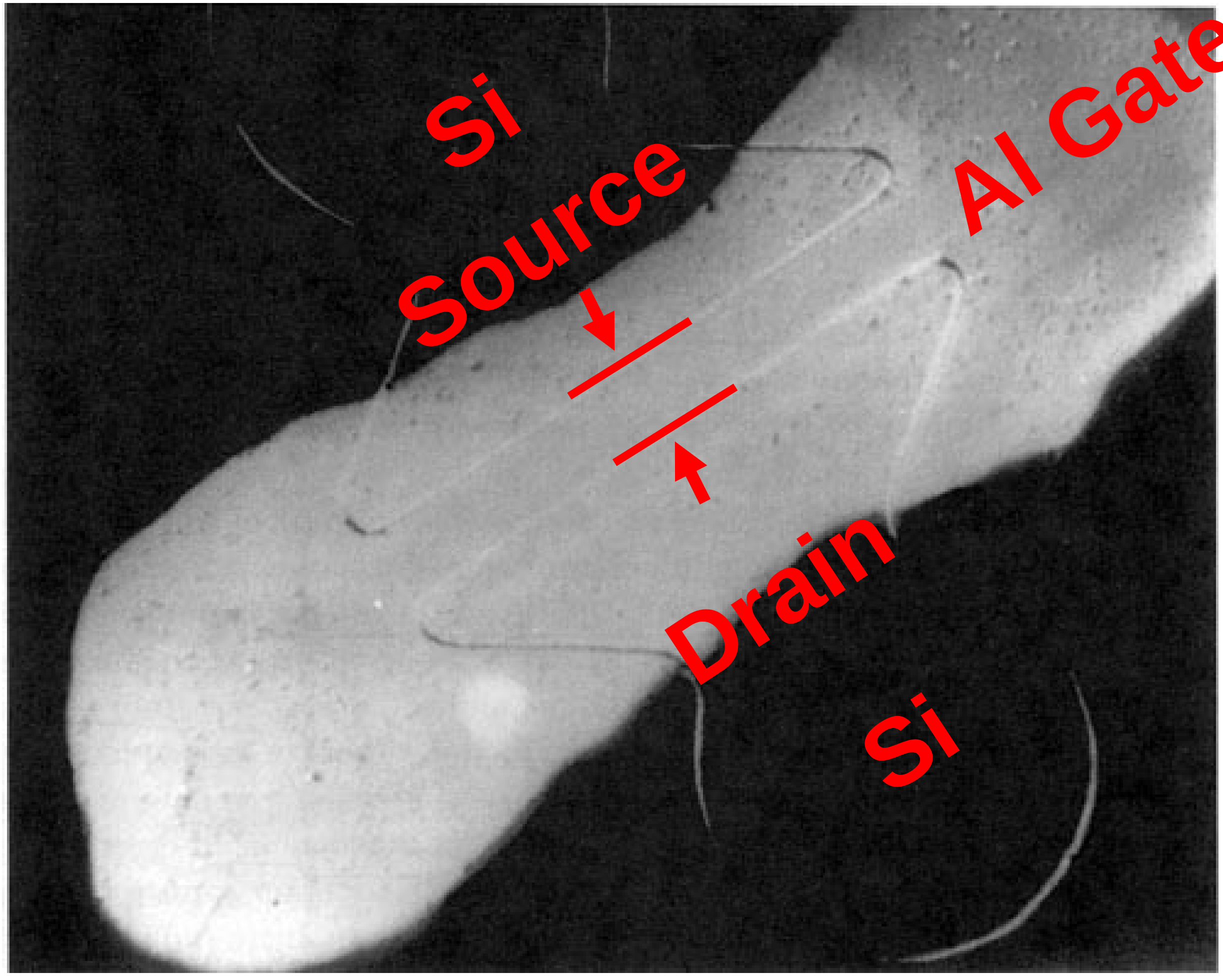
Jack S. Kilby

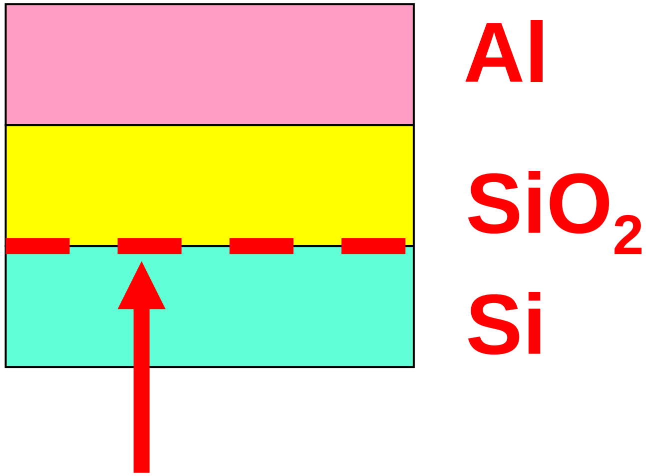
Connect 2 bipolar transistors in the
Same substrate by bonding wire.



1960: First MOSFET
by D. Kahng and M. Atalla

Top View

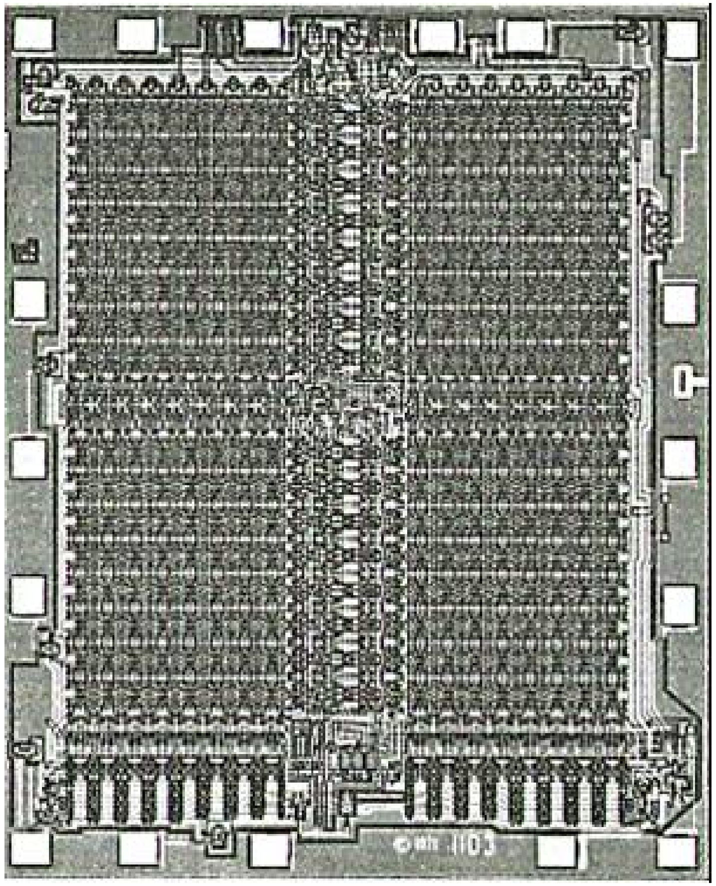




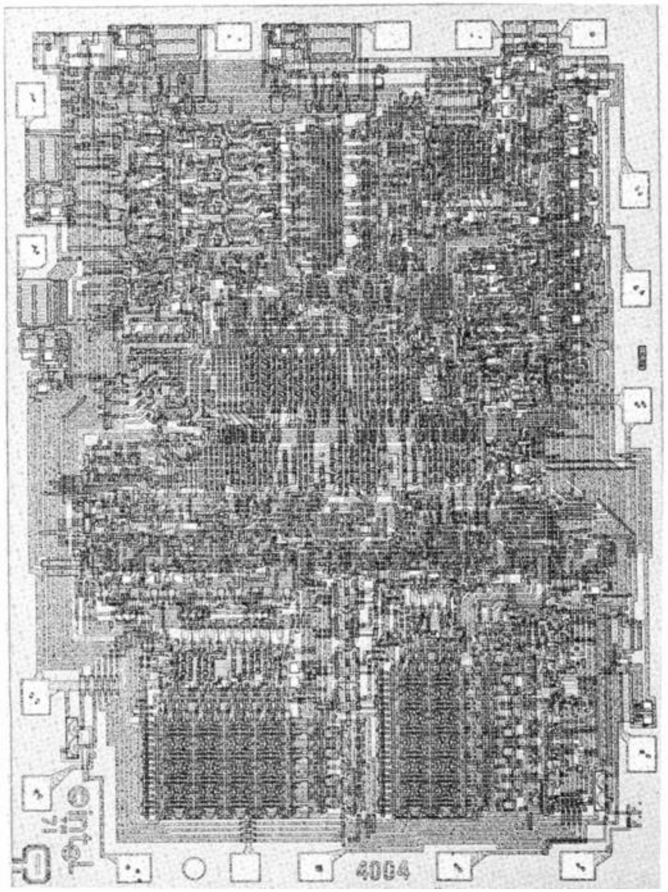
Si/SiO2 Interface is extraordinarily good

1970,71: 1st generation of LSIs

DRAM Intel 1103



MPU Intel 4004



MOS LSI experienced continuous progress for many years

	Name of Integrated Circuits	Number of Transistors
1960s	IC (Integrated Circuits)	~ 10
1970s	LSI (Large Scale Integrated Circuit)	~1,000
1980s	VLSI (Very Large Scale IC)	~10,000
1990s	ULSI (Ultra Large Scale IC)	~1,000,000
2000s	?LSI (? Large Scale IC)	~1000,000,000

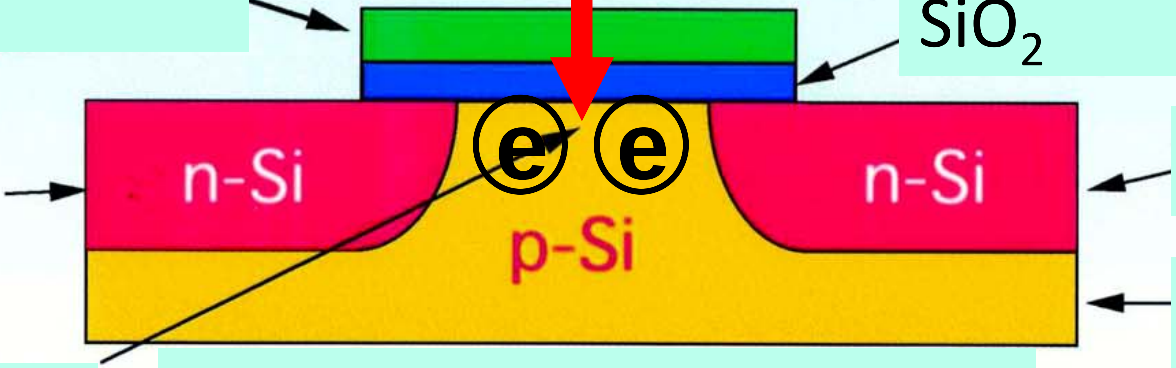
Gate Electrode
Poly Si

Gate Insulator
SiO_2

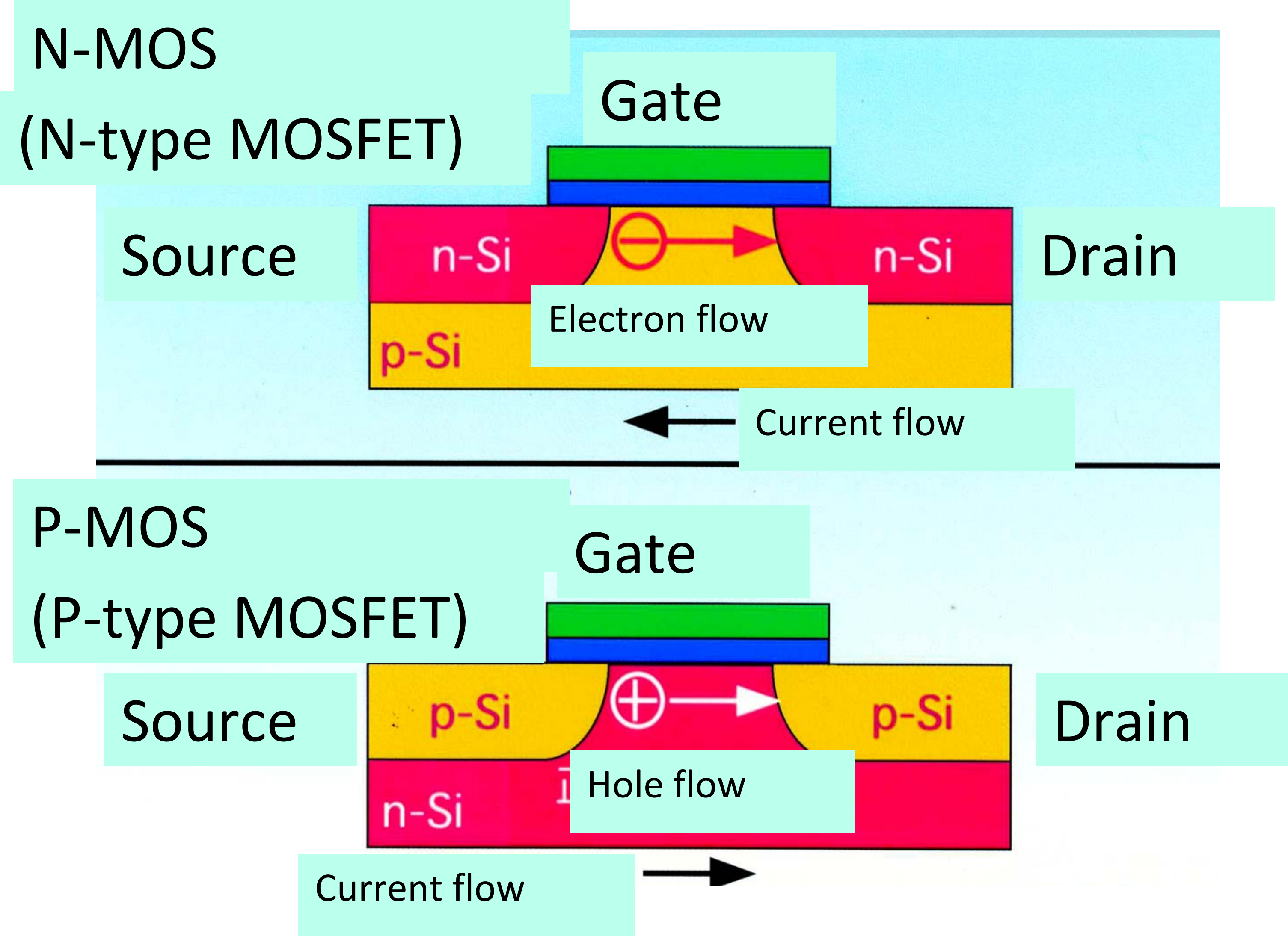
Substrate
Si

MOSFET: Metal Oxide Semiconductor
Field Effect Transistor

Use Gate Field Effect for switching



N-MOS (N-type MOSFET)



N-MOS

(N-type MOSFET)

Gate

Source

Drain

Electron flow

Current flow

P-MOS

(P-type MOSFET)

Gate

Source

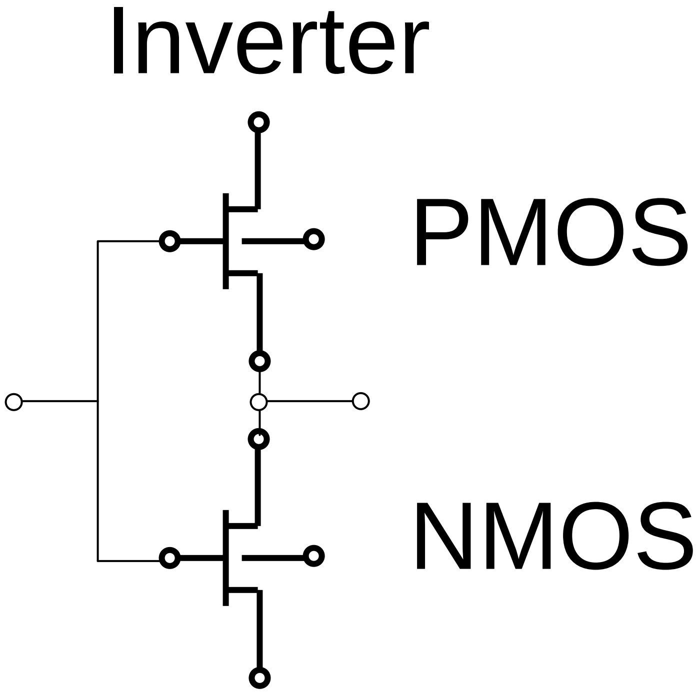
Drain

Hole flow

Current flow

CMOS

Complimentary MOS



When NMOS is ON, PMOS is OFF

When PMOS is ON, NMOS is OFF

Needless to say, but….

CMOS Technology:

Indispensible for our human society

Al the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:

There is no computer in banks, and

world economical activities immediately stop.

Cellarer phone dose not exists

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

→ **Increase clock frequency**

→ **Increase circuit operation speed**

2. **Increase number of Transistors**

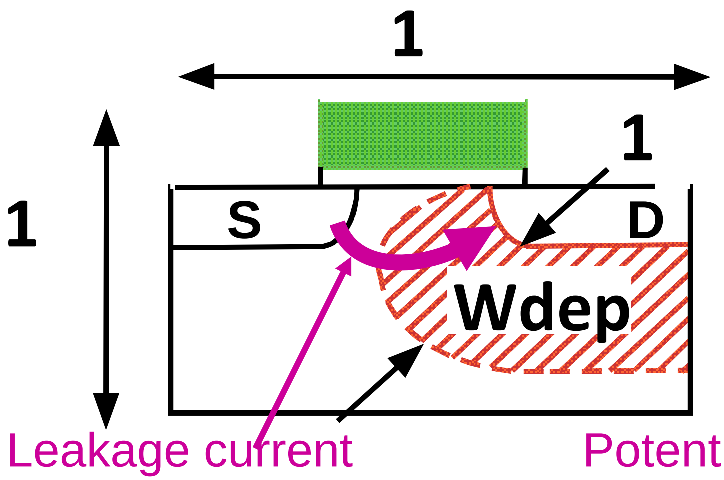
→ **Parallel processing**

→ **Increase circuit operation speed**

Downsizing contribute to the performance increase in double ways

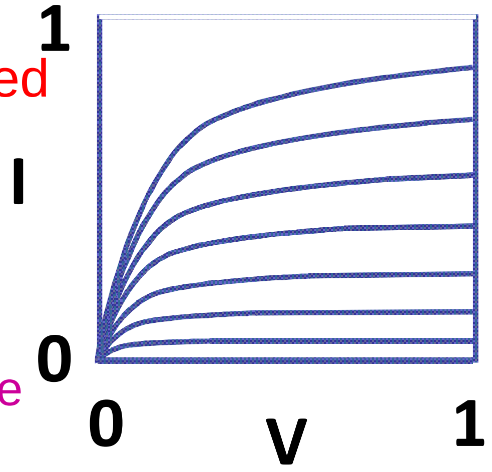
Thus, downsizing of Si devices is the most important and critical issue.

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage
between S and D



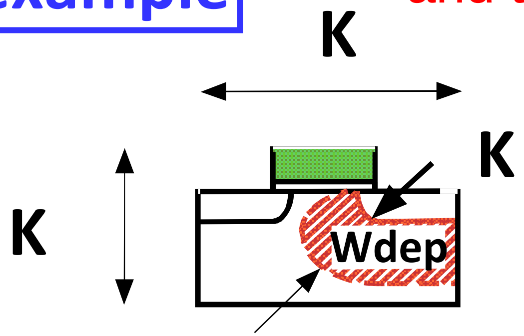
Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

K=0.7 for example

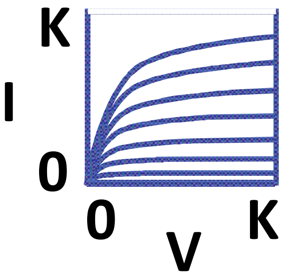
X , Y , Z : K, V : K, Na : 1/K

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



Wdep $\propto \sqrt{V/Na}$
: K



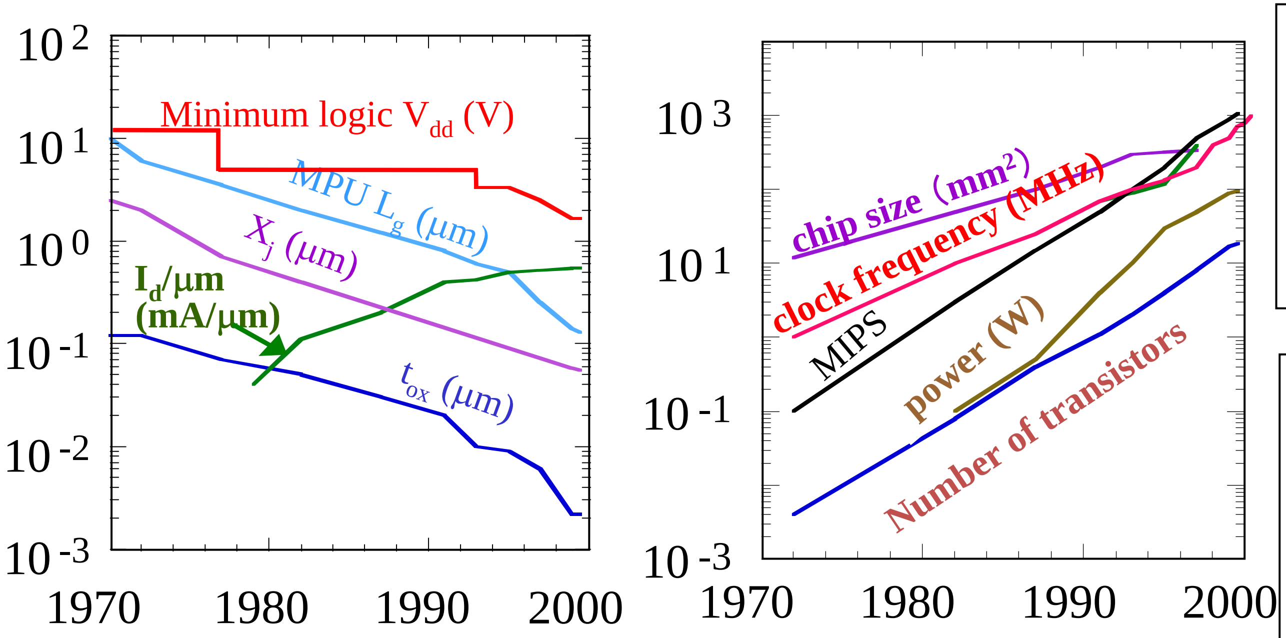
I : K

Downscaling merit: Beautiful!

Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	**Scaling K : K=0.7 for example**
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o: gate C per unit area $\rightarrow W_g (t_{ox}{}^{-1})(V_g - V_{th}) = W_g t_{ox}{}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox} \rightarrow KK/K = K$
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d \rightarrow KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α: Scaling factor → **In the past, $\alpha > 1$ for most cases**
Integration (# of Tr)	N	α/K^2	$N \rightarrow \alpha/K^2$ **$= 1/K^2$, when $\alpha = 1$**
Power per chip	P	α	$fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha$ **$= 1$, when $\alpha = 1$**

k= 0.7 and α =1	k= 0.7^2 =0.5 and α =1
Single MOFET	
Vdd → 0.7	Vdd → 0.5
Lg → 0.7	Lg → 0.5
Id → 0.7	Id → 0.5
Cg → 0.7	Cg → 0.5
P (Power)/Clock → $0.7^3 = 0.34$	P (Power)/Clock → $0.5^3 = 0.125$
τ (Switching time) → 0.7	τ (Switching time) → 0.5
Chip	
N (# of Tr) → $1/0.7^2 = 2$	N (# of Tr) → $1/0.5^2 = 4$
f (Clock) → 1/0.7 = 1.4	f (Clock) → 1/0.5 = 2
P (Power) → 1	P (Power) → 1

Actual past downscaling trend until year 2000



Source. Iwai and S. Ohmi, Microelectronics Reliability 42 (2002), pp.1251-1268

Past 30 years scaling

Merit: N, f increase

Demerit: P increase

V_{dd} scaling insufficient

⇩

Additional significant increase in I_d, f, P

Change in 30 years

	Ideal scaling	Real Change		Ideal scaling	Real Change		Ideal scaling	Real Change
L_g	K	10^{-2}	I_d	K (10^{-2})	10^{-1}	f	$1/K(10^2)$	10^3
t_{ox}	$K(10^{-2})$	10^{-2}						
V_{dd}	$K(10^{-2})$	10^{-1}	I_d/μm	1	10^1	P $= f\alpha NCV^2$	$\alpha(10^1)$	10^5
A_{chip}	α	10^1	N	$\alpha/K^2(10^5)$	10^4			

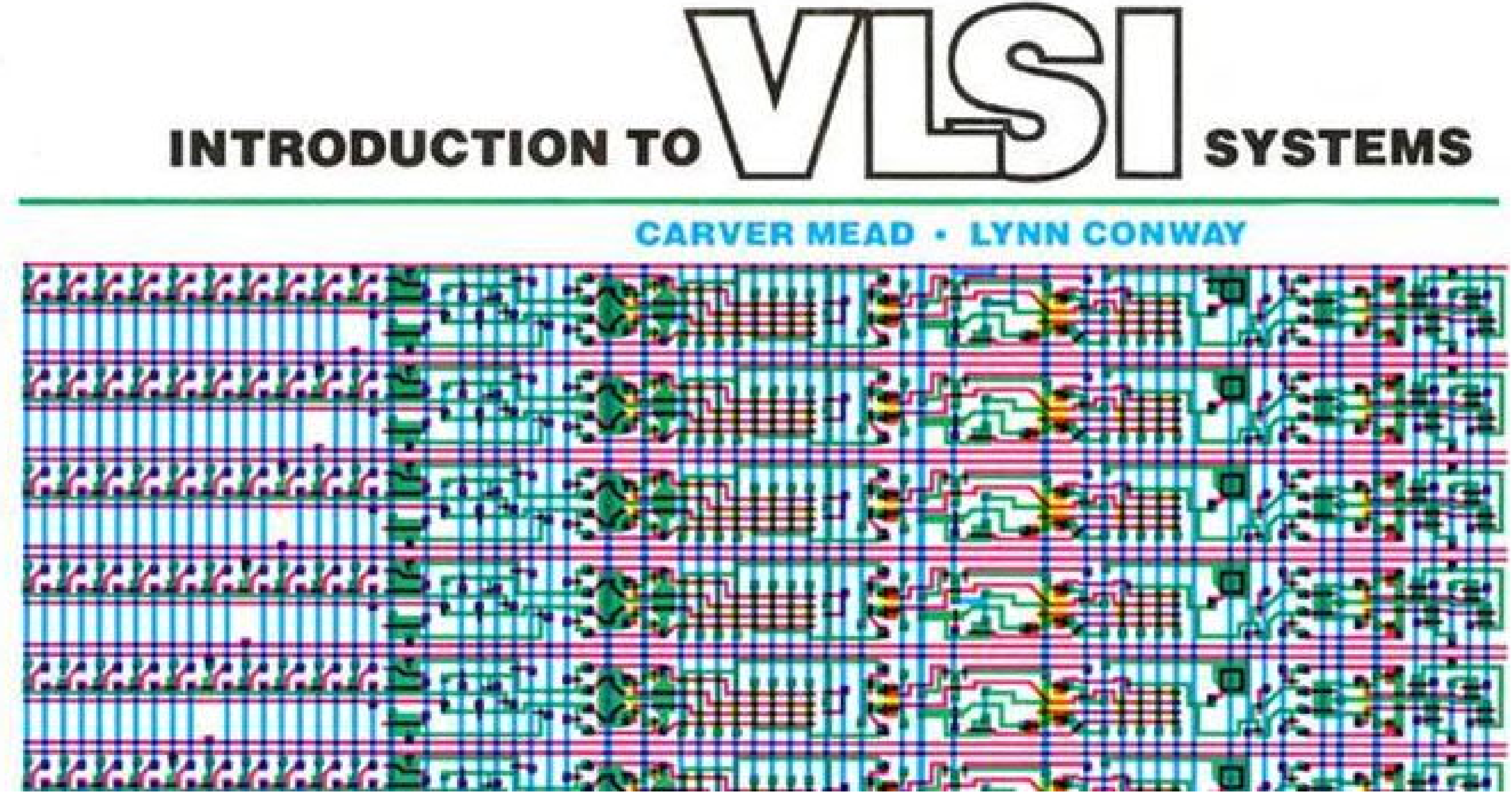
Vd scaling insufficient, α increased ➞ N, Id, f, P increased significantly

Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970’s	1μm:	SCE
Early 1980’s	0.5μm:	S/D resistance
Early 1980’s	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980’s	0.1μm:	‘0.1μm brick wall’(various)
2000	50nm:	‘Red brick wall’ (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.



INTRODUCTION TO VLSI SYSTEMS

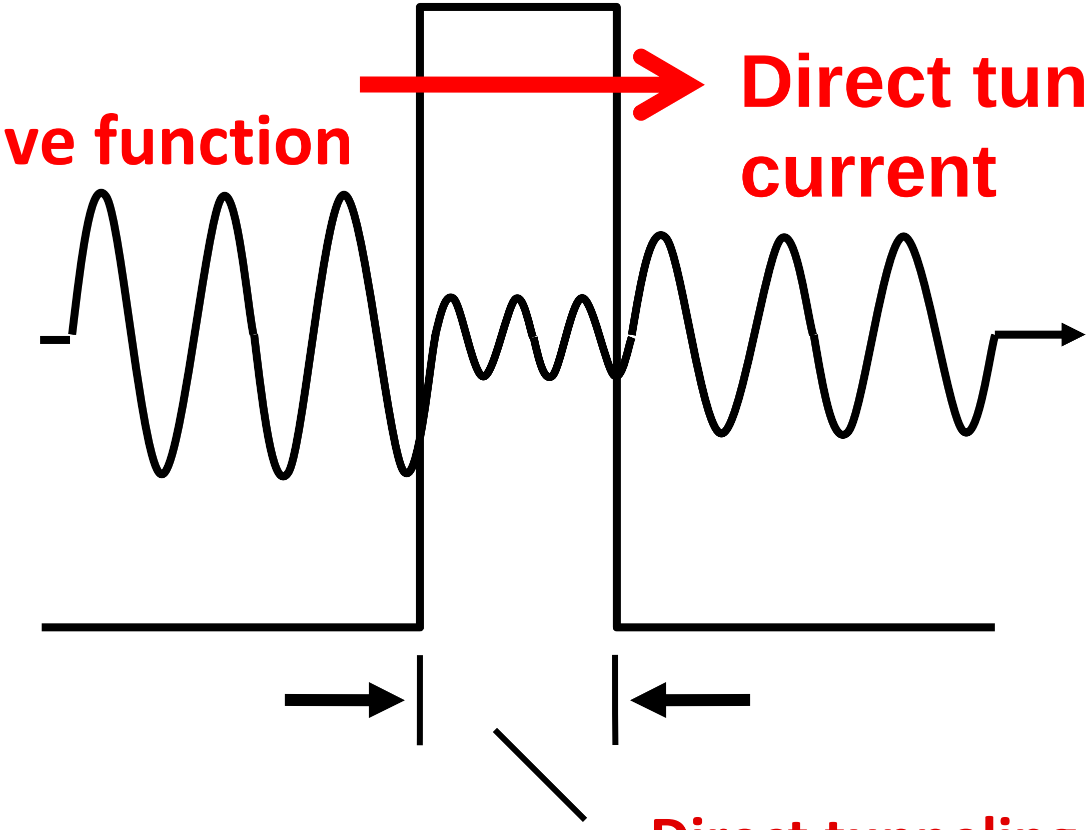
CARVER MEAD • LYNN CONWAY

C. Mead L. Conway

VLSI textbook

Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ….. begin to make the devices of smaller dimension unworkable.

Direct-tunneling effect



Gate Electrode

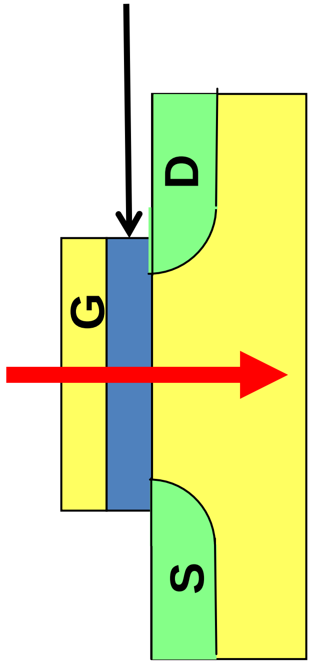
Gate Oxide

Si Substrate

Potential Barrier

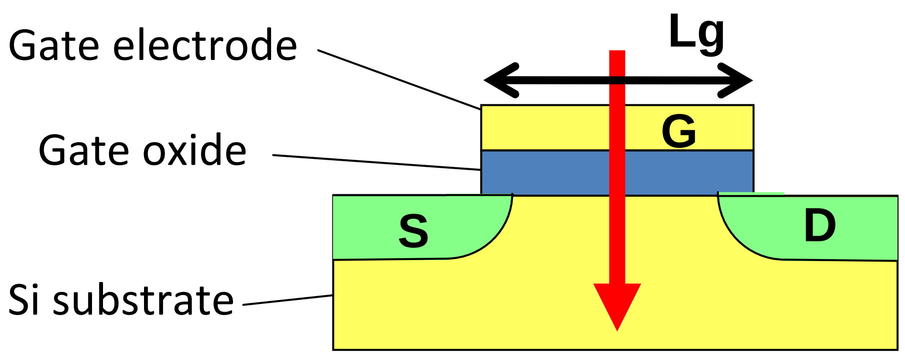
Wave function

Direct tunneling current



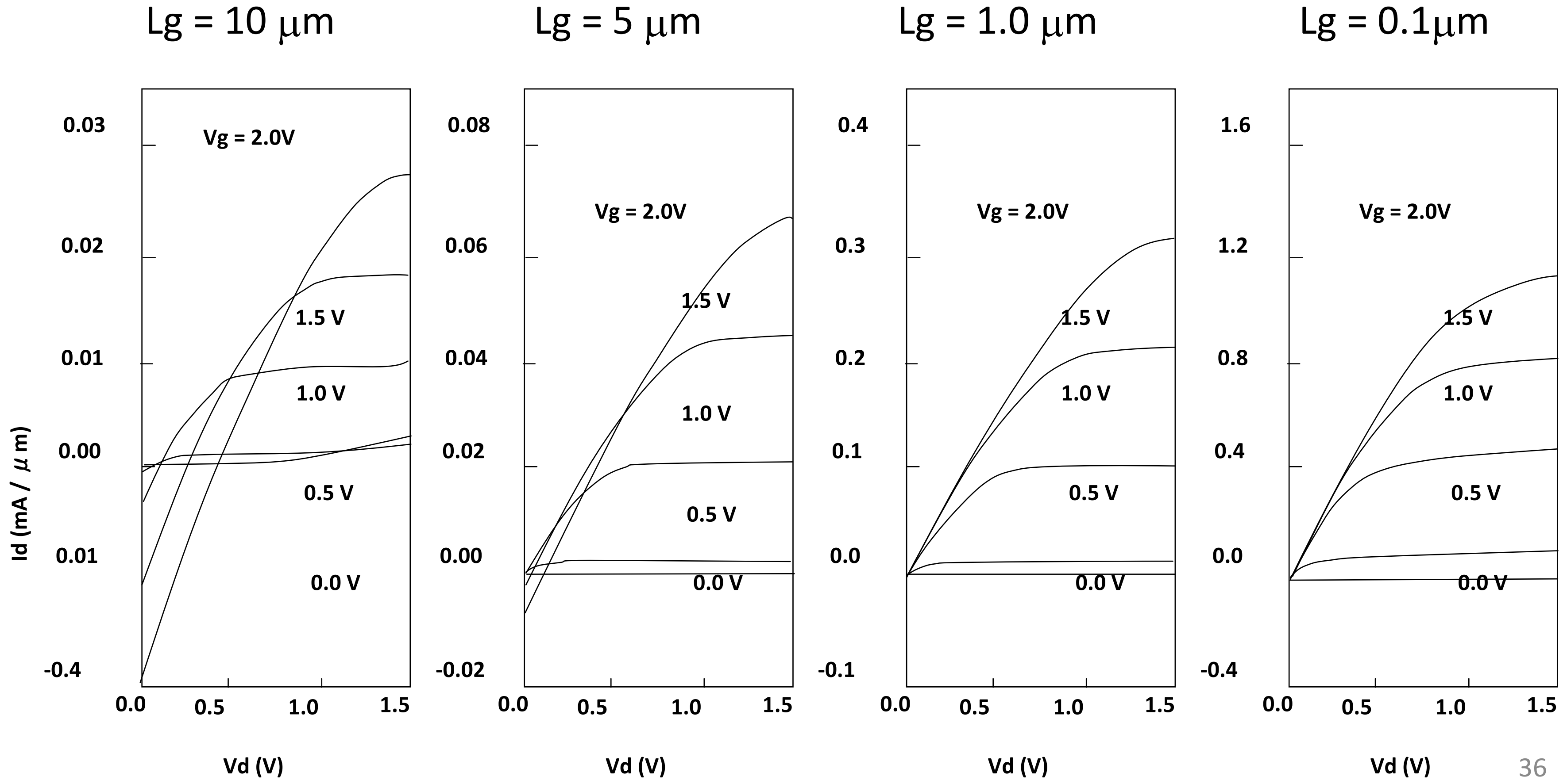
Gate Oxide

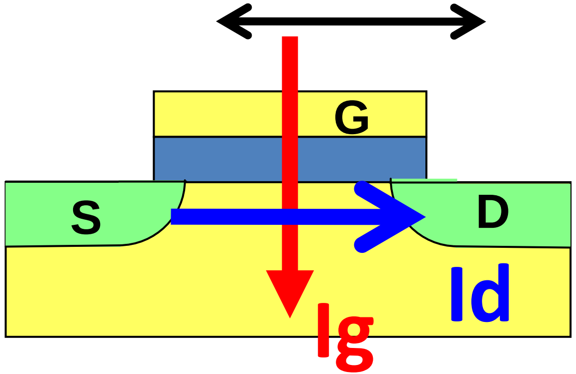
Direct tunneling leakage current start to flow when the thickness is 3 nm.



Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide



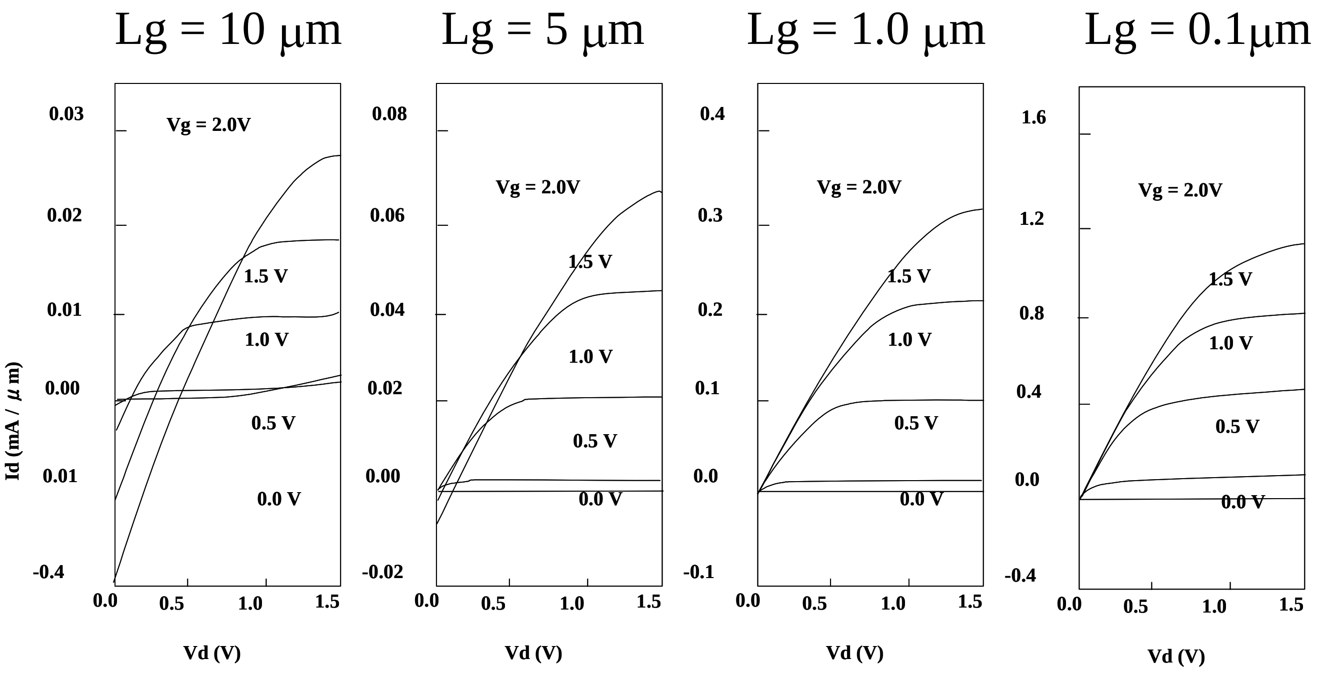


Gate leakage: Ig ∝ Gate Area ∝ Gate length (Lg)

Drain current: Id ∝ 1/Gate length (Lg)

Lg → small,
Then, Ig → small, Id → large, Thus, Ig/Id → very small

Id


Lg = 10 μm

Lg = 5 μm

Lg = 1.0 μm

Lg = 0.1μm

Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!
Some one will think for you

Transistor Scaling Continues

90nm node

Lg=50nm

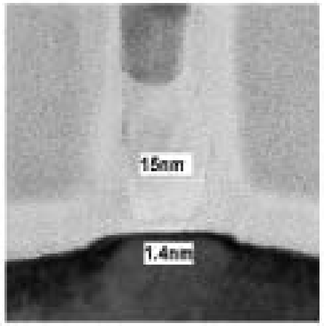
65nm node

Lg=35nm

45nm node

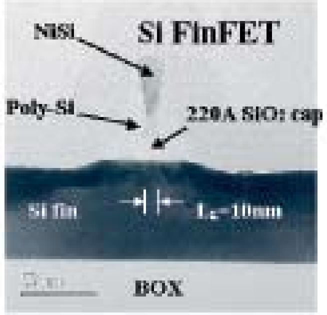
Lg=25nm

32nm node

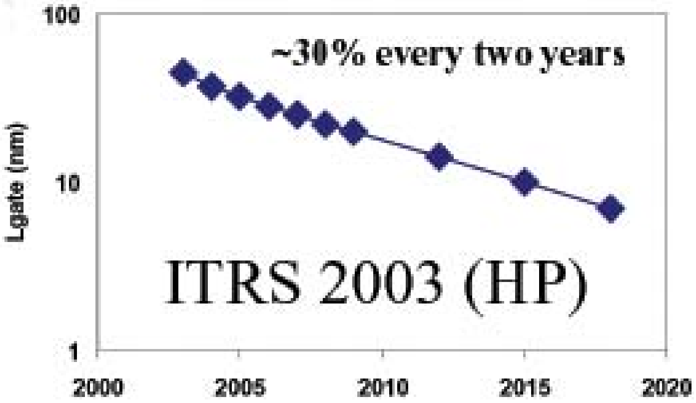


Lg=15nm

22nm node



Lg=10nm

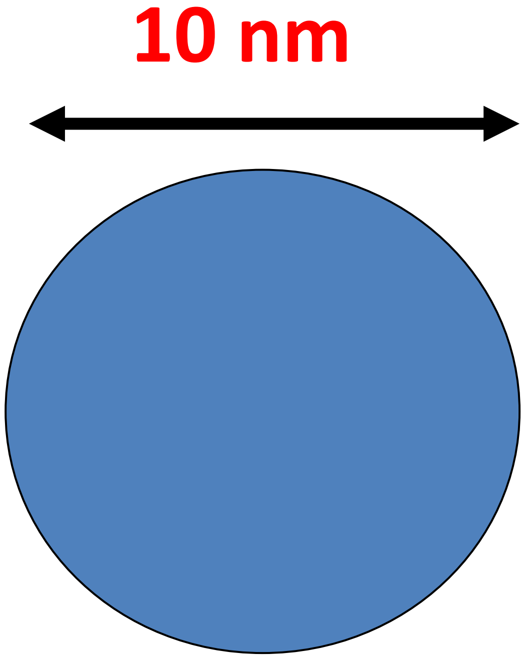


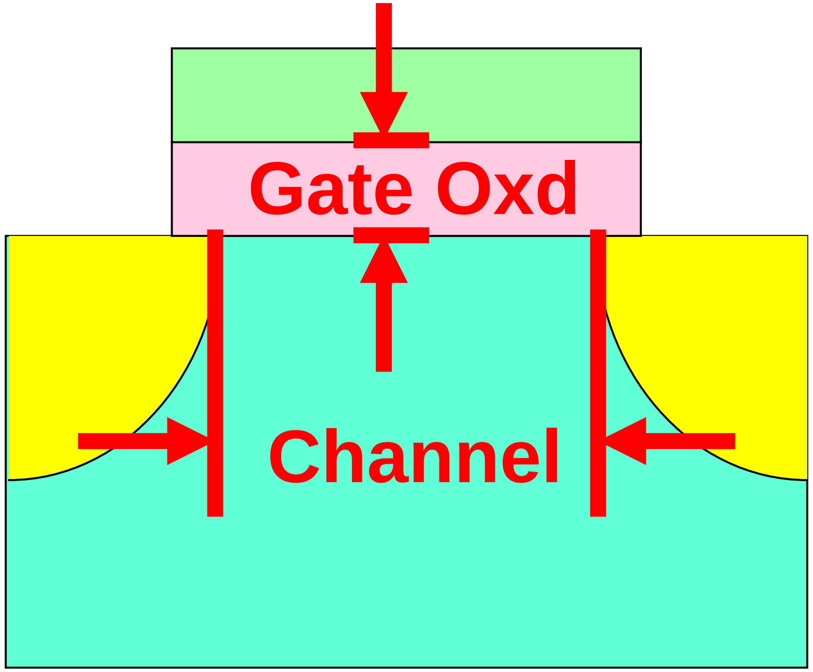
Qi Xinag, ECS 2004, AMD

Downsizing limit?

Channel length?

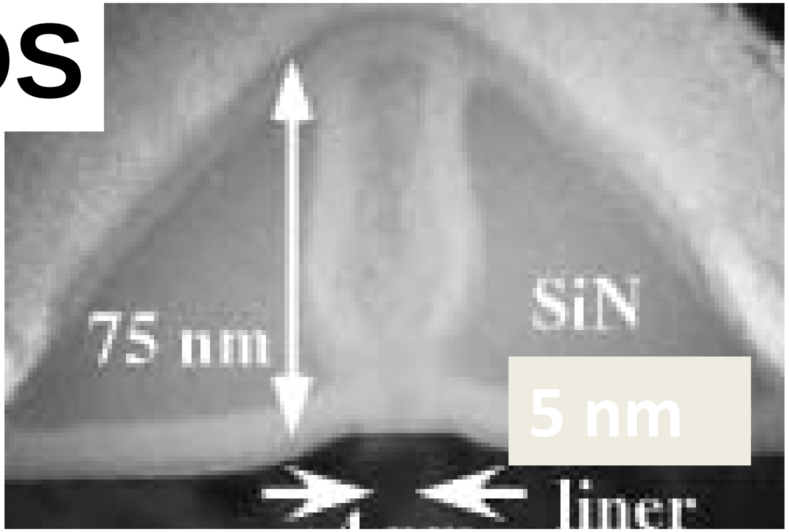
Electron wave length



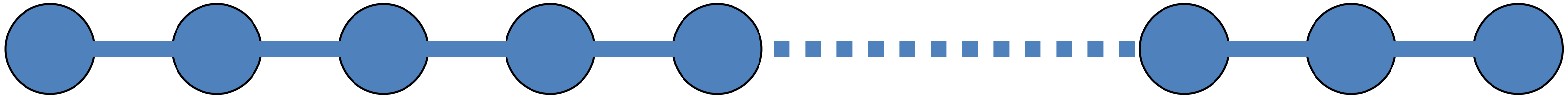


5 nm gate length CMOS

Is a Real Nano Device!!

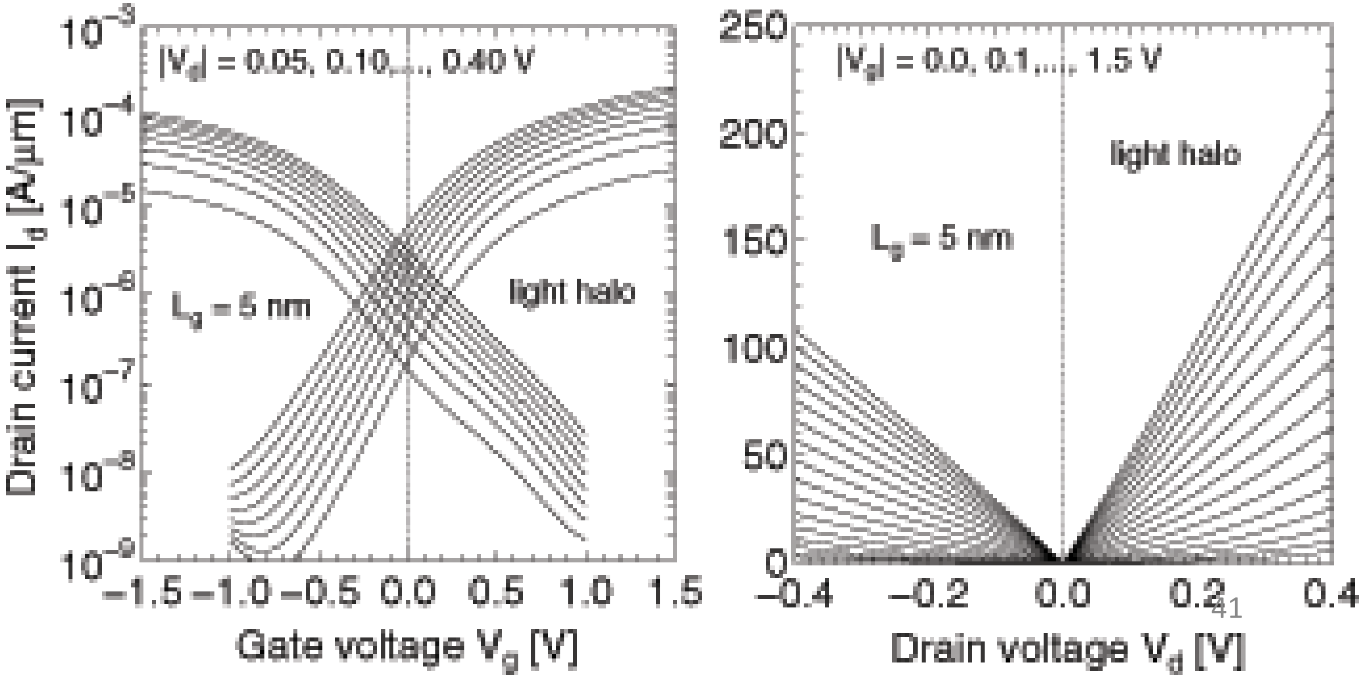


Length of 18 Si atoms



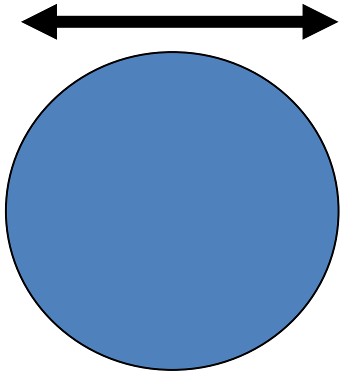
H. Wakabayashi et.al, NEC

IEDM, 2003



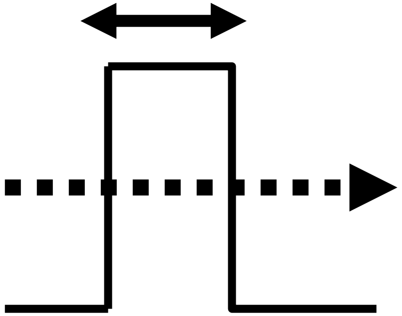
Electron wave length

10 nm



Tunneling distance

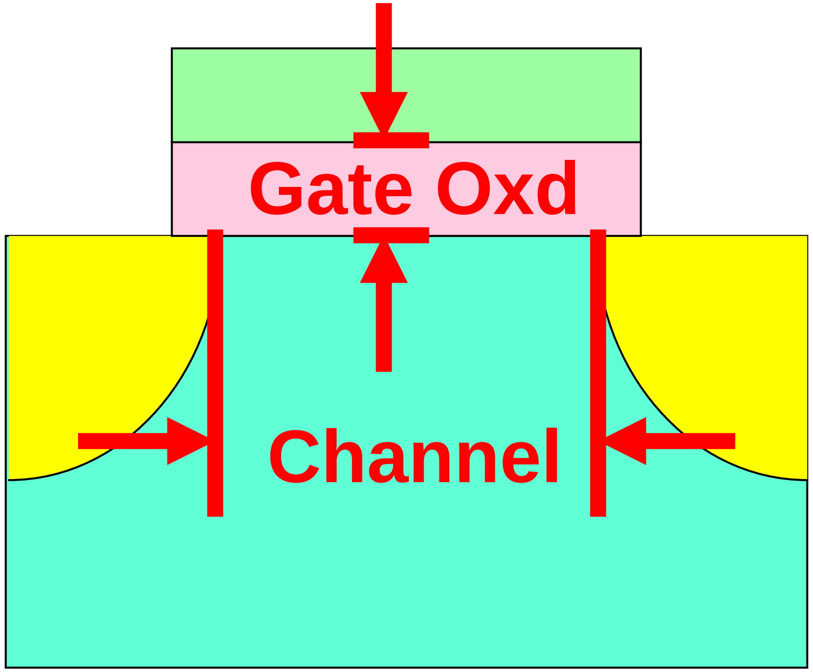
3 nm



Downsizing limit!

Channel length

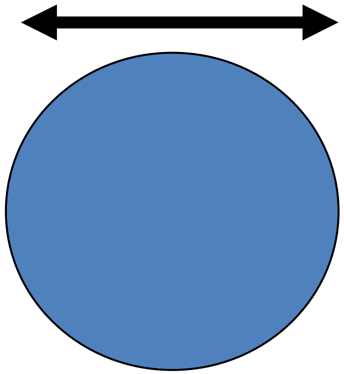
Gate oxide thickness



Prediction now!

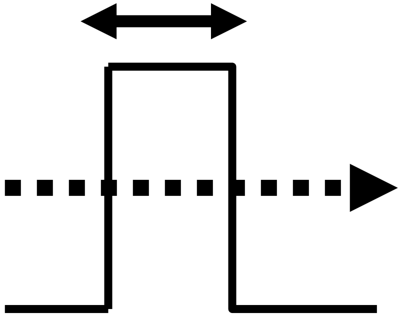
Electron wave length

10 nm



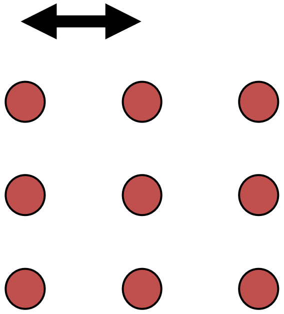
Tunneling distance

3 nm



Atom distance

0.3 nm

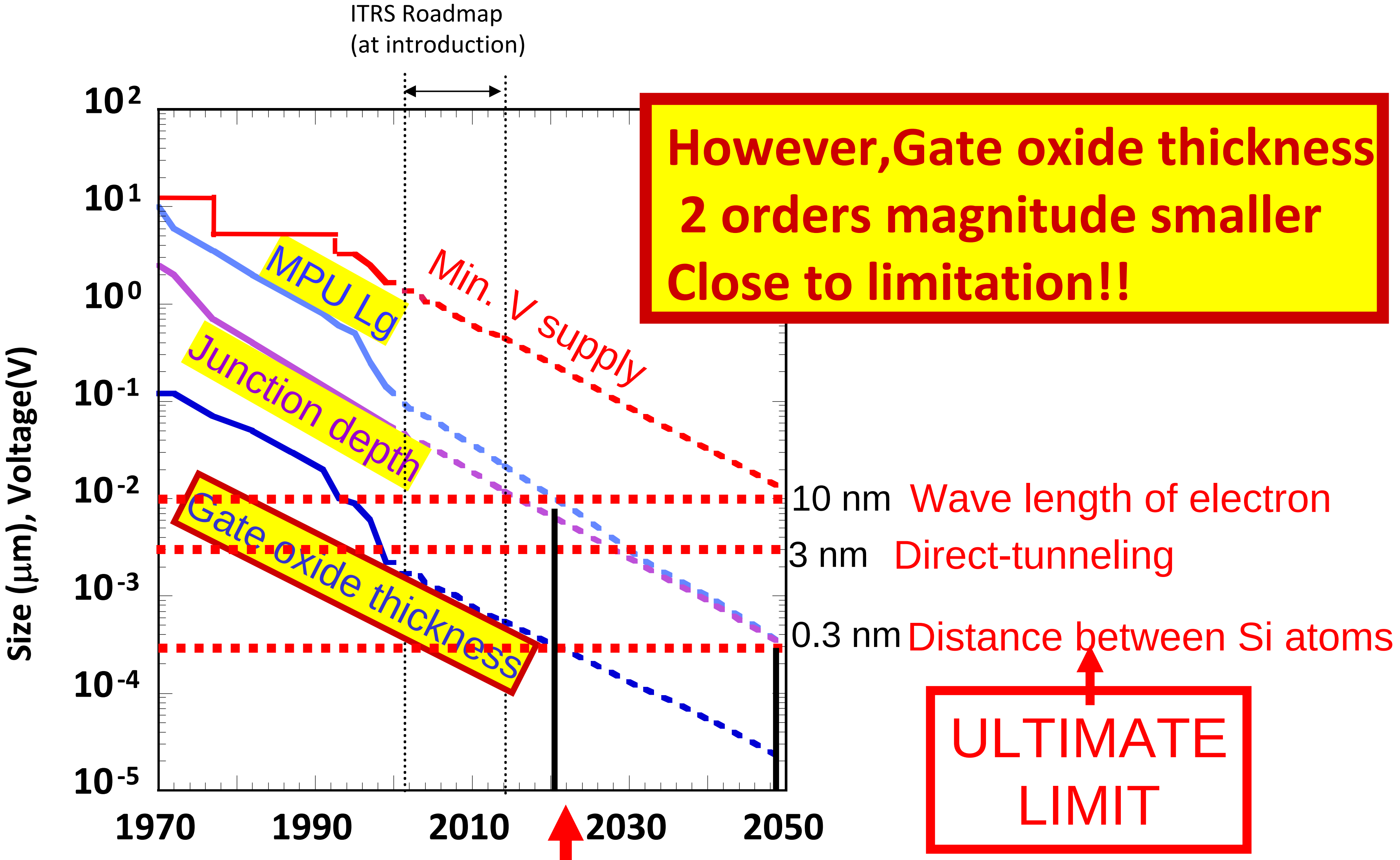


MOSFET operation

Lg = 2 ~ 1.5 nm?

Below this,
no one knows future!

Ultimate limitation

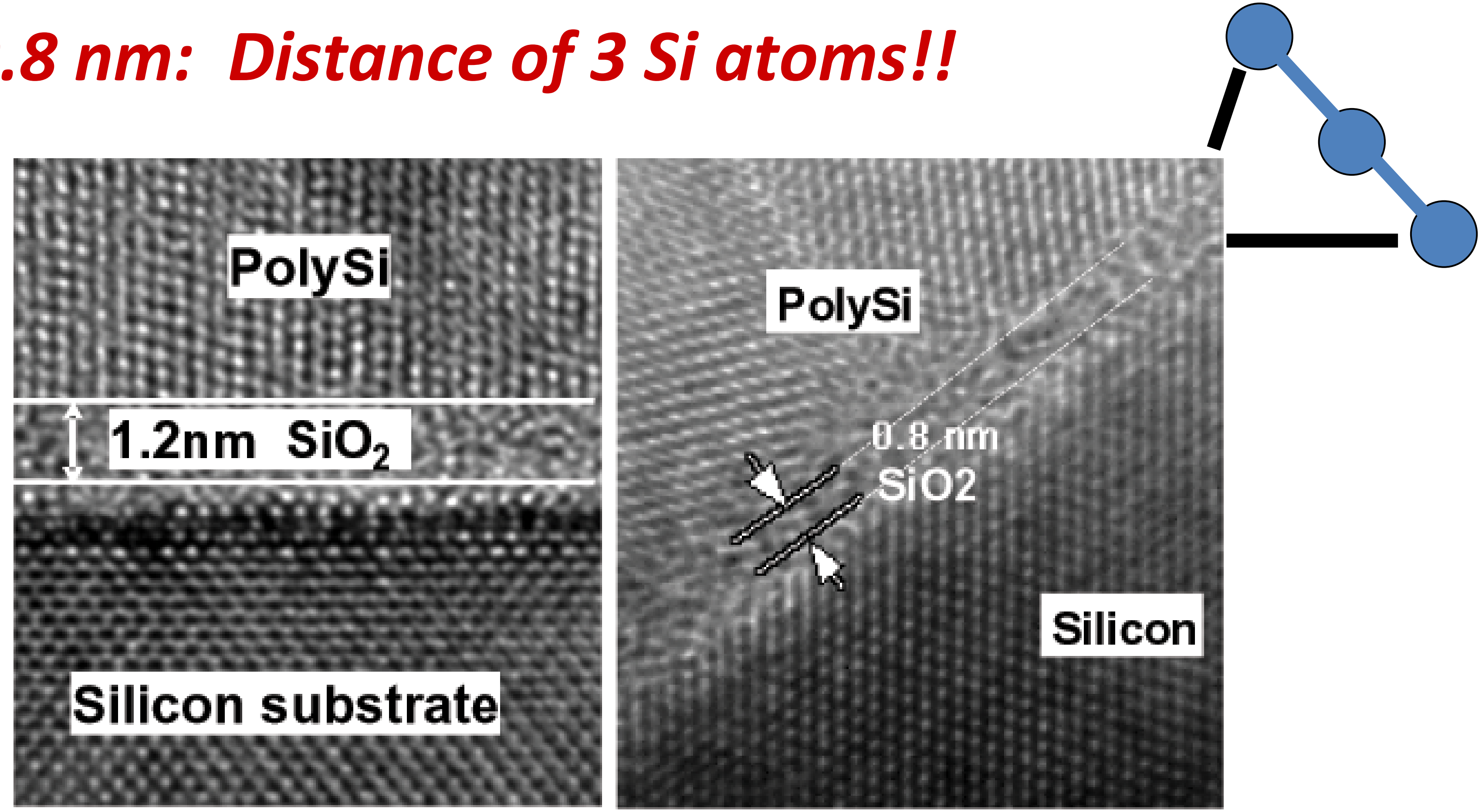


However,Gate oxide thickness 2 orders magnitude smaller Close to limitation!!

Lg: Gate length downsizing will continue to another 10-15 years

0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!



- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003

So, we are now in the limitation of downsizing?

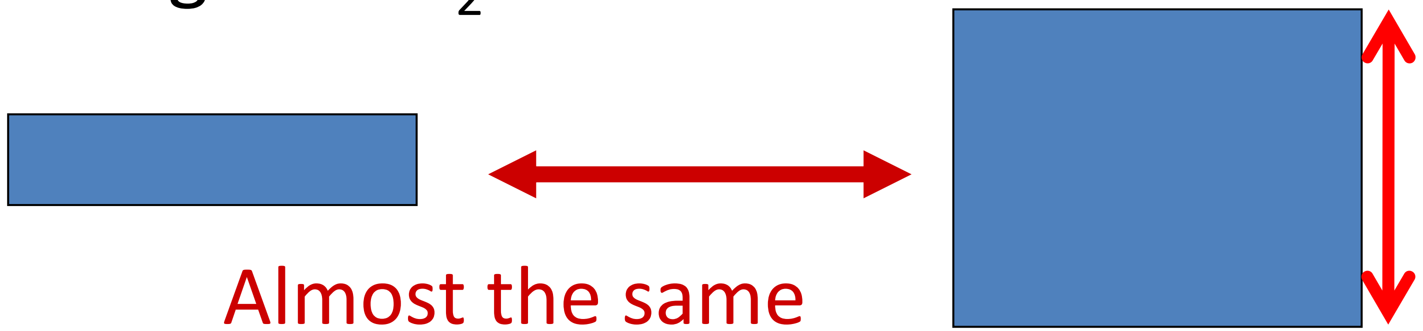
Do you believe this or do not?

There is a solution!
To use high-k dielectrics

K: Dielectric Constant

Thin gate SiO_2

Thick gate high-k dielectrics



Thick

↓

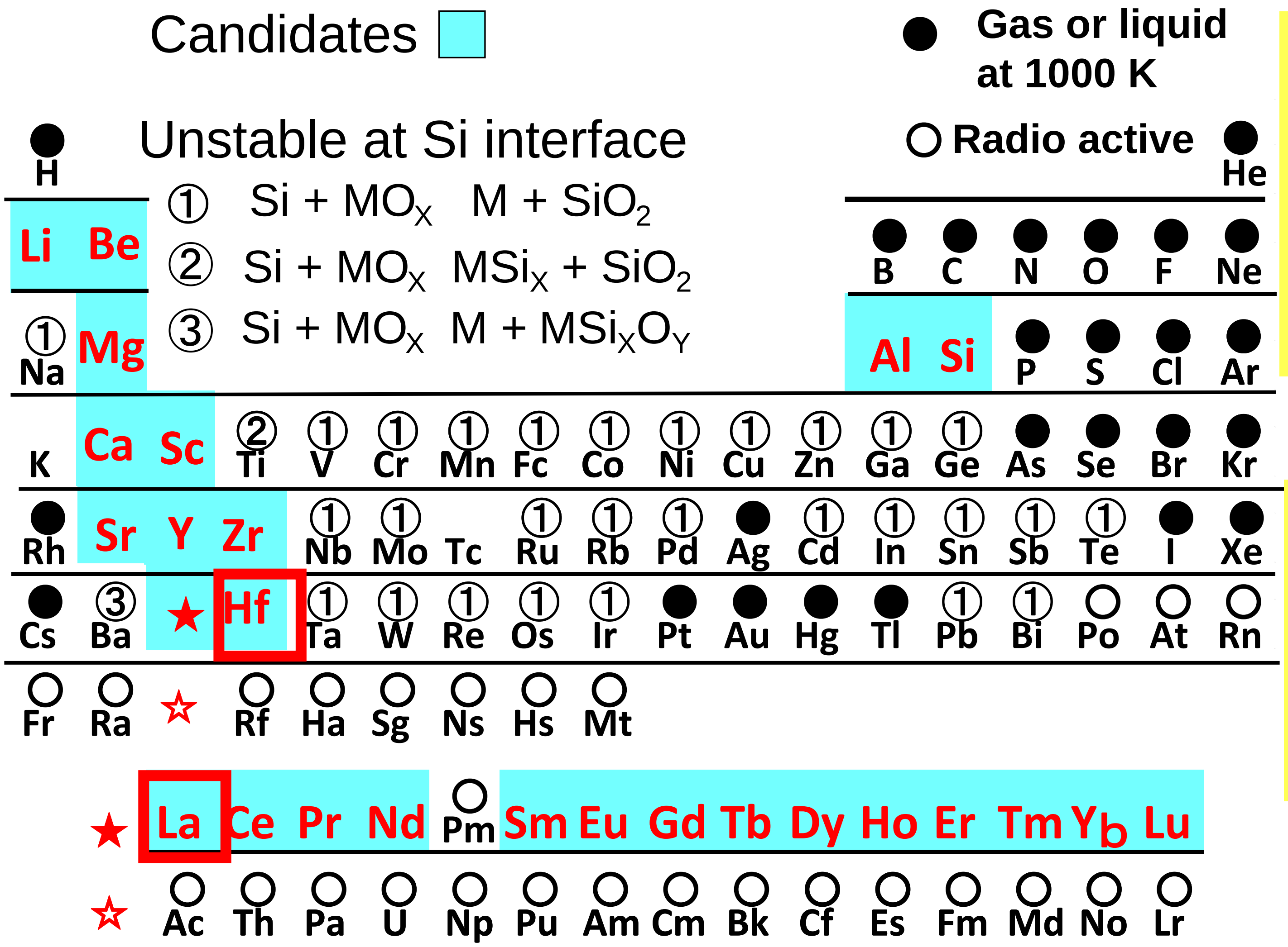
Small leakage Current

Almost the same electric characteristics

However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO_2!

Choice of High-k elements for oxide



Candidates 🟦

● Gas or liquid at 1000 K

○ Radio active

Unstable at Si interface

① Si + MO_X M + SiO_2

② Si + MO_X MSi_X + SiO_2

③ Si + MO_X M + MSi_XO_Y

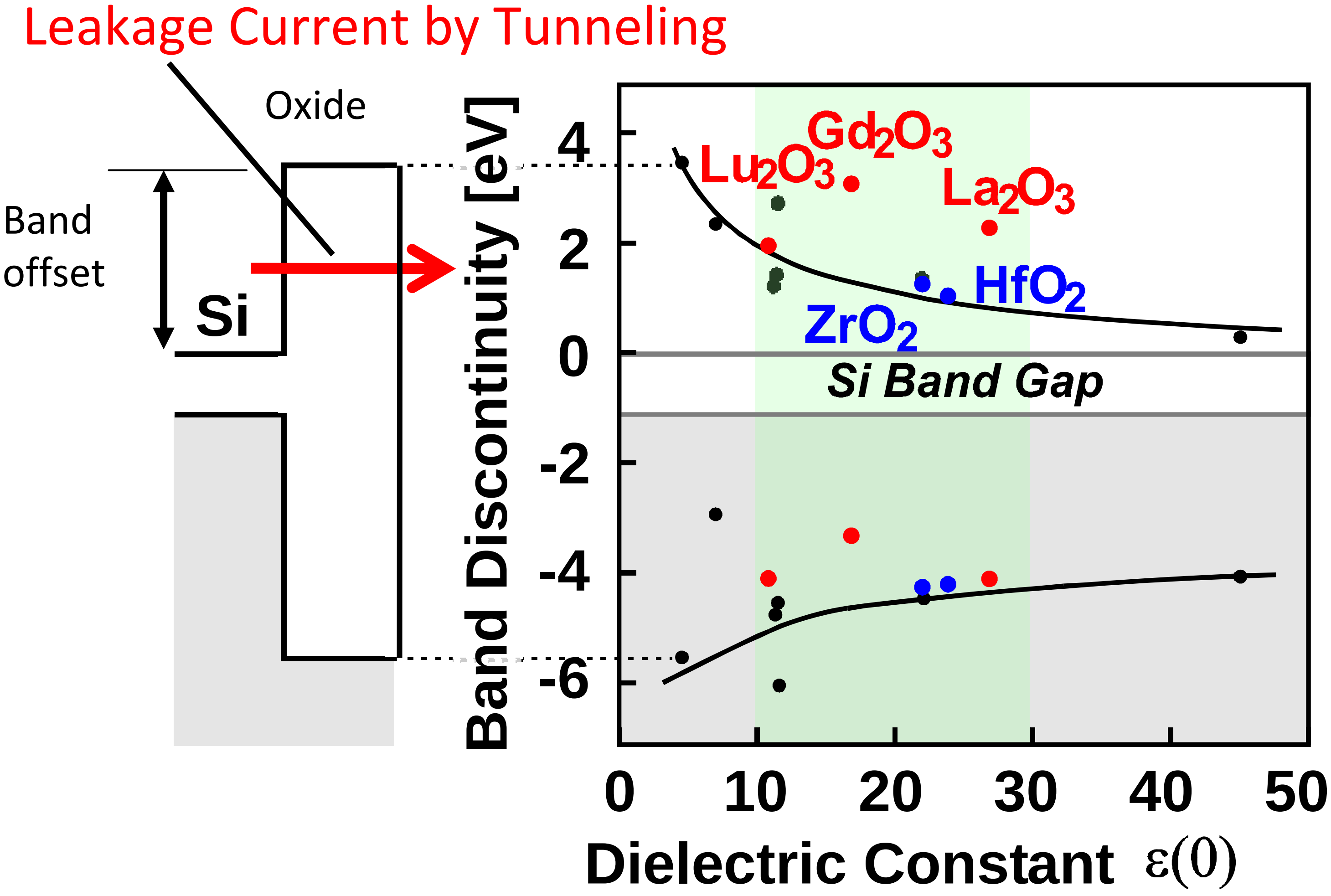
● H																	● He
🟦 Li	🟦 Be											● B	● C	● N	● O	● F	● Ne
① Na	🟦 Mg											🟦 Al	🟦 Si	● P	● S	● Cl	● Ar
K	🟦 Ca	🟦 Sc	② Ti	① V	① Cr	① Mn	① Fc	① Co	① Ni	① Cu	① Zn	① Ga	① Ge	● As	● Se	● Br	● Kr
● Rh	🟦 Sr	🟦 Y	🟦 Zr	① Nb	① Mo	Tc	① Ru	① Rb	① Pd	● Ag	① Cd	① In	① Sn	① Sb	① Te	● I	● Xe
● Cs	③ Ba	🟦 ★	🟦 Hf	① Ta	① W	① Re	① Os	① Ir	● Pt	● Au	● Hg	● Tl	① Pb	① Bi	○ Po	○ At	○ Rn
○ Fr	○ Ra	☆	○ Rf	○ Ha	○ Sg	○ Ns	○ Hs	○ Mt									
	★	🟦 La	🟦 Ce	🟦 Pr	🟦 Nd	○ Pm	🟦 Sm	🟦 Eu	🟦 Gd	🟦 Tb	🟦 Dy	🟦 Ho	🟦 Er	🟦 Tm	🟦 Yb	🟦 Lu	
	☆	○ Ac	○ Th	○ Pa	○ U	○ Np	○ Pu	○ Am	○ Cm	○ Bk	○ Cf	○ Es	○ Fm	○ Md	○ No	○ Lr	

HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

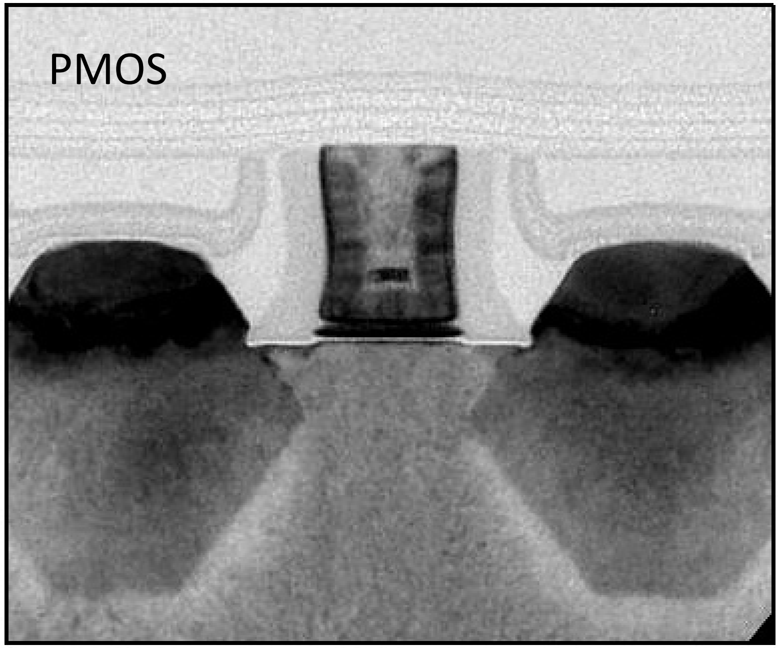
Conduction band offset vs. Dielectric Constant

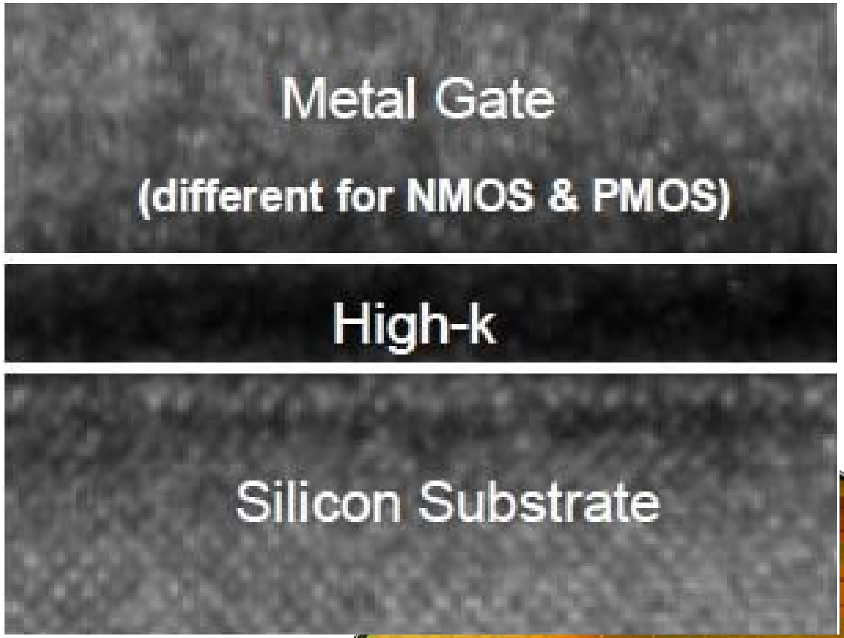


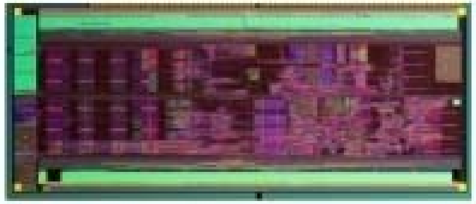
XPS measurement by Prof. T. Hattori, INFOS 2003

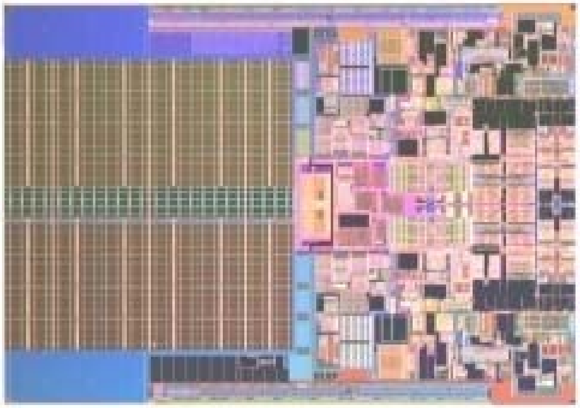
High-k gate insulator MOSFETs for Intel: EOT=1nm

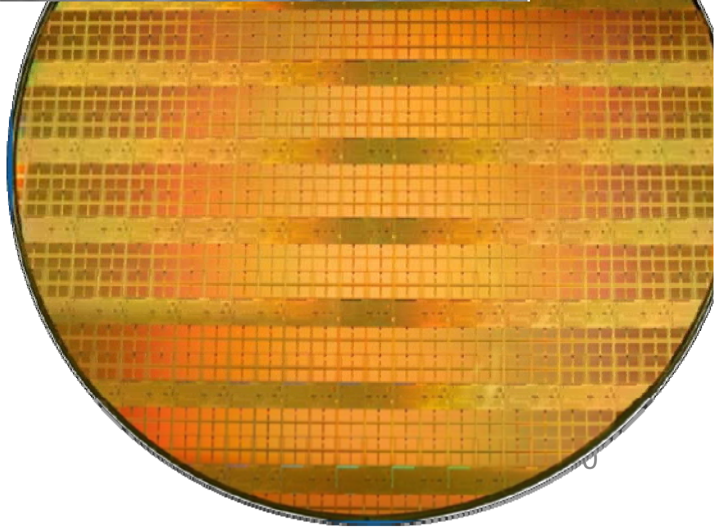
EOT: Equivalent Oxide Thickness

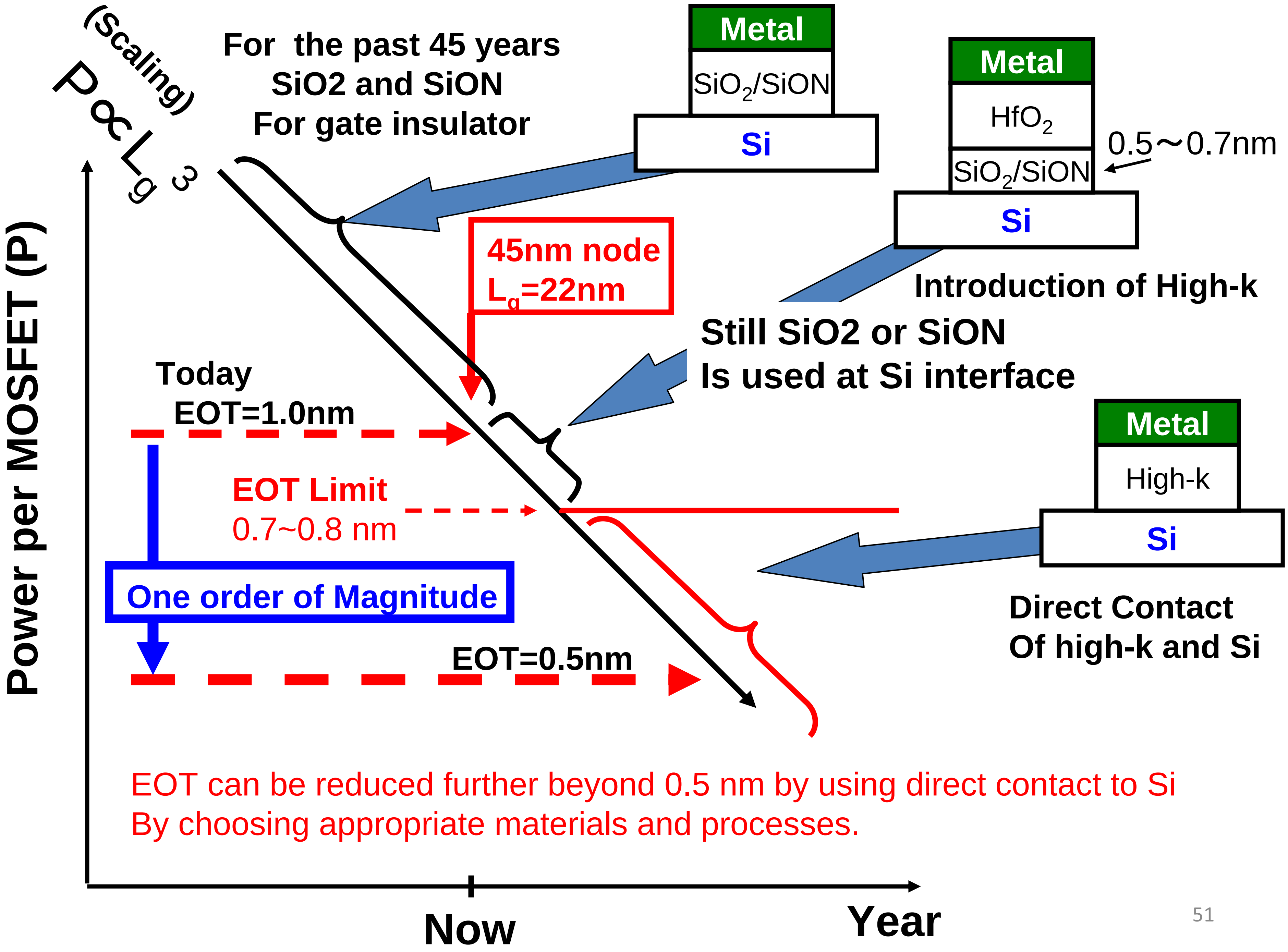












(Scaling) $P \propto L_g^{\ 3}$

For the past 45 years
SiO2 and SiON
For gate insulator

45nm node
L_g=22nm

Introduction of High-k

Still SiO2 or SiON
Is used at Si interface

Today
EOT=1.0nm

EOT Limit
0.7~0.8 nm

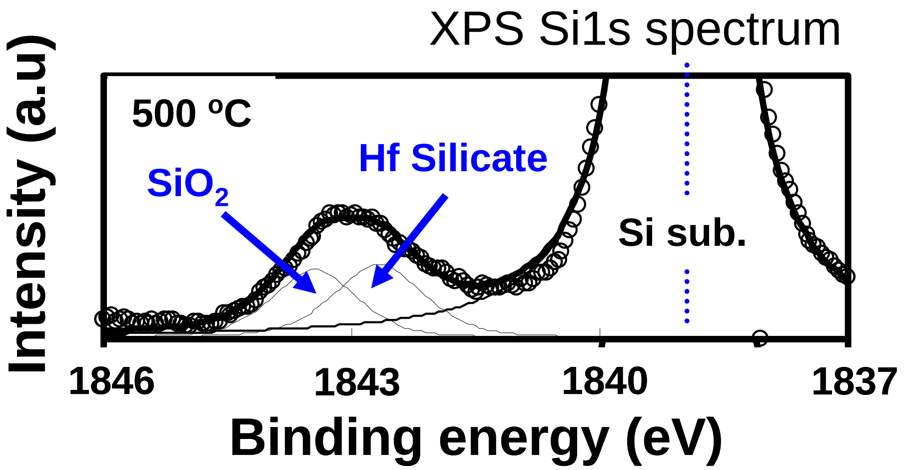
One order of Magnitude

EOT=0.5nm

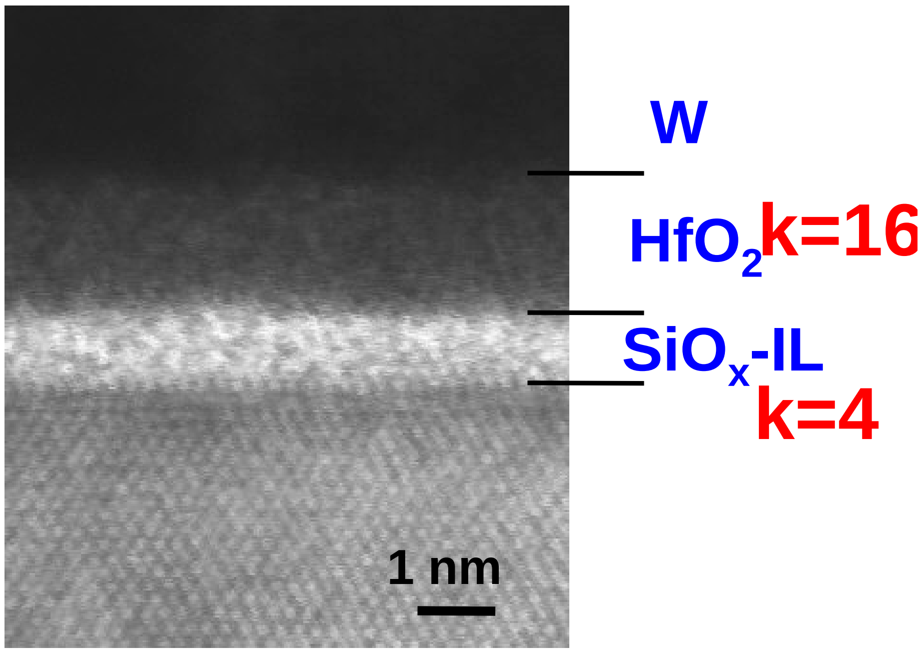
Direct Contact
Of high-k and Si

EOT can be reduced further beyond 0.5 nm by using direct contact to Si
By choosing appropriate materials and processes.

SiO_x-IL growth at HfO_2/Si Interface


XPS Si1s spectrum

TEM image 500 °C 30min



Phase separator

$$HfO_2 + Si + O_2 \rightarrow HfO_2 + Si + 2O^* \rightarrow HfO_2 + SiO_2$$

H. Shimizu, JJAP, 44, pp. 6131

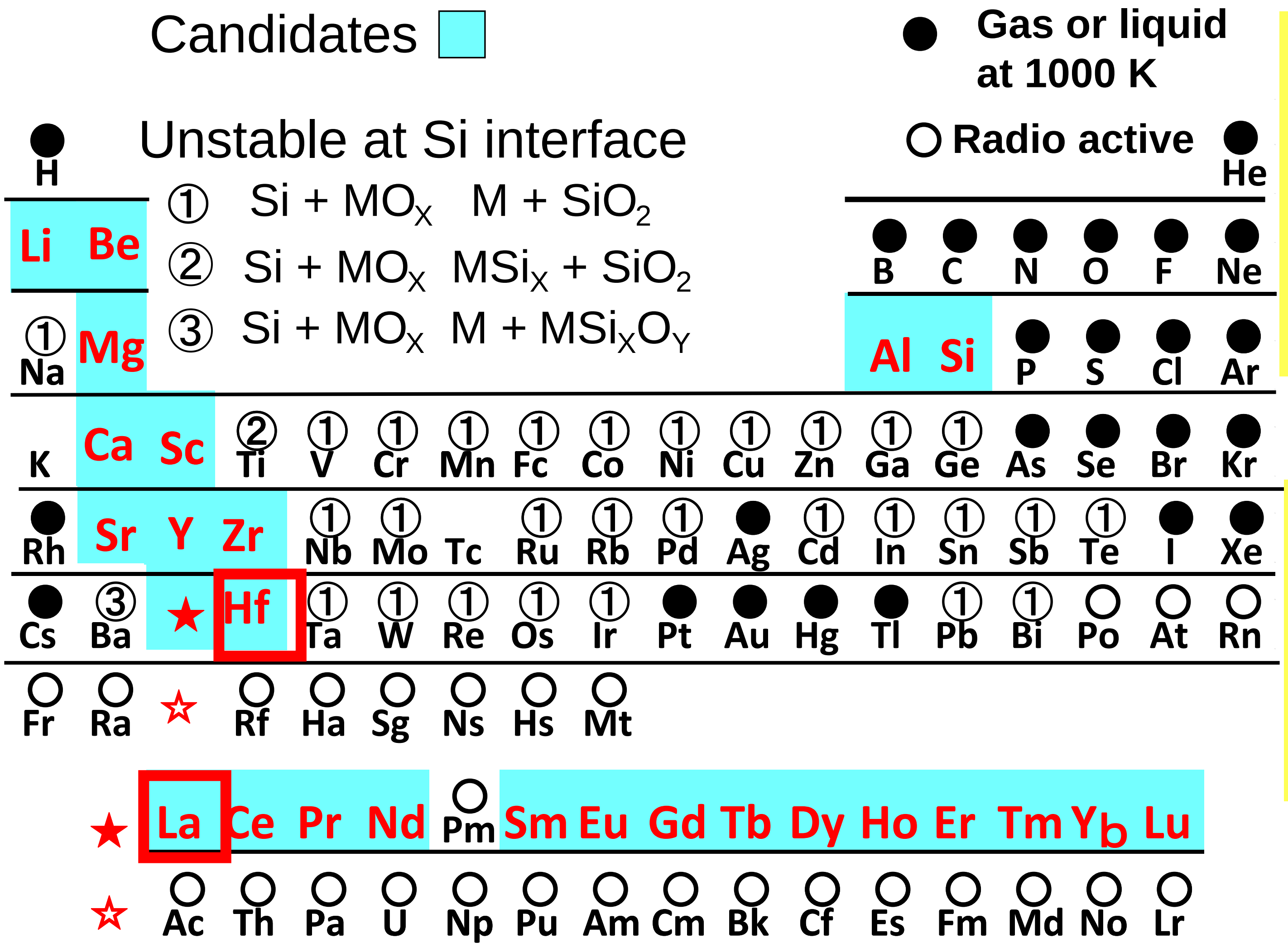
Oxygen supplied from W gate electrode

D.J.Lichtenwalner, Tans. ECS 11, 319

SiO_x-IL is formed after annealing

Oxygen control is required for optimizing the reaction

Choice of High-k elements for oxide



Candidates 🟦

● Gas or liquid at 1000 K

○ Radio active

Unstable at Si interface

① Si + MO_X M + SiO_2

② Si + MO_X MSi_X + SiO_2

③ Si + MO_X M + MSi_XO_Y

● H																	● He
Li	Be											● B	● C	● N	● O	● F	● Ne
① Na	Mg											Al	Si	● P	● S	● Cl	● Ar
K	Ca	Sc	② Ti	① V	① Cr	① Mn	① Fc	① Co	① Ni	① Cu	① Zn	① Ga	① Ge	● As	● Se	● Br	● Kr
● Rh	Sr	Y	Zr	① Nb	① Mo	Tc	① Ru	① Rb	① Pd	● Ag	① Cd	① In	① Sn	① Sb	① Te	● I	● Xe
● Cs	③ Ba	★	Hf	① Ta	① W	① Re	① Os	① Ir	● Pt	● Au	● Hg	● Tl	① Pb	① Bi	○ Po	○ At	○ Rn
○ Fr	○ Ra	☆	○ Rf	○ Ha	○ Sg	○ Ns	○ Hs	○ Mt									

★	La	Ce	Pr	Nd	○ Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
☆	○ Ac	○ Th	○ Pa	○ U	○ Np	○ Pu	○ Am	○ Cm	○ Bk	○ Cf	○ Es	○ Fm	○ Md	○ No	○ Lr

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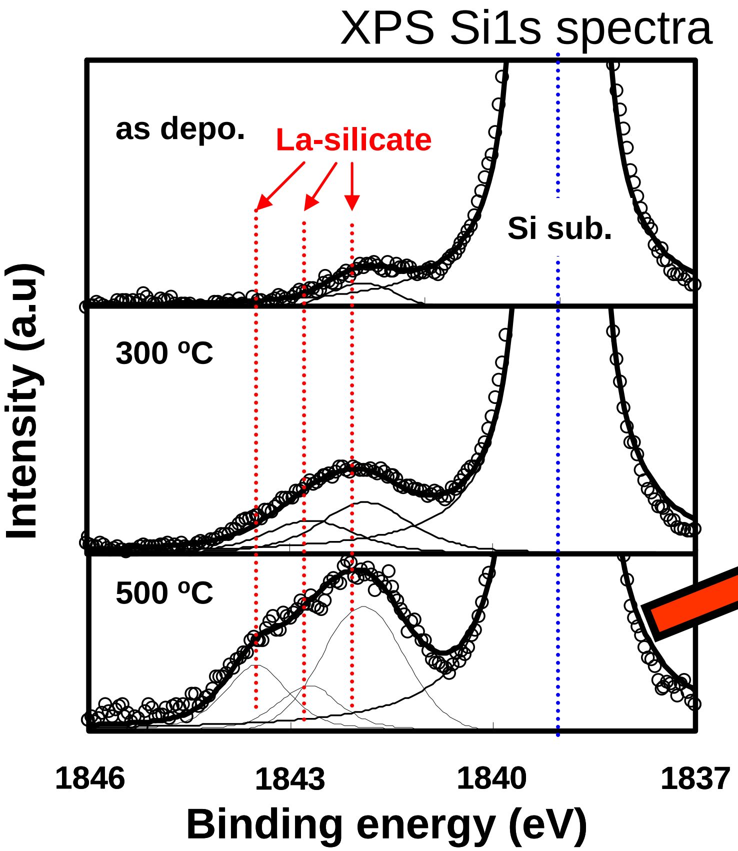
La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

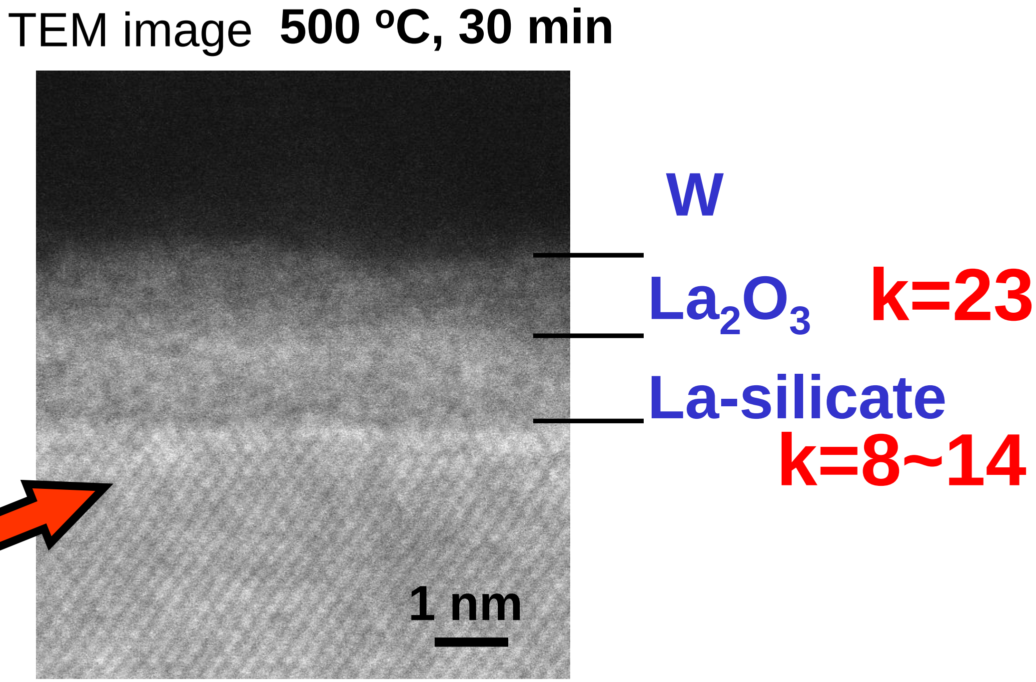
R. Hauser, IEDM Short Course, 1999

Hubbard and Schlom, J Mater Res 11 2757 (1996)

La-Silicate Reaction at La_2O_3/Si

Direct contact high-k/Si is possible

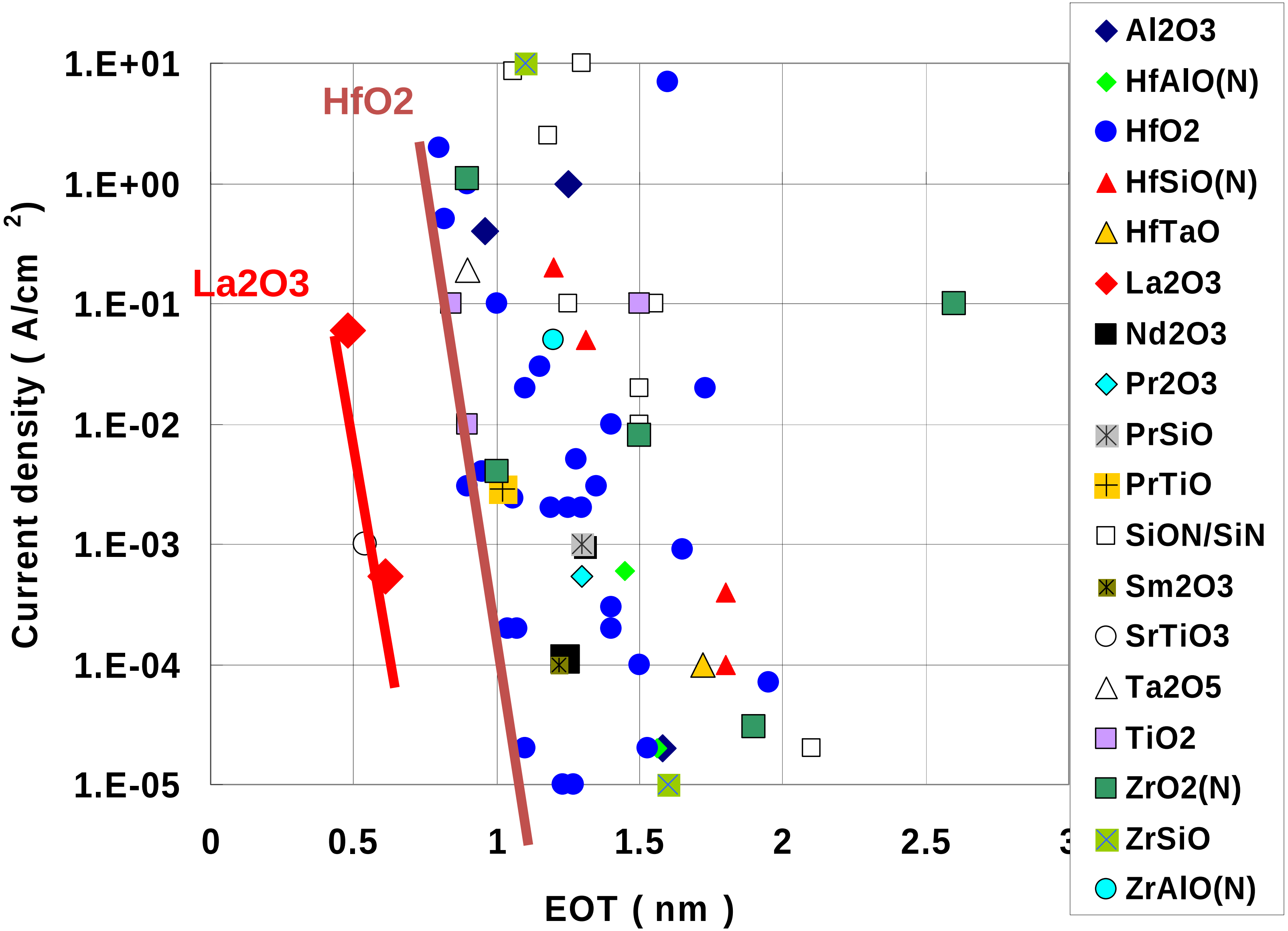




La_2O_3 + Si + nO_2
→ La_2SiO_5, $La_2Si_2O_7$,
$La_{9.33}Si_6O_{26}$, $La_{10}(SiO_4)_6O_3$, etc.

La_2O_3 can achieve direct contact of high-k/Si

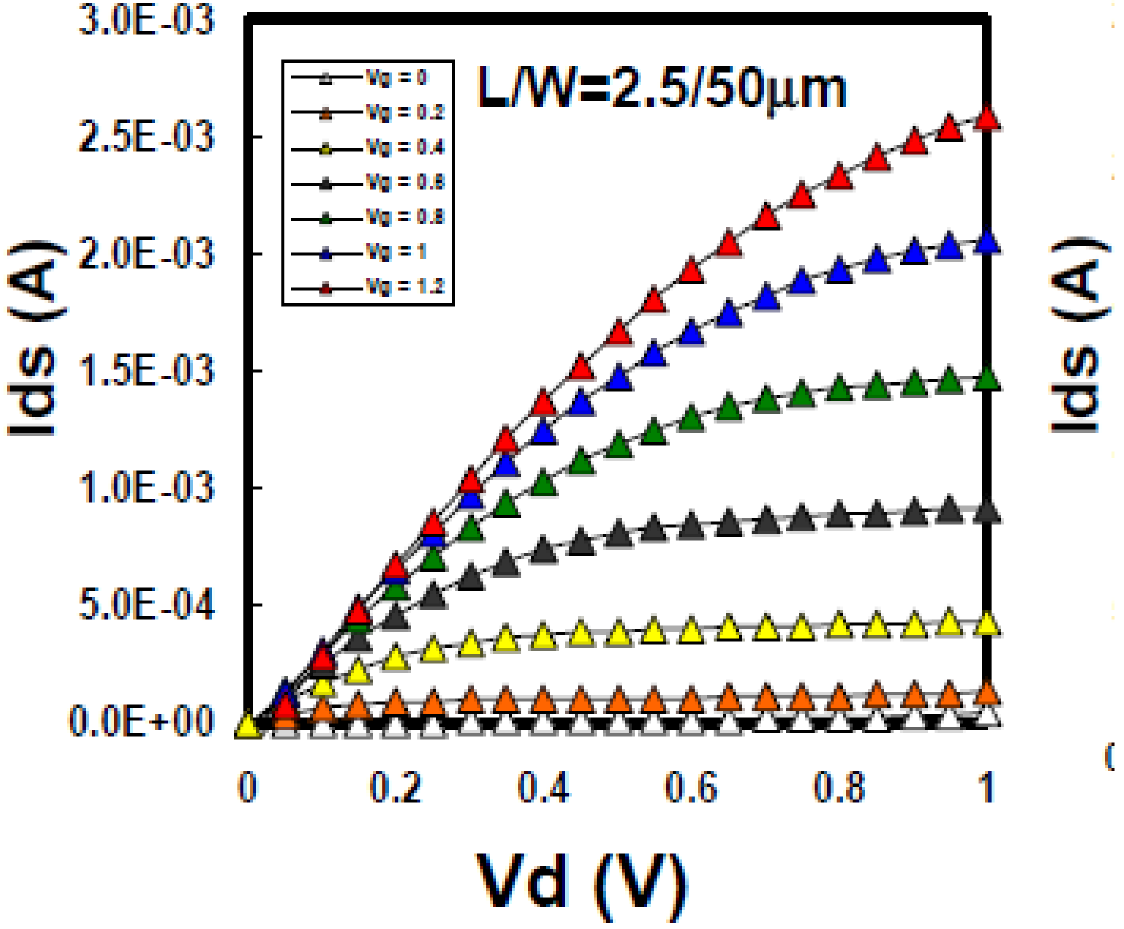
Gate Leakage vs EOT, (Vg=|1|V)



EOT = 0.48 nm

Our results

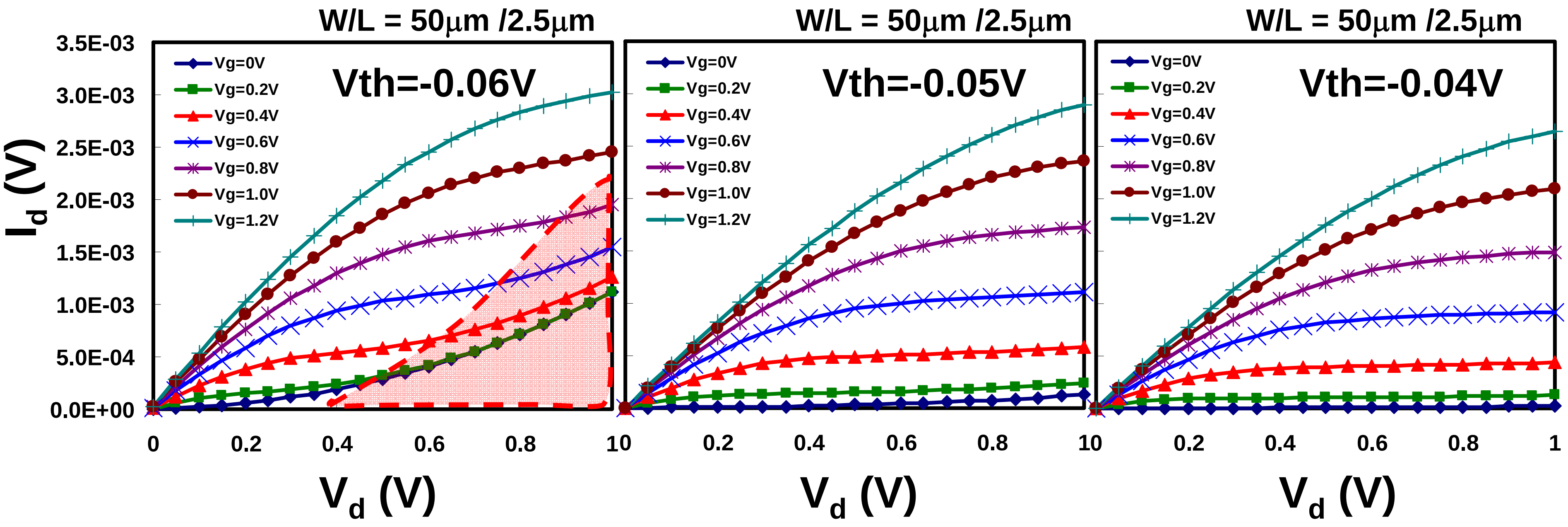
Transistor with La2O3 gate insulator



EOT=0.37nm

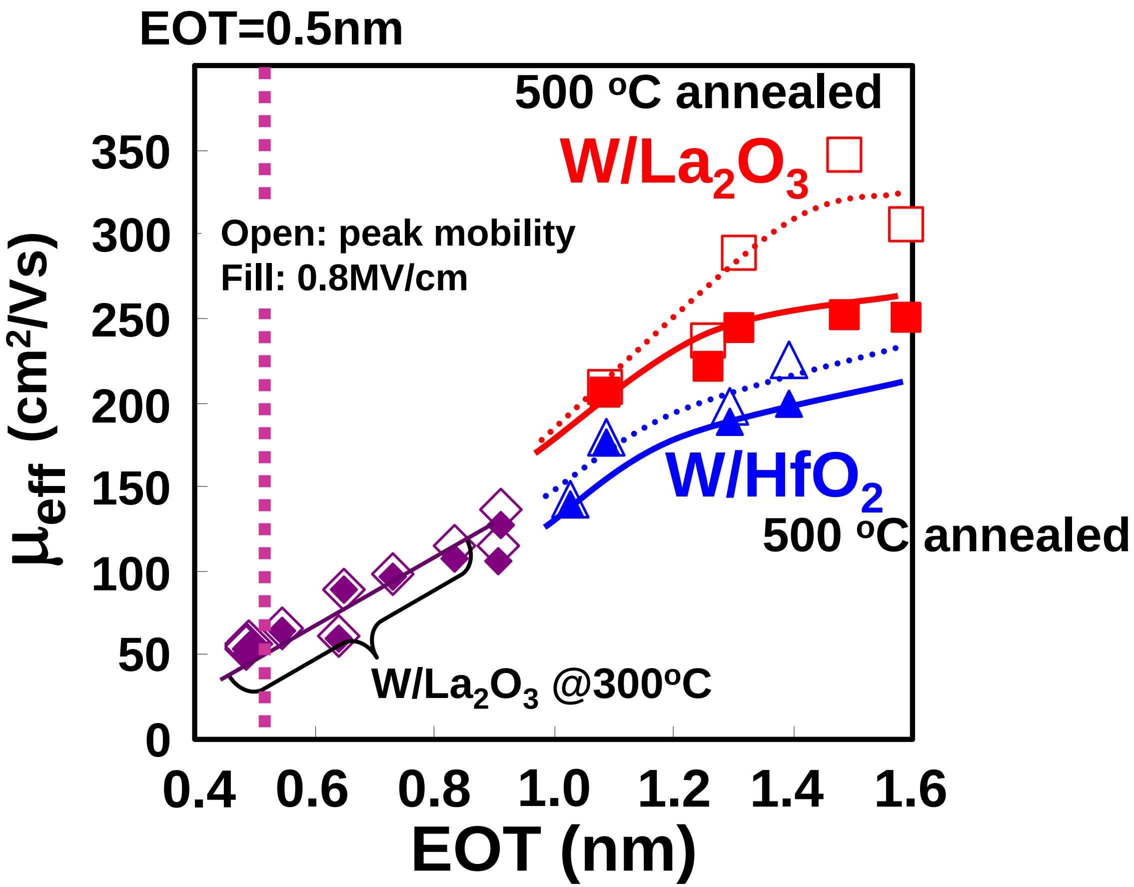
La2O3

EOT=0.37nm EOT=0.40nm EOT=0.48nm



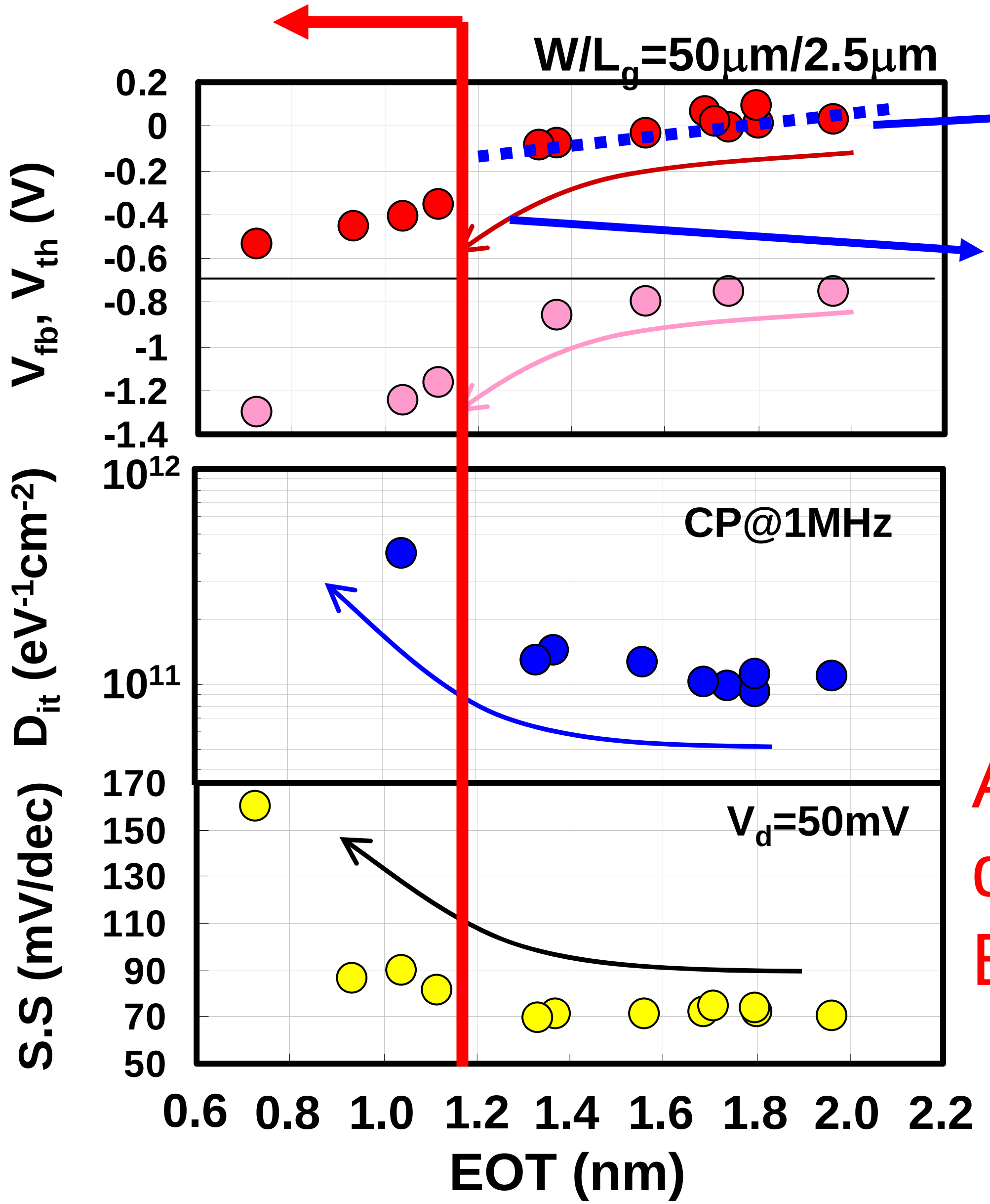
0.48 →0.37nm Increase of Id at 30%

μ_{eff} of W/La_2O_3 and W/HfO_2 nFET on EOT



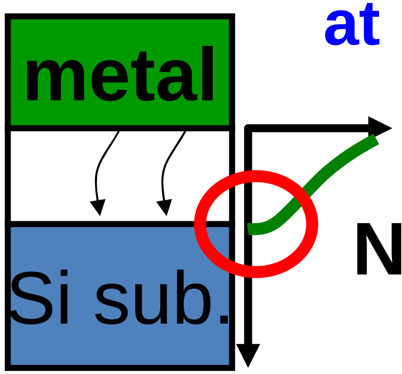
- W/La_2O_3 exhibits higher μ_{eff} than W/HfO_2
- μ_{eff} start degrades below EOT=1.4nm

FET characteristics of W/La_2O_3 on EOT



N_{fix}=7x10^{12} cm^{-2}

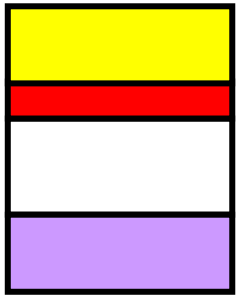
Aggressive N_{fix} generation at EOT<1.2nm



N_{fix} and D_{it}

All characteristics start to degrade or shift below EOT=1.4nm

Gate Metal Induced Defects Compensation

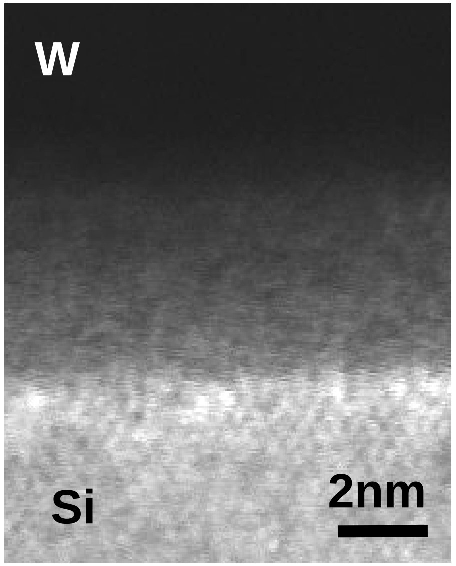


Metal Gate

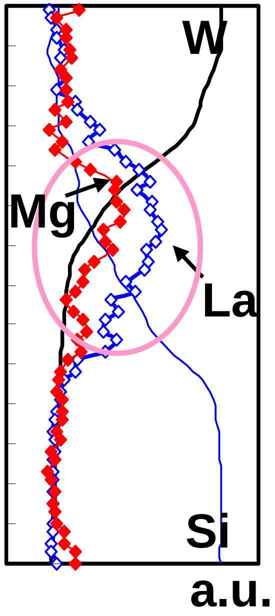
MgO

La2O3

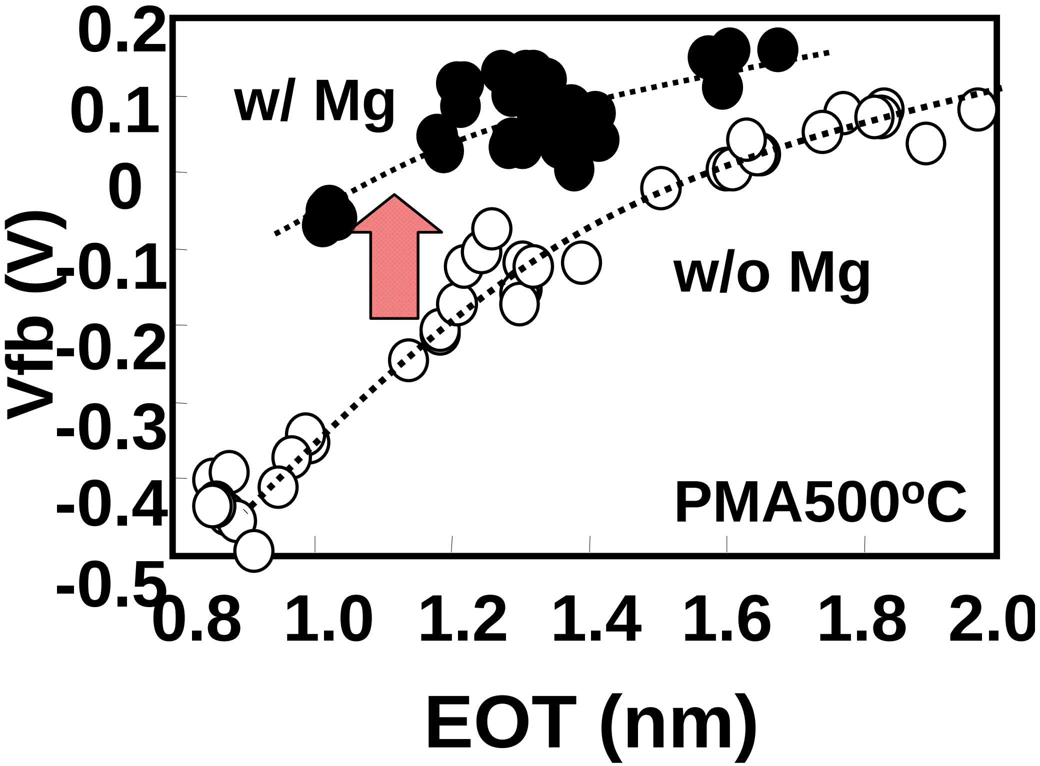
Si



TEM

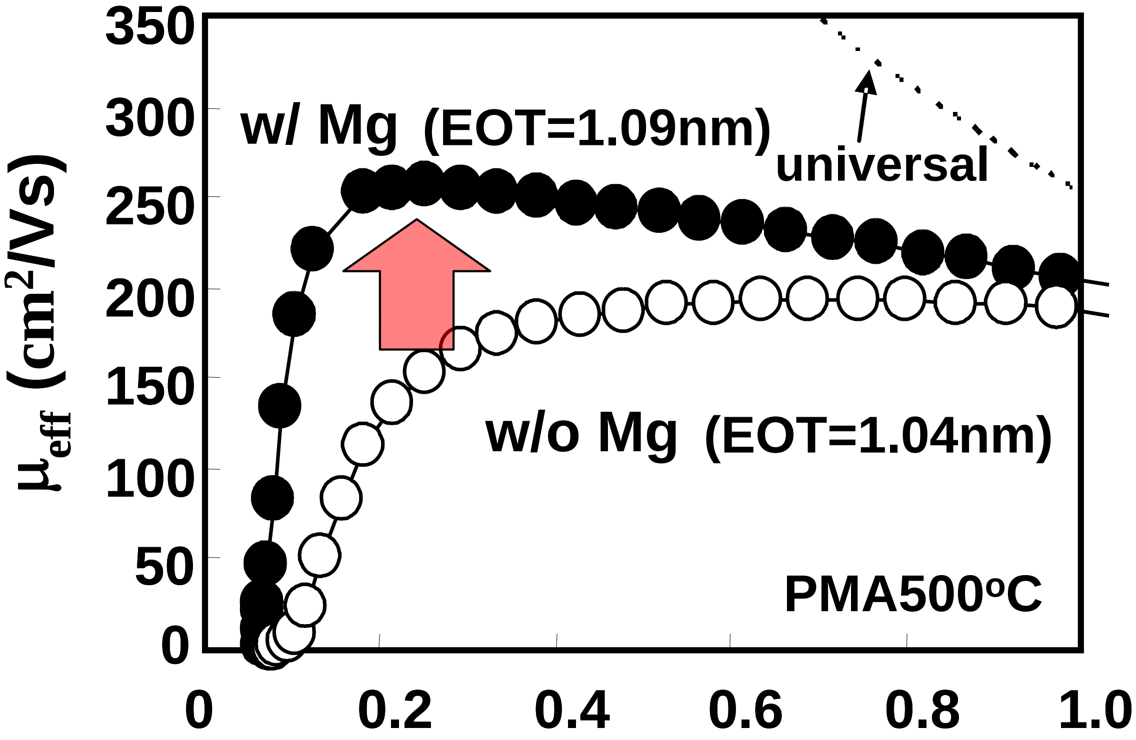


EDX



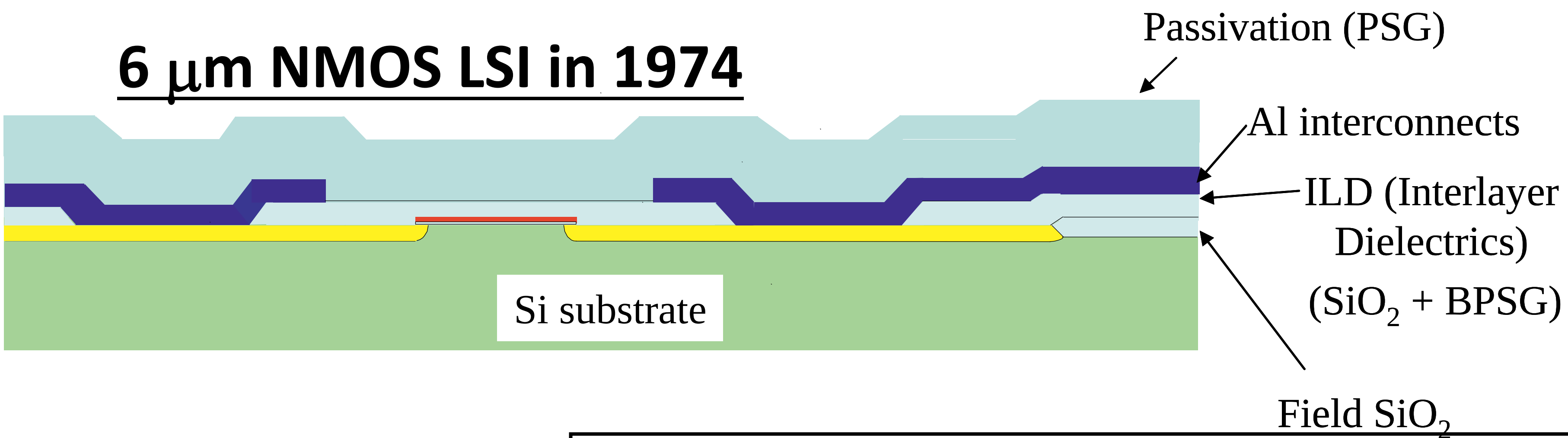
Suppression of aggressive shift in V_{fb}

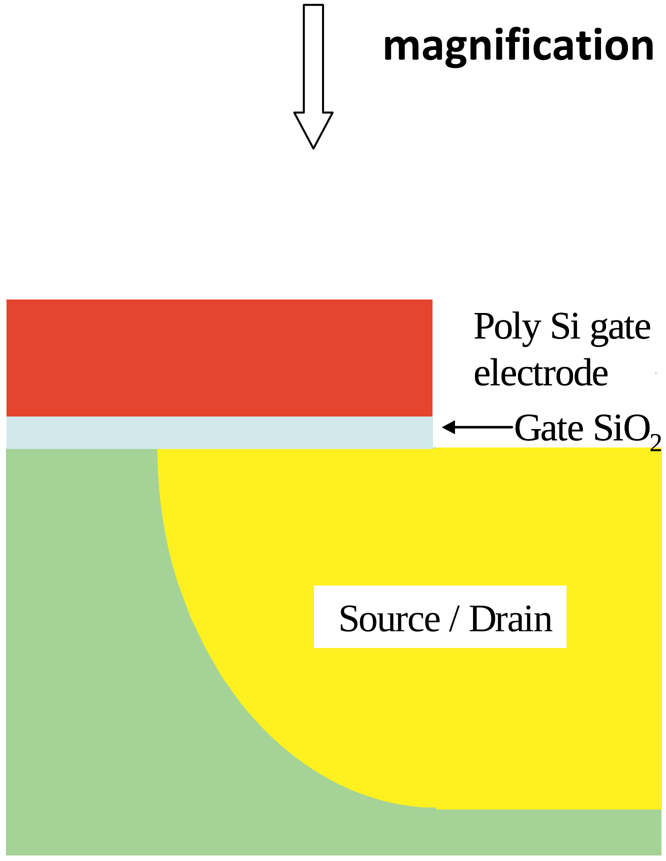
Mobility Improvement with Mg Incorporation



Recovery of μ_{eff} mainly at low E_{eff}

6 μm NMOS LSI in 1974





Layers

1. Si substrate
2. Field oxide
3. Gate oxide
4. Poly Si
5. S/D
6. Interlayer
7. Aluminum
8. Passivation

Materials

1. Si
2. SiO_2
3. BPSG
4. Al
5. PSG

Atoms

1. Si

2. O

3. P

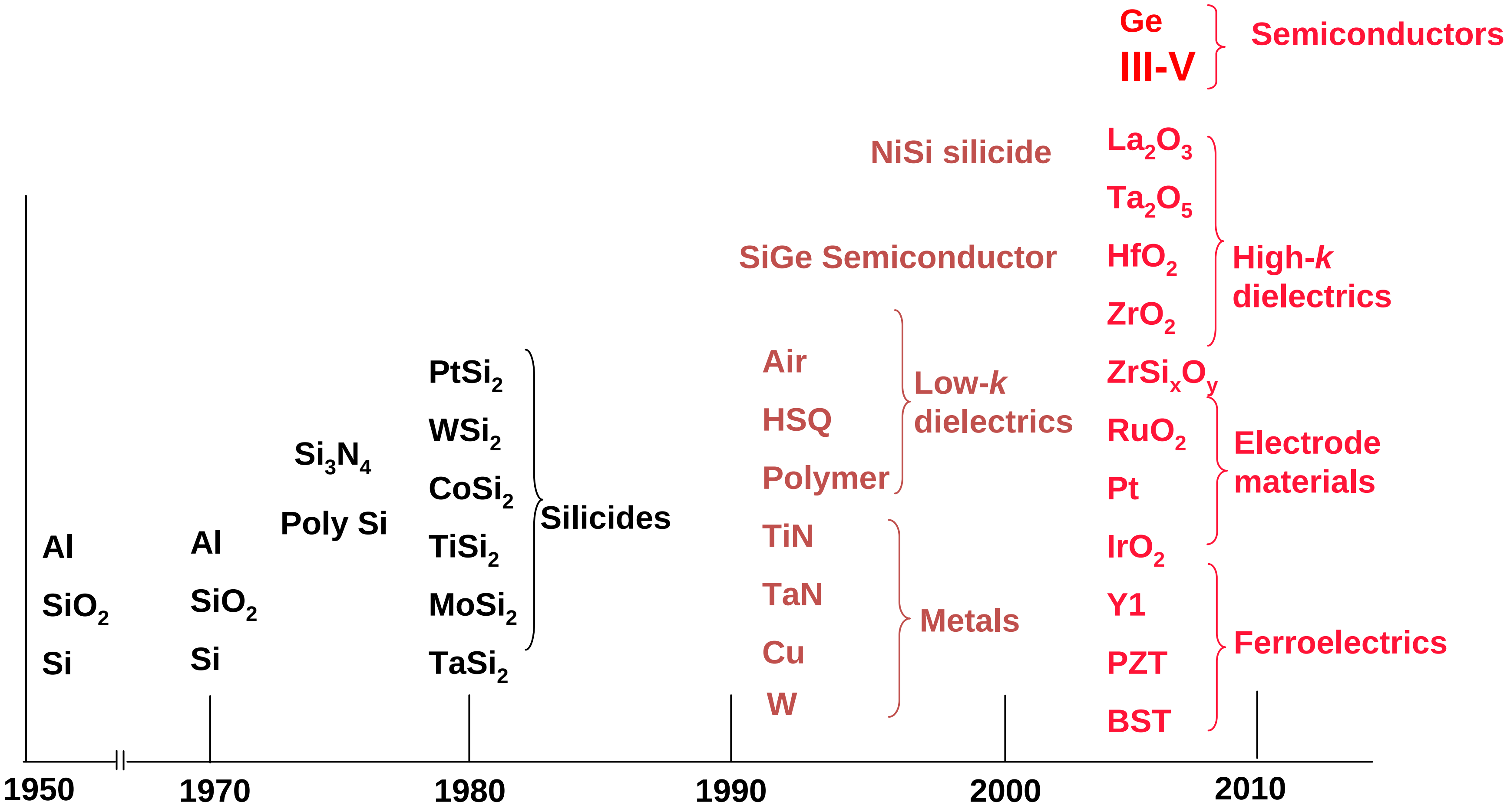
4. B

5. Al

(H, N, Cl)

Just examples!
Many other candidates

New materials



Al
SiO_2
Si

Al
SiO_2
Si

Si_3N_4
Poly Si

$PtSi_2$
WSi_2
$CoSi_2$
$TiSi_2$
$MoSi_2$
$TaSi_2$
Silicides

SiGe Semiconductor
Air
HSQ
Polymer
Low-*k* dielectrics
TiN
TaN
Cu
W
Metals

NiSi silicide

Ge
III-V
Semiconductors

La_2O_3
Ta_2O_5
HfO_2
ZrO_2
High-*k* dielectrics

$ZrSi_xO_y$
RuO_2
Pt
IrO_2
Electrode materials

Y1
PZT
BST
Ferroelectrics

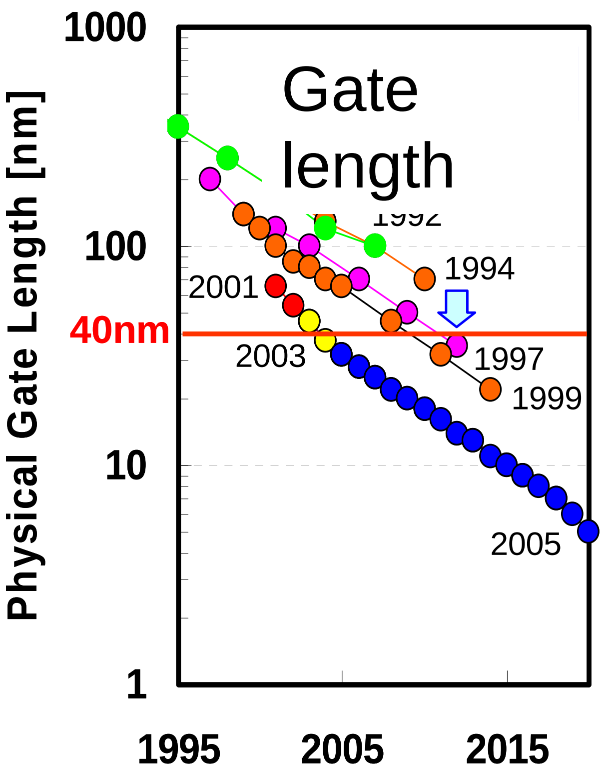
Y. Nishi, Si Nano Workshop, 2006,

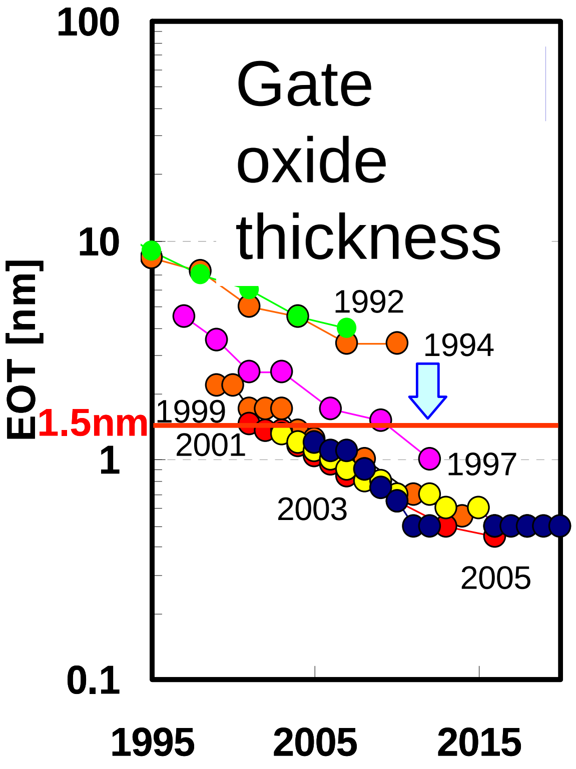
(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)

What is a roadmap?   What is ITRS?

Roadmap: Prediction of future technologies

ITRS: International Technology Roadmap for Semiconductors
made by SIA (Semiconductor Industry Association with
Collaboration with Japan, Europe, Korea and Taiwan)



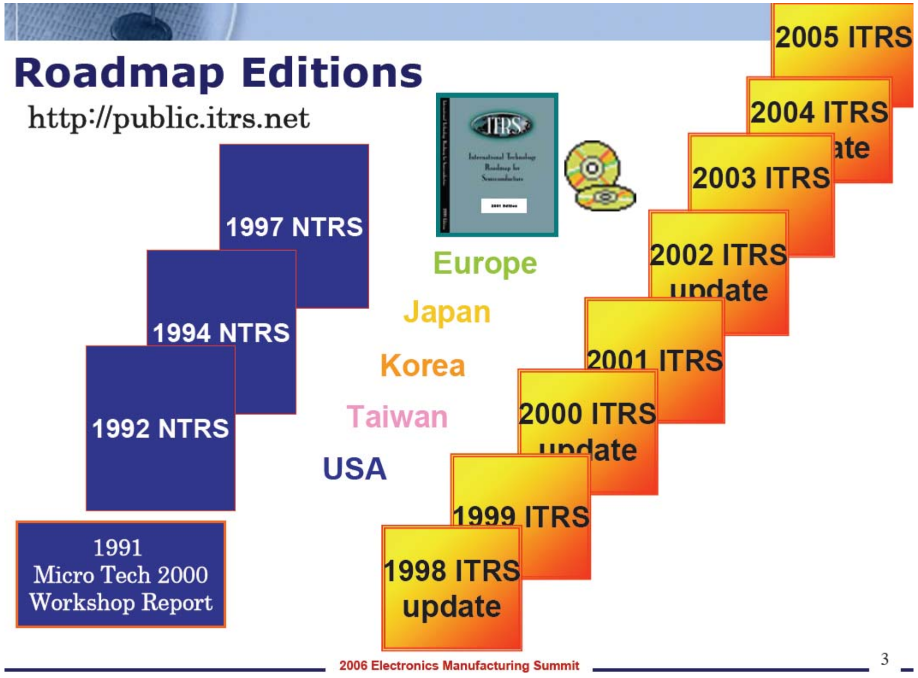


1992 -1997:NTRS (National Technology Roadmap)
1998 -   : ITRS (International Technology Roadmap)

2008 ITRS update

2007 ITRS

2006 ITRS update



Roadmap Editions

http://public.itrs.net

1991
Micro Tech 2000
Workshop Report

1992 NTRS

1994 NTRS

1997 NTRS

Europe
Japan
Korea
Taiwan
USA

1998 ITRS update

1999 ITRS

2000 ITRS update

2001 ITRS

2002 ITRS update

2003 ITRS

2004 ITRS
ate

2005 ITRS

2006 Electronics Manufacturing Summit

Question:

How far we can go with downscaling?

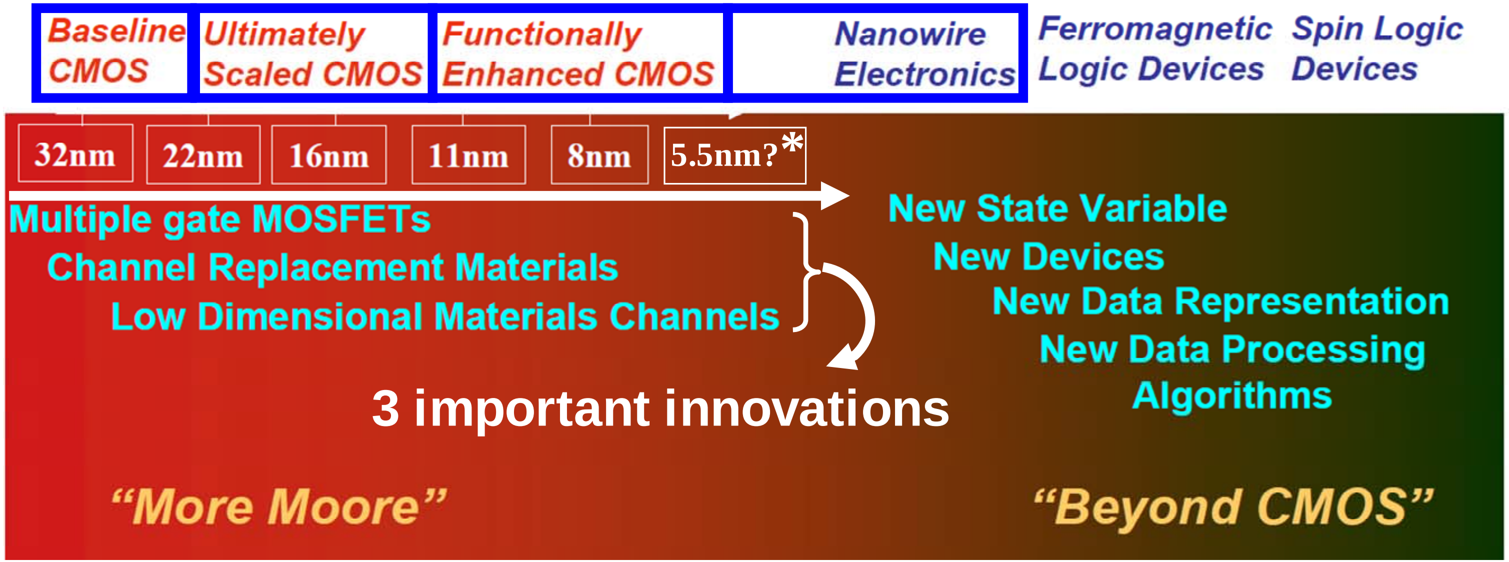
-There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

-Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

-Two candidates have emerged for R & D

1. Nanowire/tube MOSFETs
2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.



Baseline CMOS | *Ultimately Scaled CMOS* | *Functionally Enhanced CMOS* | *Nanowire Electronics* | *Ferromagnetic Logic Devices* | *Spin Logic Devices*

32nm | 22nm | 16nm | 11nm | 8nm | 5.5nm?*

Multiple gate MOSFETs
Channel Replacement Materials
Low Dimensional Materials Channels

3 important innovations

New State Variable
New Devices
New Data Representation
New Data Processing Algorithms

"More Moore"

"Beyond CMOS"

ITRS figure edited by Iwai

Source: 2008 ITRS Summer Public Conf.

***5.5nm? was added by Iwai**

How far can we go?

Past

0.7 times per 3 years

In 40 years: 15 generations,
Size 1/200, Area 1/40,000

1973年
↓

8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm

Now
↓

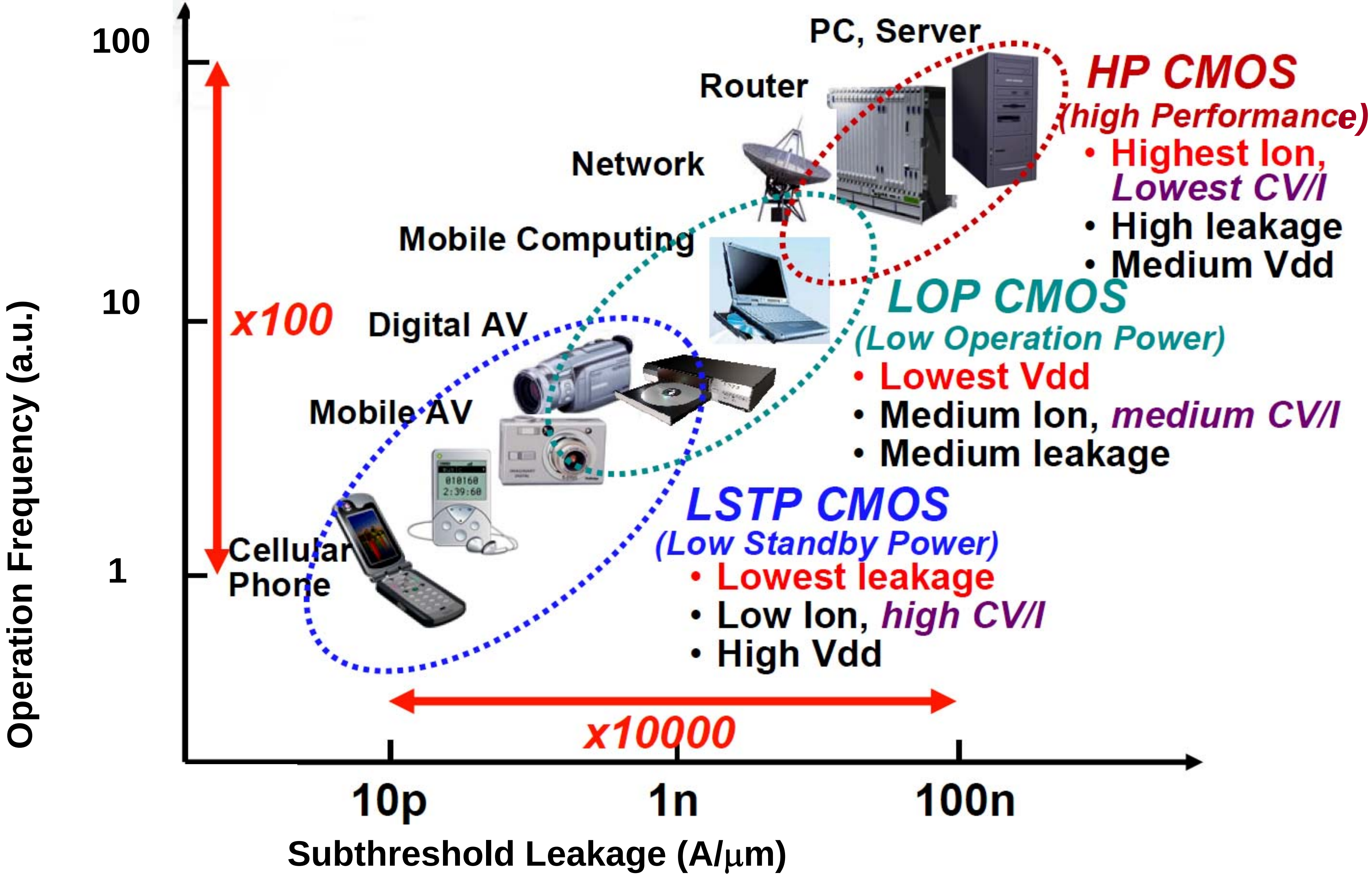
→ 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm

Future

→ 32nm → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

- At least 5,6 generations, for 15 ~ 20 years
- Hopefully 8 generations, for 30 years

HP, LOP, LSTP for Logic CMOS



HP CMOS
(high Performance)
- Highest Ion, *Lowest CV/I*
- High leakage
- Medium Vdd

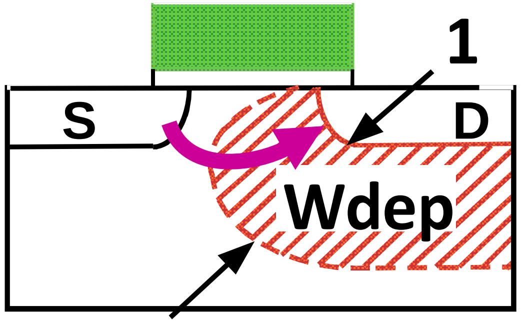
LOP CMOS
(Low Operation Power)
- Lowest Vdd
- Medium Ion, *medium CV/I*
- Medium leakage

LSTP CMOS
(Low Standby Power)
- Lowest leakage
- Low Ion, *high CV/I*
- High Vdd

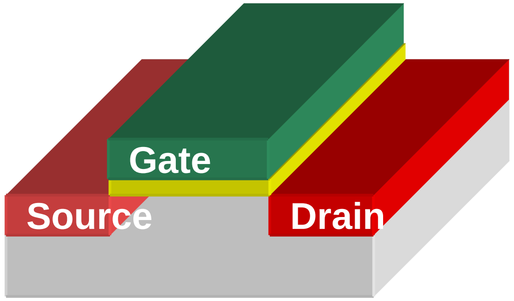
Source: 2007 ITRS Winter Public Conf.

Because of off-leakage control,

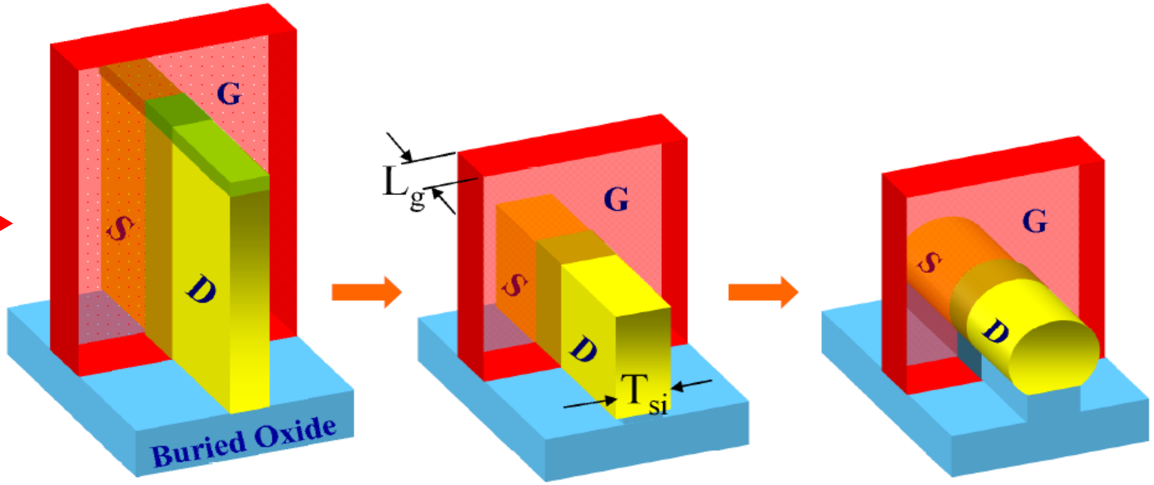
Planar → Fin→ Nanowire



Leakage current



Planar FET



Double-Gate FinFET (T_{si} = $^2/_3$ L_g)

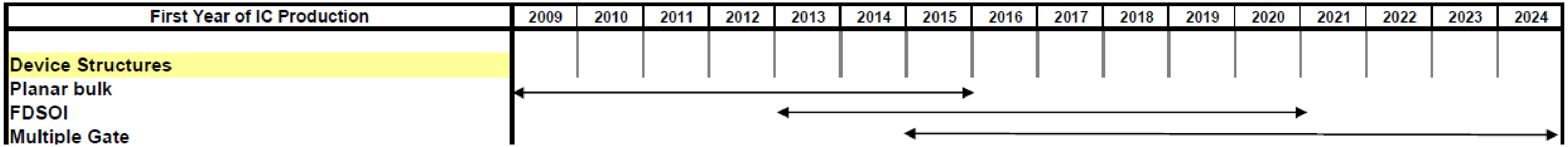
Omega FinFET (T_{si} = L_g)

Nanowire FinFET (T_{si} = $2L_g$)

Fin FET

Nanowire FET

Nanowire FET



2015

22 or 16nm node

Multiple Gate (Fin) FET

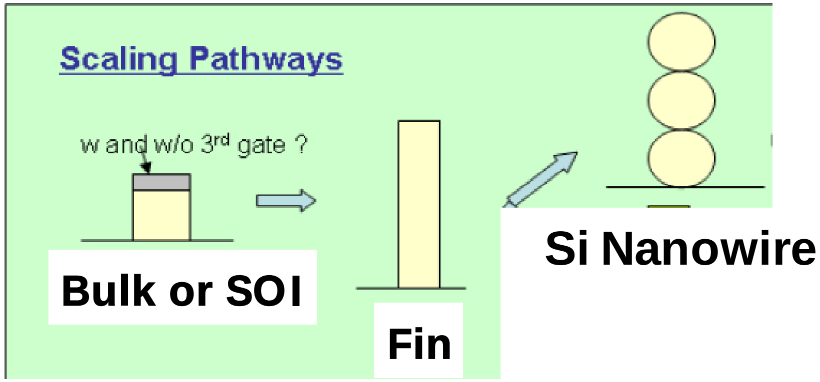
2020

11 or 8nm node

Nanowire FET

ITRS 2009

Bulk → Fin → Nanowire

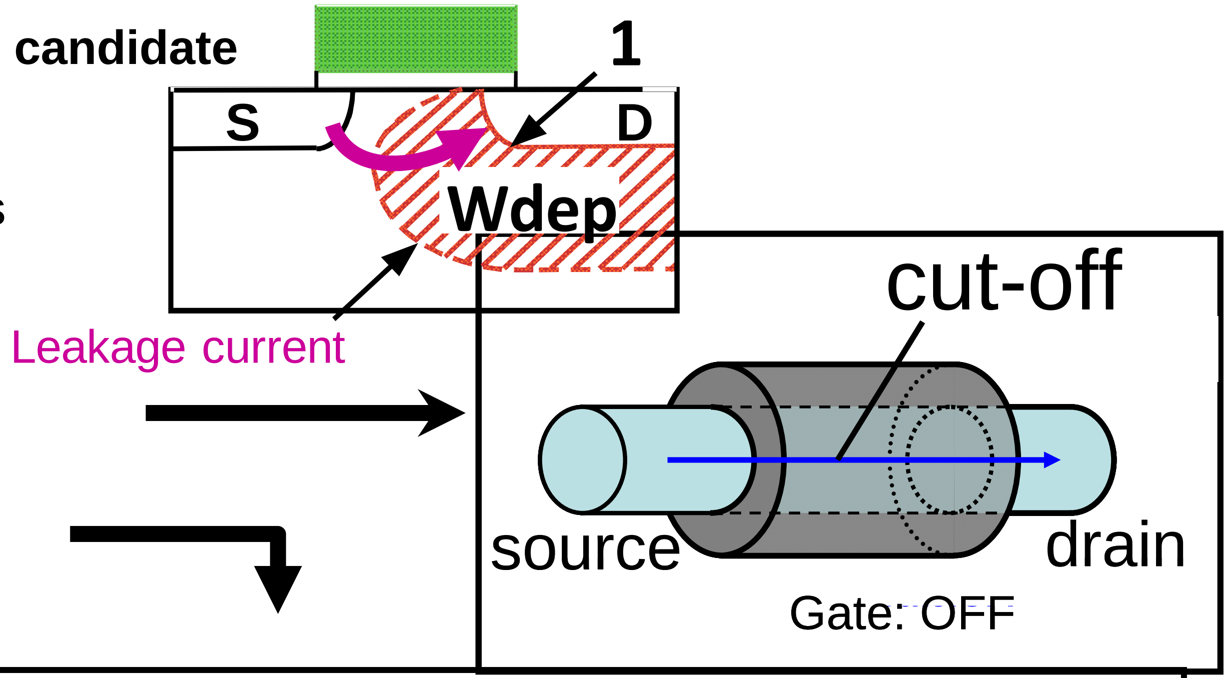


Si nanowire FET as a strong candidate

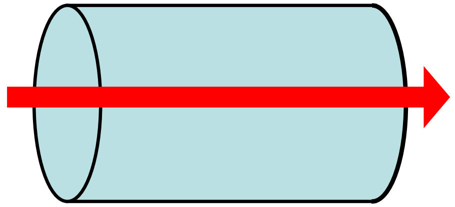
1. Compatibility with current CMOS process

2. Good controllability of I_{OFF}

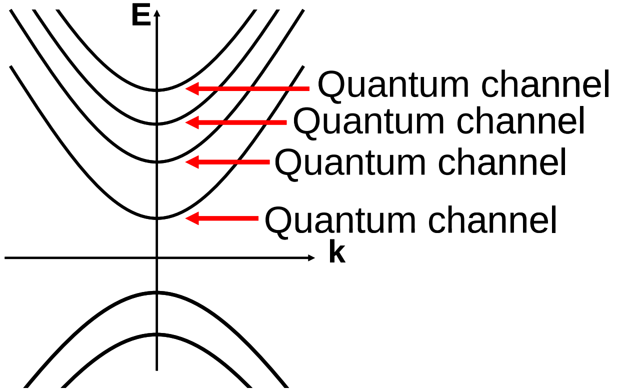
3. High drive current



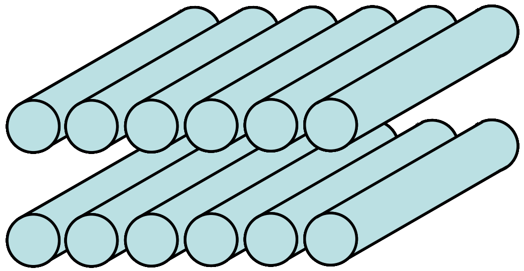
1D ballistic conduction



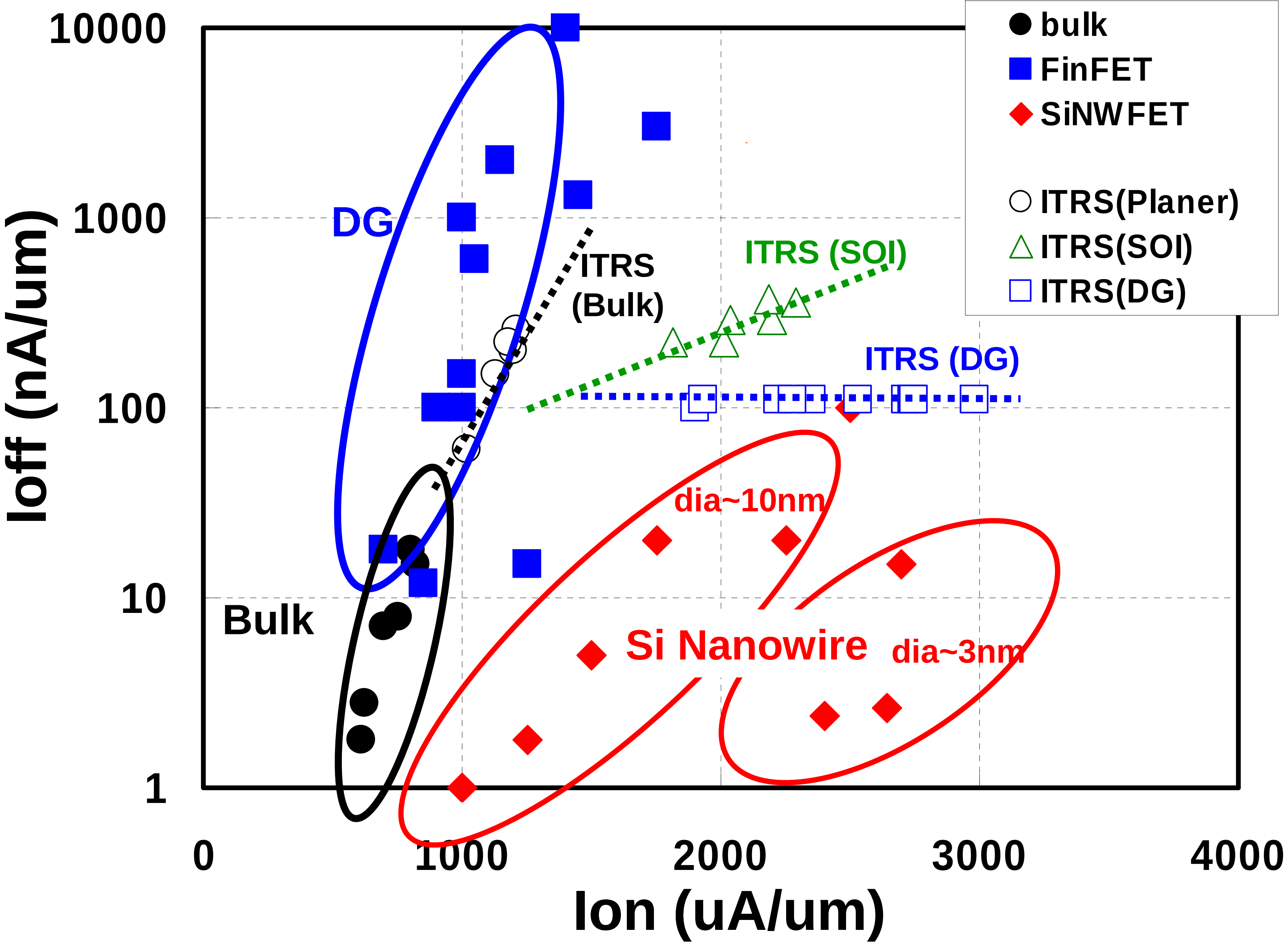
Multi quantum Channel



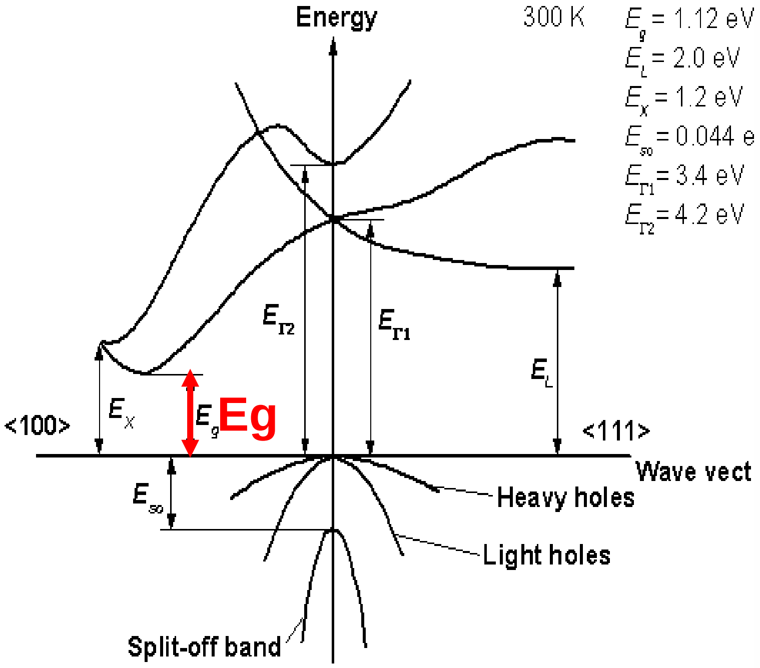
High integration of wires



Off Current

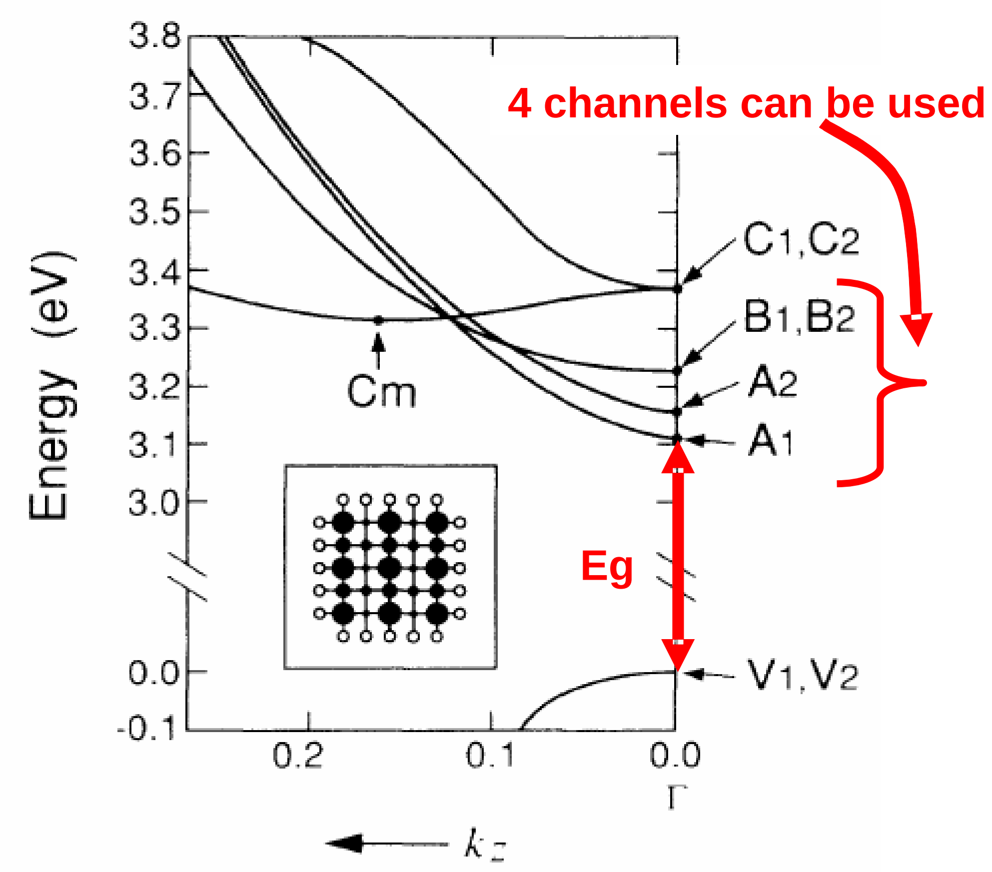

10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
● bulk
■ FinFET
◆ SiNWFET
○ ITRS(Planer)
△ ITRS(SOI)
□ ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
Bulk
dia~10nm
Si Nanowire
dia~3nm

Increase the Number of quantum channels



Energy band of Bulk Si

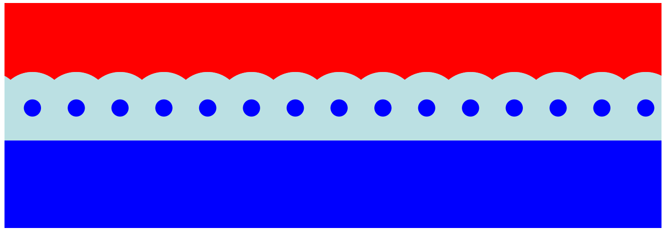
By Prof. Shiraishi of Tsukuba univ.



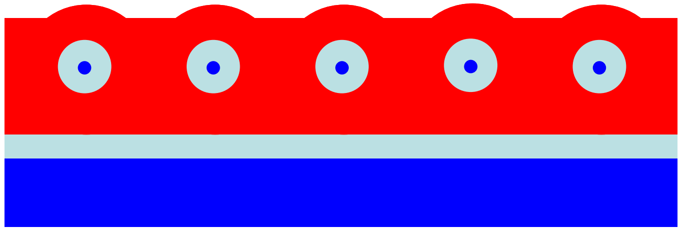
Energy band of 3 x 3 Si wire

Maximum number of wires per 1 µm

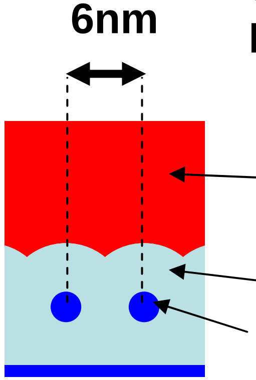
Front gate type MOS 165 wires /µm



Surrounded gate type MOS 33 wires/µm



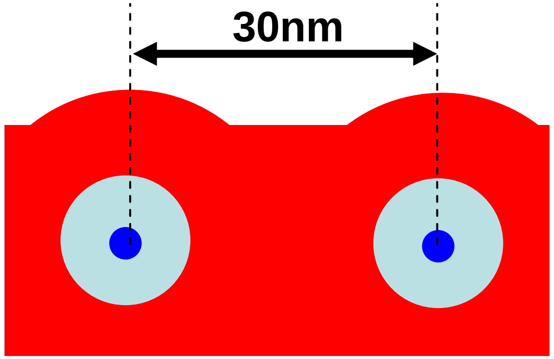
6nm pitch
By nano-imprint method



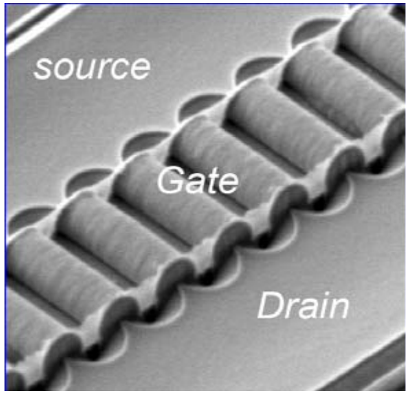
Metal gate electrode(10nm)

High-k gate insulator (4nm)

Si Nano wire (Diameter 2nm)



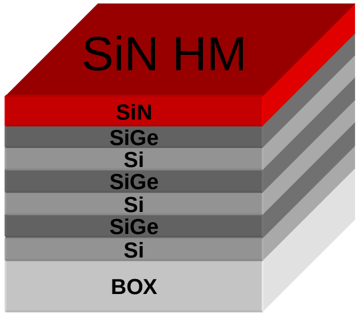
30nm pitch:
EUV lithograpy



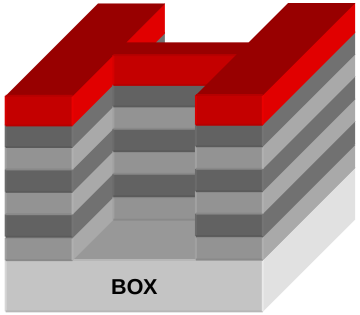
Surrounded gate MOS

Device fabrication

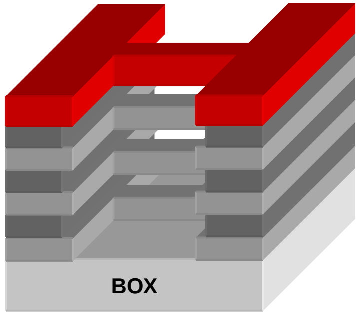
Si/$Si_{0.8}Ge_{0.2}$
superlattice
epitaxy on SOI



Anisotropic
etching
of these layers



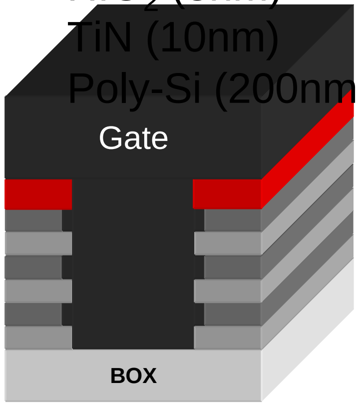
Isotropic
etching
of SiGe



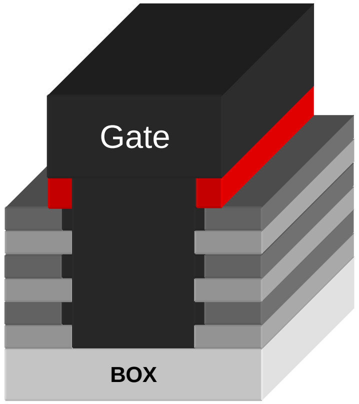
(The NW diameter
is controllable
down to 5 nm
by self limited oxidation.)

Gate depositions

HfO_2 (3nm)
TiN (10nm)
Poly-Si (200nm)



Gate etching

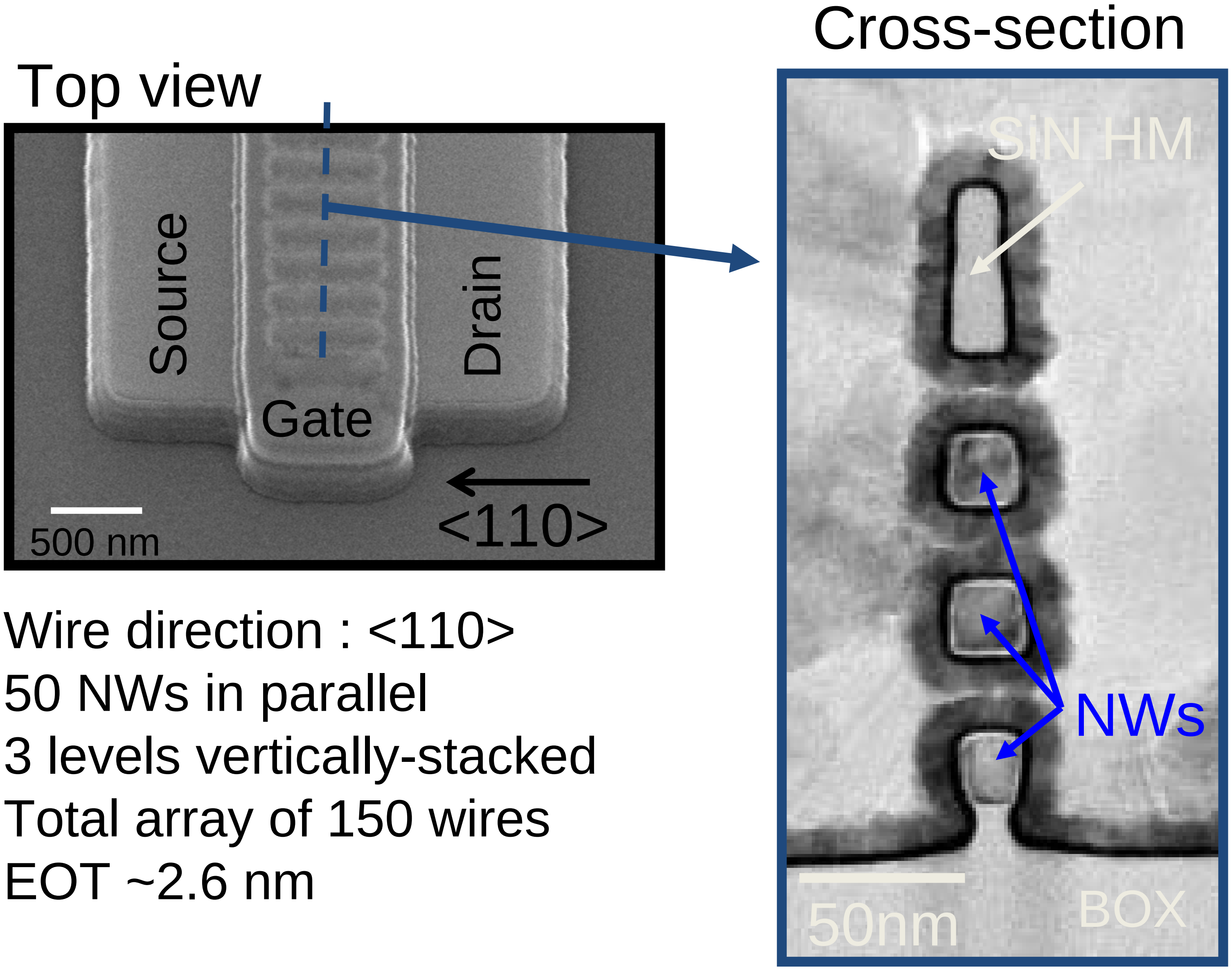


S/D implantation
Spacer formation
Activation anneal
Salicidation

Standard
Back-End
of-Line
Process

Process Details :
C. Dupre *et al.*,
IEDM Tech. Dig., p.749, 2008

3D-stacked Si NWs with Hi-*k*/MG

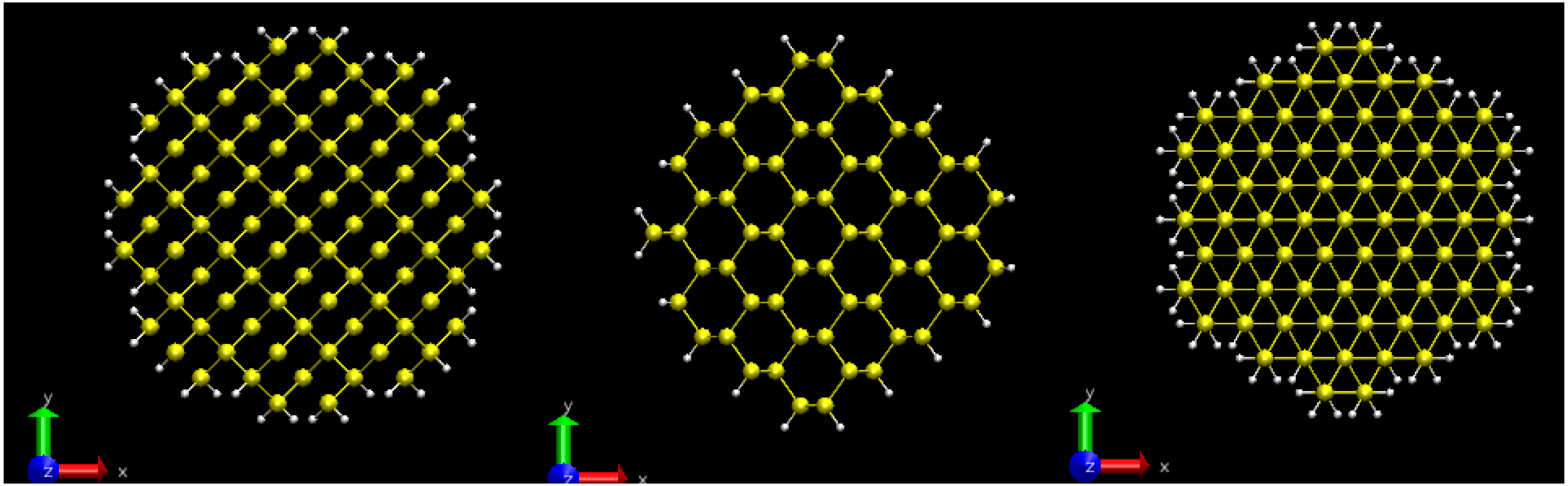


Wire direction : <110>
50 NWs in parallel
3 levels vertically-stacked
Total array of 150 wires
EOT ~2.6 nm

SiNW Band structure calculation

Cross section of Si NW

First principal calculation,

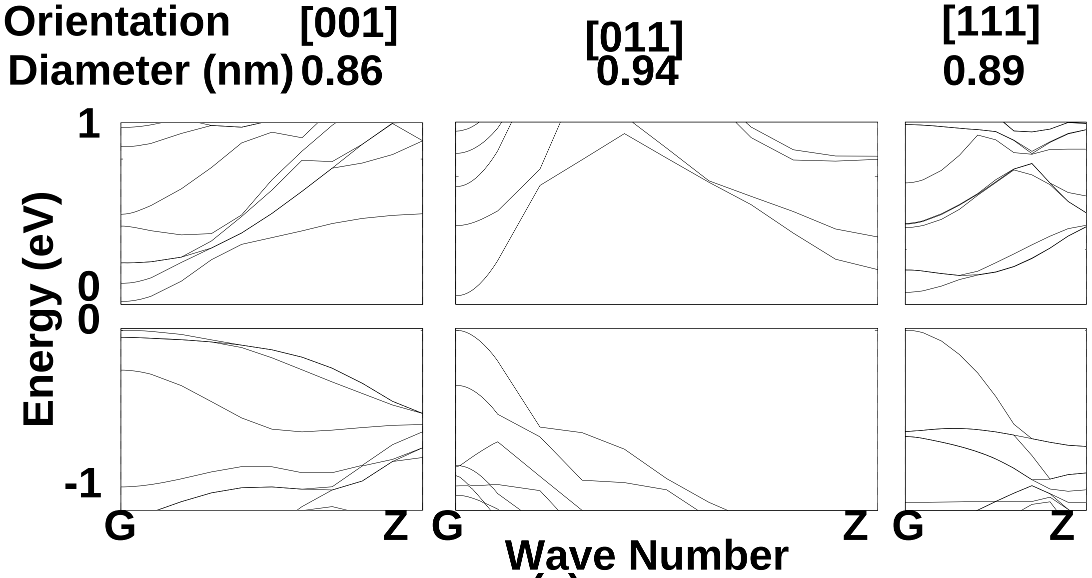


D=1.96nm
[001]

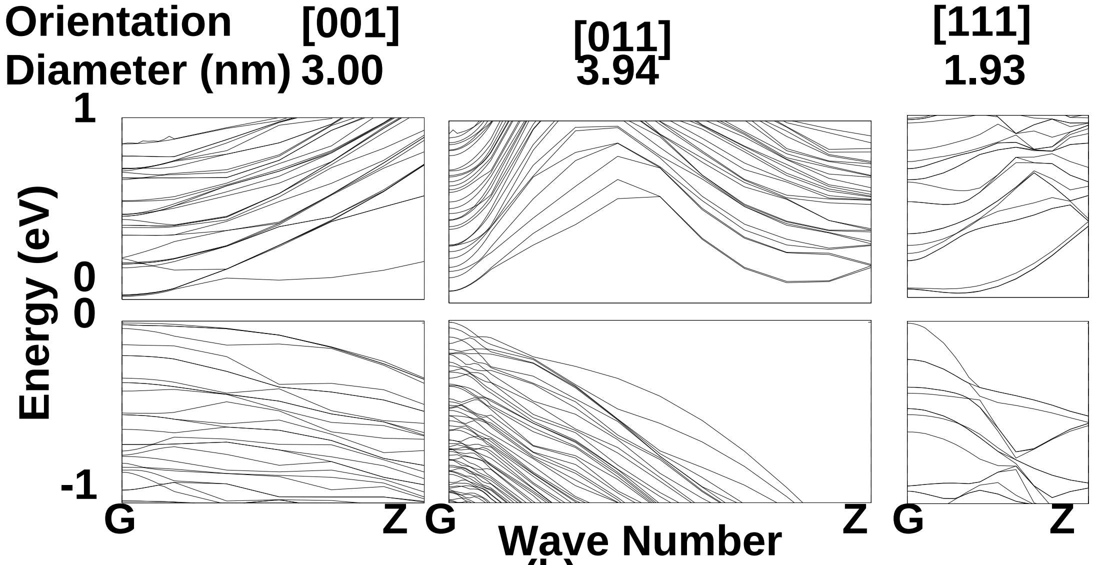
D=1.94nm
[011]

D=1.93nm
[111]

Si nanowire FET with 1D Transport



(a)

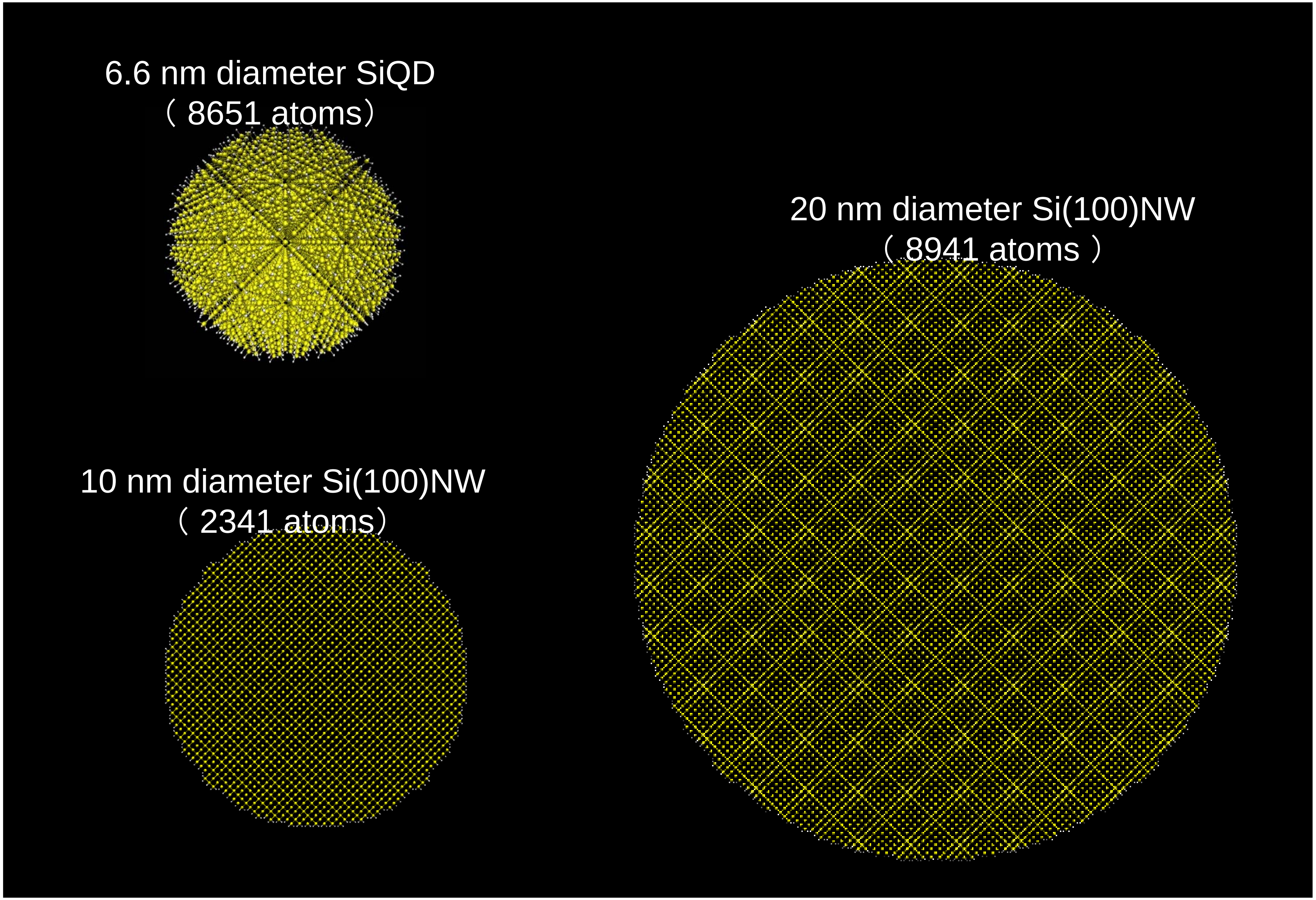


(b)

Small mass with [011]

Large number of quantum channels with [001]

Atomic models of a Si quantum dot and Si nanowires



RSDFT – suitable for parallel first-principles calculation -

✓Real-Space Finite-Difference
✓Sparse Matrix
✓FFT free (FFT is inevitable in the conventional plane-wave code)
✓MPI (Message Passing Interface) library

Higher-order finite difference pseudopotential method
J. R. Chelikowsky et al., Phys. Rev. B, (1994)

Kohn-Sham eq. (finite-difference)

$$\left(-\frac{1}{2}\nabla^2 + v_s[\rho](\mathbf{r}) + \hat{v}_{nloc}^{PP}(\mathbf{r})\right)\phi_n(\mathbf{r}) = \varepsilon_n\phi_n(\mathbf{r})$$

Higher-order finite difference

$$\frac{\partial^2}{\partial x^2}\psi_n(x,y,z) \approx \sum_{m=-6}^{6} C_m\psi_n(x+m\Delta x, y, z)$$

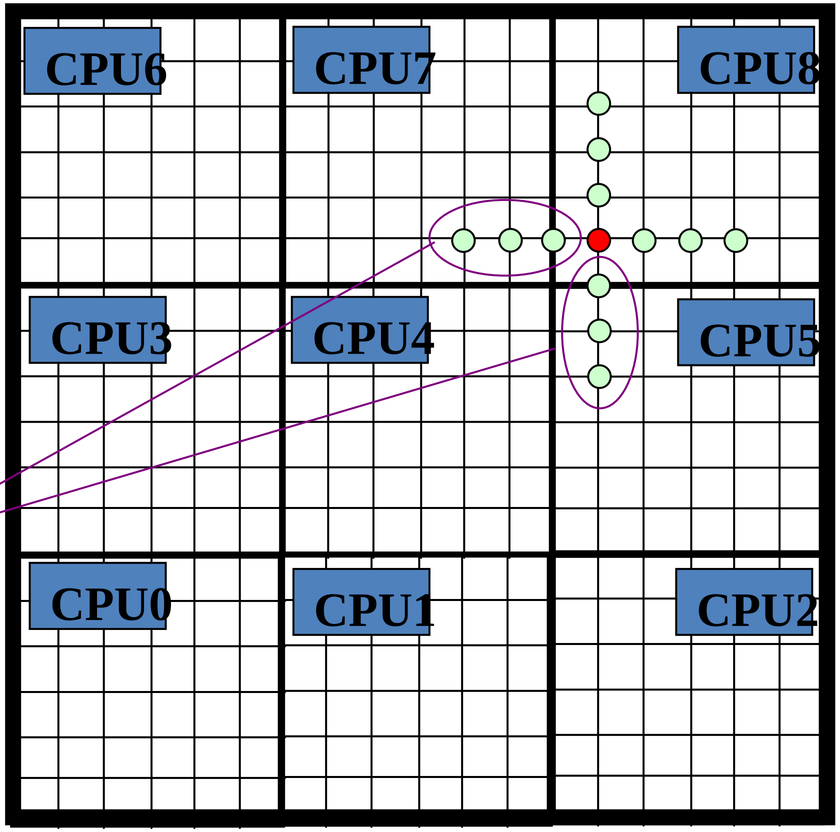
MPI_ISEND, MPI_IRECV

Integration

$$\int \psi_m(\mathbf{r})\psi_n(\mathbf{r})d\mathbf{r} \approx \sum_{i=1}^{Mesh}\psi_m(\mathbf{r}_i)\psi_n(\mathbf{r}_i)\Delta x\Delta y\Delta z$$

MPI_ALLREDUCE

3D grid is divided by several regions
for parallel computation.



Massively Parallel Computing

with our recently developed code “RSDFT”

Iwata et al, J. Comp. Phys., to be published

Real-Space Density-Functional Theory code (RSDFT)

Based on the finite-difference pseudopotential method (J. R. Chelikowsky et al., PRB1994)

Highly tuned for massively parallel computers

Computations are done on a massively-parallel cluster **PACS-CS** at University of Tsukuba.

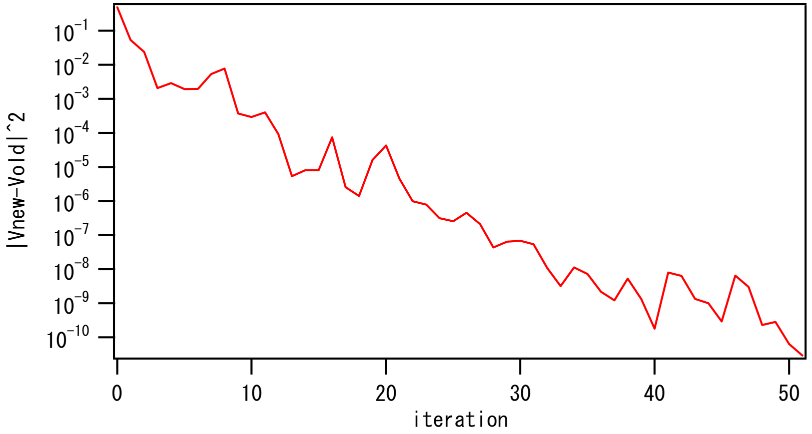
(Theoretical Peak Performance = 5.6GFLOPS/node)

e.g.) The system over 10,000 atoms → $Si_{10701}H_{1996}$

(7.6 nm diameter Si dot)

Convergence behavior for $Si_{10701}H_{1996}$

Grid points = 3,402,059
Bands = 22,432

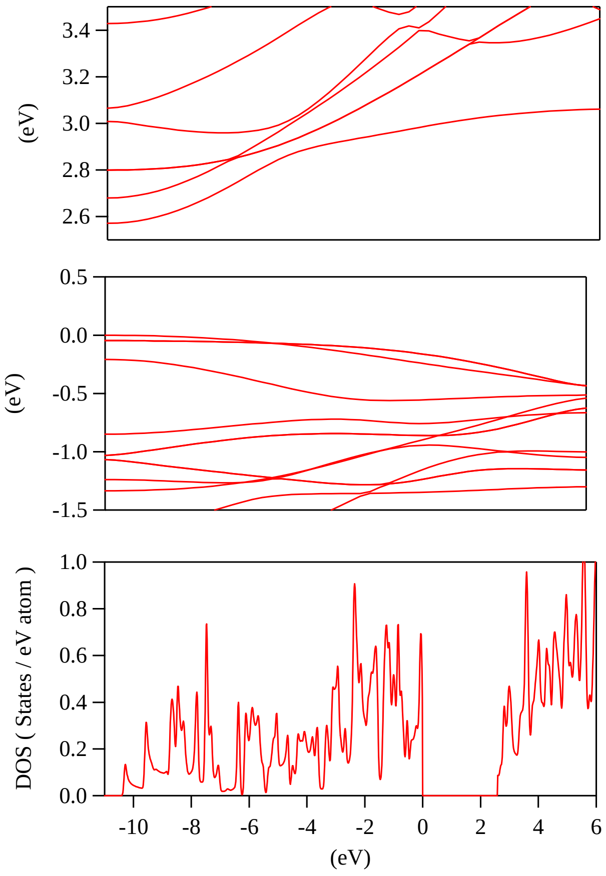


Computational Time (with 1024 nodes of PACS-C

6781 sec. × 60 iteration step = 113 hour

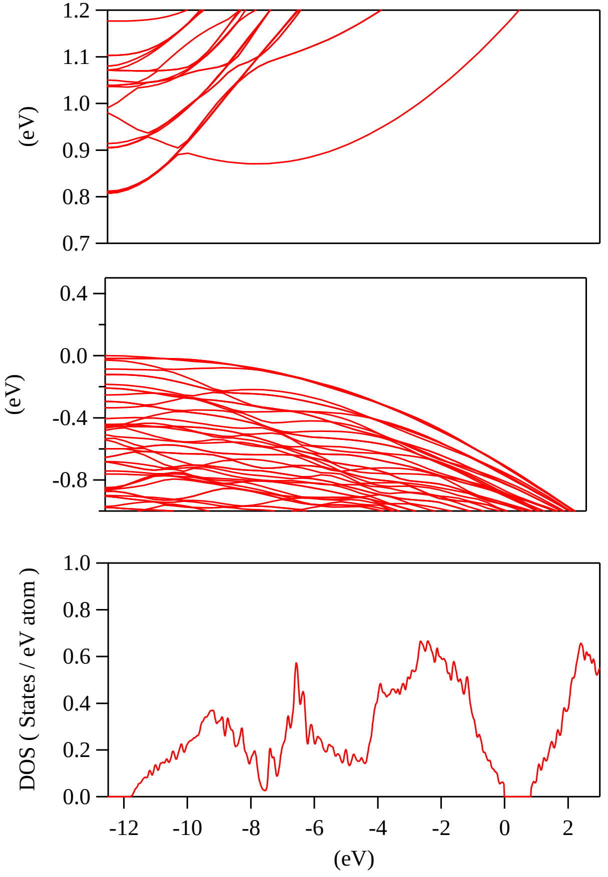
Band Structure and DOS of Si(100)NWs (D=1nm, 4nm, and 8nm)

D=1nm



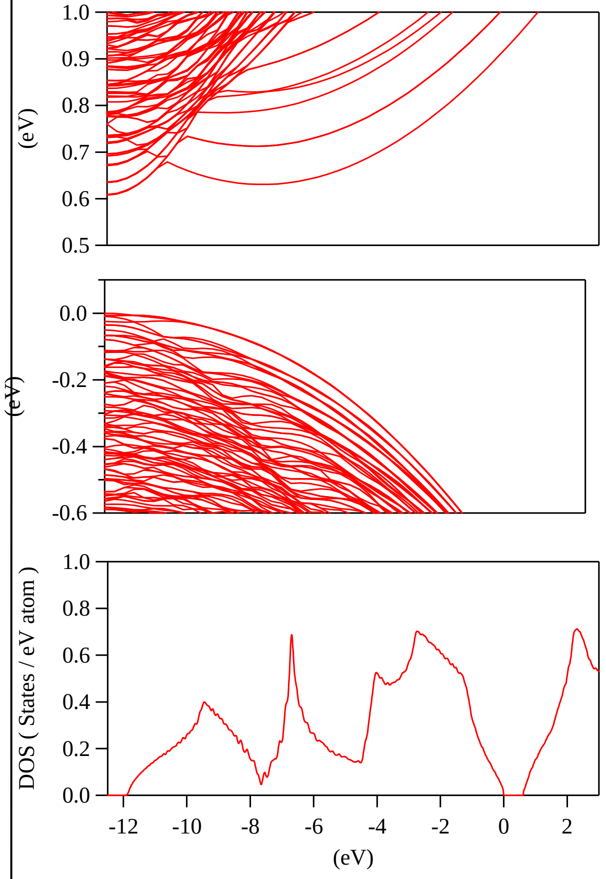
D=1 nm
Si21H20（41 atoms)
KS band gap=2.60eV

D=4nm



D = 4 nm
Si341H84（425 atoms)
KS band gap = 0.81eV

D=8nm

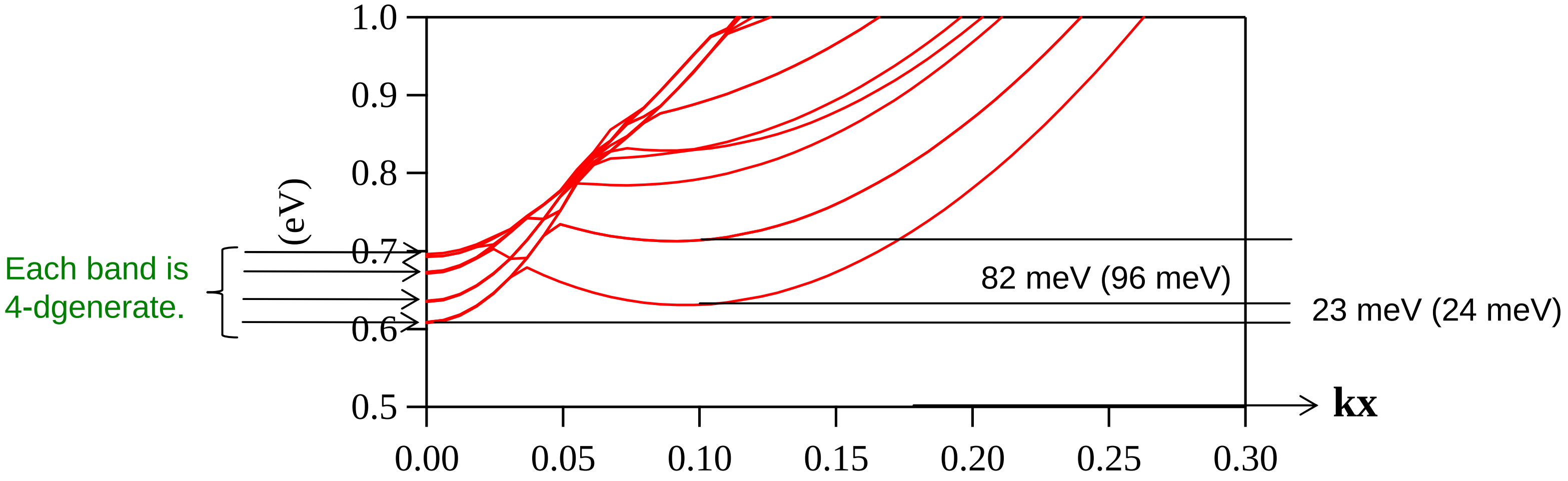


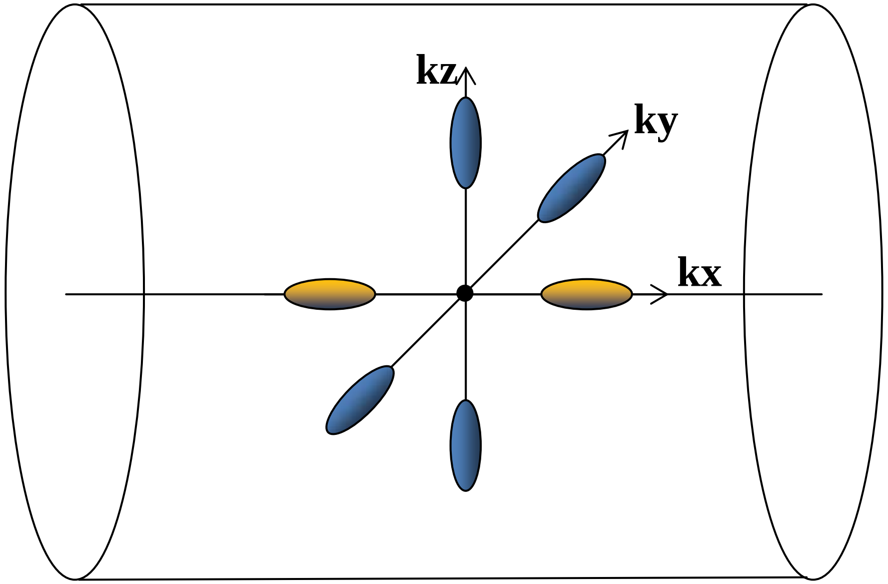
D=8 nm
Si1361H164 (1525 atoms)
KS band gap=0.61eV

KS band gap of bulk (LDA) = 0.53eV

Band structure of 8-nm-diameter Si nanowire near the CBM

- KS band gap = 0.608 eV (@Γ)



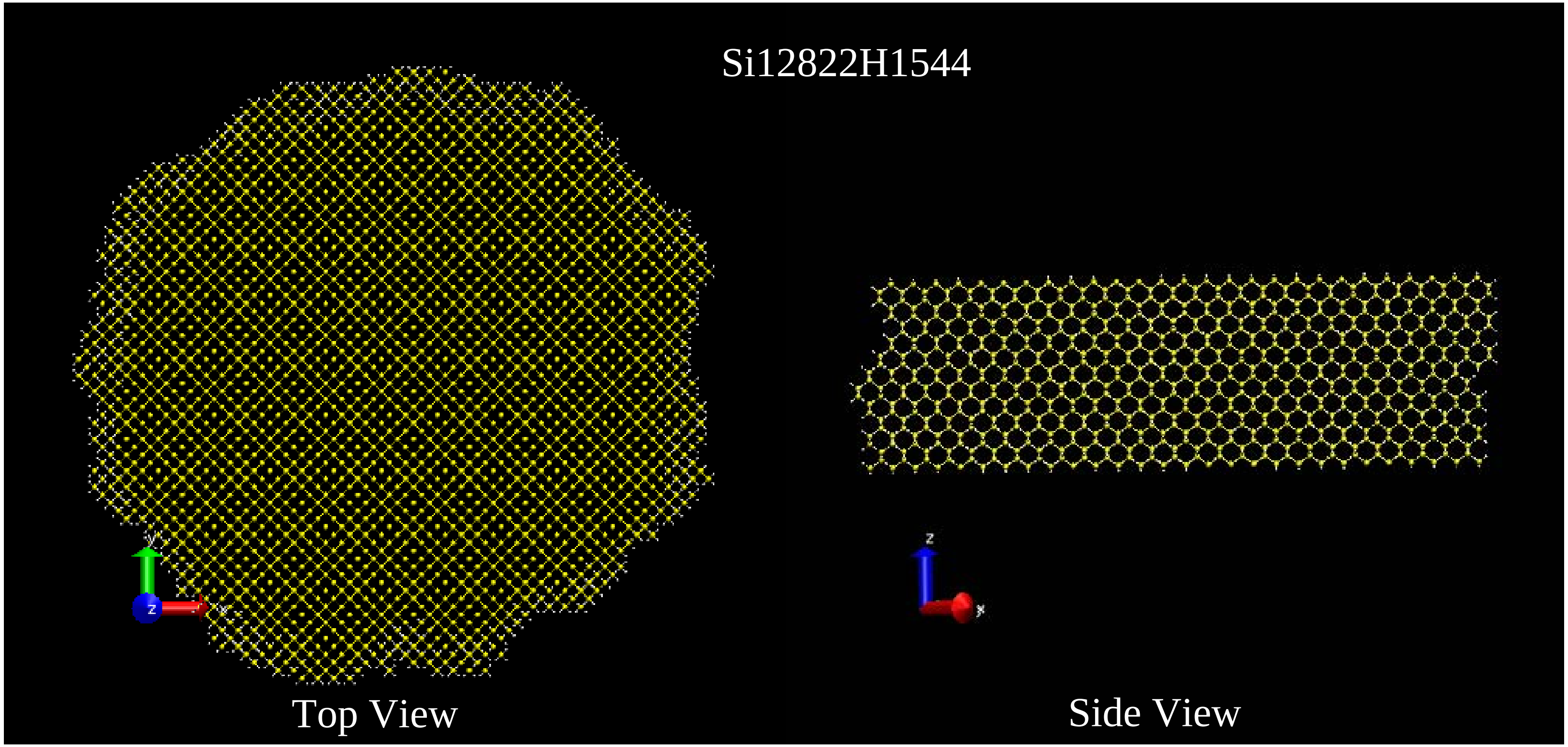


Effective mass equation

$$\left[-\frac{\hbar^2}{2m_t^*}\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}\right)-\frac{\hbar^2}{2m_l^*}\frac{\partial^2}{\partial z^2}\right]\Phi(\mathbf{r})=(\varepsilon-\varepsilon_{CBM})\Phi(\mathbf{r})$$

The band structure can be understood that electrons near the CBM in the bulk Si are Confined within a cylindrical geometry.

Si nano wire with surface roughness

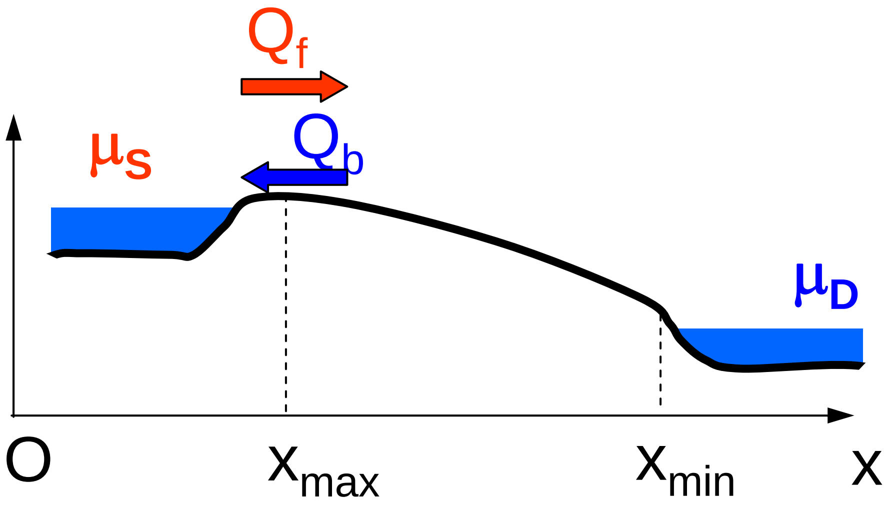


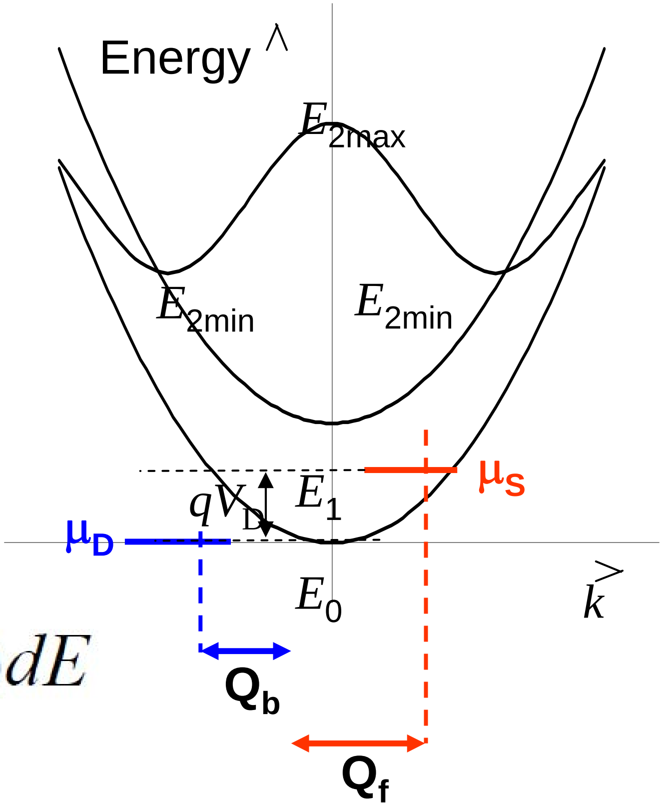
Si12822H1544（14,366 atoms）

- 10nm diameter、3.3nm height、(100)
- Grid spacing : 0.45Å (~14Ry)
- # of grid points : 4,718,592
- # of bands : 29,024
- Memory : 1,022GB～2,044GB

SiNW Band compact model

Landauer Formalism for Ballistic FET



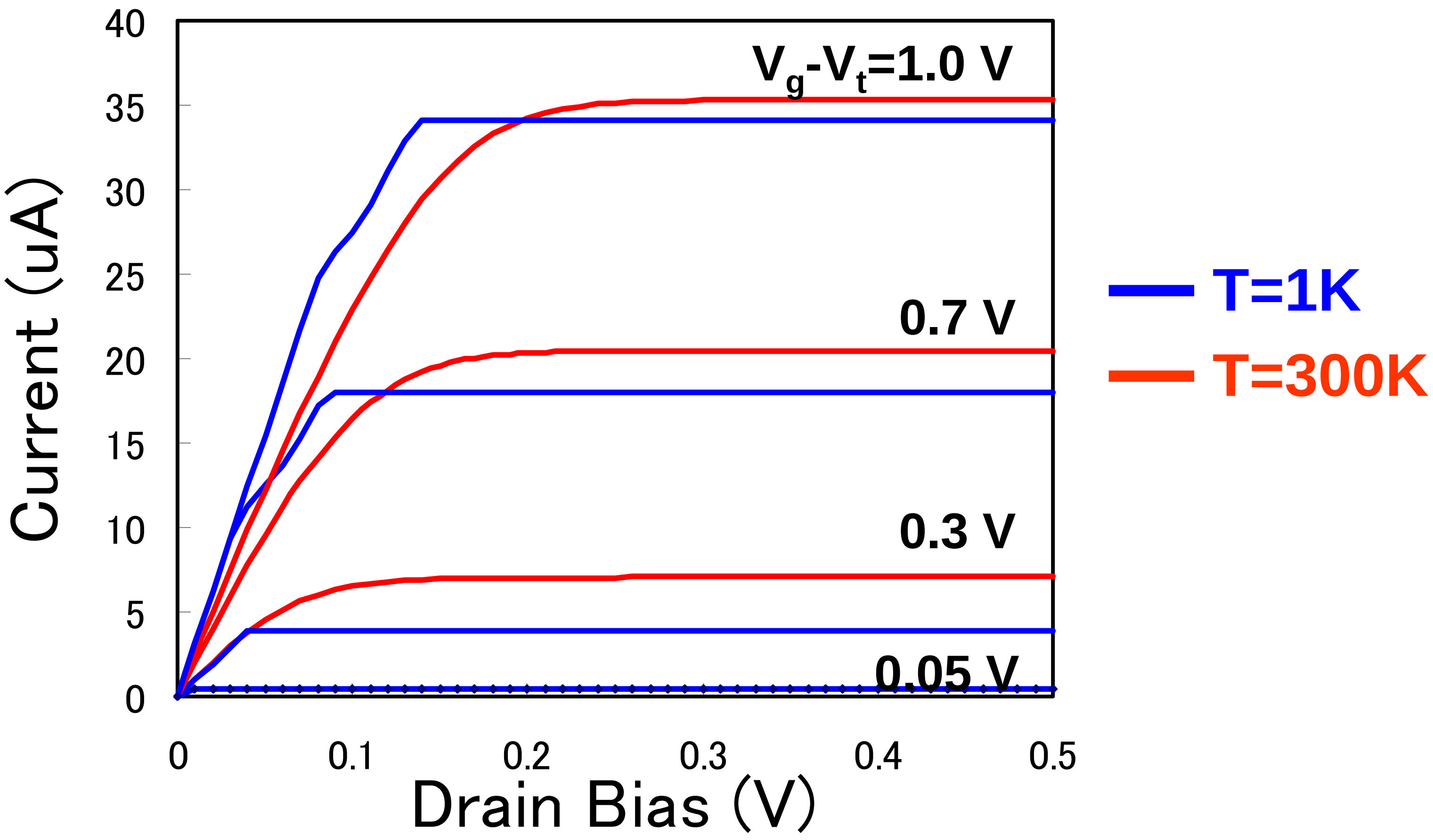


$$I_D = \frac{q}{\pi\hbar}\sum_i \int \left[f(E,\mu_S) - f(E,\mu_D)\right] T_i(E)\,dE$$

From x_{max} to x_{min} $\quad T_i(E) \approx 1$

$$\boxed{I_D = G_0\left(\frac{k_B T}{q}\right)\sum_i g_i \ln\left\{\frac{1+\exp\left[(\mu_S - E_{i0})/k_B T\right]}{1+\exp\left[(\mu_D - E_{i0})/k_B T\right]}\right\}}$$

IV Characteristics of Ballistic SiNW FET

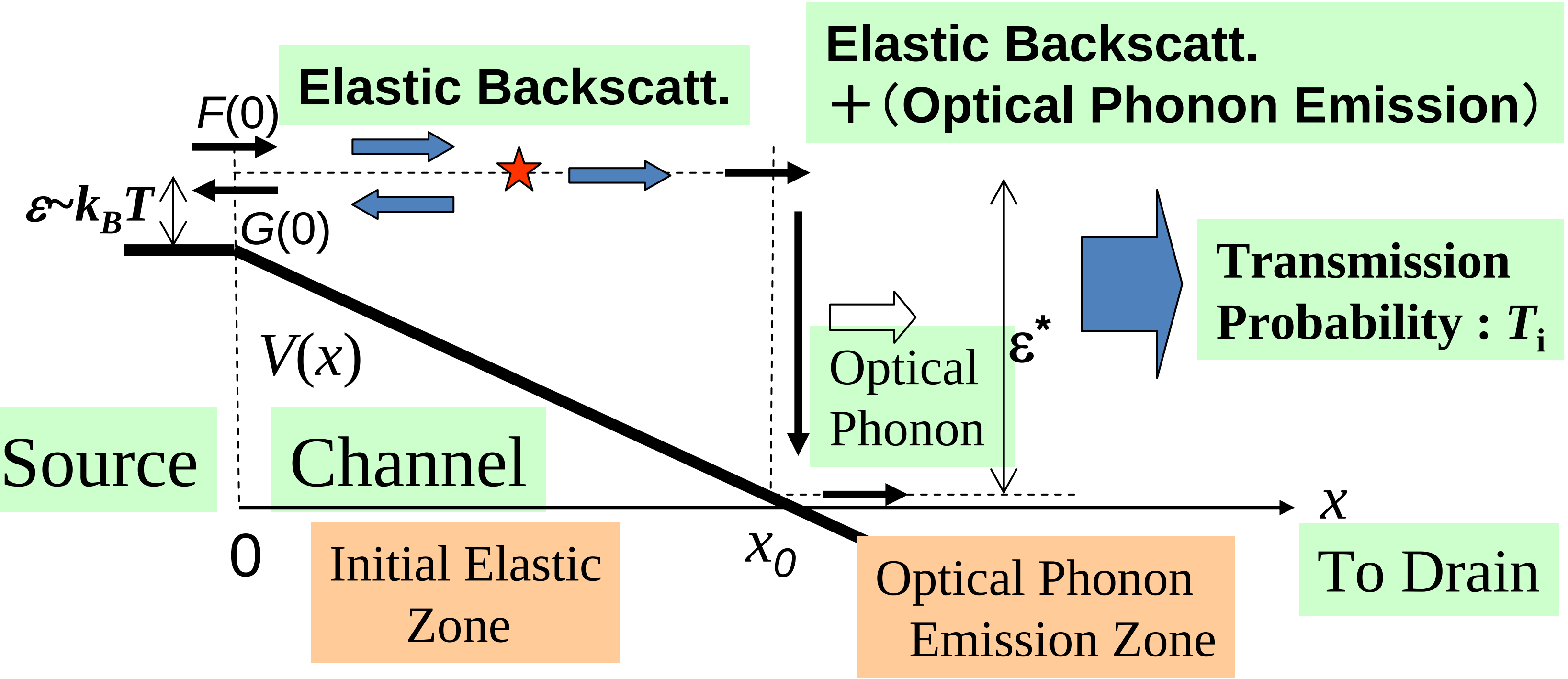


Small temperature dependency

35μA/wire for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx. :　Electric Field　*E*



$F(0)$

Elastic Backscatt.

Elastic Backscatt.
＋（Optical Phonon Emission）

$\varepsilon \sim k_B T$

$G(0)$

$V(x)$

Optical
Phonon

ε^*

Transmission
Probability : T_i

Source

Channel

x

0

Initial Elastic
Zone

x_0

Optical Phonon
Emission Zone

To Drain

Transmission
Probability
to Drain

$$T(\varepsilon) = \left.\frac{F(0) - G(0)}{F(0)}\right)_{\text{Injection from Drain}=0}$$

Résumé of the Compact Model

$$I = \frac{q}{\pi\hbar}\sum_i g_i \int \left[f(\varepsilon,\mu_s) - f(\varepsilon,\mu_D) \right] T_i \, d\varepsilon$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left\{ \frac{\sqrt{2r+t_{ox}}+\sqrt{t_{ox}}}{\sqrt{2r+t_{ox}}-\sqrt{t_{ox}}} \right\}}.$$

Planar Gate

$$(V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{\left| Q_f + Q_b \right|}{C_G}.$$

$$\mu_S - \mu_D = qV_D$$

(Electrostatics requirement)

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left(\frac{r+t_{ox}}{r} \right)}.$$

GAA

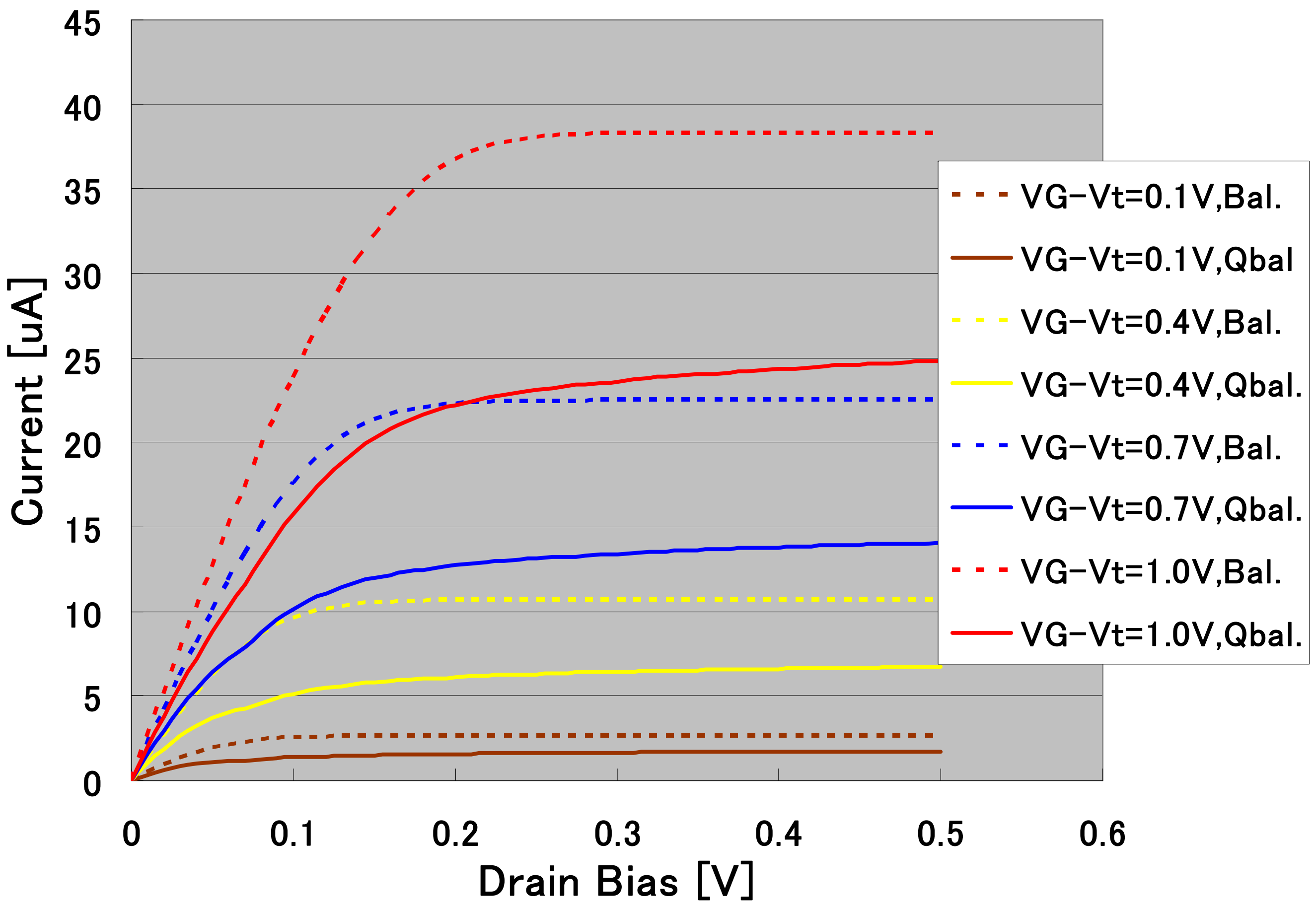
$$\left| Q_f + Q_b \right| = \frac{q}{\pi}\sum_i \; g_i \left[\int_{-\infty}^{\infty} \frac{dk}{1+\exp\left\{ \frac{\varepsilon_i(k)-\mu_S}{k_B T} \right\}} - \int_{-\infty}^{0} \left\{ \frac{1}{1+\exp\left\{ \frac{\varepsilon_i(k)-\mu_S}{k_B T} \right\}} - \frac{1}{1+\exp\left\{ \frac{\varepsilon_i(k)-\mu_D}{k_B T} \right\}} \right\} T_i(\varepsilon_i(k)) dk \right]$$

$$T(\varepsilon) = \frac{\sqrt{2D_0}\, qE}{\left(\sqrt{B_0+D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0}\, B_0 \ln\left(\frac{qEx_0 + \varepsilon}{\varepsilon} \right)}$$

(Carrier distribution in Subbands)

Unknowns are I_D, $(\mu_S-\mu_0)$, $(\mu_D-\mu_0)$, (Q_f+Q_b)

I-V_D Characteritics (RT)

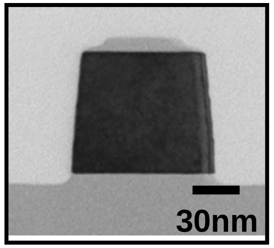


- ☐ **Electric current 20～25 μA**
- ☐ **No satruration at Large V_D**

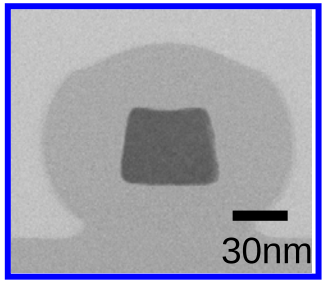
SiNW FET Fabrication

SiNW FET Fabrication

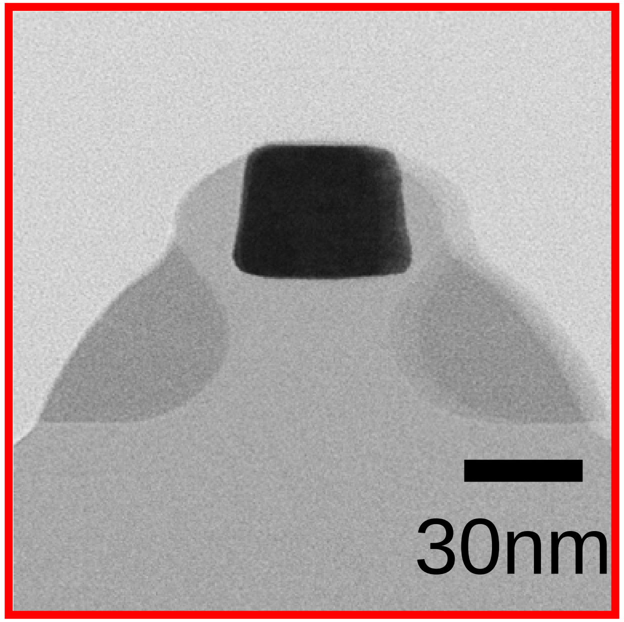
- S/D & Fin Patterning



- Sacrificial Oxidation



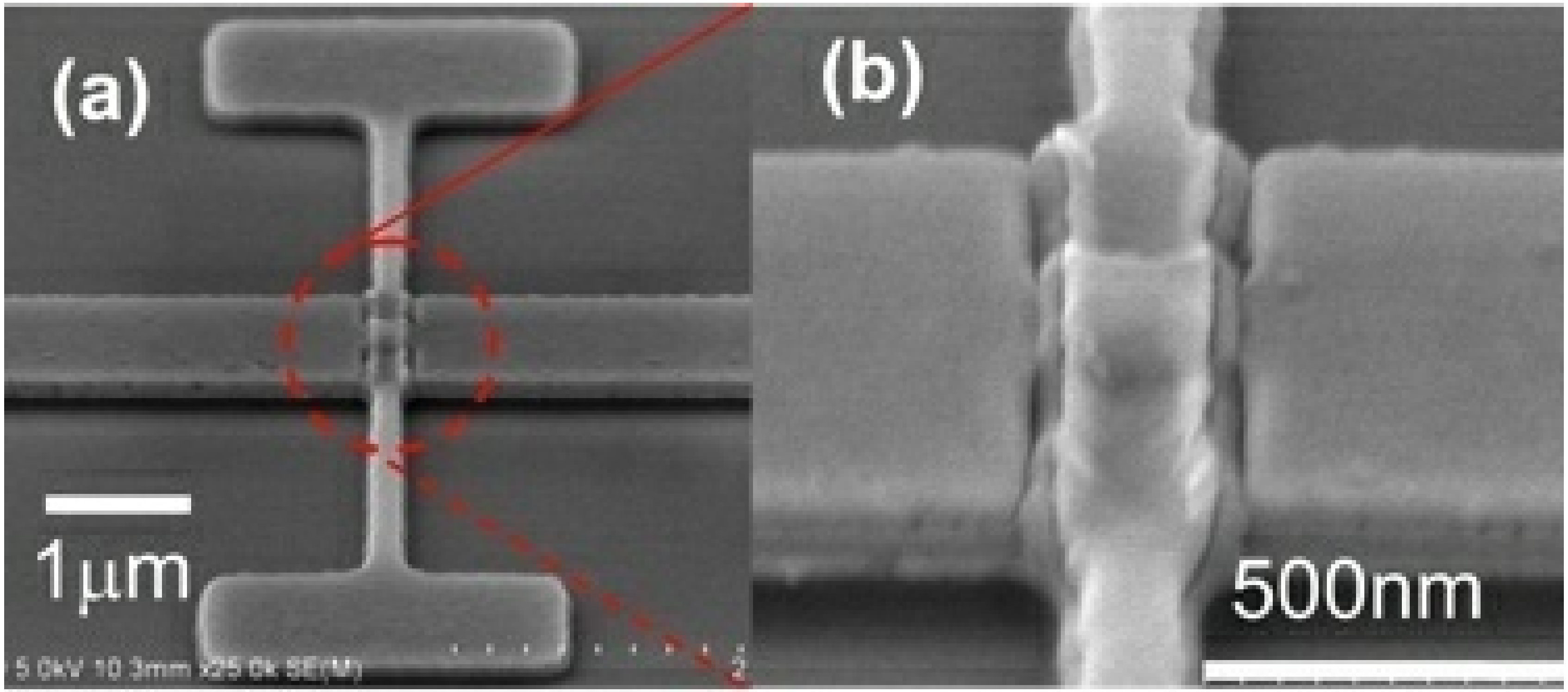
- Oixde etch back
- SiN sidewall support formation



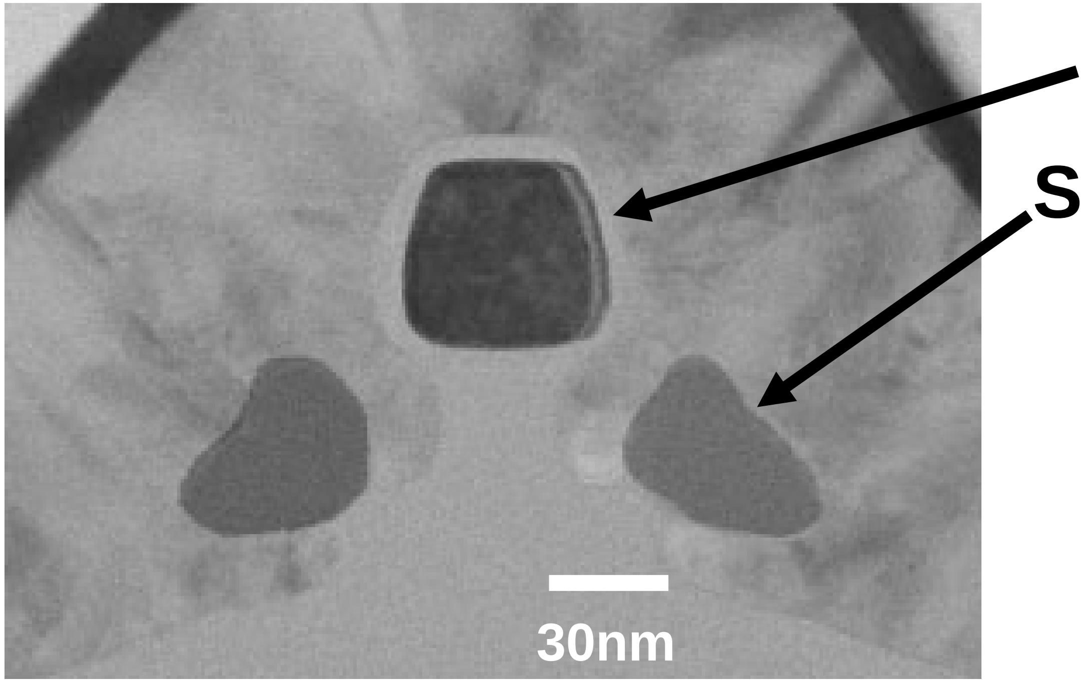
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

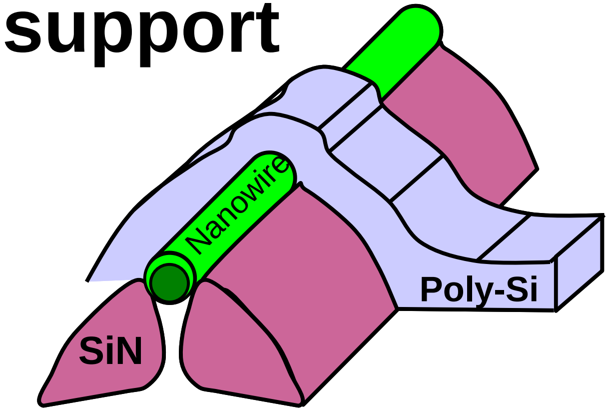
Standard recipe for gate stack formation

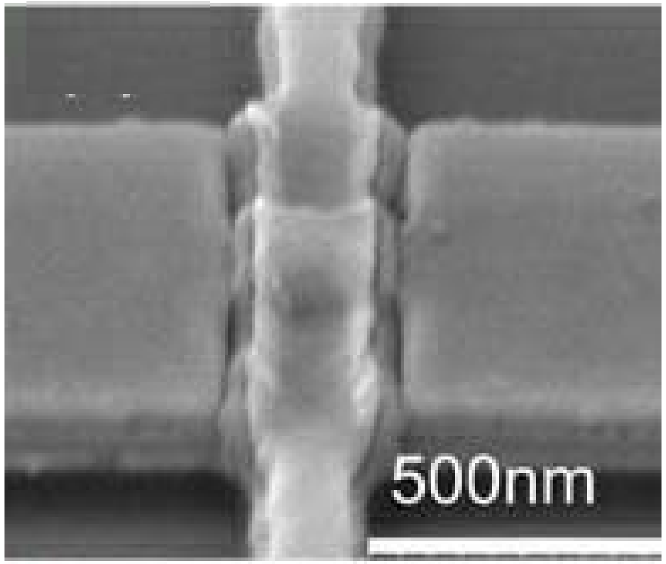
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.



Fabricated SiNW FET

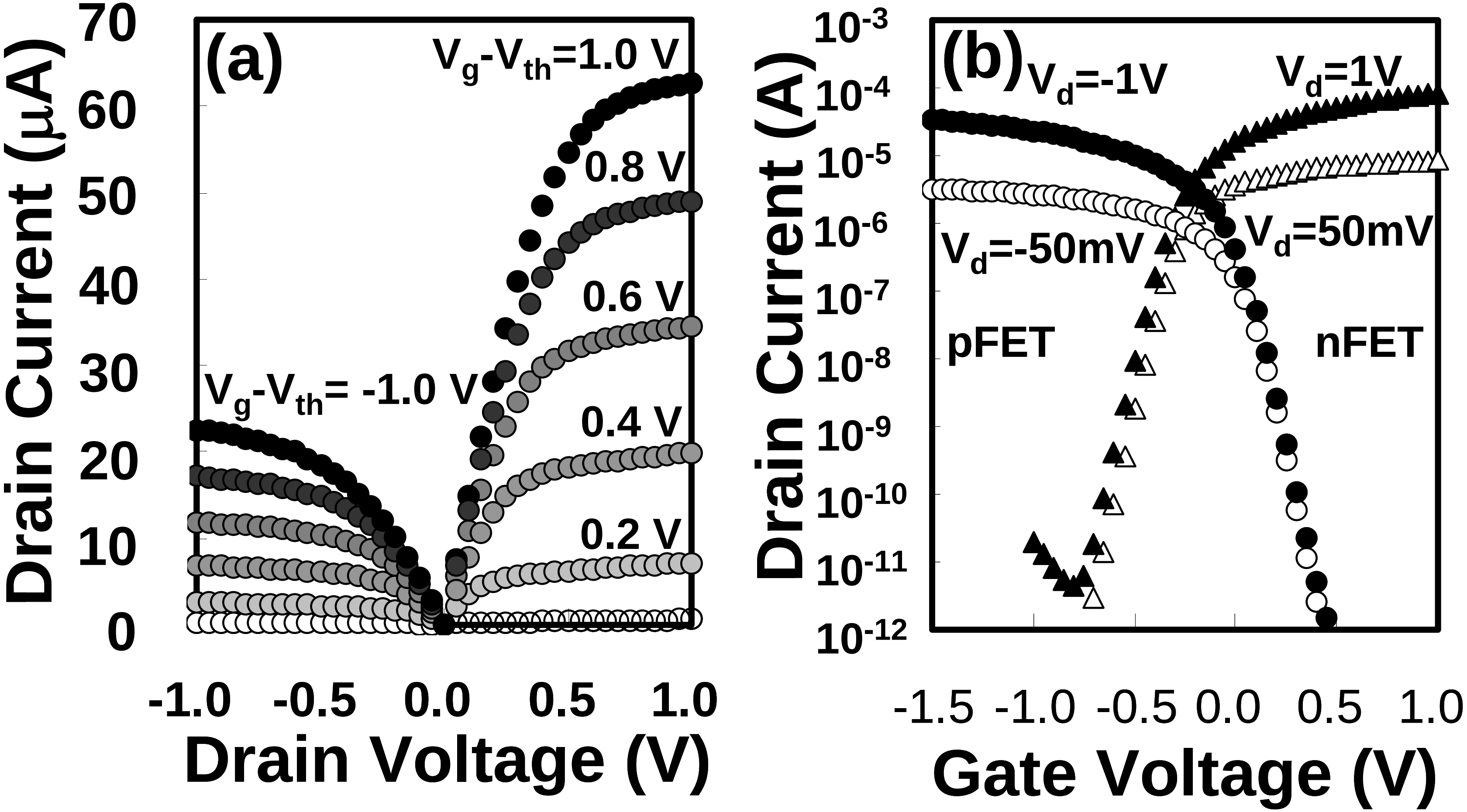






Recent results to be presented by ESSDERC 2010 next week in Sevile

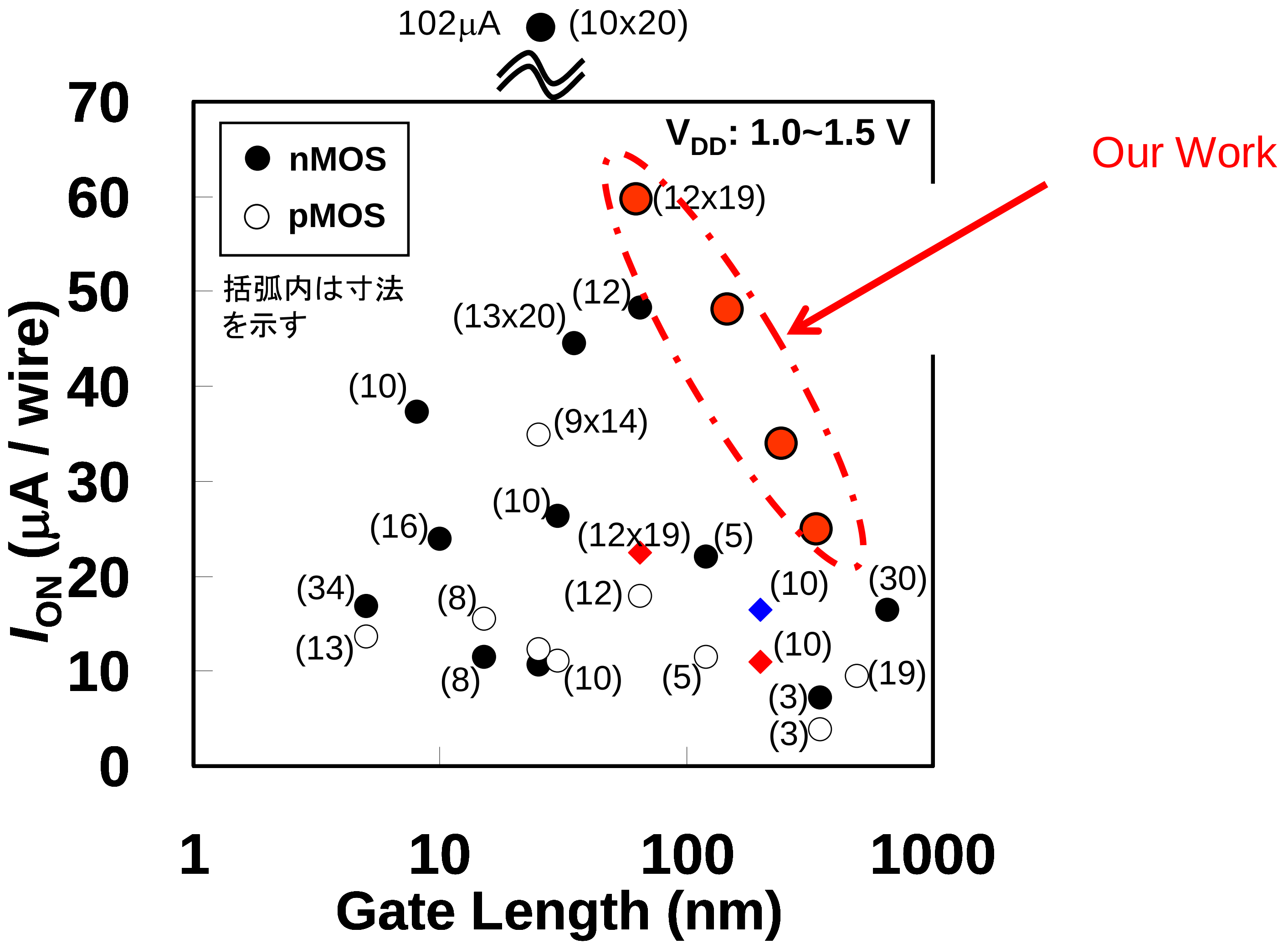
Wire cross-section: 20 nm X 10 nm



On/Off>10^6、60uA/wire

L_g=65nm, T_{ox}=3nm

Bench Mark



括弧内は寸法を示す

Our Work

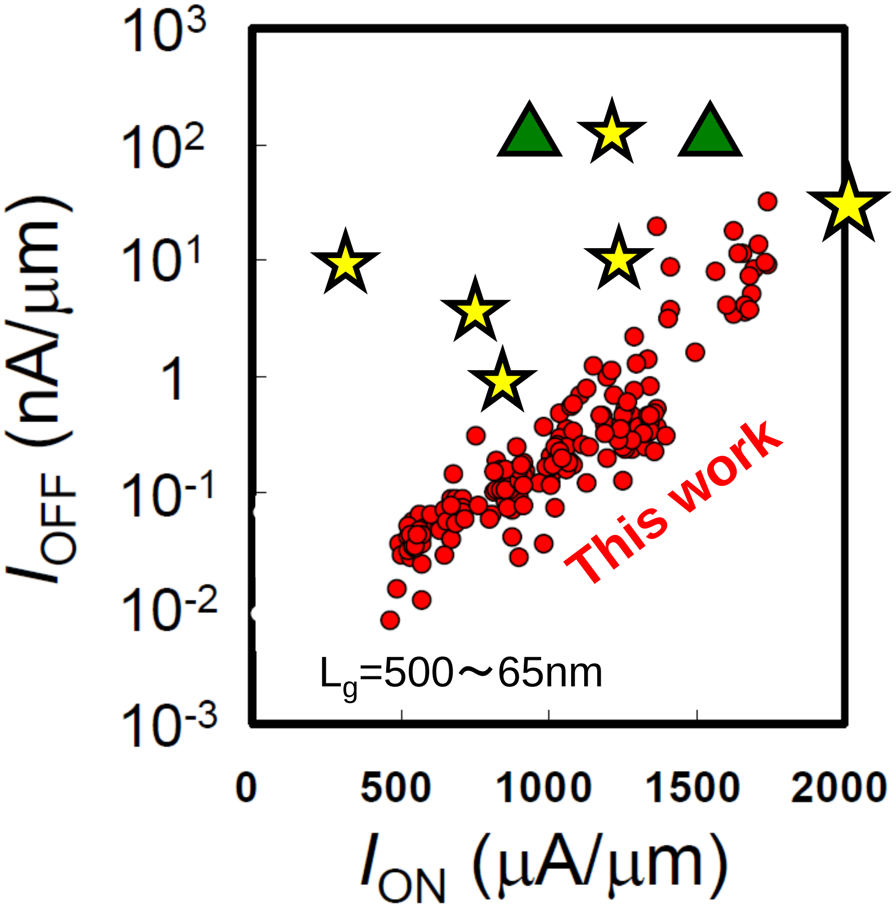
Bench Mark

	This work	Ref[11]	Ref[12]	Ref[13]	Ref[14]	Ref[15]	Ref[4]
NW Cross-section (nm)	Rect.	Rect.	Rect.	Cir.	Cir.	Elliptical	Elliptical
NW Size (nm)	10x20	10x20	14	10	10	12	13x20
Lg (nm)	65	25	100	30	8	65	35
EOT or Tox (nm)	3	1.8	1.8	2	4	3	1.5
Vdd (V)	1.0	1.1	1.2	1.0	1.2	1.2	1.0
Ion(uA) per wire	60.1	102	30.3	26.4	37.4	48.4	43.8
Ion(uA/um) by dia.	3117	5010	2170	2640	3740	4030	2592
Ion(uA/um) by cir.	1609	2054	430	841	1191	1283	825
SS (mV/dec.)	70	79	68	71	75	~75	85
DIBL (mV/V)	62	56	15	13	22	40-82	65
Ion/Ioff	~1E6	>1E6	>1E5	~1E6	>1E7	>1E7	~2E5

Ref[11] by Stmicro Lg=25nm,Tox=1.8nm

This work Lg=65nm,Tox=3nm

I_{ON}/I_{OFF} Bench mark

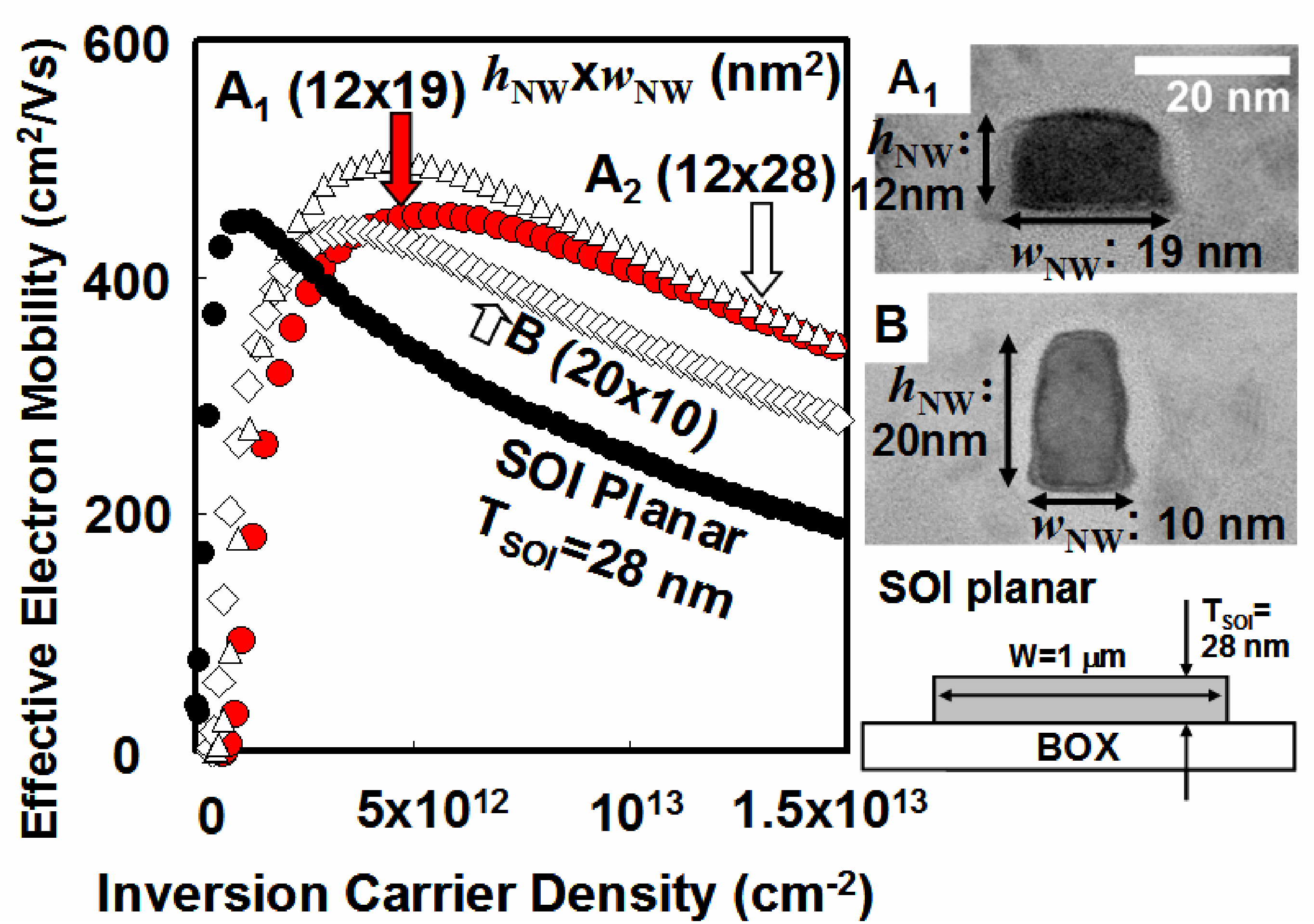


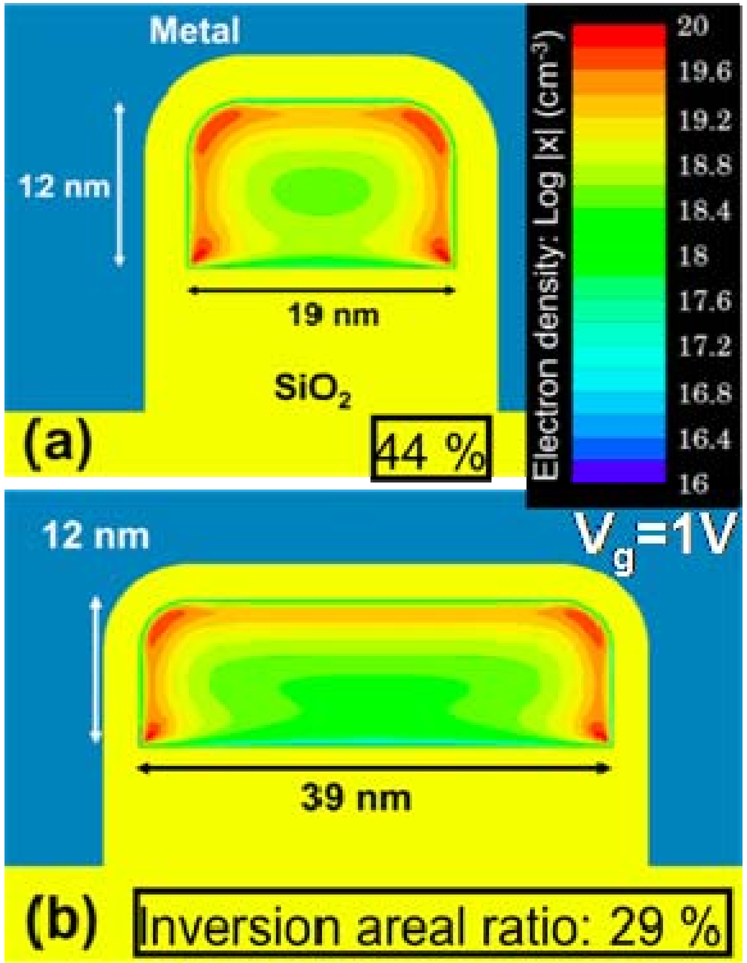
Planer FET ▲ 1.0～1.1V

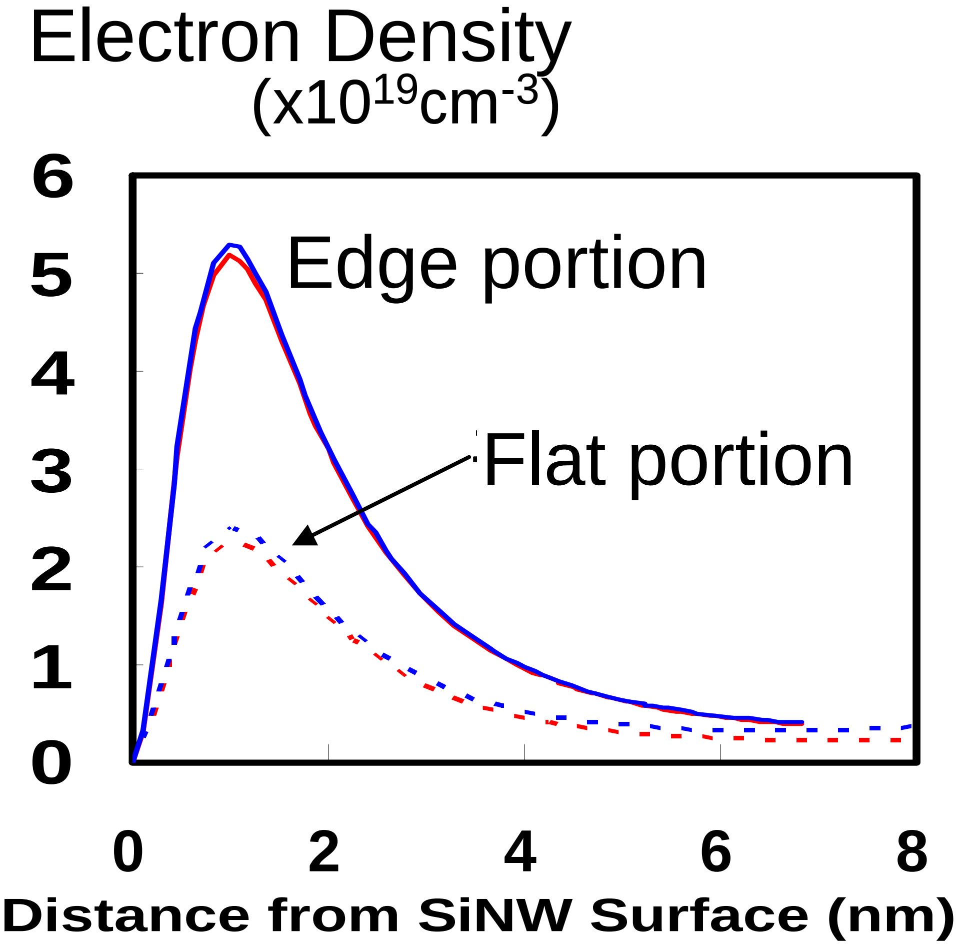
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

SiナノワイヤFET ★ 1.2～1.3V

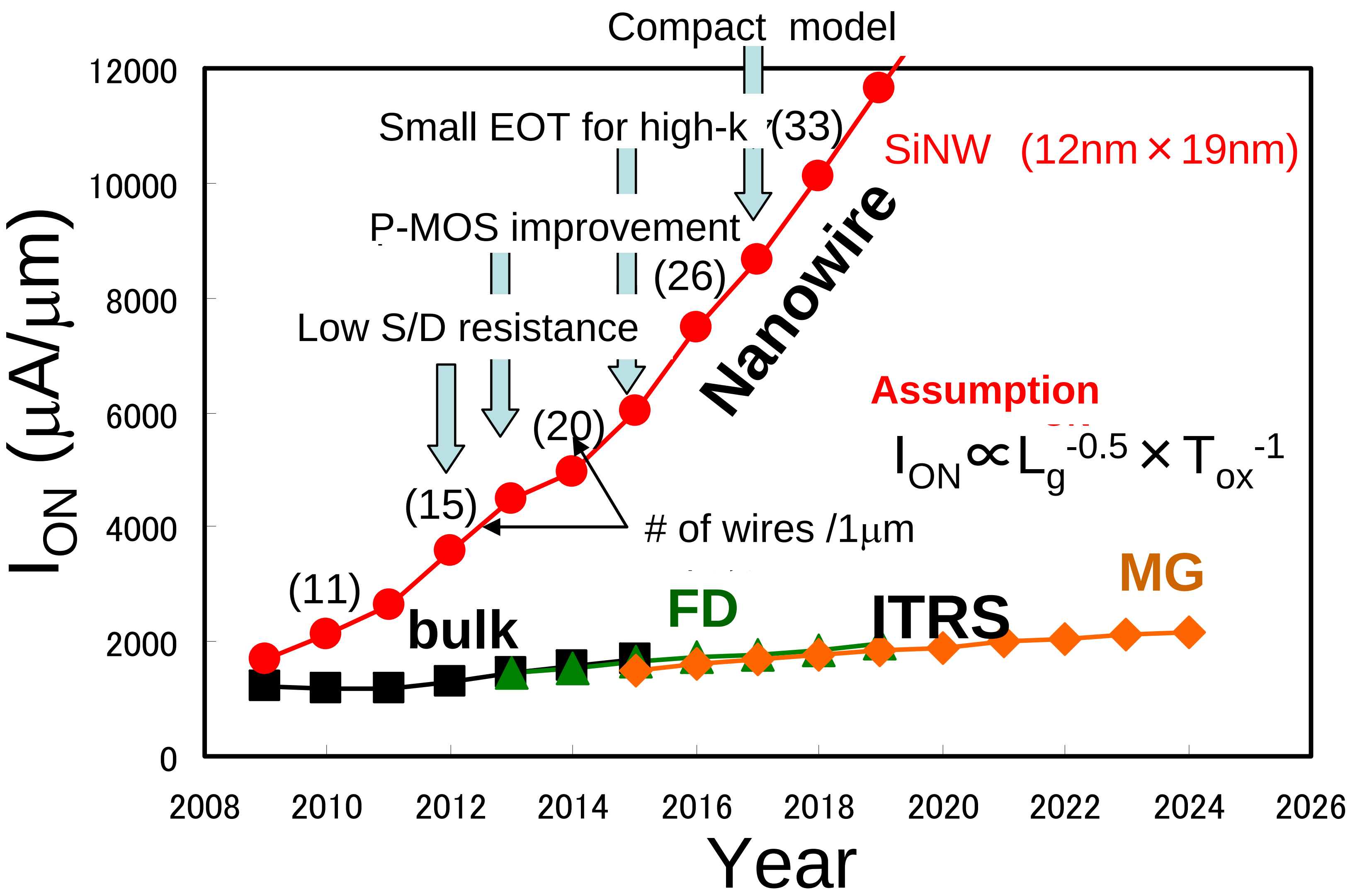
Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240


Effective Electron Mobility (cm²/Vs)
600
400
200
0
0
5x10¹²
10¹³
1.5x10¹³
Inversion Carrier Density (cm⁻²)
A1 (12x19)
hNW x wNW (nm²)
A2 (12x28)
B (20x10)
SOI Planar
TSOI=28 nm
A1
20 nm
hNW: 12nm
wNW: 19 nm
B
hNW: 20nm
wNW: 10 nm
SOI planar
TSOI= 28 nm
W=1 µm
BOX


Metal
12 nm
19 nm
SiO$_2$
(a)
44 %
Electron density: Log |x| (cm^{-3})
20
19.6
19.2
18.8
18.4
18
17.6
17.2
16.8
16.4
16
V$_g$=1V
12 nm
39 nm
(b)
Inversion areal ratio: 29 %

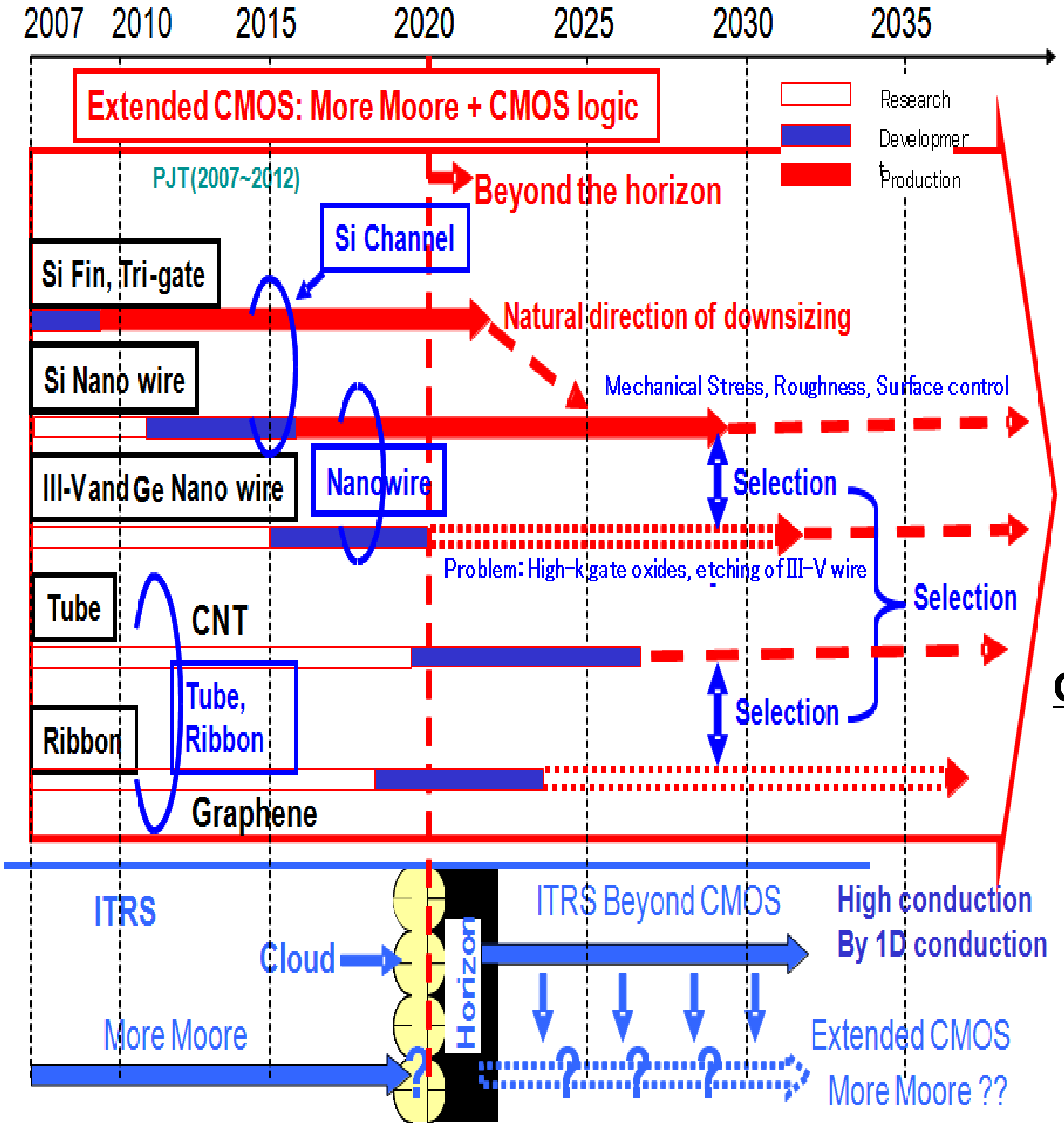

Electron Density
(x10^{19}cm^{-3})
6
5
4
3
2
1
0
Edge portion
Flat portion
0
2
4
6
8
Distance from SiNW Surface (nm)

Primitive estimation !



Our roadmap for R &D

Source: H. Iwai, IWJT 2008



Current Issues

Si Nanowire

Control of wire surface property

Source Drain contact

Optimization of wire diameter

Compact I-V model

III-V & Ge Nanowire

High-k gate insulator

Wire formation technique

CNT:

Growth and integration of CNT

Width and Chirality control

Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique

Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

Thank you
for your attention!