Past and Future of Micro/Nano-Electronics

December 28, 2010

@Gandhi Institute of Technology and Management
Bhubaneshwar, Orissa, India

Hiroshi Iwai,
Tokyo Institute of Technology
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
Institute Overview

Established in 1881 → 130th anniversary in 2011

3 undergraduate schools
School of Science, School of Engineering, School of Bioscience and Biotechnology

7 graduate schools
Science and Engineering Science, Science and Engineering Technology, Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering, Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

<table>
<thead>
<tr>
<th></th>
<th>Undergraduate</th>
<th>Graduate</th>
<th>Master's</th>
<th>Doctoral</th>
<th>Teaching Staff</th>
<th>Student/Instructor</th>
<th>Staff</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tokyo Inst.</td>
<td>5,000</td>
<td>5,000</td>
<td>3,500</td>
<td>1,500</td>
<td>1,200</td>
<td>8.3</td>
<td>550</td>
</tr>
<tr>
<td>Per Year</td>
<td>1,200</td>
<td>1,800</td>
<td>500</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Asia 847
Europe 78
Africa 16
North America 12
South America 24
Oceania 5

Total 982
(As of May. 1, 2005)
先端ナノエレクトロニクス研究コアユニット研究室メンバー

(2010年10月1日現在)
研究風景
Cluster tool for high-k thin film deposition
• There were many inventions in the 20th century: Airplane, Nuclear Power generation, Computer, Space aircraft, etc
• However, everything has to be controlled by electronics
• Electronics
  Most important invention in the 20th century
• What is Electronics: To use electrons, Electronic Circuits
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Cathode (heated)    Grid    Anode (Positive bias)

Same mechanism as that of transistor
4 wives of Lee De Forest

1906 Lucille Sheardown
1907 Nora Blatch
1912 Mary Mayo, singer
1930 Marie Mosquini, silent film actress
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
History of Semiconductor devices

1947, 1st Point Contact Bipolar Transistor:
   Ge Semiconductor, Bardeen, Brattin
   → Nobel Prize

1948, 1st Junction Bipolar Transistor,
   Ge Semiconductor, Schokley
   → Nobel Prize

1958, 1st Integrated Circuits,
   Ge Semiconductor, J.Kilby → Nobel Prize

1959, 1st Planar Integrated Circuits,
   R.Noice

1960, 1st MOS Transistor, Kahng,
   Si Semiconductor

1963, 1st CMOS Circuits, C.T. Sah and F. Wanlass
J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928

J. E. LILIENFELD
Capacitor structure with notch

Negative bias

No current

Positive bias

Current flows

Electric field

Gate Electrode

Gate Insulator

Semiconductor

Electron
Source Channel Drain

Surface Potential (Negative direction)

0V
\( N^+\text{-Si} \)
\( P\text{-Si} \)

1V
\( N\text{-Si} \)

\( 0 \) bias for gate

Positive bias for gate

Source Channel Drain

Electron flow
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator.

Interfacial Charges

Electric Shielding

Carrier Scattering

Drain Current was several orders of magnitude smaller than expected.

Even Shockley!
However, they found amplification phenomenon when investigating Ge surface when putting needles. This is the 1st Transistor:

Not Field Effect Transistor, But Bipolar Transistor (another mechanism)

1947: 1st transistor

Bipolar using Ge

J. Bardeen
W. Bratten,
W. Shockley
1958: 1st Integrated Circuit

Connect 2 bipolar transistors in the Same substrate by bonding wire.

Jack S. Kilby
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

Al Gate

Drain

Si

Si/SiO₂ Interface is extraordinarily good

Al
SiO₂
Si
1970, 71: 1st generation of LSIs

DRAM Intel 1103

MPU Intel 4004
MOS LSI experienced continuous progress for many years

<table>
<thead>
<tr>
<th>Name of Integrated Circuits</th>
<th>Number of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>1960s IC (Integrated Circuits)</td>
<td>~ 10</td>
</tr>
<tr>
<td>1970s LSI (Large Scale Integrated Circuit)</td>
<td>~ 1,000</td>
</tr>
<tr>
<td>1980s VLSI (Very Large Scale IC)</td>
<td>~ 10,000</td>
</tr>
<tr>
<td>1990s ULSI (Ultra Large Scale IC)</td>
<td>~ 1,000,000</td>
</tr>
<tr>
<td>2000s ?LSI (? Large Scale IC)</td>
<td>~1000,000,000</td>
</tr>
</tbody>
</table>
MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Use Gate Field Effect for switching

N-MOS (N-type MOSFET)
N-MOS
(N-type MOSFET)

P-MOS
(P-type MOSFET)

Source

Gate

Drain

Electron flow

Current flow

Hole flow

Current flow
When NMOS is ON, PMOS is OFF.
When PMOS is ON, NMOS is OFF.
Needless to say, but....

**CMOS Technology:**
Indispensible for our human society

All the human activities are controlled by CMOS

- living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

**Without CMOS:**

There is no computer in banks, and

- world economical activities immediately stop.

Cellarer phone dose not exists
Downsizing of the components has been the driving force for circuit evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>1900</th>
<th>1950</th>
<th>1960</th>
<th>1970</th>
<th>2000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>Vacuum Tube</td>
<td>Transistor</td>
<td>IC</td>
<td>LSI</td>
<td>ULSI</td>
</tr>
<tr>
<td>Size</td>
<td>10 cm</td>
<td>cm</td>
<td>mm</td>
<td>10 μm</td>
<td>100 nm</td>
</tr>
<tr>
<td></td>
<td>10^{-1}m</td>
<td>10^{-2}m</td>
<td>10^{-3}m</td>
<td>10^{-5}m</td>
<td>10^{-7}m</td>
</tr>
</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. **Reduce Capacitance**
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. **Increase number of Transistors**
   - Parallel processing
     - Increase circuit operation speed

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.
Scaling Method: by R. Dennard in 1974

- **Wdep**: Space Charge Region (or Depletion Region) Width

  Wdep has to be suppressed. Otherwise, large leakage between S and D.

- Wdep: Space Charge Region Width

  Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

**K=0.7 for example**

- By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

**Good scaled I-V characteristics**

- **Wdep**: \( \propto \sqrt{V/Na} \)

- By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

**K**: scaling factor
### Downscaling merit: Beautiful!

<table>
<thead>
<tr>
<th>Geometry &amp; Supply voltage</th>
<th>(L_g, W_g, T_{ox}, V_{dd})</th>
<th>(K)</th>
<th>(\text{Scaling } K : K=0.7 \text{ for example})</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Drive current in saturation</th>
<th>(I_d)</th>
<th>(K)</th>
<th>(I_d = \nu_{sat} W_g C_o (V_g - V_{th}))</th>
<th>(C_o): gate C per unit area</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_d) per unit (W_g)</td>
<td>(I_d/\mu m)</td>
<td>1</td>
<td>(I_d = I_d/W_g = 1)</td>
<td></td>
</tr>
</tbody>
</table>

| Gate capacitance            | \(C_g\) | \(K\) | \(C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox}\) | \(KK/K = K\) |

| Switching speed             | \(\tau\) | \(K\) | \(\tau = C_g V_{dd}/I_d\) | \(KK/K = K\) |

| Clock frequency             | \(f\)    | \(1/K\) | \(f = 1/\tau = 1/K\)       |                          |

| Chip area                   | \(A_{chip}\) | \(\alpha\) | \(\alpha\): Scaling factor | In the past, \(\alpha > 1\) for most cases |

| Integration (# of Tr)       | \(N\)    | \(\alpha/K^2\) | \(N \rightarrow \alpha/K^2\) | \(= 1/K^2\), when \(\alpha = 1\) |

<p>| Power per chip              | (P)    | (\alpha) | (fNCV^2/2) | (K^{-1}(\alpha K^{-2})K (K^1)^2 = \alpha = 1), when (\alpha = 1) |</p>
<table>
<thead>
<tr>
<th></th>
<th>( k = 0.7 ) and ( \alpha = 1 )</th>
<th>( k = 0.7^2 = 0.5 ) and ( \alpha = 1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Single MOFET</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{dd} \rightarrow 0.7 )</td>
<td></td>
<td>( V_{dd} \rightarrow 0.5 )</td>
</tr>
<tr>
<td>( L_g \rightarrow 0.7 )</td>
<td></td>
<td>( L_g \rightarrow 0.5 )</td>
</tr>
<tr>
<td>( I_d \rightarrow 0.7 )</td>
<td></td>
<td>( I_d \rightarrow 0.5 )</td>
</tr>
<tr>
<td>( C_g \rightarrow 0.7 )</td>
<td></td>
<td>( C_g \rightarrow 0.5 )</td>
</tr>
<tr>
<td>( \frac{P \text{ (Power)} / \text{Clock}}{0.7^3} = 0.34 )</td>
<td>( \frac{P \text{ (Power)} / \text{Clock}}{0.5^3} = 0.125 )</td>
<td></td>
</tr>
<tr>
<td>( \tau \text{ (Switching time)} \rightarrow 0.7 )</td>
<td>( \tau \text{ (Switching time)} \rightarrow 0.5 )</td>
<td></td>
</tr>
<tr>
<td><strong>Chip</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( N \text{ (# of Tr)} \rightarrow 1/0.7^2 = 2 )</td>
<td>( N \text{ (# of Tr)} \rightarrow 1/0.5^2 = 4 )</td>
<td></td>
</tr>
<tr>
<td>( f \text{ (Clock)} \rightarrow 1/0.7 = 1.4 )</td>
<td>( f \text{ (Clock)} \rightarrow 1/0.5 = 2 )</td>
<td></td>
</tr>
<tr>
<td>( P \text{ (Power)} \rightarrow 1 )</td>
<td>( P \text{ (Power)} \rightarrow 1 )</td>
<td></td>
</tr>
</tbody>
</table>
### Actual past downscaling trend until year 2000

**Change in 30 years**

<table>
<thead>
<tr>
<th></th>
<th>Ideal scaling</th>
<th>Real Change</th>
<th>Ideal scaling</th>
<th>Real Change</th>
<th>Ideal scaling</th>
<th>Real Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L )</td>
<td>K</td>
<td>10^{-2}</td>
<td>f</td>
<td>1/K(10^2)</td>
<td></td>
<td>10^3</td>
</tr>
<tr>
<td>( t_{ox} )</td>
<td>K(10^{-2})</td>
<td>10^{-2}</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{dd} )</td>
<td>K(10^{-2})</td>
<td>10^{-1}</td>
<td>( I_d )</td>
<td>K(10^{-2})</td>
<td>10^{-1}</td>
<td></td>
</tr>
<tr>
<td>( A_{chip} )</td>
<td>( \alpha )</td>
<td>10^1</td>
<td>( I_d/\mu m )</td>
<td>1</td>
<td>10^1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( N )</td>
<td>( \alpha/K^2(10^5) )</td>
<td>10^4</td>
<td></td>
</tr>
</tbody>
</table>

**Past 30 years scaling**

**Merit:** N, f increase

**Demerit:** P increase

**V_{dd} scaling insufficient**

Additional significant increase in \( I_d, f, P \)

---

**Source:** Iwai and S. Ohmi, Microelectronics Reliability 42 (2002), pp.1251-1268
Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1µm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5µm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25µm:</td>
<td>Direct-tunneling of gate SiO₂</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1µm:</td>
<td>‘0.1µm brick wall’(various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
Historically, many predictions of the limit of downsizing. VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.
Finally, there appears to be a fundamental limit of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.
Direct-tunneling effect

Direct tunneling leakage current start to flow when the thickness is 3 nm.
Direct tunneling leakage was found to be OK! In 1994!
Gate leakage: \(I_g \propto \text{Gate Area} \propto \text{Gate length (Lg)}\)

Drain current: \(I_d \propto 1/\text{Gate length (Lg)}\)

\(L_g \rightarrow \text{small},\)

Then, \(I_g \rightarrow \text{small}, I_d \rightarrow \text{large},\) Thus, \(I_g/I_d \rightarrow \text{very small}\)

\[
\begin{align*}
\text{Lg} = 10 \, \mu\text{m} & \quad \text{Lg} = 5 \, \mu\text{m} & \quad \text{Lg} = 1.0 \, \mu\text{m} & \quad \text{Lg} = 0.1\mu\text{m}
\end{align*}
\]
Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!

Some one will think for you
Transistor Scaling Continues

90nm node
Lg=50nm

65nm node
Lg=35nm

45nm node
Lg=25nm

32nm node
Lg=15nm

22nm node
Lg=10nm

~30% every two years

ITRS 2003 (HP)

Qi Xinag, ECS 2004, AMD
Downsizing limit? Channel length?

Electron wave length

10 nm

Gate Oxd

Channel
5 nm gate length CMOS Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC

IEDM, 2003
Electron wave length

10 nm

Tunneling distance

3 nm

Downsizing limit!

Channel length
Gate oxide thickness
Prediction now!

Electron wave length
10 nm

Tunneling distance
3 nm

Atom distance
0.3 nm

MOSFET operation
\( L_g = 2 \sim 1.5 \text{ nm?} \)

Below this, no one knows future!
However, Gate oxide thickness 2 orders magnitude smaller Close to limitation!!

Lg: Gate length downsizing will continue to another 10-15 years
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
So, we are now in the limitation of downsizing?

Do you believe this or do not?
There is a solution! To use high-k dielectrics

Thin gate SiO\textsubscript{2}  \hspace{3cm}  Thick gate high-k dielectrics

Almost the same electric characteristics

However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO\textsubscript{2}!
Choice of High-k elements for oxide

Candidates

Gas or liquid at 1000 K

Radio active

HfO$_2$ based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La$_2$O$_3$ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

Oxide

Band offset

Si

Dielectric Constant \( \varepsilon(0) \)

Band Discontinuity [eV]

XPS measurement by Prof. T. Hattori, INFOS 2003
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness

Metal Gate
(different for NMOS & PMOS)

High-k

Silicon Substrate
For the past 45 years, SiO₂ and SiON have been used for gate insulator. Today, EOT=1.0nm. The EOT limit is 0.7~0.8 nm. One order of magnitude can be achieved by using high-k materials. EOT can be reduced further beyond 0.5 nm by using direct contact to Si. By choosing appropriate materials and processes.
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O* $\rightarrow$ HfO$_2$ + SiO$_2$

Oxygen supplied from W gate electrode

SiO$_x$-IL is formed after annealing
Oxygen control is required for optimizing the reaction

D.J. Lichtenwalner, Trans. ECS 11, 319

H. Shimizu, JJAP, 44, pp. 6131
**Choice of High-k elements for oxide**

<table>
<thead>
<tr>
<th>Element</th>
<th>Unstable at Si interface</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Si + MOₓ M + SiO₂</td>
<td></td>
<td>He</td>
</tr>
<tr>
<td>Li, Be</td>
<td>Si + MOₓ MSiₓ + SiO₂</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mg, Na</td>
<td>Si + MOₓ M + MSiₓOᵧ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ca, Sc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sr, Y, Zr</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cs, Ba</td>
<td>Hf</td>
<td></td>
<td>Al, Si</td>
</tr>
</tbody>
</table>

- **Candidates**

- **Gas or liquid at 1000 K**

- **Radio active**

- **HfO₂ based dielectrics are selected as the first generation materials, because of their merit in**
  1) band-offset,
  2) dielectric constant
  3) thermal stability

- **La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer**

R. Hauser, IEDM Short Course, 1999
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ can achieve direct contact of high-k/Si

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

XPS Si1s spectra

TEM image 500 °C, 30 min

W
La$_2$O$_3$  k=23
La-silicate  k=8~14

1 nm
Quantum Effect in Gate Stack

- **Gate oxide capacitance**
- **Charge layer capacitance**
- **Inversion layer capacitance**

**Thickness shown in EOT**
- Poly-Si($10^{20}$ cm$^{-3}$): 0.3 nm
- Metal: 0.1 nm

K. Natori, SSDM (2005)

- **High-k (EOT)**

- **Total parasitic capacitance ~ 0.6nm of EOT**

- A question if the performance improvement can be obtained with EOT<0.5nm

- Is EOT<0.5nm achievable?
EOT = 0.48 nm

Transistor with La2O3 gate insulator

Our results
EOT=0.37nm
La2O3

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

0.48 → 0.37nm Increase of Id at 30%
\( \mu_{\text{eff}} \) of W/La\(_2\)O\(_3\) and W/HfO\(_2\) nFET on EOT

- W/La\(_2\)O\(_3\) exhibits higher \( \mu_{\text{eff}} \) than W/HfO\(_2\)
- \( \mu_{\text{eff}} \) start degrades below EOT=1.4nm
FET characteristics of W/La$_2$O$_3$ on EOT

All characteristics start to degrade or shift below EOT=1.4nm

N$_{fix}$=7x10$^{12}$ cm$^{-2}$

Aggressive N$_{fix}$ generation at EOT<1.2nm

N$_{fix}$ and D$_{it}$

All characteristics start to degrade or shift below EOT=1.4nm
Gate Metal Induced Defects Compensation

- Suppression of aggressive shift in $V_{fb}$

- Metal Gate
  - MgO
  - La2O3
  - Si

- TEM
- EDX

- Mg
- La

- W, Si, 2nm

- PMA500°C
Mobility Improvement with Mg Incorporation

Recovery of $\mu_{\text{eff}}$ mainly at low $E_{\text{eff}}$
6 µm NMOS LSI in 1974

Layers:
1. Si substrate
2. Field oxide
3. Gate oxide
4. Poly Si
5. S/D
6. Interlayer
7. Aluminum
8. Passivation

Materials:
1. Si
2. SiO₂
3. BPSG
4. Al
5. PSG

Atoms:
1. Si
2. O
3. P
4. B
5. Al
(H, N, Cl)
**New materials**

Just examples!
Many other candidates

- Ge (III-V)
- La$_2$O$_3$
- Ta$_2$O$_5$
- HfO$_2$
- ZrO$_2$
- ZrSi$_x$O$_y$
- RuO$_2$
- Pt
- IrO$_2$
- Y1
- PZT
- BST

Silicides:
- NiSi silicide
- SiGe Semiconductor
- Air
- HSQ
- Polymer
- Low-k dielectrics
- TiN
- TaN
- Metals
- Cu
- W

Diodes:
- PtSi$_2$
- WSi$_2$
- CoSi$_2$
- TiSi$_2$
- MoSi$_2$
- TaSi$_2$

Ferroelectrics:
- PtSi$_2$
- WSi$_2$
- CoSi$_2$
- TiSi$_2$
- MoSi$_2$
- TaSi$_2$

Low-k dielectrics:
- Air
- HSQ
- Polymer

High-k dielectrics:
- La$_2$O$_3$
- Ta$_2$O$_5$
- HfO$_2$
- ZrO$_2$
- ZrSi$_x$O$_y$

Semiconductors
- Ge (III-V)

Electrode materials:
- Pt
- IrO$_2$

Y. Nishi, Si Nano Workshop, 2006,
(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)
What is a roadmap? What is ITRS?

Roadmap: Prediction of future technologies

ITRS: International Technology Roadmap for Semiconductors made by SIA (Semiconductor Industry Association with Collaboration with Japan, Europe, Korea and Taiwan)
1992 -1997: NTRS (National Technology Roadmap)
1998 - : ITRS (International Technology Roadmap)
Question:
How far we can go with downscaling?
- There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

- Even after reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

- Two candidates have emerged for R & D
  1. Nanowire/tube MOSFETs
  2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.
How far can we go?

**Past** 0.7 times per 3 years  
1973年

- $8\mu m \rightarrow 6\mu m \rightarrow 4\mu m \rightarrow 3\mu m \rightarrow 2\mu m \rightarrow 1.2\mu m \rightarrow 0.8\mu m \rightarrow 0.5\mu m$
- $0.35\mu m \rightarrow 0.25\mu m \rightarrow 180nm \rightarrow 130nm \rightarrow 90nm \rightarrow 65nm \rightarrow 45nm$

**Now**

**Future**

- $32nm \rightarrow 22nm \rightarrow 16nm \rightarrow 11.5nm \rightarrow 8nm \rightarrow 5.5nm? \rightarrow 4nm? \rightarrow 2.9\ nm?$

- At least 5,6 generations, for 15 ~ 20 years
- Hopefully 8 generations, for 30 years
**HP, LOP, LSTP for Logic CMOS**

- **HP CMOS** (high Performance)
  - Highest Ion, Lowest CV/I
  - High leakage
  - Medium Vdd

- **LOP CMOS** (Low Operation Power)
  - Lowest Vdd
  - Medium Ion, medium CV/I
  - Medium leakage

- **LSTP CMOS** (Low Standby Power)
  - Lowest leakage
  - Low Ion, high CV/I
  - High Vdd

Source: 2007 ITRS Winter Public Conf.
Because of off-leakage control,

Planar $\rightarrow$ Fin $\rightarrow$ Nanowire
Nanowire FET

Multiple Gate (Fin)FET

ITRS 2009

Scaling Pathways

Bulk or SOI

Fin

Si Nanowire
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of $I_{OFF}$
3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires

Leakage current

Gate: OFF
Increase the Number of quantum channels

Energy band of Bulk Si

By Prof. Shiraishi of Tsukuba univ.

Energy band of 3 x 3 Si wire

4 channels can be used
Maximum number of wires per 1 μm

Front gate type MOS  165 wires /μm

Surrounded gate type MOS  33 wires/μm

6nm pitch
By nano-imprint method

Metal gate electrode (10nm)
High-k gate insulator (4nm)
Si Nano wire (Diameter 2nm)

30nm pitch: EUV lithography

Surrounded gate MOS
Device fabrication

Si/Si$_{0.8}$Ge$_{0.2}$ superlattice epitaxy on SOI

Anisotropic etching of these layers

Isotropic etching of SiGe

The NW diameter is controllable down to 5 nm by self limited oxidation.

Process Details:
C. Dupre et al., IEDM Tech. Dig., p.749, 2008

Standard Back-End of-Line Process
3D-stacked Si NWs with Hi-k/MG

Wire direction: <110>
- 50 NWs in parallel
- 3 levels vertically-stacked
- Total array of 150 wires
- EOT ~2.6 nm
SiNW Band structure calculation
Cross section of Si NW

First principal calculation,

D=1.96nm [001]
D=1.94nm [011]
D=1.93nm [111]
Si nanowire FET with 1D Transport

Orientation  
[001]  [011]  [111]  
Diameter (nm) 0.86 0.94 0.89

Small mass with [011]
Large number of quantum channels with [001]
Atomic models of a Si quantum dot and Si nanowires

6.6 nm diameter SiQD
(8651 atoms)

20 nm diameter Si(100)NW
(8941 atoms)

10 nm diameter Si(100)NW
(2341 atoms)
RSDFT – suitable for parallel first-principles calculation -

- Real-Space Finite-Difference
- Sparse Matrix
- FFT free (FFT is inevitable in the conventional plane-wave code)
- MPI (Message Passing Interface) library

Kohn-Sham eq. (finite-difference)

\[\left(-\frac{1}{2} \nabla^2 + v_s[\rho](\mathbf{r}) + \hat{v}_{nloc}^{PP}(\mathbf{r})\right)\phi_n(\mathbf{r}) = \varepsilon_n \phi_n(\mathbf{r})\]

Higher-order finite difference

\[\frac{\partial^2}{\partial x^2} \psi_n(x, y, z) \approx \sum_{m=-6}^{6} C_m \psi_n(x + m\Delta x, y, z)\]

Integration

\[\int \psi_m(\mathbf{r})\psi_n(\mathbf{r})d\mathbf{r} \approx \sum_{i=1}^{Mesh} \psi_m(\mathbf{r}_i)\psi_n(\mathbf{r}_i)\Delta x\Delta y\Delta z\]

3D grid is divided by several regions for parallel computation.

MPI_ISEND, MPI_IRECV

MPI_ALLREDUCE
Massively Parallel Computing

with our recently developed code “RSDFT”

Iwata et al, J. Comp. Phys., to be published

Real-Space Density-Functional Theory code (RSDFT)

Based on the finite-difference pseudopotential method (J. R. Chelikowsky et al., PRB1994)

Highly tuned for massively parallel computers

Computations are done on a massively-parallel cluster PACS-CS at University of Tsukuba.
(Theoretical Peak Performance = 5.6GFLOPS/node)

e.g.) The system over 10,000 atoms \( \text{Si}_{10701}\text{H}_{1996} \) (7.6 nm diameter Si dot)

Convergence behavior for \( \text{Si}_{10701}\text{H}_{1996} \)

Grid points = 3,402,059

Bands = 22,432

Computational Time (with 1024 nodes of PACS-CS)

6781 sec. \( \times \) 60 iteration step = 113 hour
Band Structure and DOS of Si(100)NWs (D=1nm, 4nm, and 8nm)

D=1 nm
Si21H20 (41 atoms)
KS band gap = 2.60 eV

D = 4 nm
Si341H84 (425 atoms)
KS band gap = 0.81 eV

D=8 nm
Si1361H164 (1525 atoms)
KS band gap = 0.61 eV

KS band gap of bulk (LDA) = 0.53 eV
Band structure of 8-nm-diameter Si nanowire near the CBM

- KS band gap = 0.608 eV (@Γ)

Each band is 4-dgenerate.

Effective mass equation

\[
\left[ -\frac{\hbar^2}{2m^*} \left( \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} \right) - \frac{\hbar^2}{2m^*} \frac{\partial^2}{\partial z^2} \right] \Phi(r) = (\varepsilon - \varepsilon_{CBM}) \Phi(r)
\]

The band structure can be understood that electrons near the CBM in the bulk Si are Confined within a cylindrical geometry.
Si12822H1544 (14,366 atoms)

- 10nm diameter, 3.3nm height, (100)
- Grid spacing 0.45Å (~14Ry)
- # of grid points 4,718,592
- # of bands 29,024
- Memory: 1,022GB ~ 2,044GB

Si nano wire with surface roughness
SiNW Band compact model
Landauer Formalism for Ballistic FET

\[ I_D = \frac{q}{\pi \hbar} \sum_i \int \left[ f(E, \mu_S) - f(E, \mu_D) \right] T_i(E) dE \]

From \( x_{\text{max}} \) to \( x_{\text{min}} \) \( T_i(E) \approx 1 \)

\[ I_D = G_0 \left( \frac{k_B T}{q} \right) \sum_i g_i \ln \left\{ \frac{1 + \exp\left[ (\mu_S - E_{i0}) / k_B T \right]}{1 + \exp\left[ (\mu_D - E_{i0}) / k_B T \right]} \right\} \]
IV Characteristics of Ballistic SiNW FET

Small temperature dependency
35µA/wire for 4 quantum channels
**Model of Carrier Scattering**

Linear Potential Approx. : Electric Field $E$

- **Source**
- **Channel**
- **To Drain**

- Elastic Backscatt.
- Optical Phonon Emission

Transmission Probability to Drain:

$$T(\varepsilon) = \frac{F(0) - G(0)}{F(0)}$$

Injection from Drain = 0
Résumé of the Compact Model

\[ I = \frac{q}{\pi \hbar} \sum_i g_i \int [f(\varepsilon, \mu_s) - f(\varepsilon, \mu_D)] T_i \, d\varepsilon \]

\[ (V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{|Q_f + Q_b|}{C_G}. \]

\[ \mu_S - \mu_D = qV_D \]

\[ C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left( \frac{\sqrt{2r + t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r + t_{ox}} - \sqrt{t_{ox}}} \right)}. \]

\[ C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left( \frac{r + t_{ox}}{r} \right)}. \]

\[ |Q_f + Q_b| = \frac{q}{\pi} \sum_i g_i \left[ \int_{-\infty}^{0} \frac{dk}{1 + \exp \left( \frac{\varepsilon_i(k) - \mu_S}{k_B T} \right)} - \int_{0}^{\infty} \frac{1}{1 + \exp \left( \frac{\varepsilon_i(k) - \mu_S}{k_B T} \right)} - \int_{-\infty}^{0} \frac{1}{1 + \exp \left( \frac{\varepsilon_i(k) - \mu_D}{k_B T} \right)} \right] T_i(\varepsilon_i(k))dk \]

\[ T(\varepsilon) = \frac{\sqrt{2D_0 qE}}{\left( \sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0 B_0} \ln \left( \frac{qEx_0 + \varepsilon}{\varepsilon} \right)} \]

Unknowns are \( I_D, (\mu_S-\mu_0), (\mu_D-\mu_0), (Q_f+Q_b) \)
Electric current $20\sim25\ \mu A$

No saturation at Large $V_D$
SiNW FET Fabrication
SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oxide etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

Standard recipe for gate stack formation
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.
Fabricated SiNW FET

SiNW

SiN support

Poly-Si

SiNW

Fabricated SiNW FET

30nm

500nm
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off > 10^6, 60uA/wire

L_g = 65nm, T_{ox} = 3nm
Gate Length (nm) vs. $I_{ON}$ ($\mu$A/wire)

- nMOS
- pMOS

VDD: 1.0~1.5 V

Our Work
<table>
<thead>
<tr>
<th>NW Cross-section (nm)</th>
<th>Rect.</th>
<th>Rect.</th>
<th>Rect.</th>
<th>Cir.</th>
<th>Cir.</th>
<th>Elliptical</th>
<th>Elliptical</th>
</tr>
</thead>
<tbody>
<tr>
<td>NW Size (nm)</td>
<td>10x20</td>
<td>10x20</td>
<td>14</td>
<td>10</td>
<td>10</td>
<td>12</td>
<td>13x20</td>
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<tr>
<td>Lg (nm)</td>
<td>65</td>
<td>25</td>
<td>100</td>
<td>30</td>
<td>8</td>
<td>65</td>
<td>35</td>
</tr>
<tr>
<td>EOT or Tox (nm)</td>
<td>3</td>
<td>1.8</td>
<td>1.8</td>
<td>2</td>
<td>4</td>
<td>3</td>
<td>1.5</td>
</tr>
<tr>
<td>Vdd (V)</td>
<td>1.0</td>
<td>1.1</td>
<td>1.2</td>
<td>1.0</td>
<td>1.2</td>
<td>1.2</td>
<td>1.0</td>
</tr>
<tr>
<td>Ion(uA) per wire</td>
<td>60.1</td>
<td>102</td>
<td>30.3</td>
<td>26.4</td>
<td>37.4</td>
<td>48.4</td>
<td>43.8</td>
</tr>
<tr>
<td>Ion(uA/um) by dia.</td>
<td>3117</td>
<td>5010</td>
<td>2170</td>
<td>2640</td>
<td>3740</td>
<td>4030</td>
<td>2592</td>
</tr>
<tr>
<td>Ion(uA/um) by cir.</td>
<td>1609</td>
<td>2054</td>
<td>430</td>
<td>841</td>
<td>1191</td>
<td>1283</td>
<td>825</td>
</tr>
<tr>
<td>SS (mV/dec.)</td>
<td>70</td>
<td>79</td>
<td>68</td>
<td>71</td>
<td>75</td>
<td>~75</td>
<td>85</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>62</td>
<td>56</td>
<td>15</td>
<td>13</td>
<td>22</td>
<td>40-82</td>
<td>65</td>
</tr>
<tr>
<td>Ion/Ioff</td>
<td>~1E6</td>
<td>&gt;1E6</td>
<td>&gt;1E5</td>
<td>~1E6</td>
<td>&gt;1E7</td>
<td>&gt;1E7</td>
<td>~2E5</td>
</tr>
</tbody>
</table>

Ref[11] by Stmicro Lg=25nm, Tox=1.8nm
This work Lg=65nm, Tox=3nm
This work

Planer FET
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

SiノワイヤFET
Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240
Electron Density (x10^{19} \text{cm}^{-3})

Distance from SiNW Surface (nm)

- Edge portion
- Flat portion

(a) Metal
- 12 nm
- 19 nm
- SiO₂

(b) Inversion areal ratio: 29%
- 12 nm
- 39 nm

V_g = 1V
Primitive estimation!

- Small EOT for high-k (33)
- P-MOS improvement (26)
- Low S/D resistance (20)
- # of wires /1µm (15)
- I_{ON} \propto L_{g}^{-0.5} T_{ox}^{-1}

Compact model

SiNW (12nm \& 19nm)

Assumption

bulk

FD

ITRS

MG
Our roadmap for R & D
Source: H. Iwai, IWJT 2008

Current Issues

Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap

Extended CMOS: More Moore + CMOS logic

Beyond the horizon

Si Fin, Tri-gate
Si Nano wire
III-V and Ge Nano wire
CNT
Tube, Ribbon
Graphene

PJT (2007-2012)

Control of wire surface property
Mechanical Stress, Roughness, Surface control

Problems:
- High-k gate oxides, etching of III-V wire

Selection

ITRS

More Moore

ITRS Beyond CMOS
- High conduction by 1D conduction

Extended CMOS
- More Moore ??

Horizon

Cloud

Research Development Production
Thank you for your attention!