

Si Nanowire FET Modeling and Technology

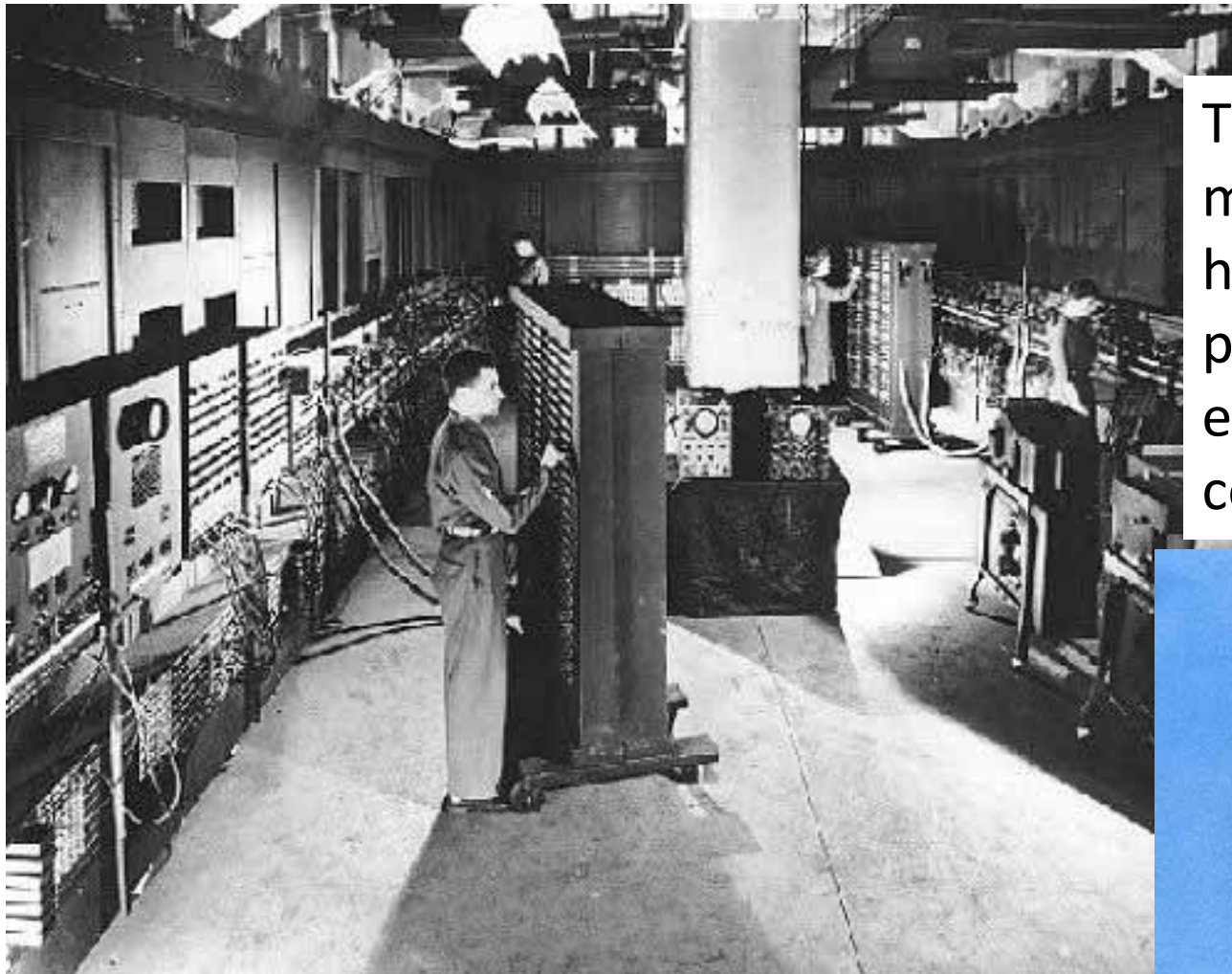
November 8, 2010

**@ Institute of Microelectronics
Chinese Academy of Sciences**

**H. Iwai
Tokyo Inst. Tech.**

First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device



Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power
consumption



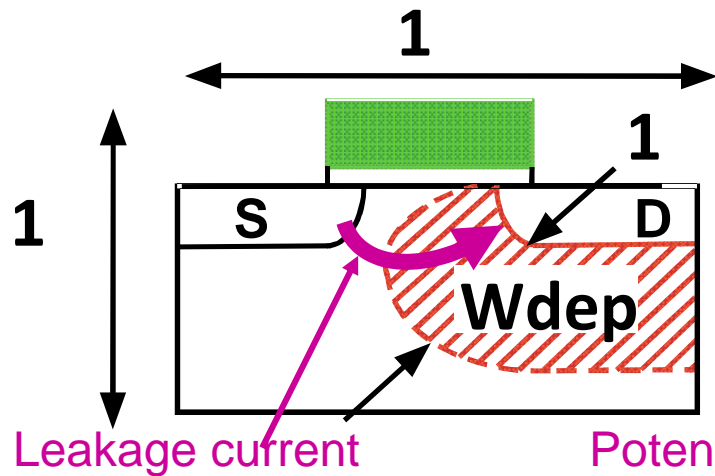
Downsizing of the components has been the driving force for circuit evolution



1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

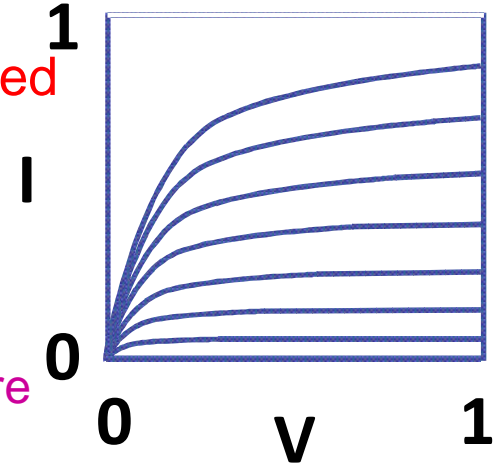
In 100 years, the size reduced by one million times. There have been many devices from stone age. **We have never experienced such a tremendous reduction of devices in human history.**

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage
between S and D



Leakage current

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

**K=0.7
for
example**

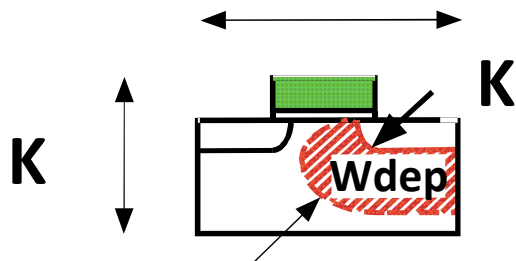


X , Y , Z : K, V : K, Na : 1/K

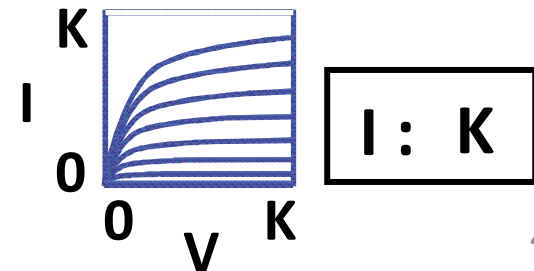
By the scaling, Wdep is suppressed in proportion,
and thus, leakage can be suppressed.

K

→ Good scaled I-V characteristics



**Wdep ∝ √(V/Na)
: K**



I : K

Downscaling merit: Beautiful!

Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	Scaling K : K=0.7 for example
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o : gate C per unit area $\rightarrow W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \epsilon_o \epsilon_{ox} L_g W_g / t_{ox} \rightarrow KK/K = K$
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d \rightarrow KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α: Scaling factor \rightarrow In the past, $\alpha > 1$ for most cases
Integration (# of Tr)	N	α/K^2	$N \rightarrow \alpha/K^2 = 1/K^2$, when $\alpha=1$
Power per chip	P	α	$fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha = 1$, when $\alpha=1$

$k = 0.7$ and $\alpha = 1$

Single MOFET

$V_{dd} \rightarrow 0.7$

$L_g \rightarrow 0.7$

$I_d \rightarrow 0.7$

$C_g \rightarrow 0.7$

P (Power)/Clock

$\rightarrow 0.7^3 = 0.34$

τ (Switching time) $\rightarrow 0.7$

$k = 0.7^2 = 0.5$ and $\alpha = 1$

$V_{dd} \rightarrow 0.5$

$L_g \rightarrow 0.5$

$I_d \rightarrow 0.5$

$C_g \rightarrow 0.5$

P (Power)/Clock

$\rightarrow 0.5^3 = 0.125$

τ (Switching time) $\rightarrow 0.5$

Chip

N (# of Tr) $\rightarrow 1/0.7^2 = 2$

f (Clock) $\rightarrow 1/0.7 = 1.4$

P (Power) $\rightarrow 1$

N (# of Tr) $\rightarrow 1/0.5^2 = 4$

f (Clock) $\rightarrow 1/0.5 = 2$

P (Power) $\rightarrow 1$

Integrated Circuits Technologies are still very important for Green or power saving!

1. Green by Integrated Circuits

Power saving by Microprocessor control for all the human systems

2. Green of Integrated Circuits

Power saving of Integrated Circuits by Down Scaling of MOSFETs in PC, Data Center, Router, etc.

Down scaling is the most effective way of Power saving.

It has been always discussed about the limit of downscaling, but the down scaling of MOSFETs is still possible for another 10 or 20 years!

3 important technological items for DS.

1. Thinning of high-k beyond 0.5 nm
2. Metal S/D
3. Si-Nanowire FET

Question:

How far we can go
with downscaling?

Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1 μ m:	SCE
Early 1980's	0.5 μ m:	S/D resistance
Early 1980's	0.25 μ m:	Direct-tunneling of gate SiO ₂
Late 1980's	0.1 μ m:	'0.1 μ m brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

VLSI text book written 1979 predict that 0.25 micrometer would be the limit because of direct-tunneling current through the very thin-gate oxide.

INTRODUCTION TO **VLSI** SYSTEMS

CARVER MEAD • LYNN CONWAY



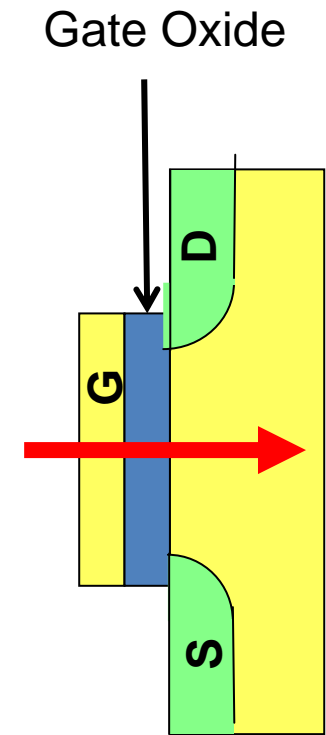
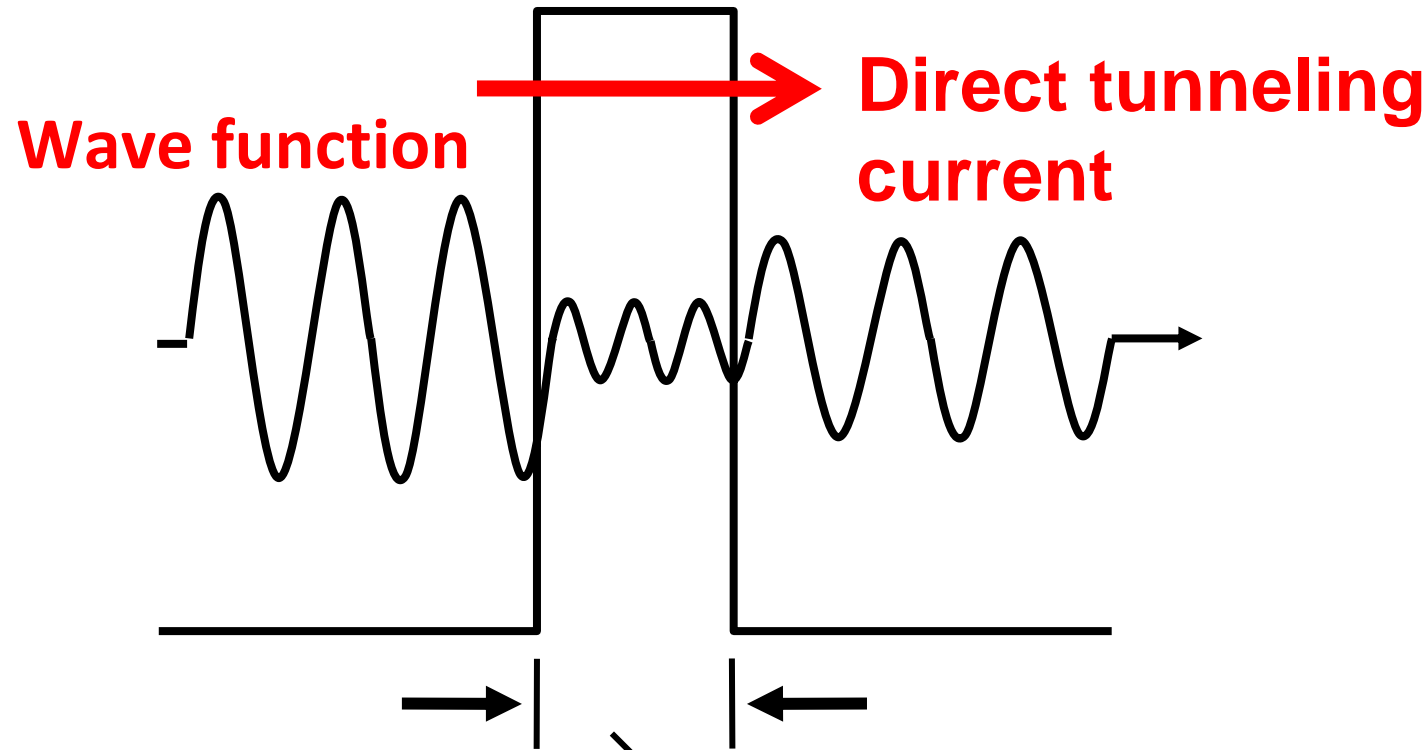
VLSI textbook

Finally, there appears to be a fundamental limit ¹⁰ of approximately quarter micron channel length, where certain physical effects such as the **tunneling through the gate oxide begin to make the devices of smaller dimension unworkable.**

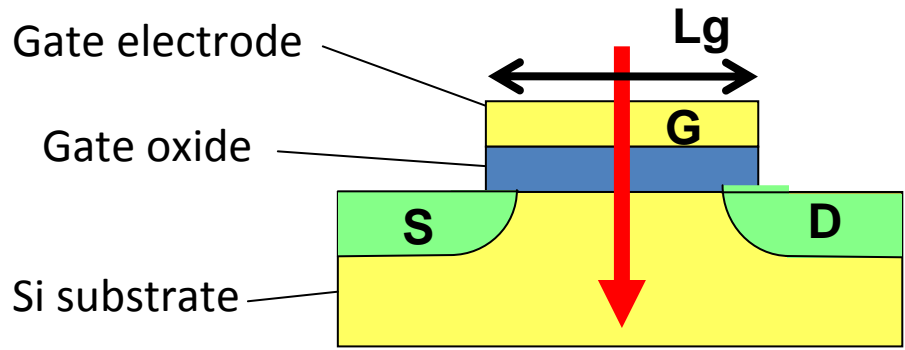
Direct-tunneling effect

Gate Electrode Gate Oxide Si Substrate

Potential Barrier

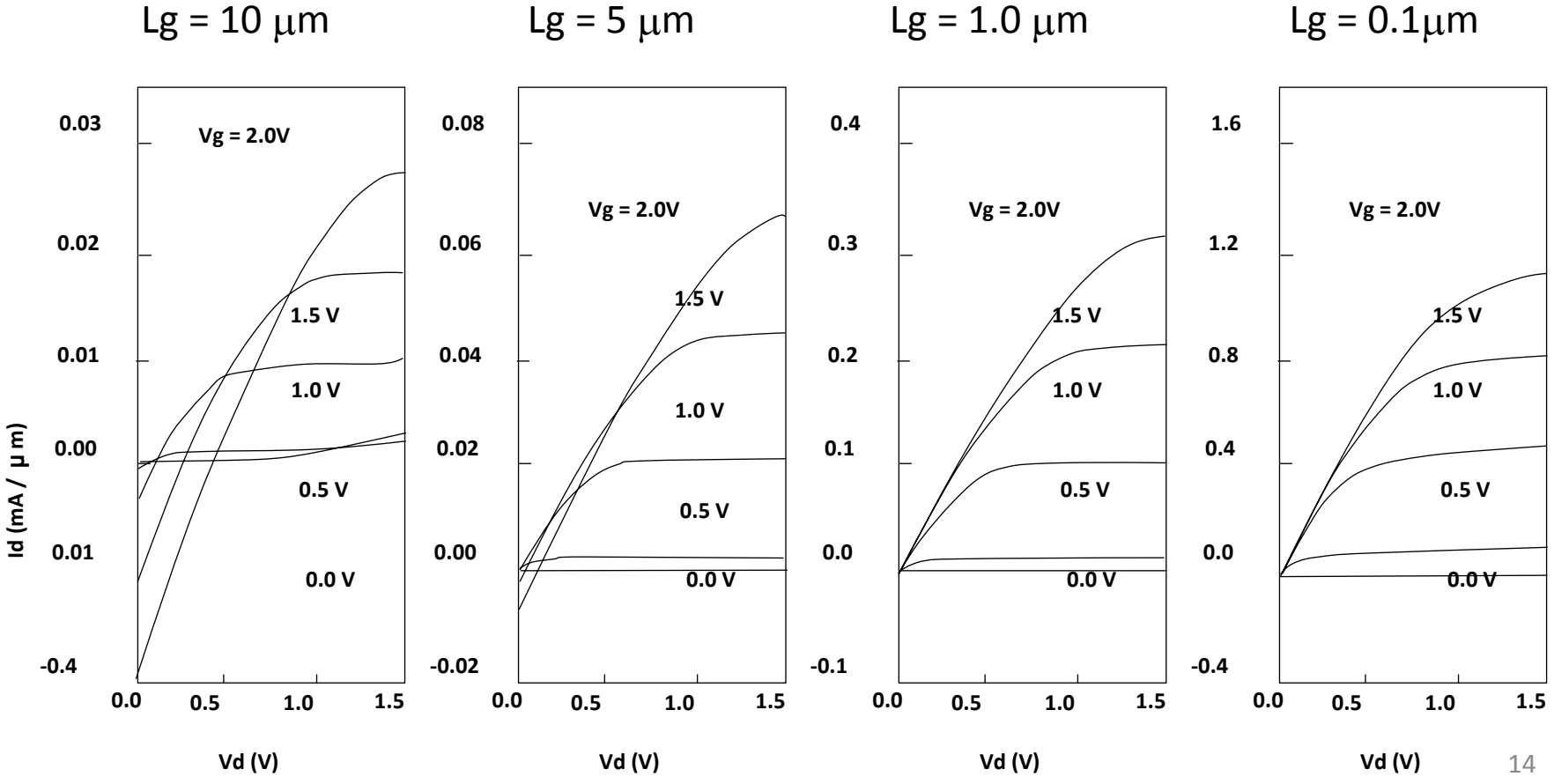


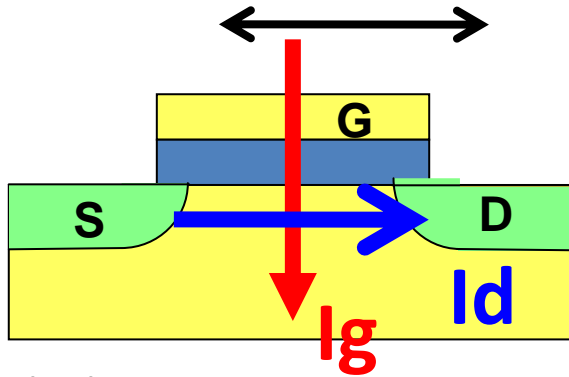
Direct tunneling leakage current start to flow when the thickness is 3 nm.



Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide





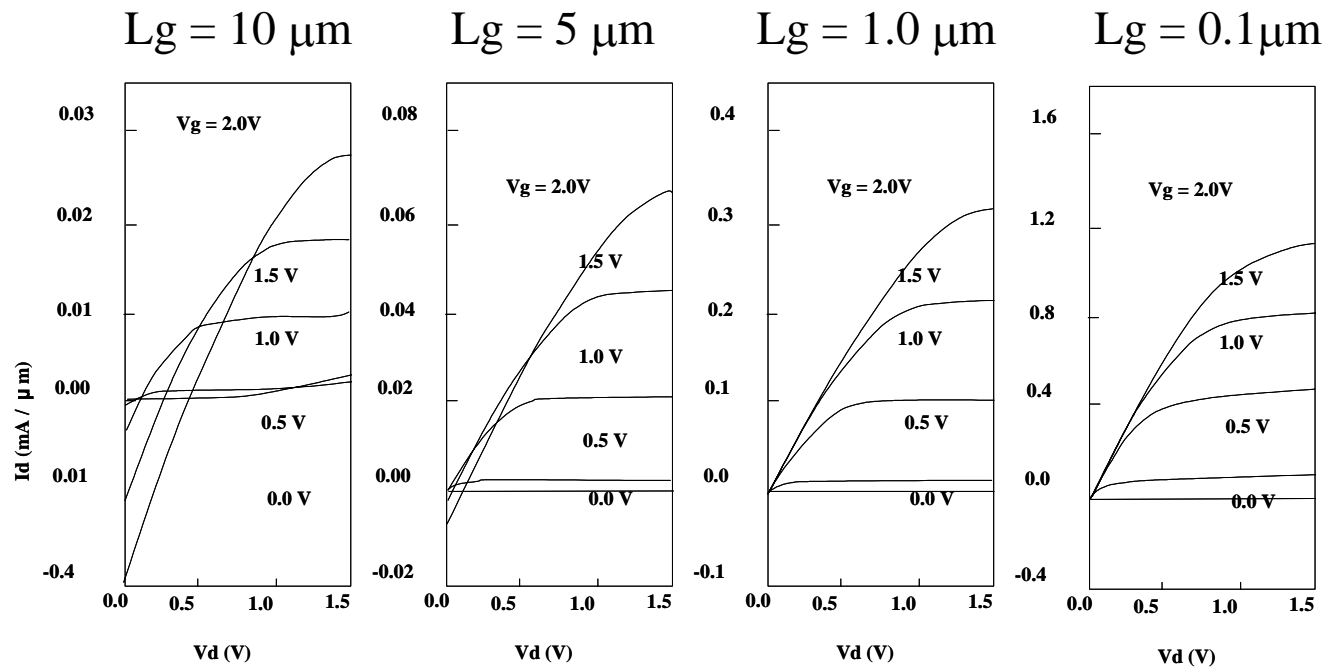
Gate leakage: $I_g \propto \text{Gate Area} \propto \text{Gate length (L}_g)$

Drain current: $I_d \propto 1/\text{Gate length (L}_g)$

$L_g \rightarrow$ small,

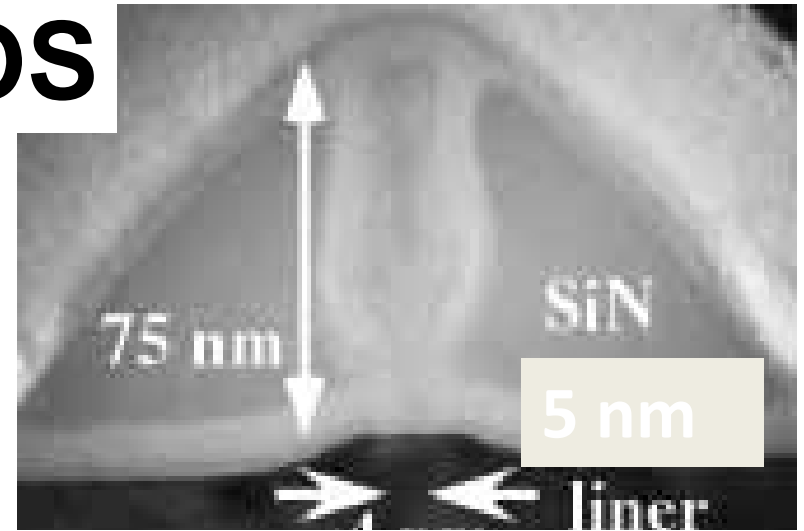
Then, $I_g \rightarrow$ small, $I_d \rightarrow$ large, Thus, $I_g/I_d \rightarrow$ very small

I_d
→

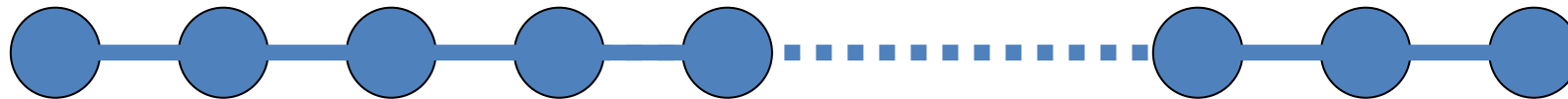


5 nm gate length CMOS

Is a Real Nano Device!!

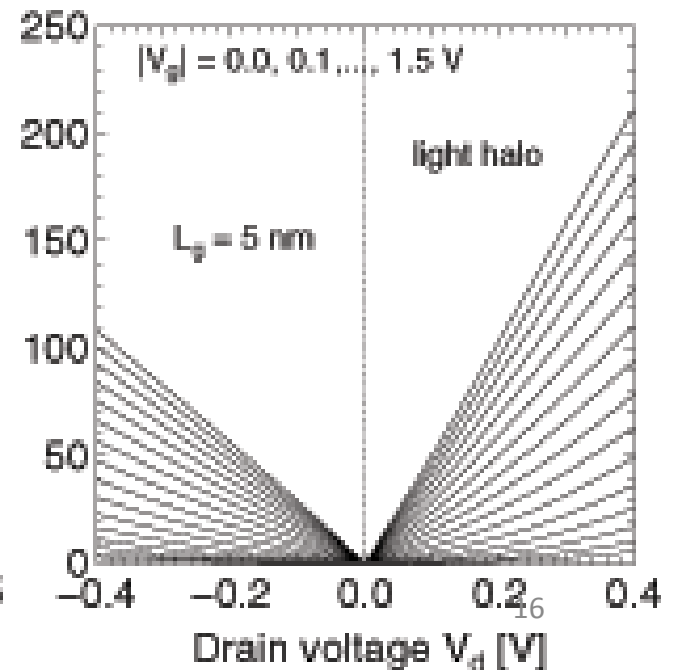
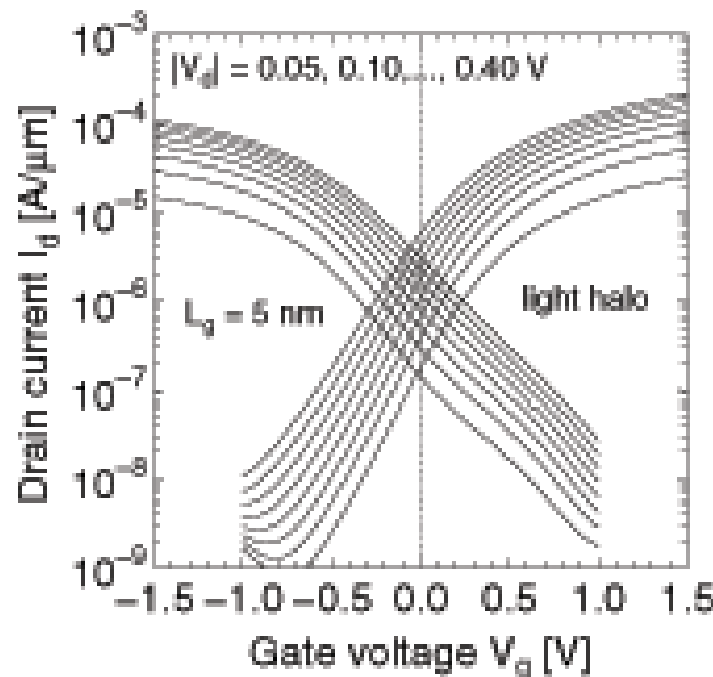


Length of 18 Si atoms



H. Wakabayashi
et.al, NEC

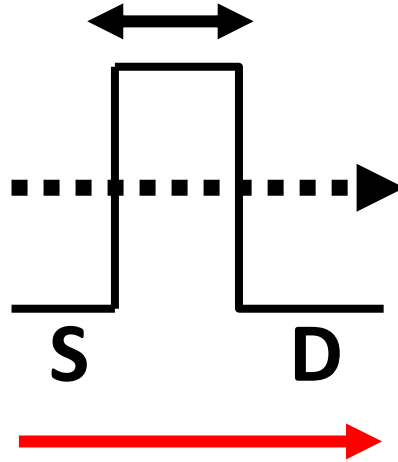
IEDM, 2003



Predicted limit now

Tunneling distance

3 nm



MOSFET operation

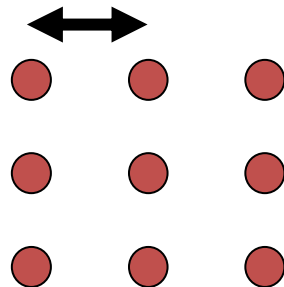
$L_g = 3 \text{ nm?}$

Below this,
no one knows future!

Ultimate Limit

Atom distance

0.3 nm



ITRS expect Lg less than 10nm

2009 ITRS Technology Trend: MPU gate length

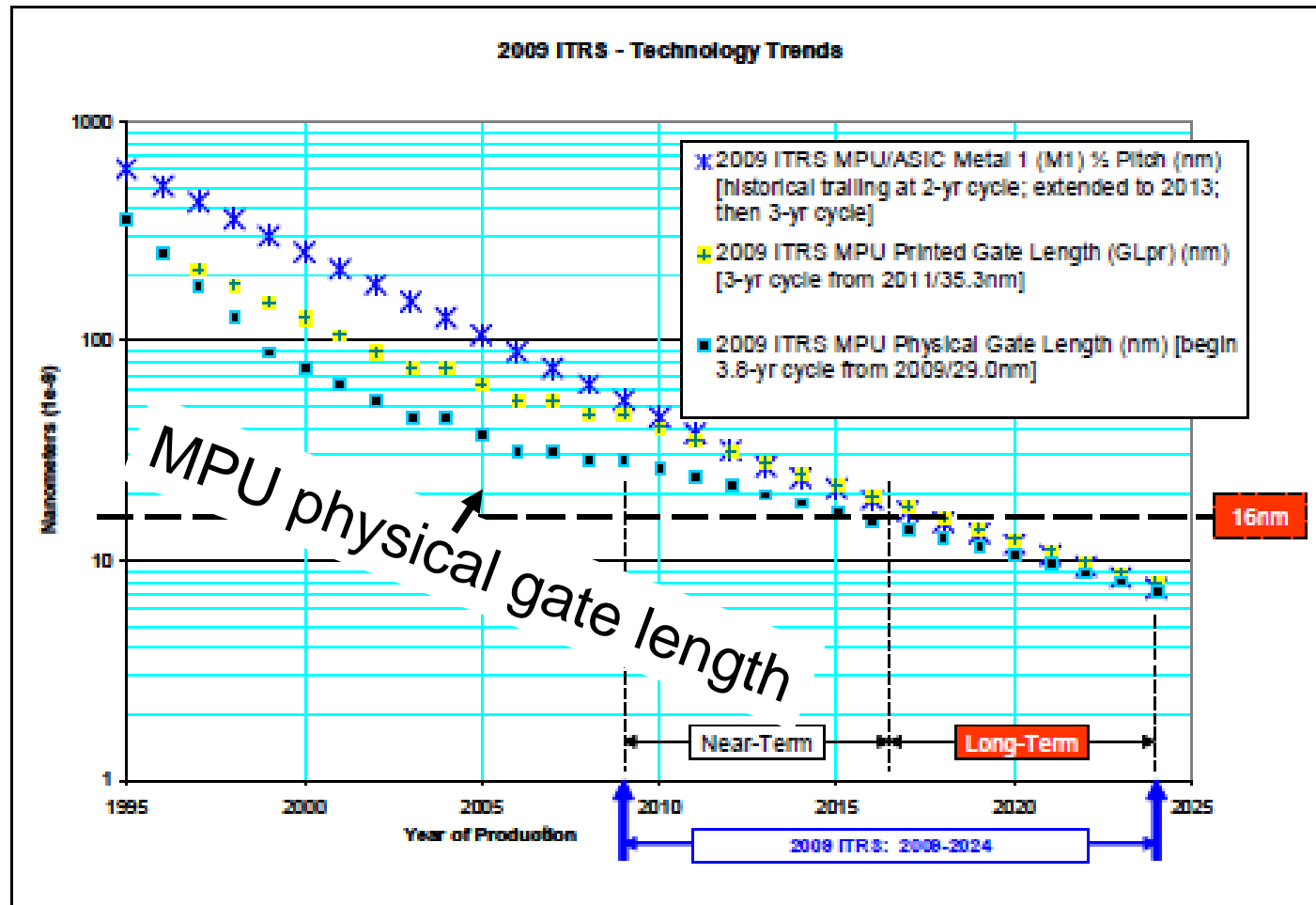


Figure 8b 2009 ITRS—MPU/high-performance ASIC Half Pitch and Gate Length Trends ITRS

How far can we go?

Past

0.7 times per 3 years In 40 years: 15 generations,
Size 1/200, Area 1/40,000

1973年



8 μm → 6 μm → 4 μm → 3 μm → 2 μm → 1.2 μm → 0.8 μm → 0.5 μm

→ 0.35 μm → 0.25 μm → 180nm → 130nm → 90nm → 65nm → 45nm

Now

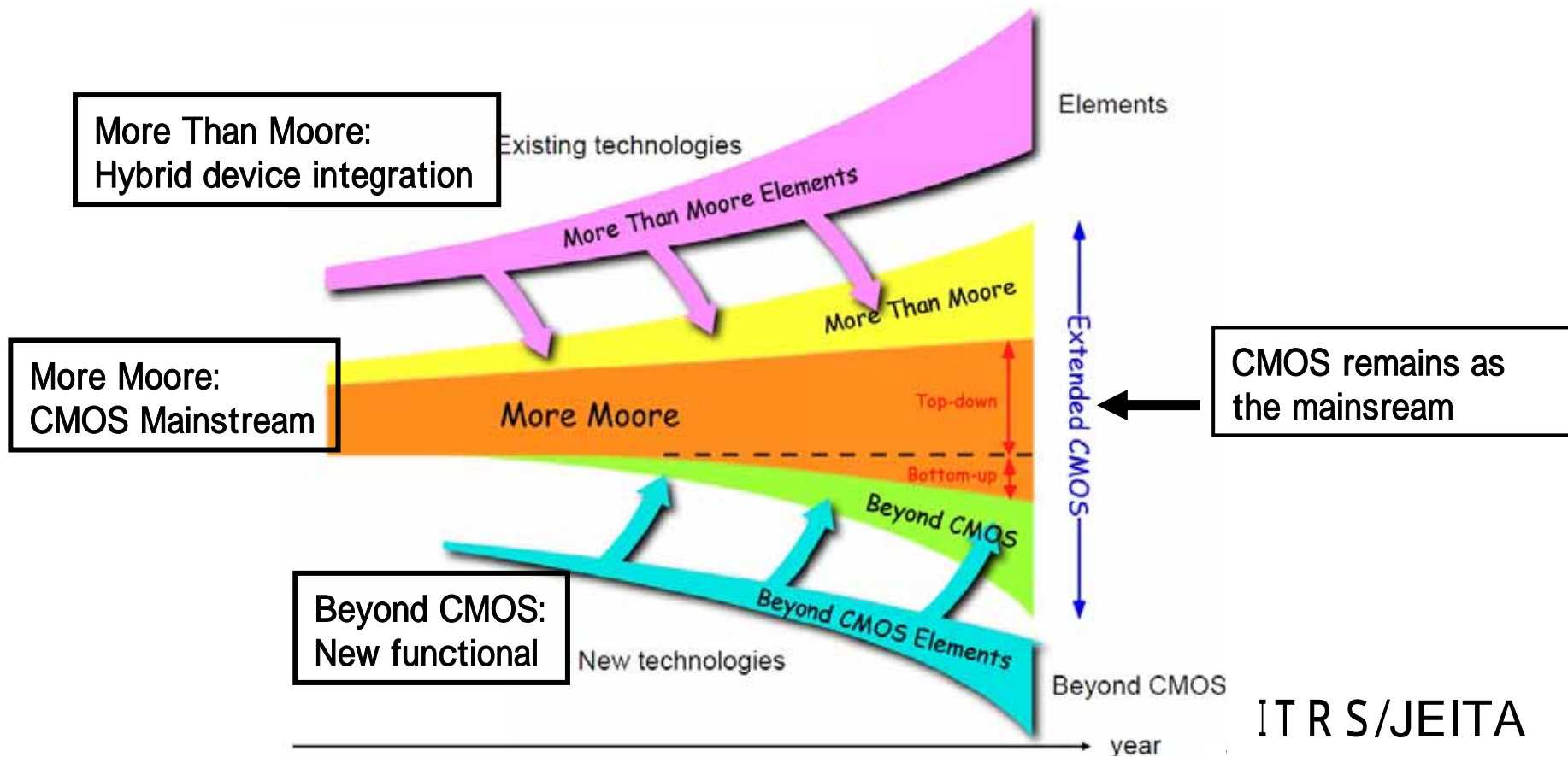


Future

→ 32nm → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

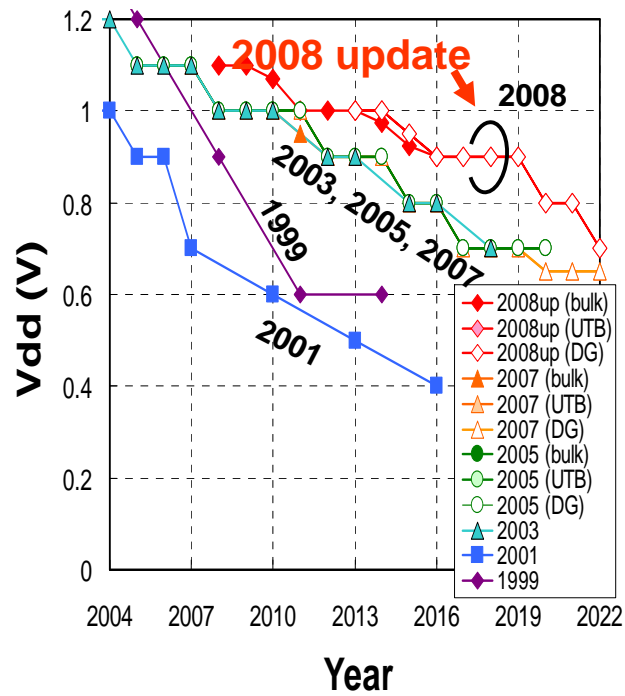
- At least 5,6 generations, for 15 ~ 20 years
- Hopefully 8 generations, for 30 years

CMOS scaling is the mainstream

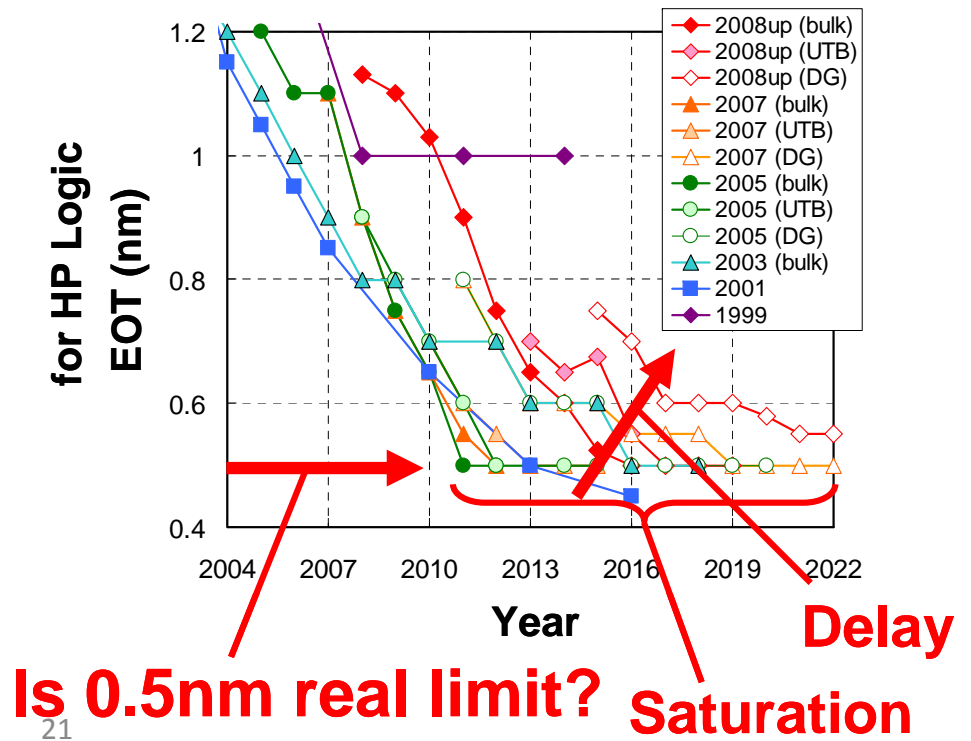


ITRS

Vdd stay high



ITRS EOT limit = 0.5 nm?

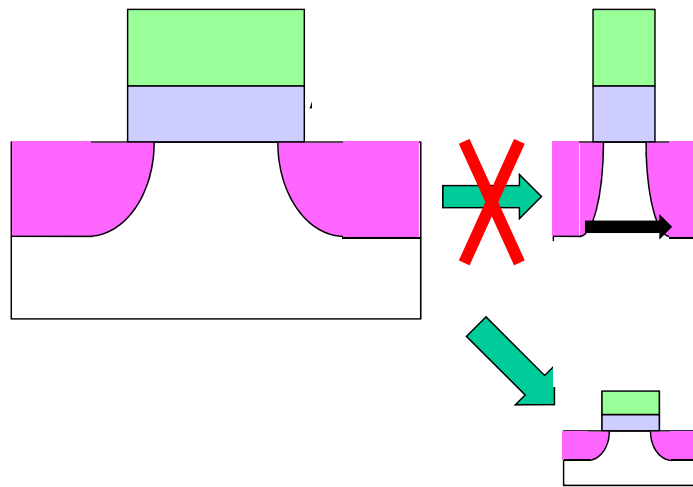


Scaling of high beyond 0.5 nm is important

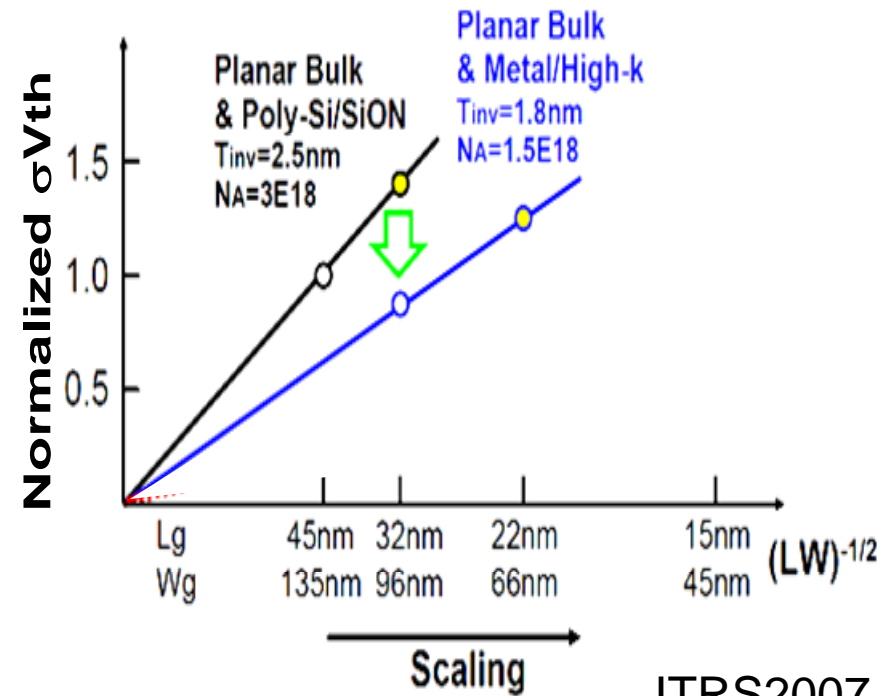
$$\text{Power of FET} = CV^2/2 \quad D^3 (=L^3)$$

Problems

- SCE
- Variation in V_{th}
- Increase in Off-leakage current

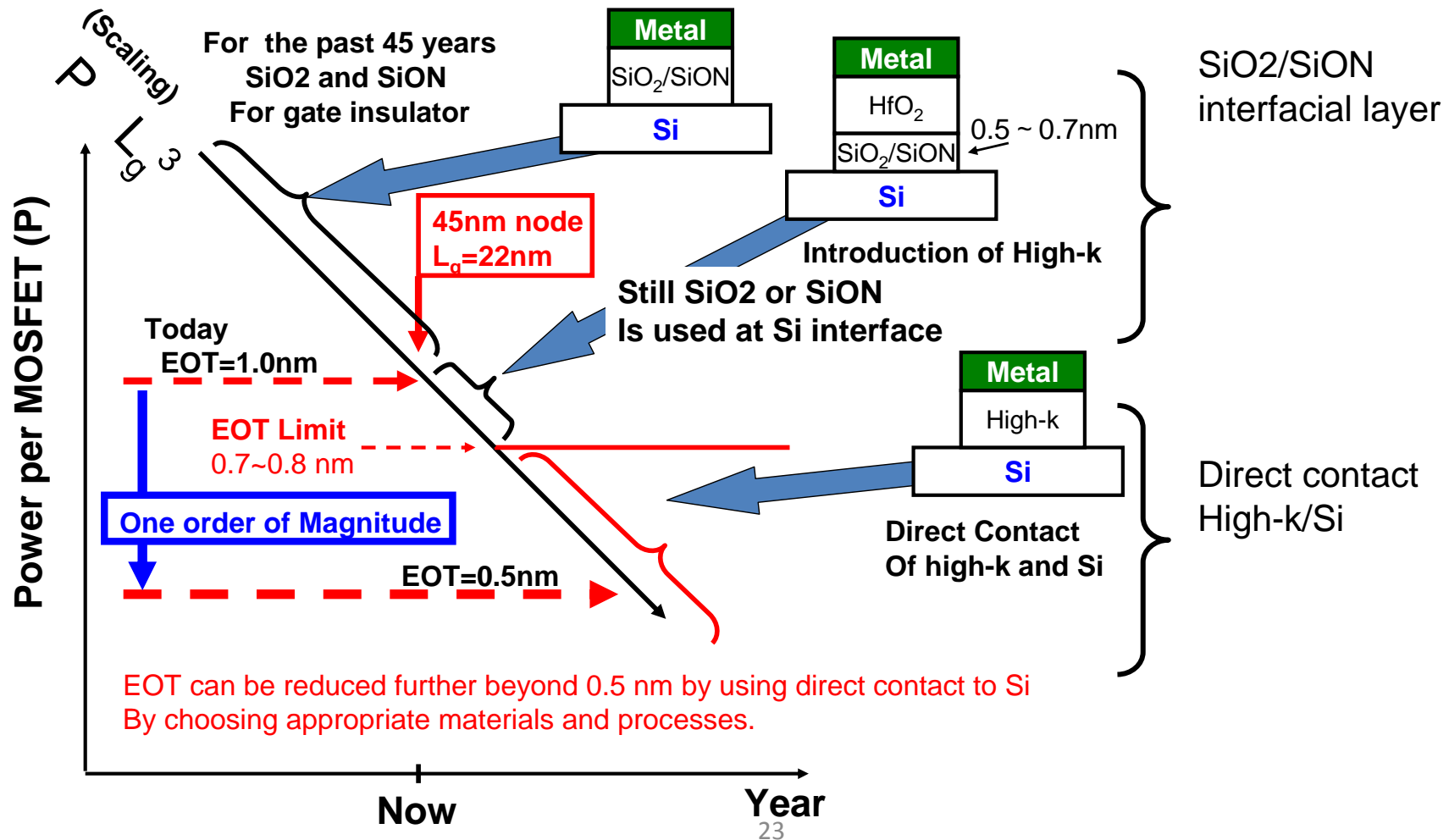


Solution

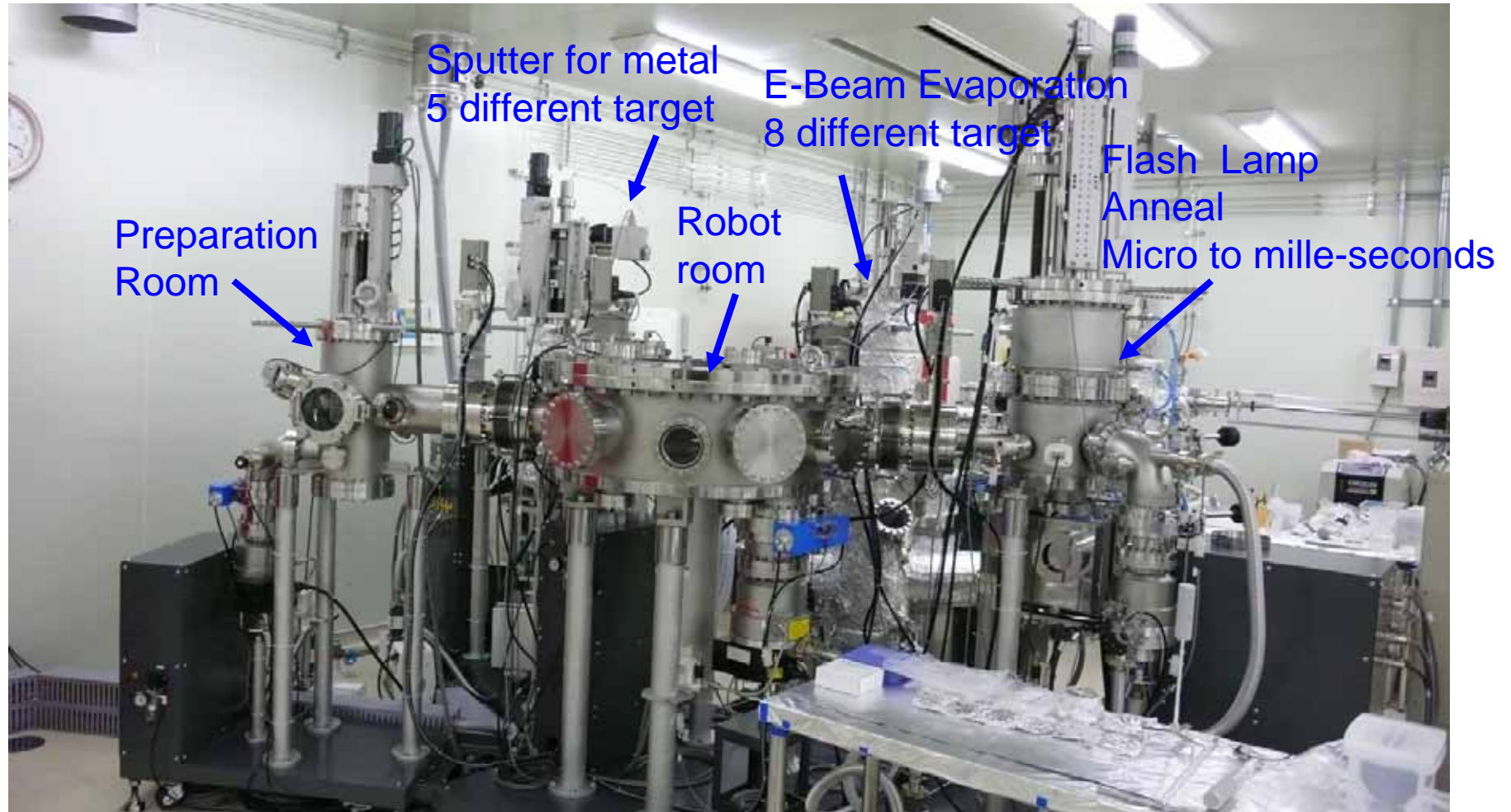


ITRS2007

Direct contact of high-k to Si

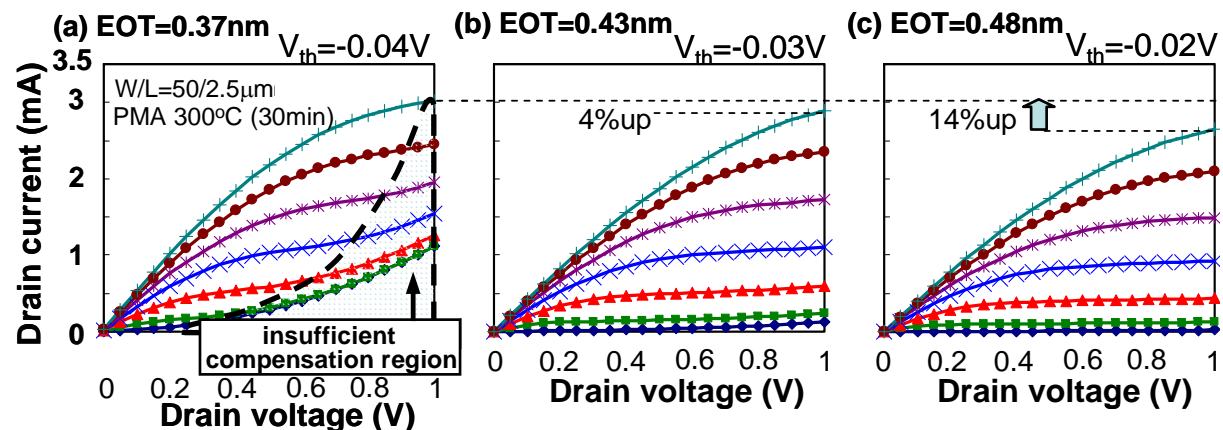


Cluster tool for high-k thin film deposition



Challenge to EOT $\sim 0.3\text{nm}$

EOT $< 0.5\text{nm}$ with Gain in Drive Current



14% of I_d increase is observed even at saturation region

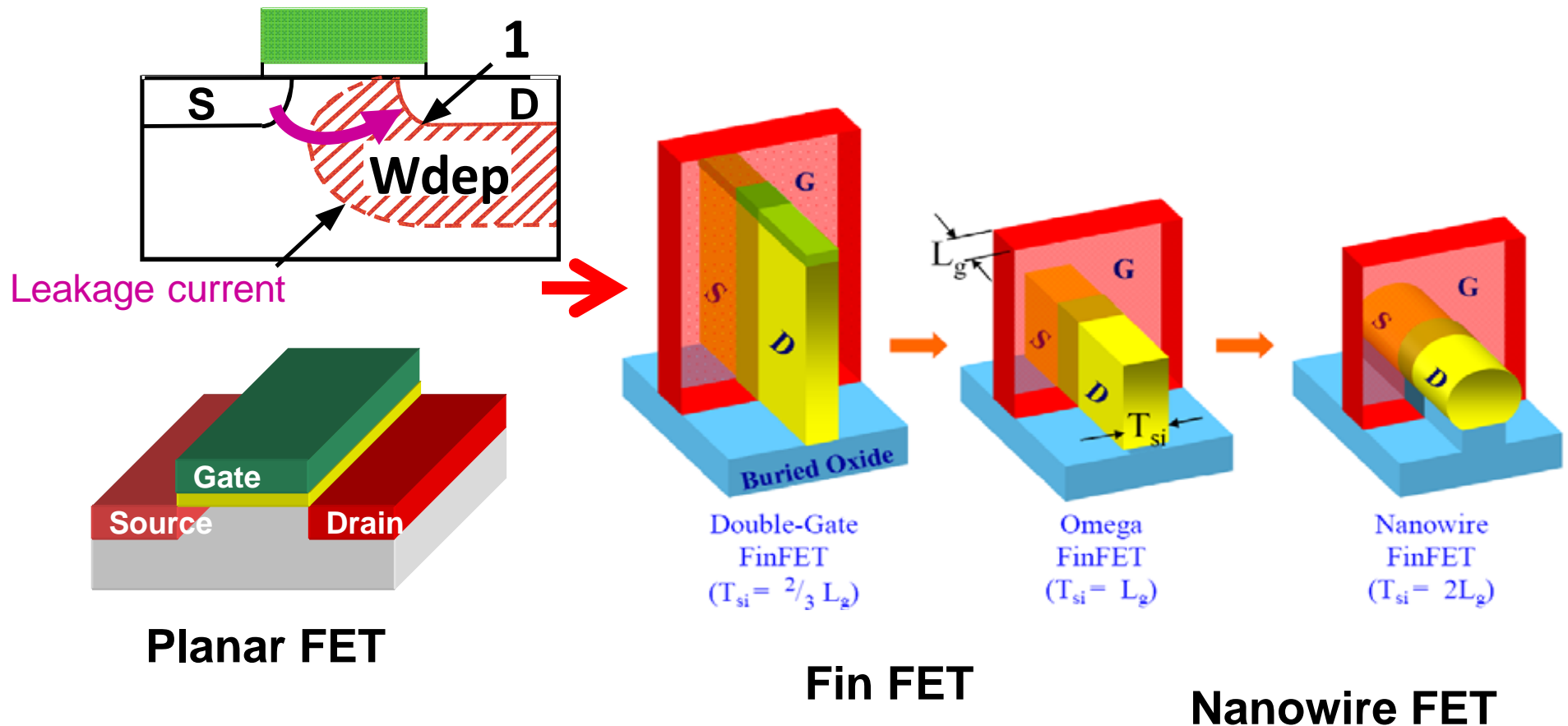


EOT below 0.4nm is still useful for scaling

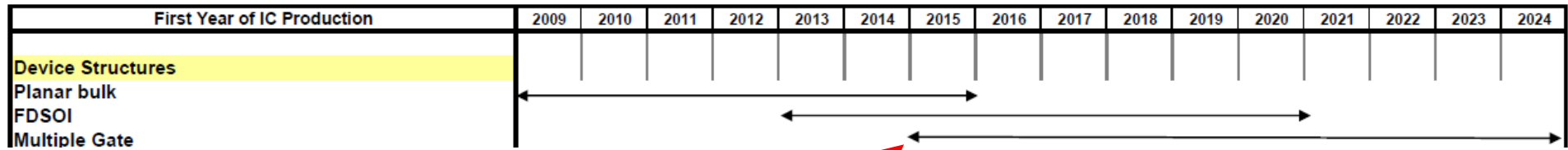
Si Nanowire FET

Because of off-leakage control,

Planar \rightarrow Fin \rightarrow Nanowire

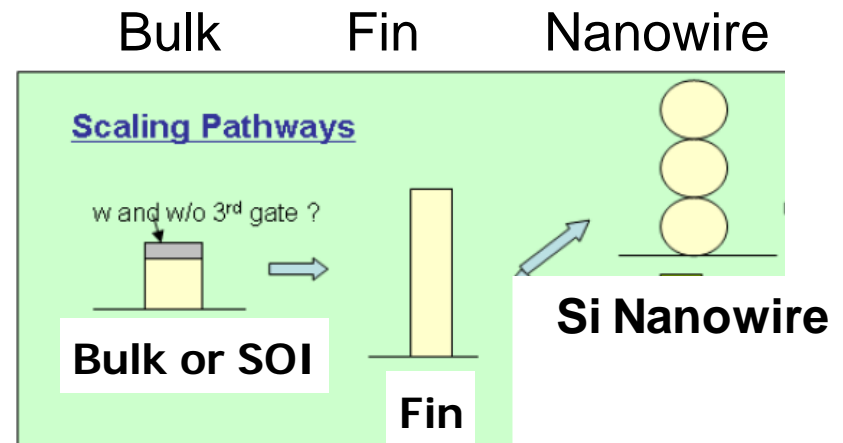


Nanowire FET



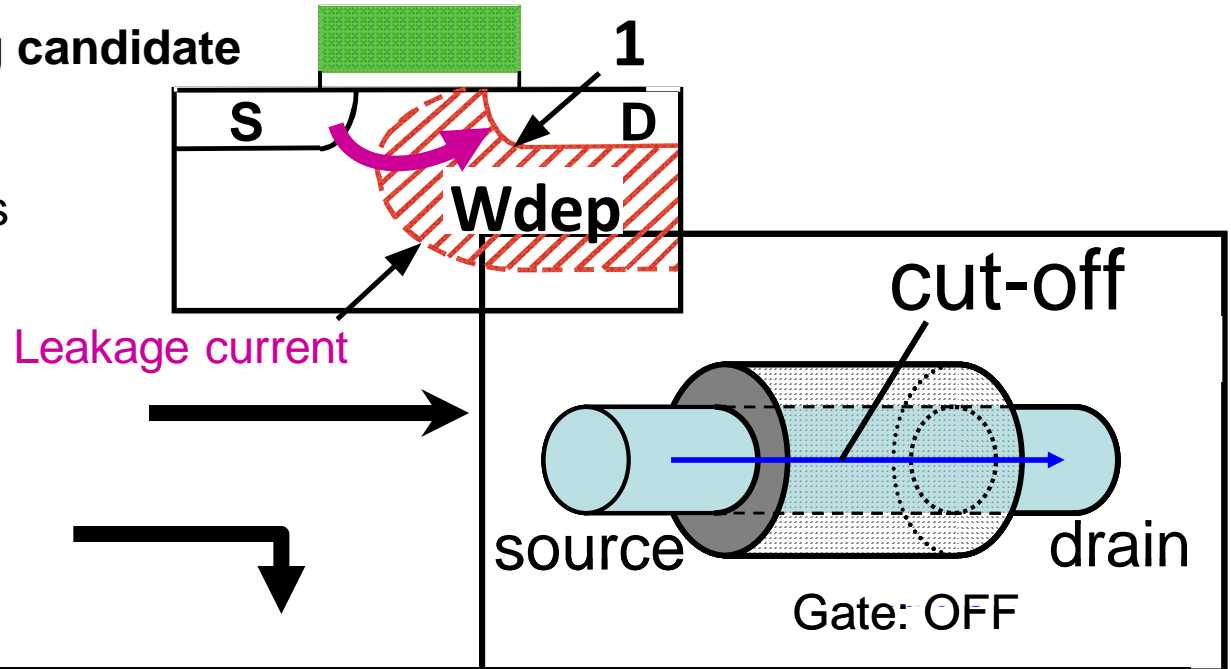
Multiple Gate (Fin)FET

ITRS 2009



Si nanowire FET as a strong candidate

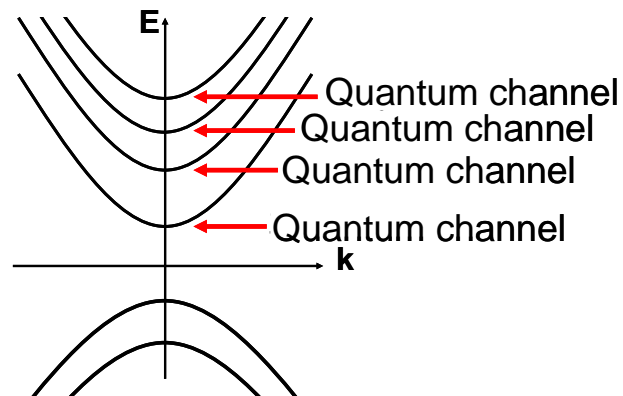
1. Compatibility with current CMOS process
2. Good controllability of I_{OFF}
3. High drive current



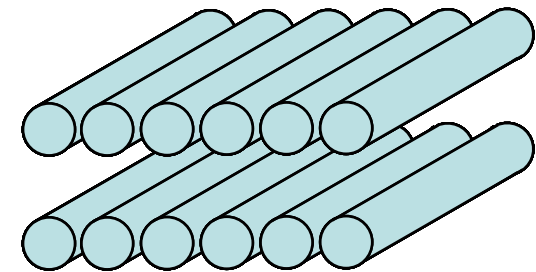
1D ballistic conduction

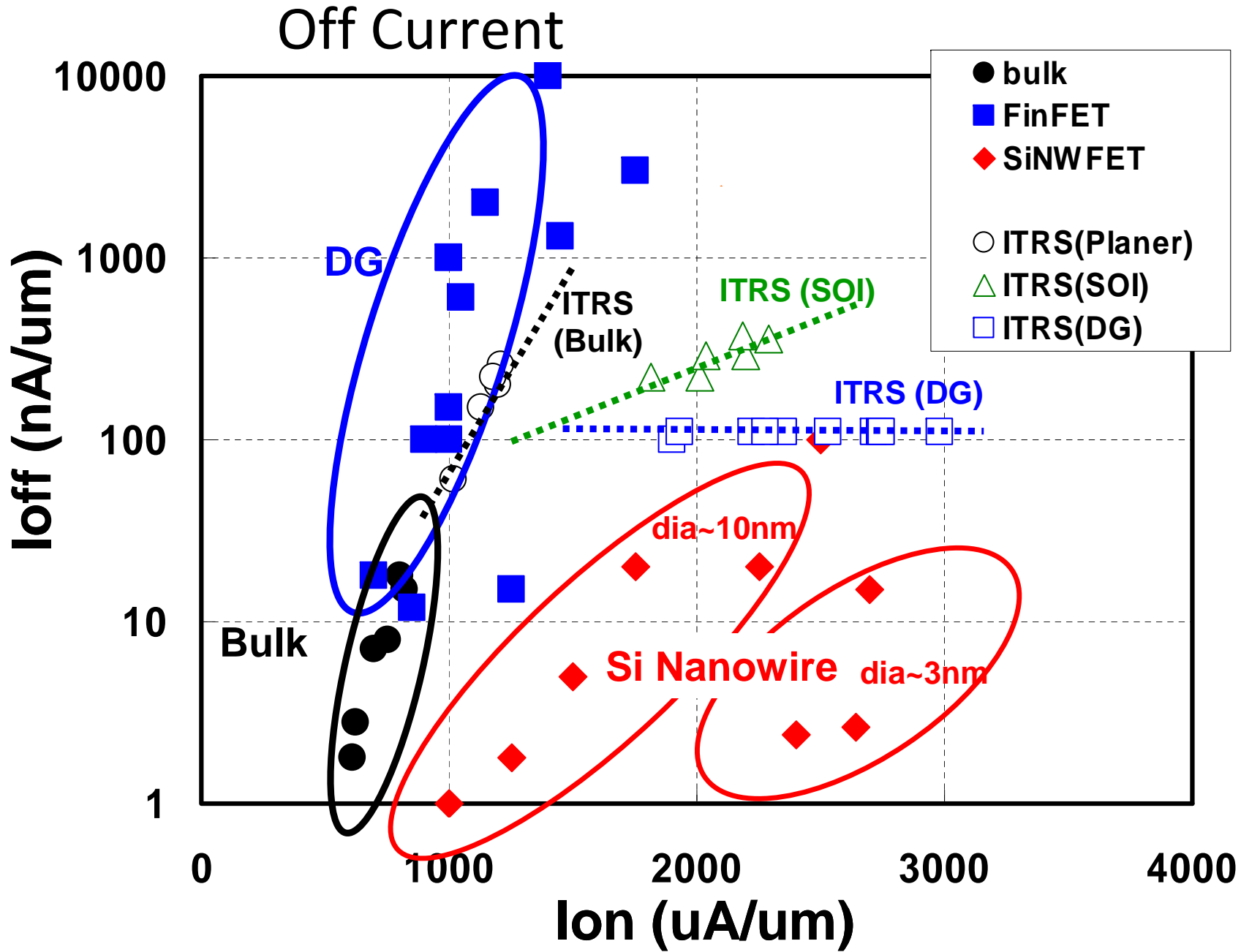


Multi quantum Channel



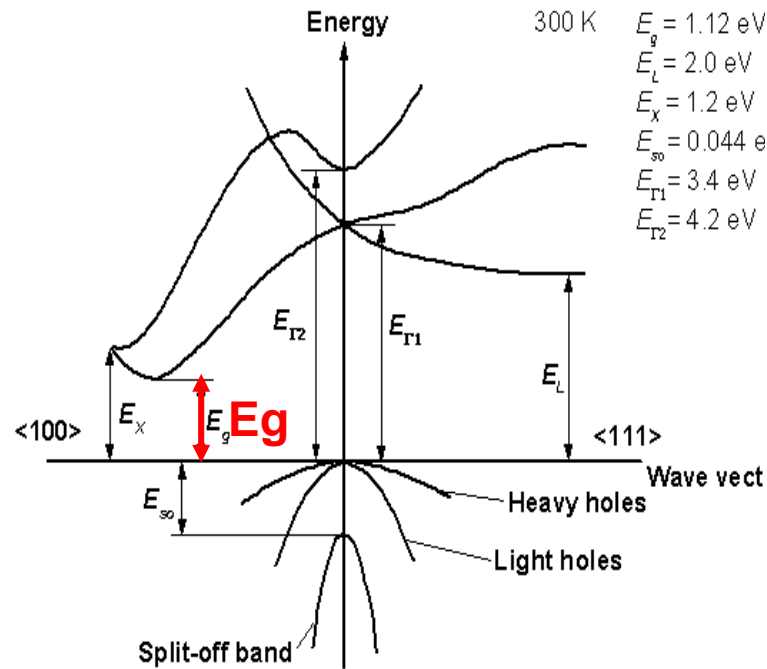
High integration of wires



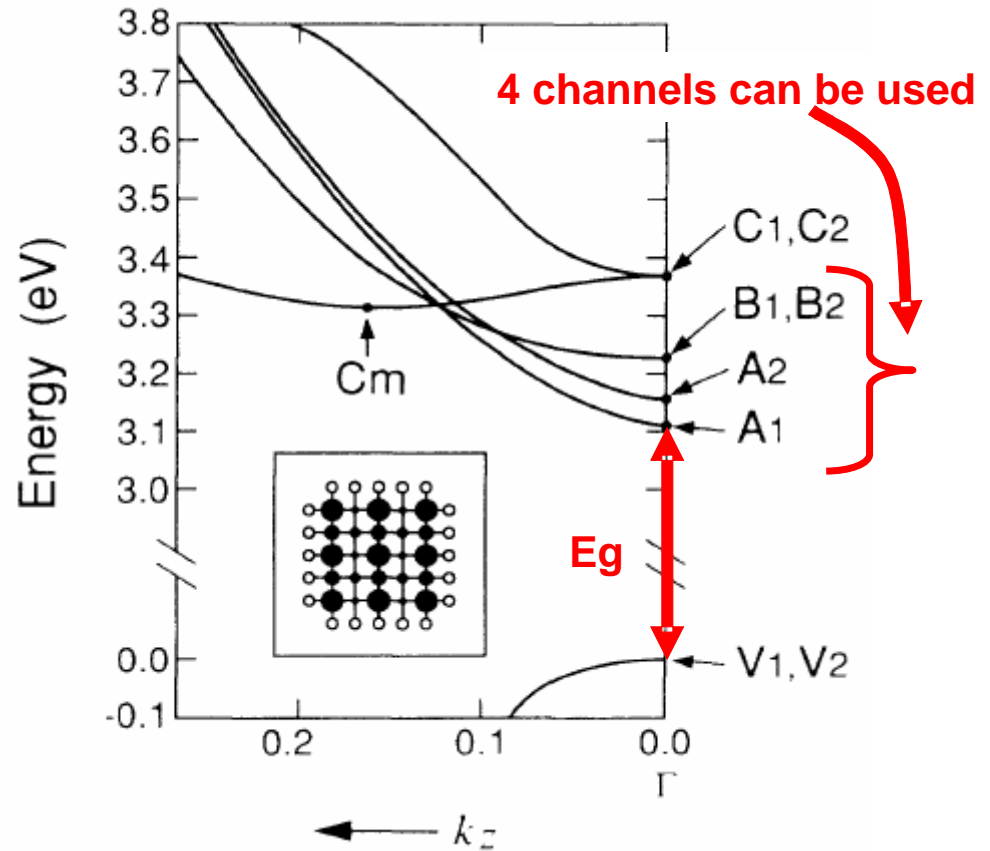


Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



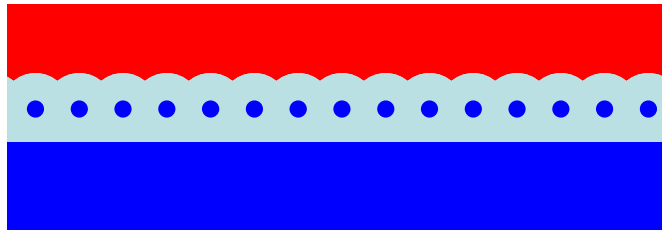
Energy band of Bulk Si



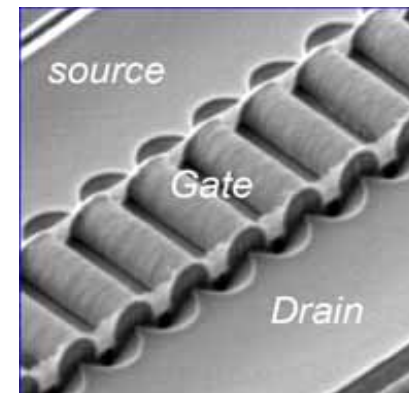
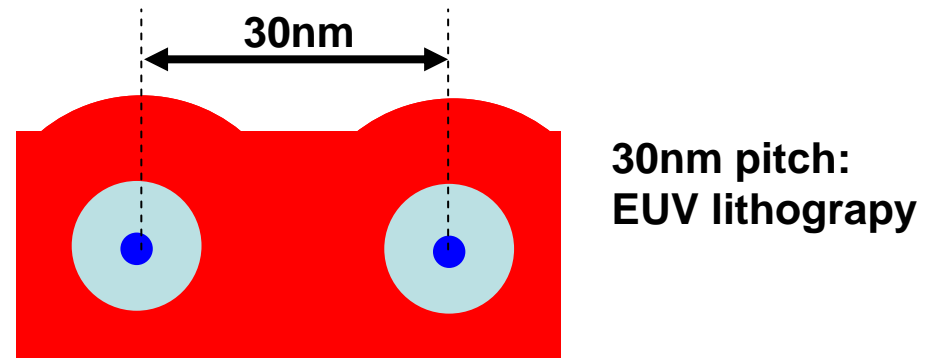
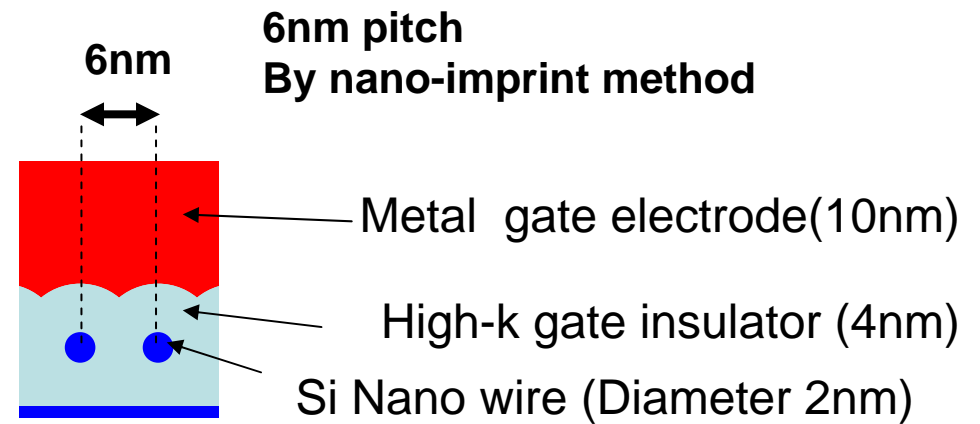
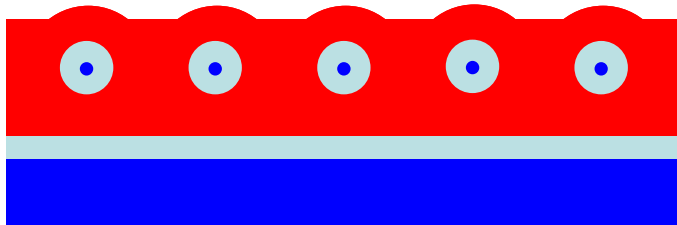
Energy band of 3 x 3 Si wire

Maximum number of wires per 1 μm

Front gate type MOS 165 wires / μm

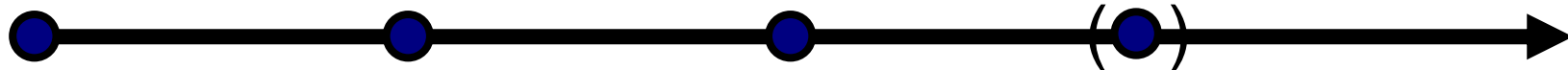


Surrounded gate type MOS 33 wires / μm

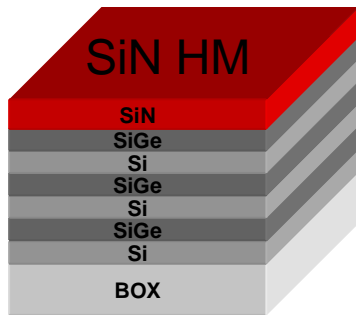


Surrounded gate MOS

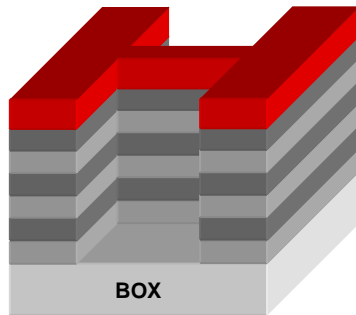
Device fabrication



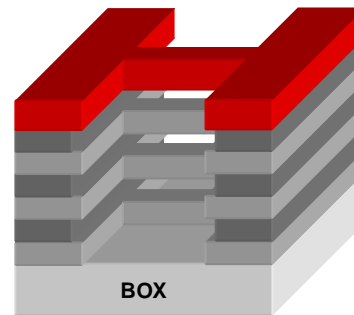
Si/Si_{0.8}Ge_{0.2}
superlattice
epitaxy on SOI



Anisotropic
etching
of these layers



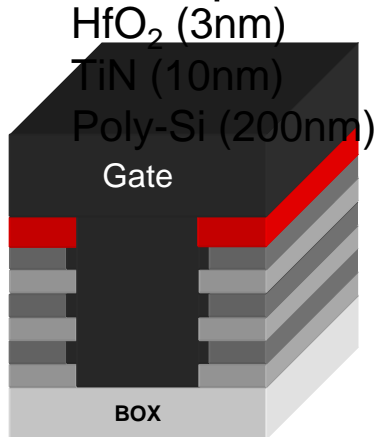
Isotropic
etching
of SiGe



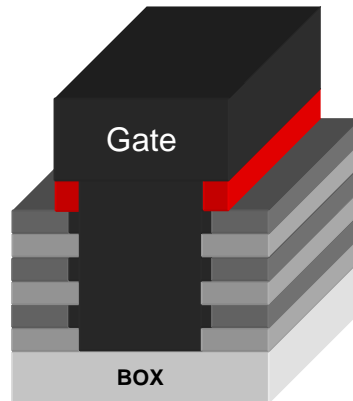
The NW diameter
is controllable
down to 5 nm
by self limited oxidation.



Gate depositions



Gate etching



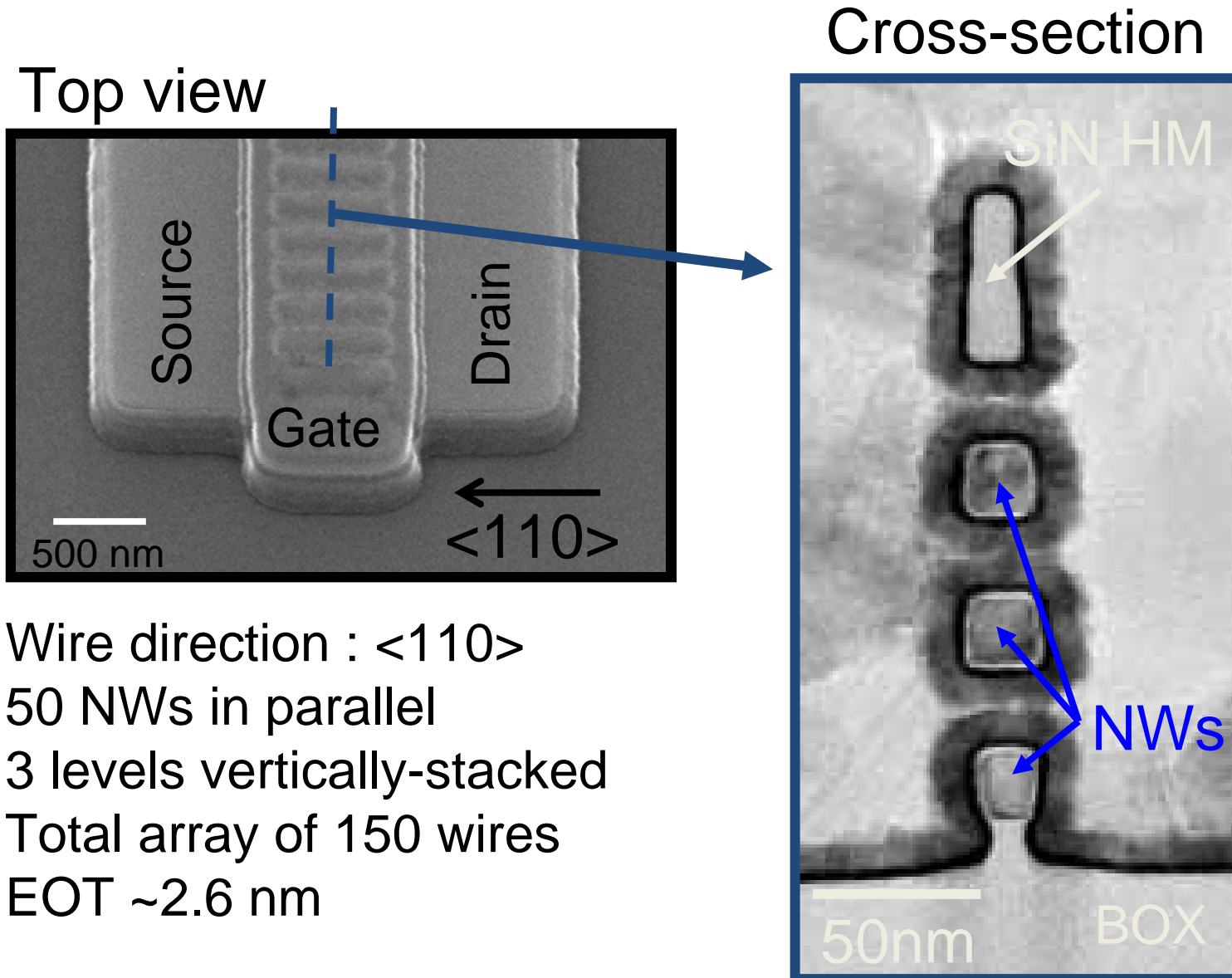
S/D implantation
Spacer formation
Activation anneal
Salicidation

Standard
Back-End
of-Line
Process

Process Details :

C. Dupre *et al.*,
IEDM Tech. Dig., p.749, 2008

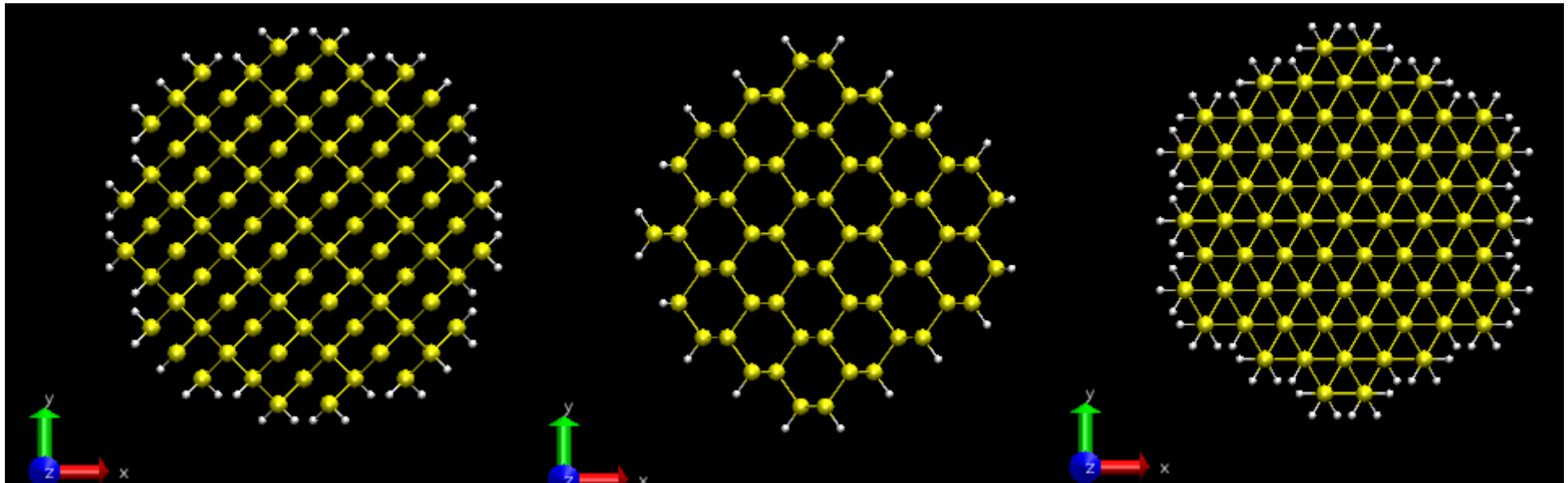
3D-stacked Si NWs with Hi-k/MG



SiNW Band structure calculation

Cross section of Si NW

First principal calculation,



D=1.96nm

[001]

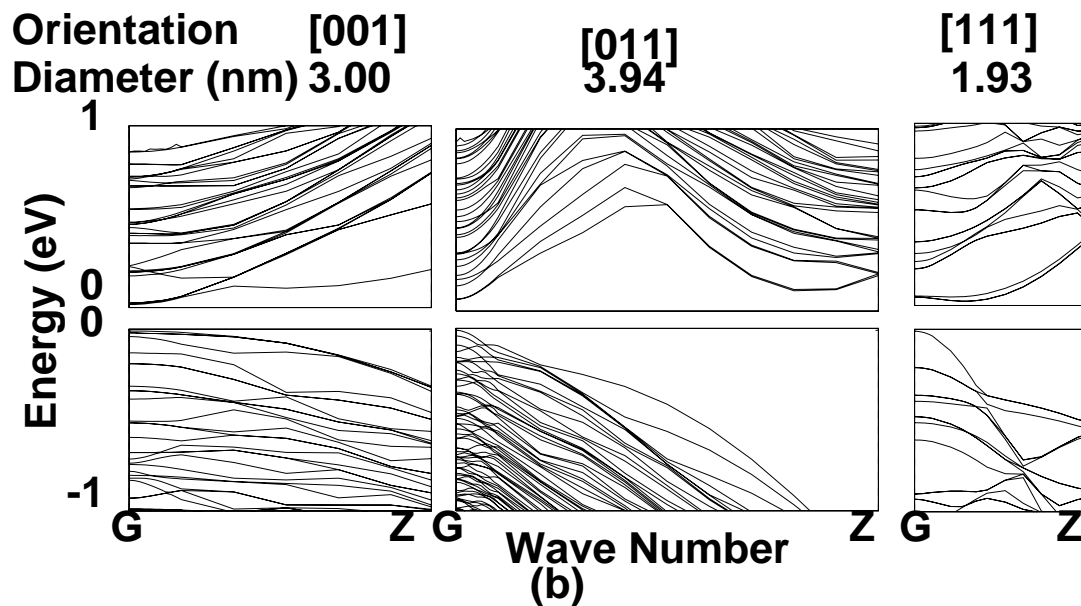
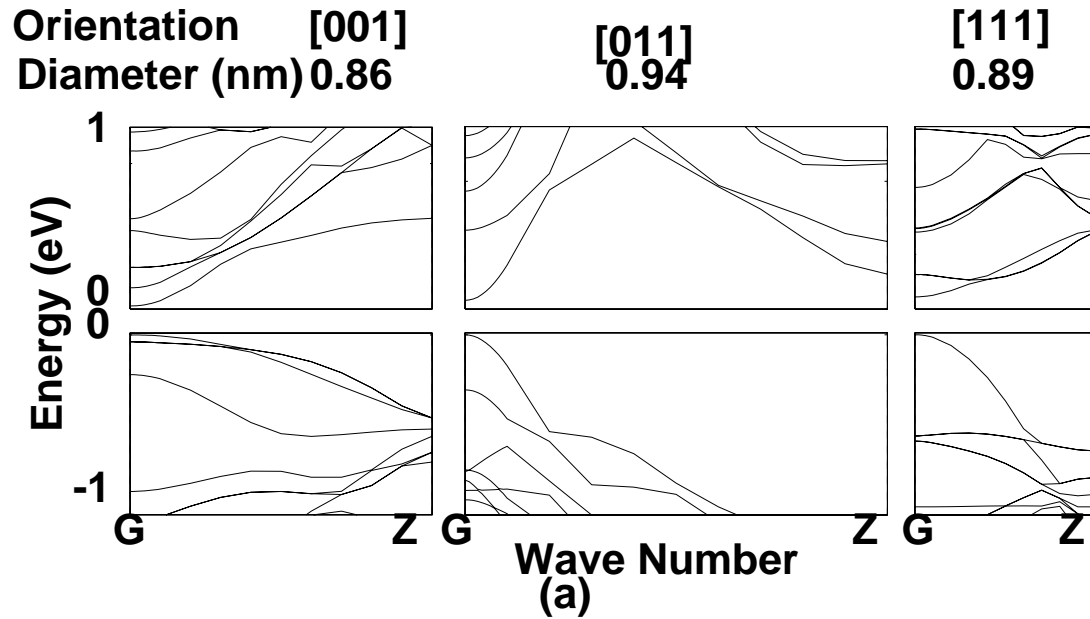
D=1.94nm

[011]

D=1.93nm

[111]

Si nanowire FET with 1D Transport

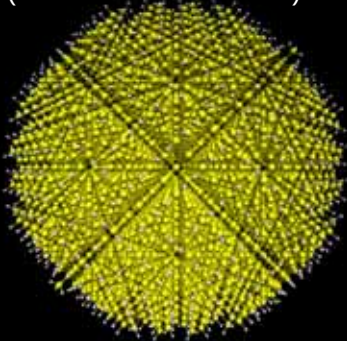


Small mass with [011]

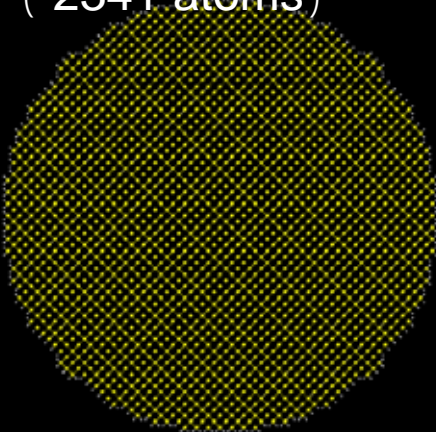
**Large number of
quantum channels
with [001]**

Atomic models of a Si quantum dot and Si nanowires

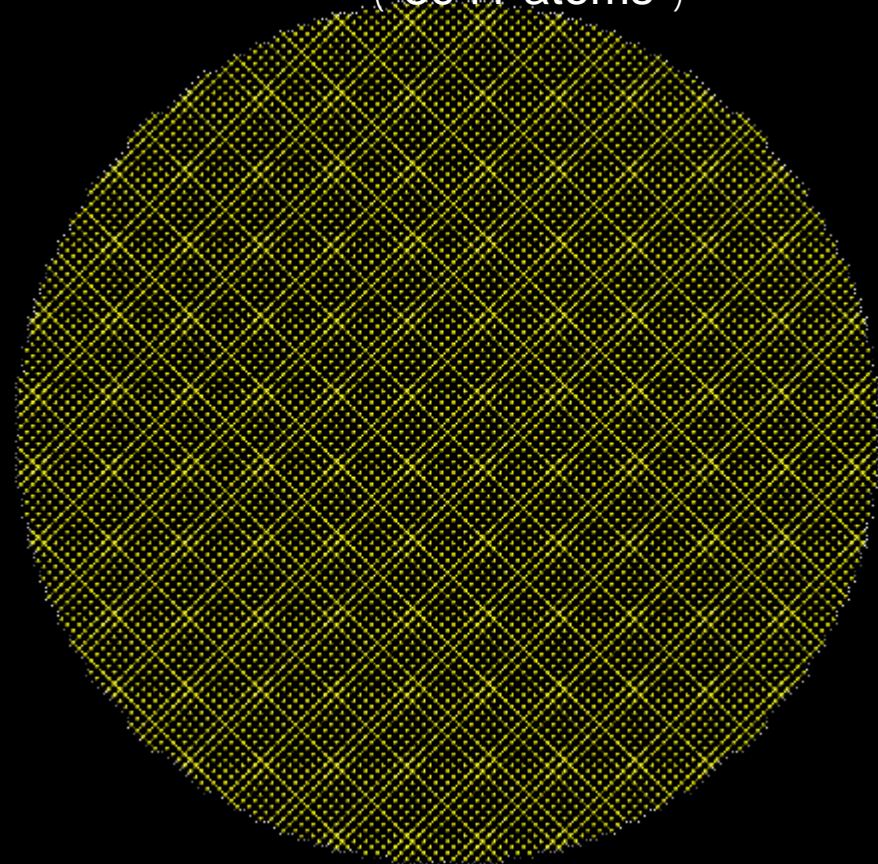
6.6 nm diameter SiQD
(8651 atoms)



10 nm diameter Si(100)NW
(2341 atoms)



20 nm diameter Si(100)NW
(8941 atoms)



RSDFT – suitable for parallel first-principles calculation -

- ✓ Real-Space Finite-Difference Higher-order finite difference pseudopotential method
- ✓ Sparse Matrix J. R. Chelikowsky et al., Phys. Rev. B, (1994)
- ✓ FFT free (FFT is inevitable in the conventional plane-wave code)
- ✓ MPI (Message Passing Interface) library

3D grid is divided by several regions for parallel computation.

Kohn-Sham eq. (finite-difference)

$$\left(-\frac{1}{2} \nabla^2 + v_s[\rho](\mathbf{r}) + \hat{v}_{nloc}^{PP}(\mathbf{r}) \right) \phi_n(\mathbf{r}) = \varepsilon_n \phi_n(\mathbf{r})$$

Higher-order finite difference

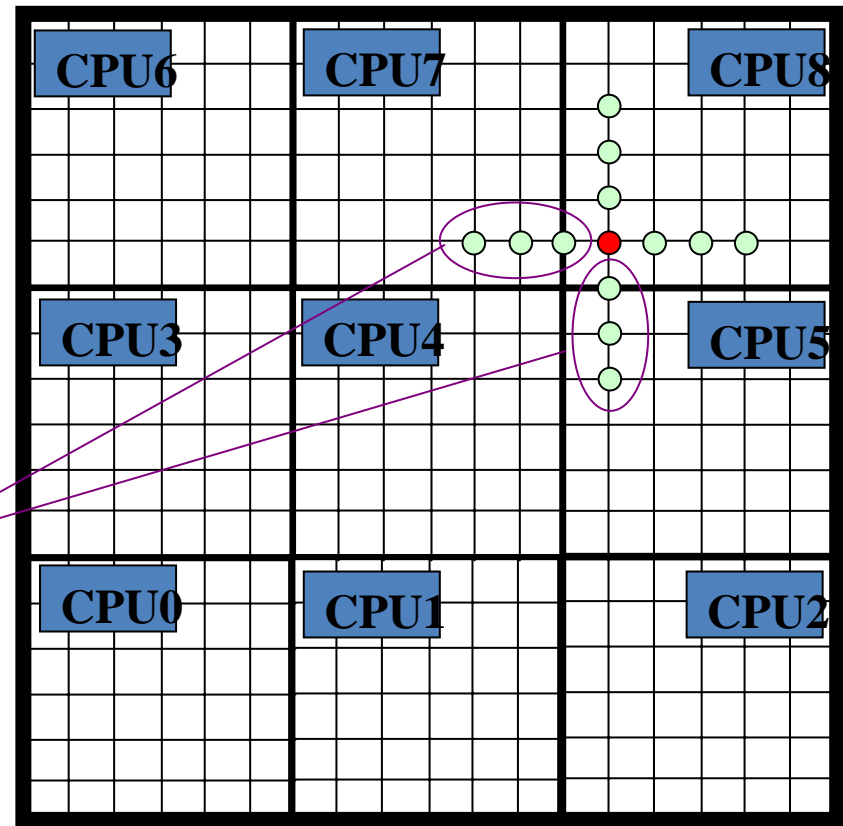
$$\frac{\partial^2}{\partial x^2} \psi_n(x, y, z) \approx \sum_{m=-6}^6 C_m \psi_n(x + m\Delta x, y, z)$$

MPI_ISEND, MPI_IRECV

Integration

$$\int \psi_m(\mathbf{r}) \psi_n(\mathbf{r}) d\mathbf{r} \approx \sum_{i=1}^{Mesh} \psi_m(\mathbf{r}_i) \psi_n(\mathbf{r}_i) \Delta x \Delta y \Delta z$$

MPI_ALLREDUCE



Massively Parallel Computing

with our recently developed code “RSDFT”

Iwata et al, J. Comp. Phys., to be published

Real-Space Density-Functional Theory code (RSDFT)

Based on the finite-difference pseudopotential method (J. R. Chelikowsky et al., PRB1994)

Highly tuned for massively parallel computers

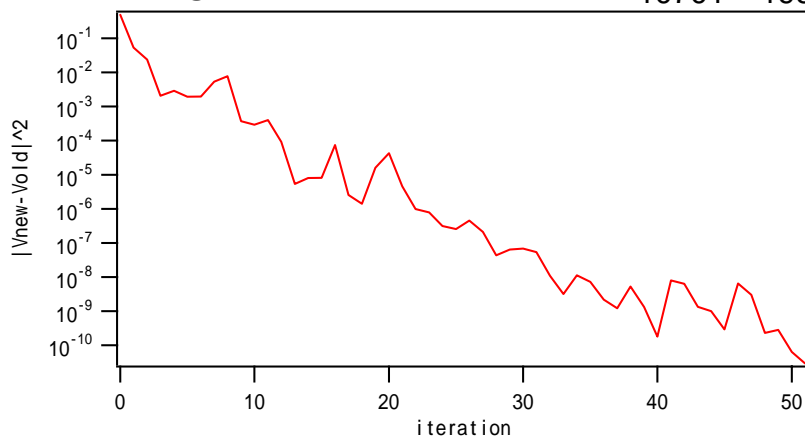
Computations are done on a massively-parallel cluster **PACS-CS** at University of Tsukuba.

(Theoretical Peak Performance = 5.6GFLOPS/node)



e.g.) The system over 10,000 atoms $\text{Si}_{10701}\text{H}_{1996}$
(7.6 nm diameter Si dot)

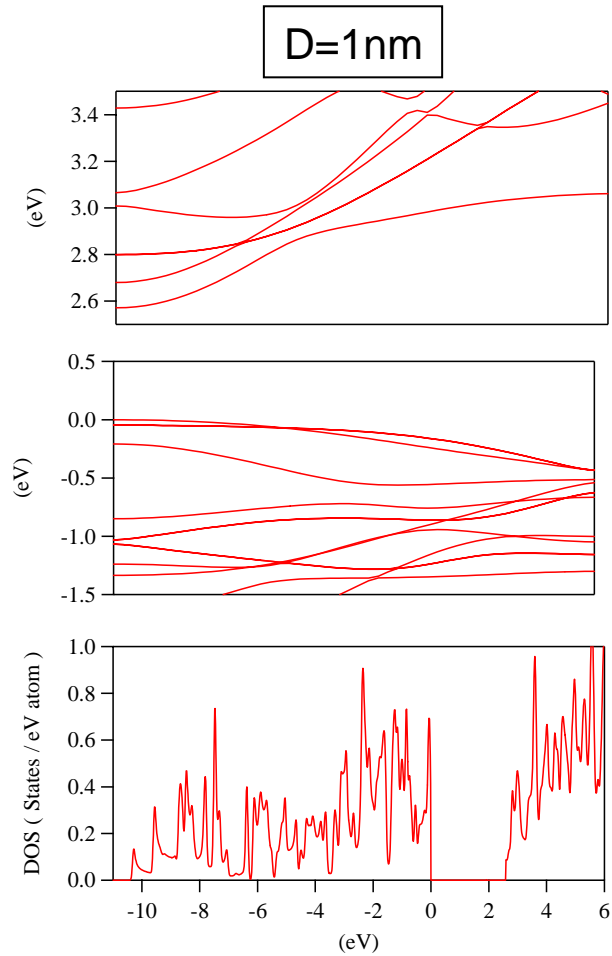
Convergence behavior for $\text{Si}_{10701}\text{H}_{1996}$ Grid points = 3,402,059
Bands = 22,432



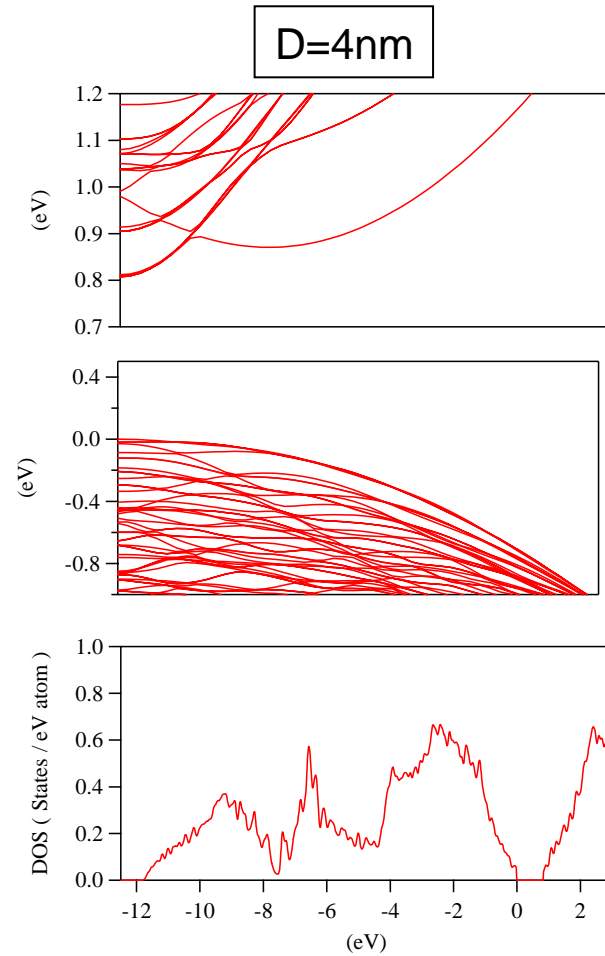
Computational Time (with 1024 nodes of PACS-CS)

6781 sec. \times 60 iteration step = 113 hour

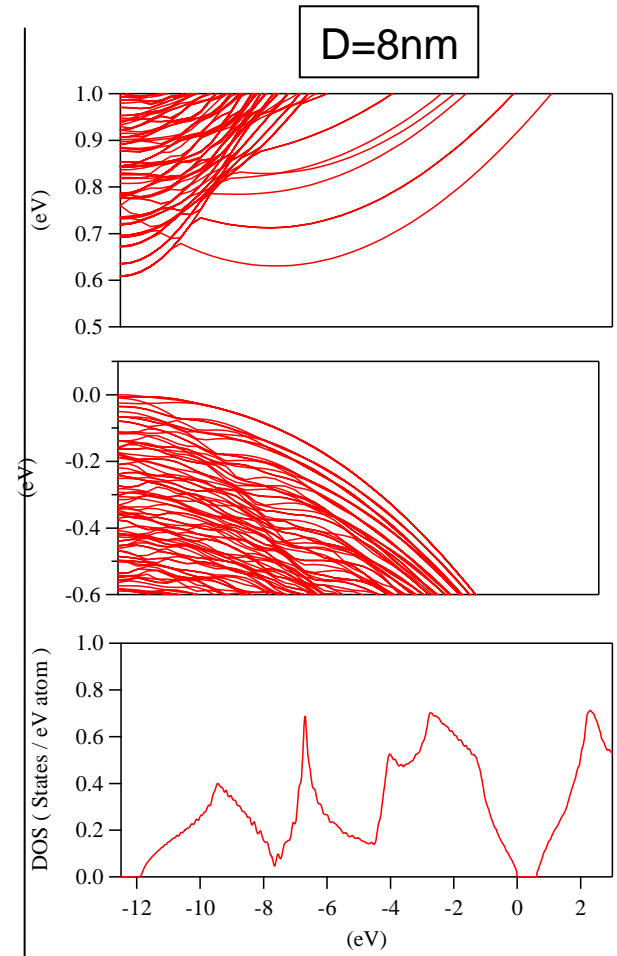
Band Structure and DOS of Si(100)NWs (D=1nm, 4nm, and 8nm)



D=1 nm
 Si₂₁H₂₀ (41 atoms)
 KS band gap=2.60eV



D = 4 nm
 Si₃₄₁H₈₄ (425 atoms)
 KS band gap = 0.81eV

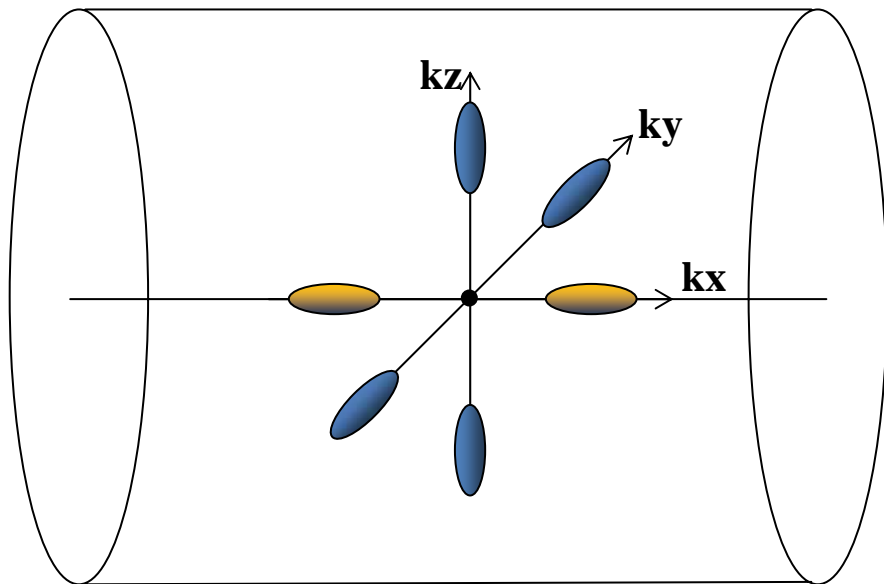
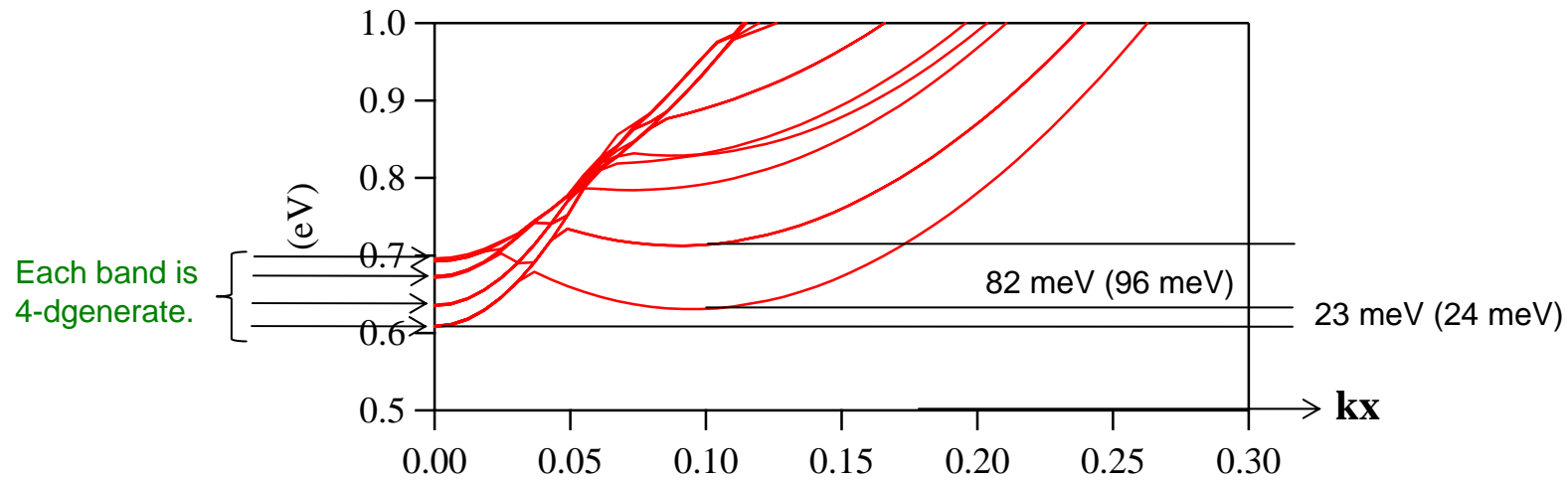


D=8 nm
 Si₁₃₆₁H₁₆₄ (1525 atoms)
 KS band gap=0.61eV

KS band gap of bulk (LDA) = 0.53eV

Band structure of 8-nm-diameter Si nanowire near the CBM

- KS band gap = 0.608 eV (@ Γ)

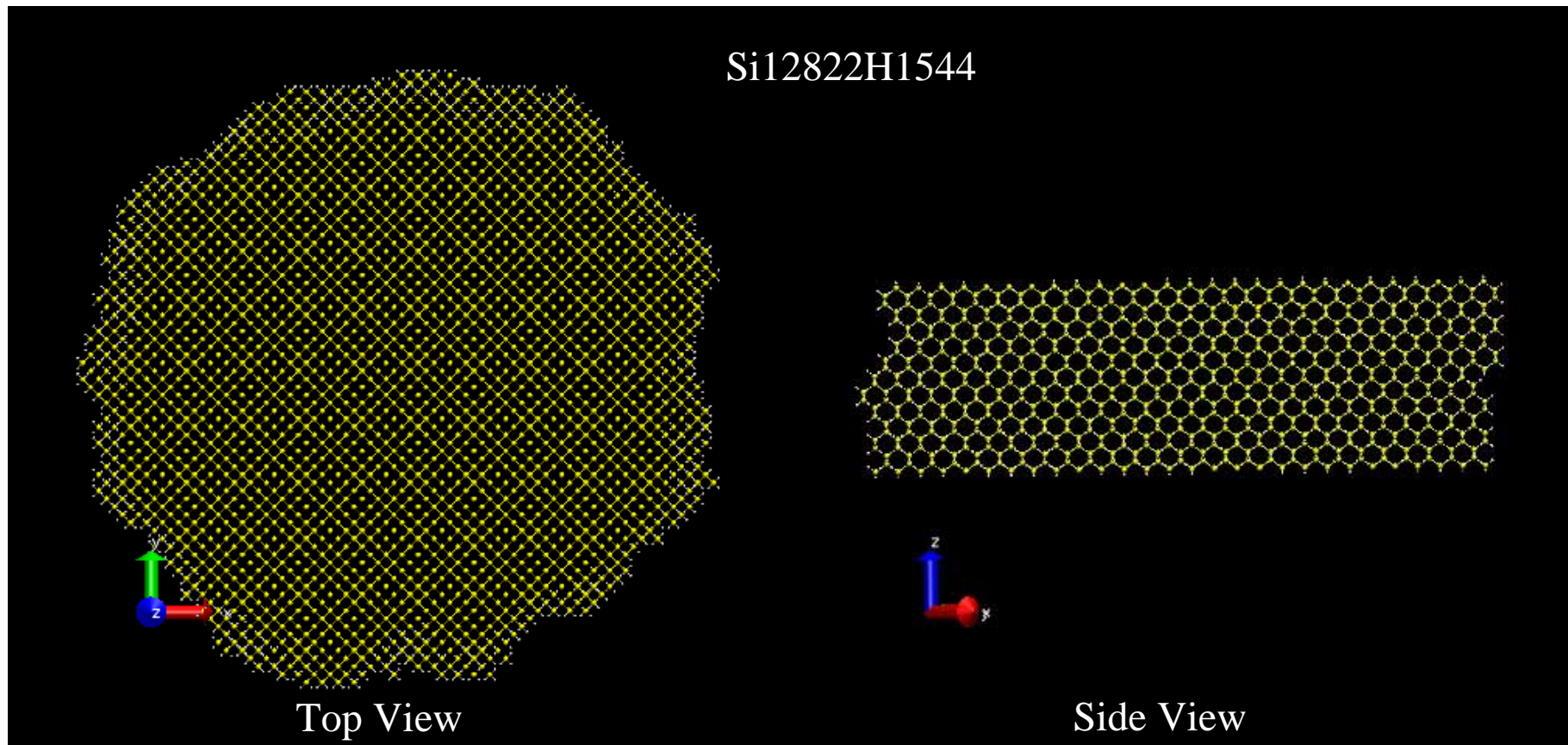


Effective mass equation

$$\left[-\frac{\hbar^2}{2m_t^*} \left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} \right) - \frac{\hbar^2}{2m_l^*} \frac{\partial^2}{\partial z^2} \right] \Phi(\mathbf{r}) = (\varepsilon - \varepsilon_{CBM}) \Phi(\mathbf{r})$$

The band structure can be understood that electrons near the CBM in the bulk Si are Confined within a cylindrical geometry.

Si nano wire with surface roughness

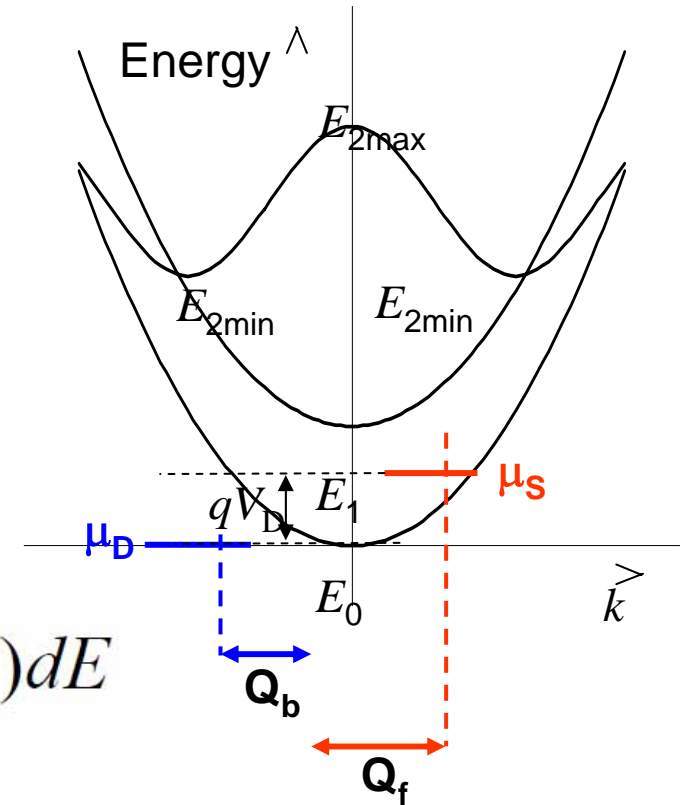
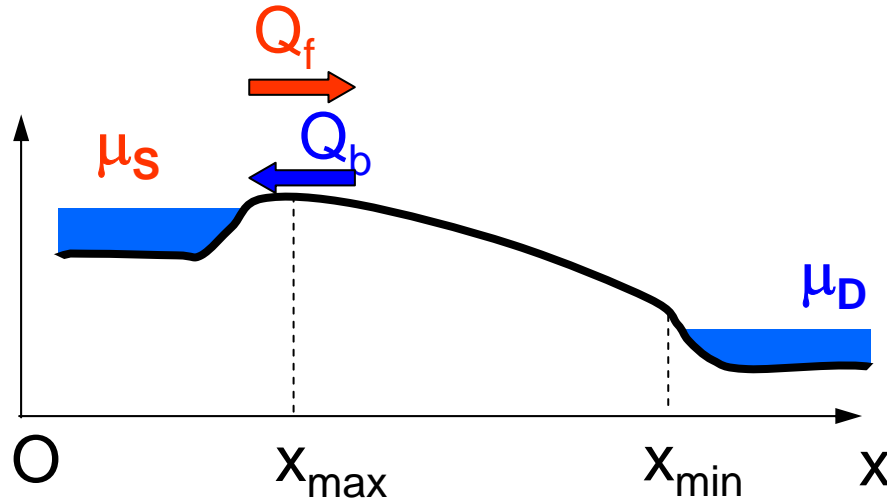


Si12822H1544 (14,366 atoms)

- 10nm diameter, 3.3nm height, (100)
- Grid spacing: 0.45\AA ($\sim 14\text{Ry}$)
- # of grid points: 4,718,592
- # of bands: 29,024
- Memory: 1,022GB \sim 2,044GB

SiNW Band compact model

Landauer Formalism for Ballistic FET

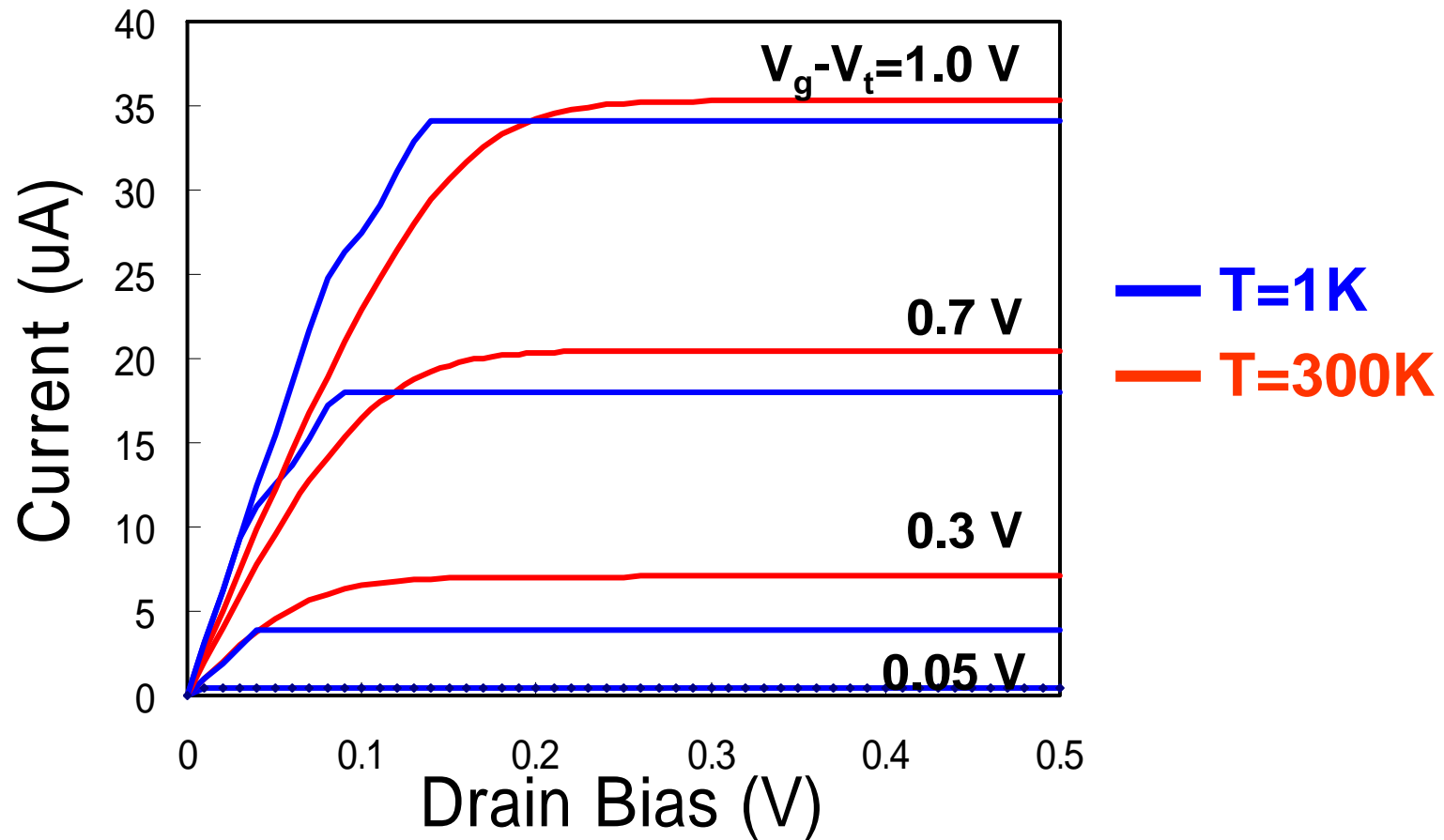


$$I_D = \frac{q}{\pi\hbar} \sum_i \int [f(E, \mu_S) - f(E, \mu_D)] T_i(E) dE$$

From x_{\max} to x_{\min} $T_i(E) \approx 1$

$$I_D = G_0 \left(\frac{k_B T}{q} \right) \sum_i g_i \ln \left\{ \frac{1 + \exp[(\mu_S - E_{i0}) / k_B T]}{1 + \exp[(\mu_D - E_{i0}) / k_B T]} \right\}$$

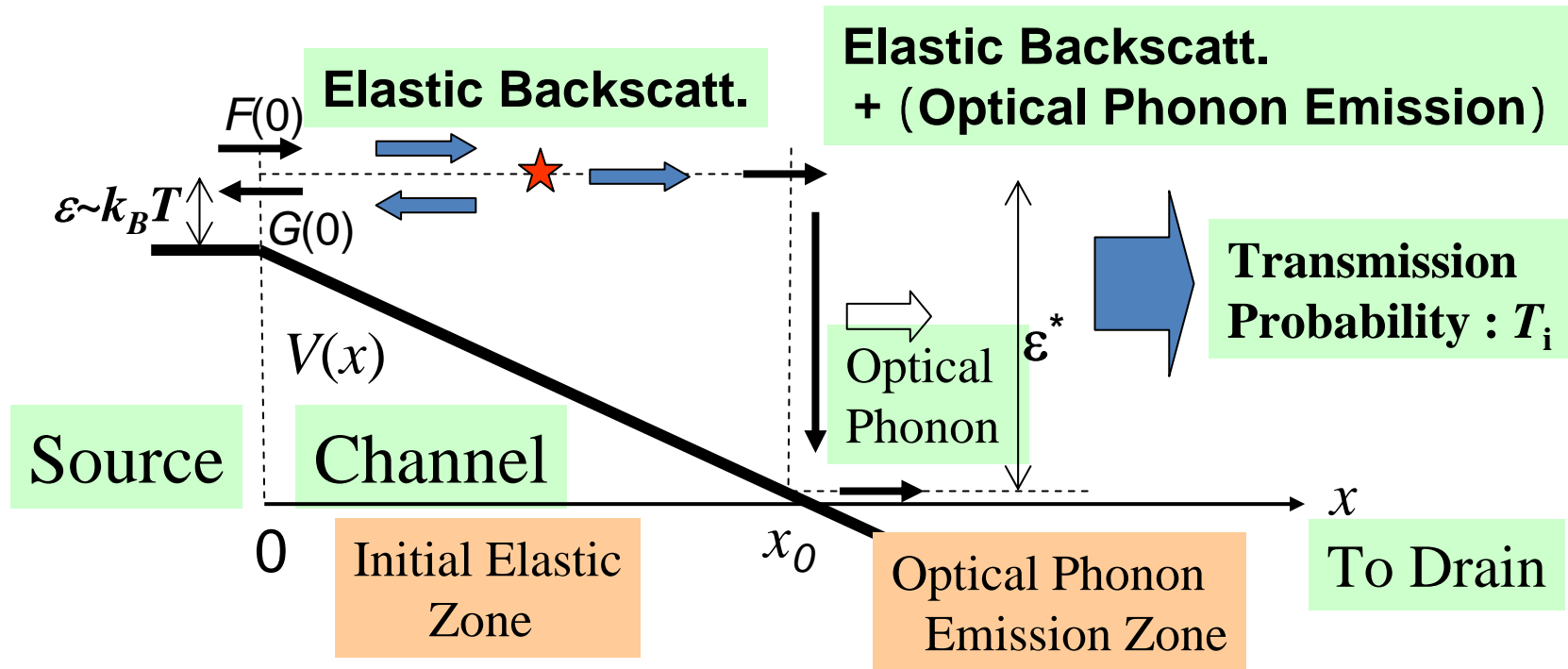
IV Characteristics of Ballistic SiNW FET



Small temperature dependency
 $35\mu A/wire$ for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx. : Electric Field E



Transmission
Probability
to Drain

$$T(\epsilon) = \frac{F(0) - G(0)}{F(0)} \quad \text{Injection from Drain}=0$$

Résumé of the Compact Model

$$I = \frac{q}{\pi \hbar} \sum_i g_i \int [f(\varepsilon, \mu_S) - f(\varepsilon, \mu_D)] T_i d\varepsilon$$

$$C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left\{ \frac{\sqrt{2r+t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r+t_{ox}} - \sqrt{t_{ox}}} \right\}}$$

Planar Gate

$$(V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{|Q_f + Q_b|}{C_G}$$

$$\mu_S - \mu_D = qV_D$$

$$C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left(\frac{r+t_{ox}}{r} \right)}$$

GAA

(Electrostatics requirement)

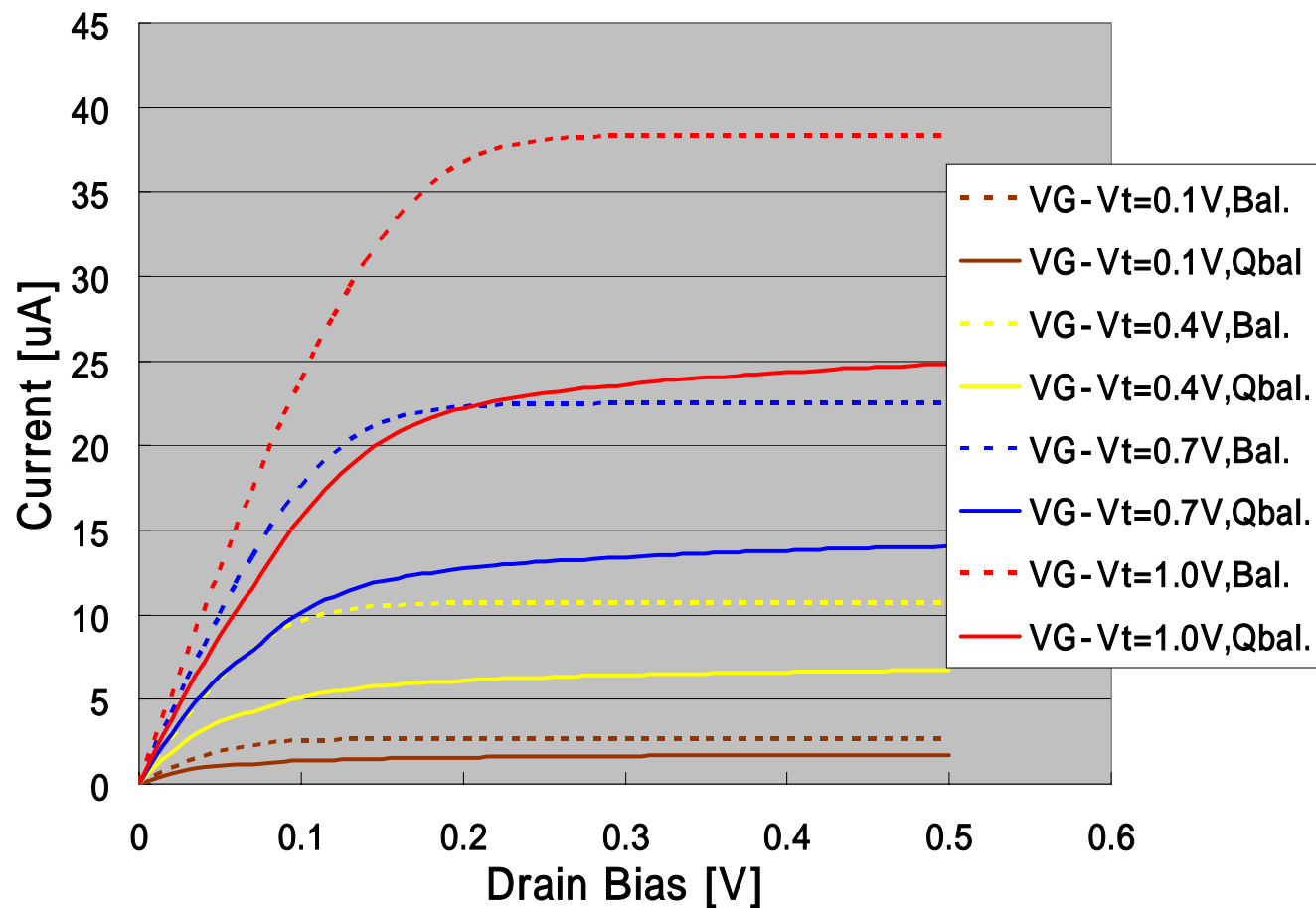
$$|Q_f + Q_b| = \frac{q}{\pi} \sum_i g_i \left[\int_{-\infty}^{\infty} \frac{dk}{1 + \exp \left\{ \frac{\varepsilon_i(k) - \mu_S}{k_B T} \right\}} - \int_{-\infty}^0 \left\{ \frac{1}{1 + \exp \left\{ \frac{\varepsilon_i(k) - \mu_S}{k_B T} \right\}} - \frac{1}{1 + \exp \left\{ \frac{\varepsilon_i(k) - \mu_D}{k_B T} \right\}} \right\} T_i(\varepsilon_i(k)) dk \right]$$

$$T(\varepsilon) = \frac{\sqrt{2D_0} qE}{\left(\sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0} B_0 \ln \left(\frac{qEx_0 + \varepsilon}{\varepsilon} \right)}$$

(Carrier distribution in Subbands)

Unknowns are $I_D, (\mu_S - \mu_0), (\mu_D - \mu_0), (Q_f + Q_b)$

I- V_D Characteristics (RT)

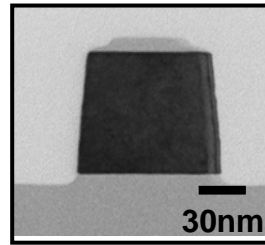


- Electric current 20 ~ 25 μ A
- No saturation at Large V_D

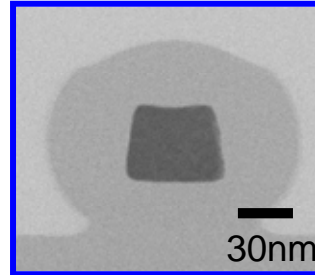
SiNW FET Fabrication

SiNW FET Fabrication

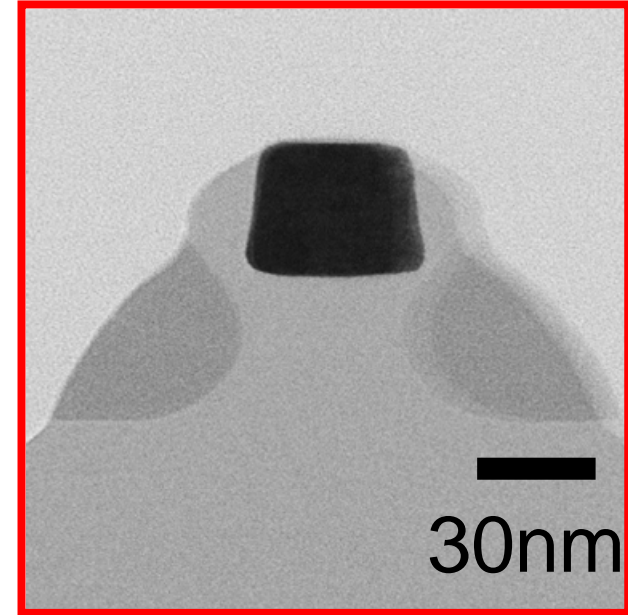
○ S/D & Fin Patterning



○ Sacrificial Oxidation



○ Oxide etch back



○ SiN sidewall support formation

○ Gate Oxidation & Poly-Si Deposition

○ Gate Lithography & RIE Etching

○ Gate Sidewall Formation

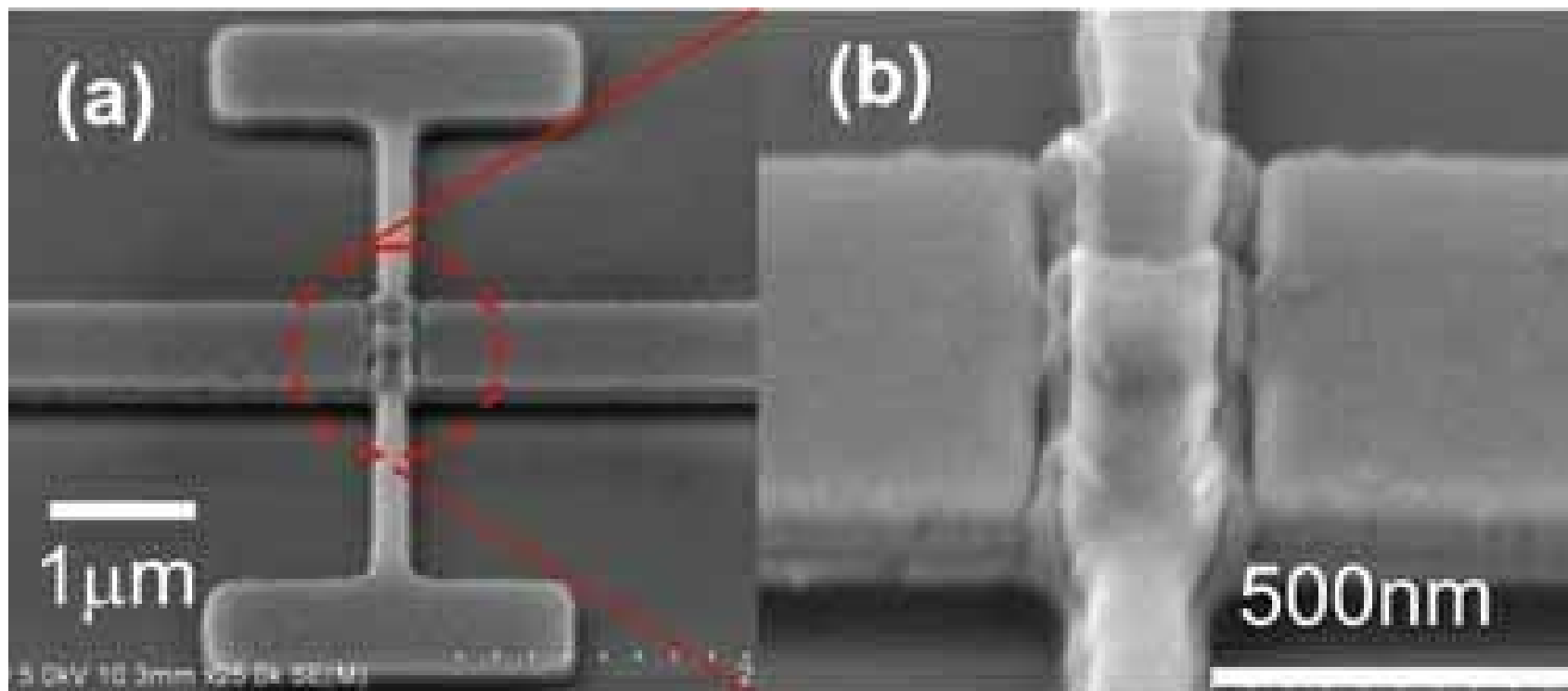
○ Ni SALISIDE Process (Ni 9nm / TiN 10nm)

○ Backend

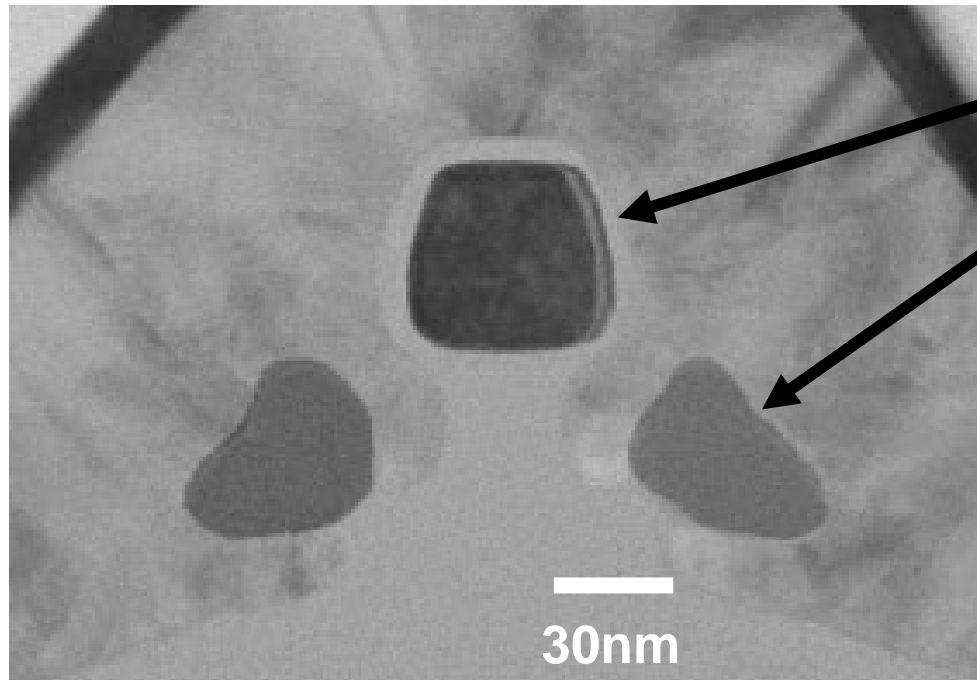
Standard recipe for gate stack formation

(a) SEM image of Si NW FET ($L_g = 200\text{nm}$)

(b) high magnification observation of gate and its sidewall.

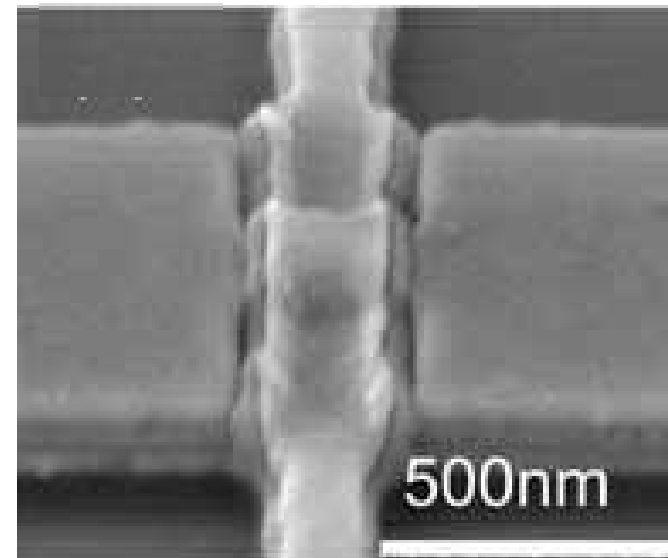
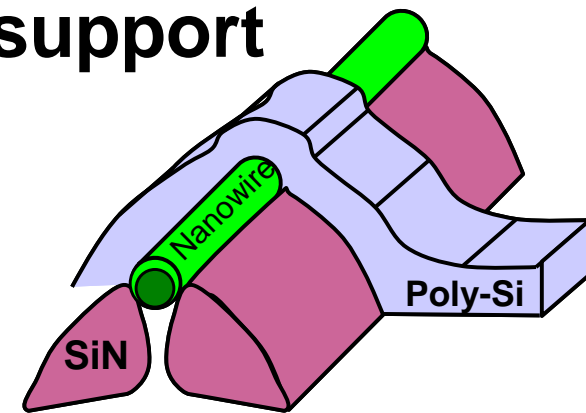


Fabricated SiNW FET



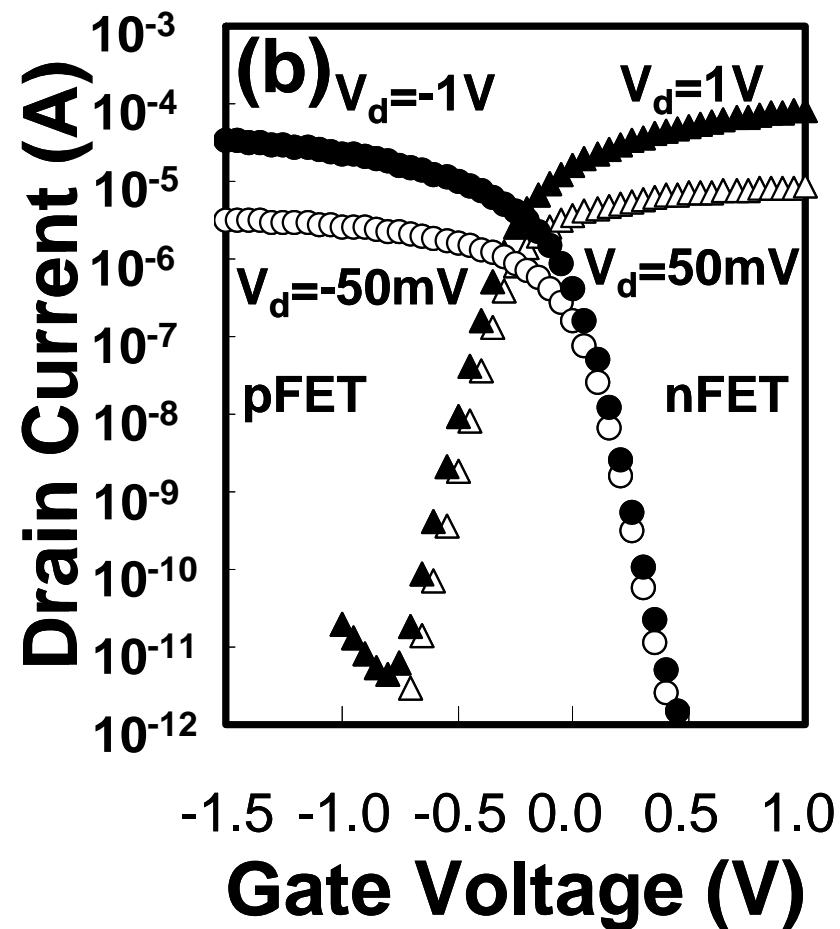
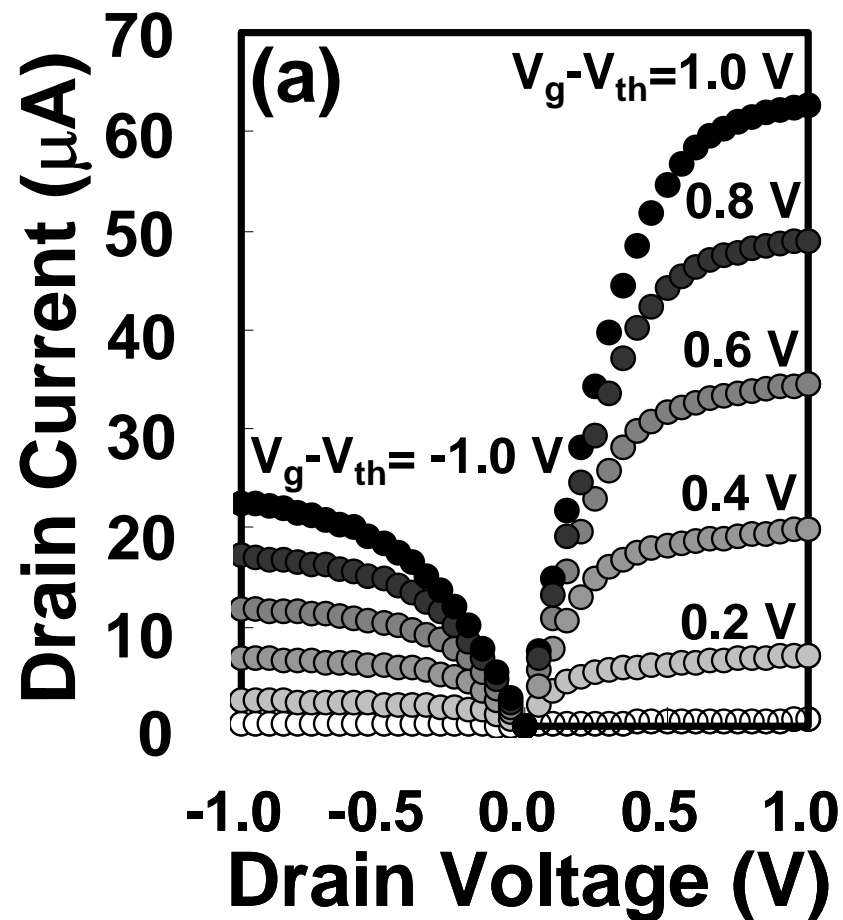
SiNW

SiN support



Recent results to be presented by ESSDERC 2010 next week in Seville

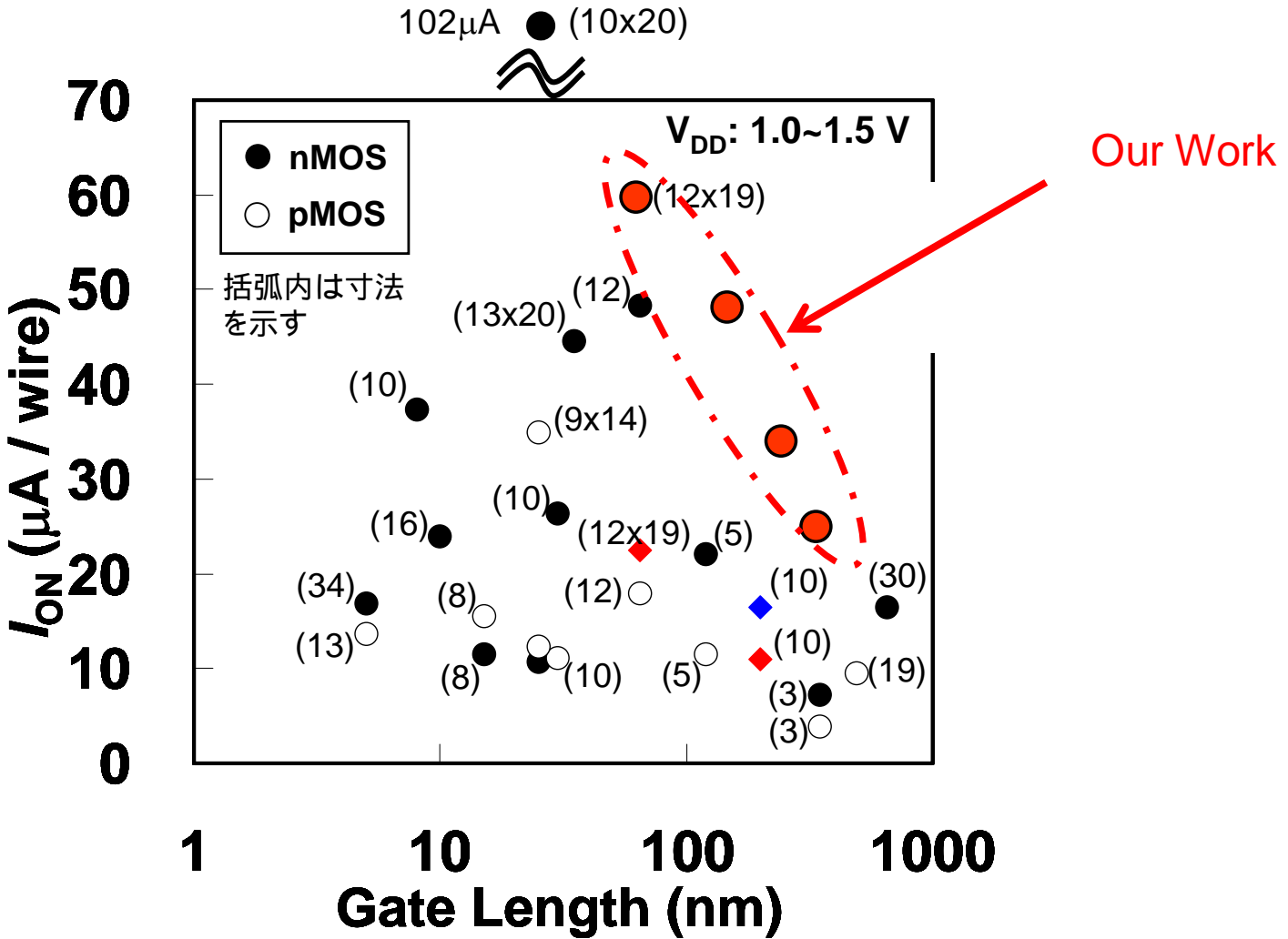
Wire cross-section: 20 nm X 10 nm



On/Off $> 10^6$, 60 μA /wire

$L_g = 65\text{ nm}$, $T_{ox} = 3\text{ nm}$

Bench Mark



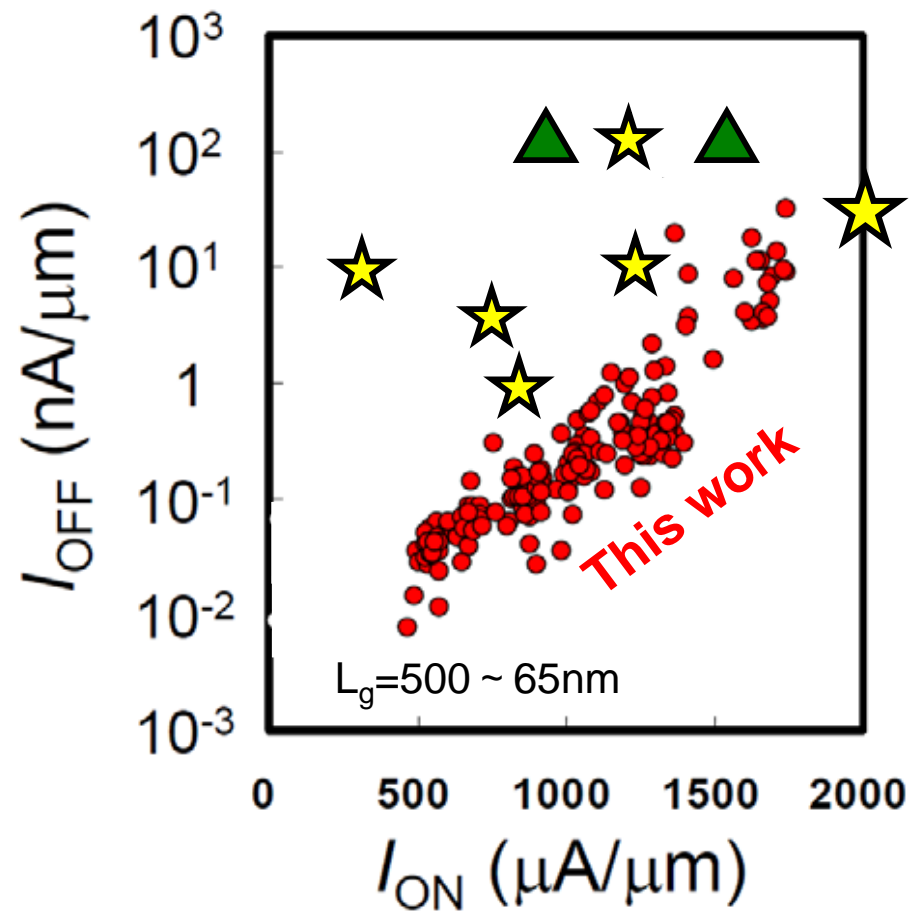
Bench Mark

	This work	Ref[11]	Ref[12]	Ref[13]	Ref[14]	Ref[15]	Ref[4]
NW Cross-section (nm)	Rect.	Rect.	Rect.	Cir.	Cir.	Elliptical	Elliptical
NW Size (nm)	10x20	10x20	14	10	10	12	13x20
Lg (nm)	65	25	100	30	8	65	35
EOT or Tox (nm)	3	1.8	1.8	2	4	3	1.5
Vdd (V)	1.0	1.1	1.2	1.0	1.2	1.2	1.0
Ion(uA) per wire	60.1	102	30.3	26.4	37.4	48.4	43.8
Ion(uA/um) by dia.	3117	5010	2170	2640	3740	4030	2592
Ion(uA/um) by cir.	1609	2054	430	841	1191	1283	825
SS (mV/dec.)	70	79	68	71	75	~75	85
DIBL (mV/V)	62	56	15	13	22	40-82	65
Ion/Ioff	~1E6	>1E6	>1E5	~1E6	>1E7	>1E7	~2E5

Ref[11] by Stmicro Lg=25nm, Tox=1.8nm

This work Lg=65nm, Tox=3nm

I_{ON}/I_{OFF} Bench mark



Planer FET



1.0 ~ 1.1V

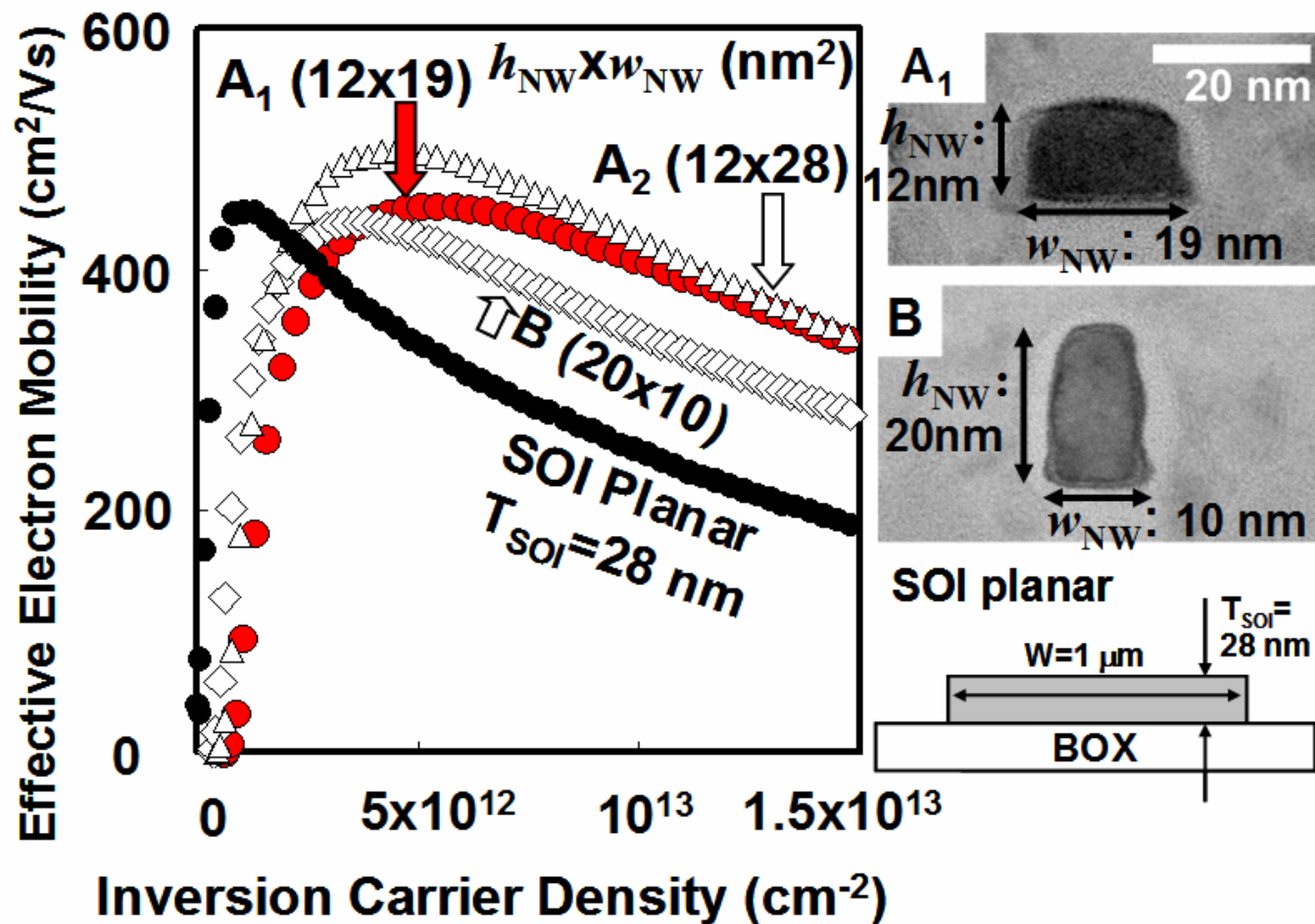
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

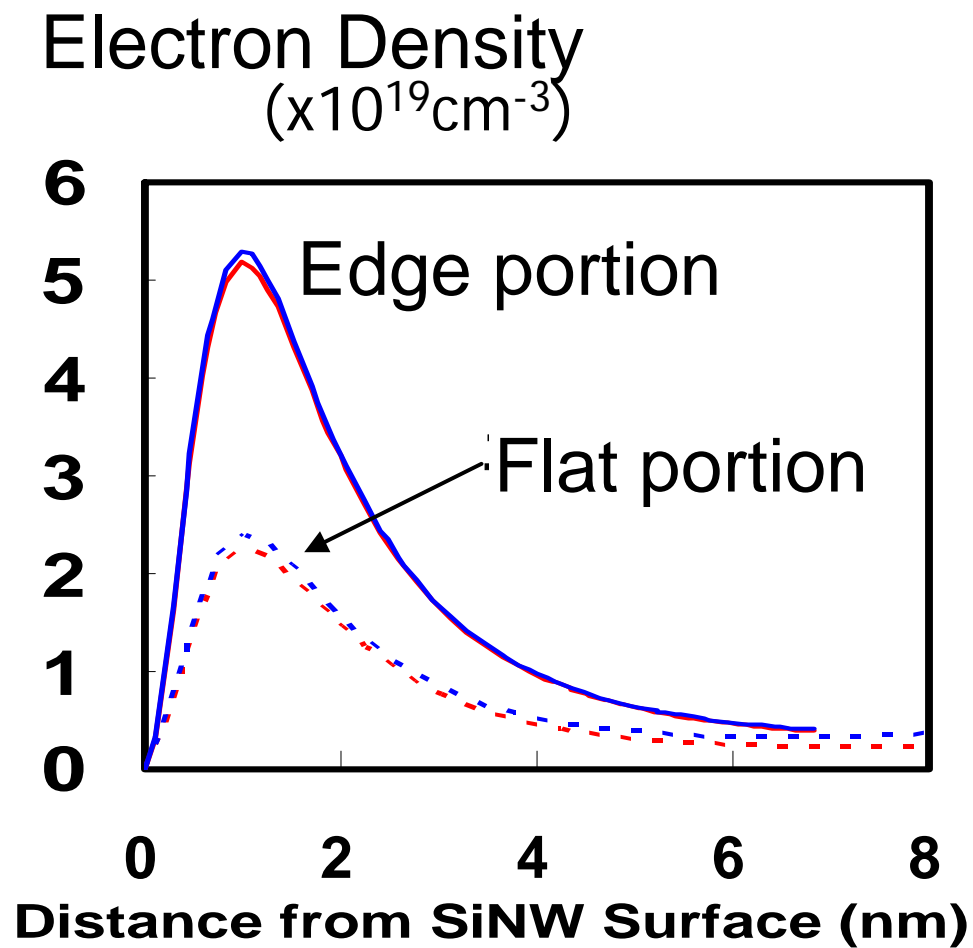
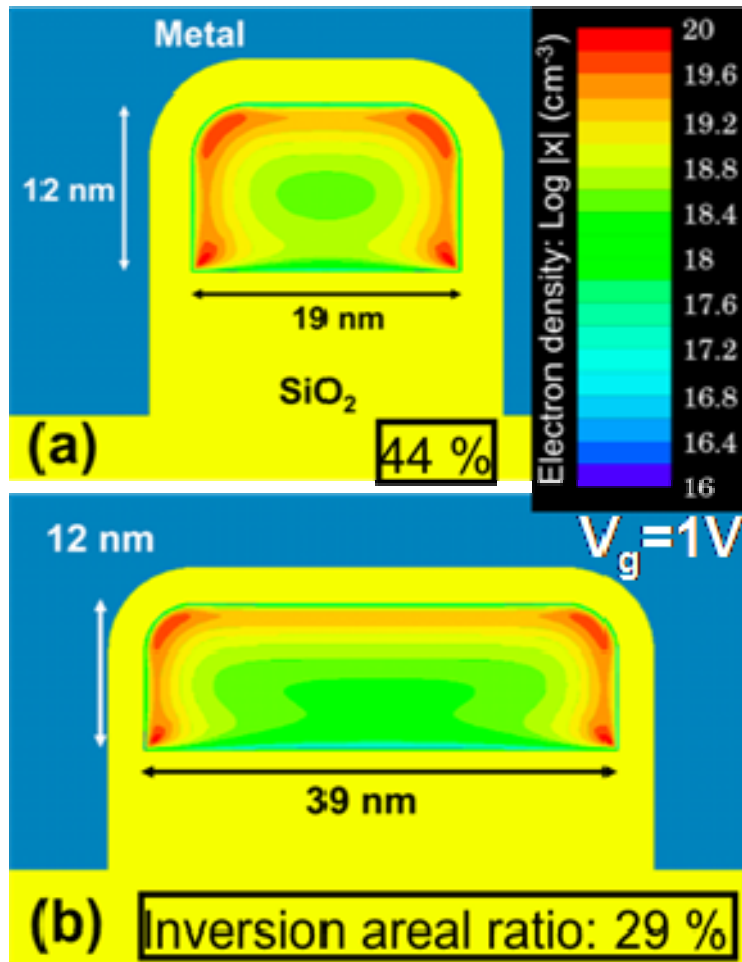
SiナノワイヤFET



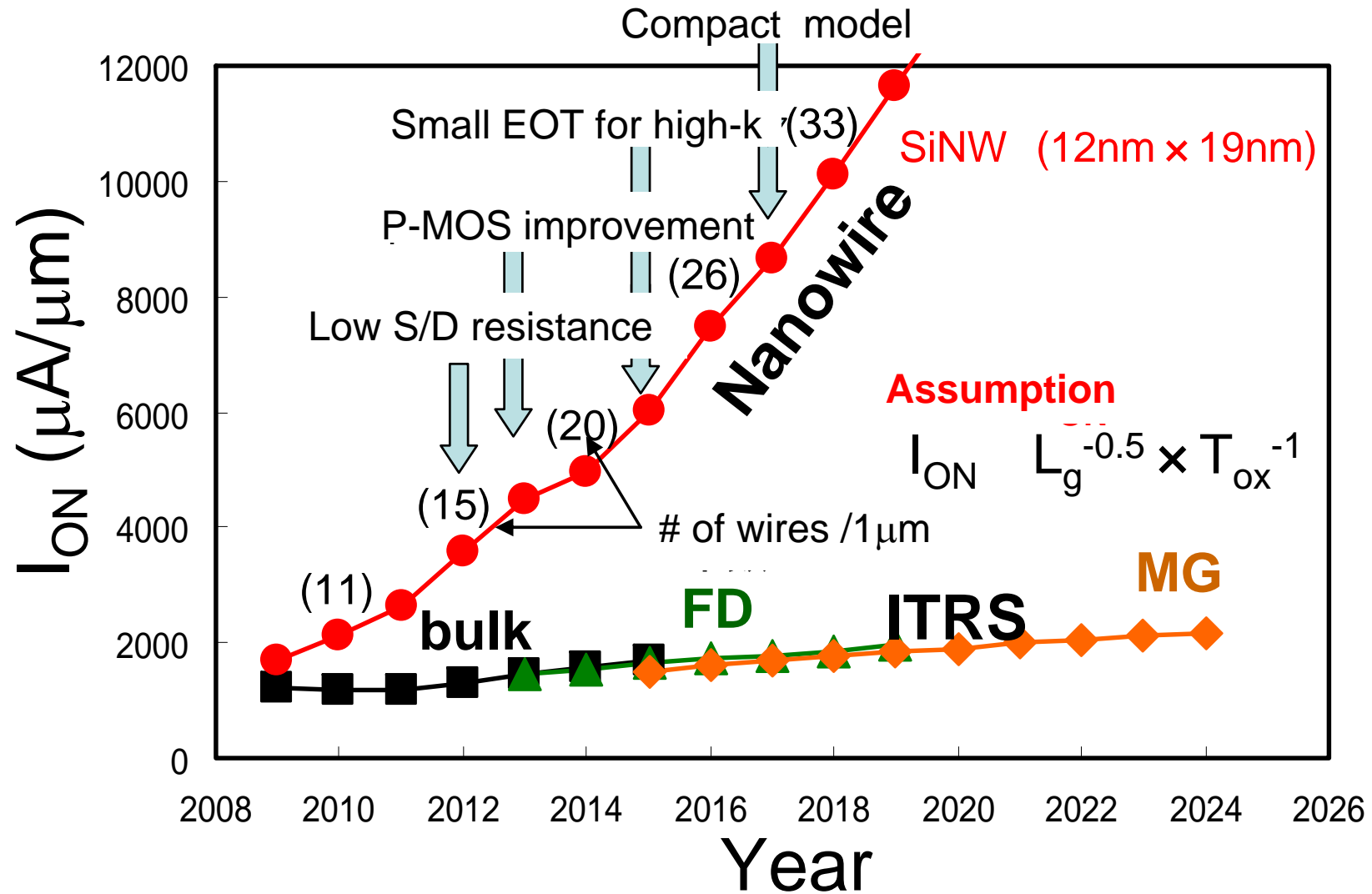
1.2 ~ 1.3V

Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240





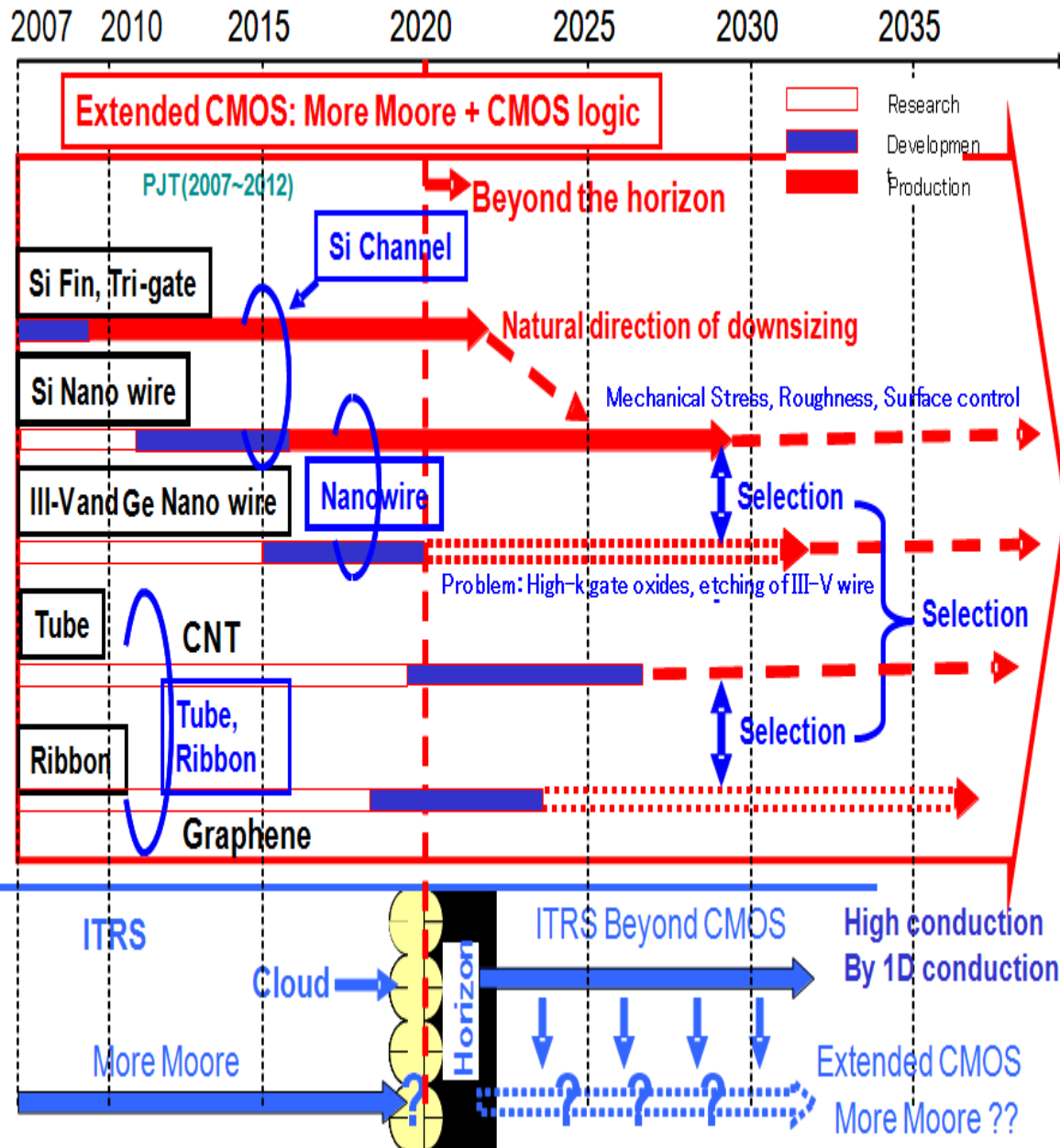
Primitive estimation !



Our roadmap for R & D

Source: H. Iwai, IWJT 2008

Current Issues



Si Nanowire

- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire

- High-k gate insulator
- Wire formation technique

CNT:

- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:

- Graphene formation technique
- Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

- Control of ribbon edge structure which affects bandgap

Thank you for your attention