Past and Future Trends of Integrated Circuit Technology

@Prithvi Narayan Campus, Trivhuvan Univ., Pokhara, Nepal

October 25, 2010

Tokyo Institute of Technology
Frontier Research Center

Hiroshi Iwai,
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
Institute Overview

Established in 1881 → 130th anniversary in 2011

3 undergraduate schools
  School of Science, School of Engineering, School of Bioscience and Biotechnology

7 graduate schools
  Science and Engineering Science, Science and Engineering Technology,
  Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
  Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

<table>
<thead>
<tr>
<th></th>
<th>Undergraduate</th>
<th>Graduate</th>
<th>Master's</th>
<th>Doctoral</th>
<th>Teaching Staff</th>
<th>Student/Instructor</th>
<th>Staff</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tokyo Inst.</td>
<td>5,000</td>
<td>5,000</td>
<td>3,500</td>
<td>1,500</td>
<td>1,200</td>
<td>8.3</td>
<td>550</td>
</tr>
<tr>
<td>Per Year</td>
<td>1,200</td>
<td>1,800</td>
<td></td>
<td>500</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Asia 847
Europe 78
Africa 16
North America 12
South America 24
Oceania 5

Total 982
(As of May. 1, 2005)
Importance of Electronics

• There were many inventions in the 20th century: Airplane, Nuclear Power generation, Computer, Space aircraft, etc

• However, everything has to be controlled by electronics

• Electronics
  
  Most important invention in the 20th century

• What is Electronics: To use electrons, Electronic Circuits
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Cathode (heated)  Grid  Anode (Positive bias)

Same mechanism as that of transistor
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

File March 28, 1928

UNITED STATES PATENT OFFICE

Patented Mar. 7, 1933

1,900,018

J. E. LILIENFELD

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928
Capacitor structure with notch

Negative bias

- - - -

No current

Positive bias

- - - -

Current flows

- - - -

Electric field

Gate Electrode

Gate Insulator

Semiconductor

Electron
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator.

Drain Current was several orders of magnitude smaller than expected.

Even Shockley!
However, they found amplification phenomenon when investigating Ge surface when putting needles. This is the 1st Transistor: Not Field Effect Transistor, But Bipolar Transistor (another mechanism)

1947: 1st transistor

J. Bardeen  W. Bratten, W. Shockley

Bipolar using Ge
1958: 1st Integrated Circuit

Connect 2 bipolar transistors in the Same substrate by bonding wire.
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si

Source

Al Gate

Drain

Si

SiO₂

Al

Si

Si/SiO₂ Interface is extraordinarily good
1970, 71: 1st generation of LSIs

DRAM    Intel 1103

MPU    Intel 4004
MOS LSI experienced continuous progress for many years

<table>
<thead>
<tr>
<th>Name of Integrated Circuits</th>
<th>Number of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>1960s IC (Integrated Circuits)</td>
<td>~10</td>
</tr>
<tr>
<td>1970s LSI (Large Scale Integrated Circuit)</td>
<td>~1,000</td>
</tr>
<tr>
<td>1980s VLSI (Very Large Scale IC)</td>
<td>~10,000</td>
</tr>
<tr>
<td>1990s ULSI (Ultra Large Scale IC)</td>
<td>~1,000,000</td>
</tr>
<tr>
<td>2000s ?LSI (? Large Scale IC)</td>
<td>~1,000,000,000</td>
</tr>
</tbody>
</table>
MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Use Gate Field Effect for switching

N-MOS (N-type MOSFET)

Gate Electrode
Poly Si

Gate Insulator
SiO₂

Substrate Si

Source

Channel

Drain

Si Substrate
Complimentary MOS

When NMOS is ON, PMOS is OFF
When PMOS is ON, NMOS is OFF
CMOS Technology: Indispensable for our human society

All the human activities are controlled by CMOS:
  living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:
  There is no computer in banks, and world economical activities immediately stop.

Cellarer phone dose not exists

Needless to say, but....
Downsizing of the components has been the driving force for circuit evolution.

<table>
<thead>
<tr>
<th>Year</th>
<th>Device Type</th>
<th>Size (cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1900</td>
<td>Vacuum Tube</td>
<td>10</td>
</tr>
<tr>
<td>1950</td>
<td>Transistor</td>
<td>cm</td>
</tr>
<tr>
<td>1960</td>
<td>IC</td>
<td>mm</td>
</tr>
<tr>
<td>1970</td>
<td>LSI</td>
<td>10 µm</td>
</tr>
<tr>
<td>2000</td>
<td>ULSI</td>
<td>100 nm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10^{-1}m</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10^{-2}m</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10^{-3}m</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10^{-5}m</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10^{-7}m</td>
</tr>
</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. **Reduce Capacitance**
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. **Increase number of Transistors**
   - Parallel processing
     - Increase circuit operation speed

Thus, downsizing of Si devices is the most important and critical issue.
Scaling Method: by R. Dennard in 1974

\( W_{\text{dep}} \): Space Charge Region (or Depletion Region) Width

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

\[
X, Y, Z : K, \quad V : K, \quad Na : 1/K
\]

By the scaling, \( W_{\text{dep}} \) is suppressed in proportion, and thus, leakage can be suppressed.

\[
W_{\text{dep}} \propto \sqrt{V/Na} : K
\]

\( I : K \)

Leakage current

Wdep has to be suppressed. Otherwise, large leakage between S and D.

\( K = 0.7 \) for example
### Downscaling merit: Beautiful!

<table>
<thead>
<tr>
<th>Geometry &amp; Supply voltage</th>
<th>Geometric parameters: $L_g$, $W_g$, $T_{ox}$, $V_{dd}$</th>
<th>Scaling $K$: $K=0.7$ for example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive current in saturation</td>
<td>$I_d$</td>
<td>$K$</td>
</tr>
<tr>
<td>$I_d$ per unit $W_g$</td>
<td>$I_d/\mu$m</td>
<td>1</td>
</tr>
<tr>
<td>Gate capacitance</td>
<td>$C_g$</td>
<td>$K$</td>
</tr>
<tr>
<td>Switching speed</td>
<td>$\tau$</td>
<td>$K$</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>$f$</td>
<td>$1/K$</td>
</tr>
<tr>
<td>Chip area</td>
<td>$A_{chip}$</td>
<td>$\alpha$</td>
</tr>
<tr>
<td>Integration (# of Tr)</td>
<td>$N$</td>
<td>$\alpha/K^2$</td>
</tr>
<tr>
<td>Power per chip</td>
<td>$P$</td>
<td>$\alpha$</td>
</tr>
<tr>
<td></td>
<td>k= 0.7 and $\alpha$ =1</td>
<td>k= 0.7$^2$ =0.5 and $\alpha$ =1</td>
</tr>
<tr>
<td>--------------------------</td>
<td>----------------------------------------------------------</td>
<td>----------------------------------------------------------</td>
</tr>
<tr>
<td><strong>Single MOFET</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vdd $\rightarrow$ 0.7</td>
<td></td>
<td>Vdd $\rightarrow$ 0.5</td>
</tr>
<tr>
<td>Lg $\rightarrow$ 0.7</td>
<td></td>
<td>Lg $\rightarrow$ 0.5</td>
</tr>
<tr>
<td>Id $\rightarrow$ 0.7</td>
<td></td>
<td>Id $\rightarrow$ 0.5</td>
</tr>
<tr>
<td>Cg $\rightarrow$ 0.7</td>
<td></td>
<td>Cg $\rightarrow$ 0.5</td>
</tr>
<tr>
<td>$P$ (Power)/Clock $\rightarrow$ $0.7^3 = 0.34$</td>
<td>$P$ (Power)/Clock $\rightarrow$ $0.5^3 = 0.125$</td>
<td></td>
</tr>
<tr>
<td>$\tau$ (Switching time) $\rightarrow$ 0.7</td>
<td>$\tau$ (Switching time) $\rightarrow$ 0.5</td>
<td></td>
</tr>
<tr>
<td><strong>Chip</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N (# of Tr) $\rightarrow$ $1/0.7^2 = 2$</td>
<td>N (# of Tr) $\rightarrow$ $1/0.5^2 = 4$</td>
<td></td>
</tr>
<tr>
<td>f (Clock) $\rightarrow$ $1/0.7 = 1.4$</td>
<td>f (Clock) $\rightarrow$ $1/0.5 = 2$</td>
<td></td>
</tr>
<tr>
<td>P (Power) $\rightarrow$ 1</td>
<td>P (Power) $\rightarrow$ 1</td>
<td></td>
</tr>
</tbody>
</table>
Actual past downscaling trend until year 2000

Change in 30 years

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ideal scaling</th>
<th>Real Change</th>
<th>Ideal scaling</th>
<th>Real Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$</td>
<td>$K$</td>
<td>$10^{-2}$</td>
<td>$I_d$</td>
<td>$K(10^{-2})$</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-2}$</td>
<td>$I_d/\mu m$</td>
<td>$1$</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-1}$</td>
<td>$N$</td>
<td>$\alpha/K^2(10^5)$</td>
</tr>
<tr>
<td>$A_{chip}$</td>
<td>$\alpha$</td>
<td>$10^1$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$V_{dd}$ scaling insufficient, $\alpha$ increased

$\Rightarrow$ $N, I_d, f, P$ increased significantly
Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1µm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5µm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25µm:</td>
<td>Direct-tunneling of gate SiO₂</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1µm:</td>
<td>‘0.1µm brick wall’(various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
Historically, many predictions of the limit of downsizing. VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.
Finally, there appears to be a fundamental limit of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.
Direct-tunneling effect

Gate Electrode  Gate Oxide  Potential Barrier  Si Substrate

Wave function  Direct tunneling current

Direct tunneling leakage current start to flow when the thickness is 3 nm.
Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide

- Lg = 10 μm
- Lg = 5 μm
- Lg = 1.0 μm
- Lg = 0.1 μm
Gate leakage: $I_g \propto \text{Gate Area} \propto \text{Gate length (Lg)}$

Drain current: $I_d \propto 1/\text{Gate length (Lg)}$

$Lg \to \text{small},$

Then, $I_g \to \text{small}, I_d \to \text{large},$ Thus, $I_g/I_d \to \text{very small}$

$Lg = 10 \, \mu m$  $Lg = 5 \, \mu m$  $Lg = 1.0 \, \mu m$  $Lg = 0.1 \mu m$
Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!

Some one will think for you
Transistor Scaling Continues

Qi Xinag, ECS 2004, AMD
5 nm gate length CMOS is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC

IEDM, 2003
What is the limit prediction now!

Tunneling distance
3 nm

Atomic distance
0.3 nm

Limit for MOSFET operation
Below this, no one knows future!
However, Gate oxide thickness 2 orders magnitude smaller Close to limitation!!

Lg: Gate length downsizing will continue to another 10-15 years
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
So, we are now in the limitation of downsizing?

Do you believe this or do not?
There is a solution! To use high-k dielectrics

K: Dielectric Constant

Thin gate SiO₂

Almost the same electric characteristics

Thick gate high-k dielectrics

Thick
Small leakage Current

However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO₂!
Historical trend of high-k R&D

<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET Gate Stack in production</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1st FET IC LSI</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>PMOS NMOS CMOS</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Gate insulator: SiO₂, SiOₓNᵧ

Gate electrode: Al, N⁺Poly Si

Silicide above Poly Si electrode: MoSi₂ → WSi₂, TiSi₂, CoSi₂, NiSi

R&D for high-k

MOSFET Ni₃Si₄ Stack NO(Ni₃Si₄/SiO₂)

Pure Si Period

Recent new high-k

DRAM Capacitor (O)NO, Ni₃Si₄ Ta₂O₅, Al₂O₃

NV Memory NO, AO (Al₂O₃/SiO₂)

Analog/RF Ta₂O₅
## Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>Unstable at Si interface</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
<th>He</th>
<th>B</th>
<th>C</th>
<th>N</th>
<th>O</th>
<th>F</th>
<th>Ne</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Si + MOX M + SiO&lt;sub&gt;2&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Li Be</td>
<td>Si + MOX MSi&lt;sub&gt;x&lt;/sub&gt; + SiO&lt;sub&gt;2&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mg Na</td>
<td>Si + MOX M + MSi&lt;sub&gt;x&lt;/sub&gt;O&lt;sub&gt;y&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Si + MOX M + SiO<sub>2</sub>
- Si + MOX MSi<sub>x</sub> + SiO<sub>2</sub>
- Si + MOX M + MSi<sub>x</sub>O<sub>y</sub>

### Candidates

- La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Y, Lu
- Ac, Th, Pa, U, Np, Pu, Am, Cm, Bk, Cf, Es, Fm, Md, No, Lr

### Notes
- HfO<sub>2</sub> based dielectrics are selected as the first generation materials, because of their merit in
  1) band-offset,
  2) dielectric constant
  3) thermal stability
- La<sub>2</sub>O<sub>3</sub> based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

---

R. Hauser, IEDM Short Course, 1999
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness
**Band Offsets**

- $E_g > 1$ V
- $E_h > 1$ V
- $E_s < 1$ V

**Calculated value**

<table>
<thead>
<tr>
<th>Material</th>
<th>Calculated Value (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>3.5</td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
<td>2.4</td>
</tr>
<tr>
<td>Ta$_2$O$_5$</td>
<td>0.3</td>
</tr>
<tr>
<td>SrTiO$_3$</td>
<td>-0.1</td>
</tr>
<tr>
<td>ZrO$_2$</td>
<td>0.8</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>1.4</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>1.5</td>
</tr>
<tr>
<td>Y$_2$O$_3$</td>
<td>2.8</td>
</tr>
<tr>
<td>La$_2$O$_3$</td>
<td>2.3</td>
</tr>
<tr>
<td>HfSiO$_4$</td>
<td>1.5</td>
</tr>
<tr>
<td>LaAlO$_3$</td>
<td>2.1</td>
</tr>
</tbody>
</table>

**Dielectric constant**

- SiO$_2$: 4
- Si$_3$N$_4$: ~7
- Al$_2$O$_3$: ~9
- Y$_2$O$_3$: ~10
- Gd$_2$O$_3$: ~10
- HfO$_2$: ~23
- La$_2$O$_3$: ~27

HfO$_2$ was chosen for the 1st generation.
La$_2$O$_3$ is more difficult material to treat.
Dielectric constant value vs. Band offset (Measured)

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric Constant</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>3.9</td>
<td></td>
</tr>
<tr>
<td>Al$_x$Si$_y$O$_z$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Ba,Sr)TiO$_3$</td>
<td>200-300</td>
<td>T. Hattori, INFOS, 2003</td>
</tr>
<tr>
<td>BeAl$_2$O$_4$</td>
<td>8.3-9.43</td>
<td></td>
</tr>
<tr>
<td>CeO$_2$</td>
<td>16.6-26</td>
<td></td>
</tr>
<tr>
<td>CeHfO$_4$</td>
<td>10-20</td>
<td></td>
</tr>
<tr>
<td>CoTiO$_3$/Si$_3$N$_4$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EuAlO$_3$</td>
<td>22.5</td>
<td>C.A. Billmann et al., MRS Spring Symp., 1999</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>26-30</td>
<td></td>
</tr>
<tr>
<td>Hf silicate</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>La$_2$O$_3$</td>
<td>20.8</td>
<td></td>
</tr>
<tr>
<td>LaScO$_3$</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>La$_2$SiO$_5$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MgAl$_2$O$_4$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NdAlO$_3$</td>
<td>22.5</td>
<td></td>
</tr>
<tr>
<td>PrAlO$_3$</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>SmAlO$_3$</td>
<td>19</td>
<td></td>
</tr>
<tr>
<td>SrTiO$_3$</td>
<td>150-250</td>
<td></td>
</tr>
<tr>
<td>Ta$_2$O$_5$</td>
<td>25-24</td>
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</tr>
<tr>
<td>Ta$_2$O$_5$-TiO$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TiO$_2$</td>
<td>86-95</td>
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</tr>
<tr>
<td>TiO$_2$/Si$_3$N$_4$</td>
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</tr>
<tr>
<td>Y$_2$O$_3$</td>
<td>8-11.6</td>
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</tr>
<tr>
<td>Y$_x$Si$_y$O$_z$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ZrO$_2$</td>
<td>22.2-28</td>
<td></td>
</tr>
<tr>
<td>Zr-Al-O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Zr silicate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Zr,Sn)TiO$_4$</td>
<td>40-60</td>
<td></td>
</tr>
</tbody>
</table>

\[ \sqrt{\phi_B} \times k \] : Figure of Merit of High-k

S. De Gebdt, IEDM Short Coyuse, 2004

T. Hattori, INFOS, 2003
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O$^*$ $\rightarrow$ HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

D.J.Lichtenwalner, Tans. ECS 11, 319

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
EOT = 0.48 nm  

Our results

Transistor with La2O3 gate insulator
Direct contact of high-k/Si with La-silicate formation

Foramtion of high-k quality La-silicate using the reaction of $\text{La}_2\text{O}_3$ and Si substrate

Originality

EOT: Equivalent oxide thickness

EOT scaling \( \text{limited by IL} \)

Issues in Dit, reailibility \( \mu_{\text{eff}}, \text{etc.} \)

Nice FET operation \( \text{EOT scaling} \)
High quality La-silicate

La$_2$O$_3$ + Si + nO$_2$  

- La$_2$SiO$_5$  
- La$_{9.33}$Si$_6$O$_{26}$  
- La$_{10}$(SiO$_4$)$_6$O$_3$  
- La$_2$Si$_2$O$_7$, etc.

La-rich silicate

Si-rich silicate

La$_2$O$_3$/Si after 500 °C 30min

Proper oxygen atom supply to form high quality Si-rich La-silicate

K. Kakushima, et al., ESSDERC ’08, Edinburgh
FET operation of EOT=0.37nm

(a) EOT=0.37nm $V_{th}=-0.04V$
(b) EOT=0.43nm $V_{th}=-0.03V$
(c) EOT=0.48nm $V_{th}=-0.02V$

Drain current (mA)

Drain voltage (V)

Insufficient compensation region

W/L=50/2.5μm
PMA 300°C (30min)

Direct contact of high-k/Si using La$_2$O$_3$/silicate

Improvement in both drain current and transconductance

EOT scaling below 0.5nm is still useful

(2) Direct high-k/Si using La-silicate/Si with high $\mu_{\text{eff}}$

EOT=1.26nm
W/\text{La}_2\text{O}_3/\text{La-silicate}/\text{nFET}, 500°C for 30min

High peak $\mu_{\text{eff}}$ of 300cm$^2$/Vs with 500°C annealing

- nice properties of Si-rich La-silicate/Si interface

Fairly nice properties can be achieved even with direct high-k/Si interface (EOT~1.2)

K. Kakushima, et al., ESSDERC '08, Edinburgh
(3) Origin of degradations at EOT<1.3nm

Defects from metal electrode

- Metal atom diffusions to degrade the $\mu_{\text{eff}}$ in EOT<1.3nm

- Low Dit at high-k/Si interface at EOT>1.3nm

- Nice Silicate/Si properties

- Metal atom diffusions to degrade the $\mu_{\text{eff}}$ in EOT<1.3nm

- W/La$_2$O$_3$/silicate nFET
  - Annealed at 500 °C

- $\mu_{\text{eff}}$ at 0.8 MV/cm

- EOT$_{\text{lim}}$ at high-k/Si interface

Gate Metal Induced Defects Compensation

Suppression of aggressive shift in $V_{fb}$
Challenge for thinning High-k

Degradation of mobility

Some solution
(5) $\mu_{\text{eff}}$ recovery with Mg incorporation

Mg incorporation into La-silicate

Suppression of $V_{\text{fb}}$ shift at small EOT

Incorporation of Mg into La-silicate can recover the $\mu_{\text{eff}}$

Cluster tool for high-k thin film deposition
Si Nanowire FET
Introduction of SiNW FETs

- Effective electrostatic control of 1-D channel due to the gate all-around structure.
- Low $I_{off}$ can be achieved.
Toward a Reduction of Power Supply Voltage

SiNW FET

Conventional FET

Higher drivability

Required $I_{ON}$ can be achieved with lower overdrive voltage.

Reduction of $V_{DD}$ and low power consumption

Capacity for reduction of $V_{th}$

Lower $I_{OFF}$
The graph compares the Off Current (Ioff) versus Ion (Ion) for different types of transistors. The x-axis represents Ion (uA/μm) ranging from 0 to 4000, and the y-axis represents Ioff (nA/μm) ranging from 0 to 10000. The graph includes data points for bulk, FinFET, SiNWFET, and GeNWFET transistors. Each type of transistor is represented by different symbols: black circles for bulk, blue squares for FinFET, red diamonds for SiNWFET, and green triangles for GeNWFET. Additionally, there are symbols for ITRS (Planer), ITRS (SOI), and ITRS (DG) with different shapes and colors. The graph also highlights the trend lines for ITRS (Bulk), ITRS (SOI), and ITRS (DG), indicating the expected performance of these technologies. The graph shows a clear separation of data points for different types of transistors, with Si Nanowire transistors (dia~3nm) and diode transistors (dia~10nm) also marked on the graph.
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process

2. Good controllability of $I_{OFF}$

3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires

Leakage current

Gate: OFF

Drain Source cut-off
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

E_g = 1.12 eV
E_C = 2.0 eV
E_V = 1.2 eV
E_e = 0.044 eV
E_T1 = 3.4 eV
E_T2 = 4.2 eV

4 channels can be used
Maximum number of wires per 1 µm

Front gate type MOS  165 wires /µm

Surrounded gate type MOS  33 wires/µm

6nm pitch
By nano-imprint method

Metal gate electrode (10nm)
High-k gate insulator (4nm)
Si Nano wire (Diameter 2nm)

30nm pitch:
EUV lithography

Surrounded gate MOS
Device fabrication

- Si/Si$_{0.8}$Ge$_{0.2}$ superlattice epitaxy on SOI
- Anisotropic etching of these layers
- Isotropic etching of SiGe
- The NW diameter is controllable down to 5 nm by self limited oxidation.

Process Details:
C. Dupre et al., IEDM Tech. Dig., p.749, 2008
3D-stacked Si NWs with Hi-$k$/MG

Wire direction: $\langle 110 \rangle$
- 50 NWs in parallel
- 3 levels vertically-stacked
- Total array of 150 wires
- EOT $\sim 2.6$ nm
SiNW Band structure calculation
Cross section of Si NW

First principal calculation,

D=1.96nm [001]  
D=1.94nm [011]  
D=1.93nm [111]
Si nanowire FET with 1D Transport

Orientation  [001]  [011]  [111]
Diameter (nm)  0.86  0.94  0.89

(a)

Energy (eV)

Wave Number

G Z G Z G Z

Small mass with [011]

Large number of quantum channels with [001]
Atomic models of a Si quantum dot and Si nanowires

6.6 nm diameter SiQD (8651 atoms)

10 nm diameter Si(100)NW (2341 atoms)

20 nm diameter Si(100)NW (8941 atoms)
**RSDFT – suitable for parallel first-principles calculation**

- Real-Space Finite-Difference
- Sparse Matrix
- FFT free (FFT is inevitable in the conventional plane-wave code)
- MPI (Message Passing Interface) library

Kohn-Sham eq. (finite-difference)

\[
\left( -\frac{1}{2} \nabla^2 + v_s[\rho](r) + \hat{v}^{PP}_{\text{loc}}(r) \right) \phi_n(r) = \varepsilon_n \phi_n(r)
\]

Higher-order finite difference

\[
\frac{\partial^2}{\partial x^2} \psi_n(x, y, z) \approx \sum_{m=-6}^6 C_m \psi_n(x + m\Delta x, y, z)
\]

Integration

\[
\int \psi_m(r) \psi_n(r) d\mathbf{r} \approx \sum_{i=1}^{Mesh} \psi_m(r_i) \psi_n(r_i) \Delta x \Delta y \Delta z
\]
Massively Parallel Computing

Iwata et al, J. Comp. Phys., to be published

Real-Space Density-Functional Theory code (RSDFT)

Based on the finite-difference pseudopotential method (J. R. Chelikowsky et al., PRB1994)

Highly tuned for massively parallel computers

Computations are done on a massively-parallel cluster PACS-CS at University of Tsukuba.
(Theoretical Peak Performance = 5.6GFLOPS/node)

e.g.) The system over 10,000 atoms $\text{Si}_{10701}\text{H}_{1996}$
(7.6 nm diameter Si dot)

Convergence behavior for $\text{Si}_{10701}\text{H}_{1996}$

Grid points = 3,402,059
Bands = 22,432

Computational Time (with 1024 nodes of PACS-CS)
6781 sec. $\Leftrightarrow$ 60 iteration step = 113 hour
Band Structure and DOS of Si(100)NWs (D=1nm, 4nm, and 8nm)

D = 1 nm
Si21H20 (41 atoms)
KS band gap = 2.60eV

D = 4 nm
Si341H84 (425 atoms)
KS band gap = 0.81eV

D = 8 nm
Si1361H164 (1525 atoms)
KS band gap = 0.61eV

KS band gap of bulk (LDA) = 0.53eV
Band structure of 8-nm-diameter Si nanowire near the CBM

- KS band gap = 0.608 eV (@Γ)

Each band is 4-dgernate.

Effective mass equation:

\[
\left[-\frac{\hbar^2}{2m^*} \left( \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} \right) - \frac{\hbar^2}{2m^*} \frac{\partial^2}{\partial z^2} \right] \Phi(r) = (\varepsilon - \varepsilon_{CBM}) \Phi(r)
\]

The band structure can be understood that electrons near the CBM in the bulk Si are Confined within a cylindrical geometry.
Si12822H1544 (14,366 atoms)
- 10nm diameter, 3.3nm height, (100)
- Grid spacing $0.45\AA$ (~14Ry)
- # of grid points 4,718,592
- # of bands 29,024
- Memory 1,022GB～2,044GB
SiNW Band compact model
Landauer Formalism for Ballistic FET

\[ I_D = \frac{q}{\pi \hbar} \sum_i \int \left[ f(E, \mu_S) - f(E, \mu_D) \right] T_i(E) dE \]

From \( x_{\text{max}} \) to \( x_{\text{min}} \) \( T_i(E) \approx 1 \)

\[ I_D = G_0 \left( \frac{k_B T}{q} \right) \sum_i g_i \ln \left\{ \frac{1 + \exp\left[ (\mu_S - E_{i0}) / k_B T \right]}{1 + \exp\left[ (\mu_D - E_{i0}) / k_B T \right]} \right\} \]
IV Characteristics of Ballistic SiNW FET

Small temperature dependency
35μA/wire for 4 quantum channels
Model of Carrier Scattering

Linear Potential Approx. : Electric Field $E$

$\varepsilon \sim k_B T$

Source

Channel

Initial Elastic Zone

Elastic Backscatt.

$T_i$

Optical Phonon Emission Zone

To Drain

$T(\varepsilon) = \frac{F(0) - G(0)}{F(0)}$

Injection from Drain = 0
Résumé of the Compact Model

\[ I = \frac{q}{\pi \hbar} \sum_i g_i \int [f(\varepsilon, \mu_s) - f(\varepsilon, \mu_D)] T_i \, d\varepsilon \]

\[ C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left( \frac{\sqrt{2r + t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r + t_{ox}} - \sqrt{t_{ox}}} \right)} \]

\[ (V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{Q_f + Q_b}{C_G} \]

\[ \mu_S - \mu_D = qV_D \]

\[ |Q_f + Q_b| = \frac{q}{\pi} \sum_i g_i \left[ \int_{-\infty}^{\infty} \frac{dk}{1 + \exp \left( \frac{\varepsilon_i(k) - \mu_S}{k_B T} \right)} - \int_{-\infty}^{0} \frac{1}{1 + \exp \left( \frac{\varepsilon_i(k) - \mu_S}{k_B T} \right)} - \frac{1}{1 + \exp \left( \frac{\varepsilon_i(k) - \mu_D}{k_B T} \right)} \right] T_i(\varepsilon_i(k)) \, dk \]

\[ T(\varepsilon) = \frac{\sqrt{2D_0 qE}}{\left( \sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0 B_0} \ln \left( \frac{qE x_0 + \varepsilon}{\varepsilon} \right)} \]

Unknowns are \( I_D, (\mu_S - \mu_0), (\mu_D - \mu_0), (Q_f + Q_b) \)

Planar Gate

GAA

Electrostatics requirement

Carrier distribution in Subbands
I-\(V_D\) Characteristics (RT)

- Electric current: 20–25 \(\mu\)A
- No saturation at large \(V_D\)
SiNW FET Fabrication
SiNW FET Fabrication

S/D & Fin Patterning

Sacrificial Oxidation

Oxide etch back

SiN sidewall support formation

Gate Oxidation & Poly-Si Deposition

Gate Lithography & RIE Etching

Gate Sidewall Formation

Ni SALISIDE Process (Ni 9nm / TiN 10nm)

Backend

Standard recipe for gate stack formation
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.
Fabricated SiNW FET
Recent results to be presented by ESSDERC 2010 next week in Seville

Wire cross-section: 20 nm X 10 nm

On/Off > 10^6, 60uA/wire

L_g = 65nm, T_ox = 3nm
Bench Mark

- **Gate Length (nm)**
- **I_{ON} (µA/wire)**

- **nMOS**
- **pMOS**

- **V_{DD}: 1.0~1.5 V**

- **Our Work**
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<tbody>
<tr>
<td>Rect.</td>
<td>Rect.</td>
<td>Rect.</td>
<td>Cir.</td>
<td>Cir.</td>
<td>Elliptical</td>
<td>Elliptical</td>
<td></td>
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<tr>
<td>NW Size (nm)</td>
<td>10x20</td>
<td>10x20</td>
<td>14</td>
<td>10</td>
<td>10</td>
<td>12</td>
<td>13x20</td>
</tr>
<tr>
<td>Lg (nm)</td>
<td>65</td>
<td>25</td>
<td>100</td>
<td>30</td>
<td>8</td>
<td>65</td>
<td>35</td>
</tr>
<tr>
<td>EOT or Tox (nm)</td>
<td>3</td>
<td>1.8</td>
<td>1.8</td>
<td>2</td>
<td>4</td>
<td>3</td>
<td>1.5</td>
</tr>
<tr>
<td>Vdd (V)</td>
<td>1.0</td>
<td>1.1</td>
<td>1.2</td>
<td>1.0</td>
<td>1.2</td>
<td>1.2</td>
<td>1.0</td>
</tr>
<tr>
<td>Ion (uA) per wire</td>
<td>60.1</td>
<td>102</td>
<td>30.3</td>
<td>26.4</td>
<td>37.4</td>
<td>48.4</td>
<td>43.8</td>
</tr>
<tr>
<td>Ion (uA/um) by dia.</td>
<td>3117</td>
<td>5010</td>
<td>2170</td>
<td>2640</td>
<td>3740</td>
<td>4030</td>
<td>2592</td>
</tr>
<tr>
<td>Ion (uA/um) by cir.</td>
<td>1609</td>
<td>2054</td>
<td>430</td>
<td>841</td>
<td>1191</td>
<td>1283</td>
<td>825</td>
</tr>
<tr>
<td>SS (mV/dec.)</td>
<td>70</td>
<td>79</td>
<td>68</td>
<td>71</td>
<td>75</td>
<td>~75</td>
<td>85</td>
</tr>
<tr>
<td>DIBL (mV/V)</td>
<td>62</td>
<td>56</td>
<td>15</td>
<td>13</td>
<td>22</td>
<td>40-82</td>
<td>65</td>
</tr>
<tr>
<td>Ion/loff</td>
<td>~1E6</td>
<td>&gt;1E6</td>
<td>&gt;1E5</td>
<td>~1E6</td>
<td>&gt;1E7</td>
<td>&gt;1E7</td>
<td>~2E5</td>
</tr>
</tbody>
</table>

Ref[11] by Stmicro Lg=25nm, Tox=1.8nm
This work Lg=65nm, Tox=3nm
$I_{ON}/I_{OFF}$ Bench mark

Planer FET

S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

Si ノワイヤ FET

Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240

$L_g = 500 \sim 65 \text{nm}$

This work

$V_{GS} = 1.0 \sim 1.1 \text{V}$

$V_{GS} = 1.2 \sim 1.3 \text{V}$
1. Increase of Inversion Carrier Density
Electron Density
(x$10^{19}$cm$^{-3}$)

- **Edge portion**
- **Flat portion**

Distance from SiNW Surface (nm)

(a) Metal

(b) Inversion areal ratio: 29 %

$V_g = 1$V

Electron density: Log $|k|$ (cm$^{-3}$)

- 20
- 19.6
- 19.2
- 18.8
- 18.4
- 18.0
- 17.6
- 17.2
- 16.8
- 16.4
- 16.0
Evaluation of Inversion carrier extracted using advanced split-CV measurement

Higher inversion carrier density was obtained with smaller dimensions.

The result of two-dimensional simulation in the previous slide supports these experimental results.

2. Enhancement of Effective Carrier Mobility
Primitive estimation!

Year

ION (µA/µm)

SiNW (12nm □ 19nm)

Small EOT for high-k (33)

P-MOS improvement (26)

Low S/D resistance (20)

(15)

# of wires /1µm

Compact model

SI NW (12nm □ 19nm)

Assumption

ION □ Lg^{-0.5} □ T_{ox}^{-1}

bulk

FD

ITRS

MG

Compact model

Small EOT for high-k (33)

P-MOS improvement (26)

Low S/D resistance (20)

(15)

# of wires /1µm

ION □ Lg^{-0.5} □ T_{ox}^{-1}

bulk

FD

ITRS

MG
Our roadmap for R&D
Source: H. Iwai, IWJT 2008

Current Issues

Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Brain

Ultra small volume
Small number of neuron cells
Extremely low power
Real time image processing
(Artificial) Intelligence
3D flight control

System and Algorism becomes more important!

Sensor
Infrared
Humidity
CO₂

Dragonfly is further high performance

But do not know how?