Si Nanowire Device and its Modeling

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Integrated Circuits Technologies are still very important for Green or power saving!

1. Green by Integrated Circuits

   Power saving by Microprocessor control for all the human systems

2. Green of Integrated Circuits

   Power saving of Integrated Circuits by Down Scaling of MOSFETs in PC, Data Center, Router, etc.

Down scaling is the most effective way of Power saving.

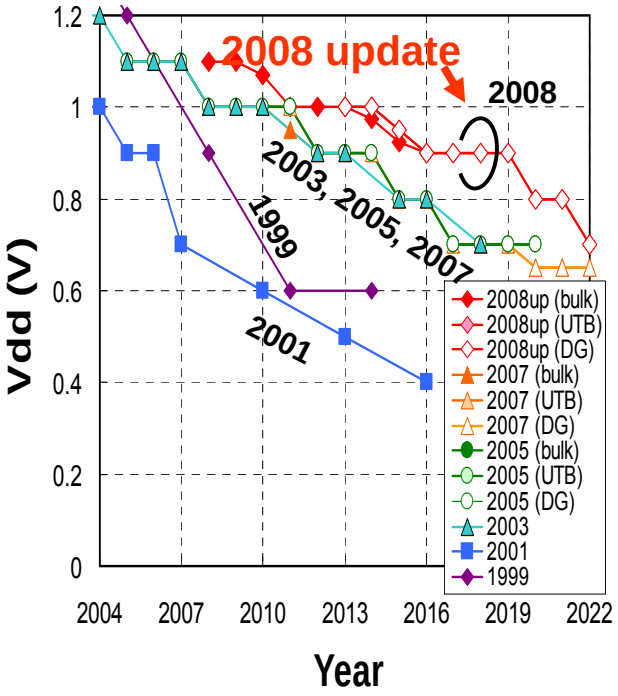
It has been always discussed about the limit of downscaling, but the down scaling of MOSFETs is still possible for another 10 or 20 years!

3 important technological items for DS.

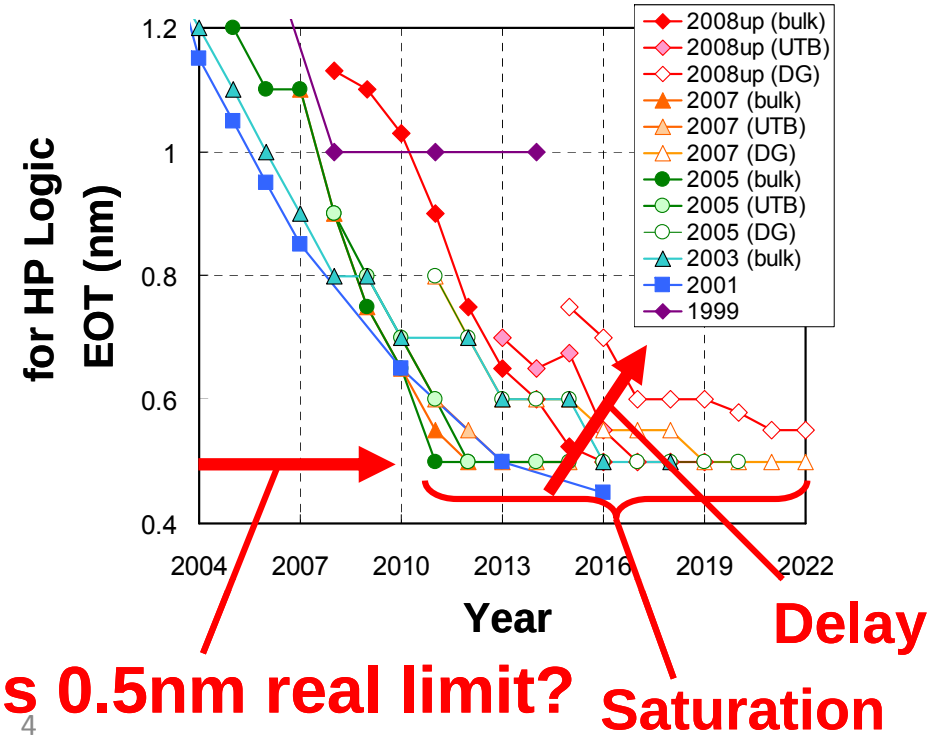
1. Thinning of high-k beyond 0.5 nm
2. Metal S/D
3. Si-Nanowire FET

ITRS

Vdd stay high



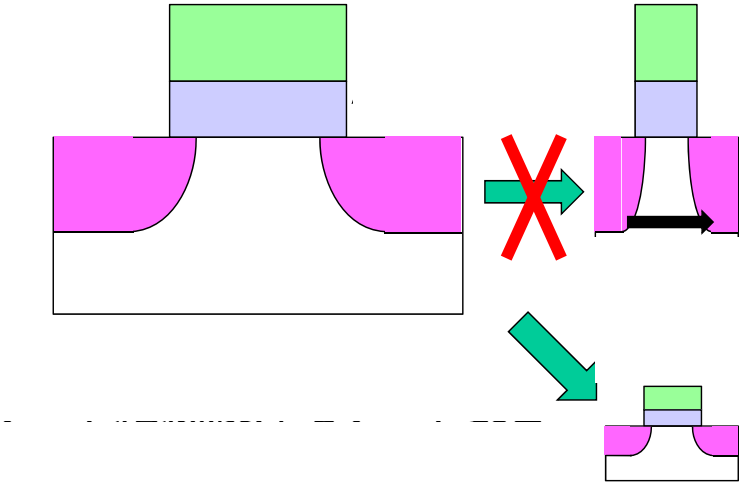
ITRS EOT limit = 0.5 nm?



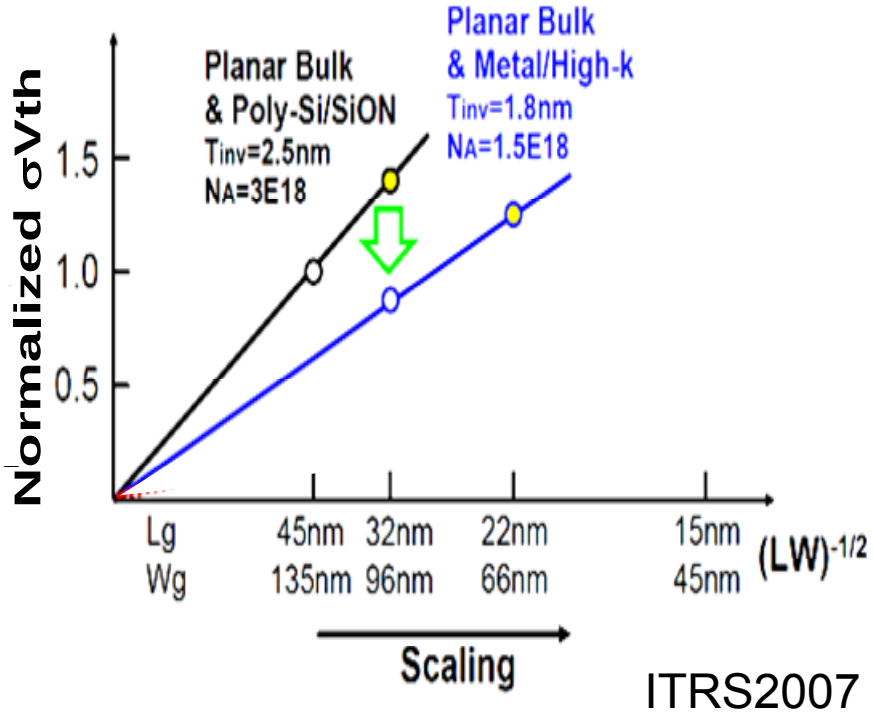
Scaling of high beyond 0.5 nm is important

$$\text{Power of FET} = CV^2/2 \propto D^3 \ (=L^3)$$

Problems
→SCE
→Variation in Vth
→Increase in Off-leakage current

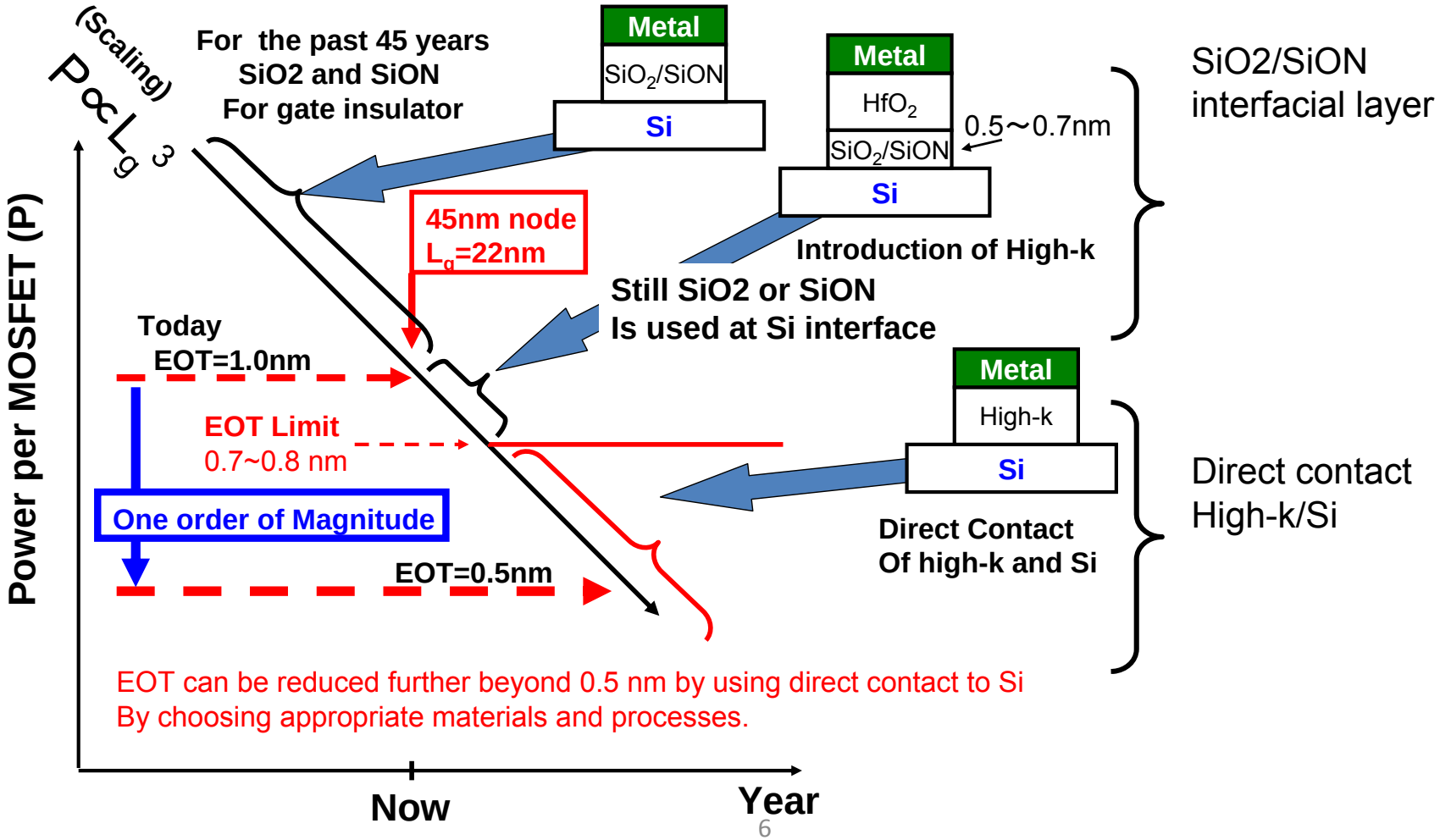


Solution

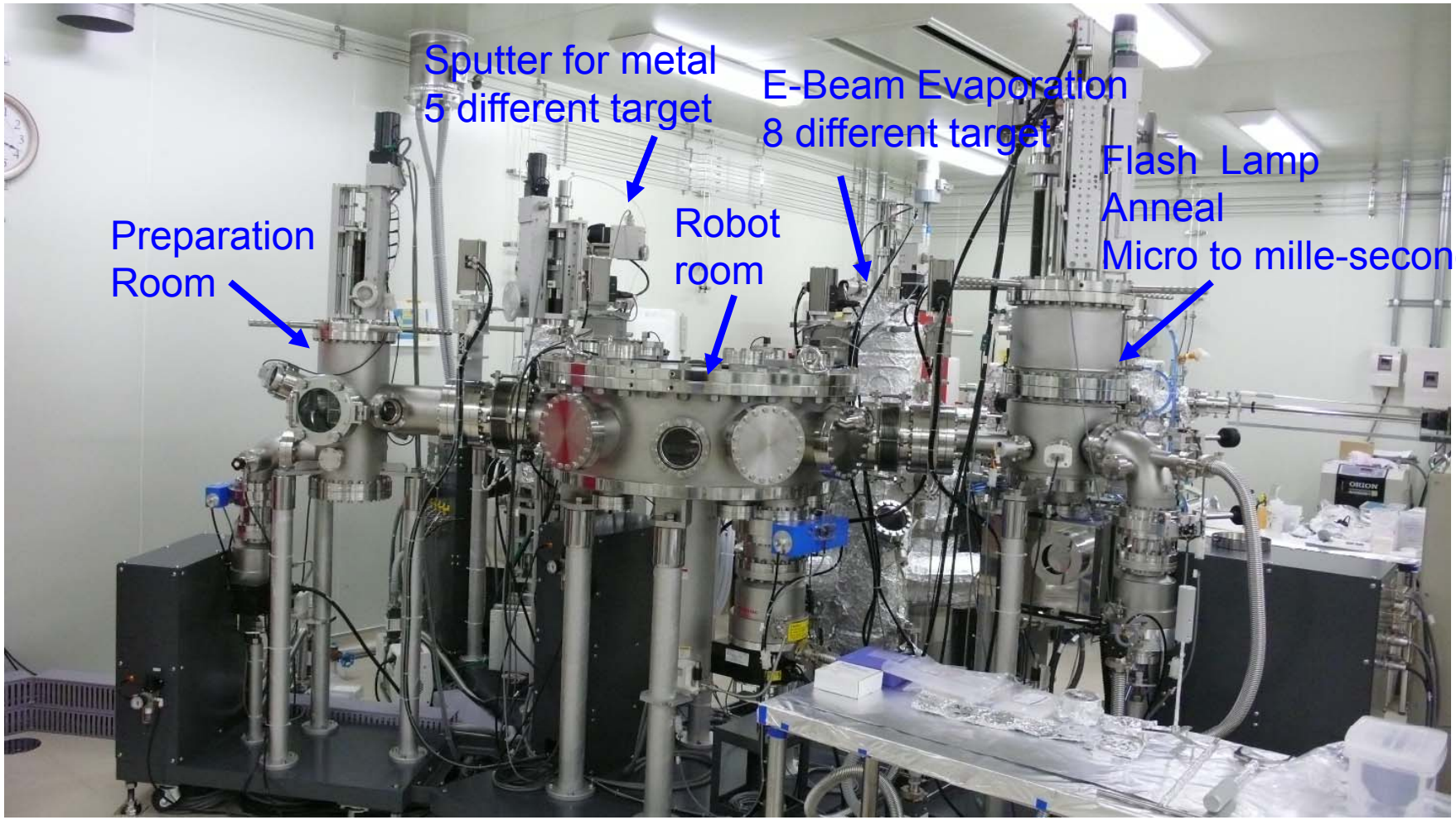


ITRS2007

Direct contact of high-k to Si

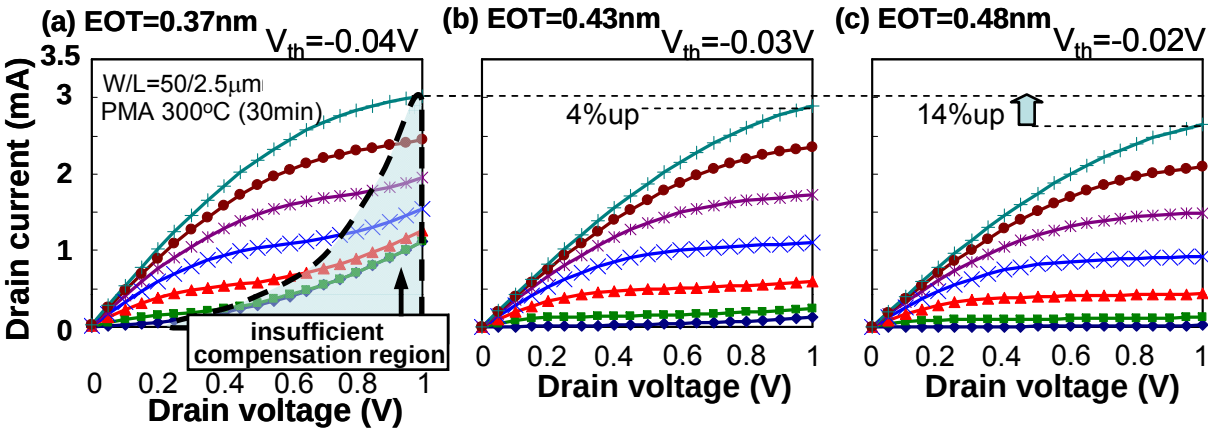


Cluster tool for high-k thin film deposition



Challenge to EOT~0.3nm

EOT<0.5nm with Gain in Drive Current

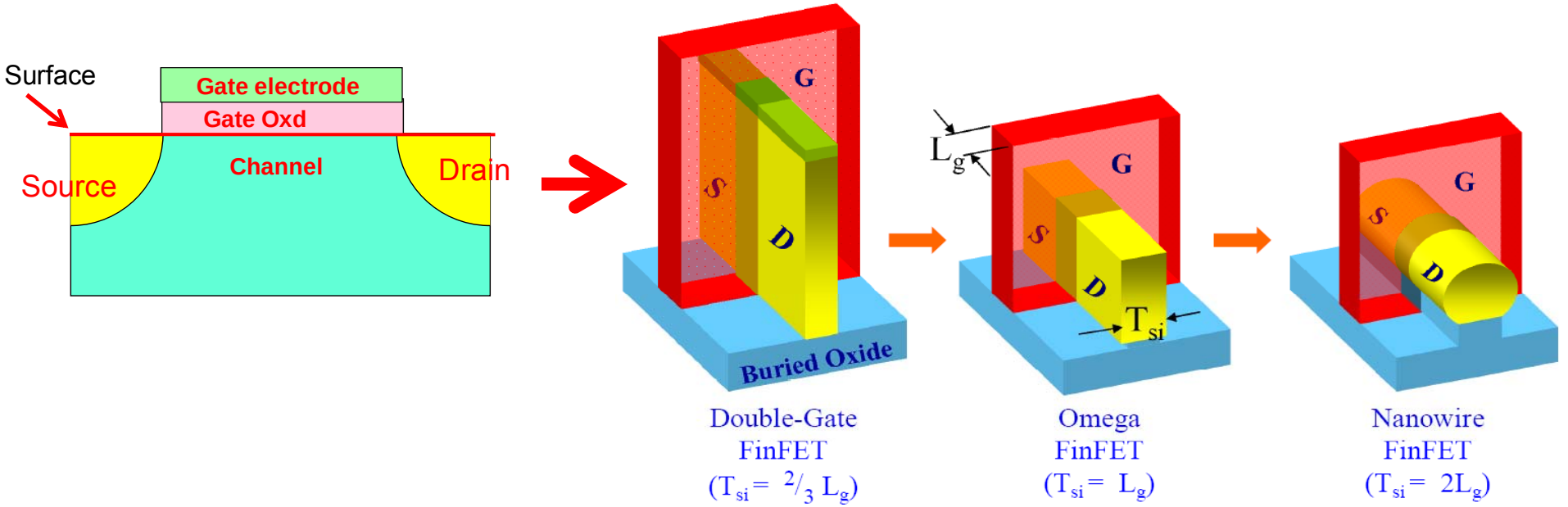


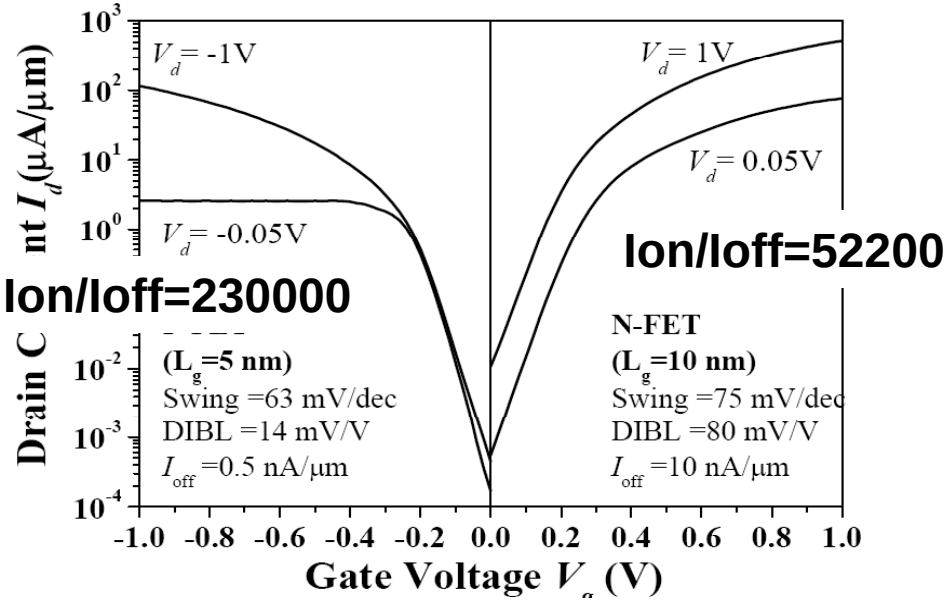
14% of I_d increase is observed even at saturation region

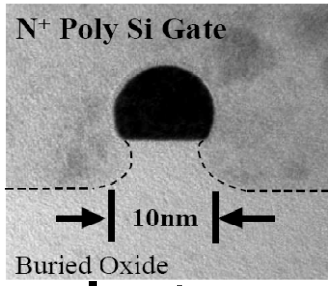
EOT below 0.4nm is still useful for scaling

Si Nanowire FET

FinFET to Nanowire







Channel conductance is well controlled by Gate even at L=5nm

F.-L.Yang, VLSI2004

Nanowire FET

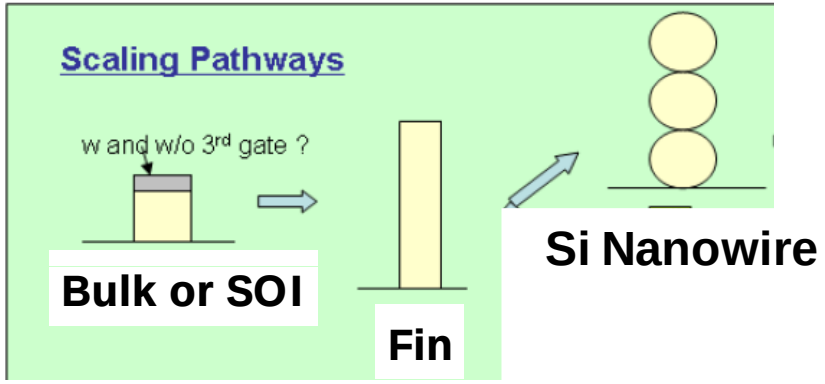
First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
Device Structures																
Planar bulk	←							→								
FDSOI					←								→			
Multiple Gate							←									→

Nanowire FET

Multiple Gate (Fin)FET

ITRS 2009

Bulk → Fin → Nanowire

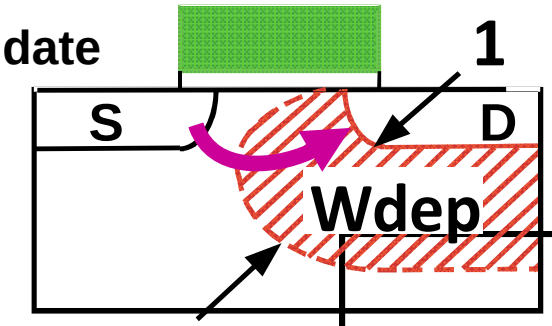


Si nanowire FET as a strong candidate

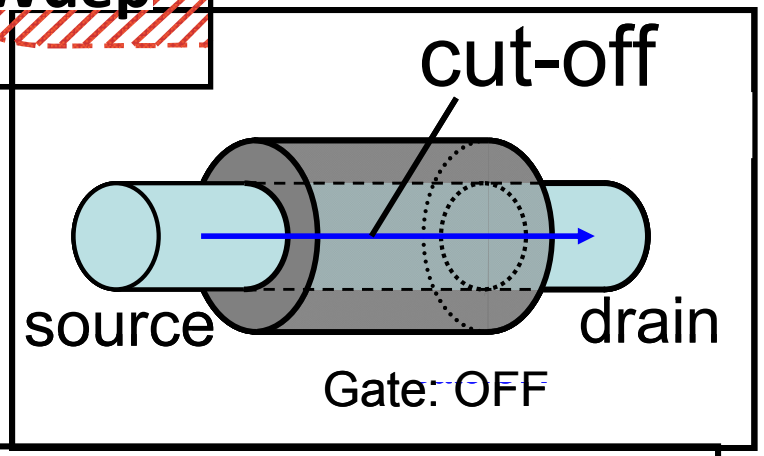
1. Compatibility with
   current CMOS process

2. Good controllability of I_{OFF}

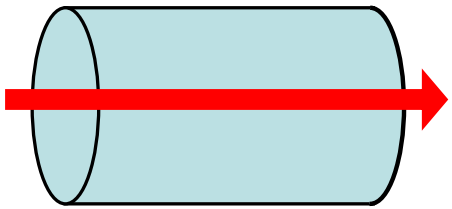
3. High drive current



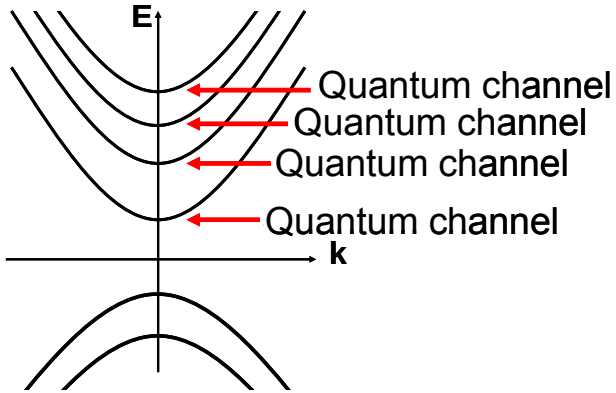
Leakage current



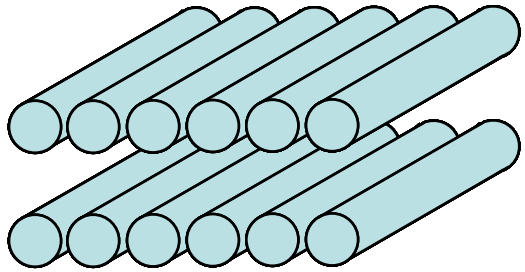
1D ballistic conduction

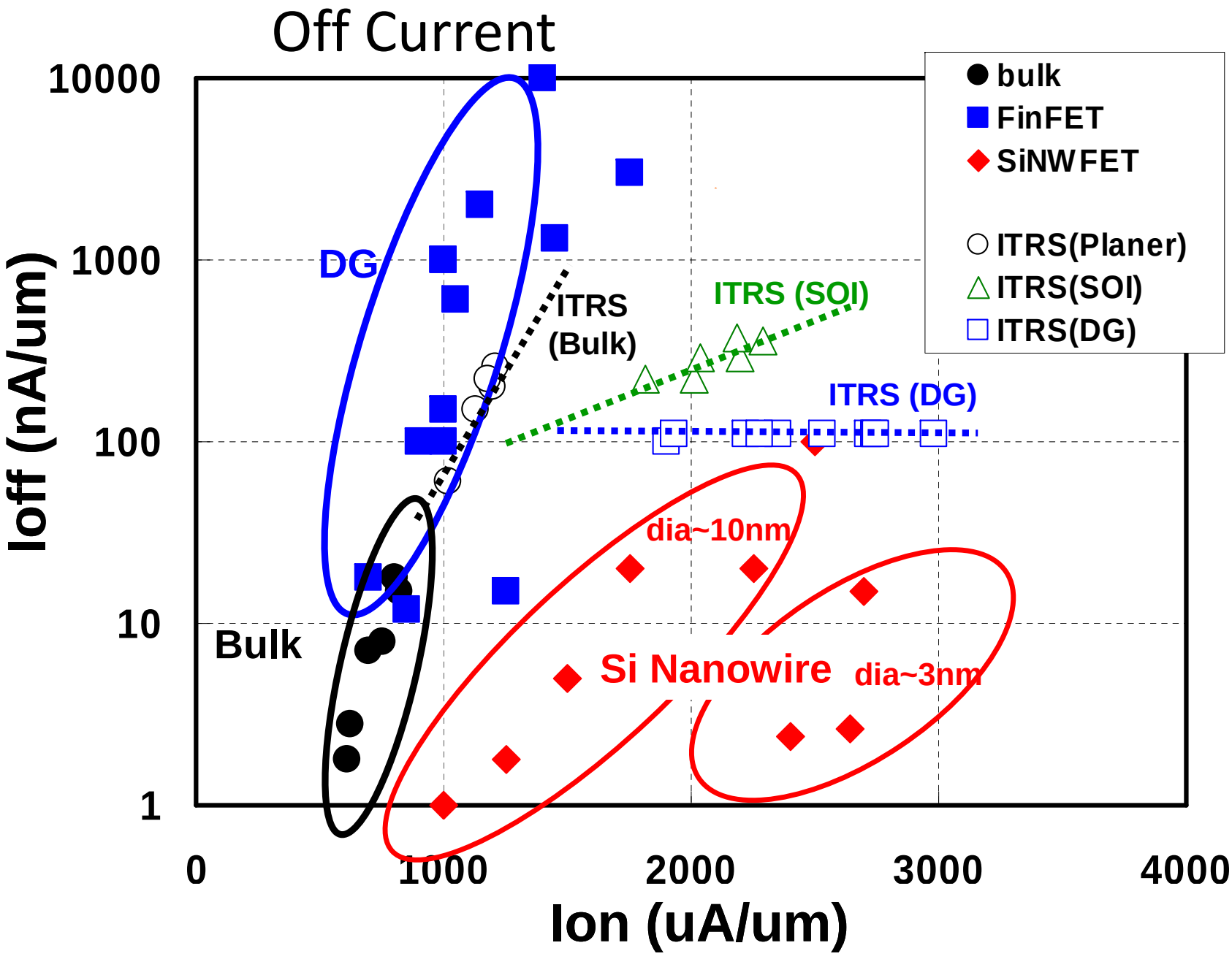


Multi quantum Channel



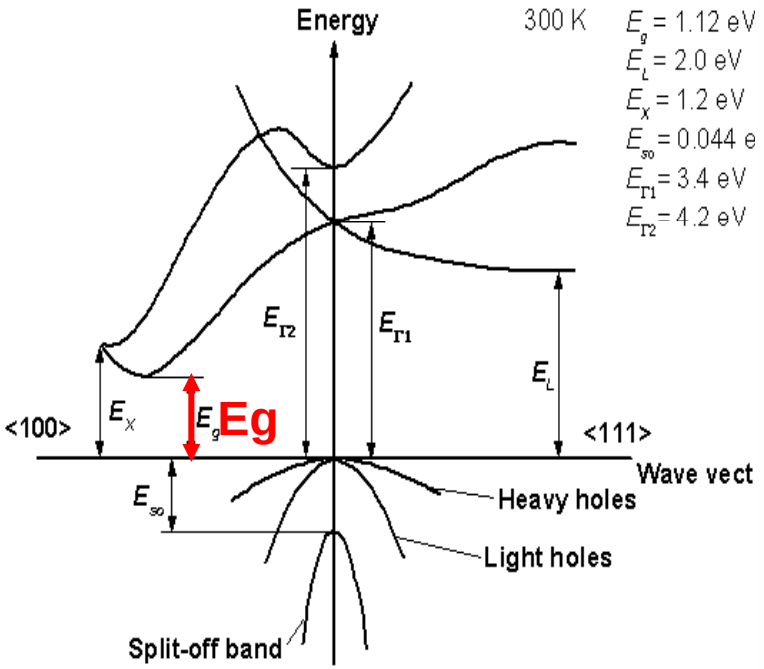
High integration of wires



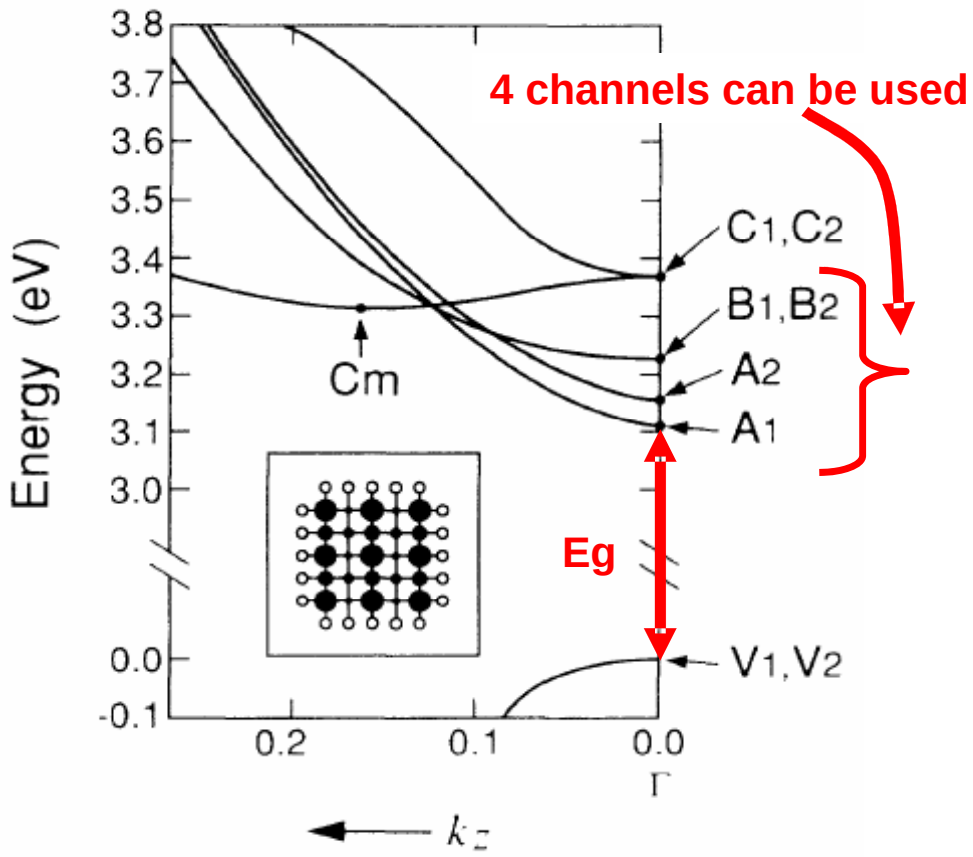

Off Current
10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



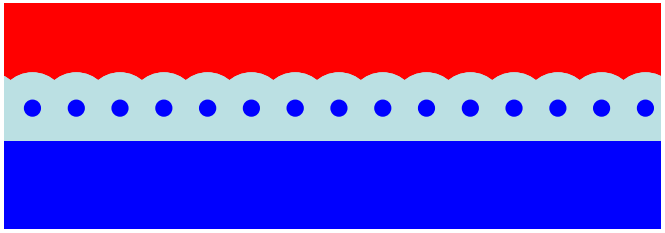
Energy band of Bulk Si



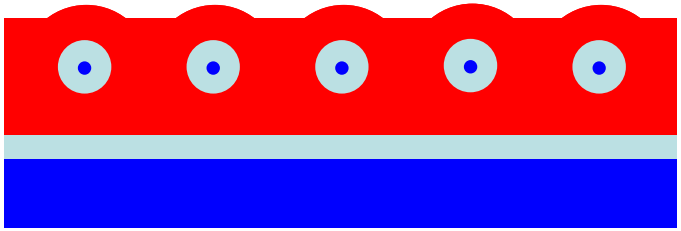
Energy band of 3 x 3 Si wire

Maximum number of wires per 1 μm

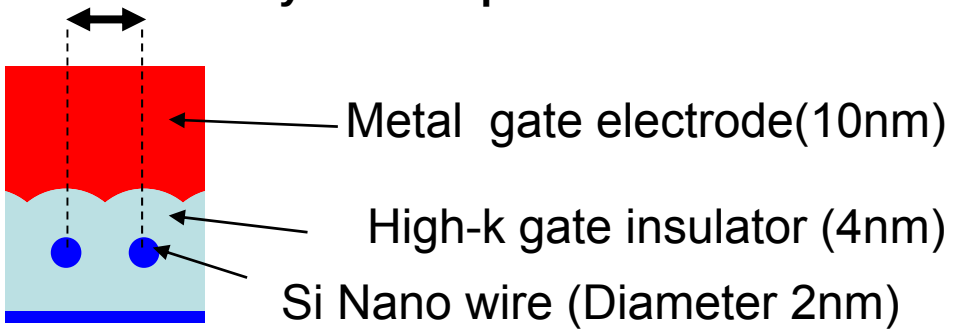
Front gate type MOS 165 wires /μm

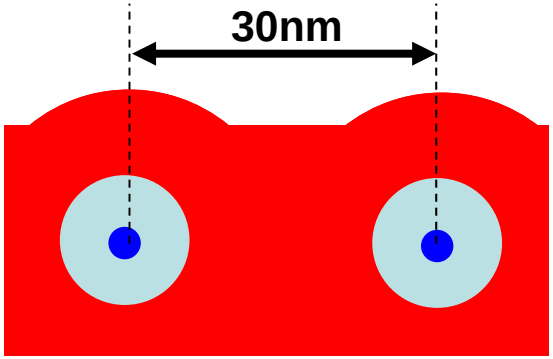


Surrounded gate type MOS 33 wires/μm

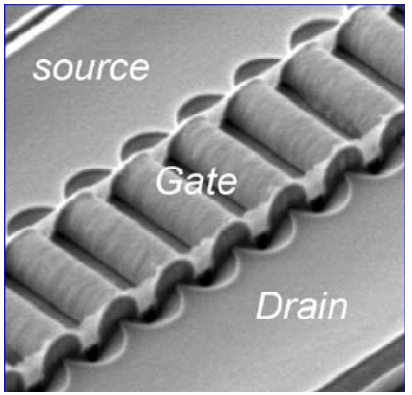


6nm pitch
By nano-imprint method



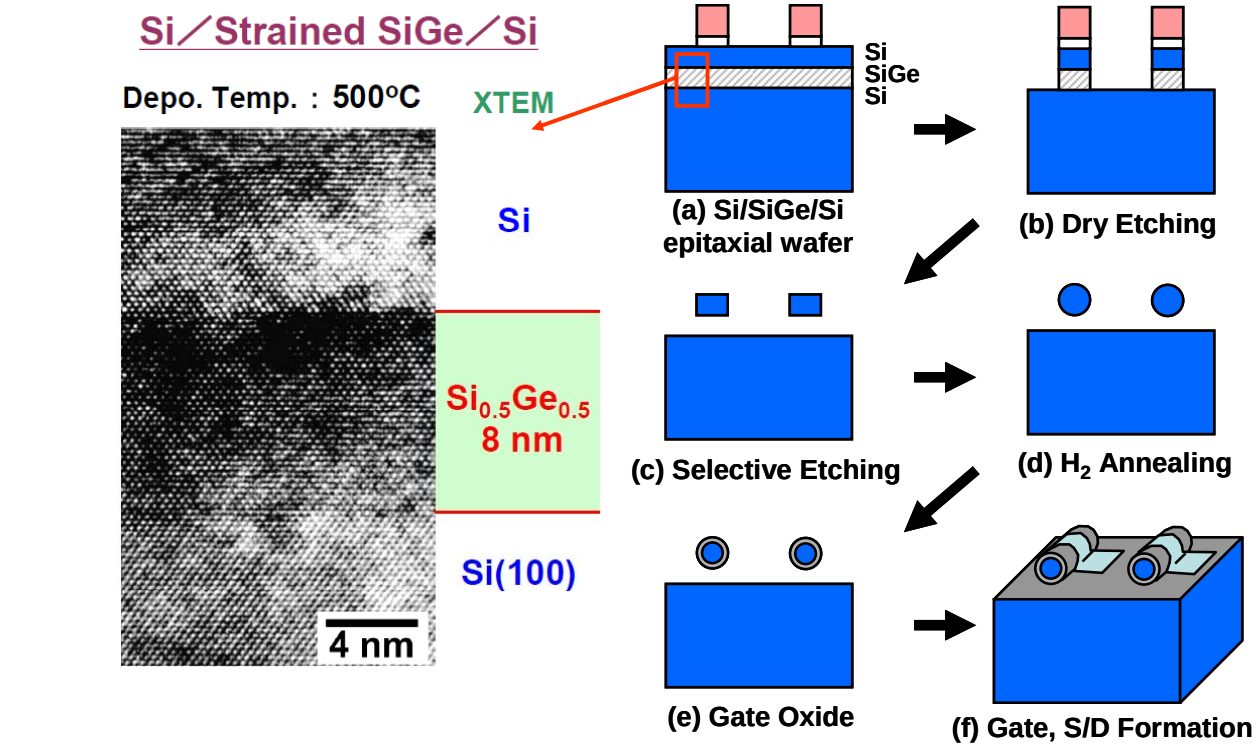


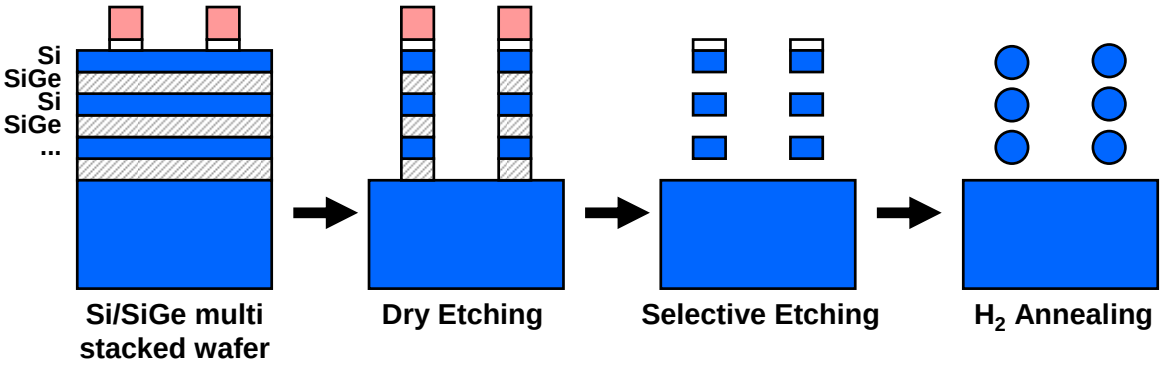
30nm pitch:
EUV lithograpy



Surrounded gate MOS

Increase the number of wires towards vertical dimension

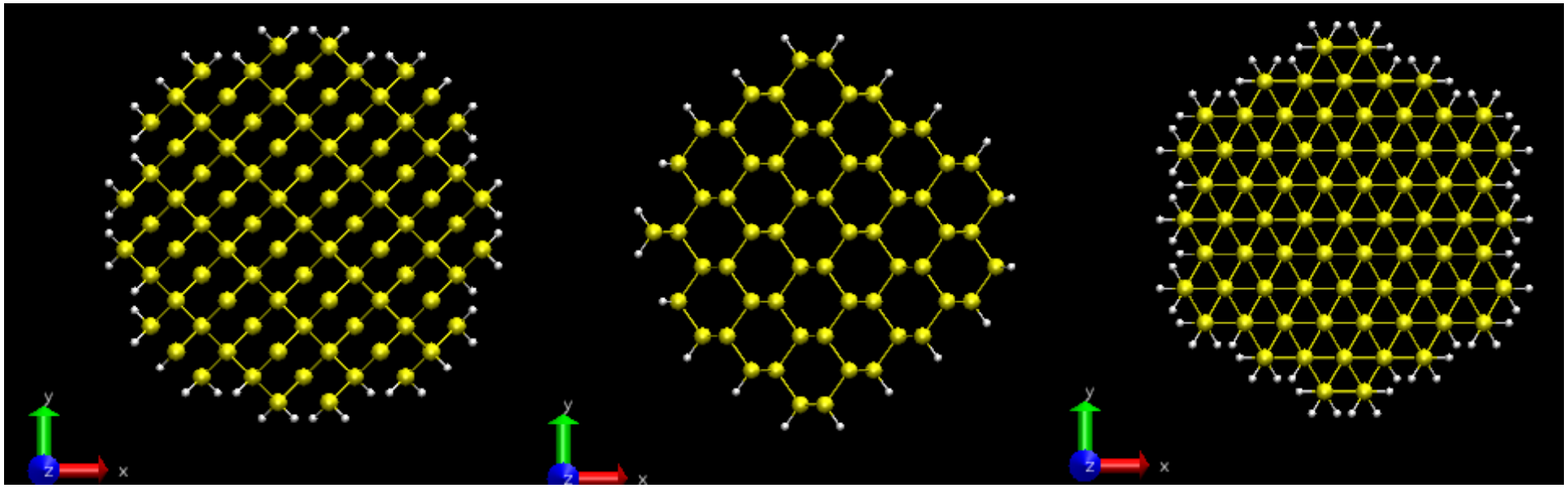




SiNW Band structure calculation

Cross section of Si NW

First principal calculation,

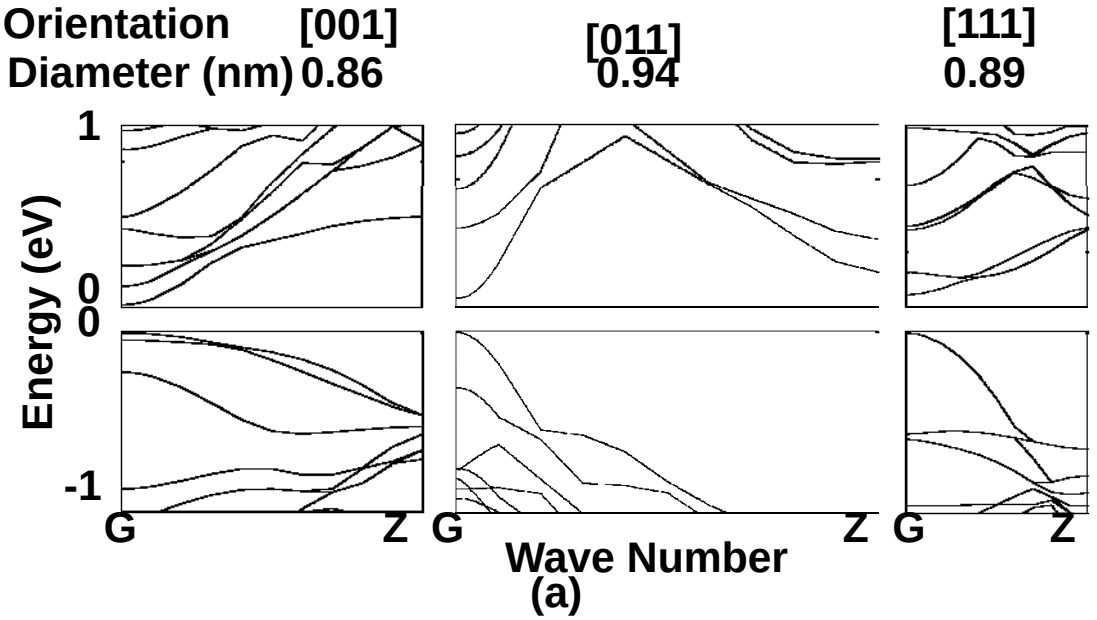


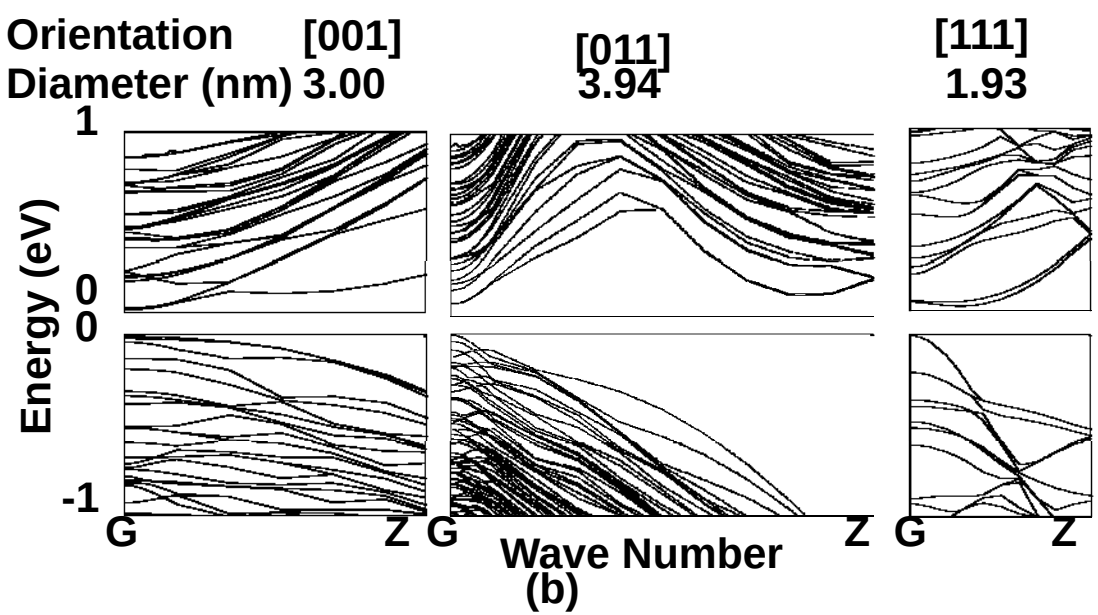
D=1.96nm
[001]

D=1.94nm
[011]

D=1.93nm
[111]

Si nanowire FET with 1D Transport

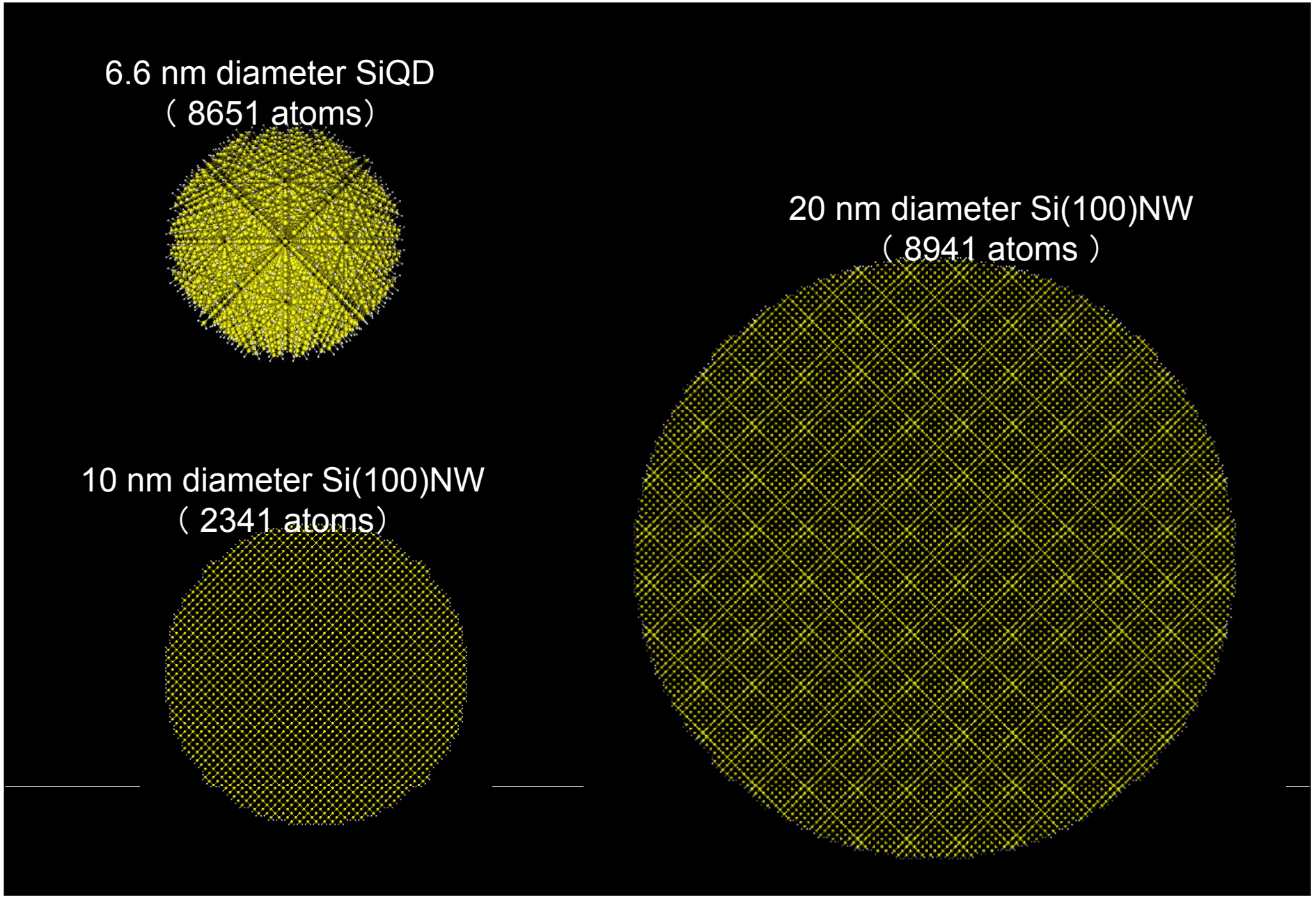




Small mass with [011]

Large number of quantum channels with [001]

Atomic models of a Si quantum dot and Si nanowires



RSDFT – suitable for parallel first-principles calculation -

- ✓Real-Space Finite-Difference
- ✓Sparse Matrix
- ✓FFT free (FFT is inevitable in the conventional plane-wave code)
- ✓MPI (Message Passing Interface) library

Higher-order finite difference pseudopotential method
J. R. Chelikowsky et al., Phys. Rev. B, (1994)

3D grid is divided by several regions for parallel computation.

Kohn-Sham eq. (finite-difference)

$$\left(-\frac{1}{2}\nabla^2 + v_s[\rho](\mathbf{r}) + \hat{v}_{nloc}^{PP}(\mathbf{r})\right)\phi_n(\mathbf{r}) = \varepsilon_n\phi_n(\mathbf{r})$$

Higher-order finite difference

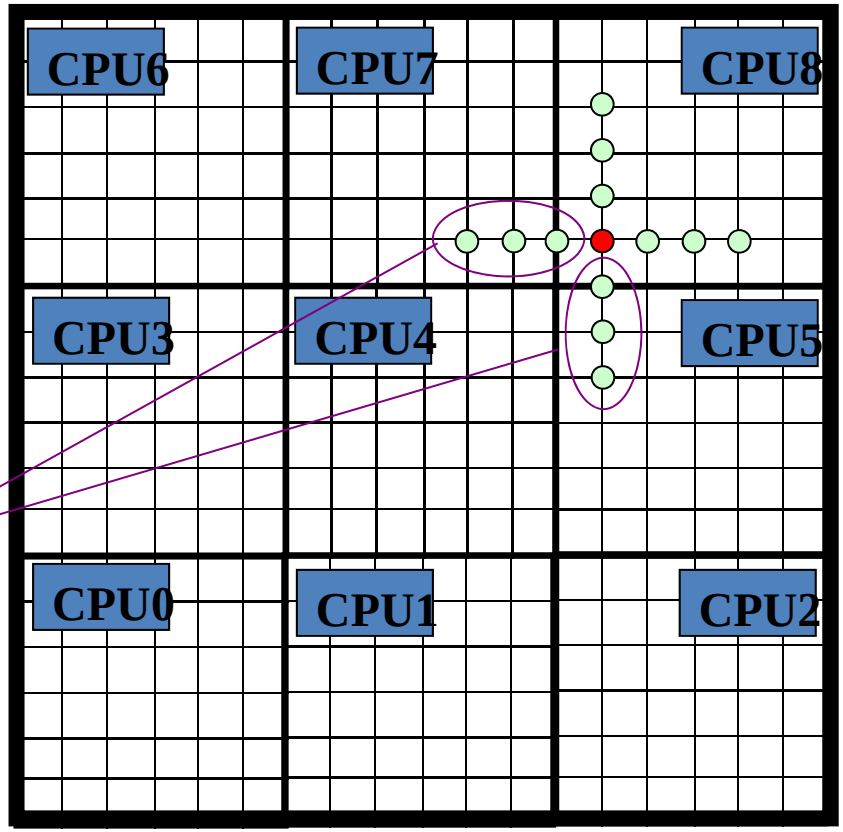
$$\frac{\partial^2}{\partial x^2}\psi_n(x,y,z) \approx \sum_{m=-6}^{6} C_m\psi_n(x+m\Delta x, y, z)$$

MPI_ISEND, MPI_IRECV

Integration

$$\int \psi_m(\mathbf{r})\psi_n(\mathbf{r})d\mathbf{r} \approx \sum_{i=1}^{Mesh} \psi_m(\mathbf{r}_i)\psi_n(\mathbf{r}_i)\Delta x\Delta y\Delta z$$

MPI_ALLREDUCE



Massively Parallel Computing

with our recently developed code “RSDFT”

Iwata et al, J. Comp. Phys., to be published

Real-Space Density-Functional Theory code (RSDFT)

Based on the finite-difference pseudopotential method (J. R. Chelikowsky et al., PRB1994)

Highly tuned for massively parallel computers

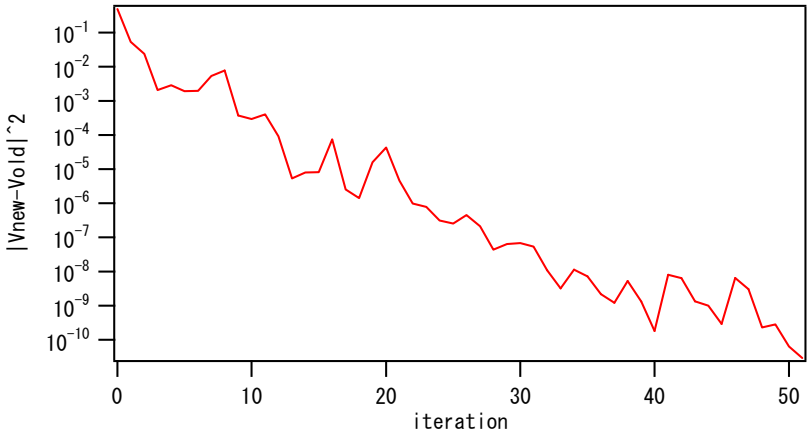
Computations are done on a massively-parallel cluster **PACS-CS** at University of Tsukuba.

(Theoretical Peak Performance = 5.6GFLOPS/node)

e.g.) The system over 10,000 atoms → $Si_{10701}H_{1996}$
(7.6 nm diameter Si dot)

Convergence behavior for $Si_{10701}H_{1996}$

Grid points = 3,402,059
Bands = 22,432

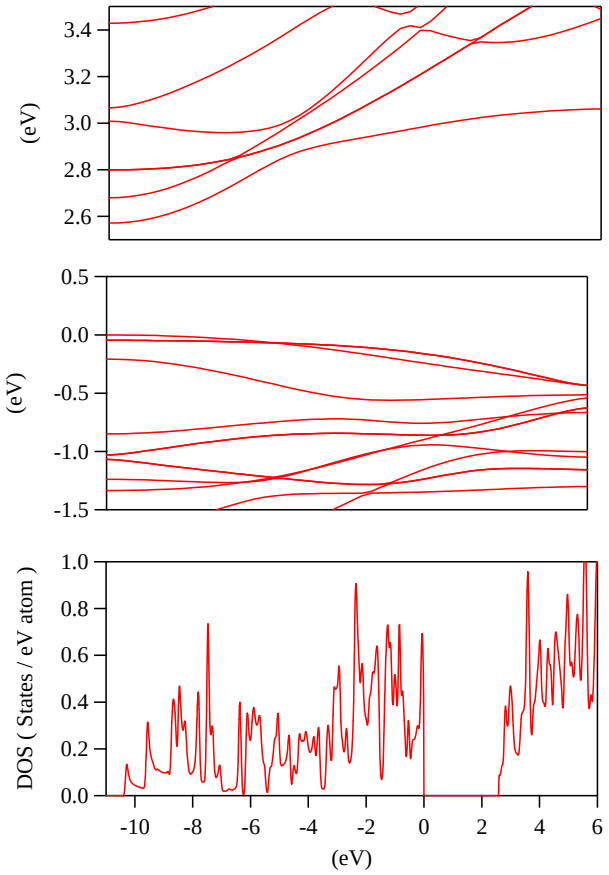


Computational Time (with 1024 nodes of PACS-CS)

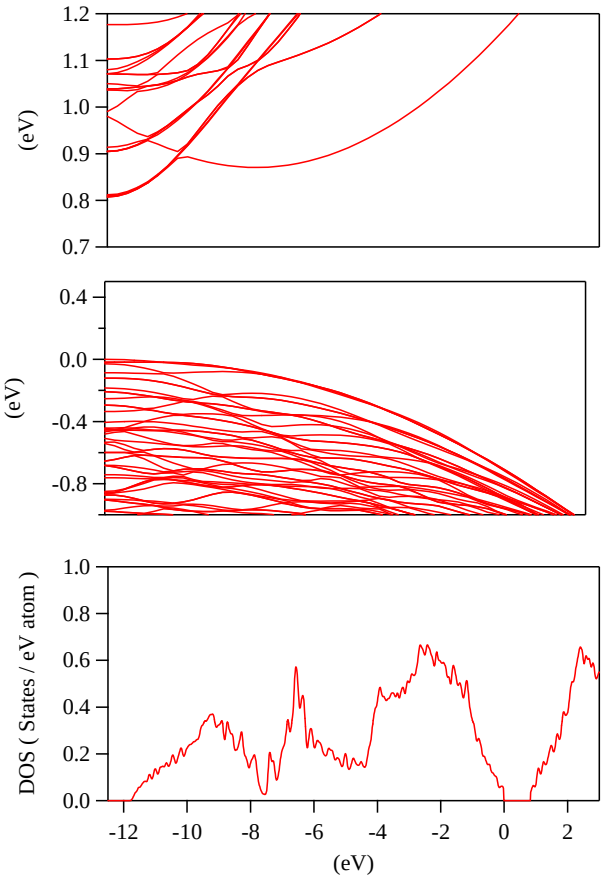
6781 sec. × 60 iteration step = 113 hour

Band Structure and DOS of Si(100)NWs (D=1nm, 4nm, and 8nm)

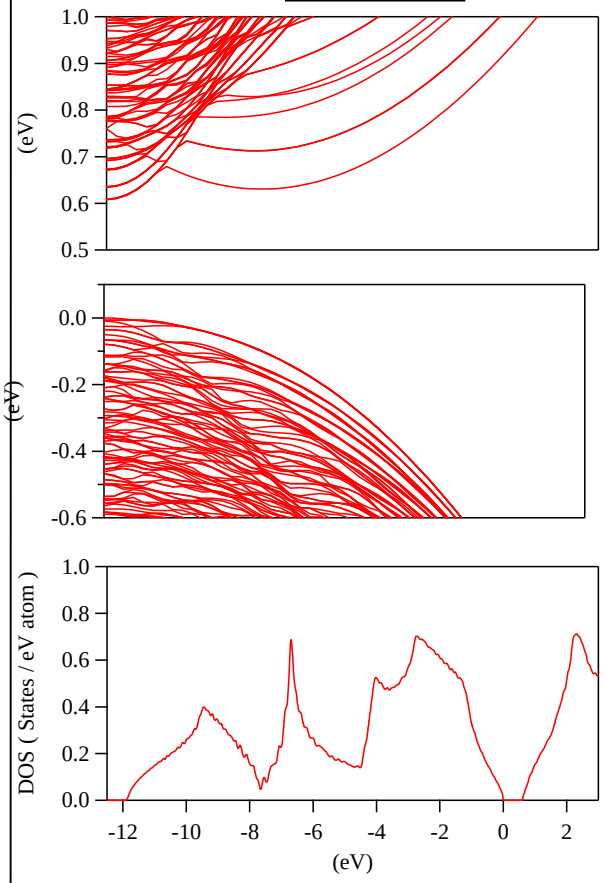
D=1nm



D=4nm



D=8nm



D=1 nm
Si21H20（41 atoms)
KS band gap=2.60eV

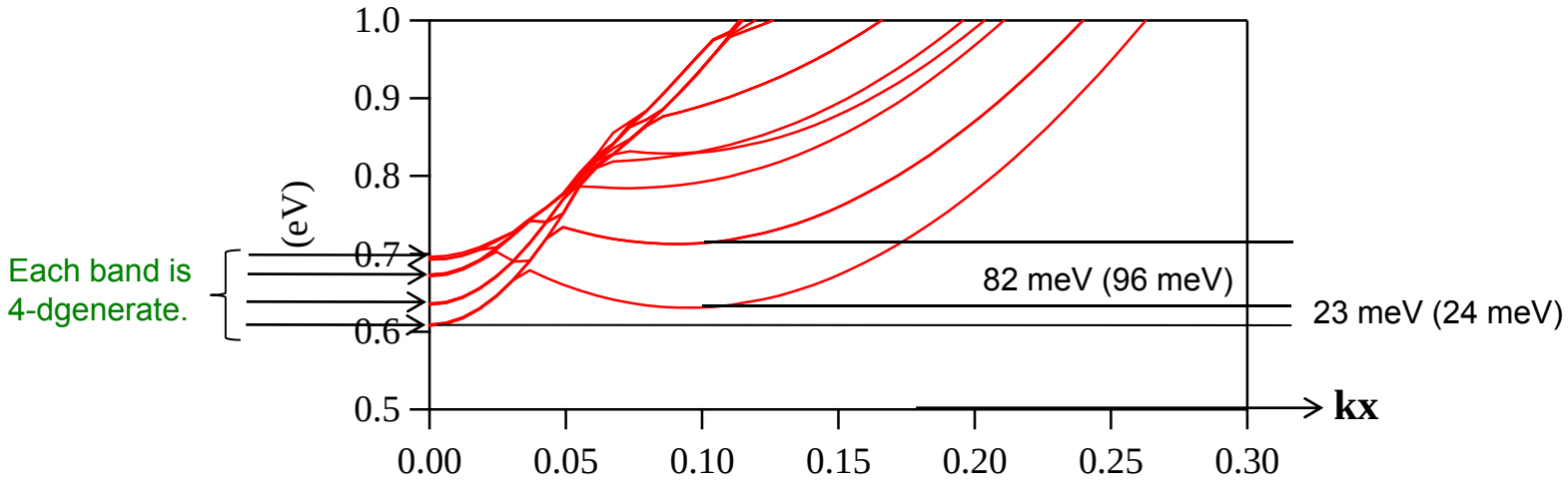
D = 4 nm
Si341H84（425 atoms)
KS band gap = 0.81eV

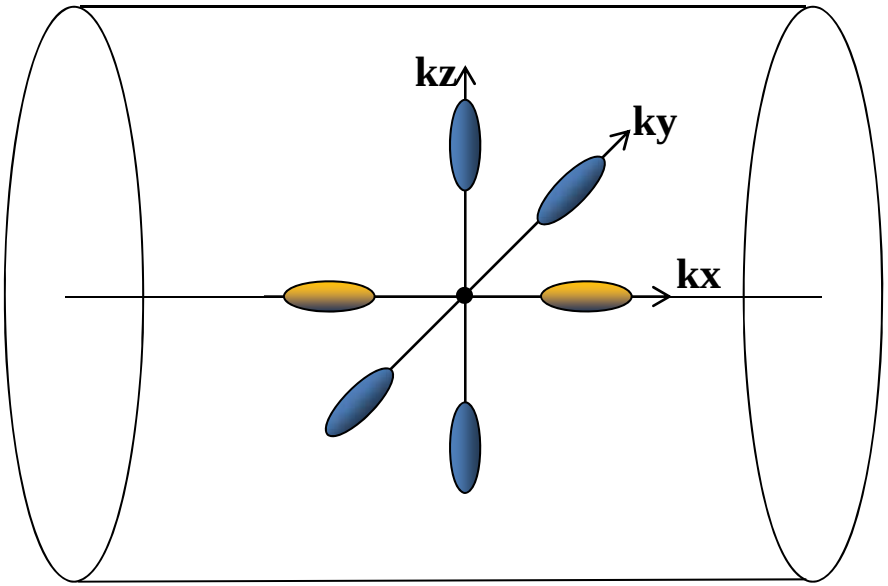
D=8 nm
Si1361H164 (1525 atoms)
KS band gap=0.61eV

KS band gap of bulk (LDA) = 0.53eV

Band structure of 8-nm-diameter Si nanowire near the CBM

- KS band gap = 0.608 eV (@Γ)



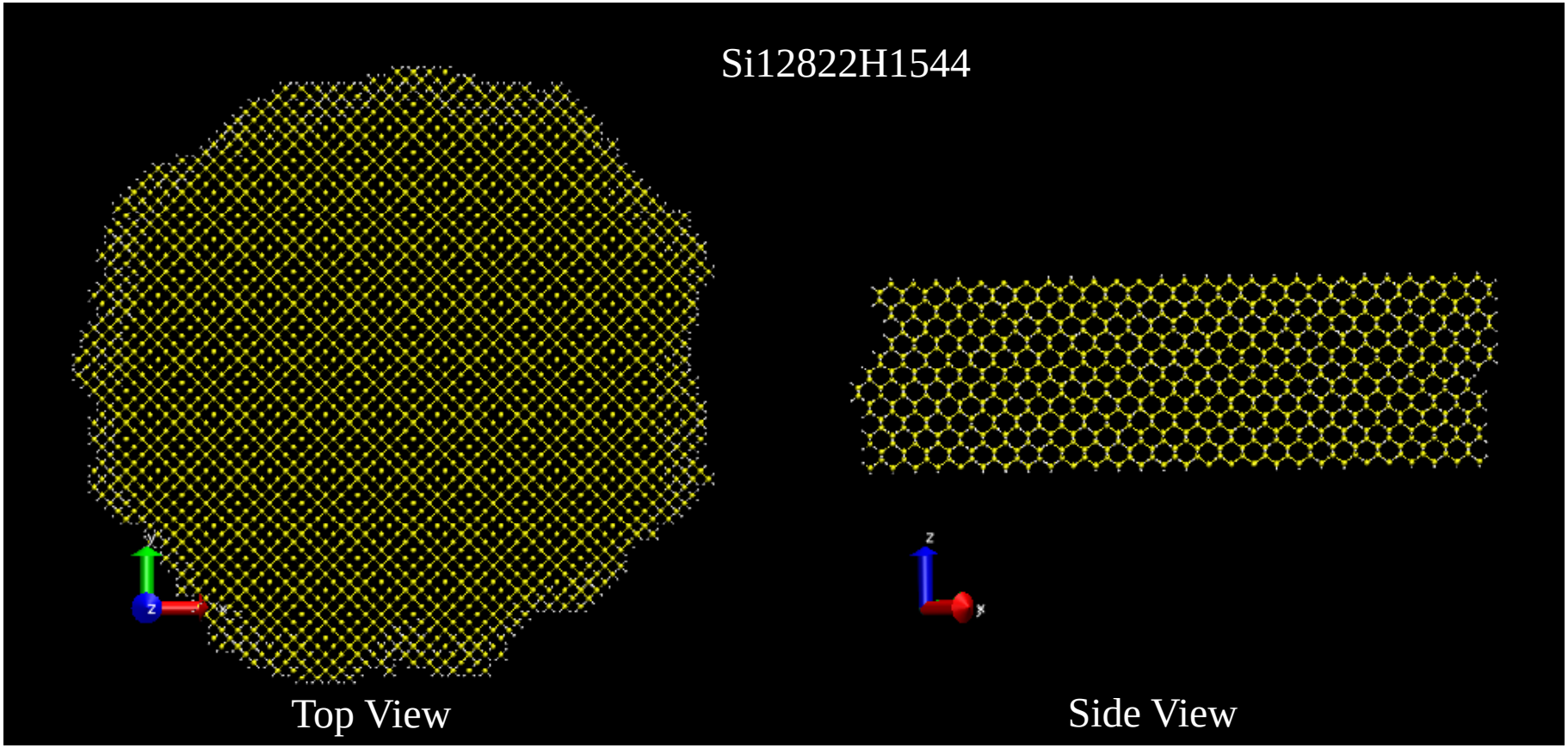


Effective mass equation

$$\left[-\frac{\hbar^2}{2m_t^*}\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}\right)-\frac{\hbar^2}{2m_l^*}\frac{\partial^2}{\partial z^2}\right]\Phi(\mathbf{r})=(\varepsilon-\varepsilon_{CBM})\Phi(\mathbf{r})$$

The band structure can be understood that electrons near the CBM in the bulk Si are Confined within a cylindrical geometry.

Si nano wire with surface roughness

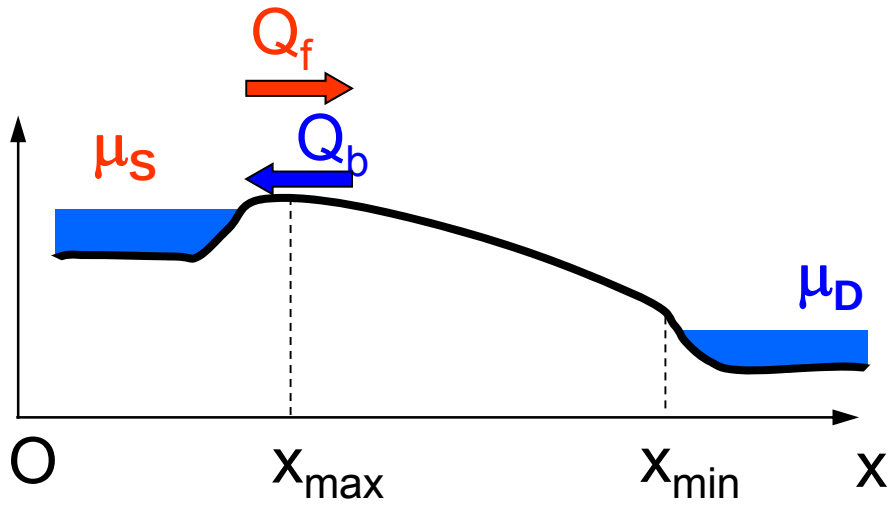


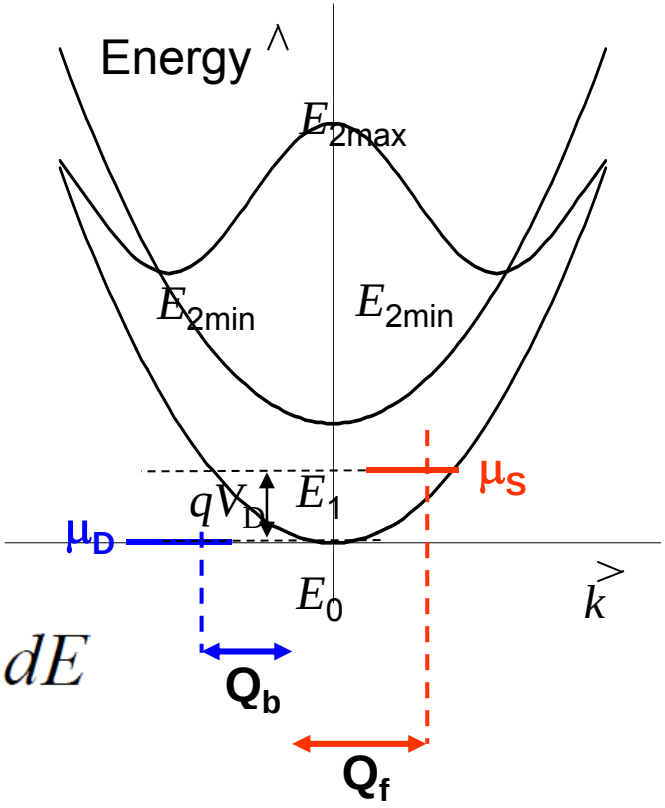
Si12822H1544（14,366 atoms）

- 10nm diameter、3.3nm height、(100)
- Grid spacing：0.45Å (~14Ry)
- # of grid points：4,718,592
- # of bands：29,024
- Memory：1,022GB～2,044GB

SiNW Band compact model

Landauer Formalism for Ballistic FET



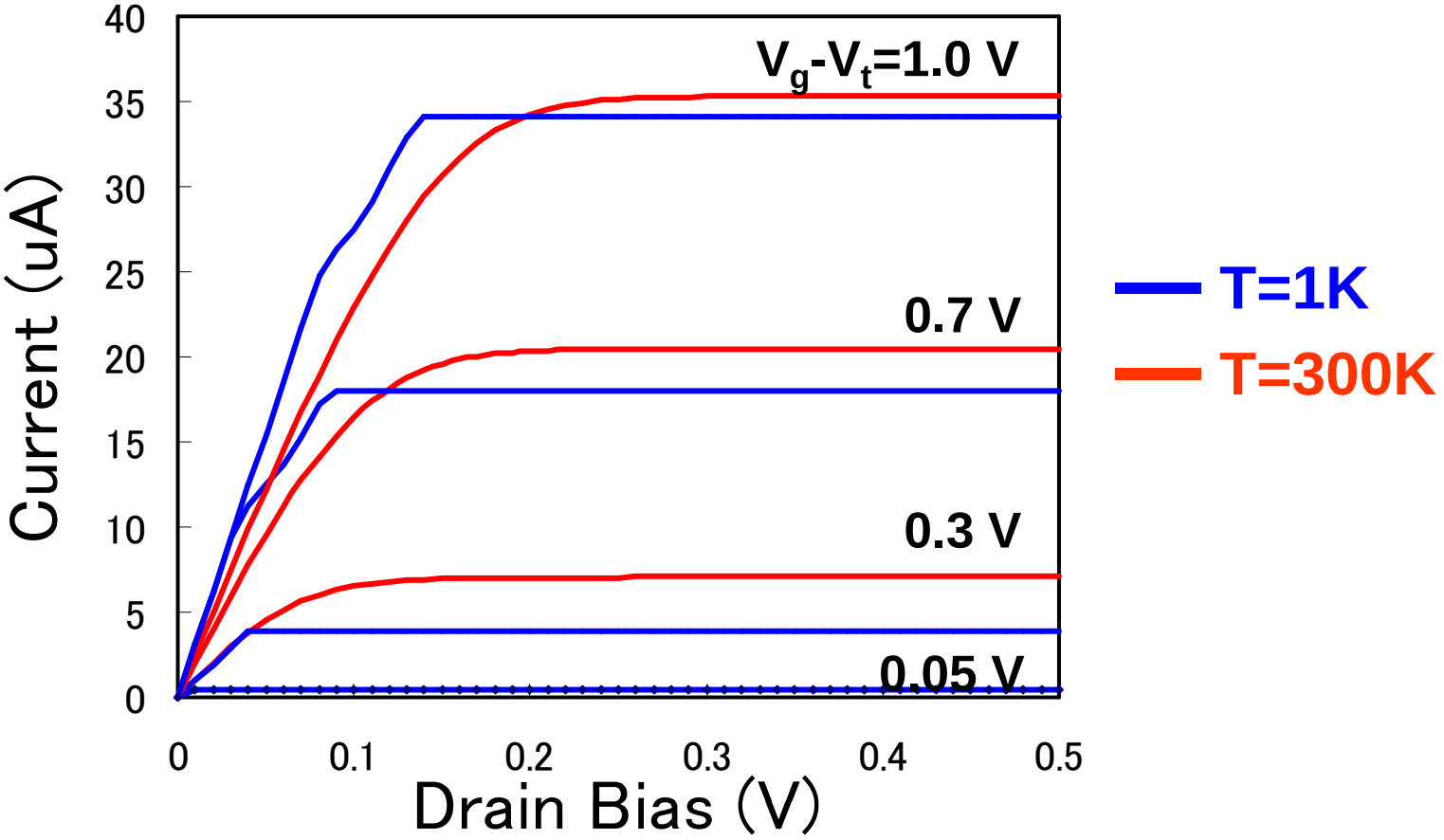


$$I_D = \frac{q}{\pi\hbar}\sum_i \int \left[f(E,\mu_S) - f(E,\mu_D) \right] T_i(E)\, dE$$

From x_{max} to x_{min} $\quad T_i(E) \approx 1$

$$I_D = G_0 \left(\frac{k_B T}{q} \right) \sum_i g_i \ln\left\{ \frac{1+\exp\left[(\mu_S - E_{i0})/k_B T\right]}{1+\exp\left[(\mu_D - E_{i0})/k_B T\right]} \right\}$$

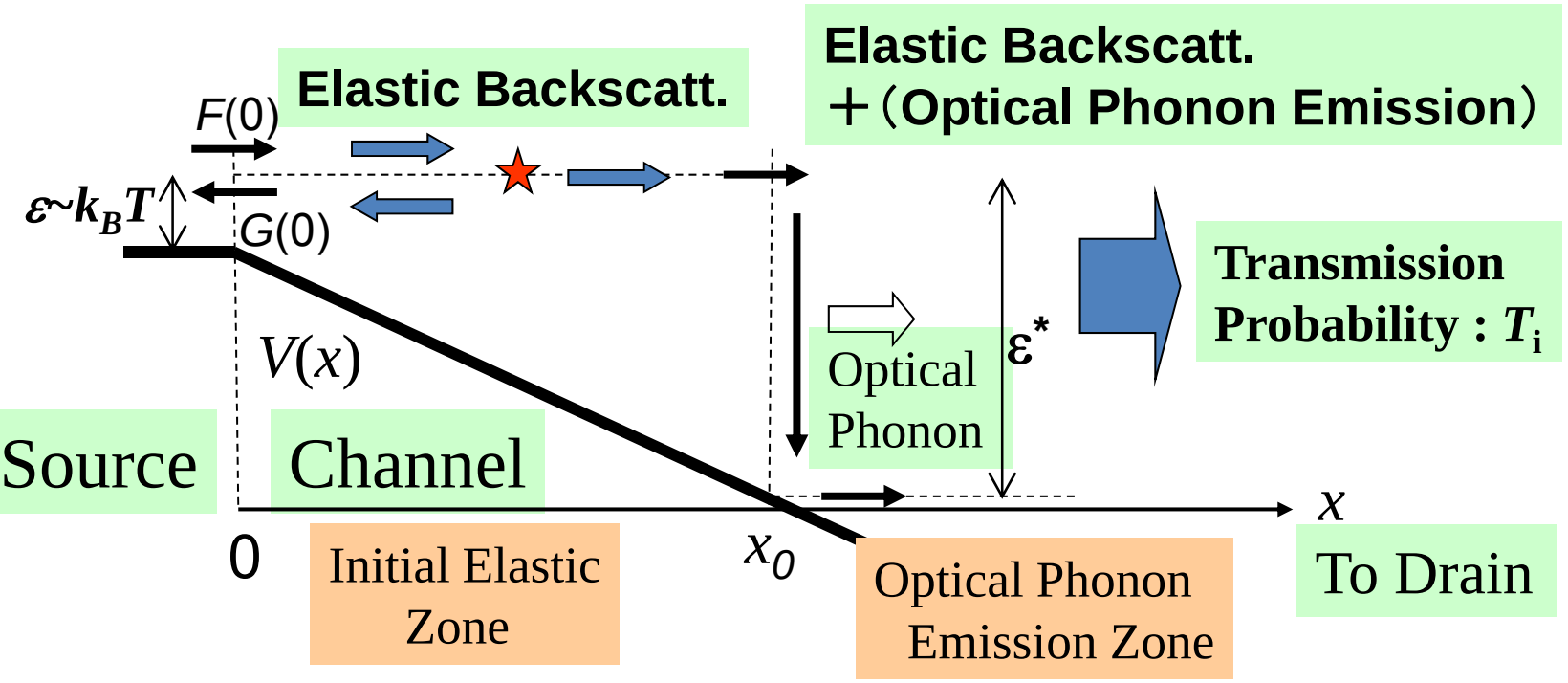
IV Characteristics of Ballistic SiNW FET



Small temperature dependency
35μA/wire for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx. : Electric Field E



Transmission Probability to Drain

$$T(\varepsilon) = \left.\frac{F(0) - G(0)}{F(0)}\right)_{\text{Injection from Drain}=0}$$

Résumé of the Compact Model

$$I = \frac{q}{\pi \hbar} \sum_i g_i \int \left[f(\varepsilon, \mu_s) - f(\varepsilon, \mu_D) \right] T_i \, d\varepsilon$$

$$C_G = \frac{2\pi \varepsilon_{ox}}{\ln\left\{ \dfrac{\sqrt{2r + t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r + t_{ox}} - \sqrt{t_{ox}}} \right\}}.$$

Planar Gate

$$(V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{\left| Q_f + Q_b \right|}{C_G}.$$

$$\mu_S - \mu_D = qV_D$$

$$C_G = \frac{2\pi \varepsilon_{ox}}{\ln\left(\dfrac{r + t_{ox}}{r} \right)}.$$

GAA

(Electrostatics requirement)

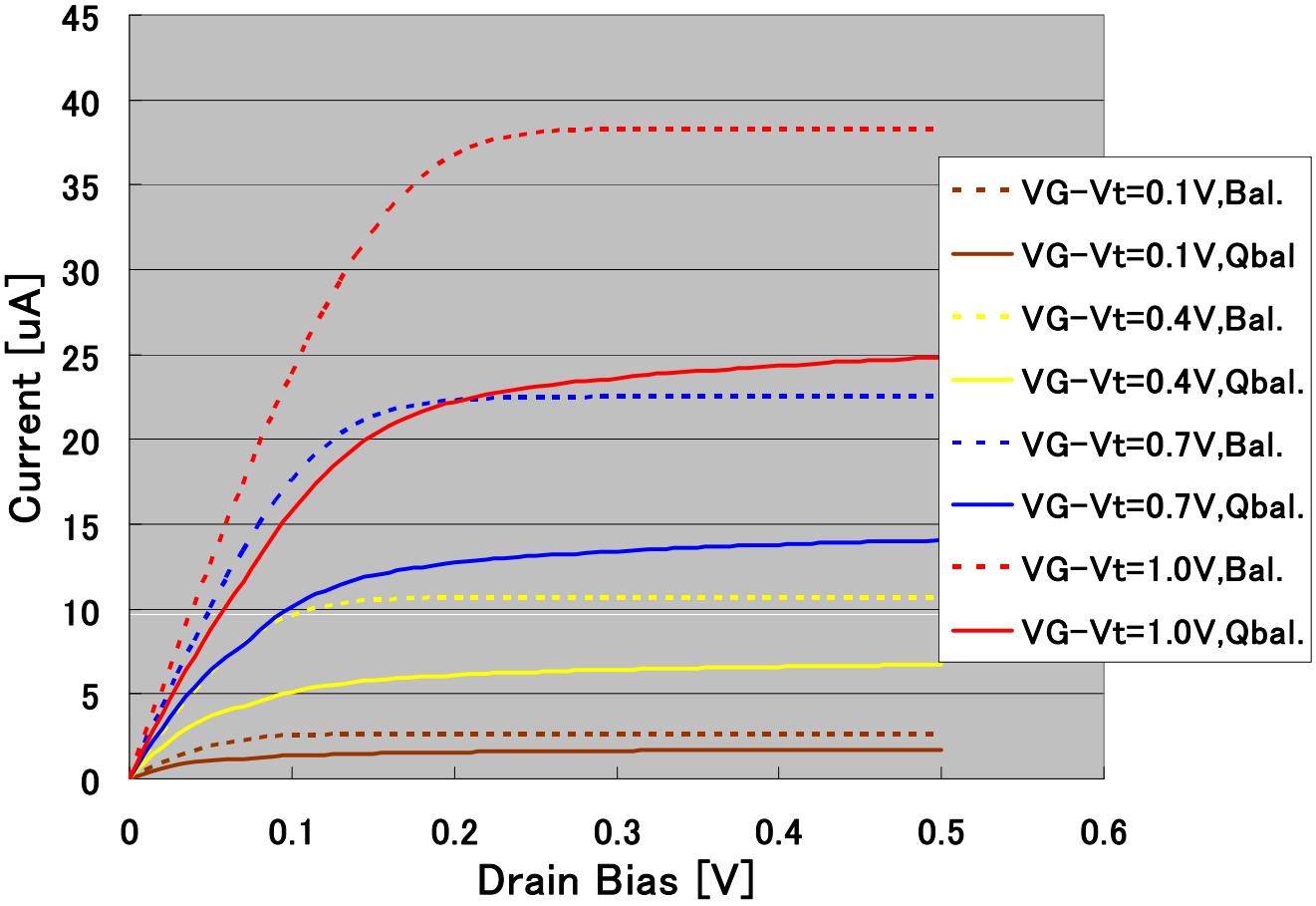
$$\left| Q_f + Q_b \right| = \frac{q}{\pi} \sum_i g_i \left[\int_{-\infty}^{\infty} \frac{dk}{1 + \exp\left\{ \dfrac{\varepsilon_i(k) - \mu_S}{k_B T} \right\}} - \int_{-\infty}^{0} \left\{ \frac{1}{1 + \exp\left\{ \dfrac{\varepsilon_i(k) - \mu_S}{k_B T} \right\}} - \frac{1}{1 + \exp\left\{ \dfrac{\varepsilon_i(k) - \mu_D}{k_B T} \right\}} \right\} T_i(\varepsilon_i(k)) dk \right]$$

$$T(\varepsilon) = \frac{\sqrt{2D_0} qE}{\left(\sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0} B_0 \ln\left(\dfrac{qEx_0 + \varepsilon}{\varepsilon} \right)}$$

(Carrier distribution in Subbands)

Unknowns are I_D, $(\mu_S - \mu_0)$, $(\mu_D - \mu_0)$, $(Q_f + Q_b)$

I-V_D Characteritics (RT)

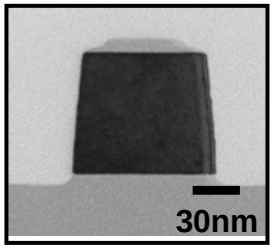


- Electric current 20～25 μA
- No satruration at Large V_D

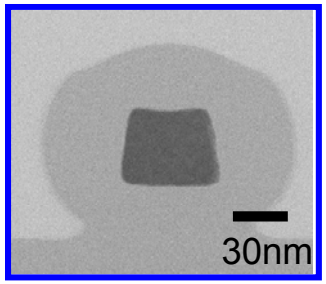
SiNW FET Fabrication

SiNW FET Fabrication

S/D & Fin Patterning

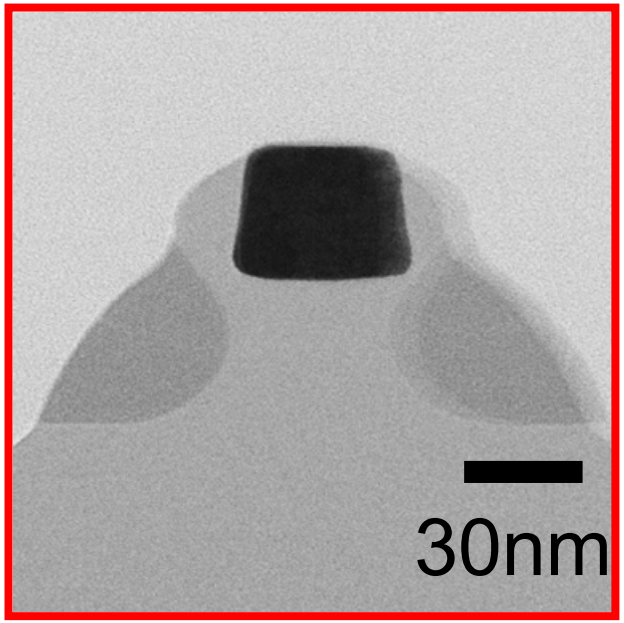


Sacrificial Oxidation



Oixde etch back

SiN sidewall support formation



Gate Oxidation & Poly-Si Deposition

Gate Lithography & RIE Etching

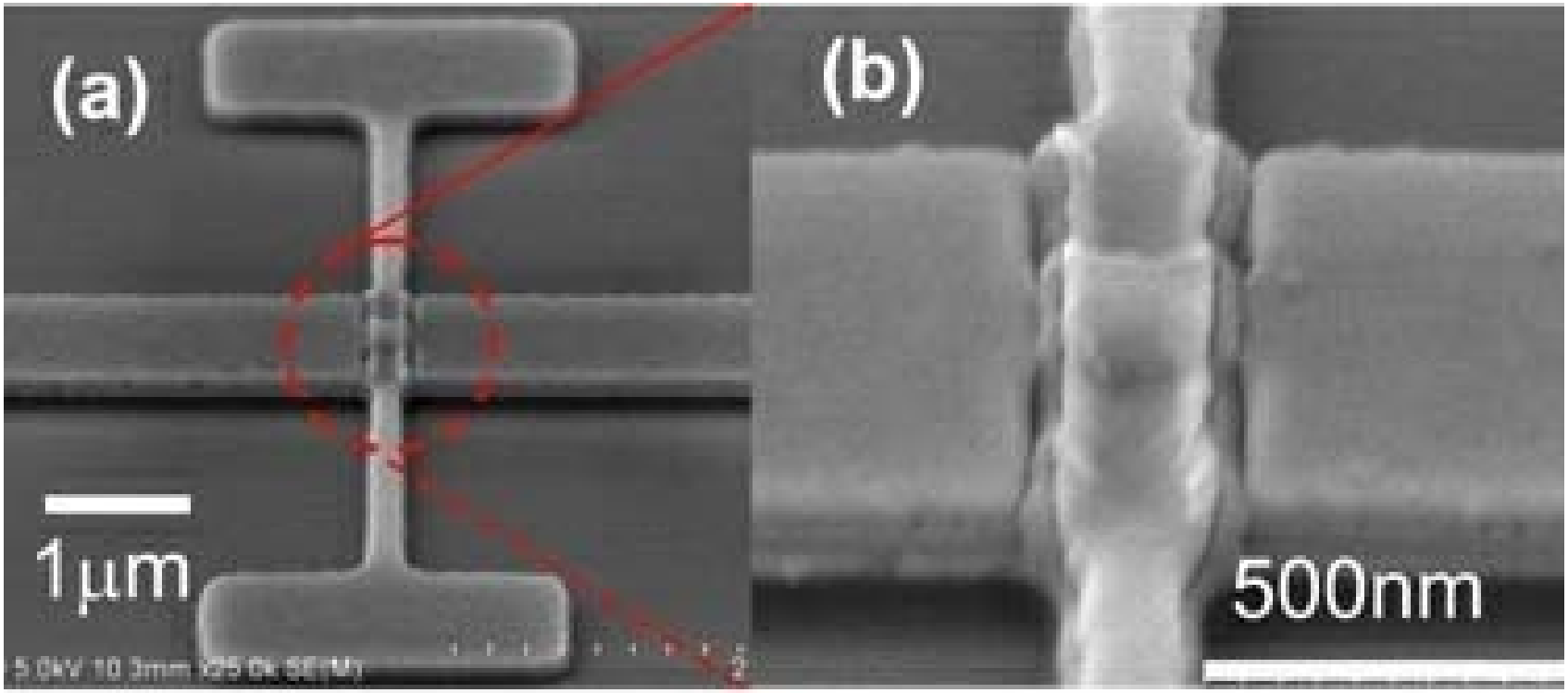
Gate Sidewall Formation

Ni SALISIDE Process (Ni 9nm / TiN 10nm)

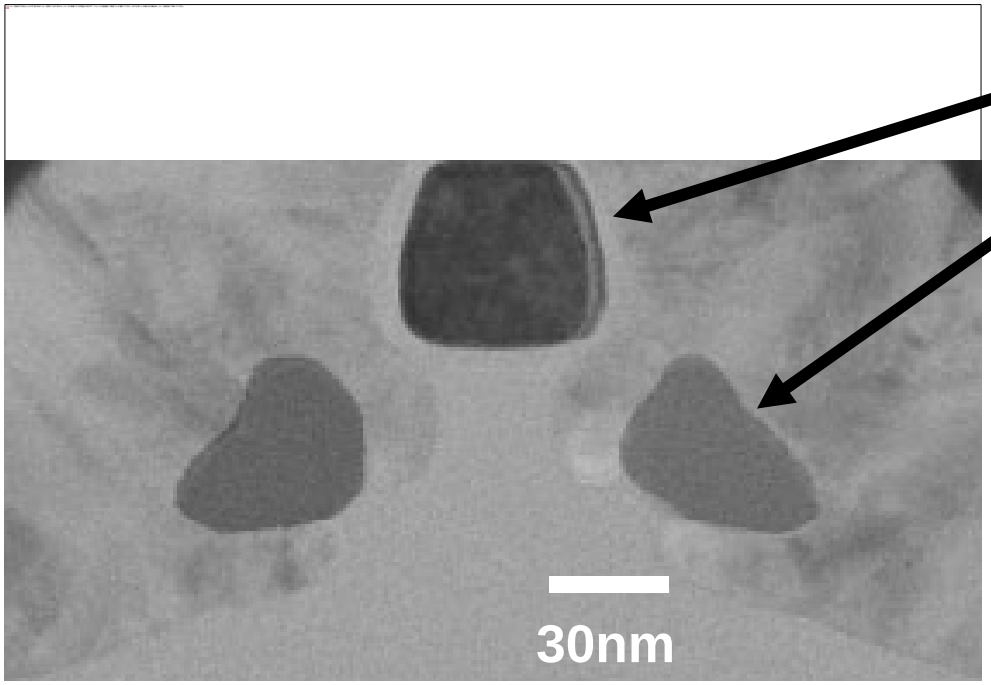
Backend

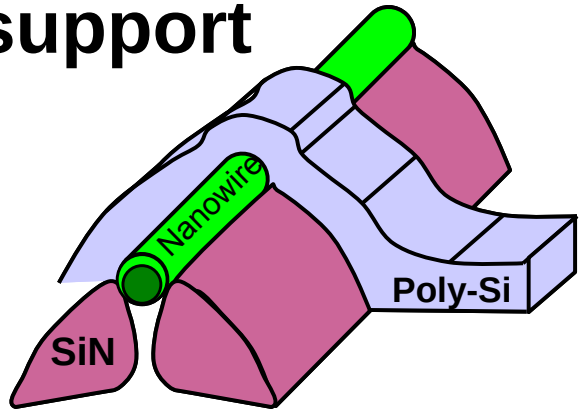
Standard recipe for gate stack formation

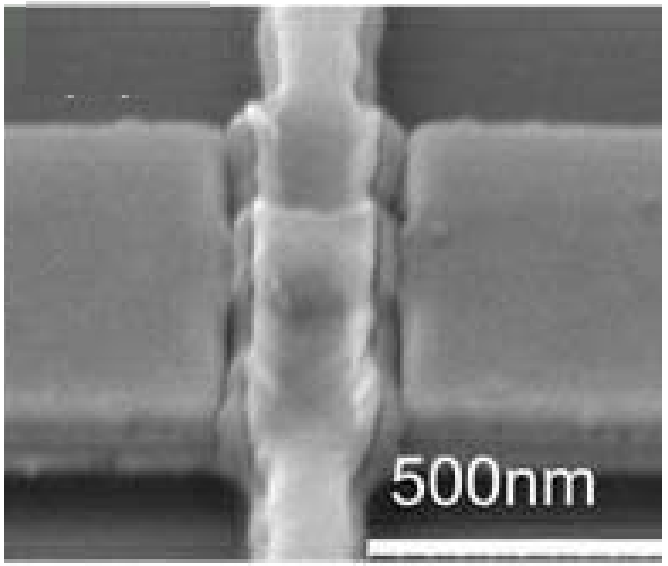
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.



Fabricated SiNW FET

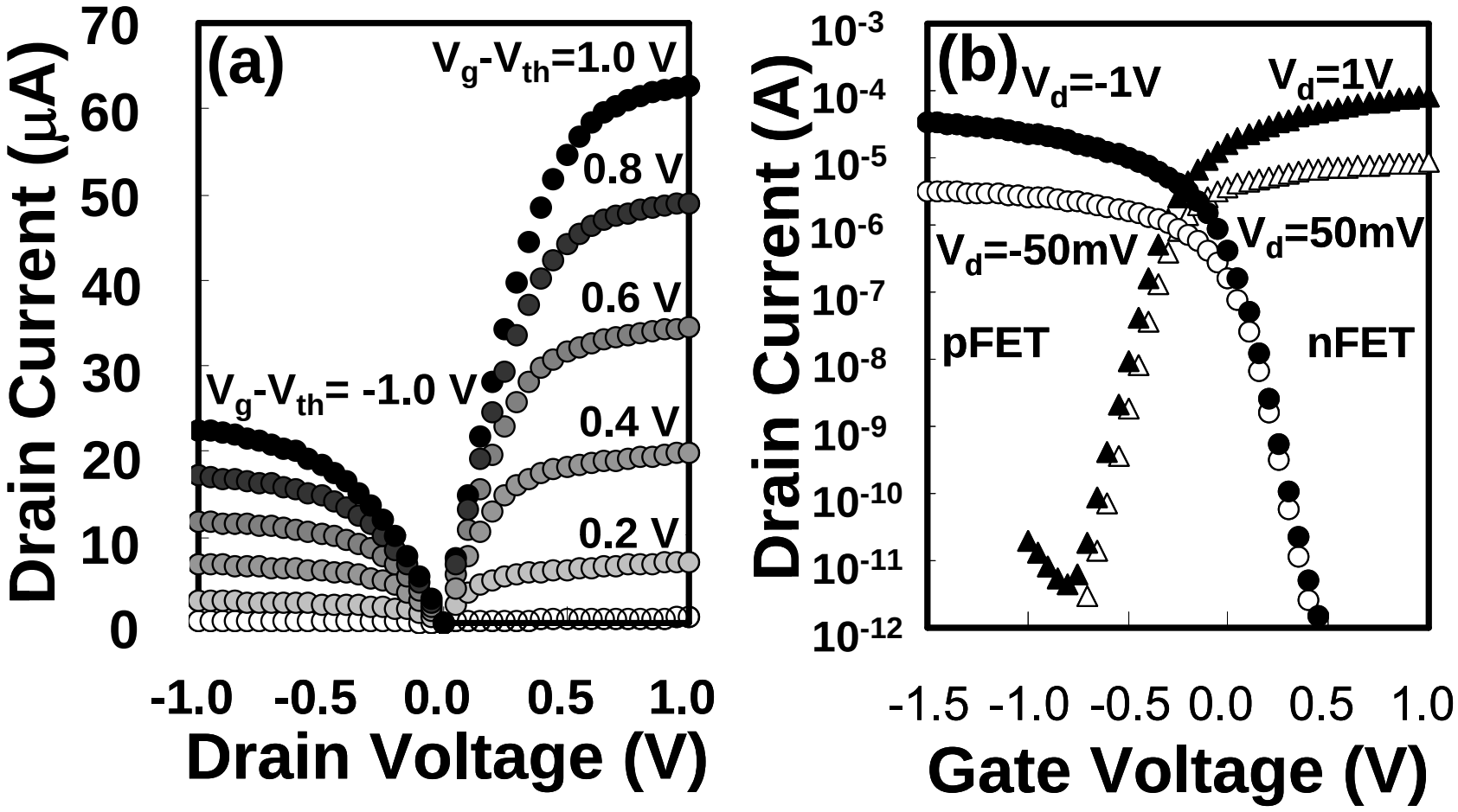






Recent results to be presented by ESSDERC 2010 next week in Sevile

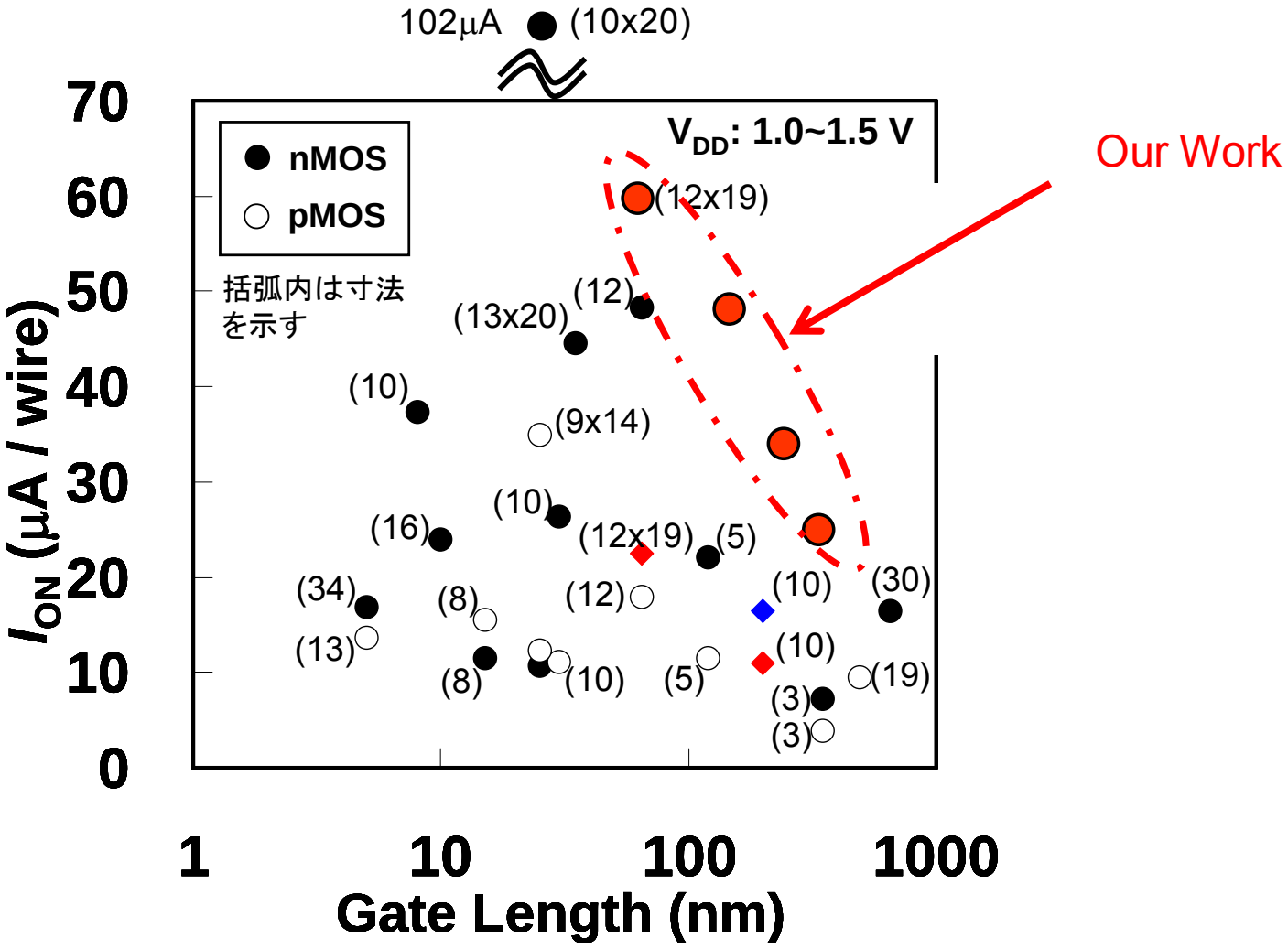
Wire cross-section: 20 nm X 10 nm



On/Off>10^6、60uA/wire

L_g=65nm, T_{ox}=3nm

Bench Mark

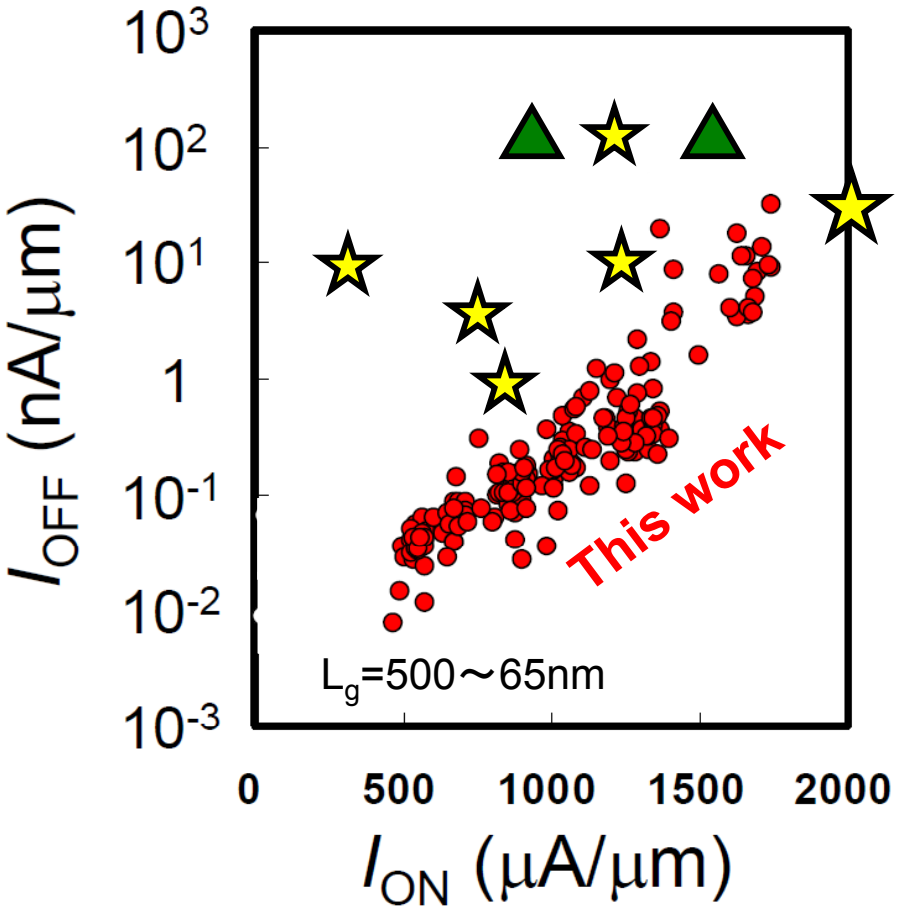

102μA
(10x20)
70
60
50
40
30
20
10
0
I_{ON} (μA / wire)
nMOS
pMOS
括弧内は寸法を示す
V_{DD}: 1.0~1.5 V
(12x19)
(12)
(13x20)
(10)
(9x14)
(10)
(16)
(12x19)
(5)
(34)
(8)
(12)
(10)
(30)
(13)
(10)
(8)
(10)
(5)
(19)
(3)
(3)
1
10
100
1000
Gate Length (nm)
Our Work

Bench Mark

	This work	Ref[11]	Ref[12]	Ref[13]	Ref[14]	Ref[15]	Ref[4]
NW Cross-section (nm)	Rect.	Rect.	Rect.	Cir.	Cir.	Elliptical	Elliptical
NW Size (nm)	10x20	10x20	14	10	10	12	13x20
Lg (nm)	65	25	100	30	8	65	35
EOT or Tox (nm)	3	1.8	1.8	2	4	3	1.5
Vdd (V)	1.0	1.1	1.2	1.0	1.2	1.2	1.0
Ion(uA) per wire	60.1	102	30.3	26.4	37.4	48.4	43.8
Ion(uA/um) by dia.	3117	5010	2170	2640	3740	4030	2592
Ion(uA/um) by cir.	1609	2054	430	841	1191	1283	825
SS (mV/dec.)	70	79	68	71	75	~75	85
DIBL (mV/V)	62	56	15	13	22	40-82	65
Ion/Ioff	~1E6	>1E6	>1E5	~1E6	>1E7	>1E7	~2E5

Ref[11] by Stmicro Lg=25nm,Tox=1.8nm
This work Lg=65nm,Tox=3nm

I_{ON}/I_{OFF} Bench mark

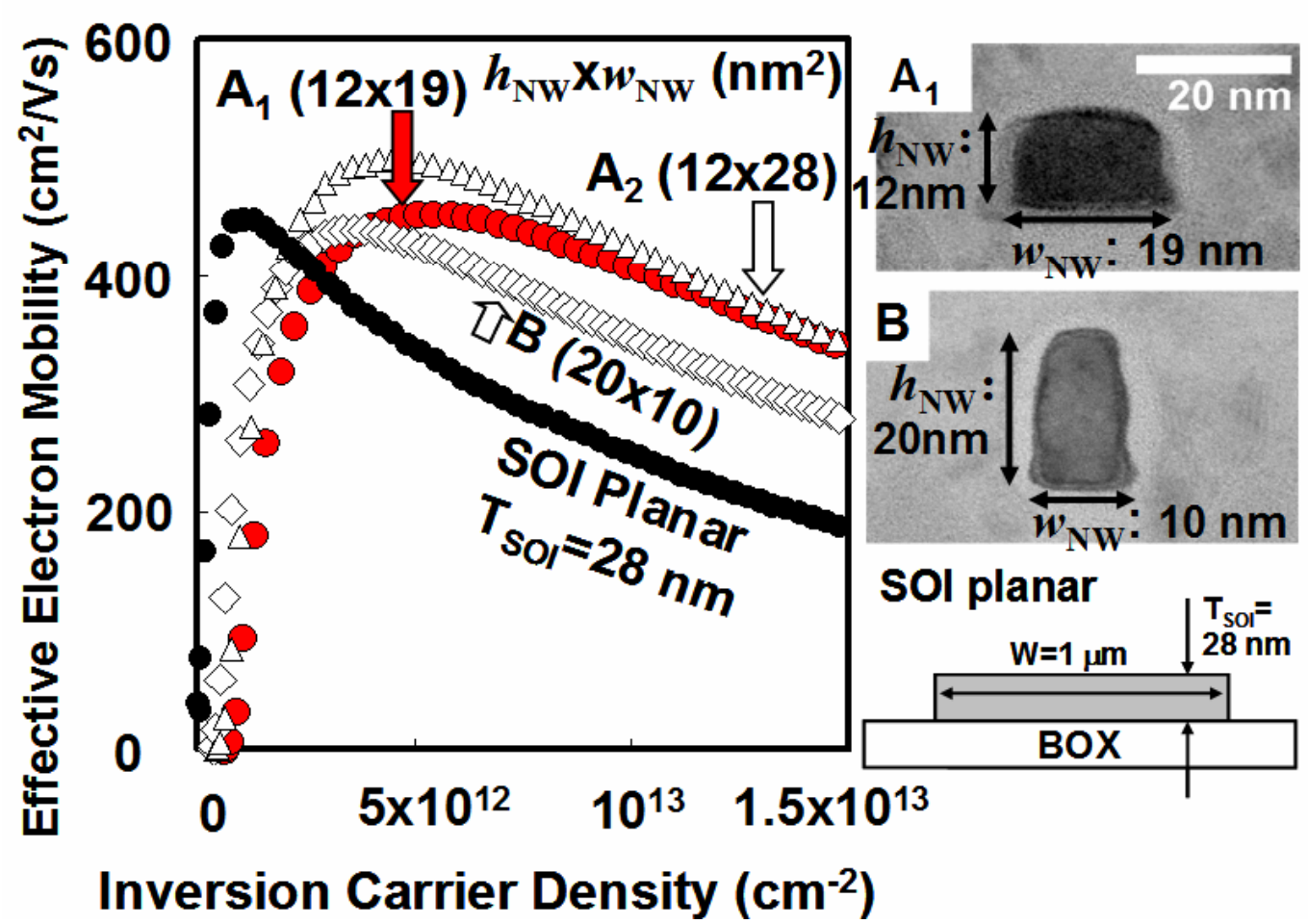


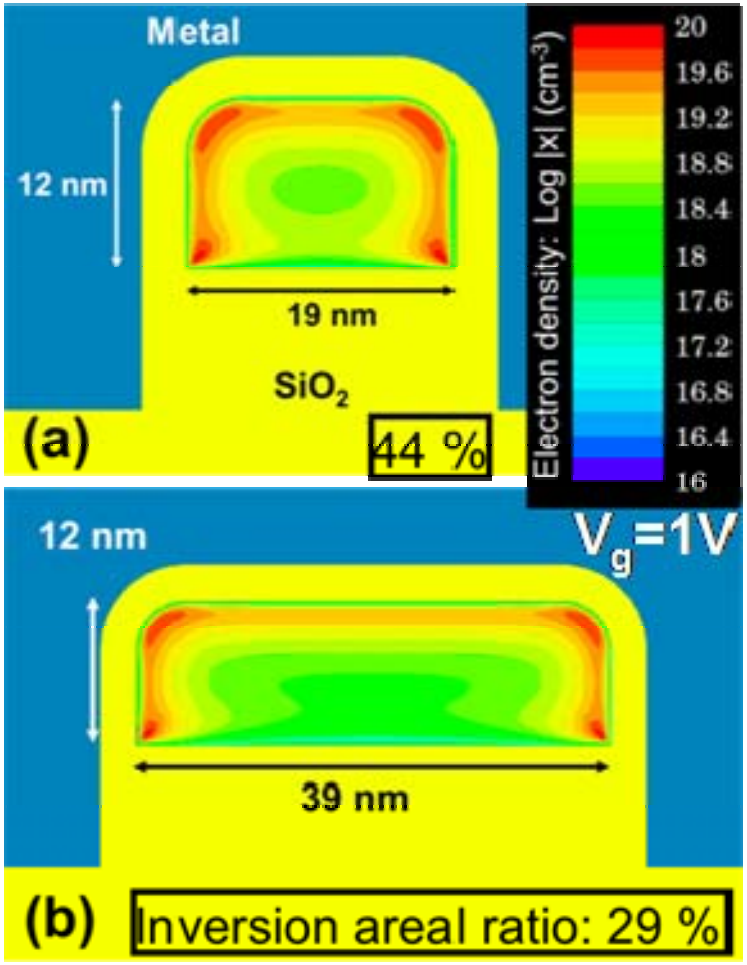
Planer FET ▲ 1.0～1.1V

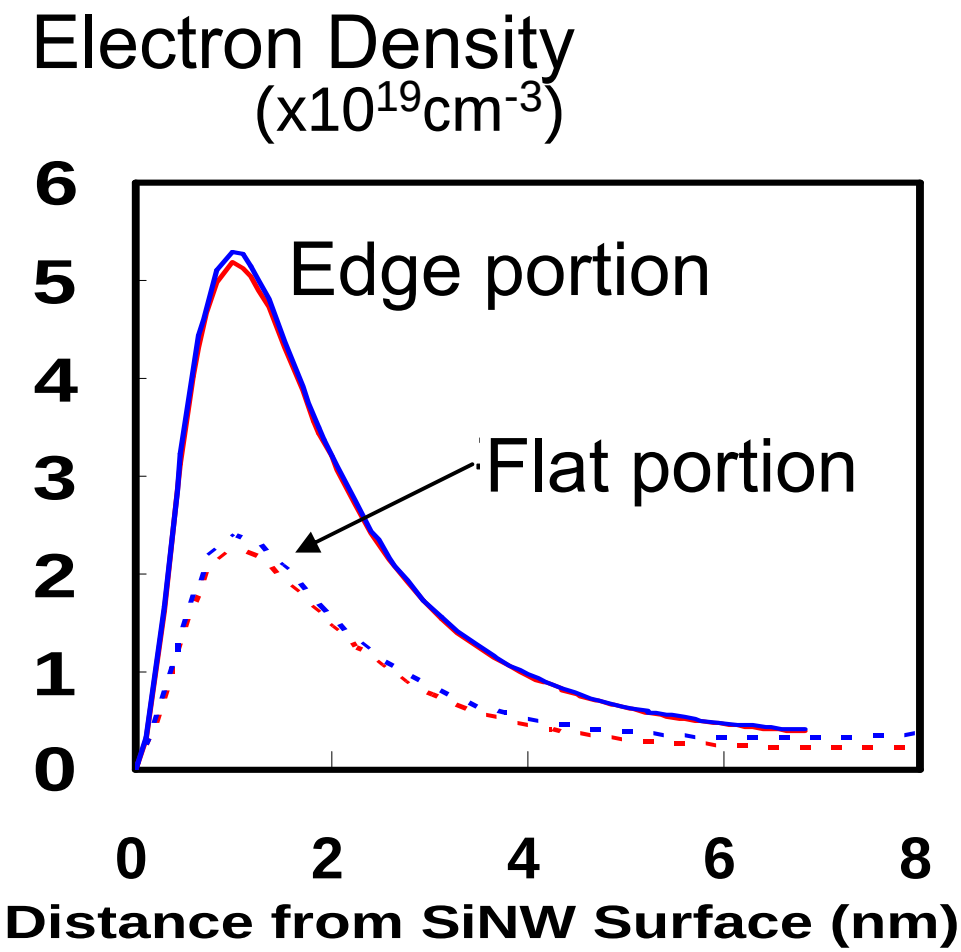
S. Kamiyama, IEDM 2009, p. 431
P. Packan, IEDM 2009, p.659

Siナノワイヤ FET ★ 1.2～1.3V

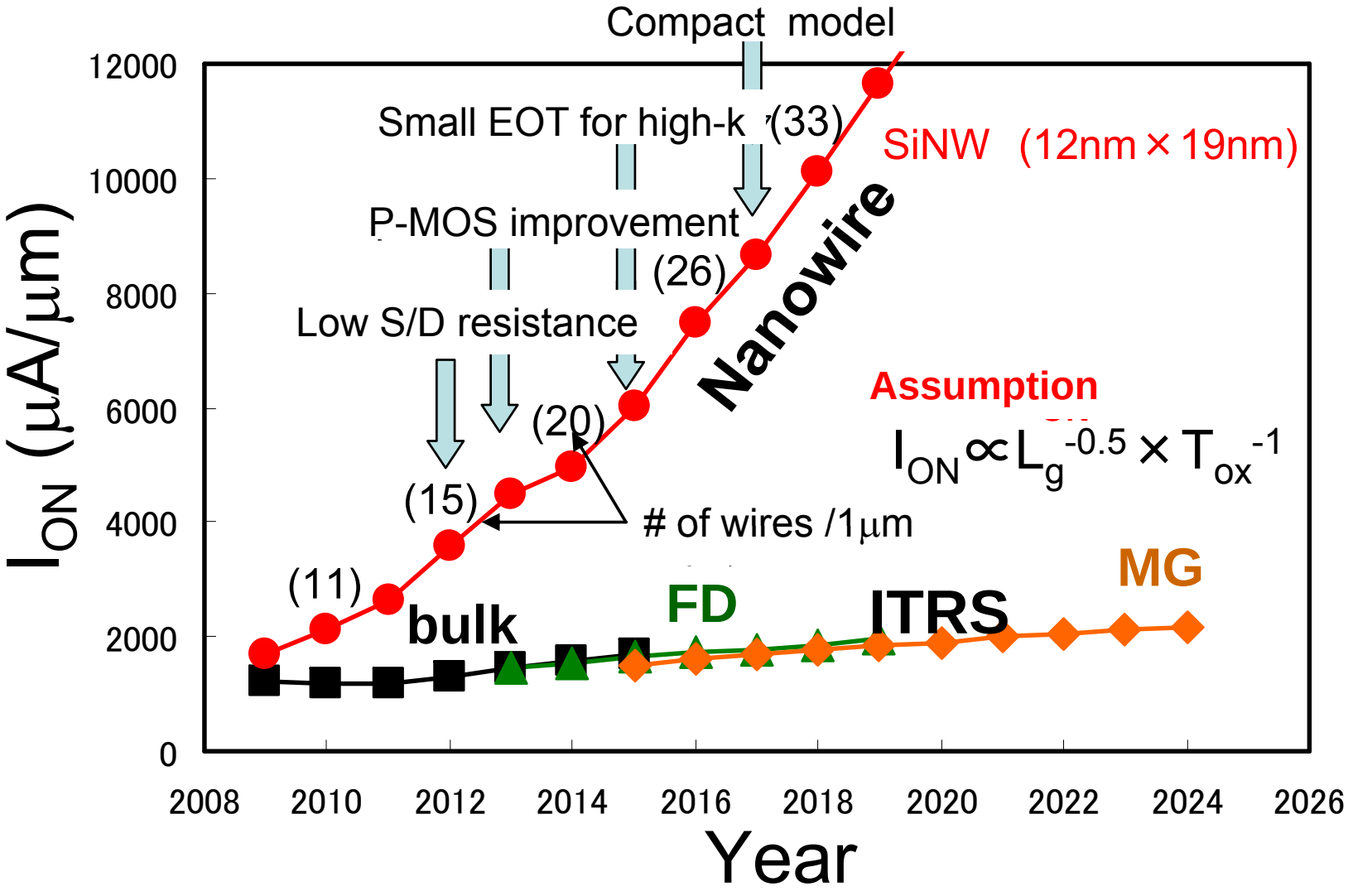
Y. Jiang, VLSI 2008, p.34
H.-S. Wong, VLSI 2009, p.92
S. Bangsaruntip, IEDM 2009, p.297
C. Dupre, IEDM 2008, p. 749
S.D.Suk, IEDM 2005, p.735
G.Bidel, VLSI 2009, p.240


Effective Electron Mobility (cm²/Vs)
600
400
200
0
0
5x10¹²
10¹³
1.5x10¹³
Inversion Carrier Density (cm⁻²)
A₁ (12x19) h_NW x w_NW (nm²)
A₂ (12x28)
B (20x10)
SOI Planar
T_SOI=28 nm
A₁
20 nm
h_NW: 12nm
w_NW: 19 nm
B
h_NW: 20nm
w_NW: 10 nm
SOI planar
T_SOI= 28 nm
W=1 μm
BOX


Metal
12 nm
19 nm
SiO2
(a)
44 %
Electron density: Log |x| (cm-3)
20
19.6
19.2
18.8
18.4
18
17.6
17.2
16.8
16.4
16
12 nm
Vg=1V
39 nm
(b)
Inversion areal ratio: 29 %

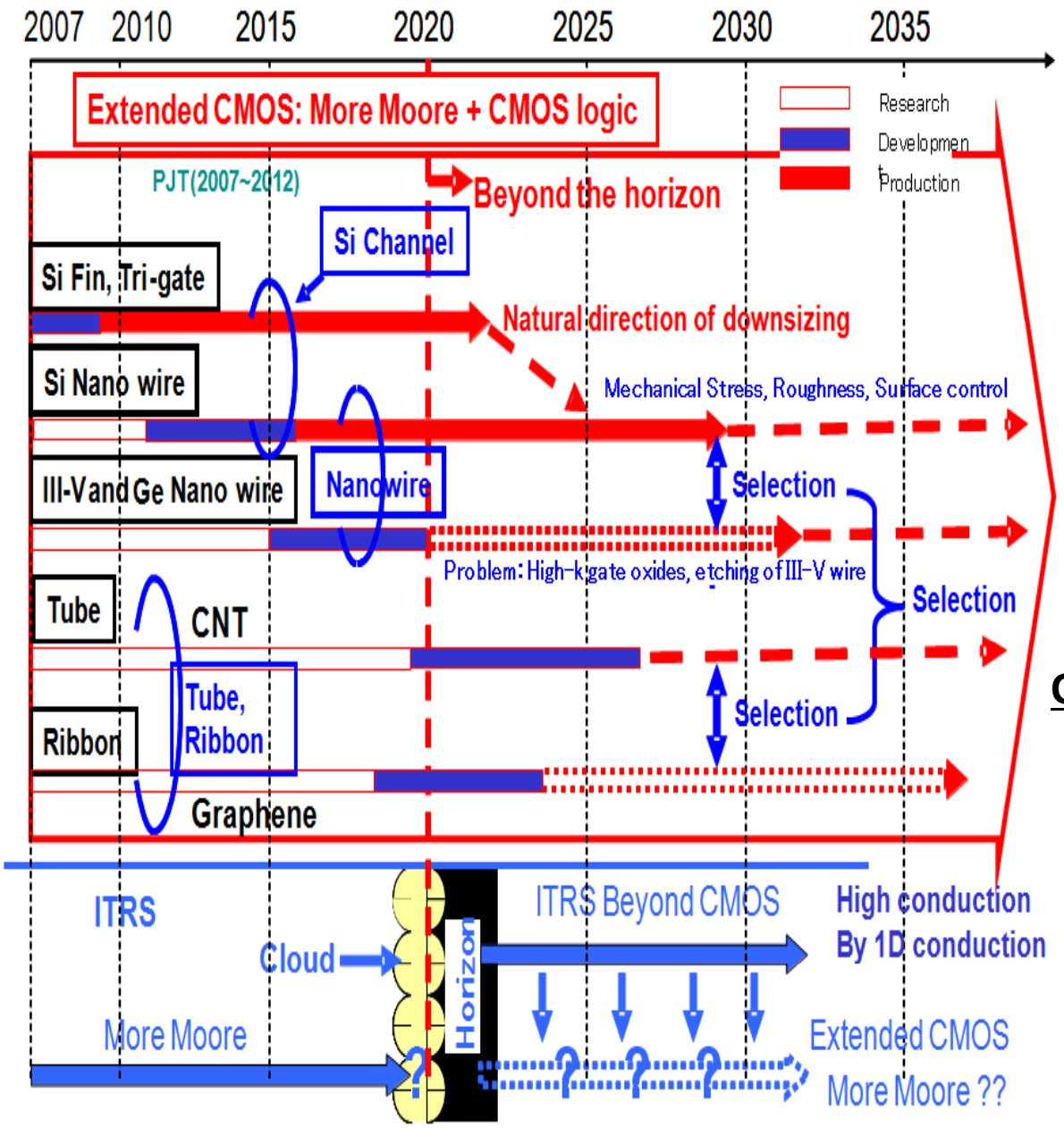

Electron Density
(x10^19cm^-3)
6
5
4
3
2
1
0
Edge portion
Flat portion
0
2
4
6
8
Distance from SiNW Surface (nm)

Primitive estimation !



Our roadmap for R &D

Source: H. Iwai, IWJT 2008



Current Issues

Si Nanowire

Control of wire surface property

Source Drain contact

Optimization of wire diameter

Compact I-V model

III-V & Ge Nanowire

High-k gate insulator

Wire formation technique

CNT:

Growth and integration of CNT

Width and Chirality control

Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique

Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

Acknowledgement

This work was supported by
METI and NEDO, Japan.

Fabrication of Si-nanowire FETs
Were supported by Selete.

Some simulator of Si-nanowire FETs
were done by using Selete T-CAD
simulator tool.

Thank you for your attention