Nanoelectronic Device Technology
-- Future perspective for the mainstream CMOS technology --

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Frontier Research Center
Tokyo Institute of Technology, Yokohama, Japan

Hiroshi Iwai

1. Back ground

Japanese government announced 25% reduction of greenhouse gas in 2020 compared with 1990

Rapid growth of energy consumed by IT
→ Reaching 10 % of Total Energy of our human society

Innovation in Integrated circuits technology will contribute to the cool earth significantly.

Cool Earth by IT or integrated circuits

Green by IT

1.By controlling the system by microprocessor (Integrated Circuits) more efficiently, energy consumption of the system will be significantly reduced.

Every human system ：transportation system, manufacturing, Office

Green of IT

2.Power saving of Integrated Circuits in IT network （Server, Data Center, Router）

First Computer Eniac: made of huge number of vacuum tubes 1946

Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

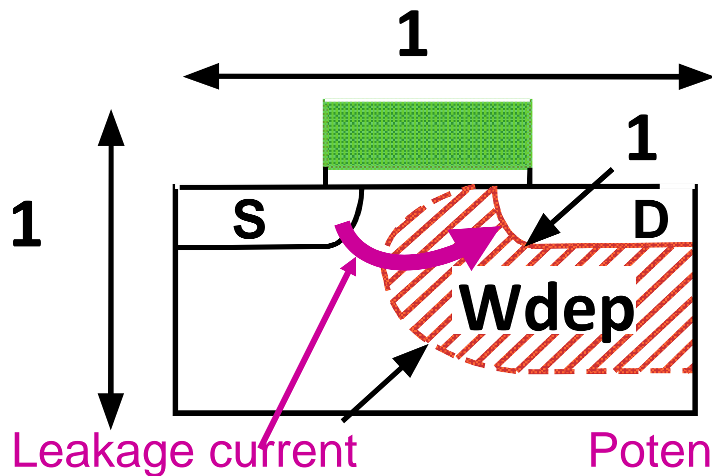
Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

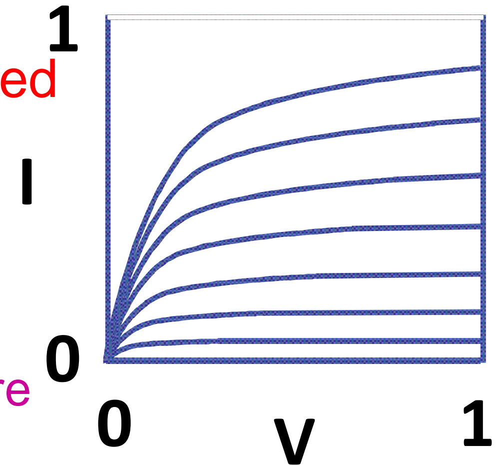
In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

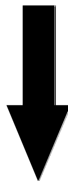
Wdep has to be suppressed
Otherwise, large leakage between S and D



Leakage current

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

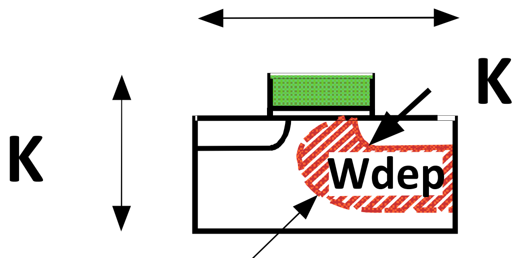
K=0.7 for example



X , Y , Z : K, V : K, Na : 1/K

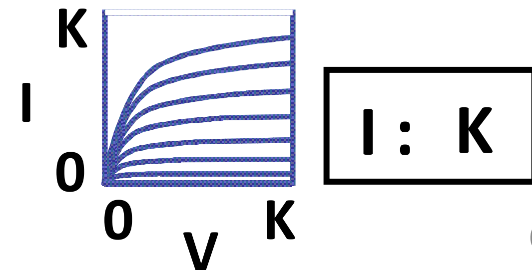
By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$\mathrm{Wdep} \propto \sqrt{V/Na}$$

: K



I : K

Downscaling merit: Beautiful!

Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	**Scaling K : K=0.7 for example**
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o: gate C per unit area $\rightarrow W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox} \rightarrow KK/K = K$
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d \rightarrow KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α: Scaling factor $\rightarrow$ **In the past, $\alpha > 1$ for most cases**
Integration (# of Tr)	N	α/K^2	$N \rightarrow \alpha/K^2$ **$= 1/K^2$, when $\alpha = 1$**
Power per chip	P	α	$fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2}) K (K^1)^2 = \alpha$ **= 1, when $\alpha = 1$**

k= 0.7 and α =1	k= 0.7^2 =0.5 and α =1
Single MOFET Vdd → 0.7 Lg → 0.7 Id → 0.7 Cg → 0.7 P (Power)/Clock → $0.7^3 = 0.34$ τ (Switching time) → 0.7	Vdd → 0.5 Lg → 0.5 Id → 0.5 Cg → 0.5 P (Power)/Clock → $0.5^3 = 0.125$ τ (Switching time) → 0.5
Chip N (# of Tr) → $1/0.7^2 = 2$ f (Clock) → 1/0.7 = 1.4 P (Power) → 1	N (# of Tr) → $1/0.5^2 = 4$ f (Clock) → 1/0.5 = 2 P (Power) → 1

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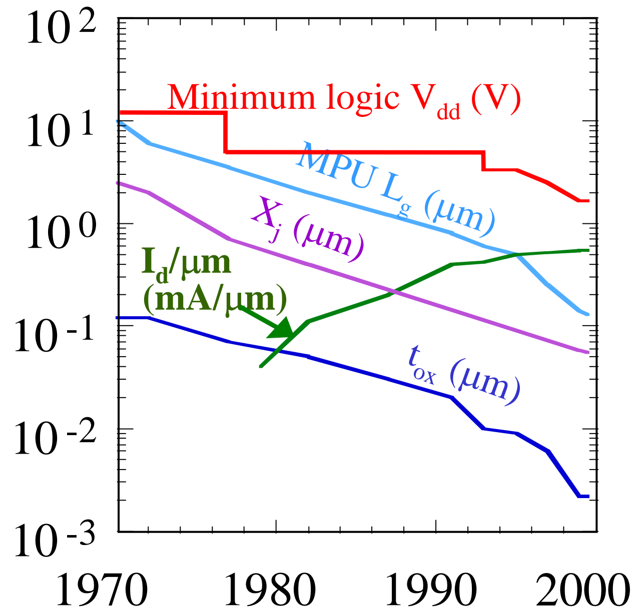
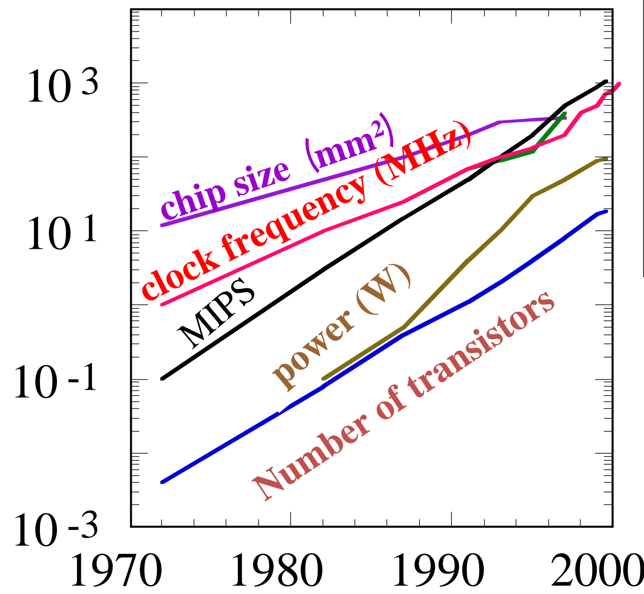
Actual past downscaling trend until year 2000





Past 30 years scaling

Merit: N, f increase

Demerit: P increase

V_{dd} scaling insufficient

⇩

Additional significant increase in I_d, f, P

Source. Iwai and S. Ohmi, Microelectronics Reliability 42 (2002), pp.1251-1268

Change in 30 years

	Ideal scaling	Real Change
L_g	K	10^{-2}
t_{ox}	$K(10^{-2})$	10^{-2}
V_{dd}	$K(10^{-2})$	10^{-1}
A_{chip}	α	10^{1}

	Ideal scaling	Real Change
I_d	$K(10^{-2})$	10^{-1}
$I_d/\mu m$	1	10^{1}
N	$\alpha/K^2(10^{5})$	10^{4}

	Ideal scaling	Real Change
f	$1/K(10^{2})$	10^{3}
P $= f\alpha NCV^2$	$\alpha(10^{1})$	10^{5}

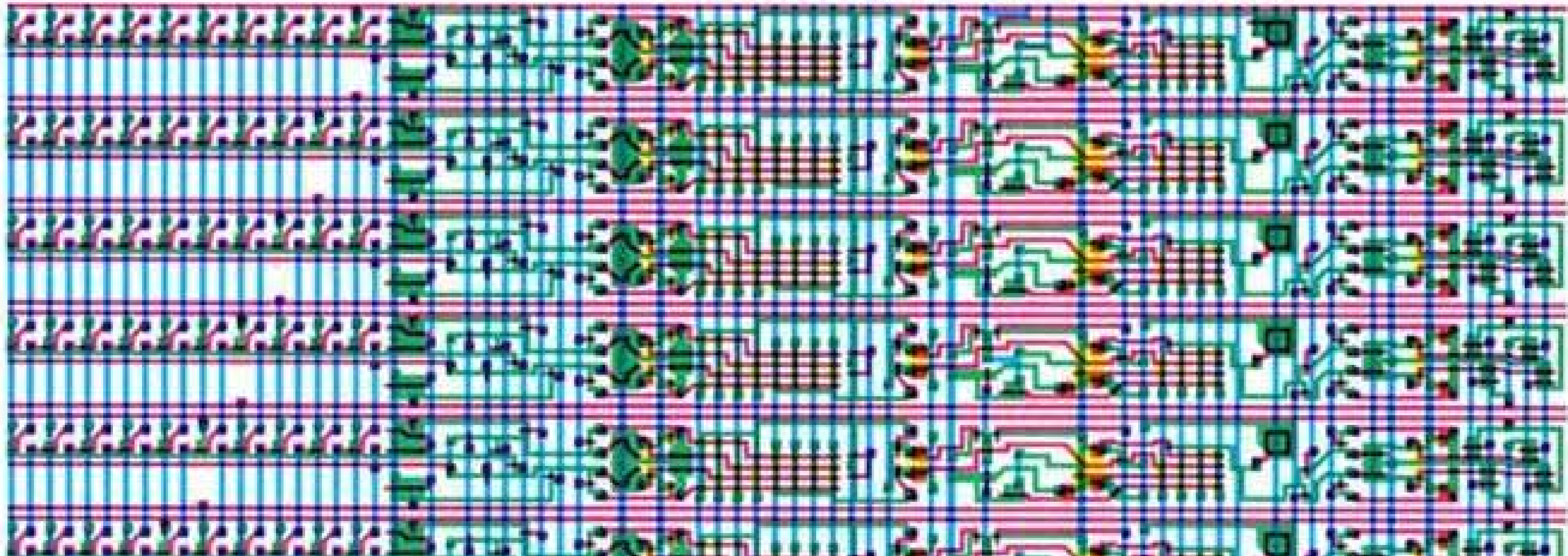
Vd scaling insufficient, α increased → N, Id, f, P increased significantly

Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

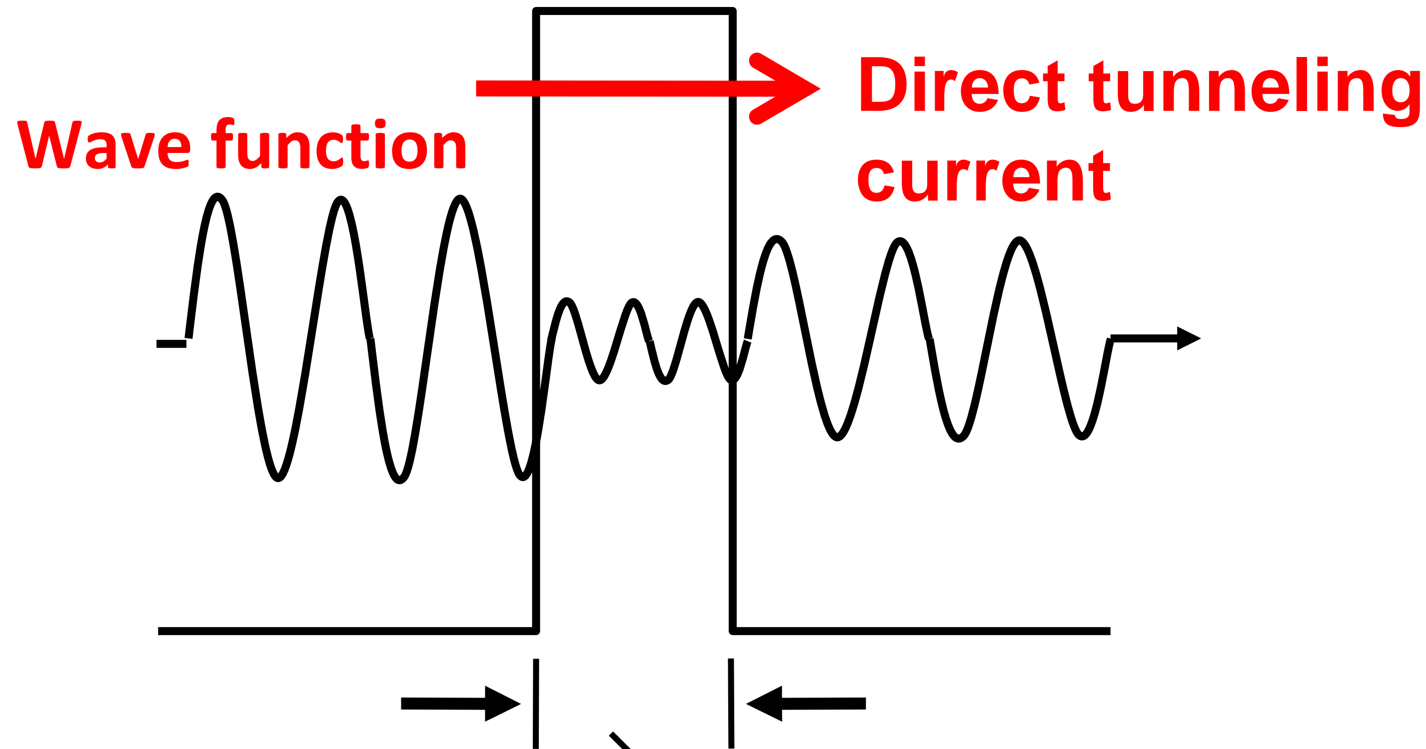
VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.

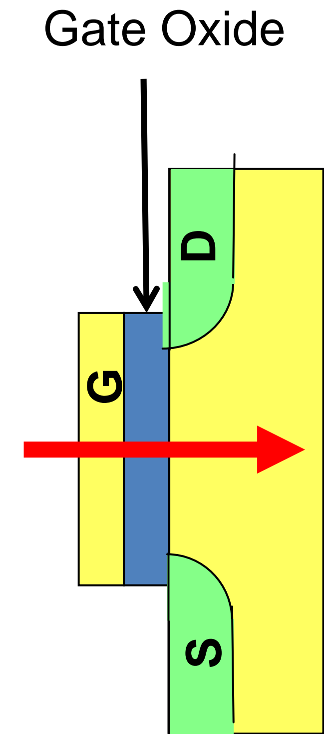


VLSI textbook

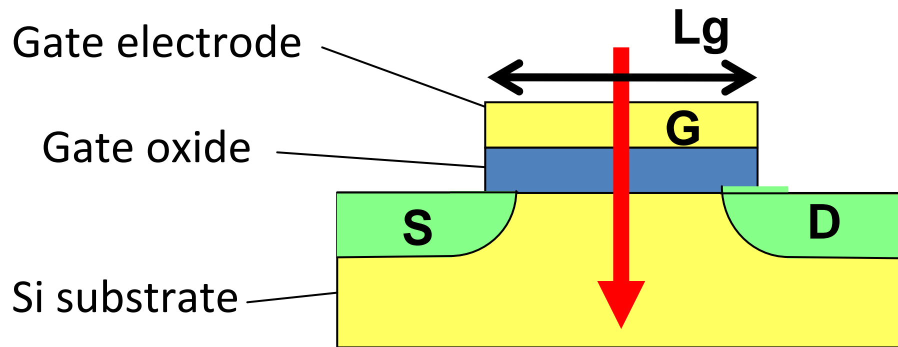
Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.

Direct-tunneling effect



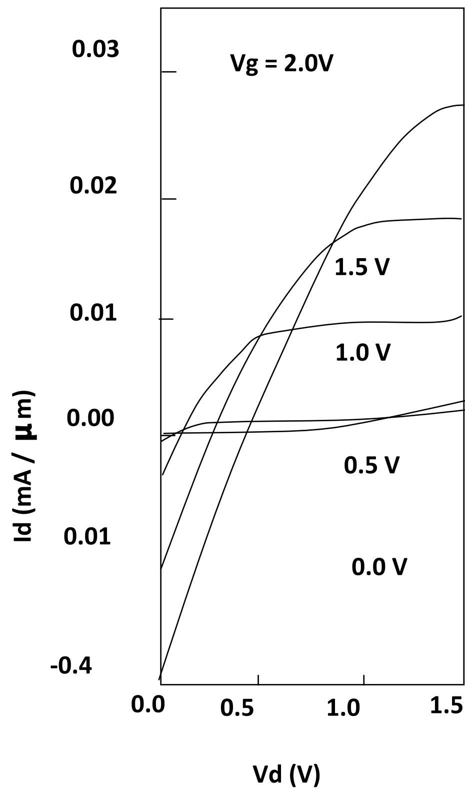


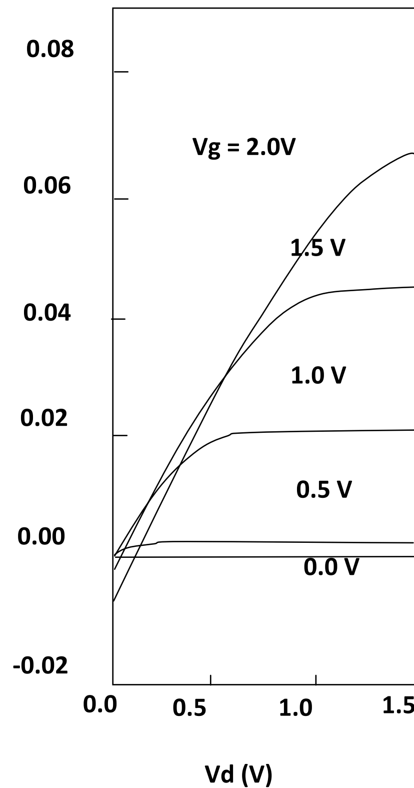
Direct tunneling leakage current start to flow when the thickness is 3 nm.

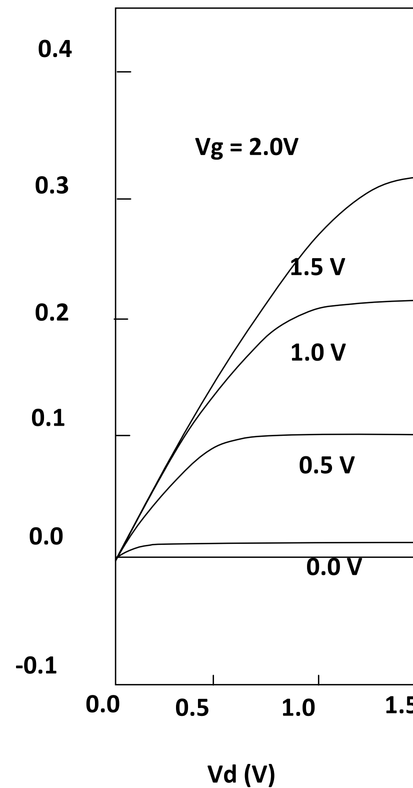


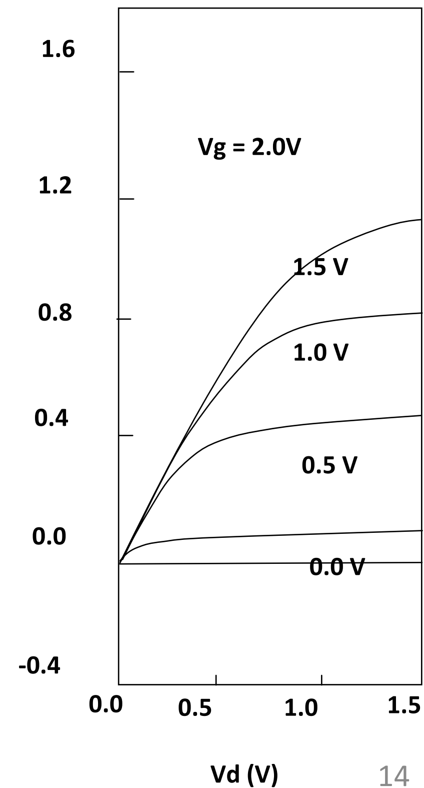
Direct tunneling leakage was found to be OK! In 1994!

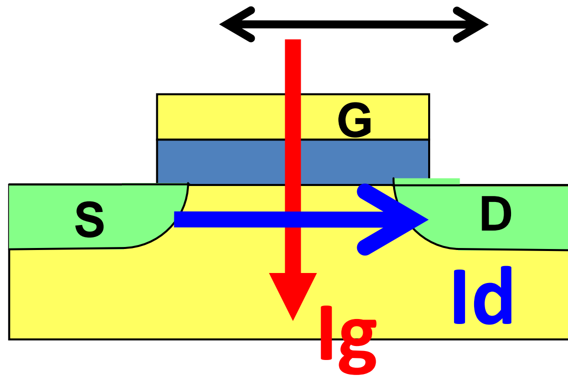
MOSFETs with 1.5 nm gate oxide











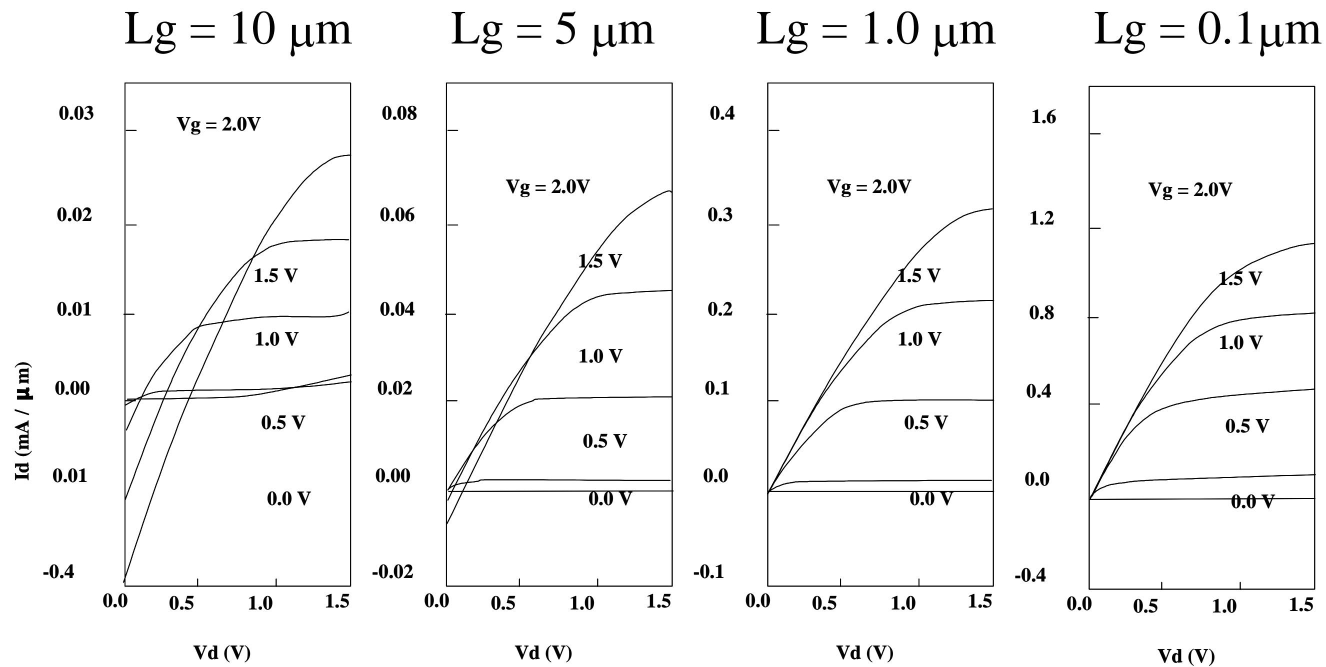
Gate leakage: Ig ∝ Gate Area ∝ Gate length (Lg)

Drain current: Id ∝ 1/Gate length (Lg)

Lg → small,

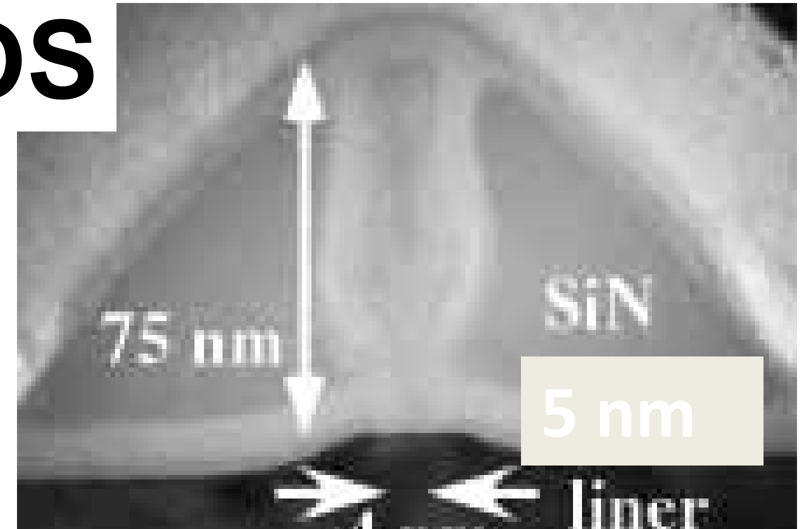
Then, Ig → small, Id → large, Thus, Ig/Id → very small

Id

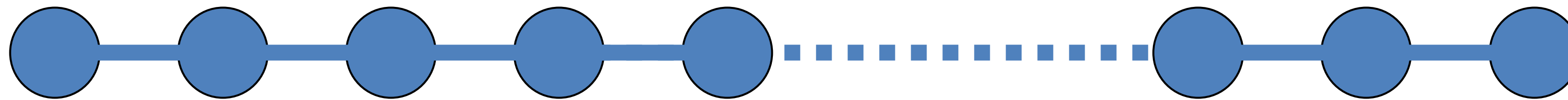


5 nm gate length CMOS

Is a Real Nano Device!!

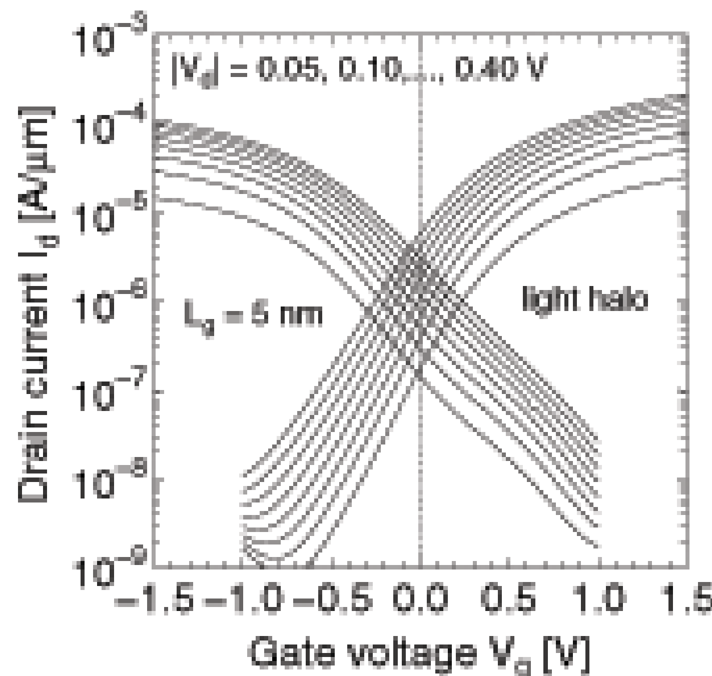


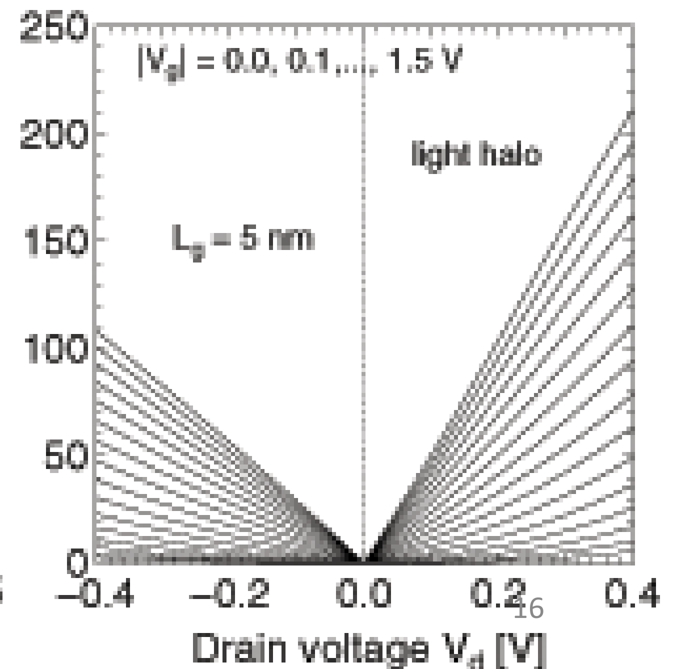
Length of 18 Si atoms



H. Wakabayashi et.al, NEC

IEDM, 2003

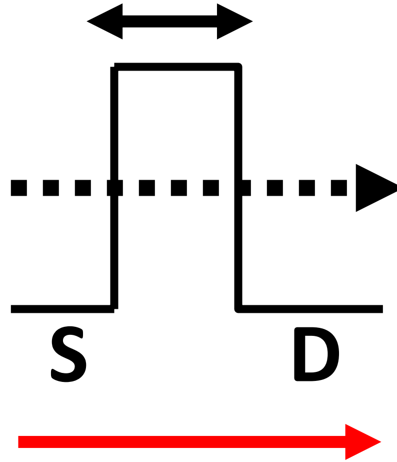




Predicted limit now

Tunneling distance

3 nm



MOSFET operation

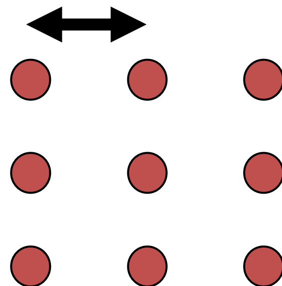
Lg = 3 nm?

Below this, no one knows future!

Ultimate Limit

Atom distance

0.3 nm



ITRS expect Lg less than 10nm

2009 ITRS Technology Trend: MPU gate length

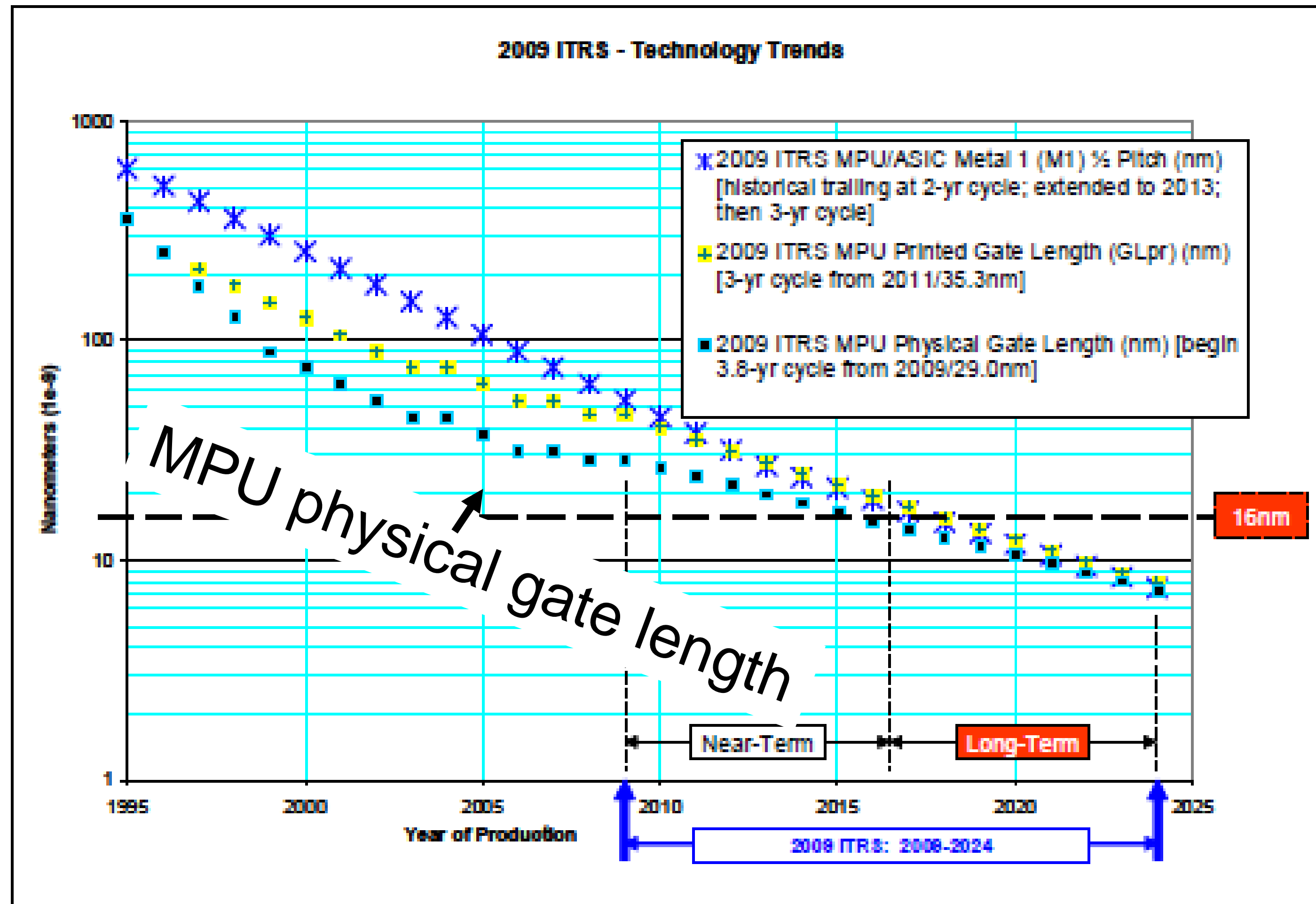
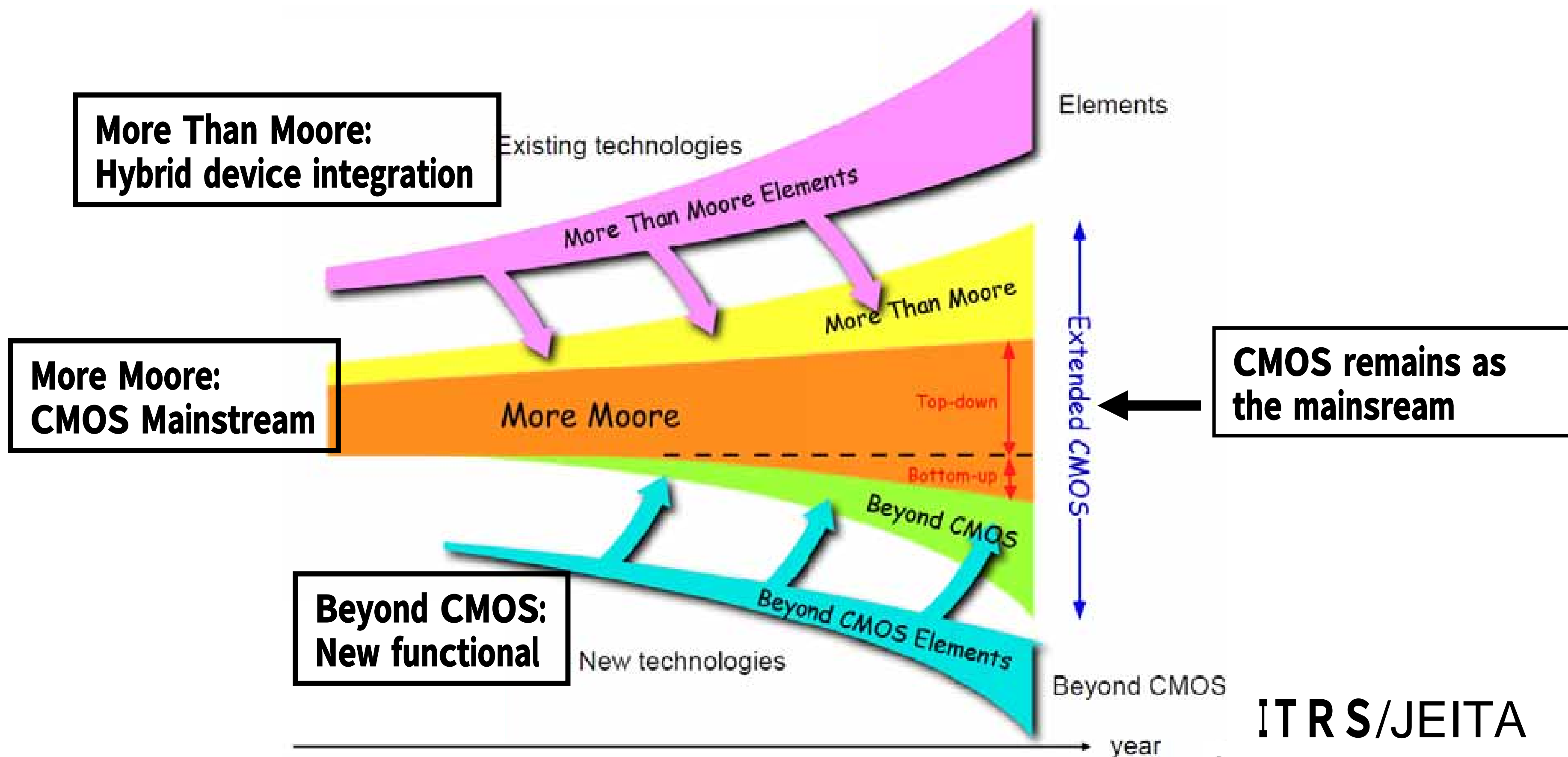


Figure 8b 2009 ITRS—MPU/high-performance ASIC Half Pitch and Gate Length Trends

CMOS scaling is the mainstream



How far can we go?

Past

0.7 times per 3 years

In 40 years: 15 generations,
Size 1/200, Area 1/40,000

1973年

Now

8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm

→ 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm

Future

→ 32nm → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

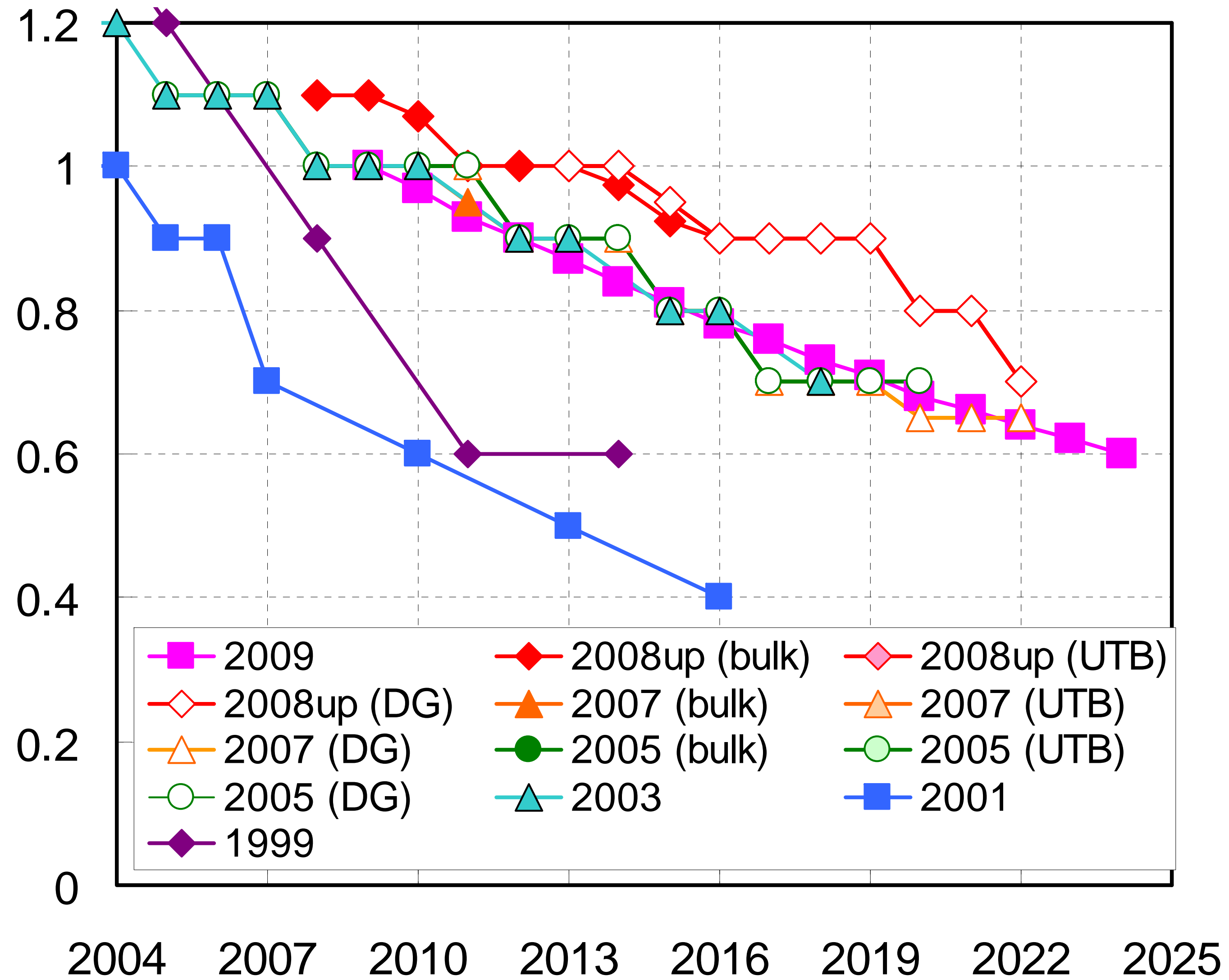
- At least 5,6 generations, for 15 ~ 20 years
- Hopefully 8 generations, for 30 years

3 important items for *More* Moore

1. Scaling of high-k beyond 0.5 nm
2. Metal/Silicide S/D
3. Si-Nanowire FET

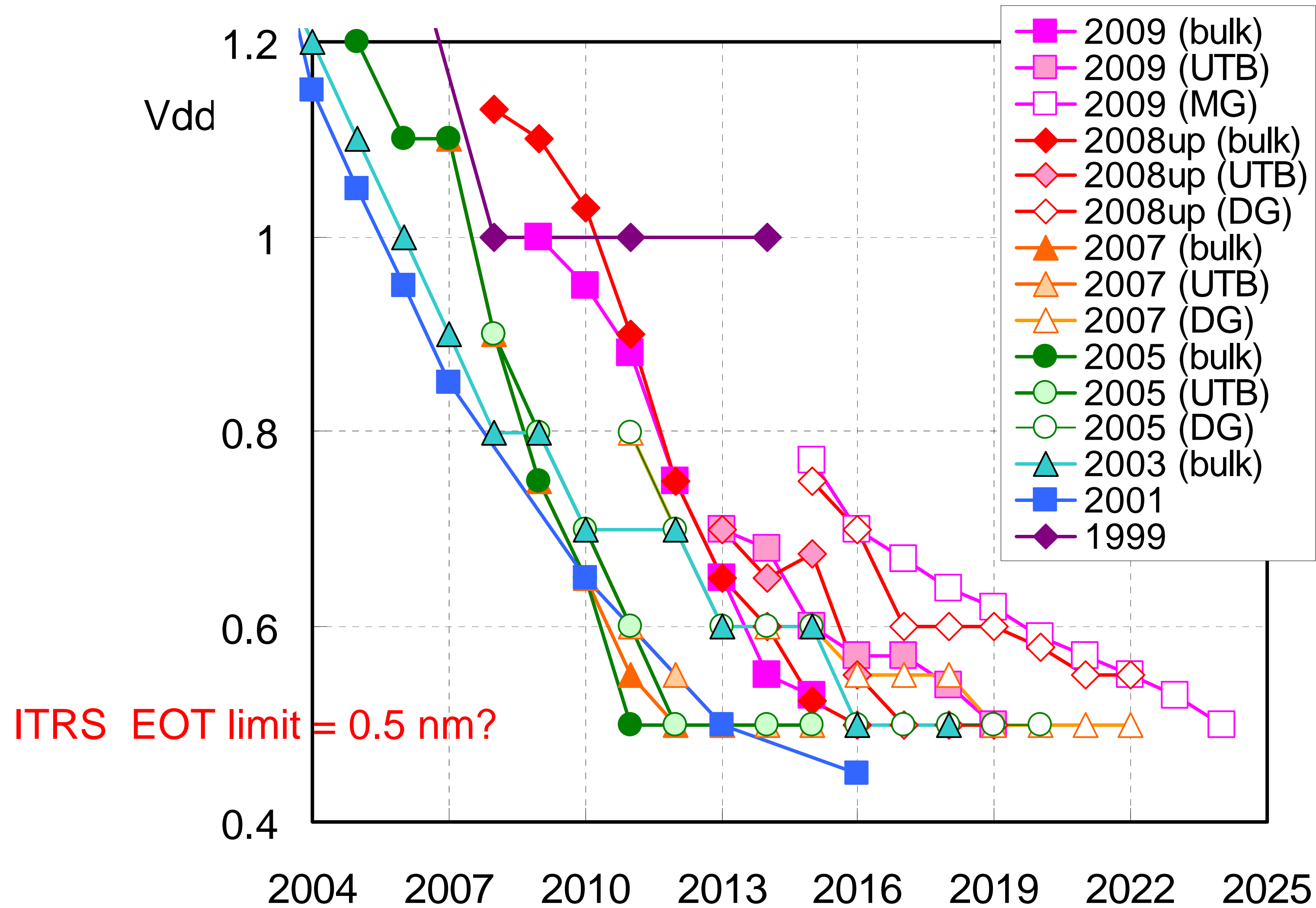
Vdd stay high

ITRS

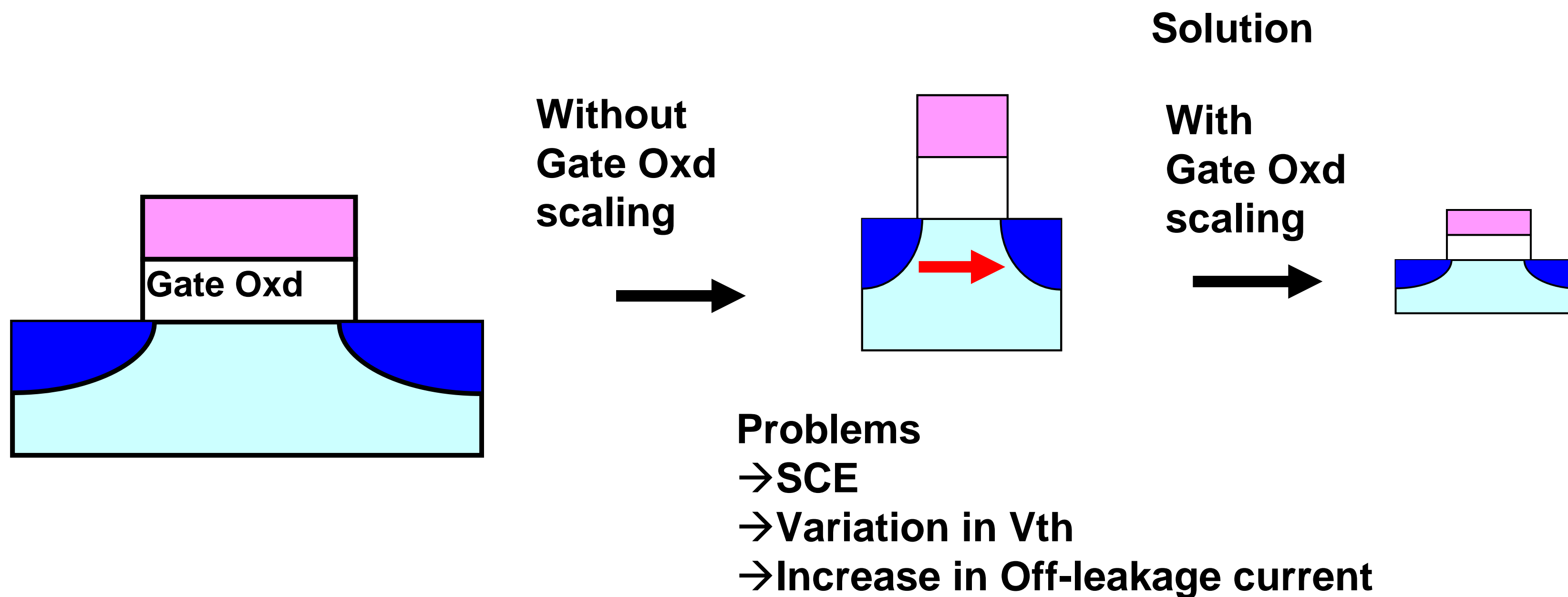


ITRS

EOT (Equivalent oxide thickness of gate insulator)



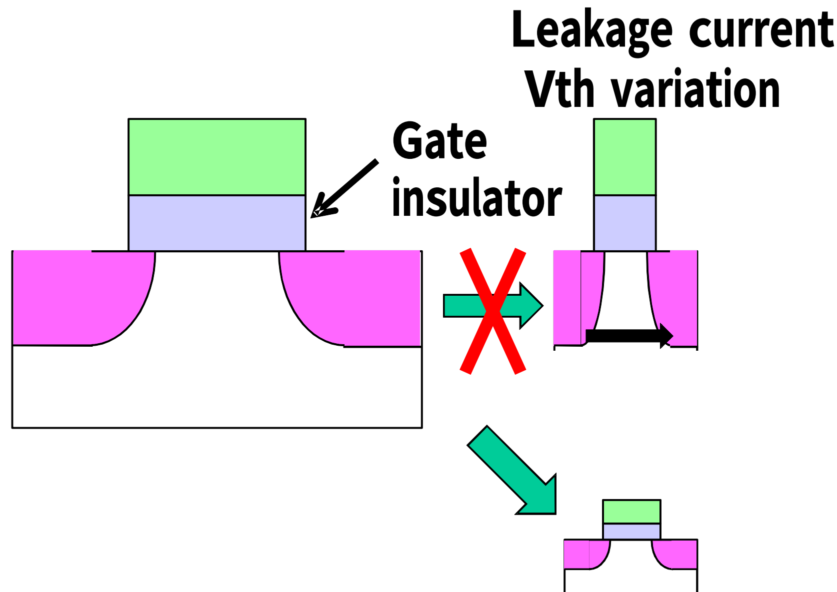
Scaling of high beyond 0.5 nm is important



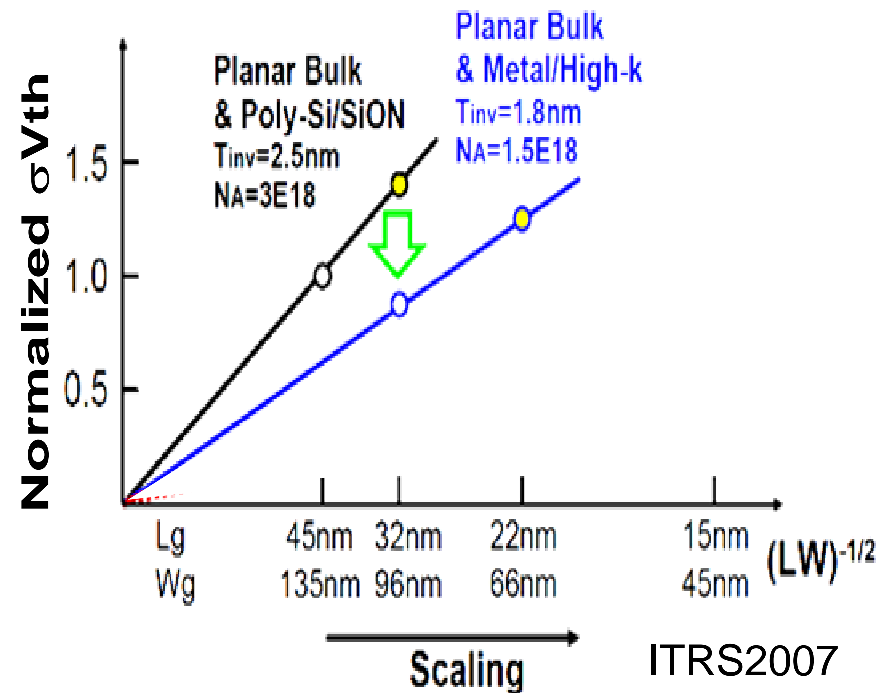
Power of Transistor $= CV^2/2 \propto D^3\ (=L^3)$

D：Size, L：Gate length

Scaling approach is very important

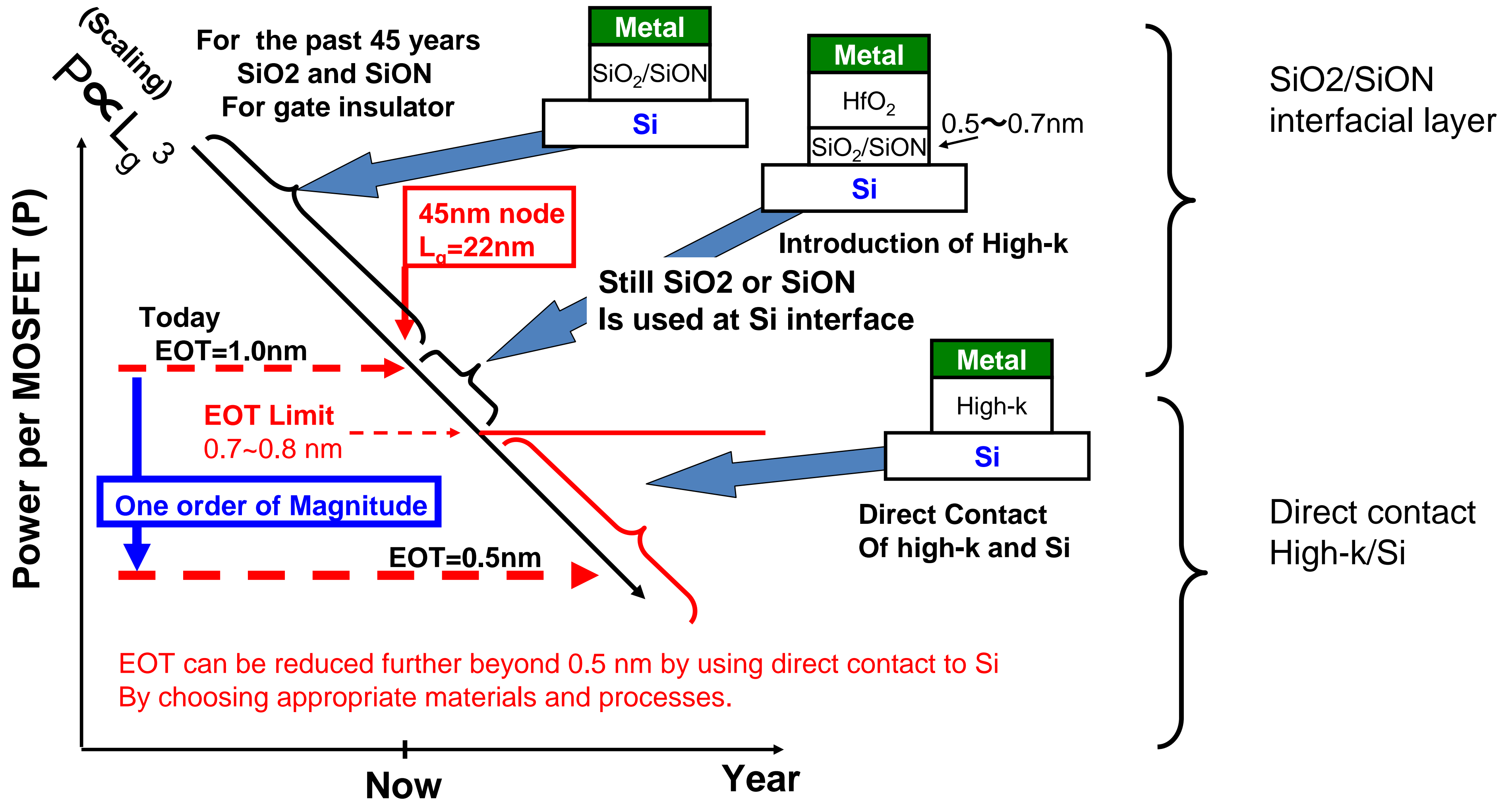


Vth variation

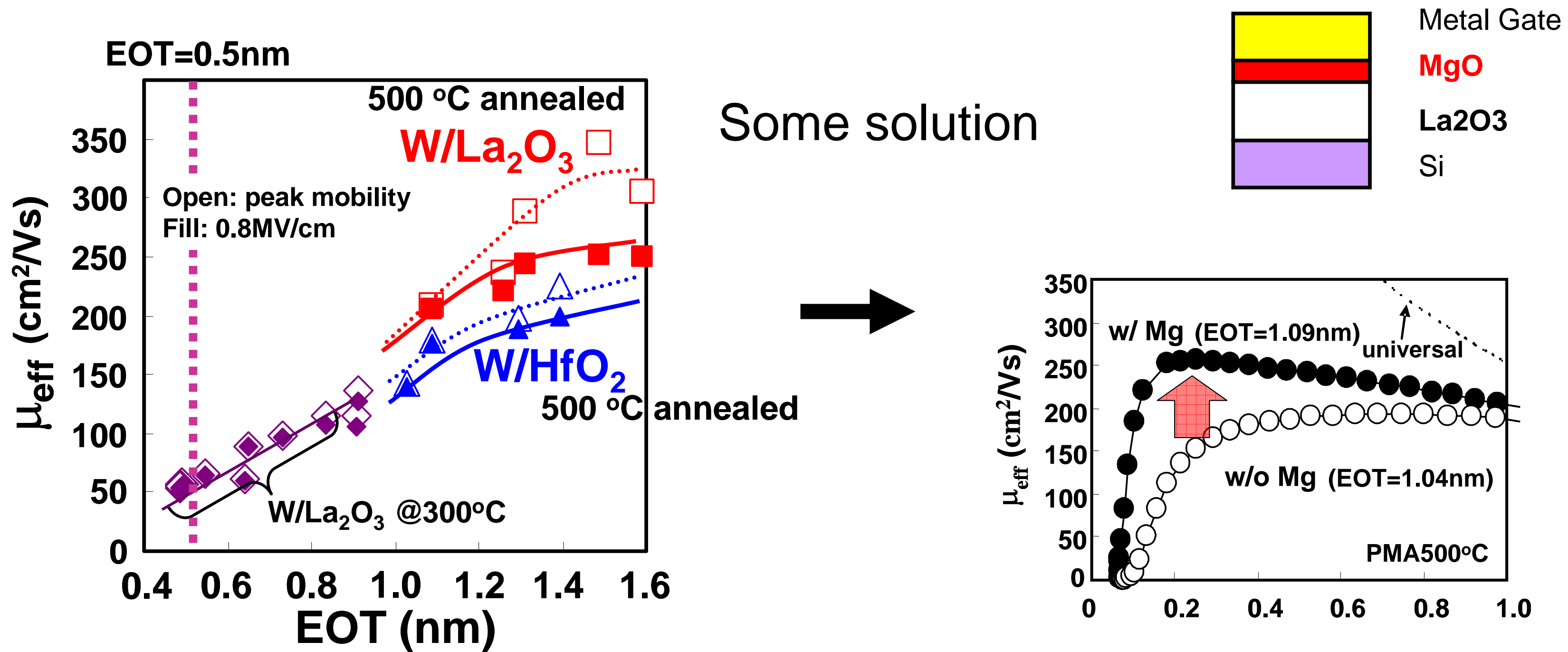


ITRS2007

Direct contact technology of high-k to Si

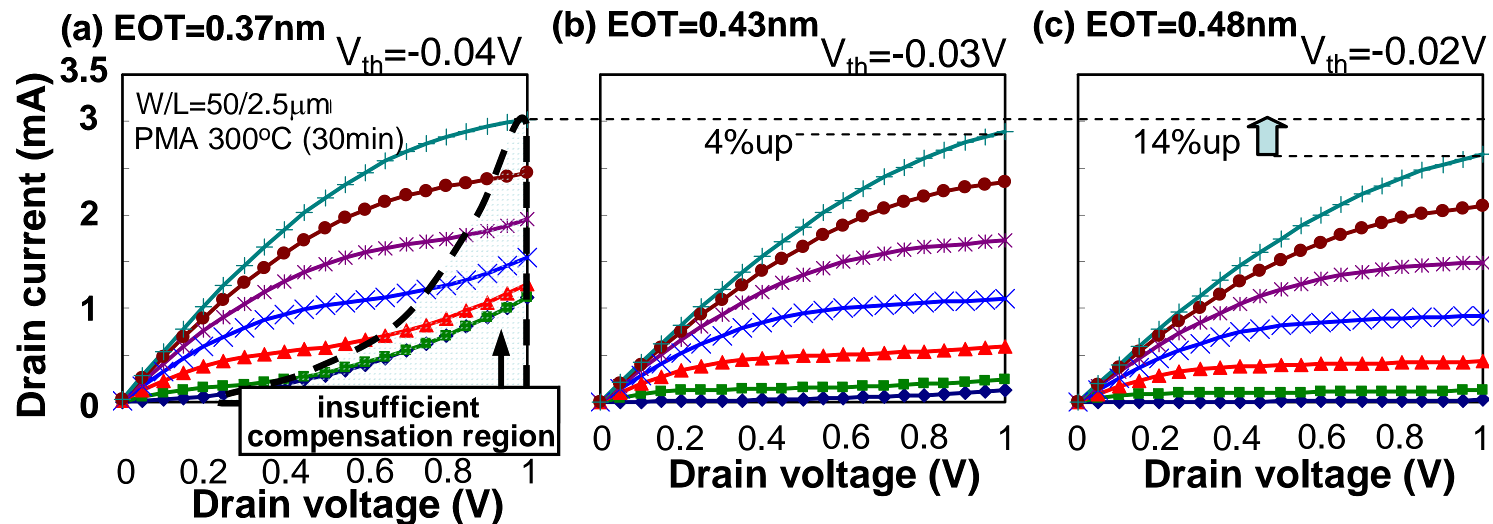


Challenge for thinning High-k

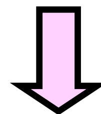


Challenge to EOT~0.3nm

EOT<0.5nm with Gain in Drive Current

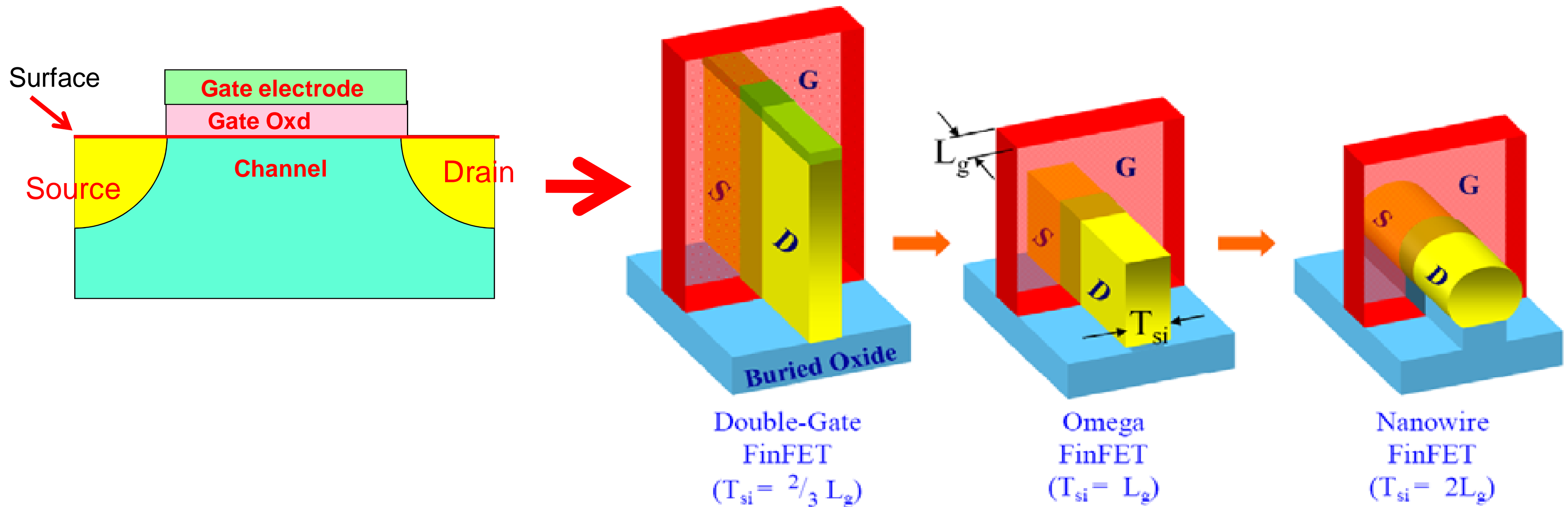


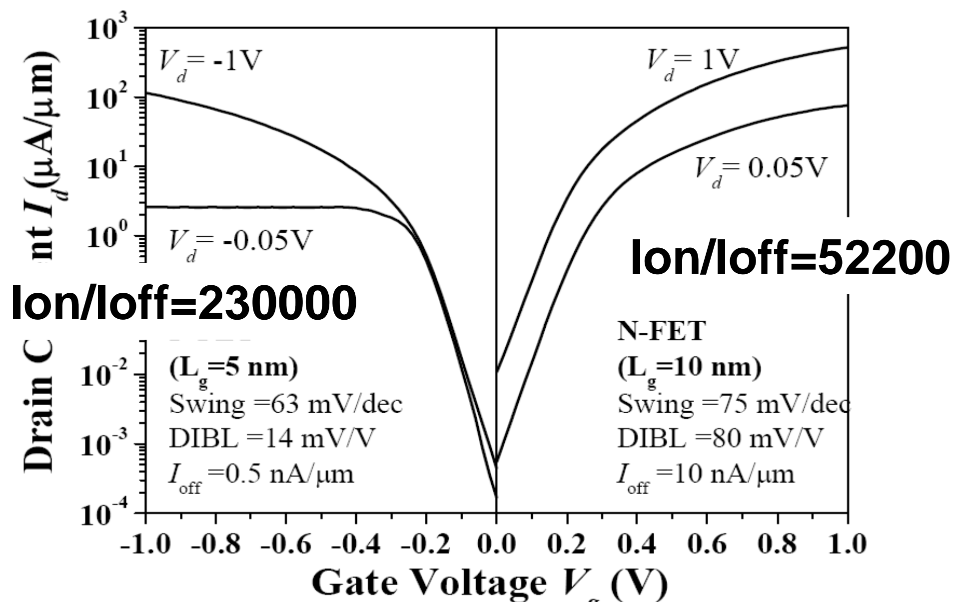
14% of I_d increase is observed even at saturation region

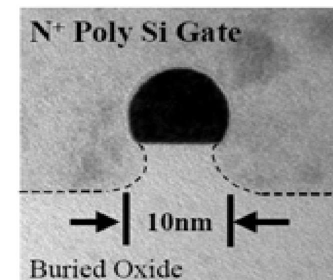


EOT below 0.4nm is still useful for scaling

FinFET to Nanowire



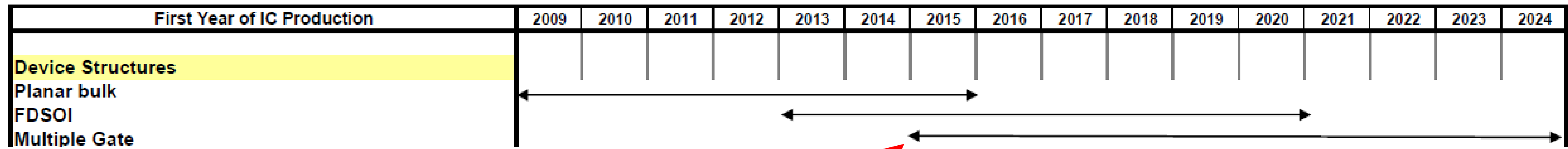




Channel conductance is well controlled by Gate even at L=5nm

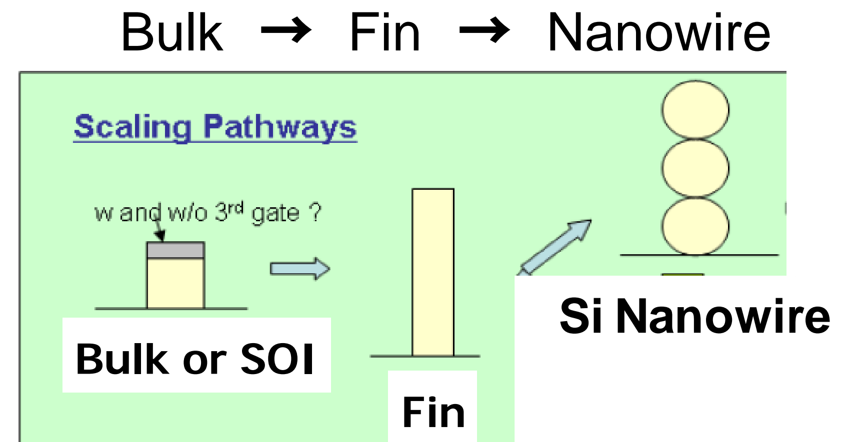
F.-L.Yang, VLSI2004

Nanowire FET



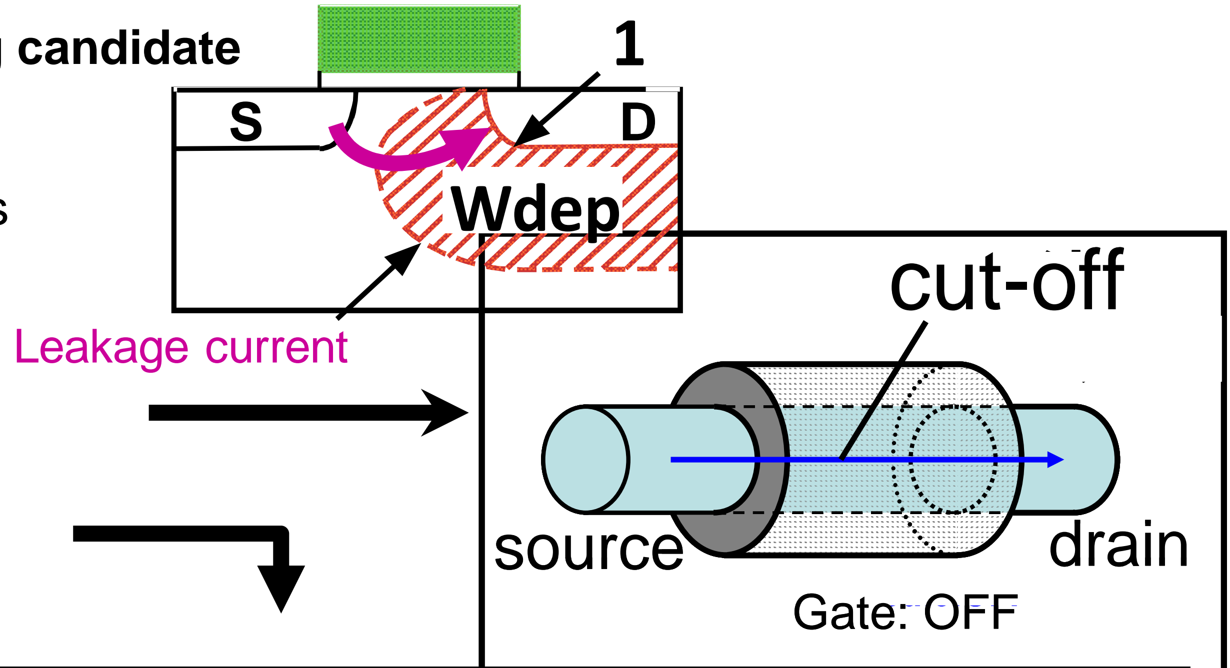
Multiple Gate (Fin)FET

ITRS 2009



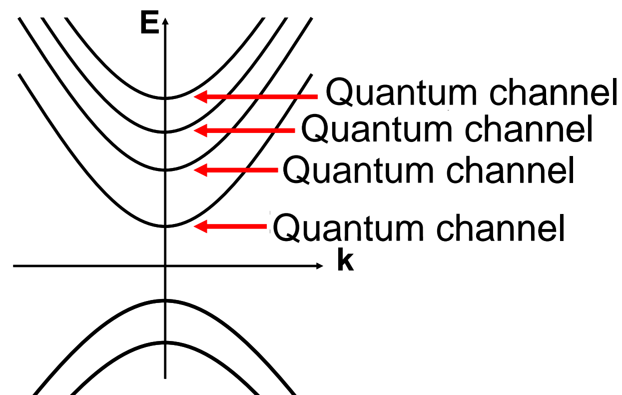
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process
2. Good controllability of I_{OFF}
3. High drive current

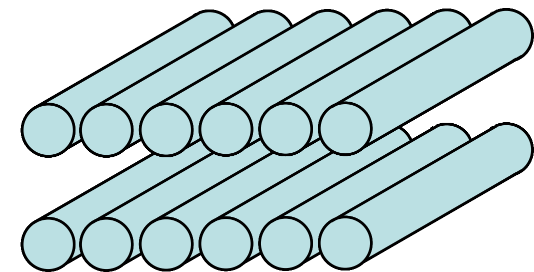


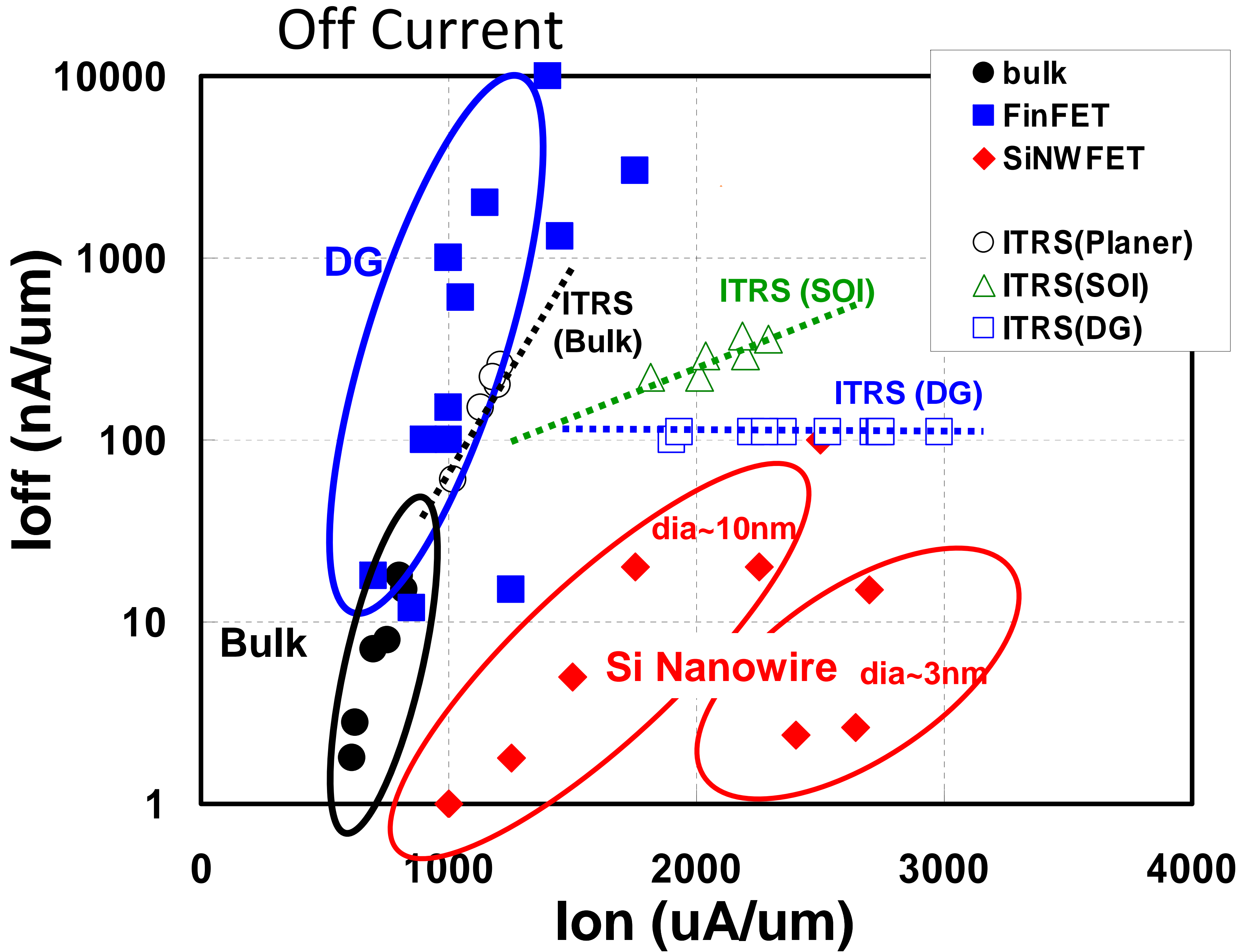
1D ballistic conduction

Multi quantum Channel



High integration of wires

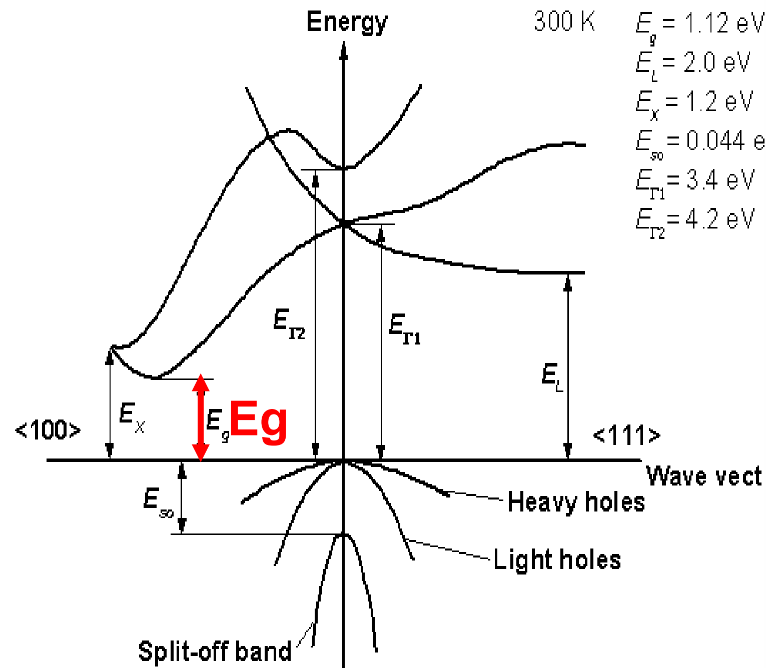




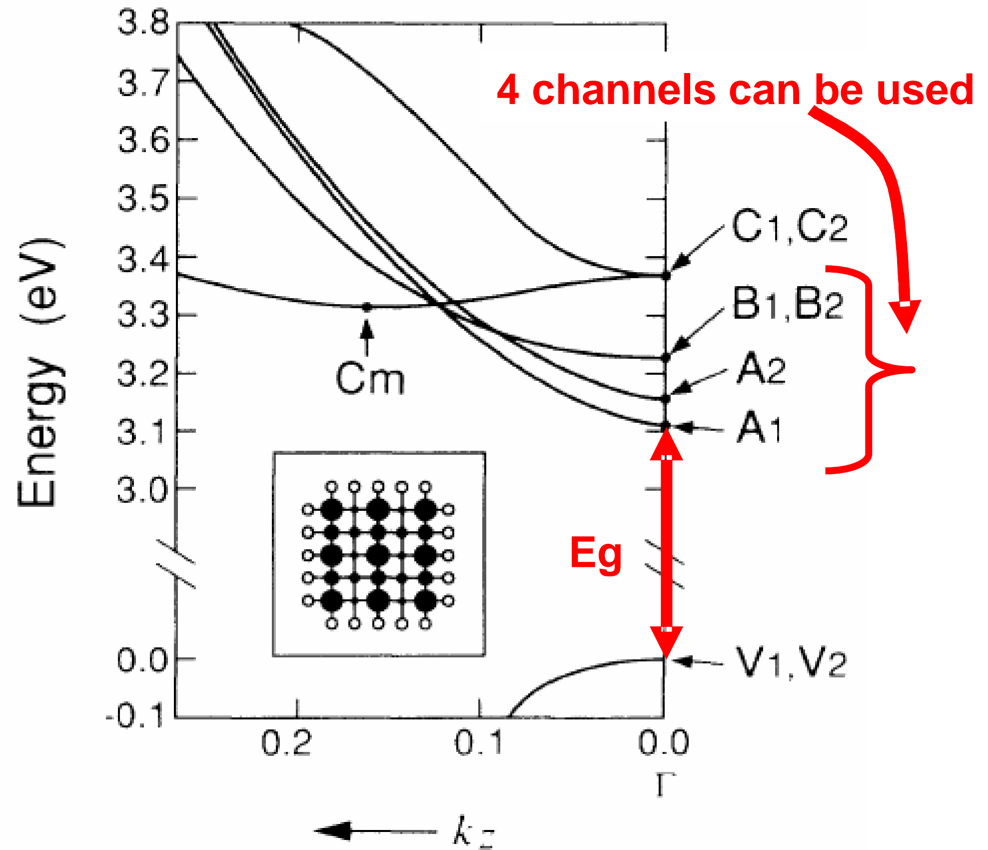
Off Current
10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

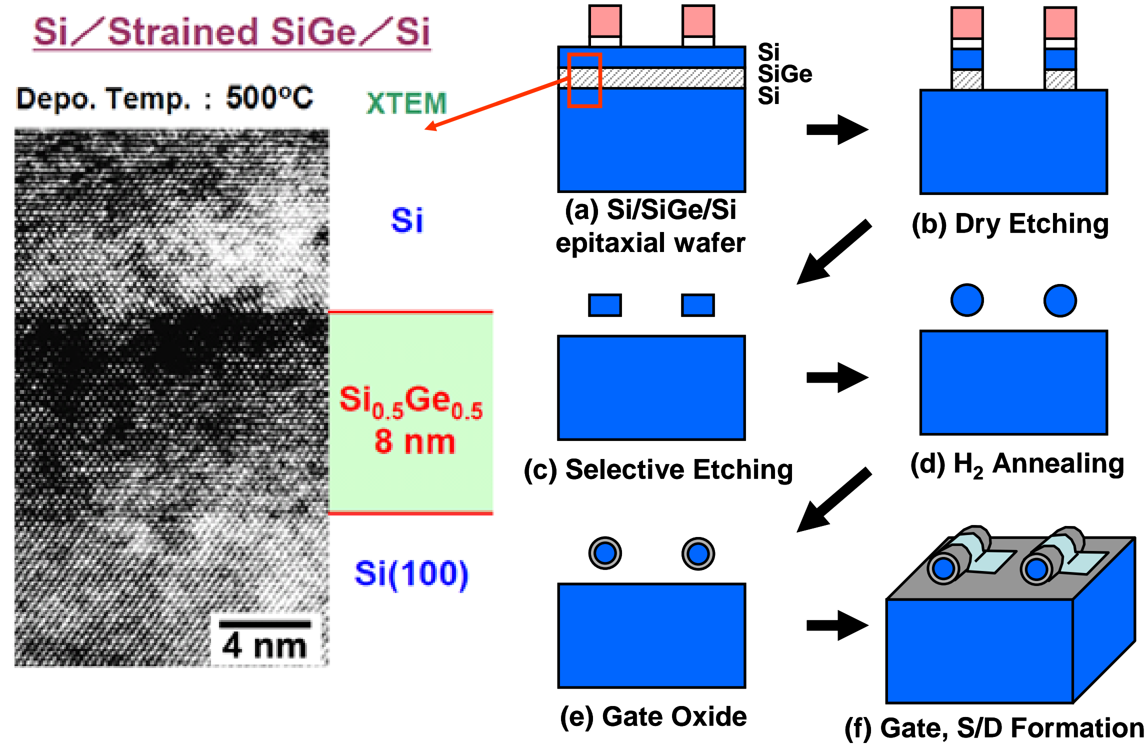


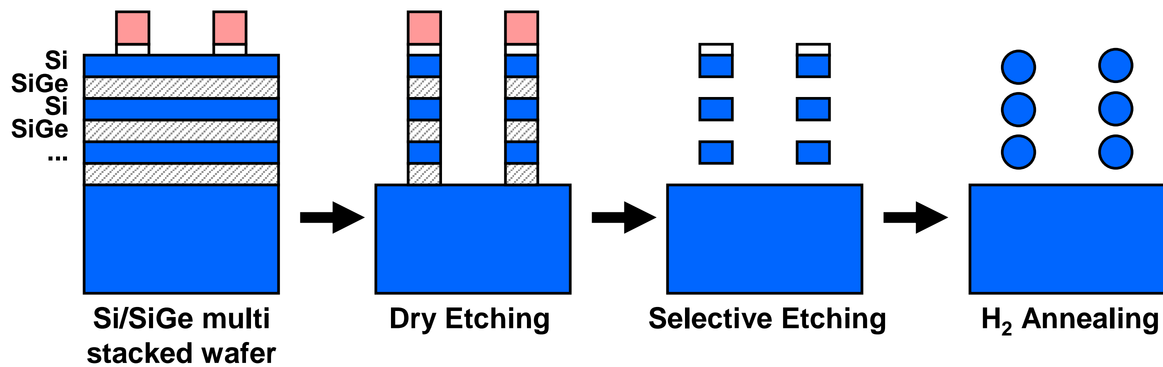
Energy band of Bulk Si



Energy band of 3 x 3 Si wire

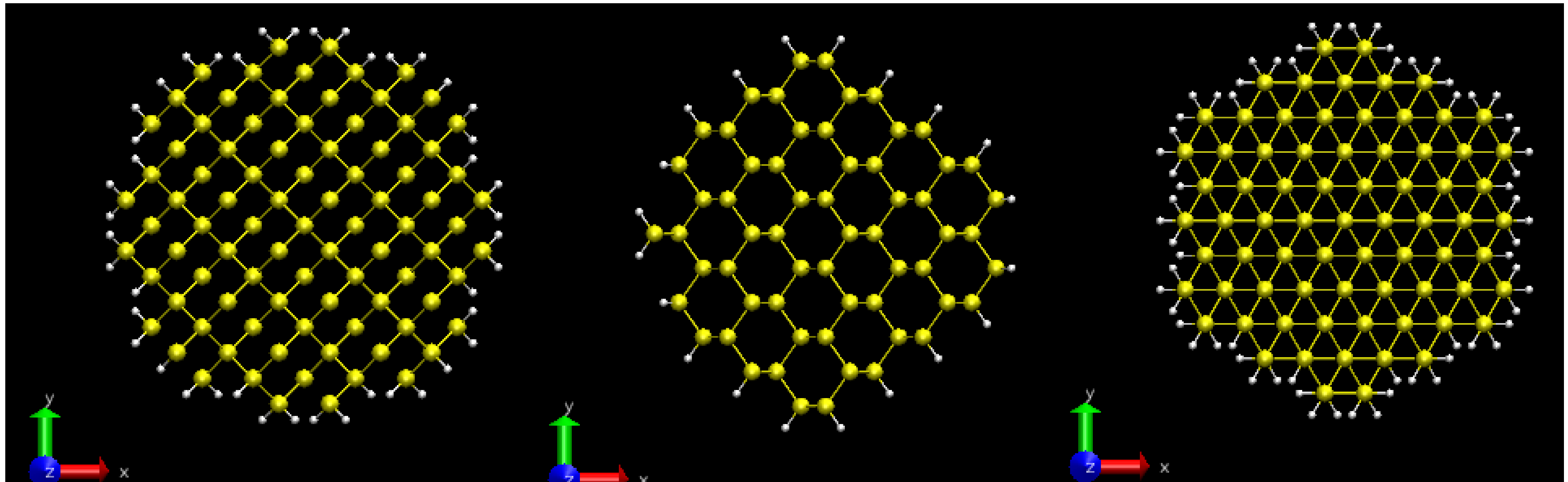
Increase the number of wires towards vertical dimension





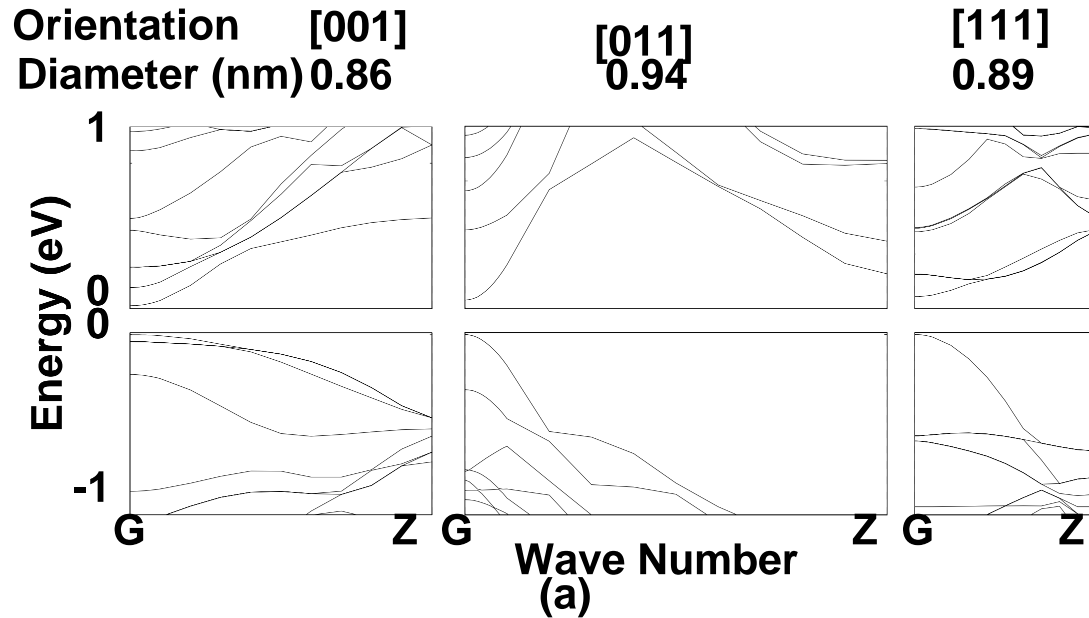
Cross section of Si NW

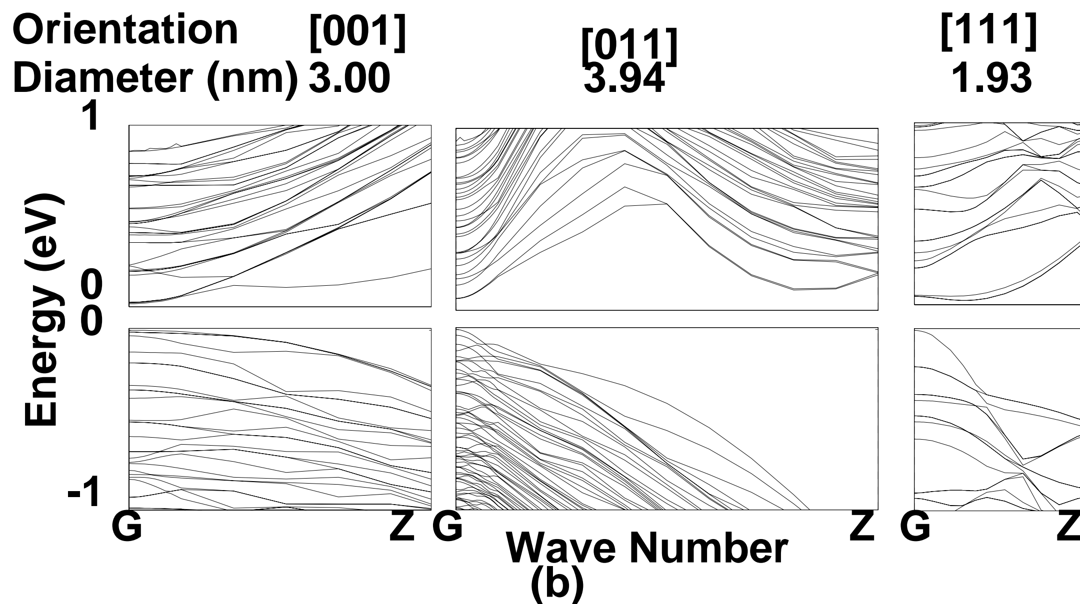
First principal calculation, TAPP



D=1.96nm	D=1.94nm	D=1.93nm
[001]	[011]	[111]

Si nanowire FET with 1D Transport

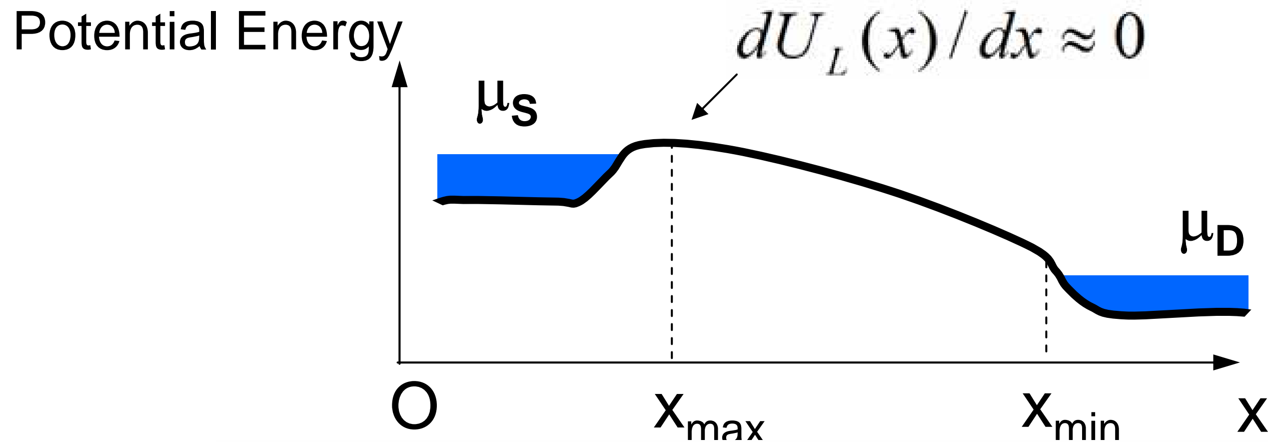




Small mass with [011]

Large number of quantum channels with [001]

Landauer Formalism for Ballistic FET

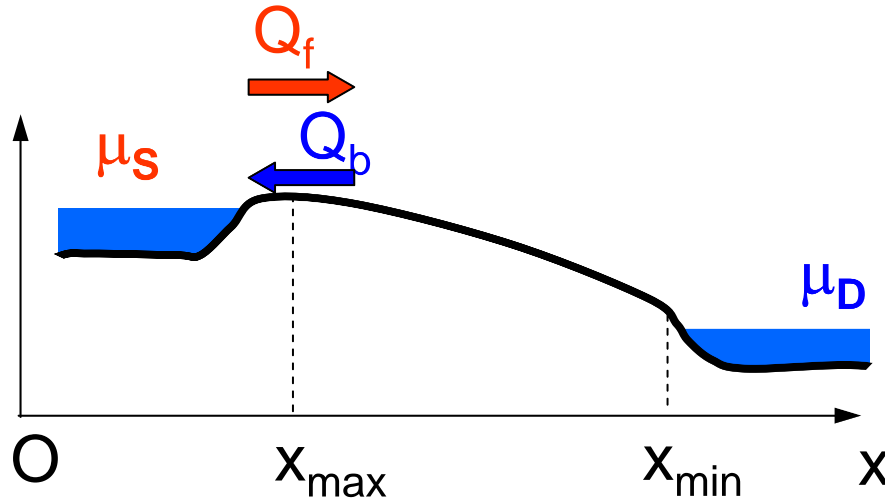


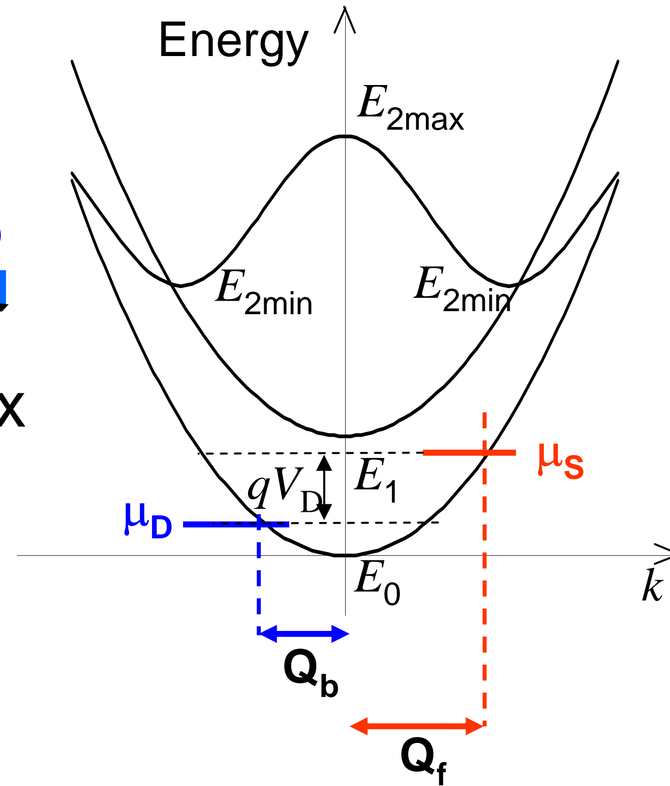
$$I_D = \frac{q}{\pi\hbar}\sum_i \int \left[f(E,\mu_S) - f(E,\mu_D)\right] T_i(E)\,dE$$

From x_{max} to x_{min} $\quad T_i(E) \approx 1$

$$I_D = G_0\left(\frac{k_B T}{q}\right)\sum_i g_i \ln\left\{\frac{1+\exp\left[(\mu_S - E_{i0})/k_B T\right]}{1+\exp\left[(\mu_D - E_{i0})/k_B T\right]}\right\}$$

Carrier Density obtained from E-k Band

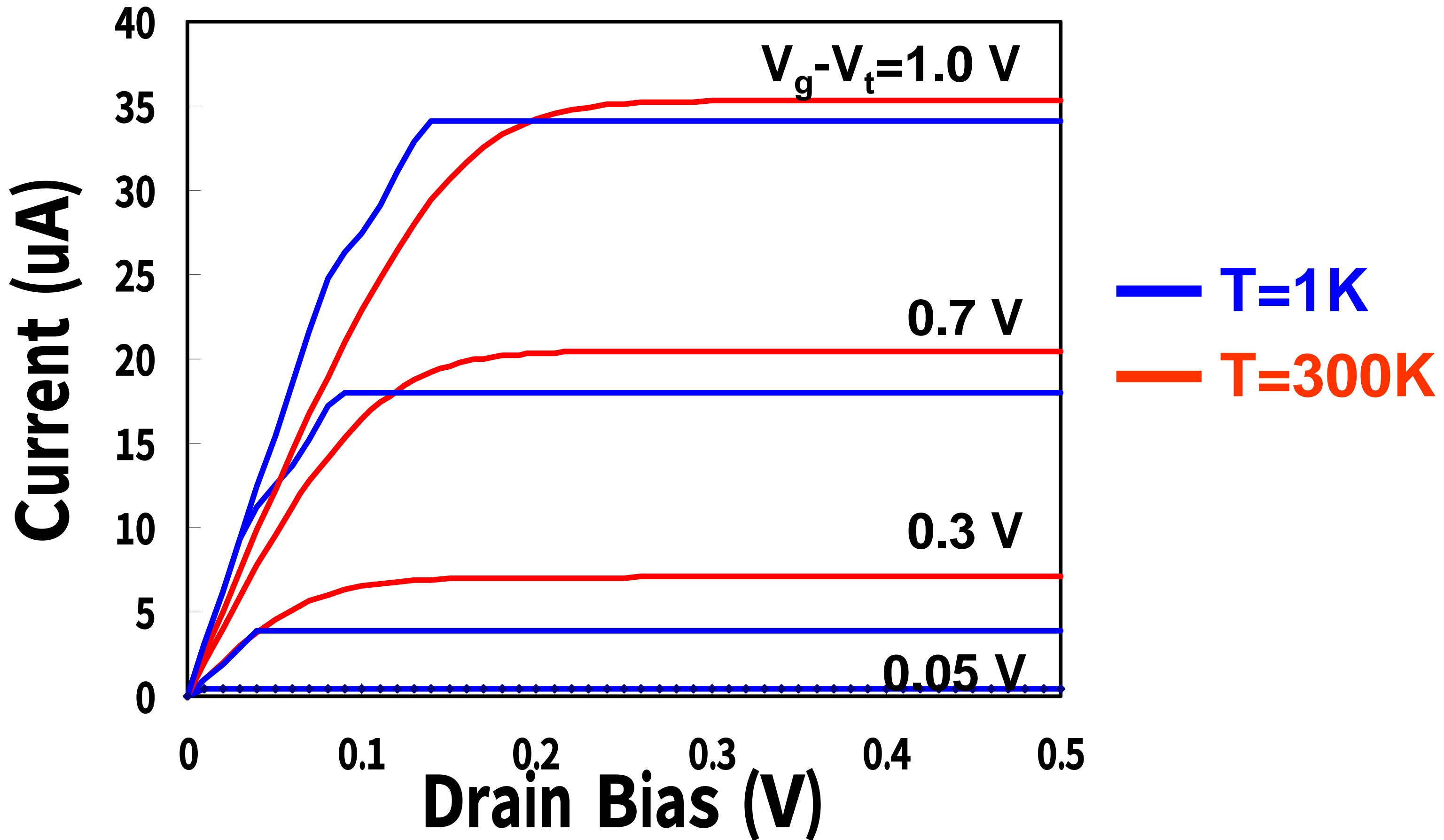




$$|Q| = |Q_f| + |Q_b|$$

$$= \frac{q}{\pi} \sum_i g_i \left[\int_{k_{i\min}}^{\infty} \frac{dk}{1 + \exp\left\{ \frac{E_i(k) - \mu_S}{k_B T} \right\}} + \int_{-\infty}^{k_{i\min}} \frac{dk}{1 + \exp\left\{ \frac{E_i(k) - \mu_D}{k_B T} \right\}} \right]$$

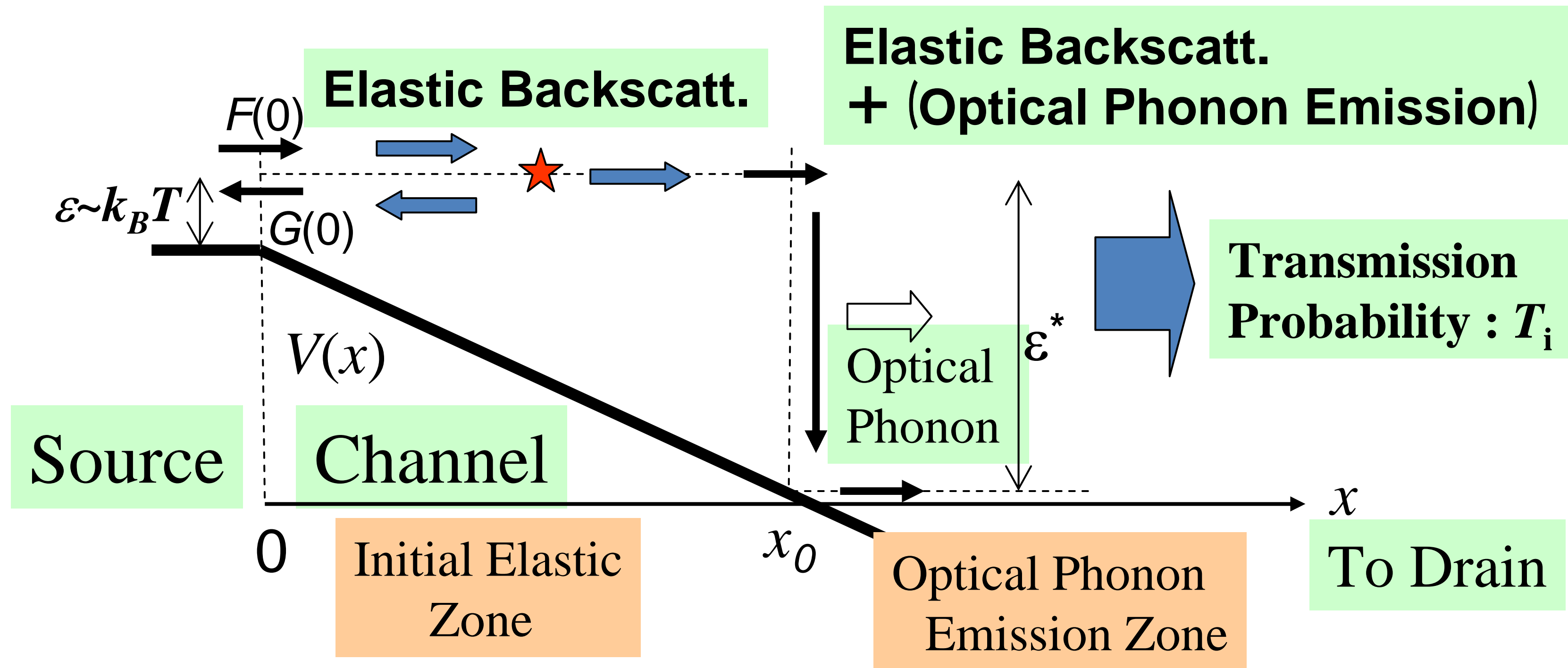
IV Characteristics of Ballistic SiNW FET



Small temperature dependency
35μA/wire for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx. : Electric Field E



Transmission Probability to Drain

$$T(\varepsilon) = \left.\frac{F(0) - G(0)}{F(0)}\right)_{\text{Injection from Drain}=0}$$

Résumé of the Compact Model

$$I = \frac{q}{\pi\hbar}\sum_i g_i \int \left[f(\varepsilon,\mu_s) - f(\varepsilon,\mu_D) \right] T_i \, d\varepsilon$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left\{ \frac{\sqrt{2r+t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r+t_{ox}} - \sqrt{t_{ox}}} \right\}}.$$

Planar Gate

$$(V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{\left| Q_f + Q_b \right|}{C_G}.$$

$$\mu_S - \mu_D = qV_D$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left(\frac{r+t_{ox}}{r} \right)}.$$

GAA

(Electrostatics requirement)

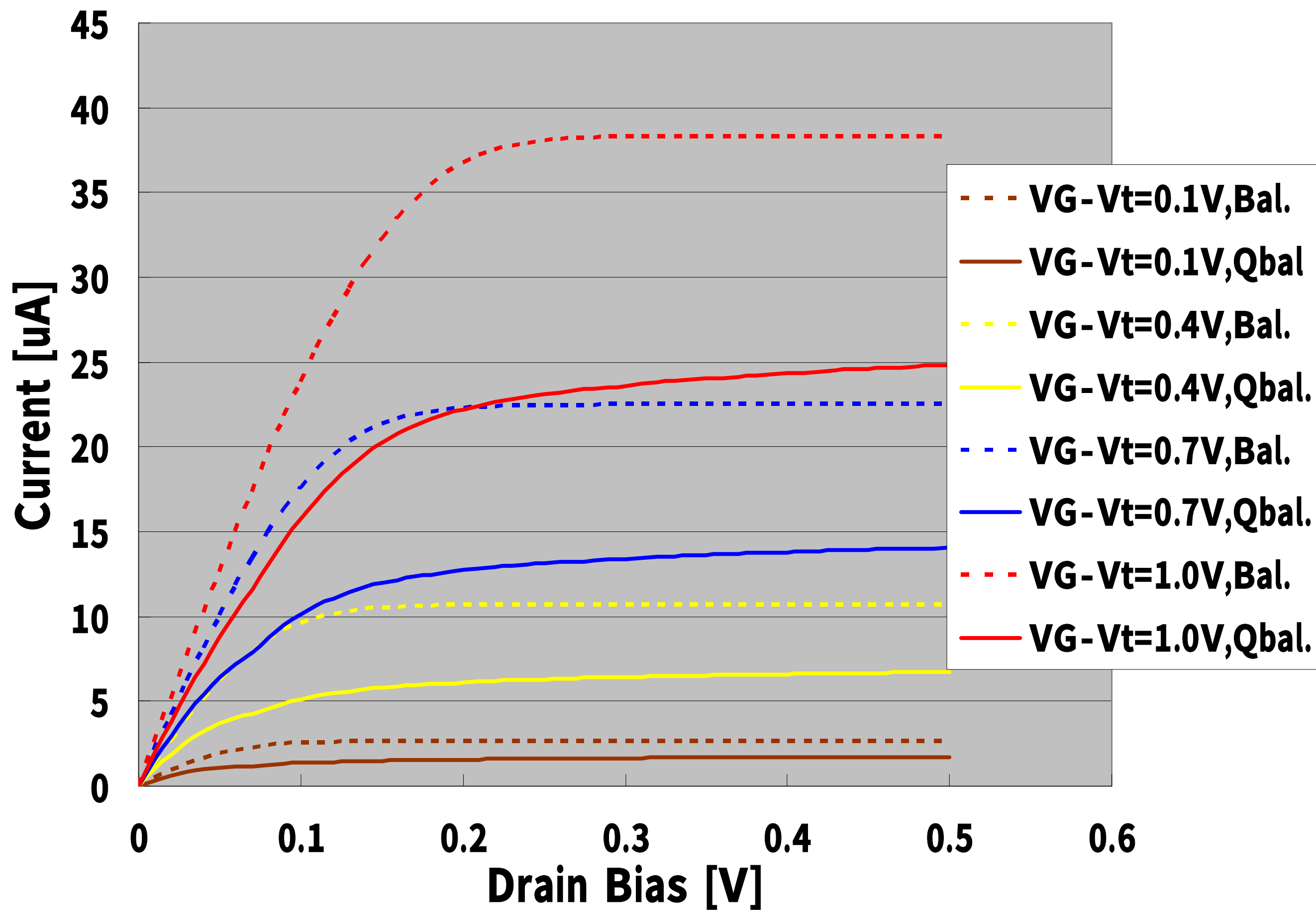
$$\left| Q_f + Q_b \right| = \frac{q}{\pi}\sum_i g_i \left[\int_{-\infty}^{\infty} \frac{dk}{1+\exp\left\{ \frac{\varepsilon_i(k) - \mu_S}{k_B T} \right\}} - \int_{-\infty}^{0} \left\{ \frac{1}{1+\exp\left\{ \frac{\varepsilon_i(k) - \mu_S}{k_B T} \right\}} - \frac{1}{1+\exp\left\{ \frac{\varepsilon_i(k) - \mu_D}{k_B T} \right\}} \right\} T_i(\varepsilon_i(k))\, dk \right]$$

$$T(\varepsilon) = \frac{\sqrt{2D_0}\, qE}{\left(\sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0}\, B_0 \ln\left(\frac{qEx_0 + \varepsilon}{\varepsilon} \right)}$$

(Carrier distribution in Subbands)

Unknowns are I_D, $(\mu_S - \mu_0)$, $(\mu_D - \mu_0)$, および $(Q_f + Q_b)$

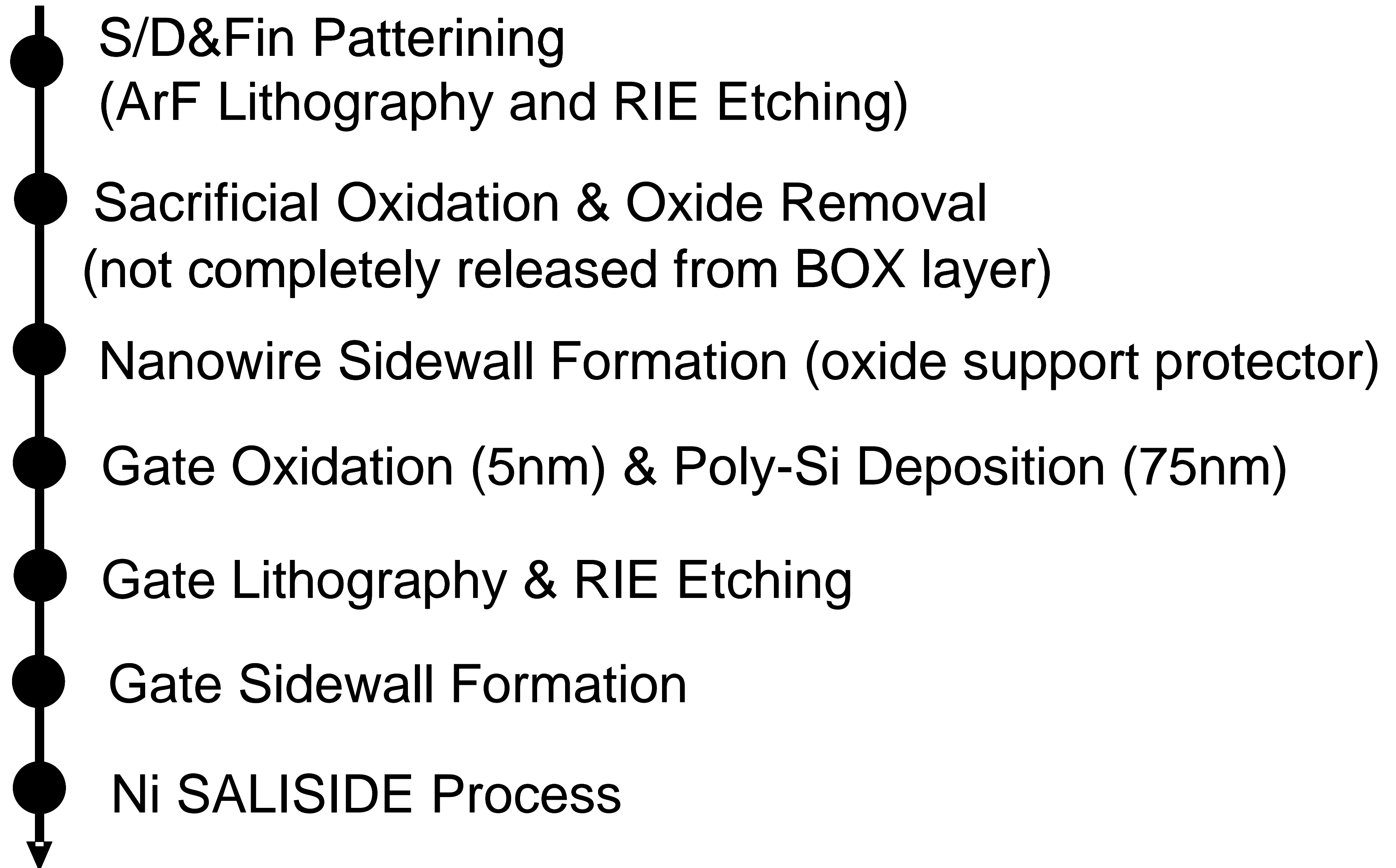
I-V_D Characteritics (RT)



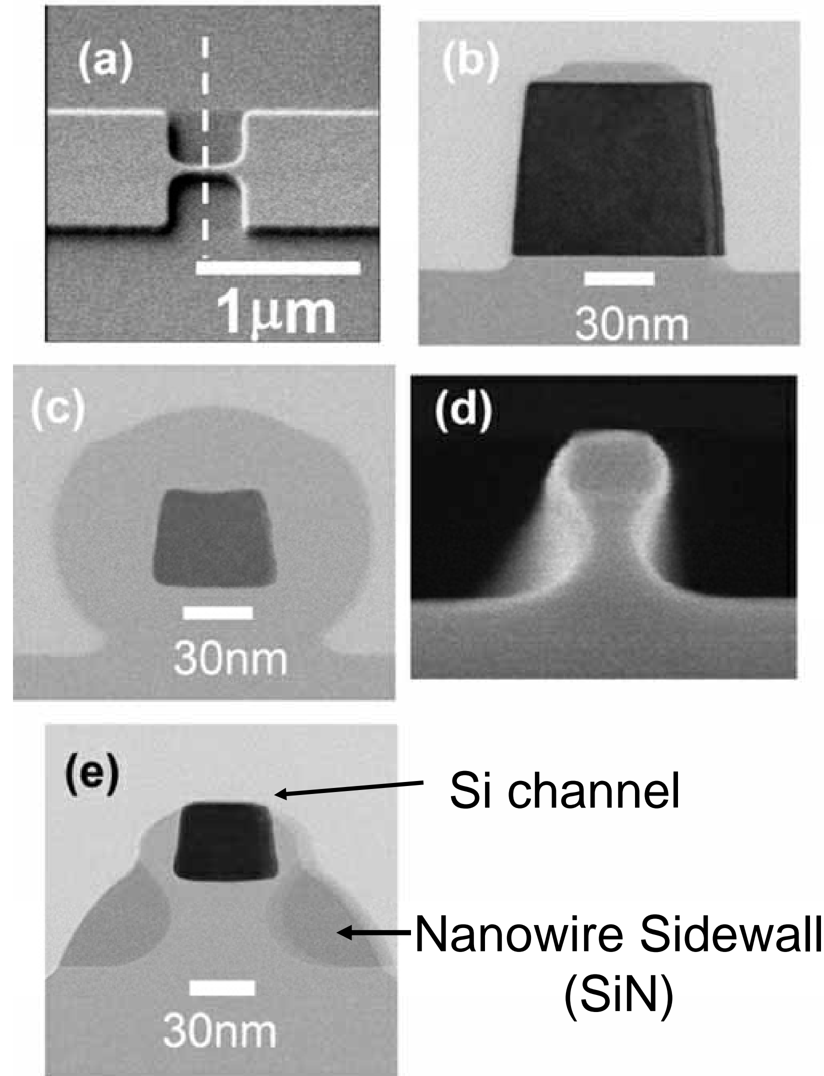
- Electric current 20～25 μA
- No saturation at Large V_D

SiNW FET Fabrication

Brief process flow of Si Nanowire FET

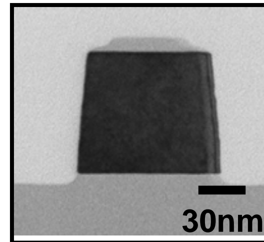


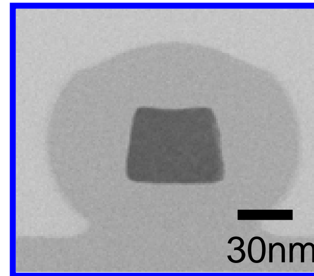
(a) Fin structure formed on BOX layer. (b)XTEM image of fin shown in (a) (c) XTEM image after sacrificial oxidation (d) Cross sectional SEM image after partial removal of sacrificial oxide (e) XTEM after nanowire sidewall formation

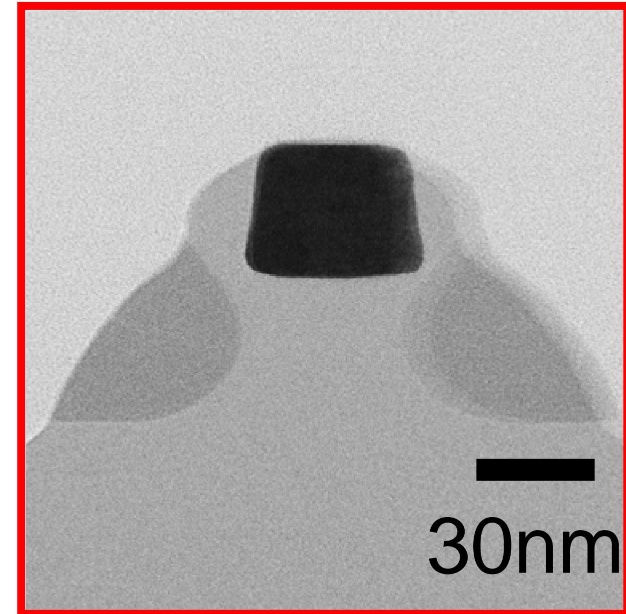


SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oixde etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

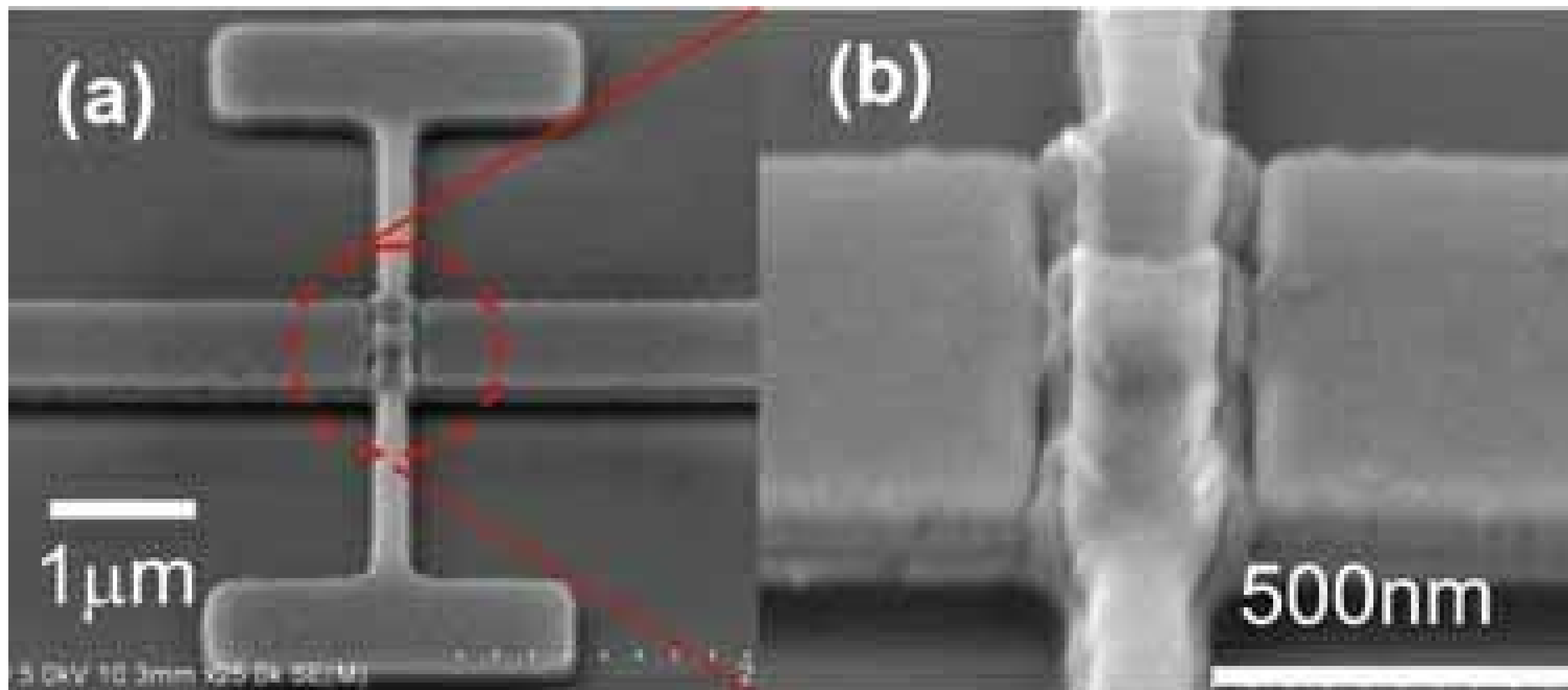




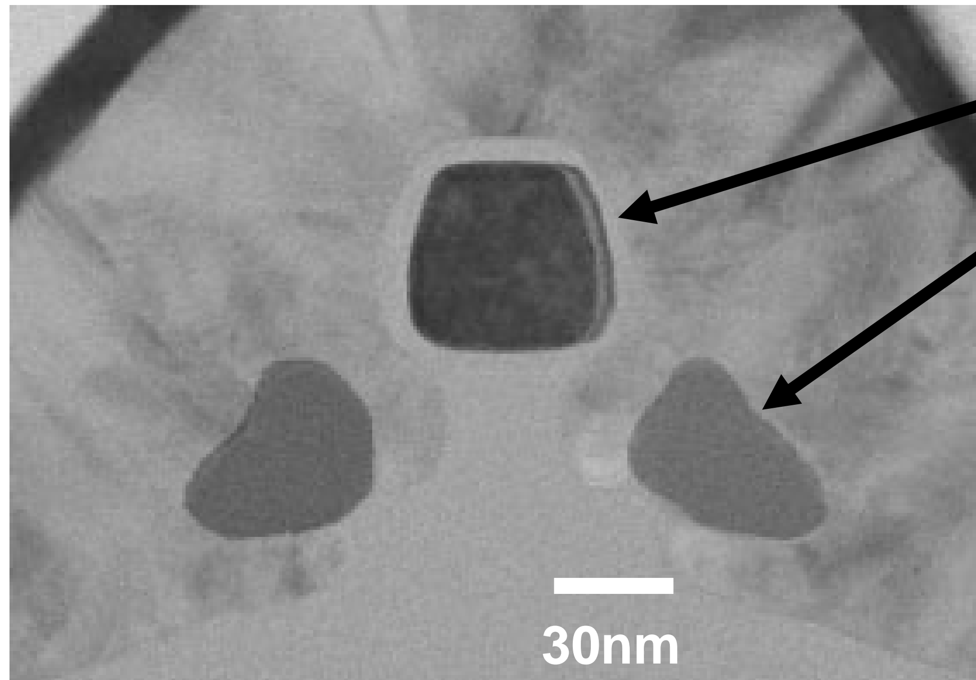


Standard recipe for gate stack formation

(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.

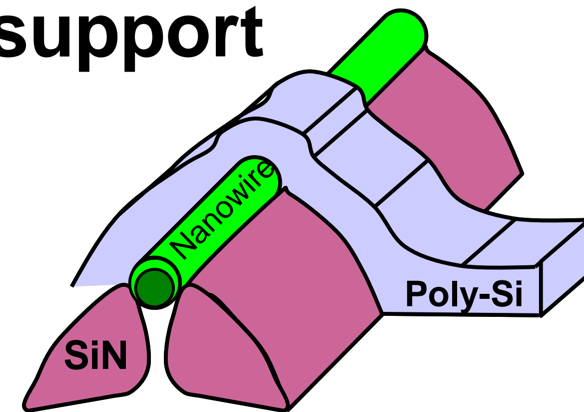


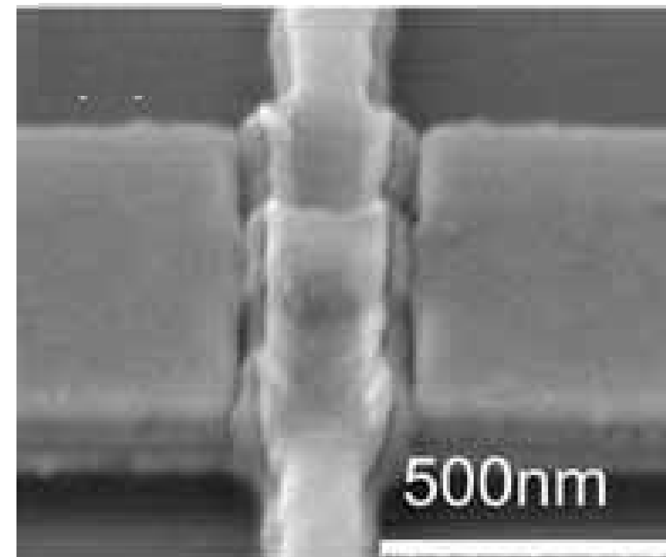
Fabricated SiNW FET



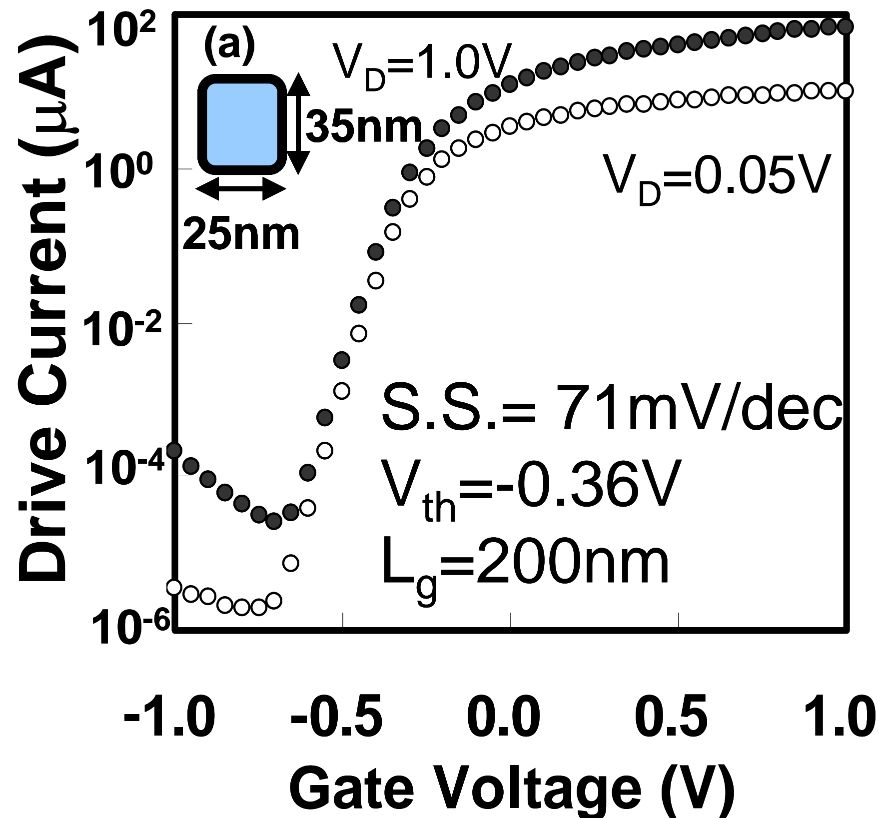
SiNW

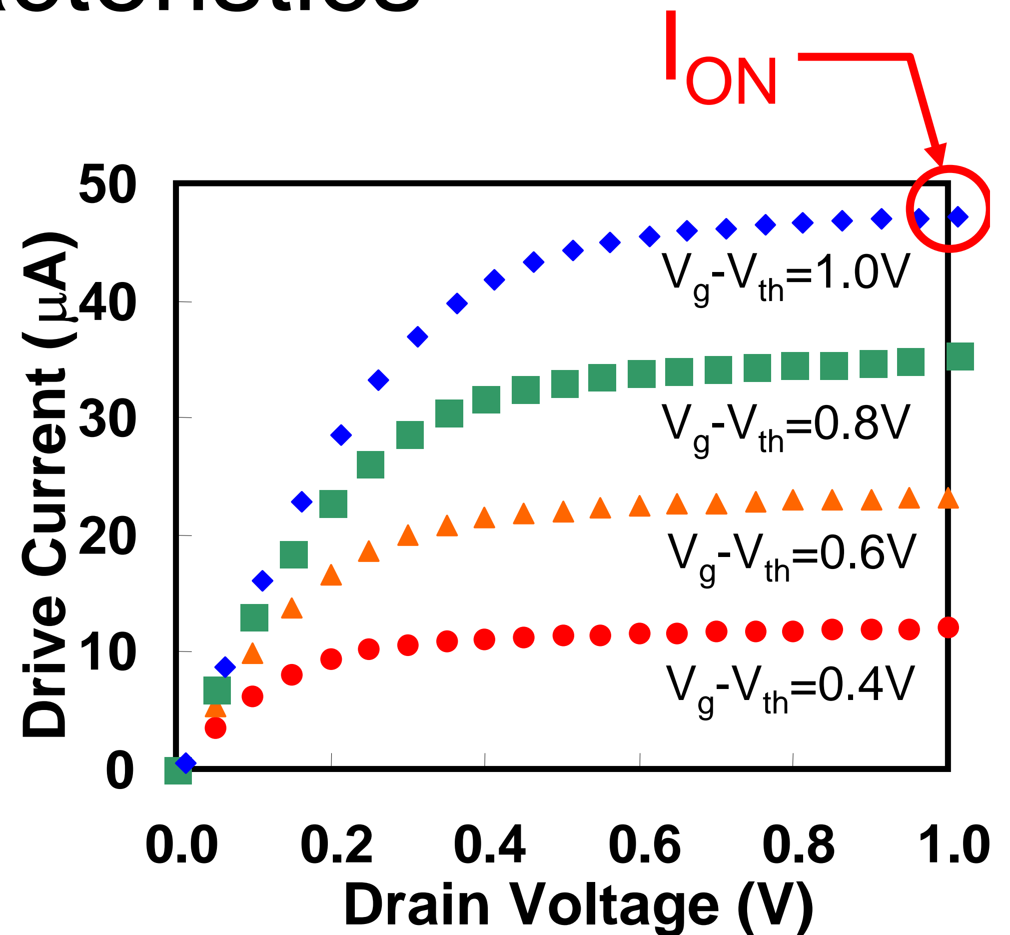
SiN support





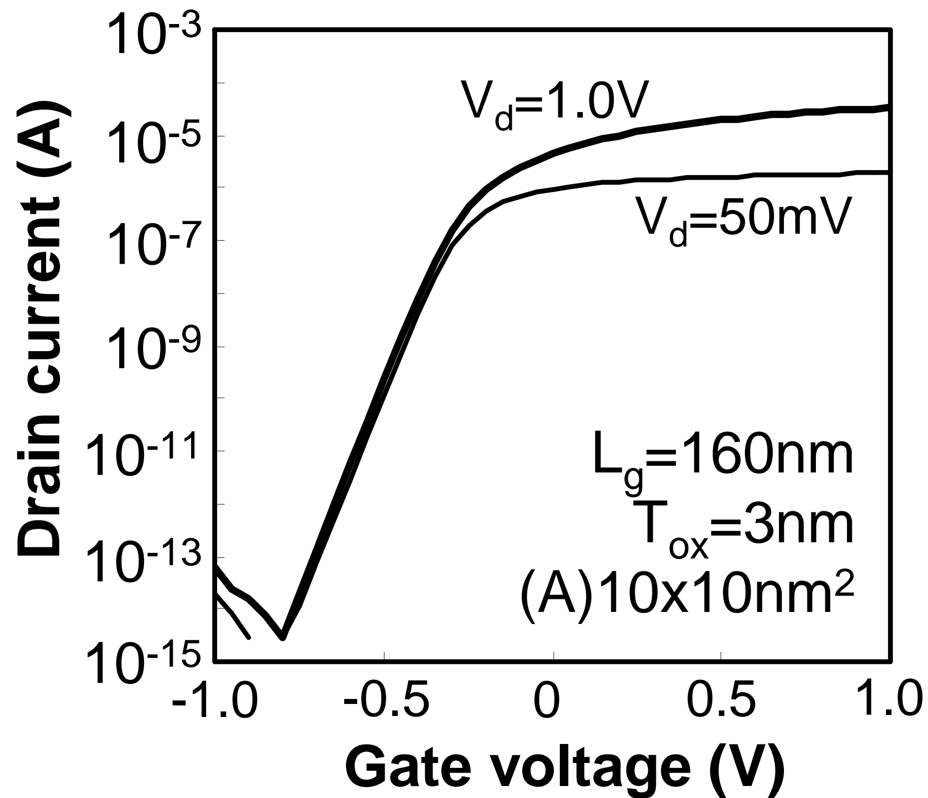
I_dV_g and I_dV_d Characteristics

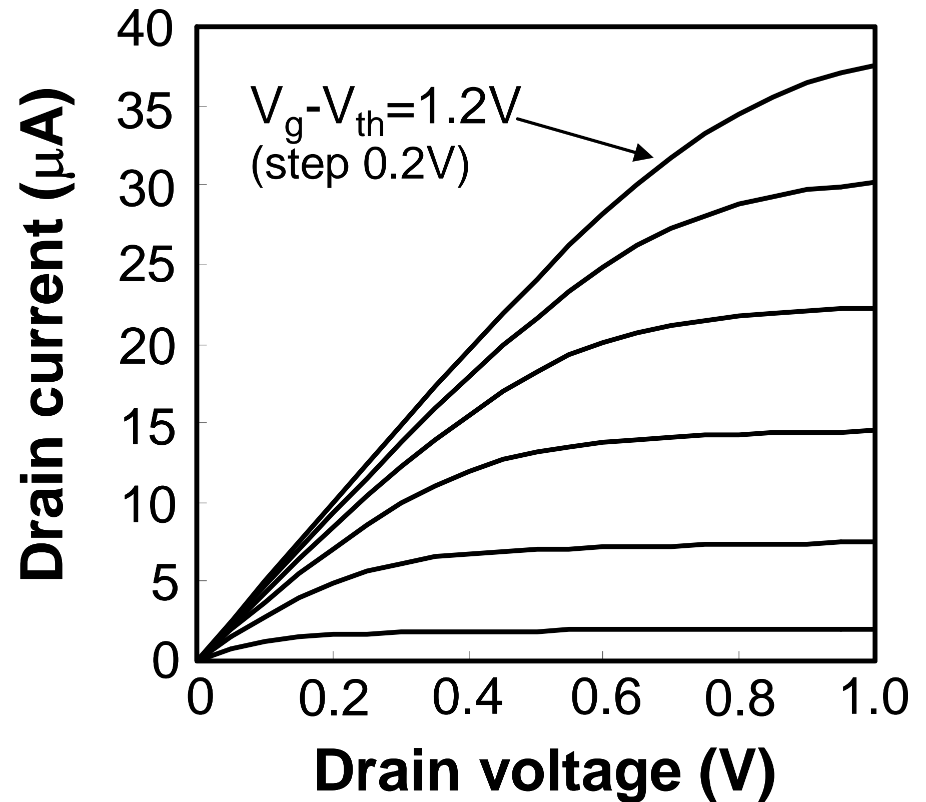


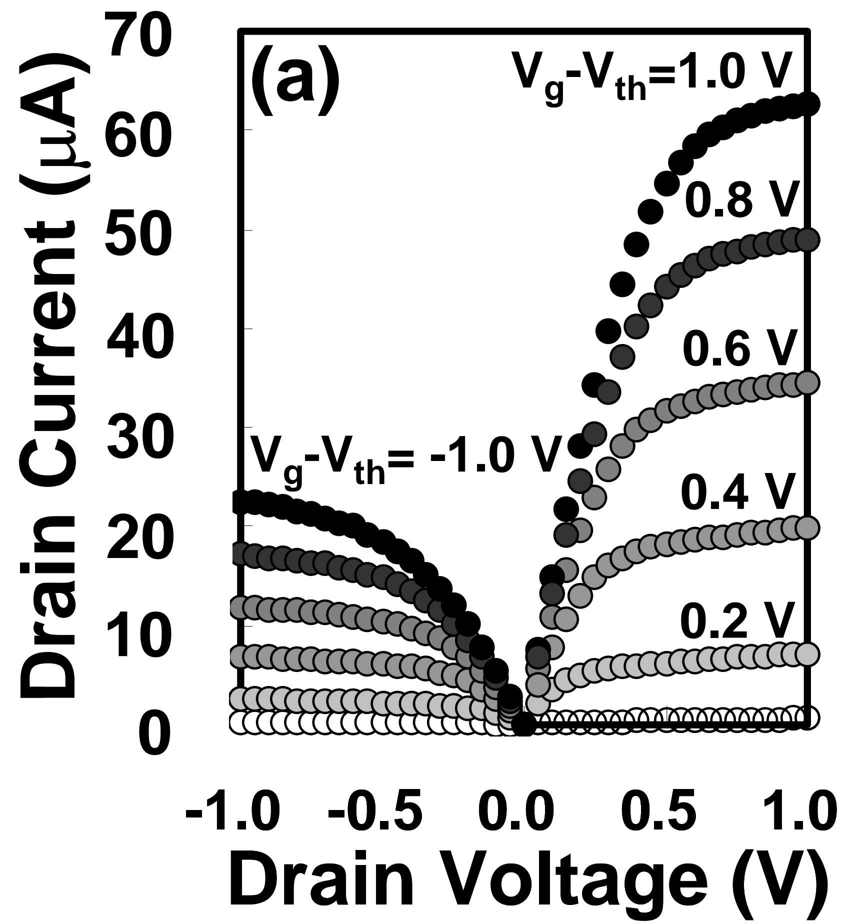


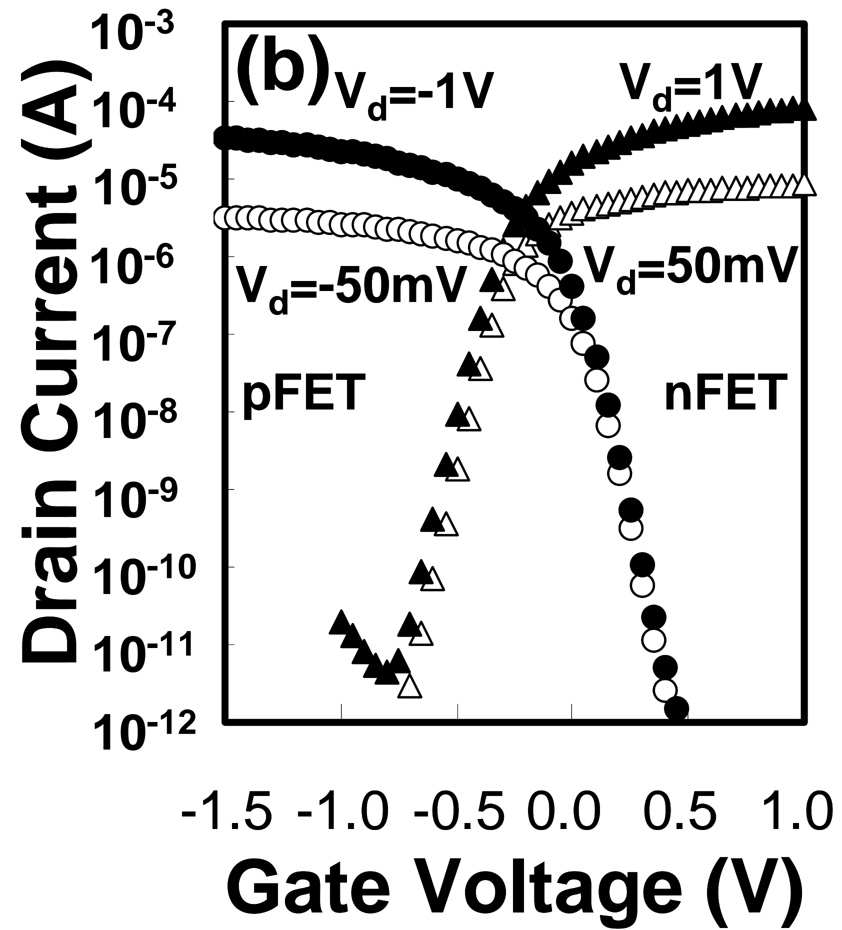
I_{on}/I_{off} ratio of ~10^7, high I_{on} of 49.6 μA/wire

Output characteristics of 10x10nm^2 SiNW FET









On/Off>10^6、60uA/wire

L_g=65nm, T_{ox}=3nm

102μA (10x20)

V_{DD}: 1.0~1.5 V

nMOS
pMOS

括弧内は寸法を示す

Our Work

(12x19) (12) (13x20) (10) (9x14) (16) (10) (12x19) (5) (34) (8) (12) (10) (30) (13) (8) (10) (5) (10) (19) (3) (3)

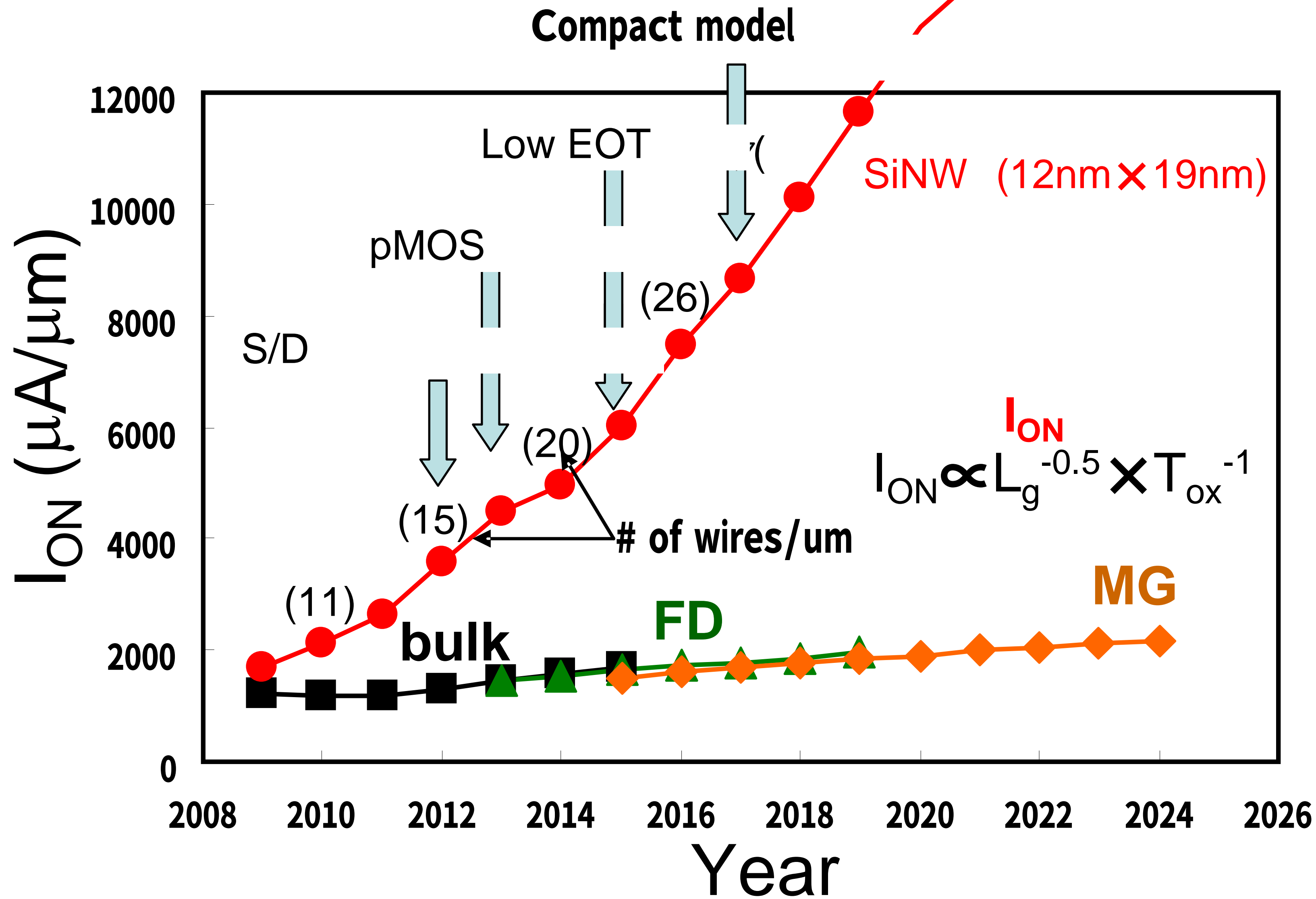
I_{ON} (μA / wire)

0 10 20 30 40 50 60 70

1 10 100 1000

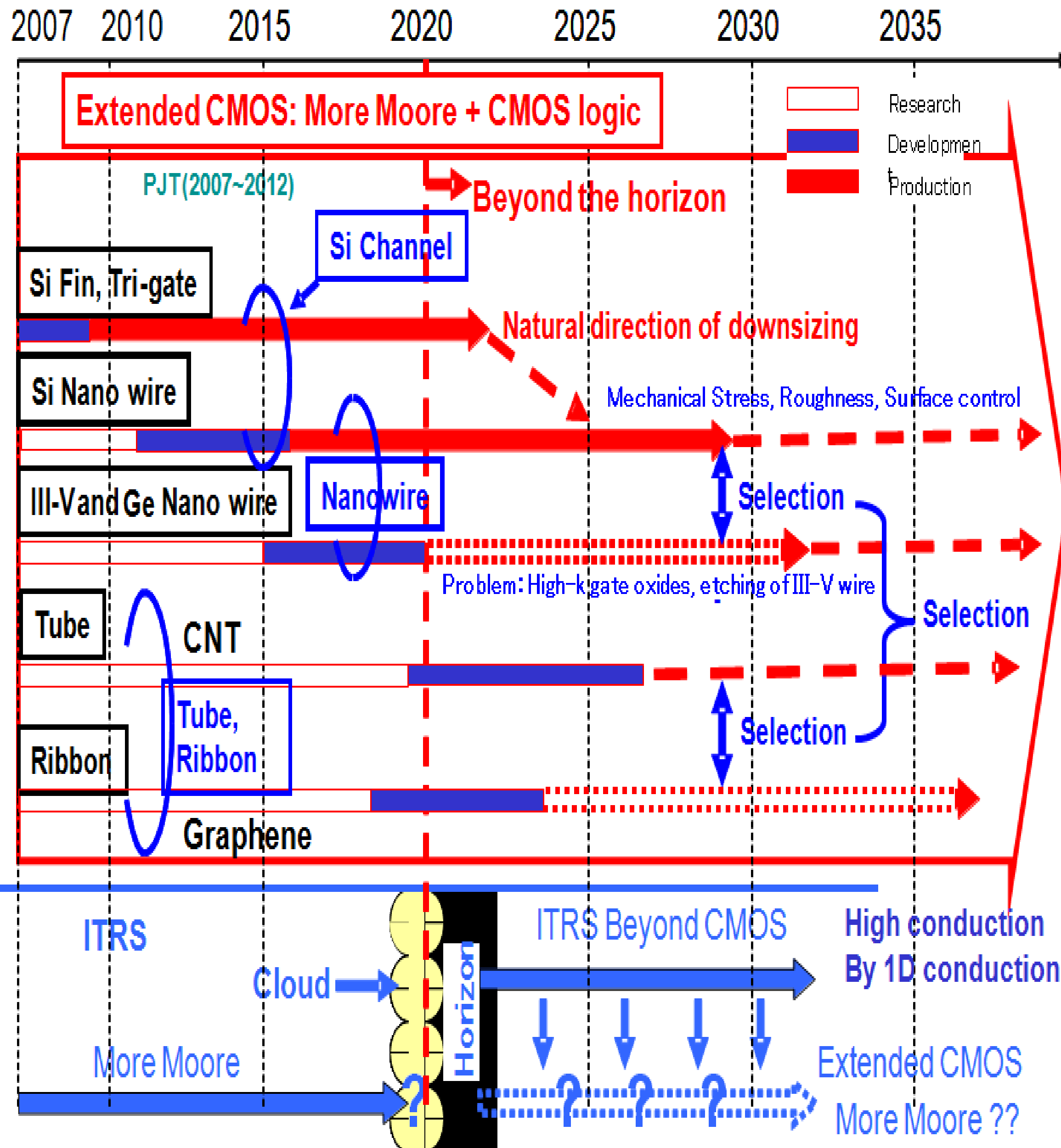
Gate Length (nm)

Simple prediction from experimental data



Our roadmap for R &D

Source: H. Iwai, IWJT 2008



Current Issues

Si Nanowire

Control of wire surface property
Source Drain contact
Optimization of wire diameter
Compact I-V model

III-V & Ge Nanowire

High-k gate insulator
Wire formation technique

CNT:

Growth and integration of CNT
Width and Chirality control
Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique
Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

Conclusion

Si CMOS is still the most important mainstream technology for another 20~30 years, and we have to make effort to continue the scaling with by all means.

This will contribute significantly for the cool earth in short and long terms/

Acknowledgement

People in

TIT, Waseda Univ

Tsukuba Univ, U of Tokyo

Sponsor

NEDO/METI

Thank you for your attention