

Future perspective for the mainstream CMOS technology and their contribution to green technologies

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Abstract Recently, CMOS technology has been recognized as an ultimate technology towards the limit of downscaling of electronic devices for logic circuits. In other words, CMOS will keep the position of mainstream device technology as the key components for logic integrated circuits almost for ever as long as the integrated circuits are necessary for our society, even after all the logic electronic devices reach their downsizing limits. It is expected that there are still several generations or 15 ~ 25 years until the CMOS device really reaches the downsizing limit caused by the direct-tunneling between the source and drain. In order to accomplish the downscaling of CMOS devices successfully, suppressing the SCE (Short Channel Effect) or suppressing the off-leakage current with keeping its high performance is the most important. There are two major solutions to suppress the SCE; One is pushing high-k gate insulator technologies to keep thinning the gate oxide, and the other is changing the transistor structure from the planar to the 3D multiple gate structures towards nanowire FETs. In this paper, future perspective for the mainstream CMOS technology is described from the view point of its downsizing. The downsizing of CMOS devices is still the very effective way to increase the performance and to decrease the power consumption of integrated circuits, and the progress of CMOS device technology will contribute to the 'green technologies' by increasing the efficiency of the operation of every system controlled by microprocessors.

Key words Silicon, CMOS, mainstream, high-k, nanowire, green,

1. Introduction

Recently, power saving for all the human activities are strongly requested in order to prevent the global warming, and high efficiency control of every system by high-performance microprocessors is thought to be very important to save the energy loss. At the same time, energy required for information and data communication becomes non-negligible value in our society, as we can see in the case of data centers, and thus, the saving of the power consumption of integrated circuits themselves becomes also very important.

For more than 40 years, the down-scaling of MOSFETs has been the most important and effective way for achieving the high performance and low power consumption of LSIs. Now, the power consumption became the limiting factor for the LSI technology design [1], and clock frequency and chip area cannot very much increased recently. Furthermore, the concern for the technological difficulty for the downsizing becomes much stronger than the past with expected large variations of electrical characteristics of smaller geometry MOSFETs. We are also facing the tremendous cost increase in future EUV lithography as well as that in the development various sophisticated new technologies.

However, still, the downsizing is the ‘royal road’ for increasing the performance and decreasing the production cost and power consumption, and thus, the effort of downsizing of CMOS devices will be continued by all means towards the limit at least for several more generations or 15 to 20 years, even though the duration between the generations would become longer, because the products with successfully down-scaled CMOS device will dominate the market.

This paper describes a future perspective for the mainstream CMOS technology from the view point of its downsizing.

2 . Limit of CMOS downscaling and important technology development towards the limit

So far, the physical gate length of the logic CMOS has been much smaller than the half pitch of the lithography, however, the trends of the physical gate-length shrinkage predicted by recent versions of the ITRS have been even

further aggressive for the most of logic semiconductor companies to catch up. Thus, the future trend for logic device has to be adjusted to be slightly less aggressive in ITRS 2009, resulting in the delay in the gate-length shrinkage for several years in future as shown in Fig. 1 [2].

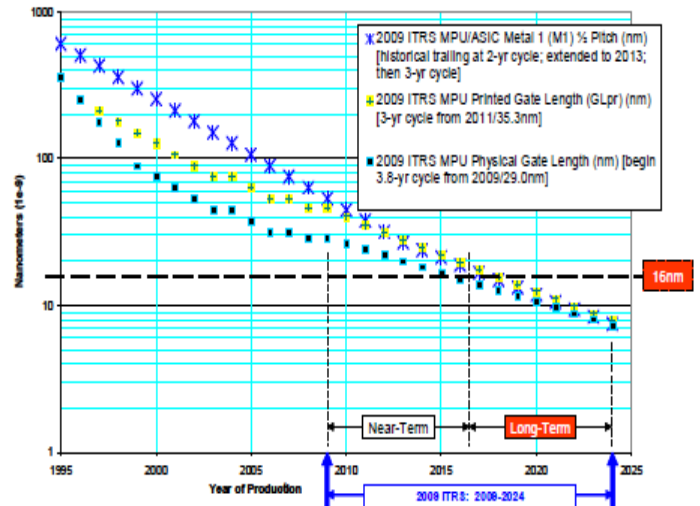


Fig. 1 2009 ITRS trend for gate length [2]

However, the trend of gate length shrinkage continues till 8 nm in 2024 in the roadmap. Now, the question is what is the limit of the gate length shrinkage. Of course, there are many arguments regarding the reasons for the limit, such as sub-threshold leakage and cost of small geometry lithography. However, the fundamental limit will be caused by the direct-tunneling between source and drain and that the limit will be about 3 nm as shown in Fig.2, and there is a possibility that CMOS gate length is reduced to that value.

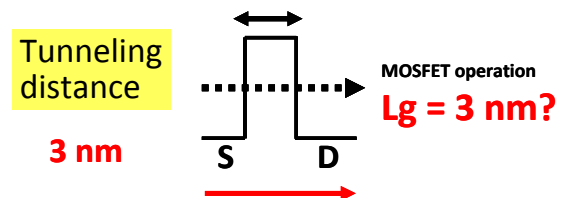


Fig.2 Gate length shrinkage limit by SD direct-tunneling

Although, we do not know how far we can down-scale the CMOS device, the following three technologies are thought to be the keys for pursuing the downsizing CMOS devices as the mainstream technology; The first is high-k gate

stack with EOT (Equivalent Oxide Thickness) less than 0.5 nm, the second is Si nanowire FET technology, and the third one is metal (silicide) source/drain technology. Those three are very effective to suppress the SCE or off-leakage current between source and drain, and also to increase the on-current. In this paper, the status of high-k gate and Si nanowire technologies are explained.

3 . High-k gate technology with EOT less than 0.5 nm

The increasing power consumption is the limiting factor of the logic CMOS, and lowering the supply voltage is the most effective way to decrease the dynamic power consumption. However, in order to decrease the supply voltage, the threshold voltage has to be reduced. This results in the significant increase in the 'off-leakage' current because of the significant increase of the subthreshold leakage current with low threshold voltage. Thus, the threshold and hence, the supply voltages cannot be scaled-down easily. Their values are supposed to stay above 0.1 and 0.9 V, respectively for next 10 years in recent ITRS as shown in Fig.3.

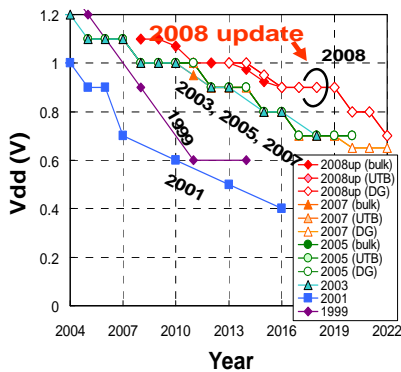


Fig. 3 Supply voltage trend in ITRS

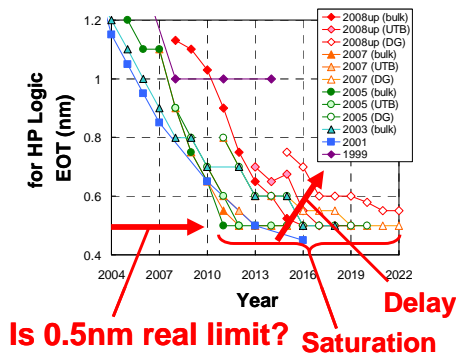


Fig.4 Gate insulator EOT trend in ITRS

It should be noted that the gate insulator EOT value stay at 0.5 nm as shown in Fig. 4. This kind of improper down scaling, – with keeping higher supply voltage and larger gate oxide thickness –, is the scheme of the downsizing for the moment. However, the improper scaling as shown in Fig. 5 enhances the short channel effects, resulting in the larger off-leakage current and larger variation of the threshold voltage. The solution to the above problems is to develop high-k gate technology with EOT below 0.5 nm, and key to this technology is to use the direct contact between the high-k and silicon substrate using rare earth oxides as the material as shown in Fig. 6.

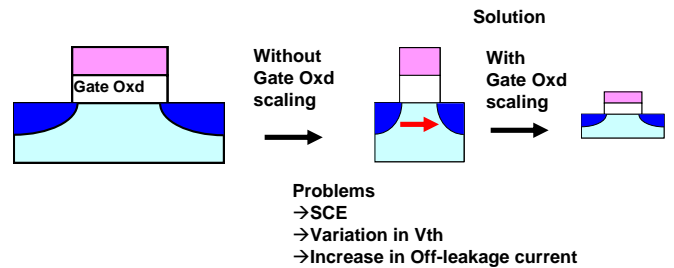


Fig. 5 Problems caused by improper scaling scheme with out gate oxide thickness scaling

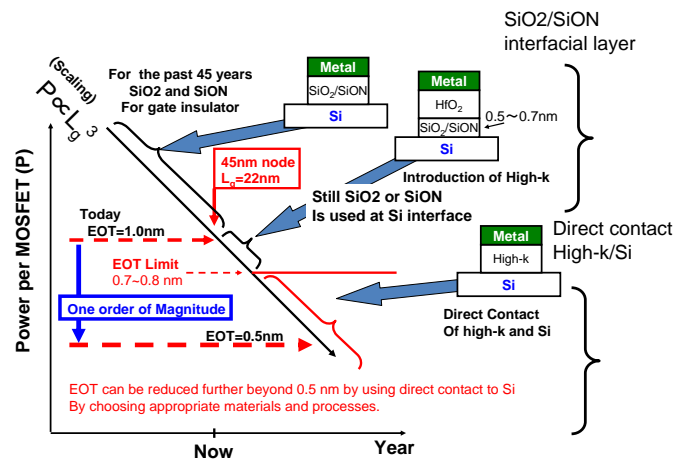
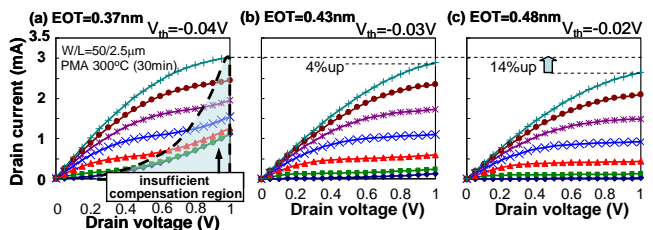


Fig. 6 Direct contact of high-k film to Si substrate



14% of I_d increase is observed even at saturation region

Fig. 7 MOSFET operation with EOT less than 0.4 nm

We have already experimentally confirmed a good operation of MOSFETs with EOT of 0.37 nm using the La_2O_3 gate insulator as shown in Fig 7 [3]. Thus, in future the EOT value predicted in the roadmap will decrease a little further to solve the problems, and then, the supply voltage would decrease further in order to suppress the short channel effects.

4 . Si nanowire FET

The planar logic CMOS devices will encounter its downsizing limit due to the huge off-leakage. In fact, according to ITRS 2009, planar MOSFETs will disappear from the advanced MOSFET structure, and 3D multiple gate (or Fin type) structure will be introduced because of its nature to easily suppress the SCE as shown in Fig. 8. It is a natural trend that the Fin FETs will change to nanowire FETs, because of more control of SCE and more channel surface in a unit area as shown also in the figure

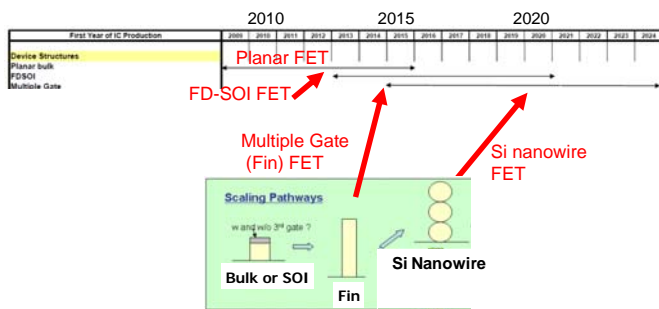


Fig. 8 MOSFET structure trend in ITRS 2009

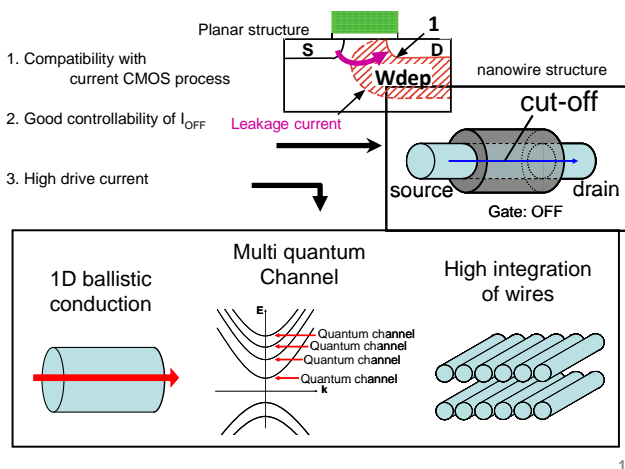


Fig. 9 Advantages of nanowire FET over planer

One of the big advantages of Si nanowire FETs are their compatibility with today's Si CMOS process. Si

nanowire FETs have advantages not only on the suppression of off-leakage current, but also on the on-current as shown in Fig. 8. Multi-layer nanowire [4] will increase the drain current density significantly. Because the nanowire pattern itself is simple, nano-inprint technology could be used for future high-density lithography with extremely small pitch.

Also, The Si nanowire FET has higher on-current conduction due to their quantum nature. If the ideal one dimensional ballistic conduction is realized for the nanowire, the nanowire itself has basically a high quantum conduction with very small freedom of carrier scattering. In addition, the channel current is multiplied with the number of the quantum channel available for the conduction.

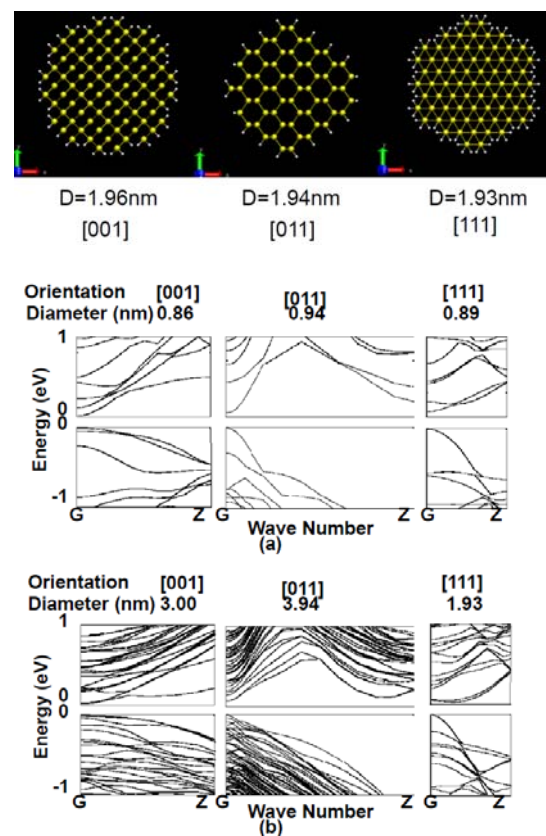


Fig. 10 Band structure for different width and orientation nanowire

With increasing the diameter of the nanowire, the number of the conduction band available significantly increases as shown in Fig. 10 [5]. However the increase of the quantum channel degrades the conduction because of the carrier scattering between the conduction bands, and there is a trade off relation between the one-dimensional

ballistic conduction and the number of quantum channel in terms of the nanowire width. Smaller wire diameter is desirable for one-dimensional ballistic conduction and larger diameter is desirable for the number of quantum channel.

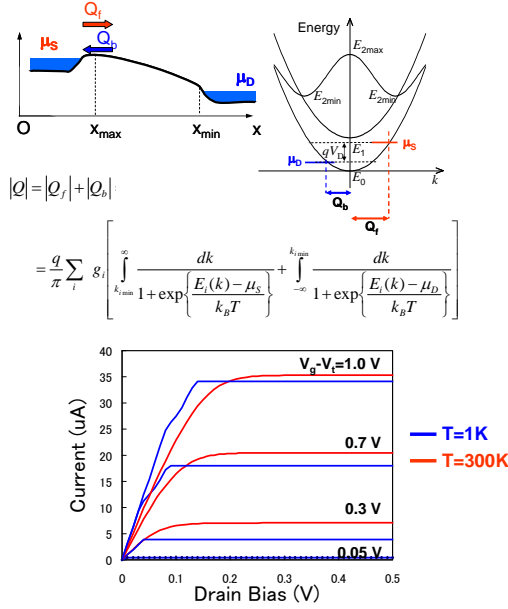


Fig. 11 Compact model for Si nanowire with ideal ballistic conduction and calculated Id-Vd characteristics

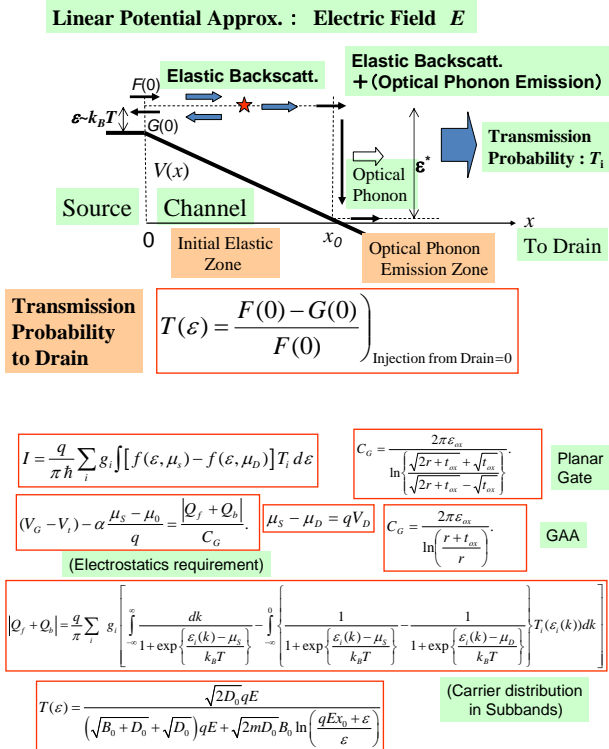


Fig. 12 Compact model for Si nanowire with carrier scattering

One of the big problems for introducing Si nanowire

FETs into the products is that there is no compact model to describe the Id-Vd characteristics of the MOSFETs for the circuit designers. Recently, primitive model under ideal ballistic conduction [6] and that with scattering [7,8] were published as shown in Figs. 11 and 12, respectively. Figure 13 shows the comparison of the calculated characteristics with ballistic conduction and scattering model. The calculation needs the E-k relation in the band structure, which is significantly affected by the nanowire diameter and orientation. It would take several more years to describe the Id-Vd characteristics with nanowire diameter and orientation dependence.

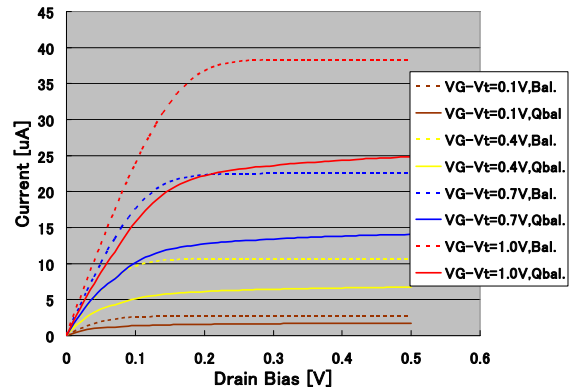


Fig.13 Comparison of the calculated Id-Vd characteristics with ballistic conduction (broken line) and scattering (solid line) model.

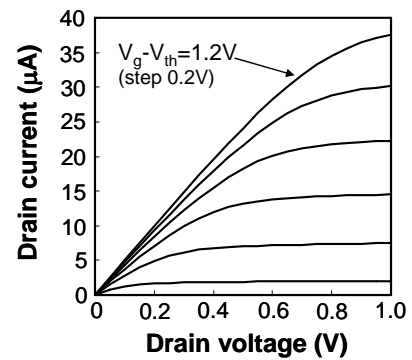


Fig. 14 Experimental results of Id-Vs characteristics of Si nanowire FET with 10 nm diameter with gate length 200 nm and gate oxide thickness 3 nm

Experimental results of Si nanowire FETs show extremely high drain current with good off-leakage control as shown in Fig. 14 [9]. Furthermore, recent experimental data shows very good potential for the Si nanowire FET as

shown in Fig. 15 [10]. Based on those result, nanowire FET will have much higher on-current which is predicted in ITRS for future planar, SOI and multiple gate MOSFETs.

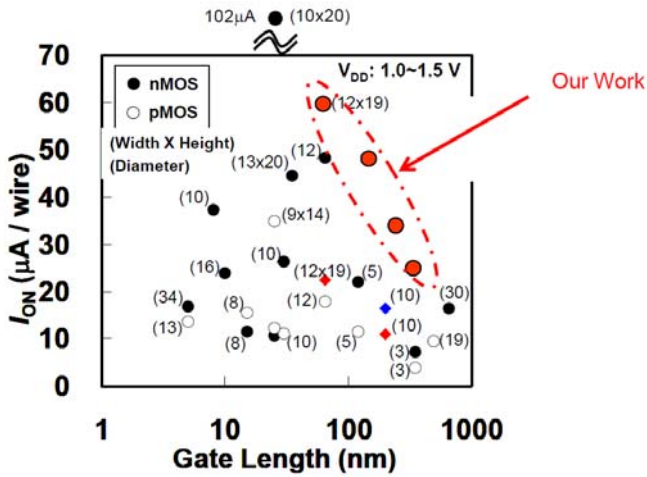


Fig. 15 Bench mark of published nanowire FET drain current and our recent work.

5 . Long term future perspective

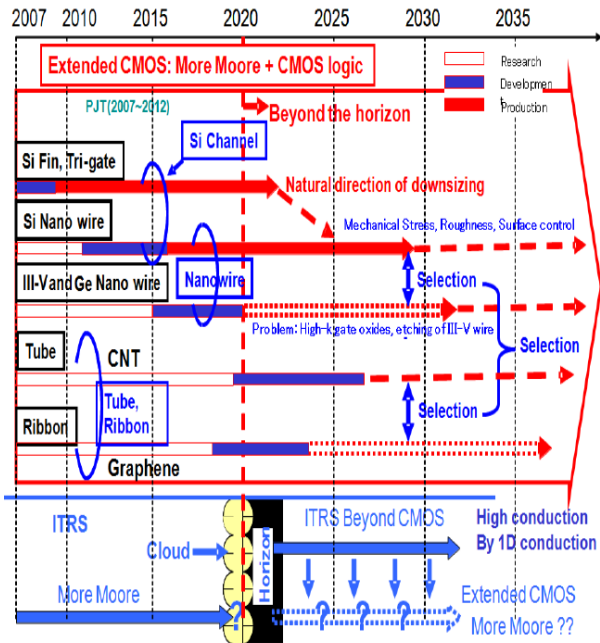


Fig. 16 Long term road map

Figure 16 [11] shows a long range roadmap including the period which ITRS does not covers. The Si nanowire FETs is the most promising candidate as explained. III-V and Ge nanowire FETs are the 2nd candidate, which could replace Si nanowire FETs. However, technical barrier for the fabrication process is much higher compared with the Si nanowire at this moment. In further future, CNTs (Carbon Nanowire Transistor) and graphene ribbon FETs could be candidates to replace the Si nanowire FETs. However, they are still too far to say at this moment because of no substantial idea for the integration method of so huge number transistors in a chip and bandgap control for high on/off ratio.

7 .Acknowledgement

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