Past and future of Si integrated circuit device technologies

IEEE EDS Mini Colloquium

@Institute for Microelectronics Stuttgart (IMS-CHIPS), Stuttgart, Germany

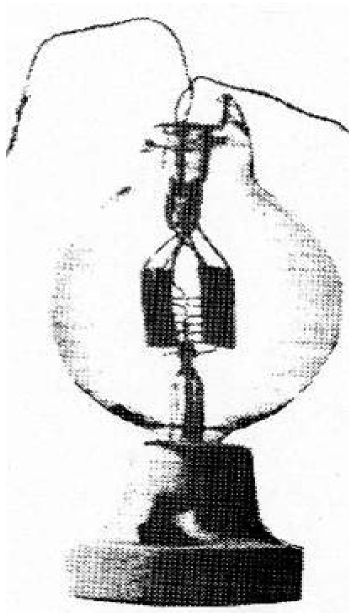
June 7, 2010

Frontier Research Center

Tokyo Institute of Technology, Yokohama, Japan

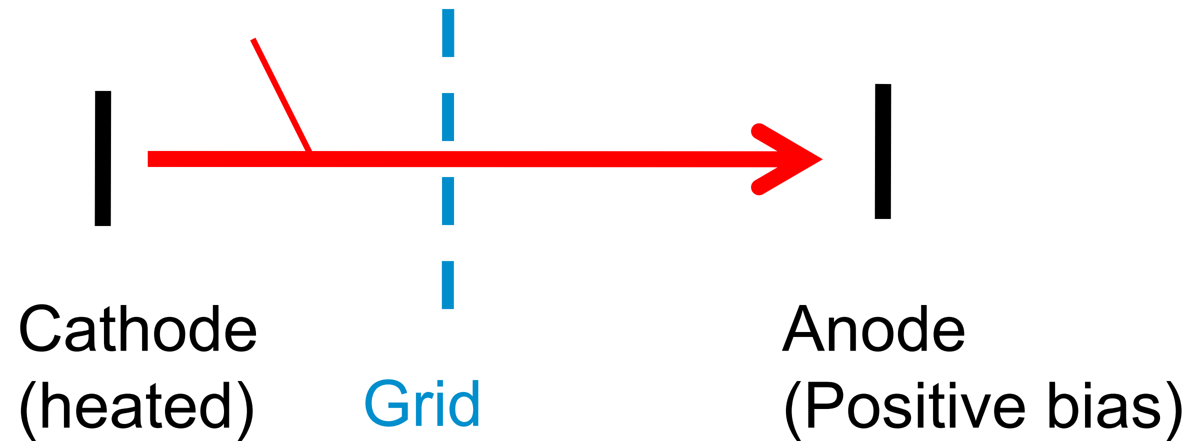
Hiroshi Iwai

Lee De Forest



Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias



Same mechanism as that of transistor

First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

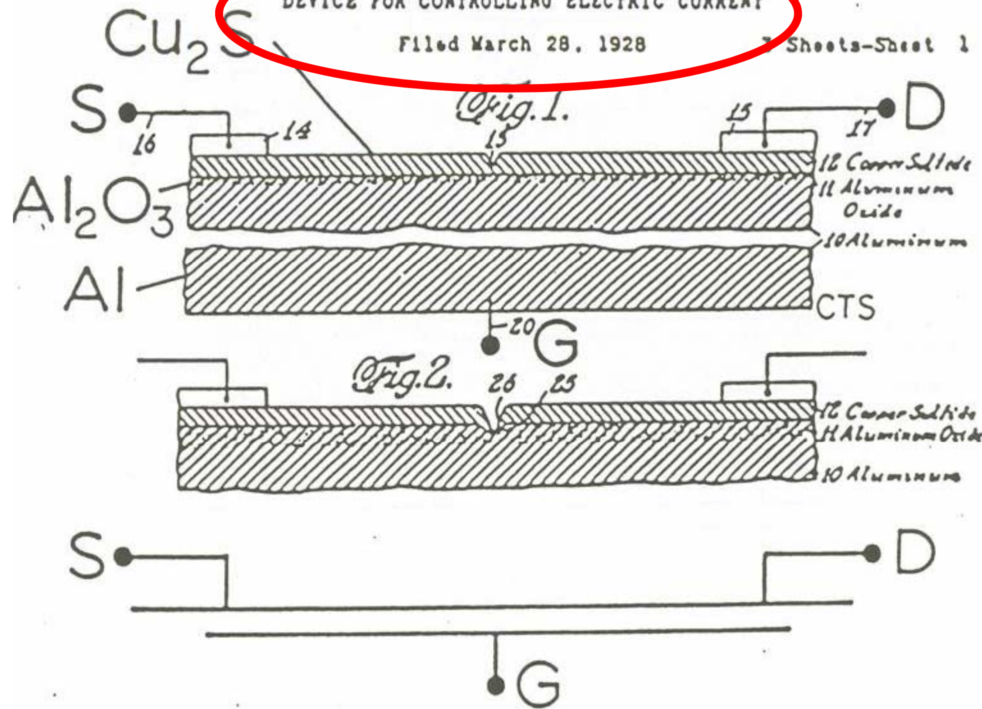
→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

J. E. LILIENFELD

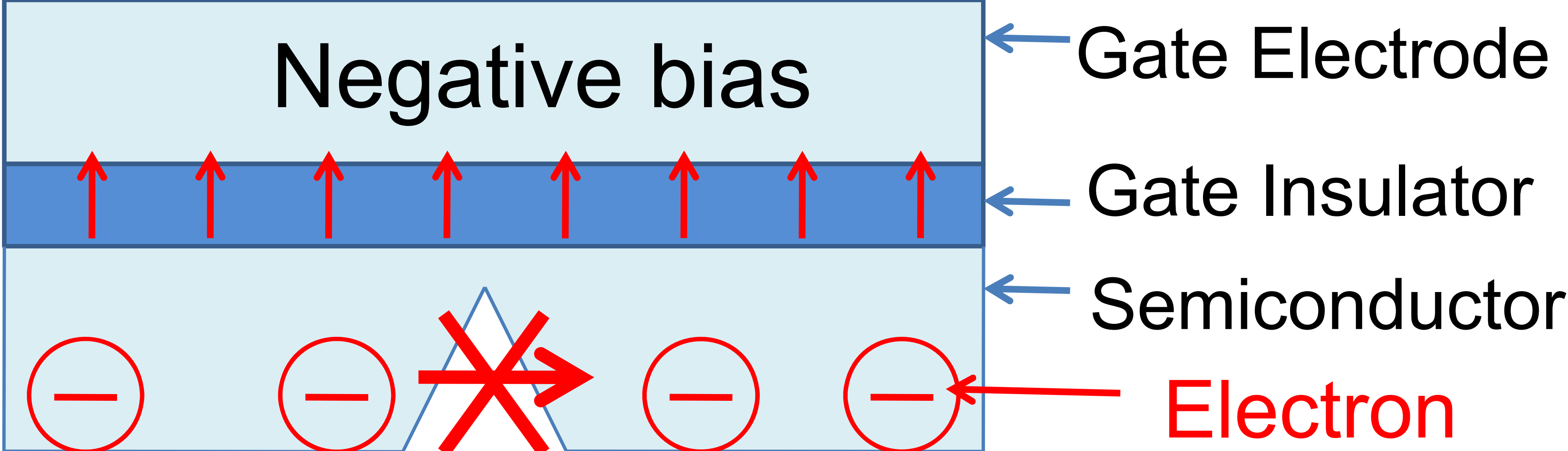
DEVICES FOR CONTROLLED ELECTRIC CURRENT

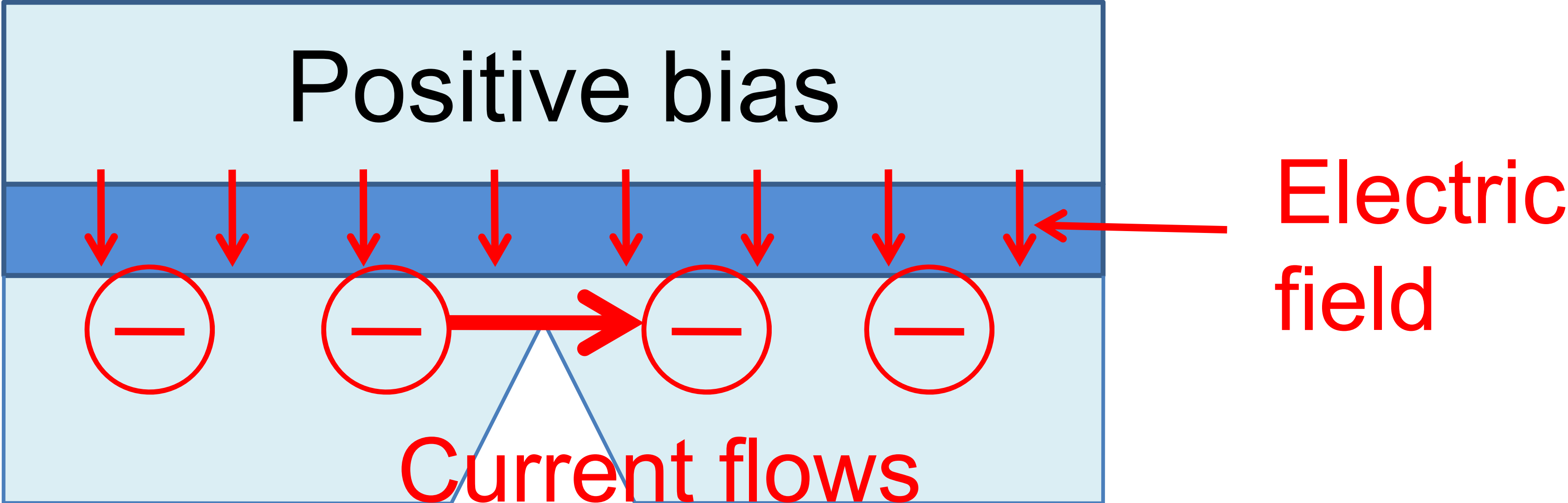
Filed March 28, 1928



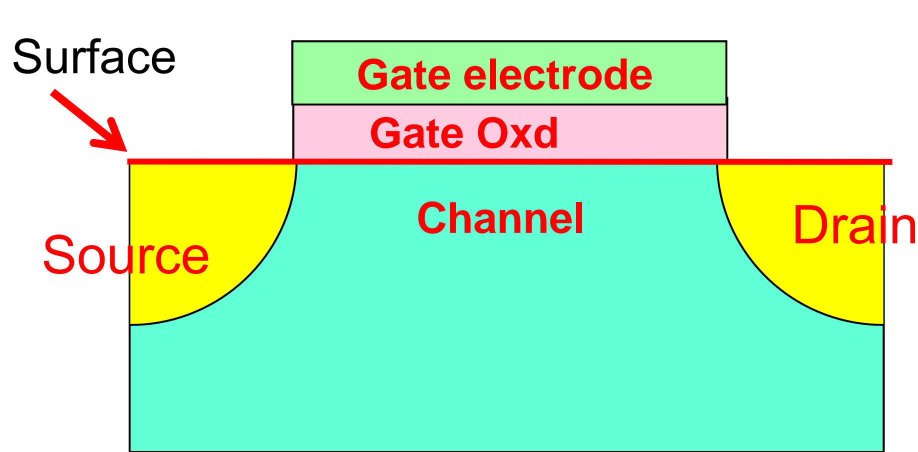
J.E.LILIENFELD

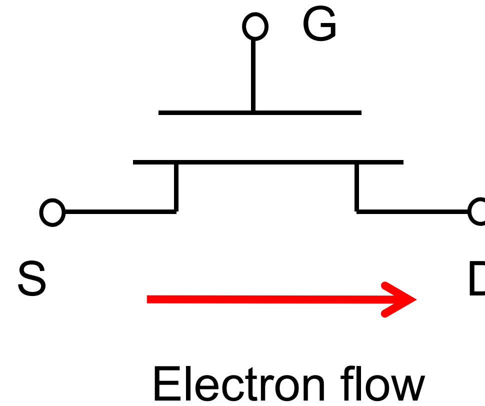
Capacitor structure with notch





Today's transistor: MOSFET for CMOS LSI

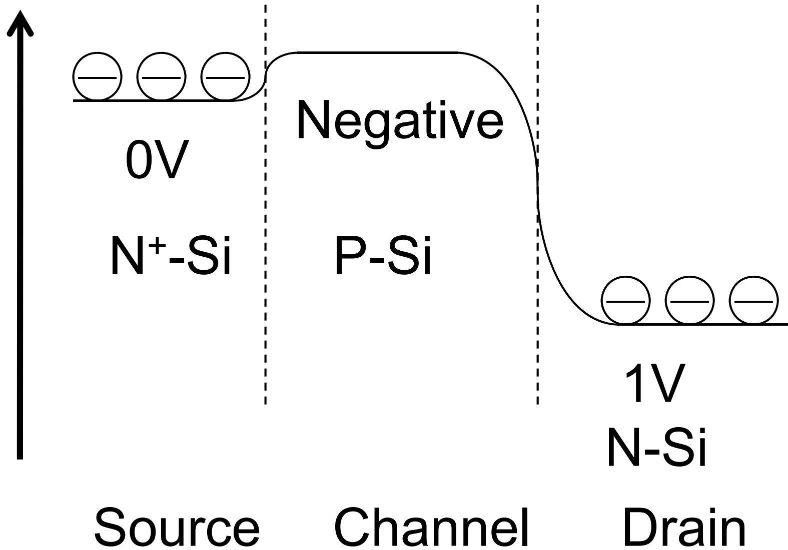


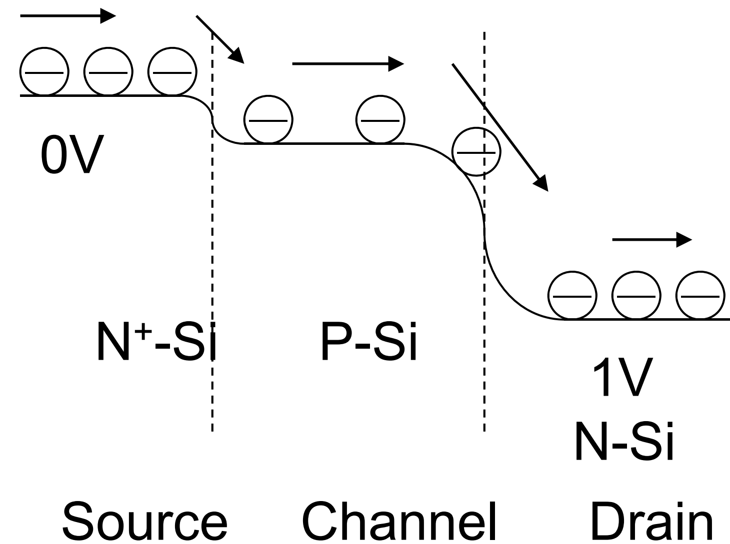


0 bias for gate

Positive bias for gate

Surface Potential (Negative direction)



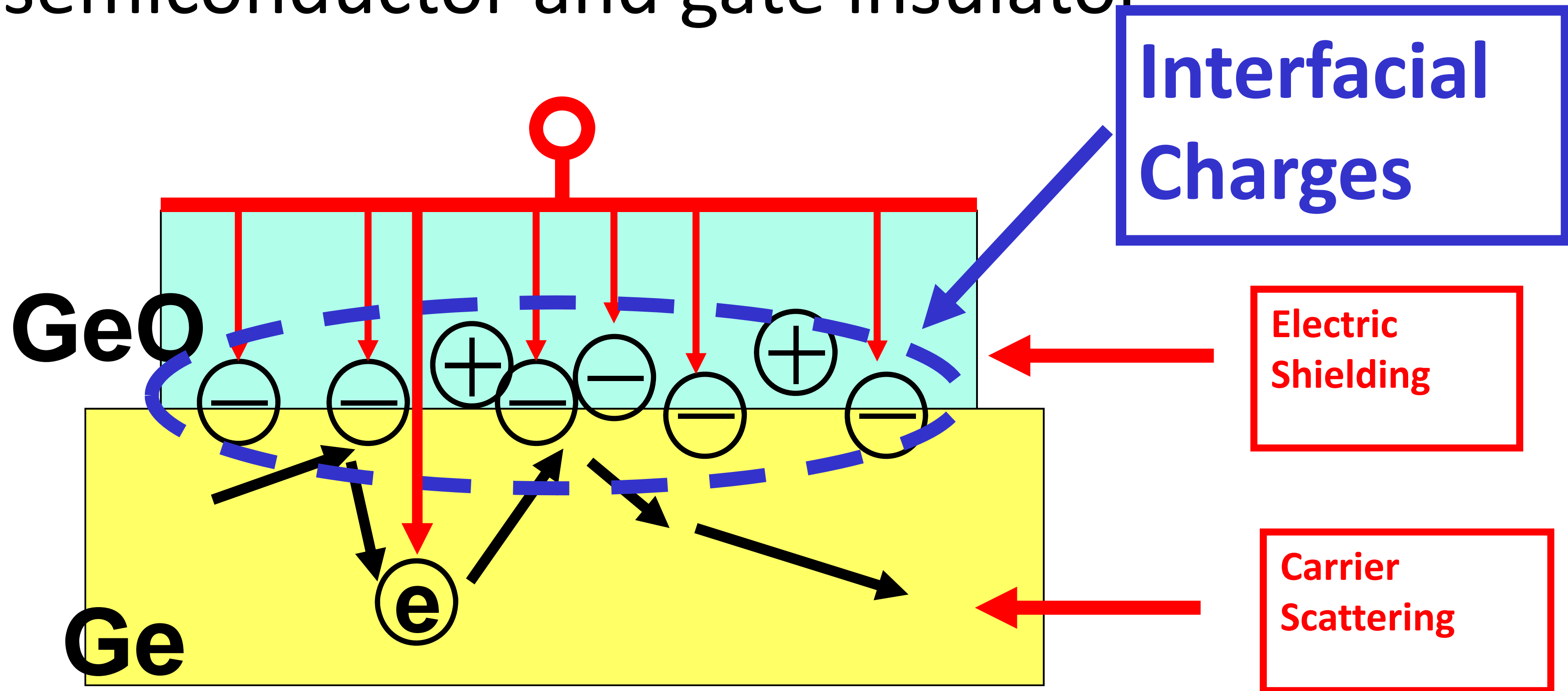


However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!

Very bad interface property between the semiconductor and gate insulator



Drain Current was several orders of magnitude smaller than expected

Even Shockley!

However, they found amplification phenomenon when investigating Ge surface when putting needles.
This is the 1st Transistor:
Not Field Effect Transistor,
But Bipolar Transistor (another mechanism)

1947: 1st transistor

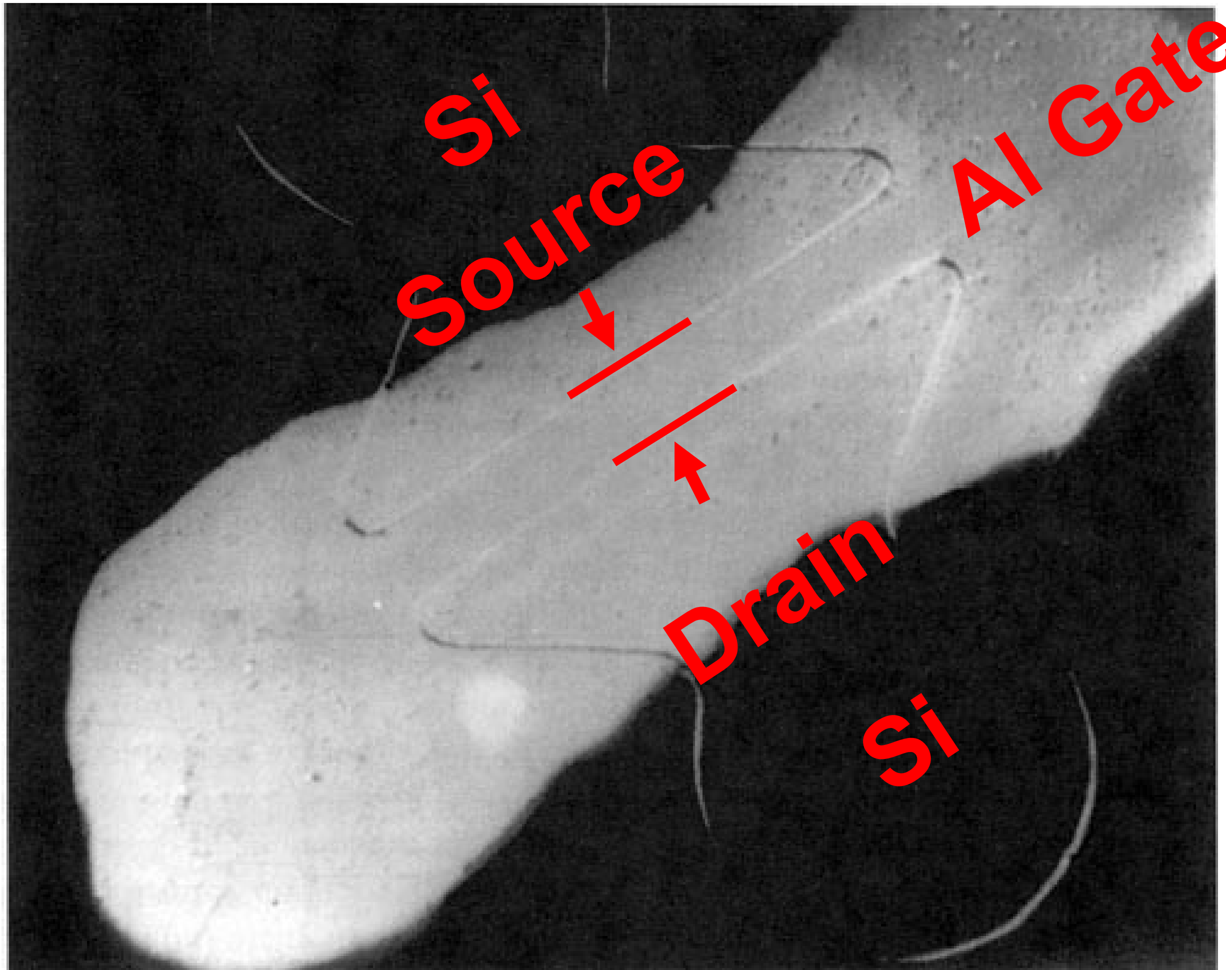
J. Bardeen W. Bratten,

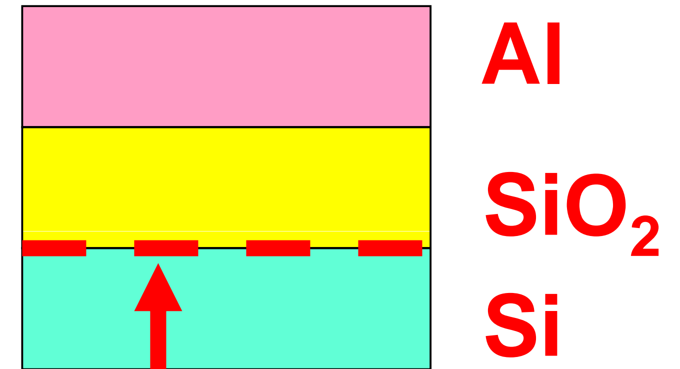
Bipolar using Ge

W. Shockley

1960: First MOSFET
by D. Kahng and M. Atalla

Top View

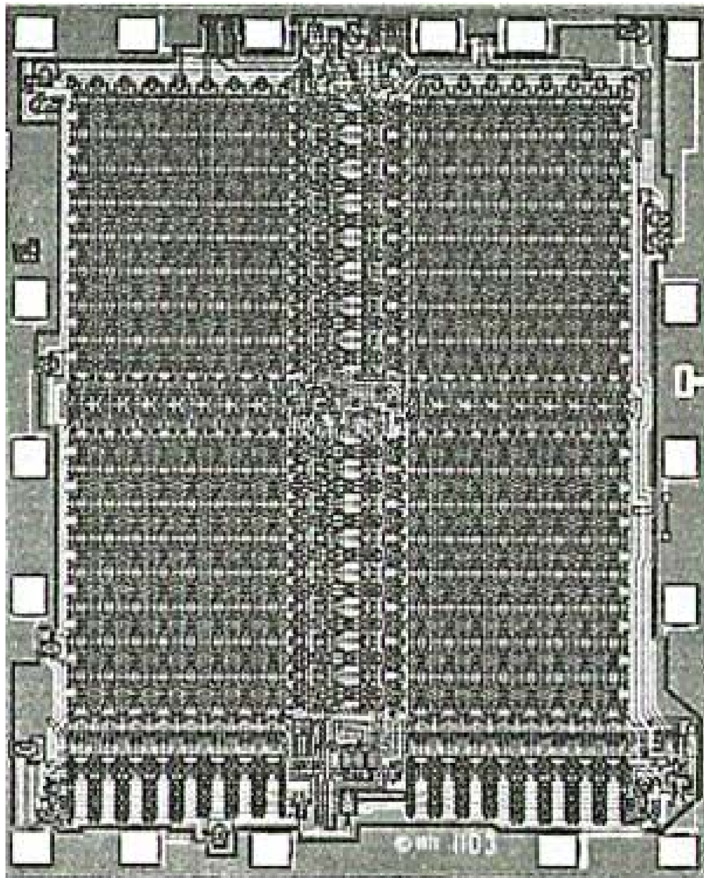


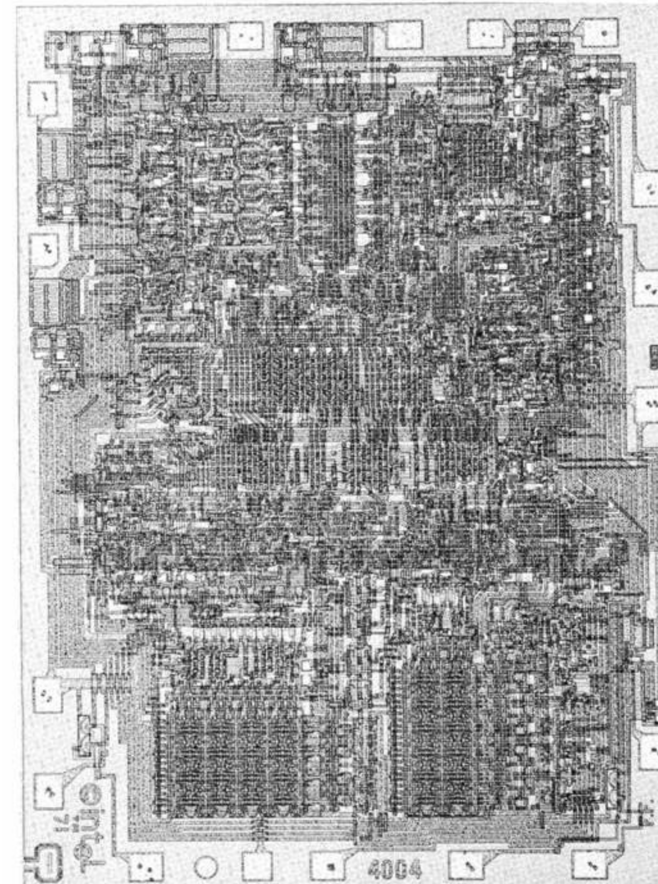


Si/SiO2 Interface is extraordinarily good

1970,71: 1st generation of LSIs

DRAM Intel 1103 **MPU Intel 4004**





Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

→ **Increase clock frequency**

→ **Increase circuit operation speed**

2. **Increase number of Transistors**

→ **Parallel processing**

→ **Increase circuit operation speed**

Downsizing contribute to the performance increase in double ways

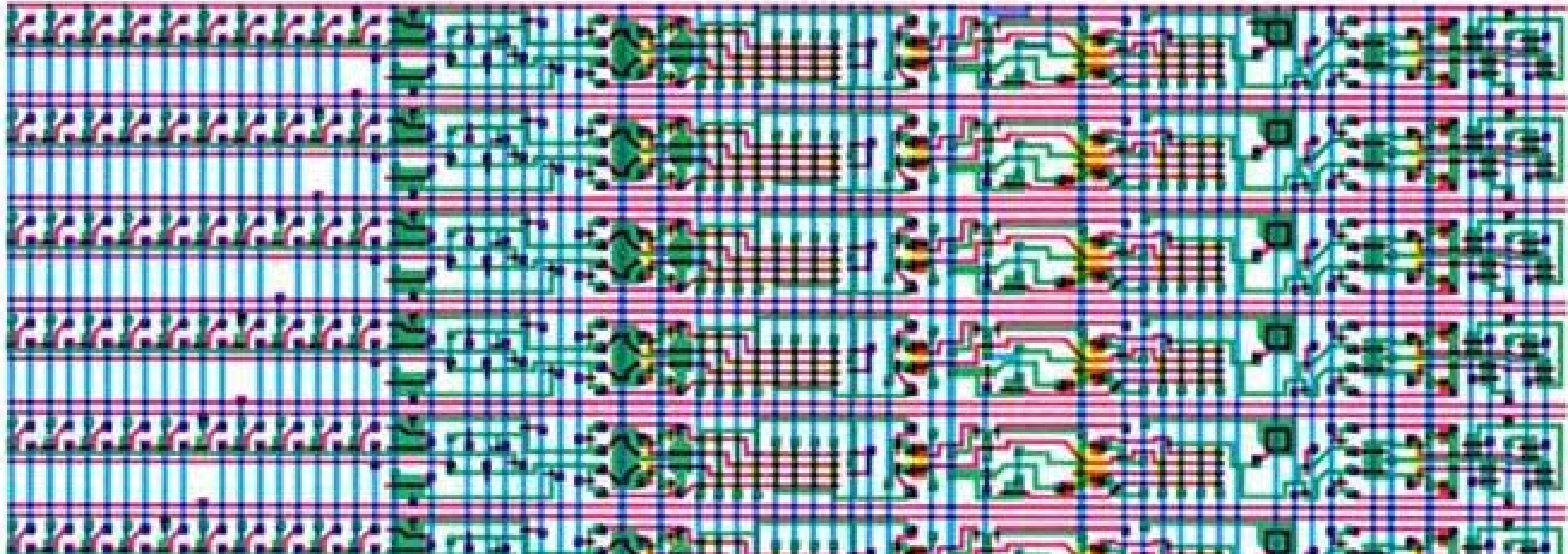
Thus, downsizing of Si devices is the most important and critical issue.

Many people wanted to say about the limit.
Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

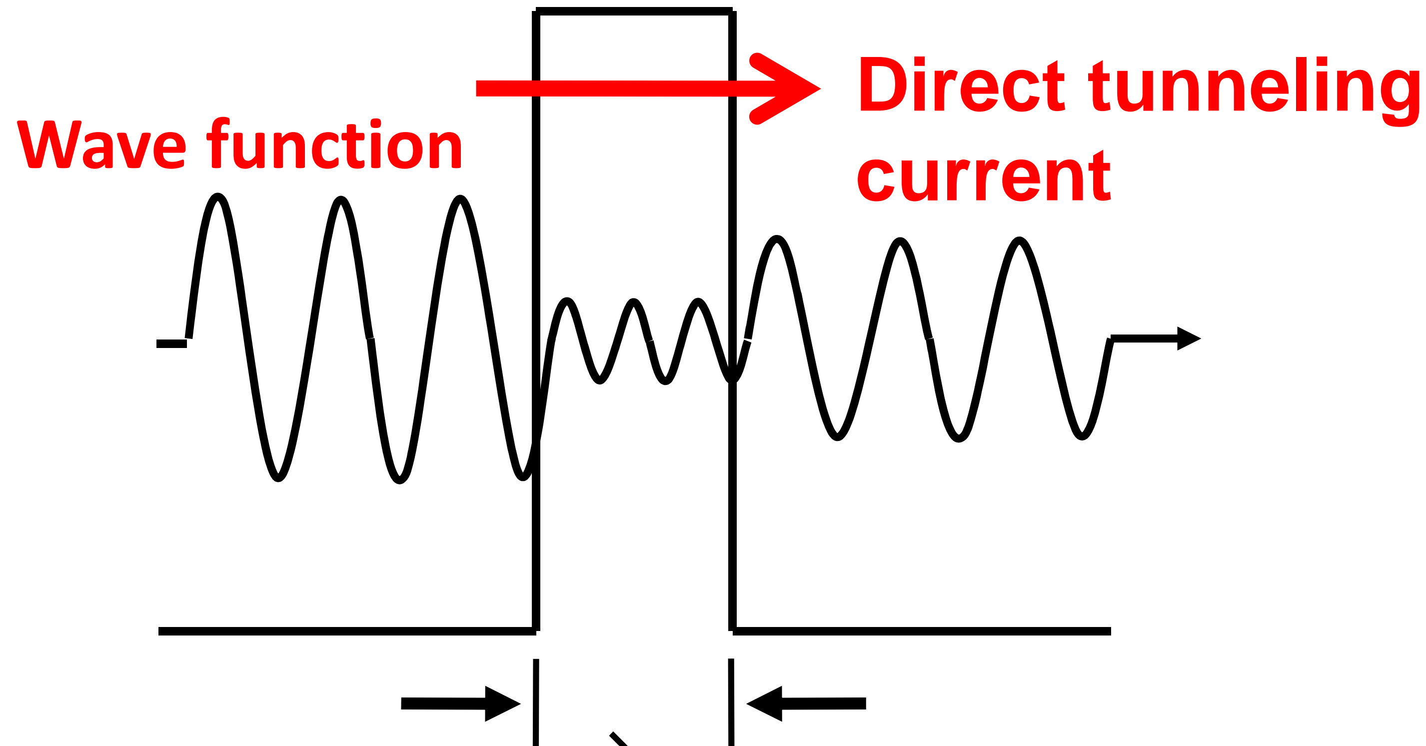
VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.

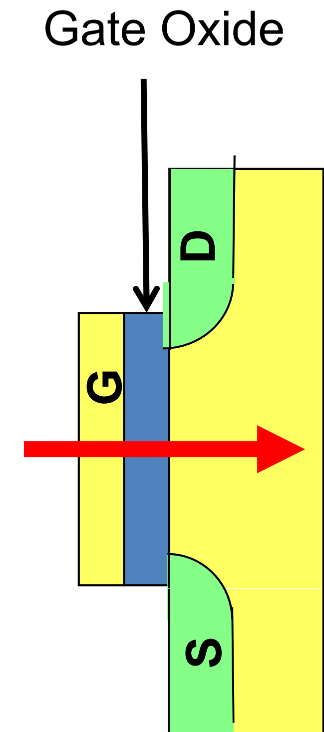


VLSI textbook

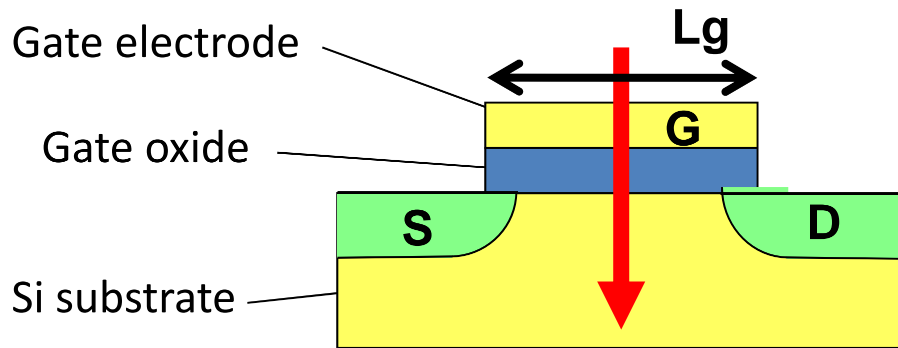
Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.

Direct-tunneling effect



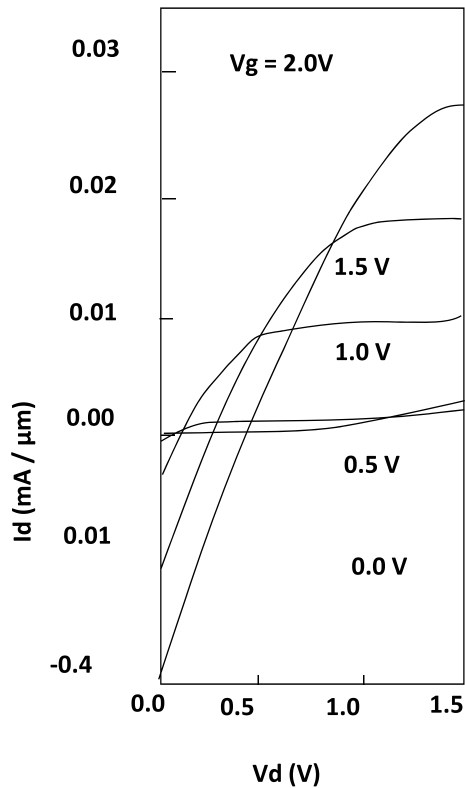


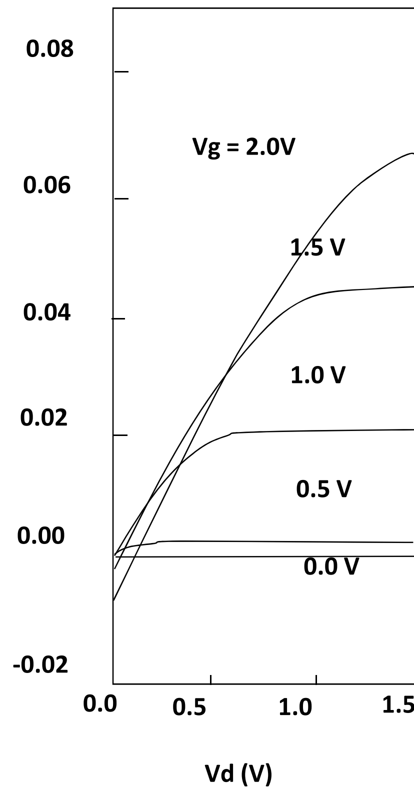
Direct tunneling leakage current start to flow when the thickness is 3 nm.

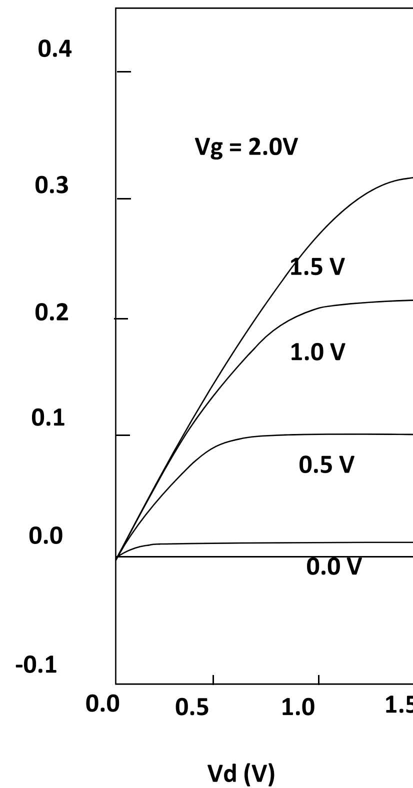


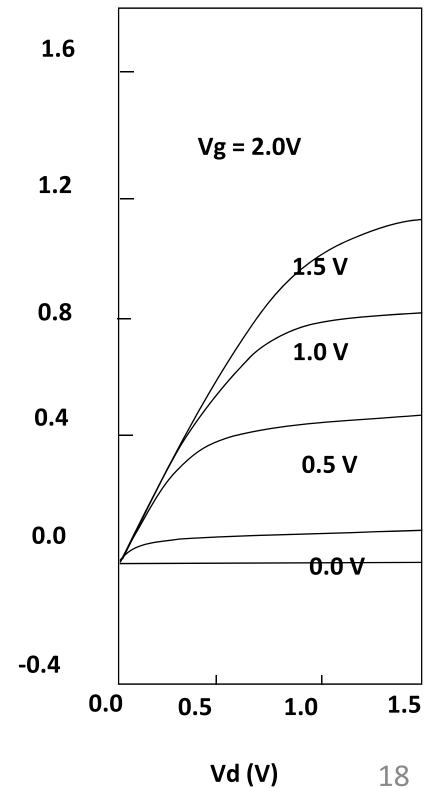
Direct tunneling leakage was found to be OK! In 1994!

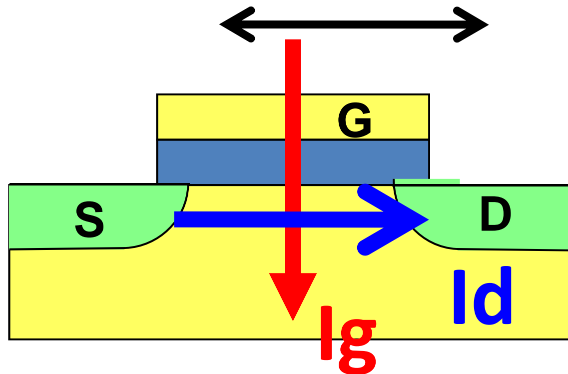
MOSFETs with 1.5 nm gate oxide











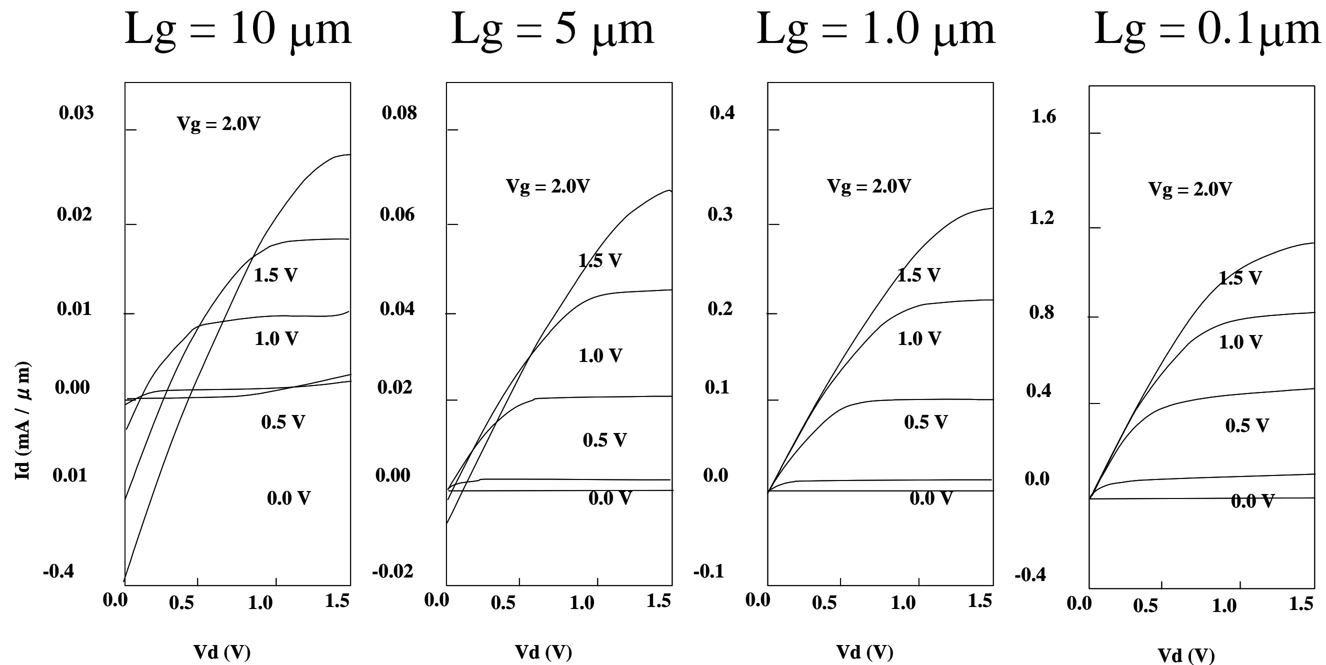
Gate leakage: Ig $\propto$ Gate Area $\propto$ Gate length (Lg)

Drain current: Id $\propto$ 1/Gate length (Lg)

Lg → small,

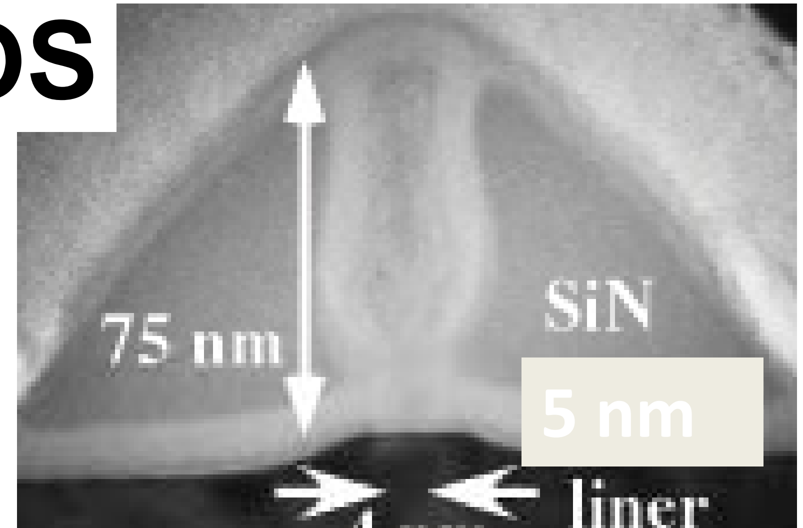
Then, Ig → small, Id → large, Thus, Ig/Id → very small

Id

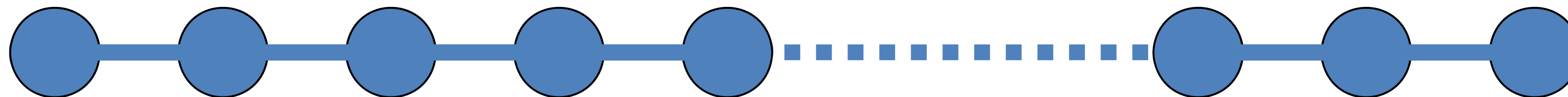


5 nm gate length CMOS

Is a Real Nano Device!!

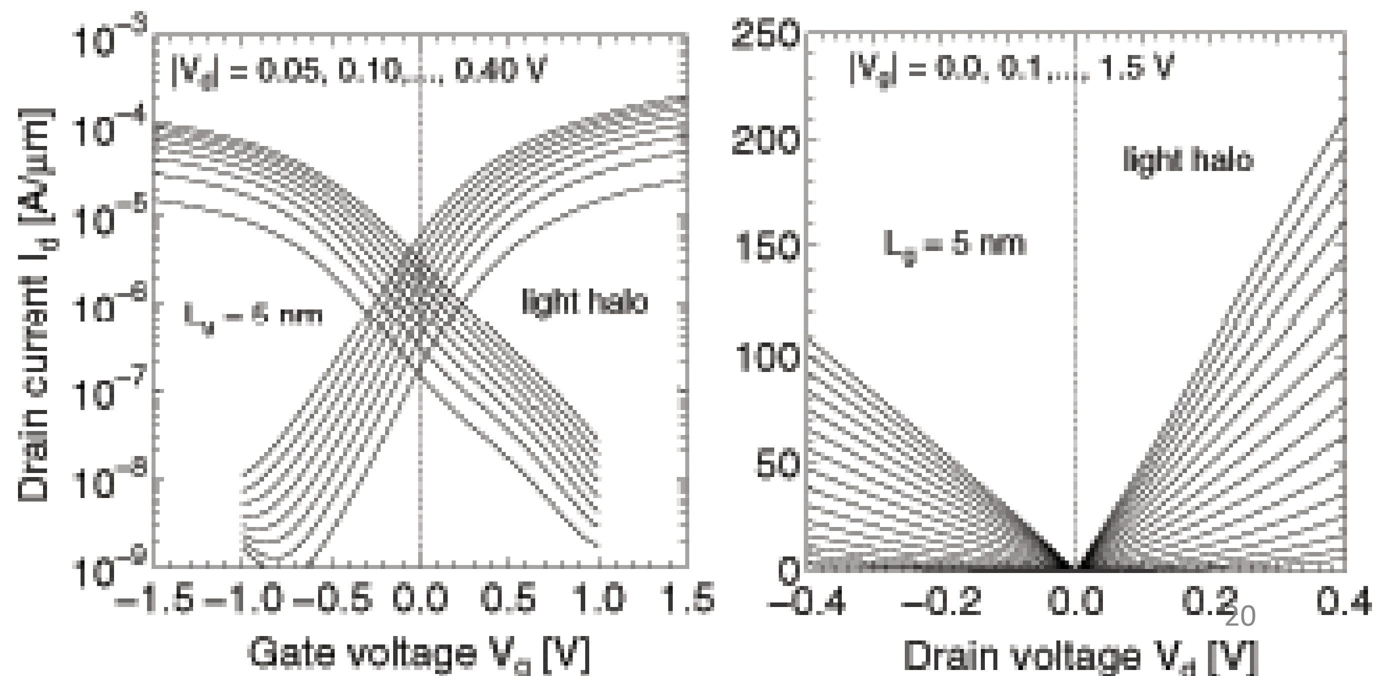


Length of 18 Si atoms



H. Wakabayashi
et.al, NEC

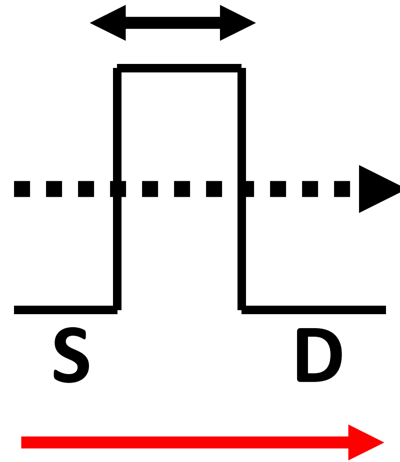
IEDM, 2003



Predictied limit now

Tunneling distance

3 nm



MOSFET operation

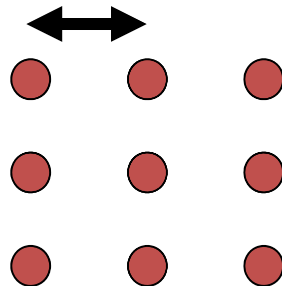
Lg = 3 nm?

Below this, no one knows future!

Ultimate Limit

Atom distance

0.3 nm



3 important items for *More* Moore

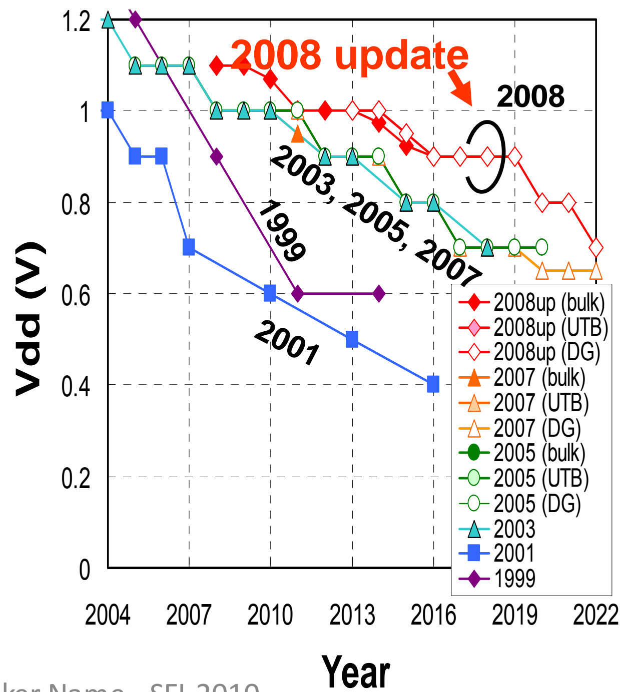
1. Scaling of high-k beyond 0.5 nm

2. Metal S/D

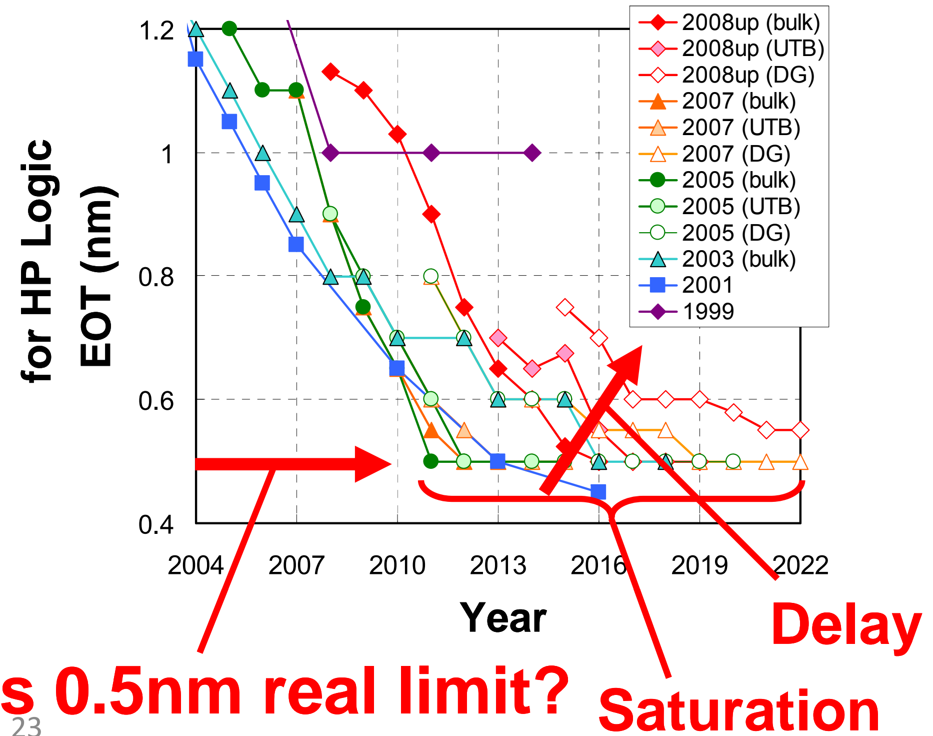
3. Si-Nanowire FET

ITRS

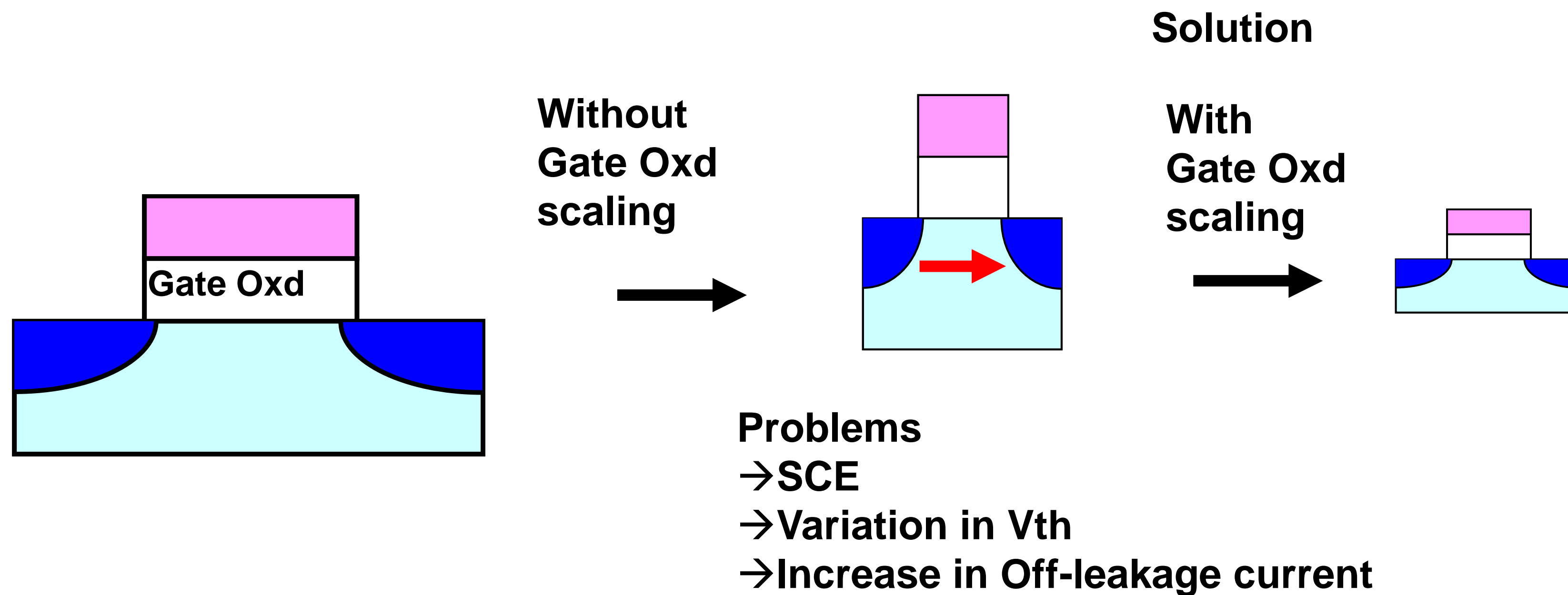
Vdd stay high



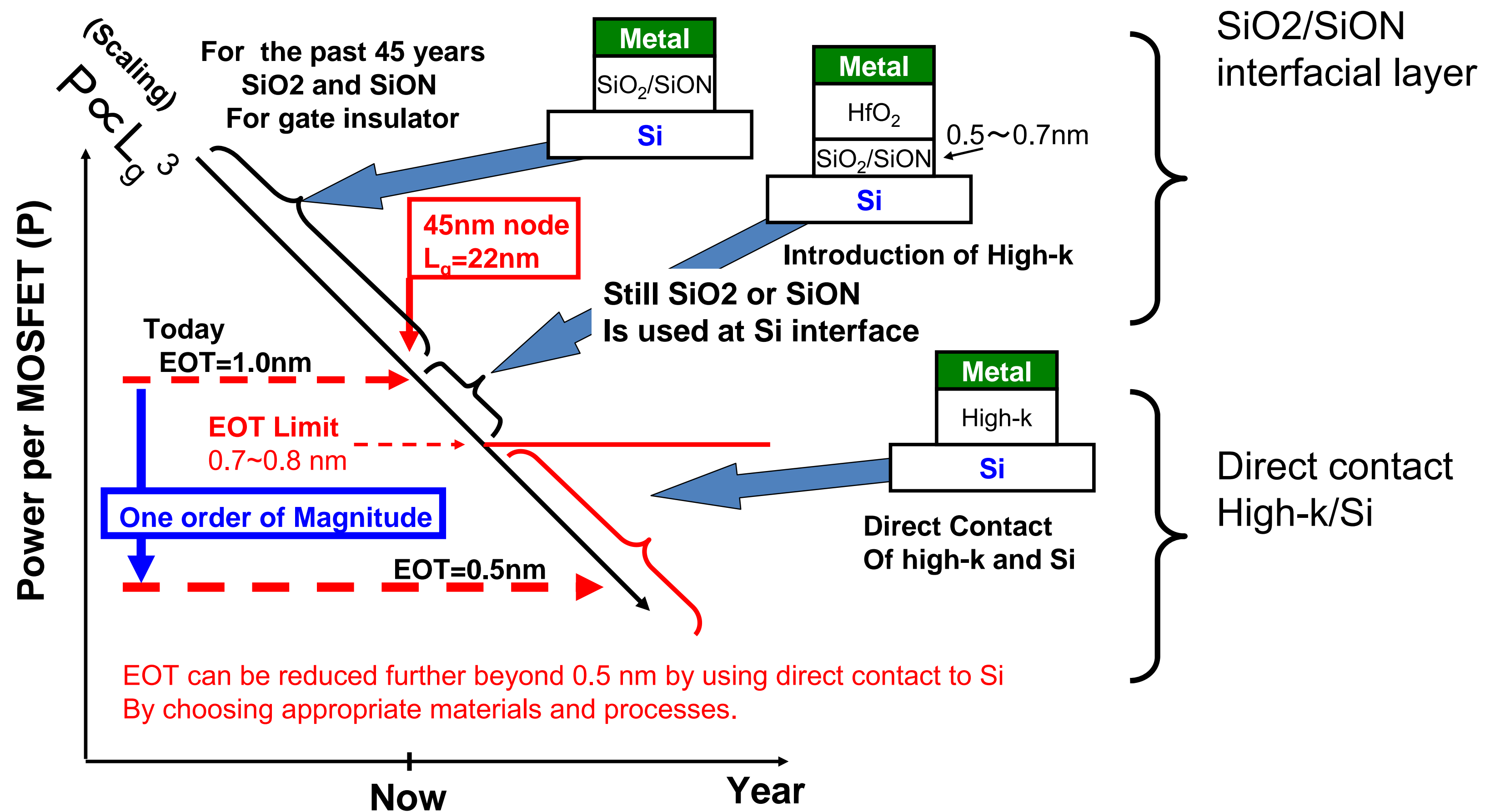
ITRS EOT limit = 0.5 nm?



Scaling of high beyond 0.5 nm is important



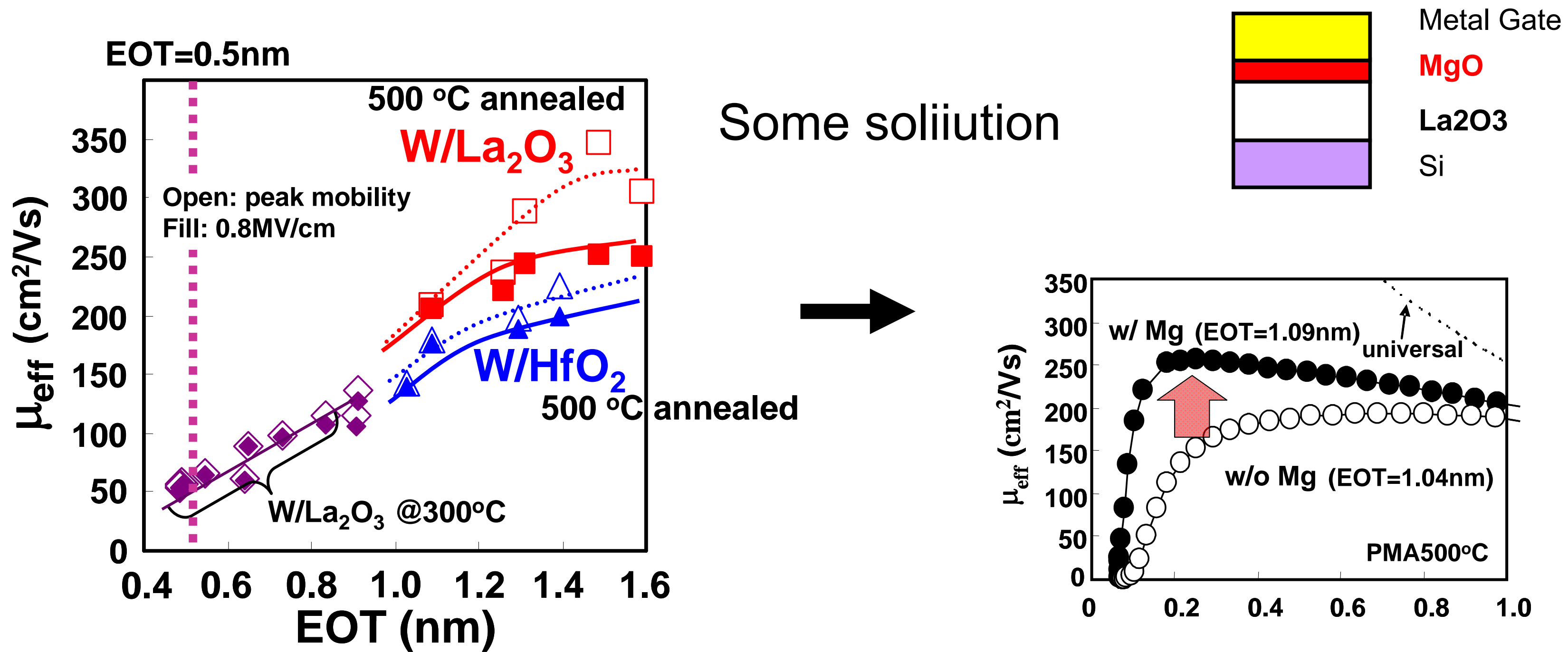
Direct contact of high-k to Si



Challenge for thinning High-k

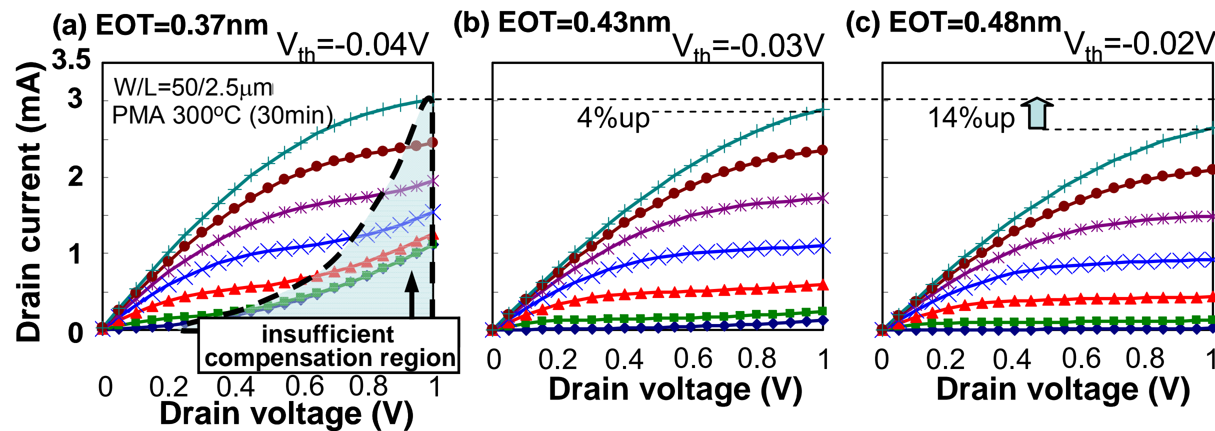
Degradation of mobility

Some soliiution

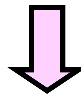


Challenge to EOT~0.3nm

EOT<0.5nm with Gain in Drive Current

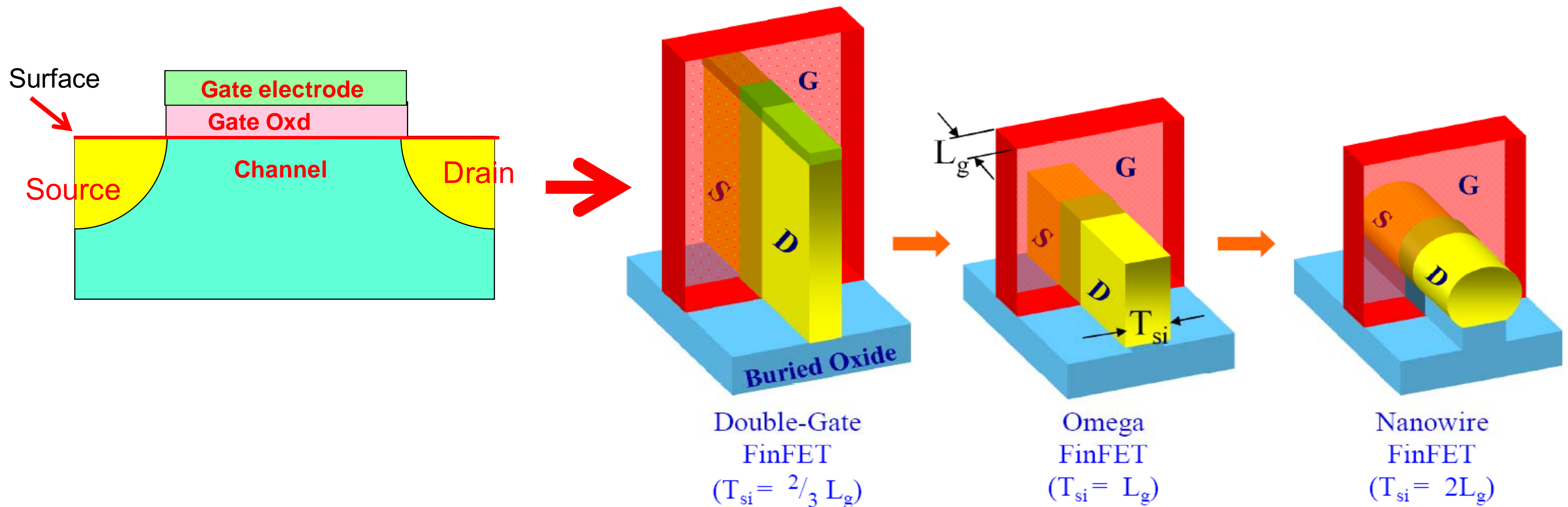


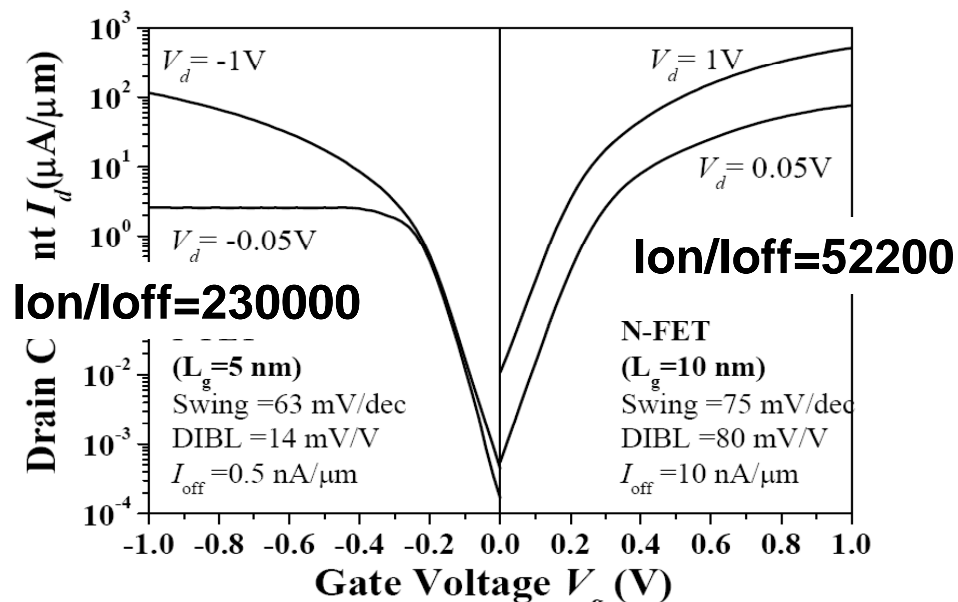
14% of I_d increase is observed even at saturation region

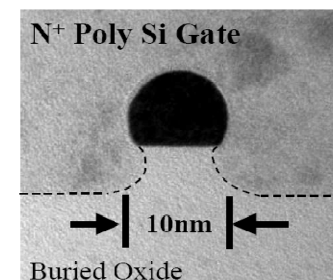


EOT below 0.4nm is still useful for scaling

FinFET to Nanowire



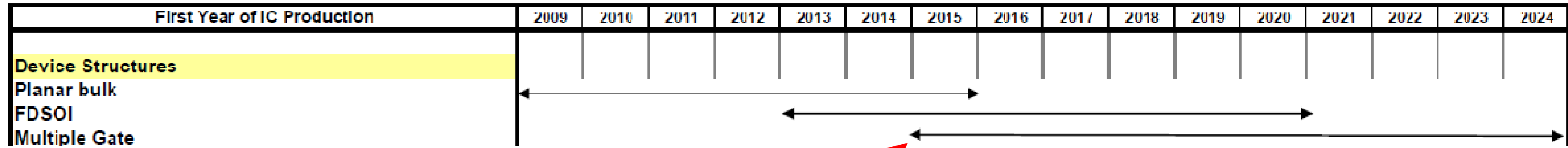




Channel conductance is well controlled by Gate even at L=5nm

F.-L.Yang, VLSI2004

Nanowire FET

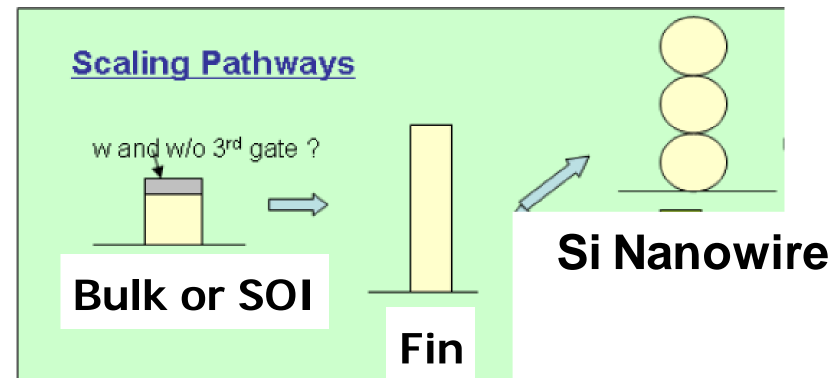


Nanowire FET

Multiple Gate (Fin)FET

ITRS 2009

Bulk → Fin → Nanowire

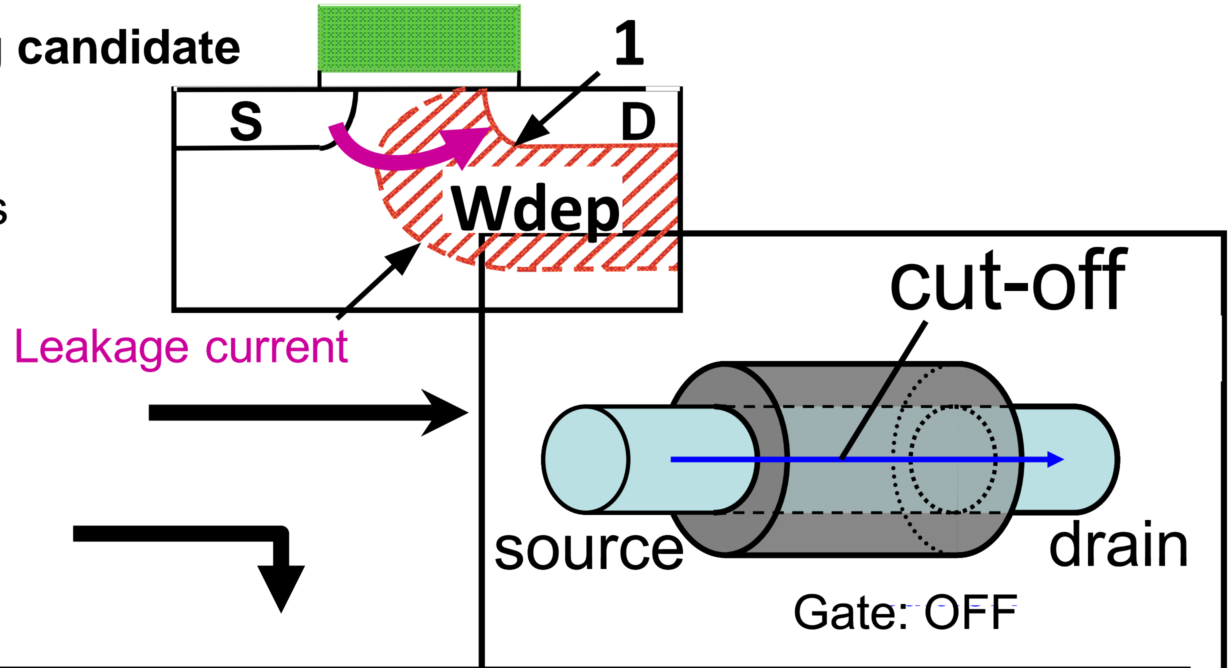


Si nanowire FET as a strong candidate

1. Compatibility with
   current CMOS process

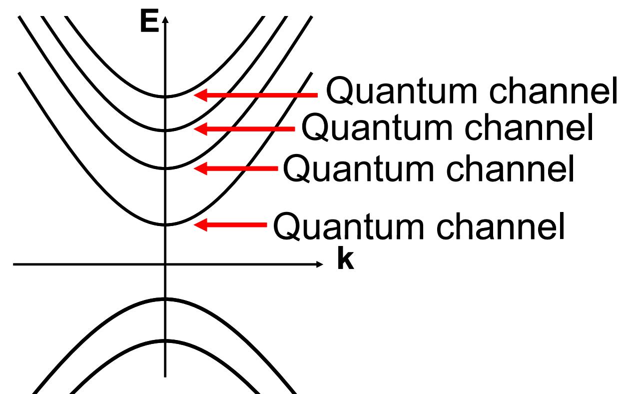
2. Good controllability of I_{OFF}

3. High drive current

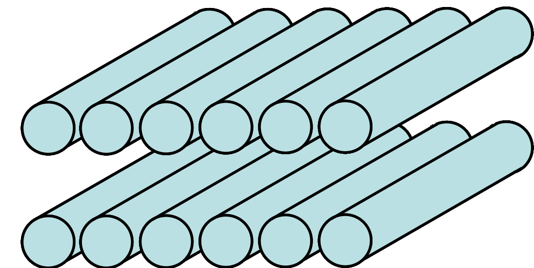


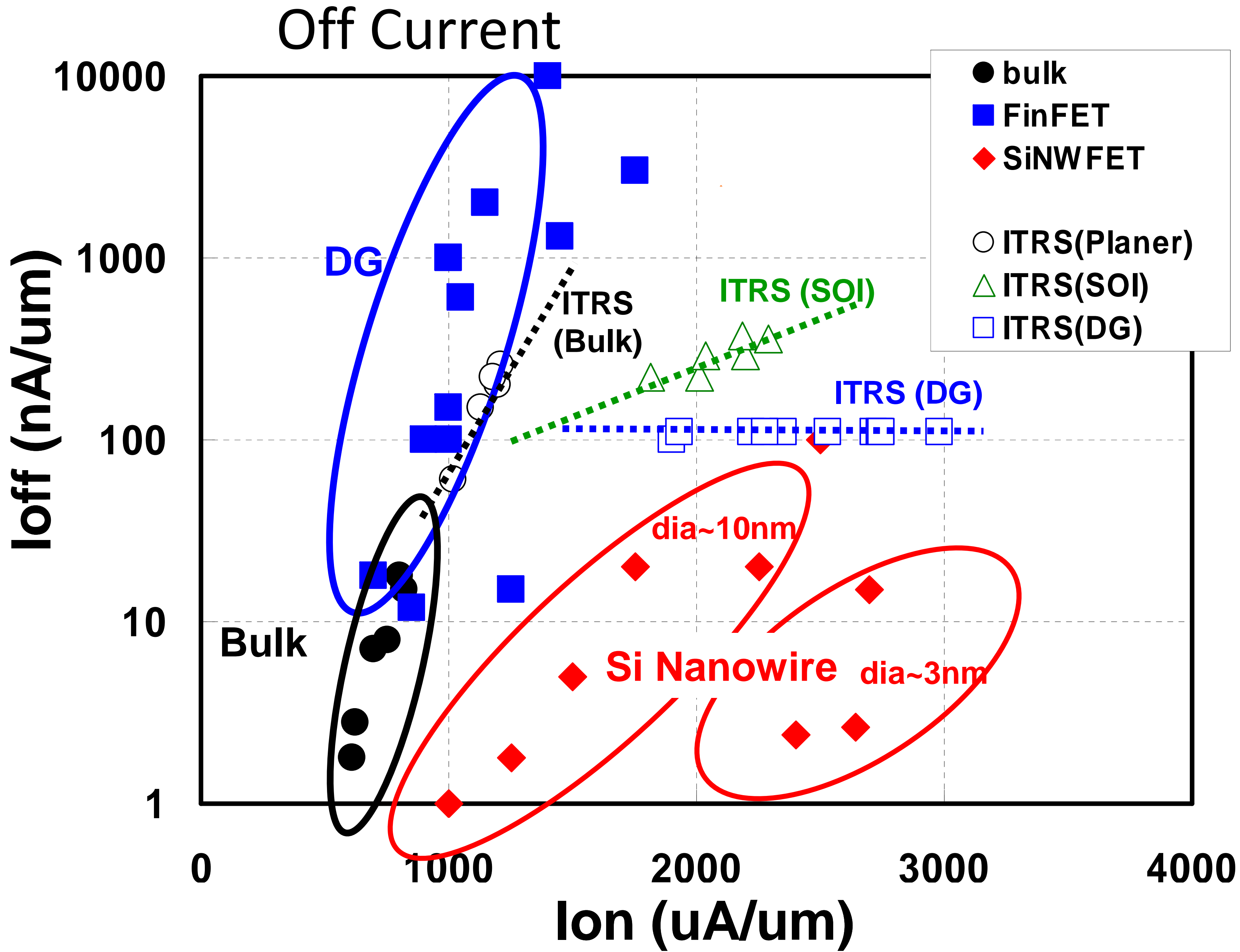
Multi quantum Channel

1D ballistic conduction



High integration of wires

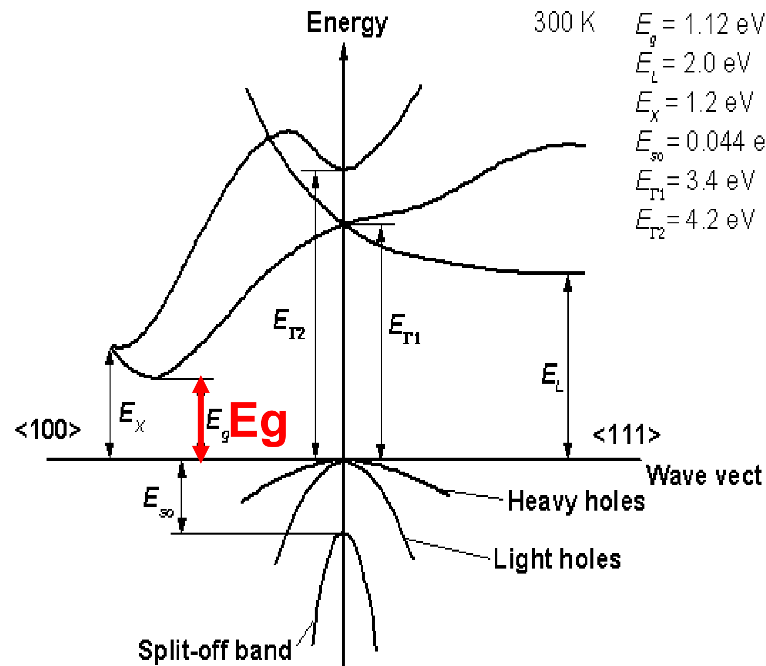




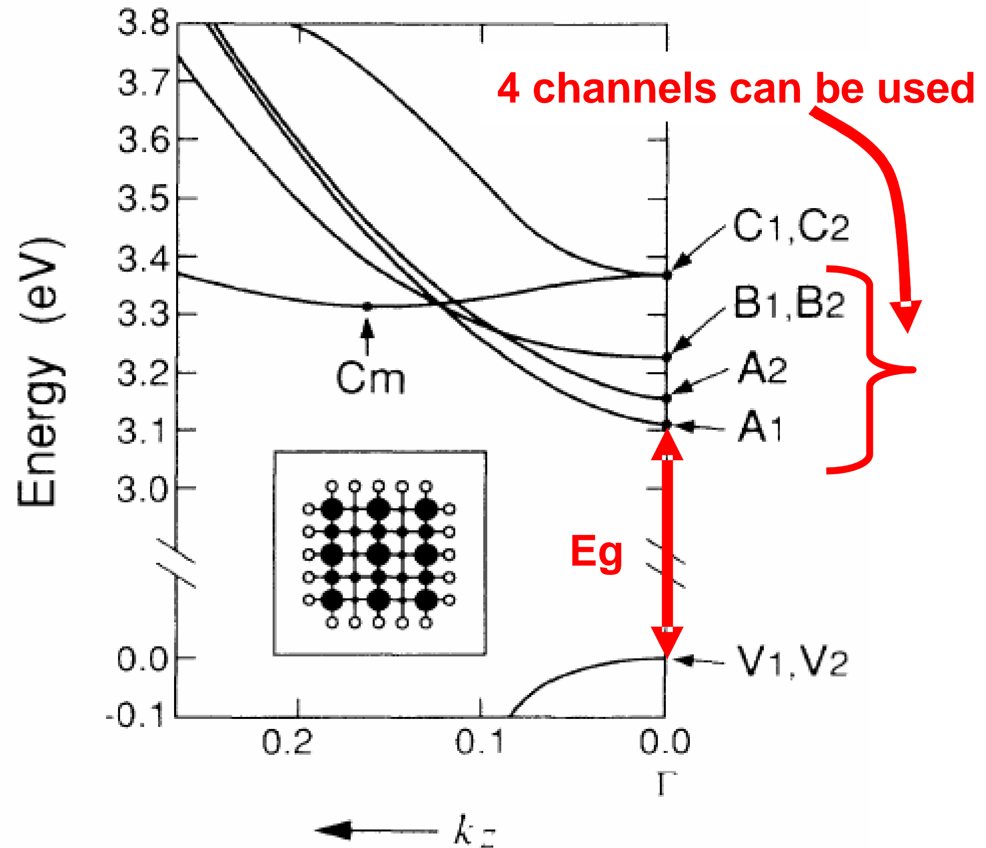
Off Current
10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS (Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



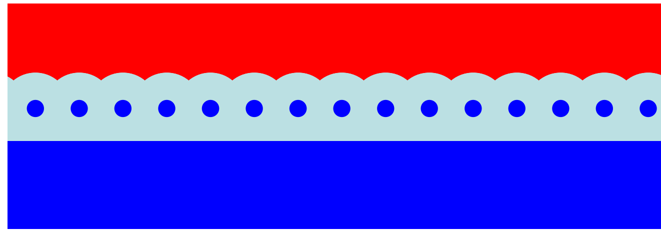
Energy band of Bulk Si



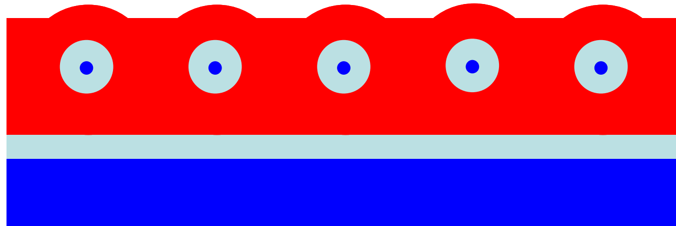
Energy band of 3 x 3 Si wire

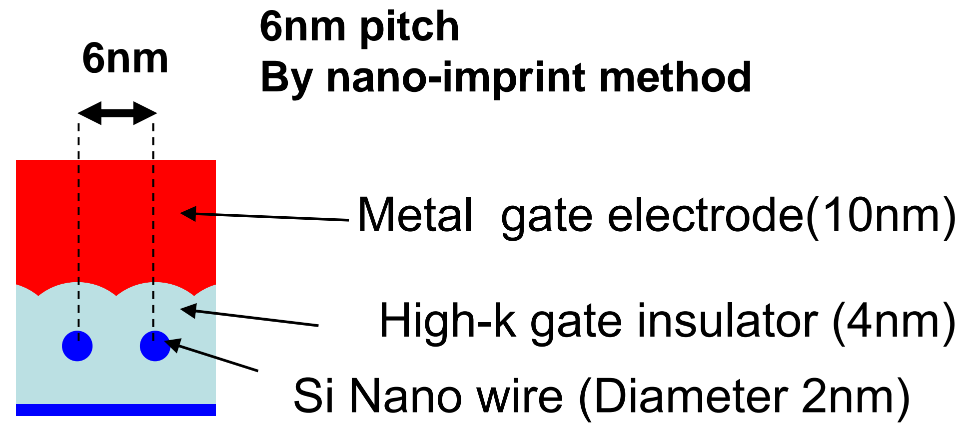
Maximum number of wires per 1 μm

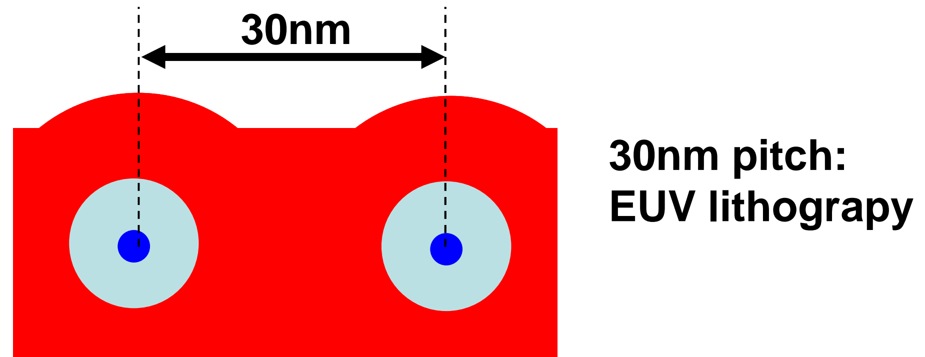
Front gate type MOS 165 wires /μm

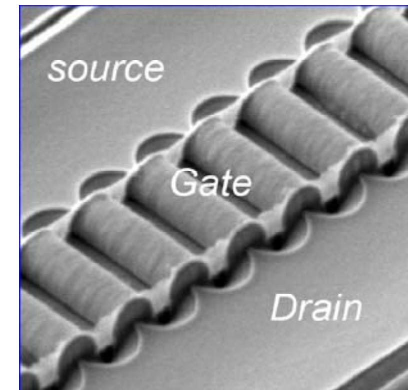


Surrounded gate type MOS 33 wires/μm



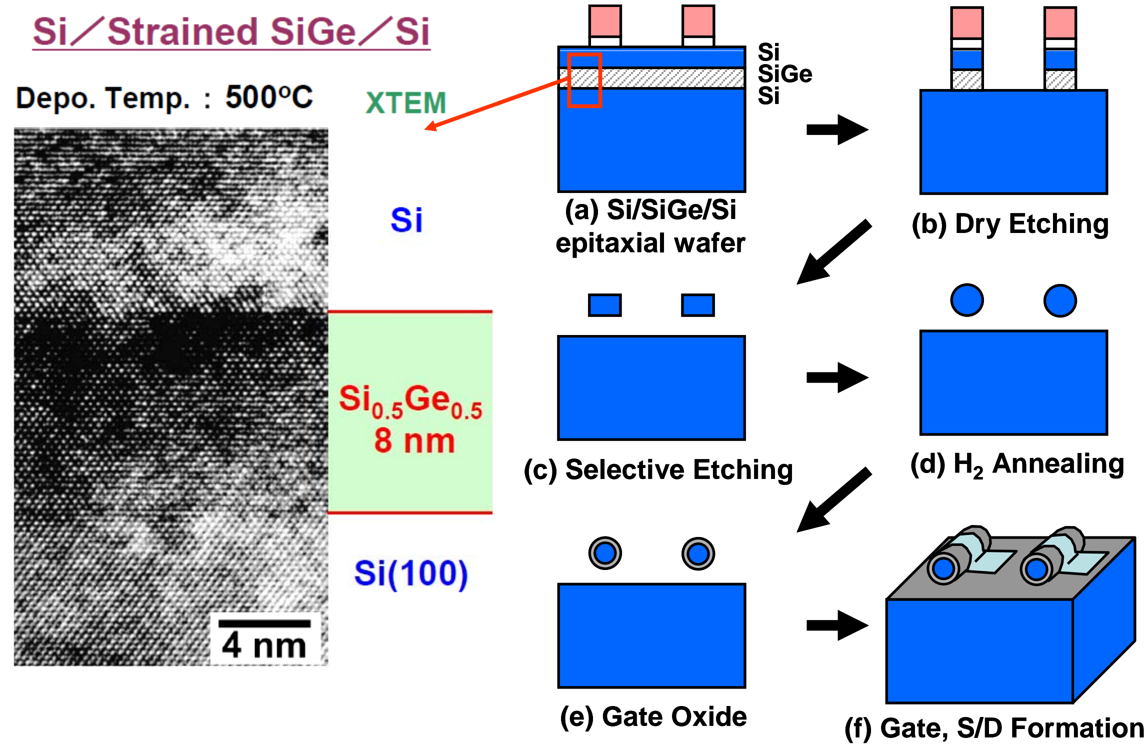


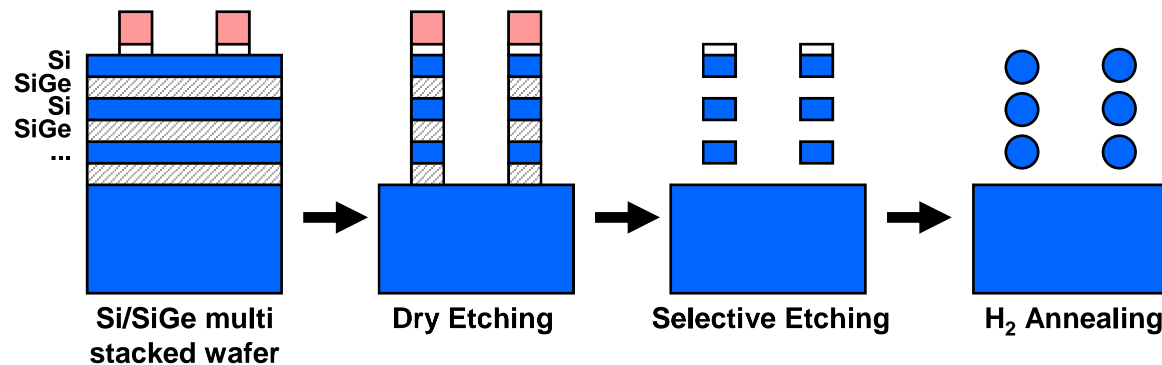




Surrounded gate MOS

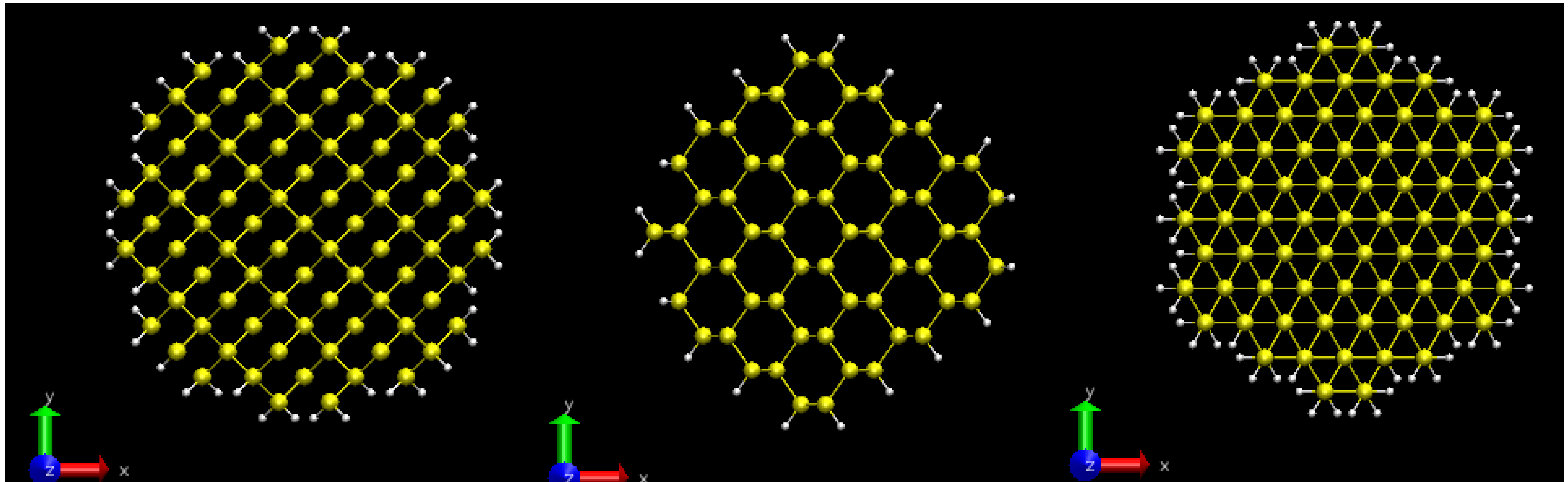
Increase the number of wires towards vertical dimension





Cross section of Si NW

First principal calculation, TAPP

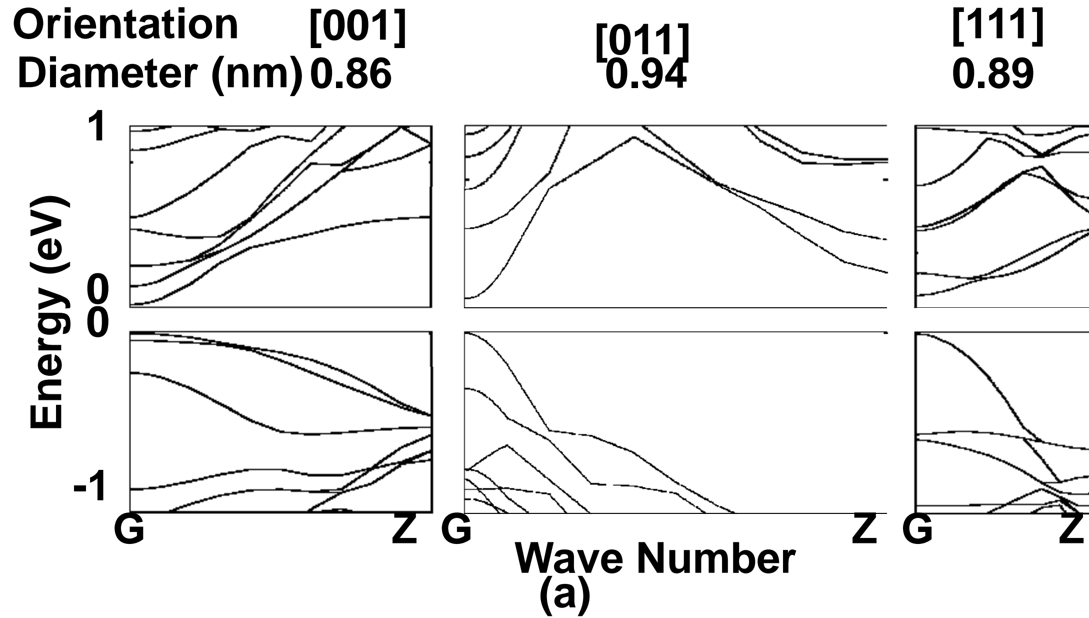


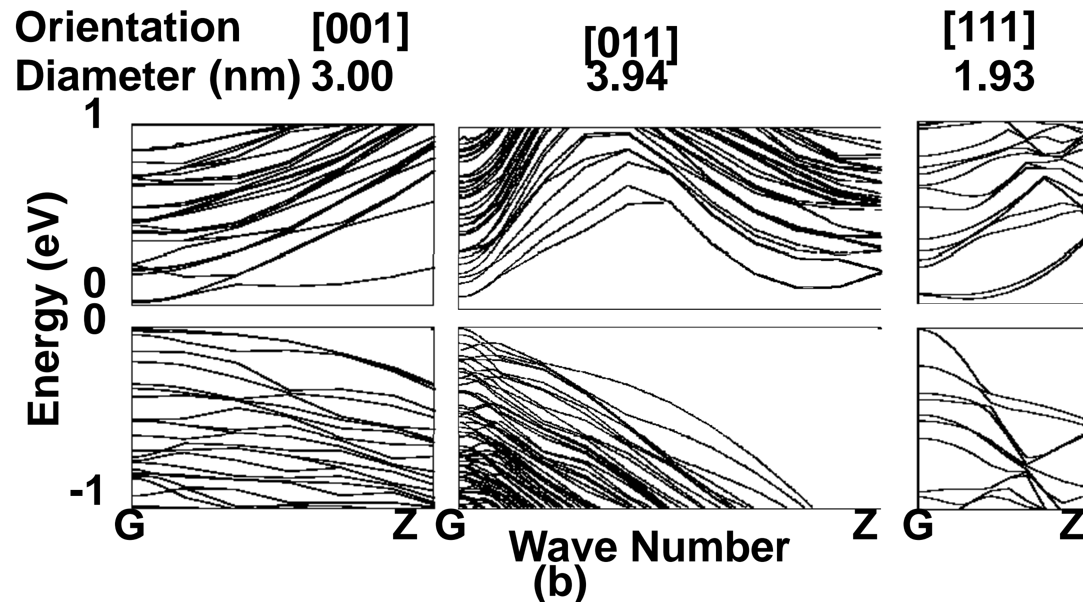
D=1.96nm [001]

D=1.94nm [011]

D=1.93nm [111]

Si nanowire FET with 1D Transport

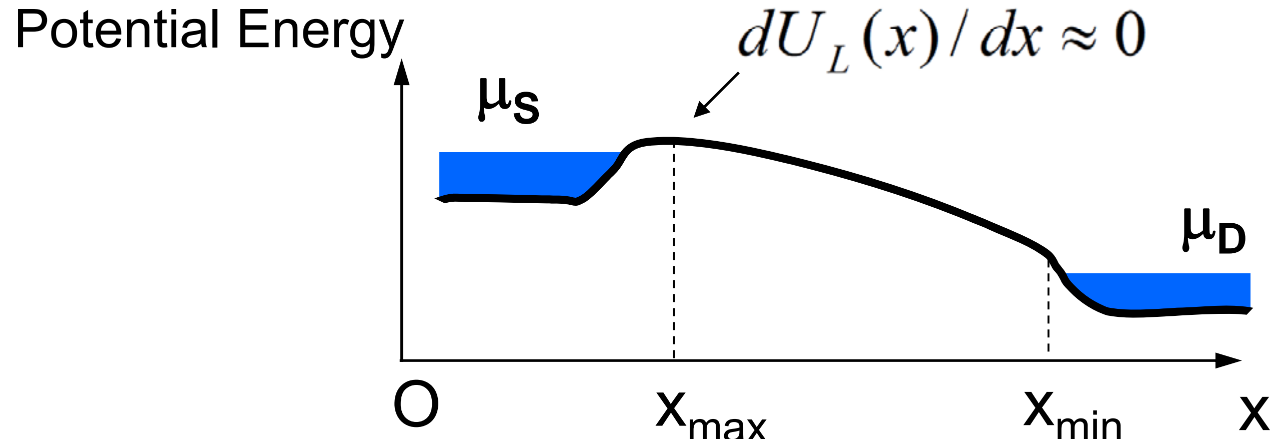




Small mass with [011]

Large number of quantum channels with [001]

Landauer Formalism for Ballistic FET

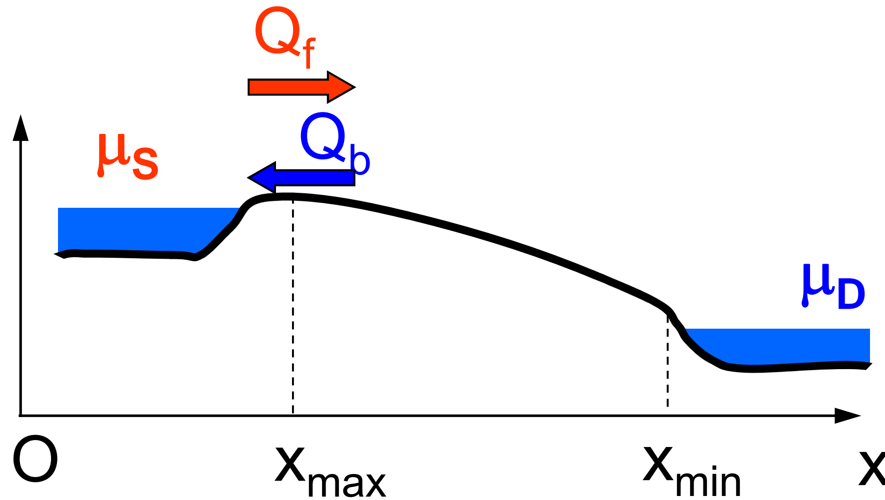


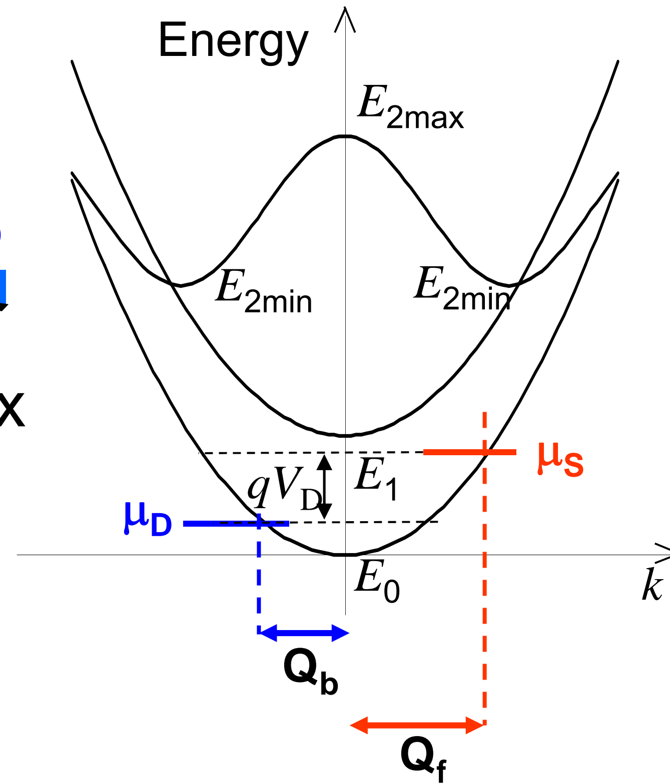
$$I_D = \frac{q}{\pi\hbar}\sum_i \int \left[f(E,\mu_S) - f(E,\mu_D)\right] T_i(E)\, dE$$

From x_{max} to x_{min} $\quad T_i(E) \approx 1$

$$I_D = G_0\left(\frac{k_B T}{q}\right)\sum_i g_i \ln\left\{\frac{1+\exp\left[(\mu_S - E_{i0})/k_B T\right]}{1+\exp\left[(\mu_D - E_{i0})/k_B T\right]}\right\}$$

Carrier Density obtained from E-k Band

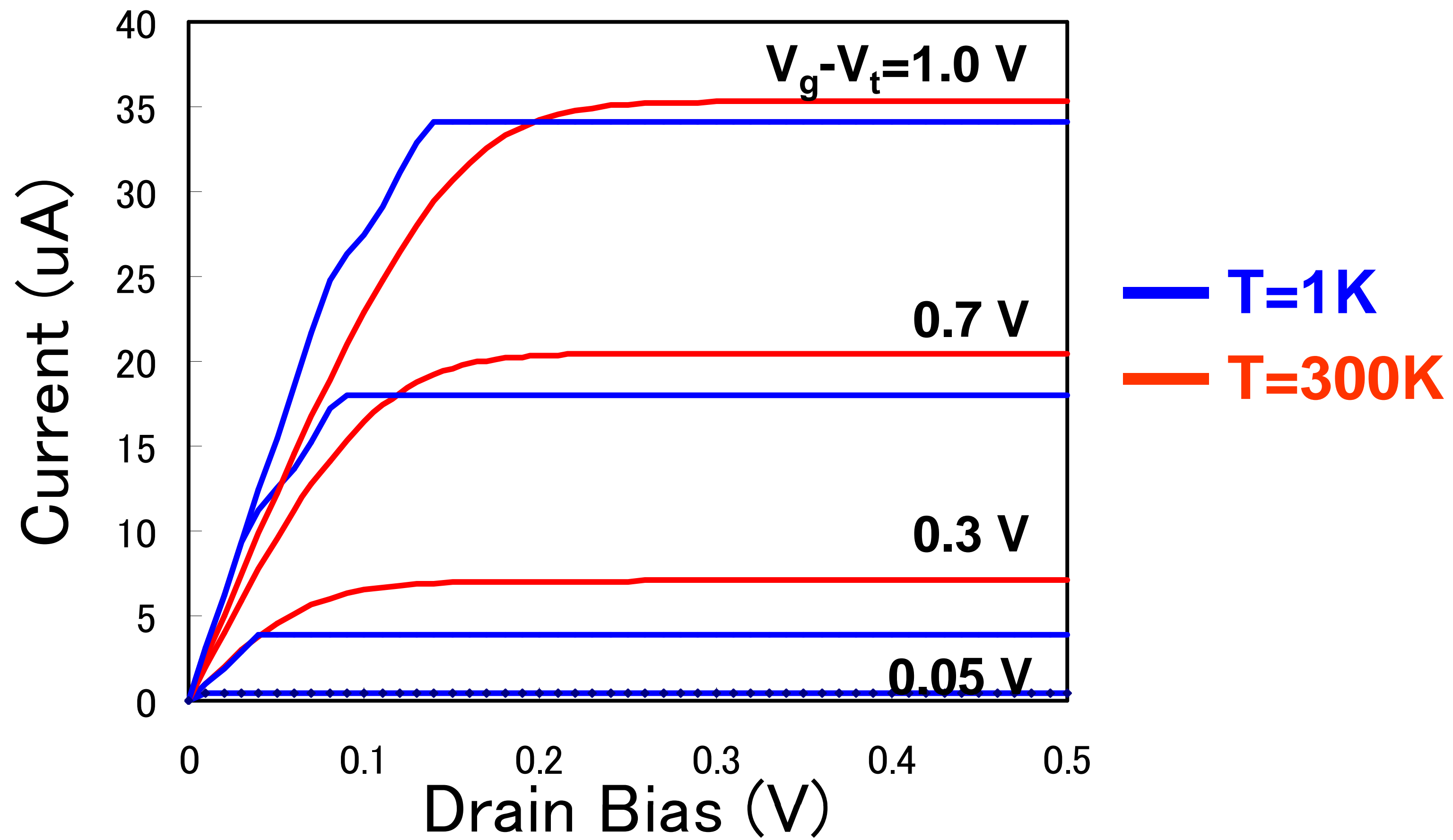




$$|Q| = |Q_f| + |Q_b|$$

$$= \frac{q}{\pi} \sum_i g_i \left[\int_{k_{i\,\min}}^{\infty} \frac{dk}{1 + \exp\left\{ \frac{E_i(k) - \mu_S}{k_B T} \right\}} + \int_{-\infty}^{k_{i\,\min}} \frac{dk}{1 + \exp\left\{ \frac{E_i(k) - \mu_D}{k_B T} \right\}} \right]$$

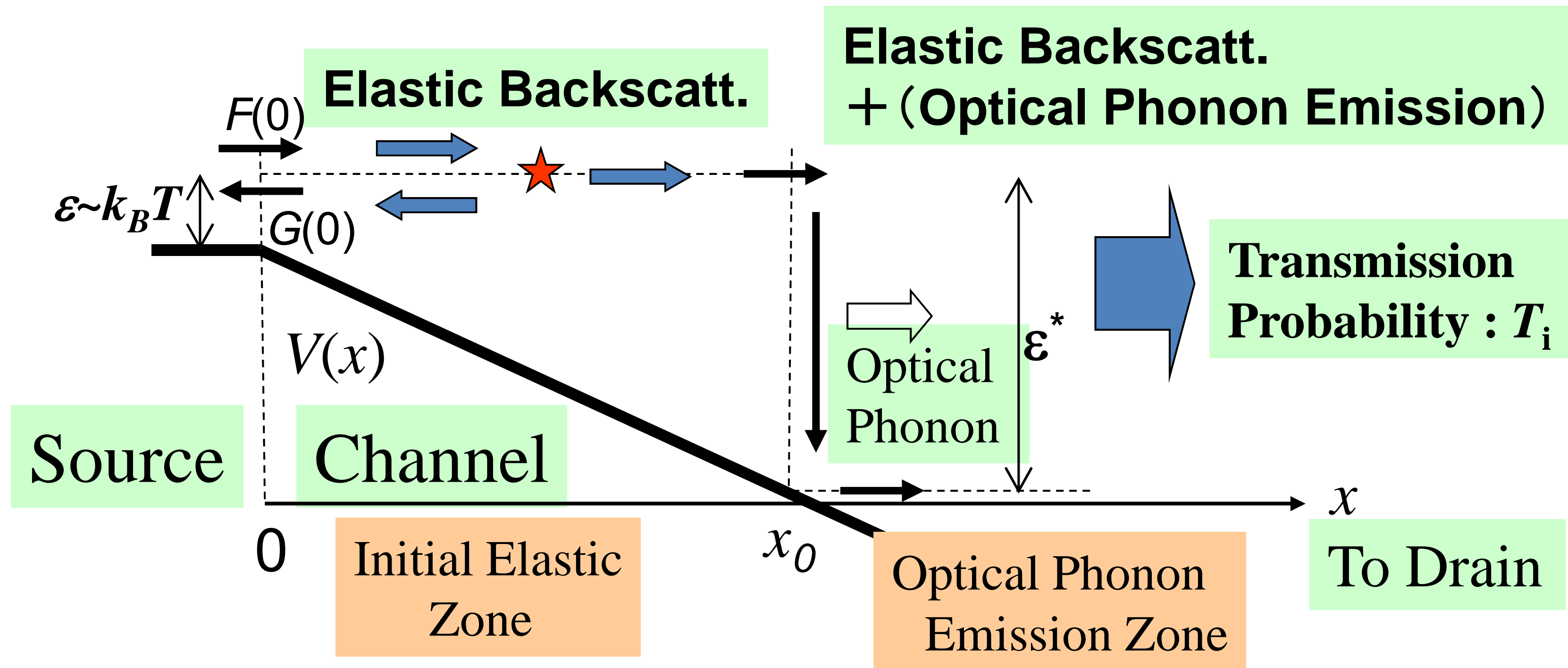
IV Characteristics of Ballistic SiNW FET



Small temperature dependency
35μA/wire for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx. : Electric Field E



Transmission Probability to Drain

$$T(\varepsilon) = \left.\frac{F(0) - G(0)}{F(0)}\right)_{\text{Injection from Drain}=0}$$

Résumé of the Compact Model

$$I = \frac{q}{\pi\hbar}\sum_i g_i \int \left[f(\varepsilon,\mu_s) - f(\varepsilon,\mu_D) \right] T_i \, d\varepsilon$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left\{ \frac{\sqrt{2r+t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r+t_{ox}} - \sqrt{t_{ox}}} \right\}}.$$

Planar Gate

$$(V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{|Q_f + Q_b|}{C_G}.$$

$$\mu_S - \mu_D = qV_D$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left(\frac{r+t_{ox}}{r}\right)}.$$

GAA

(Electrostatics requirement)

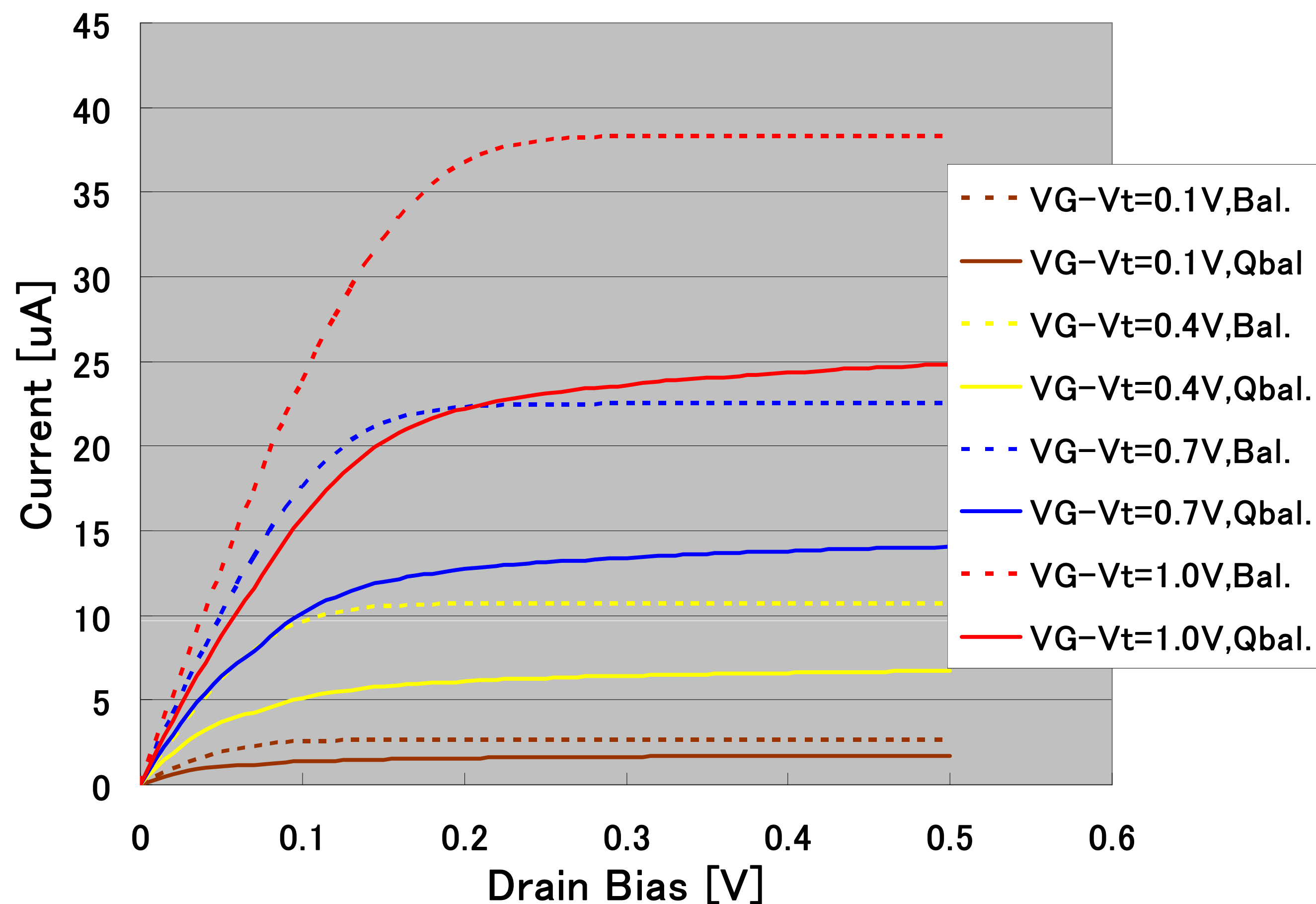
$$|Q_f + Q_b| = \frac{q}{\pi}\sum_i g_i \left[\int_{-\infty}^{\infty} \frac{dk}{1+\exp\left\{\frac{\varepsilon_i(k)-\mu_S}{k_B T}\right\}} - \int_{-\infty}^{0} \left\{ \frac{1}{1+\exp\left\{\frac{\varepsilon_i(k)-\mu_S}{k_B T}\right\}} - \frac{1}{1+\exp\left\{\frac{\varepsilon_i(k)-\mu_D}{k_B T}\right\}} \right\} T_i(\varepsilon_i(k))\,dk \right]$$

$$T(\varepsilon) = \frac{\sqrt{2D_0}\,qE}{\left(\sqrt{B_0+D_0} + \sqrt{D_0}\right) qE + \sqrt{2mD_0}\,B_0 \ln\left(\frac{qEx_0 + \varepsilon}{\varepsilon}\right)}$$

(Carrier distribution in Subbands)

Unknowns are I_D, $(\mu_S-\mu_0)$, $(\mu_D-\mu_0)$, および (Q_f+Q_b)

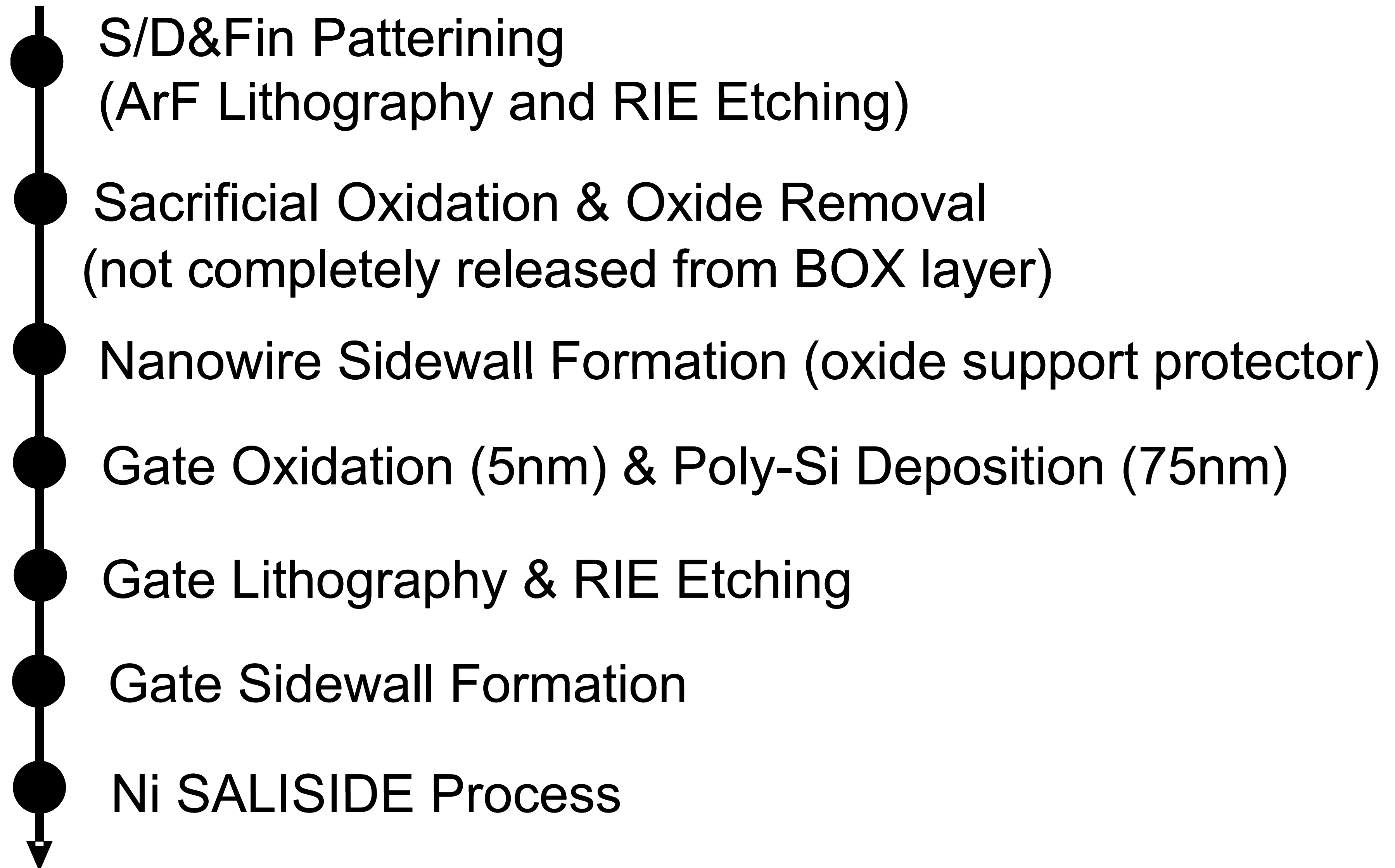
I-V_D Characteritics (RT)



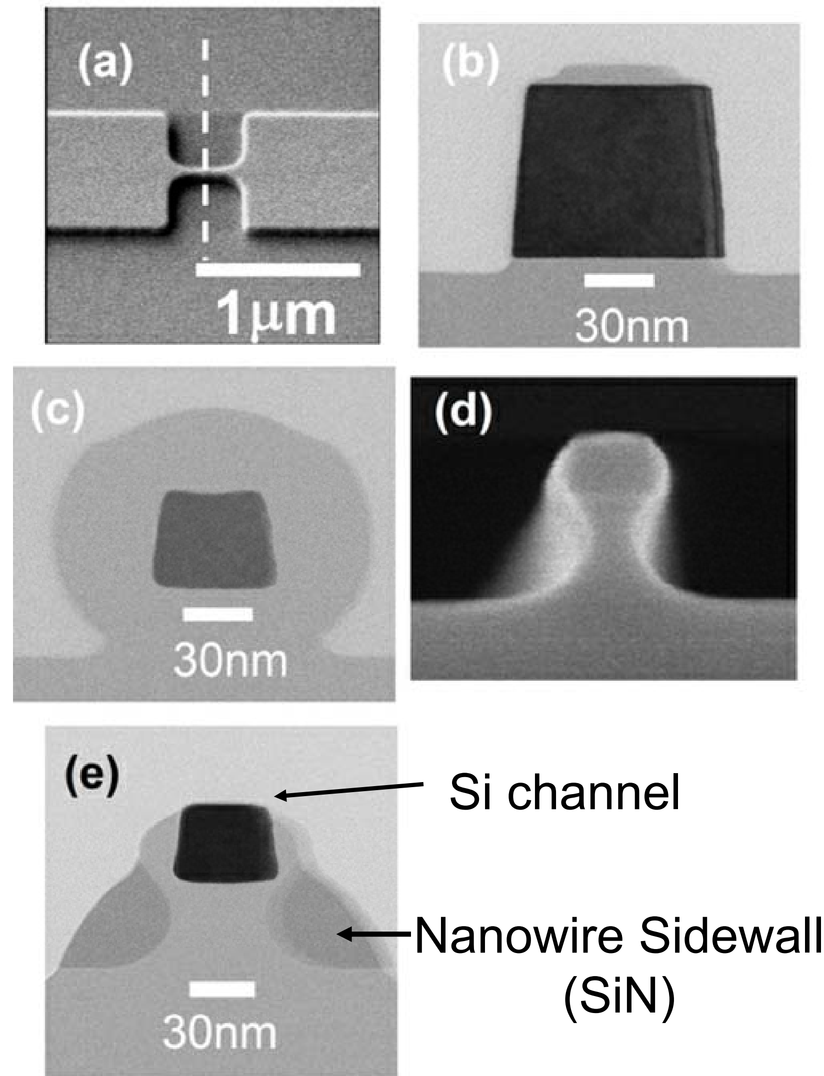
- **Electric current 20～25 μA**
- **No satruration at Large V_D**

SiNW FET Fabrication

Brief process flow of Si Nanowire FET



(a) Fin structure formed on BOX layer. (b)XTEM image of fin shown in (a) (c) XTEM image after sacrificial oxidation (d) Cross sectional SEM image after partial removal of sacrificial oxide (e) XTEM after nanowire sidewall formation

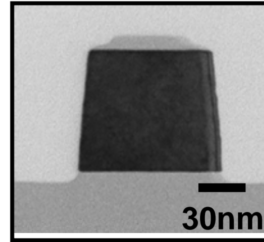


Si channel

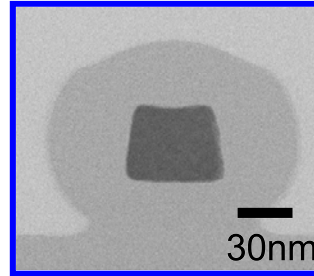
Nanowire Sidewall (SiN)

SiNW FET Fabrication

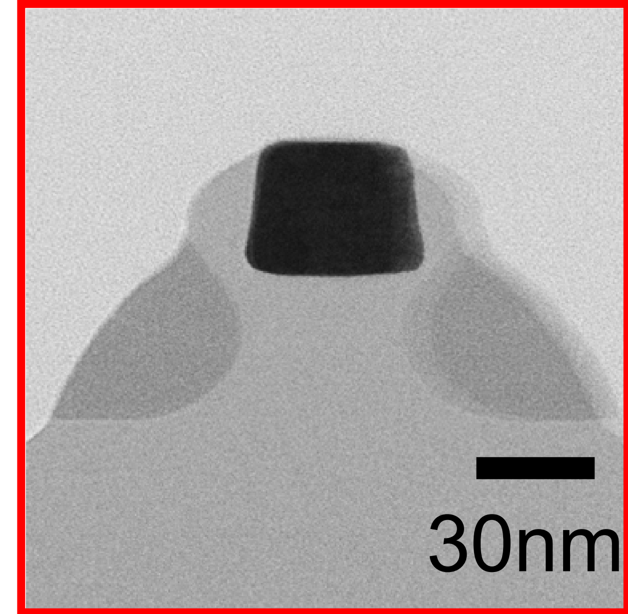
- S/D & Fin Patterning



- Sacrificial Oxidation



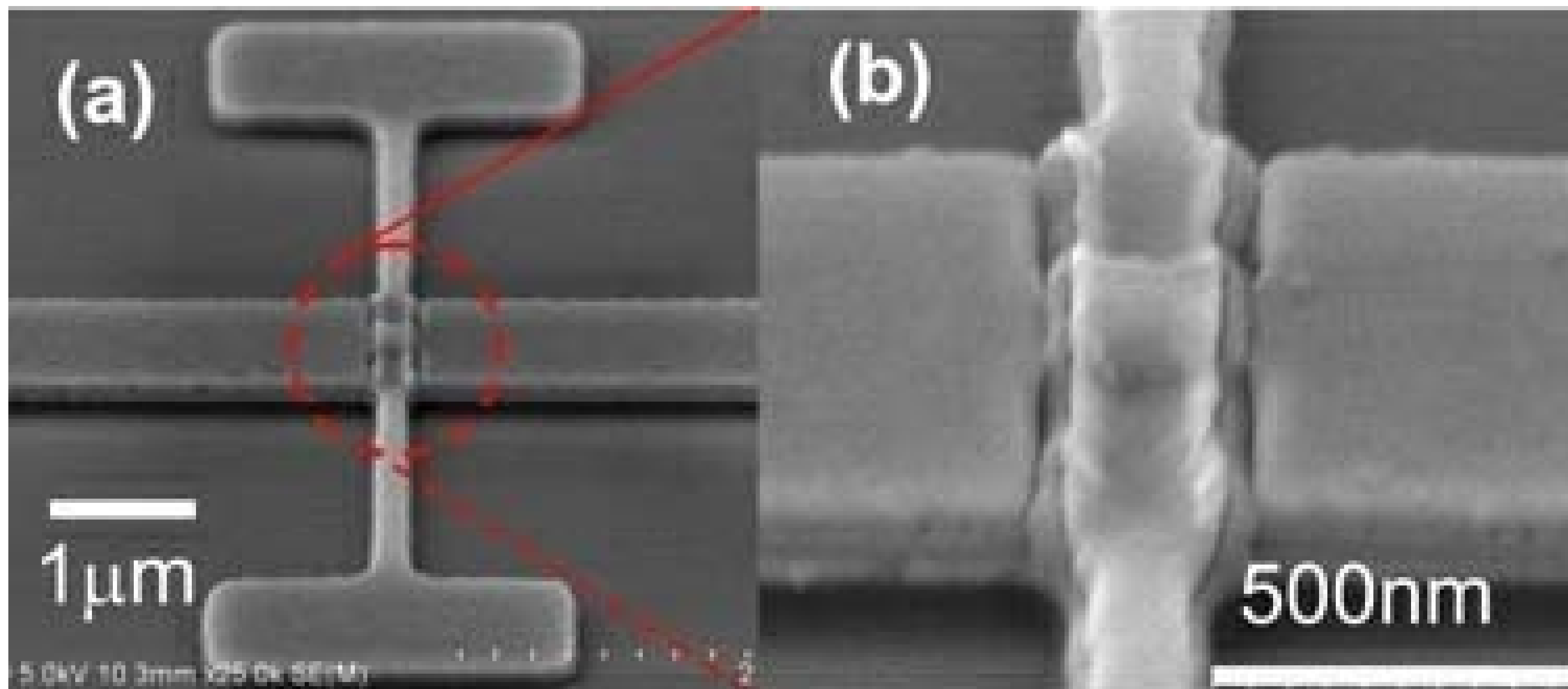
- Oixde etch back
- SiN sidewall support formation



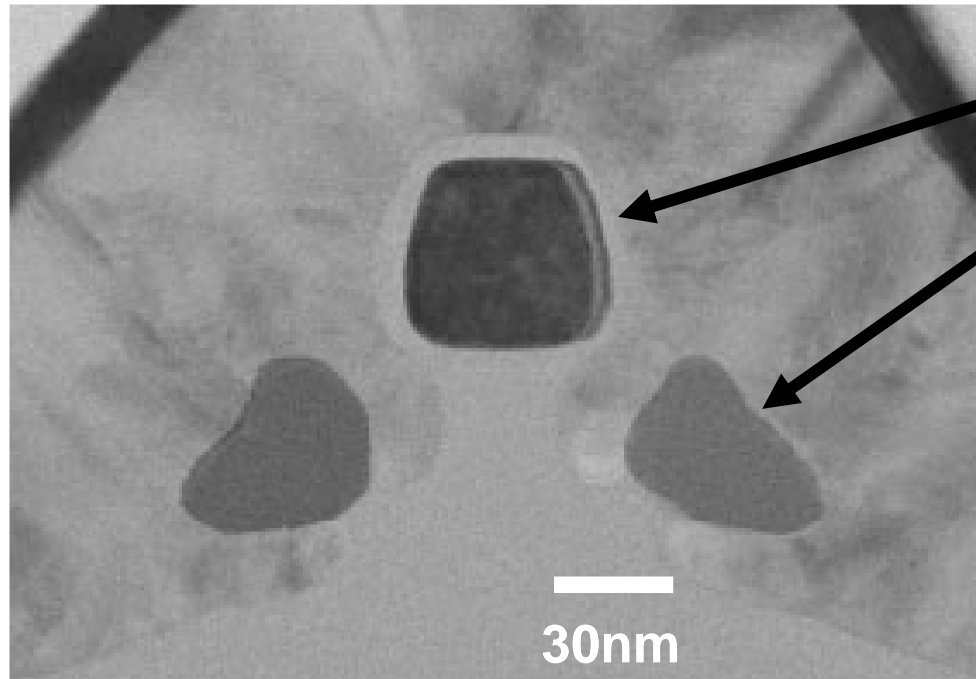
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

Standard recipe for gate stack formation

(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.

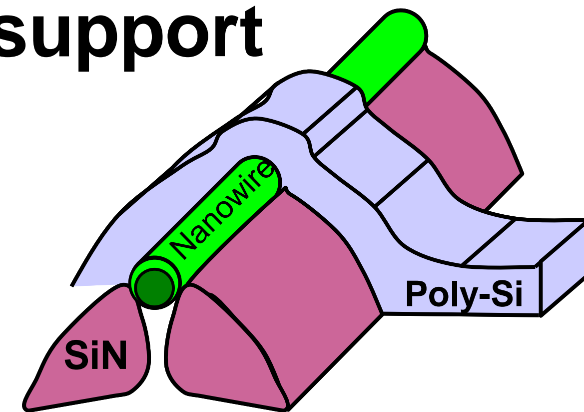


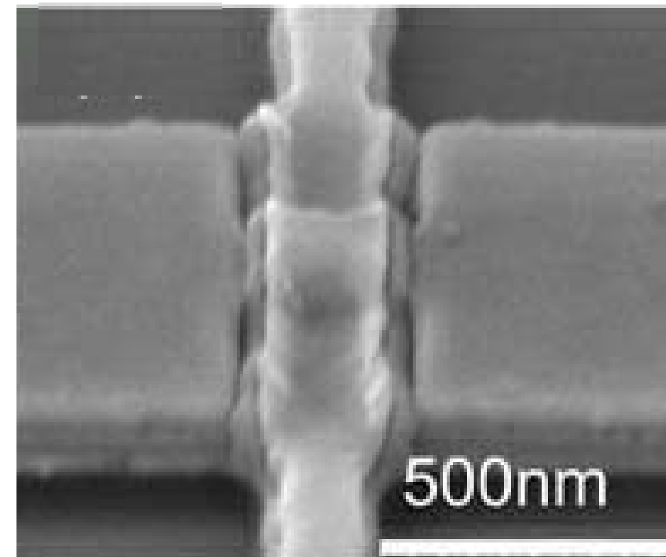
Fabricated SiNW FET



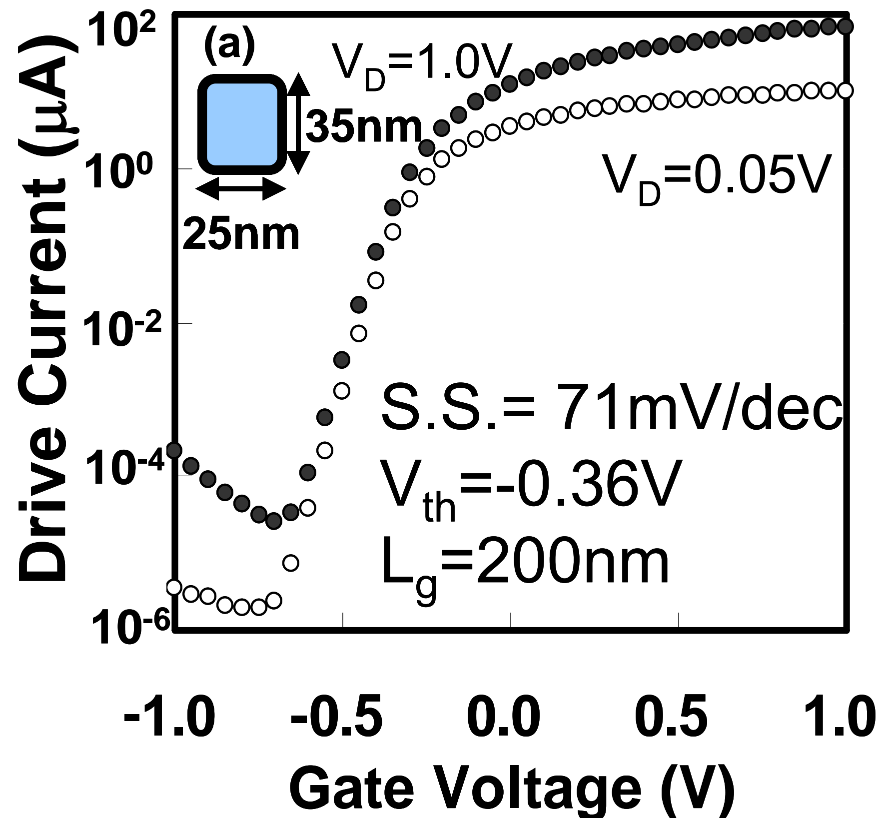
SiNW

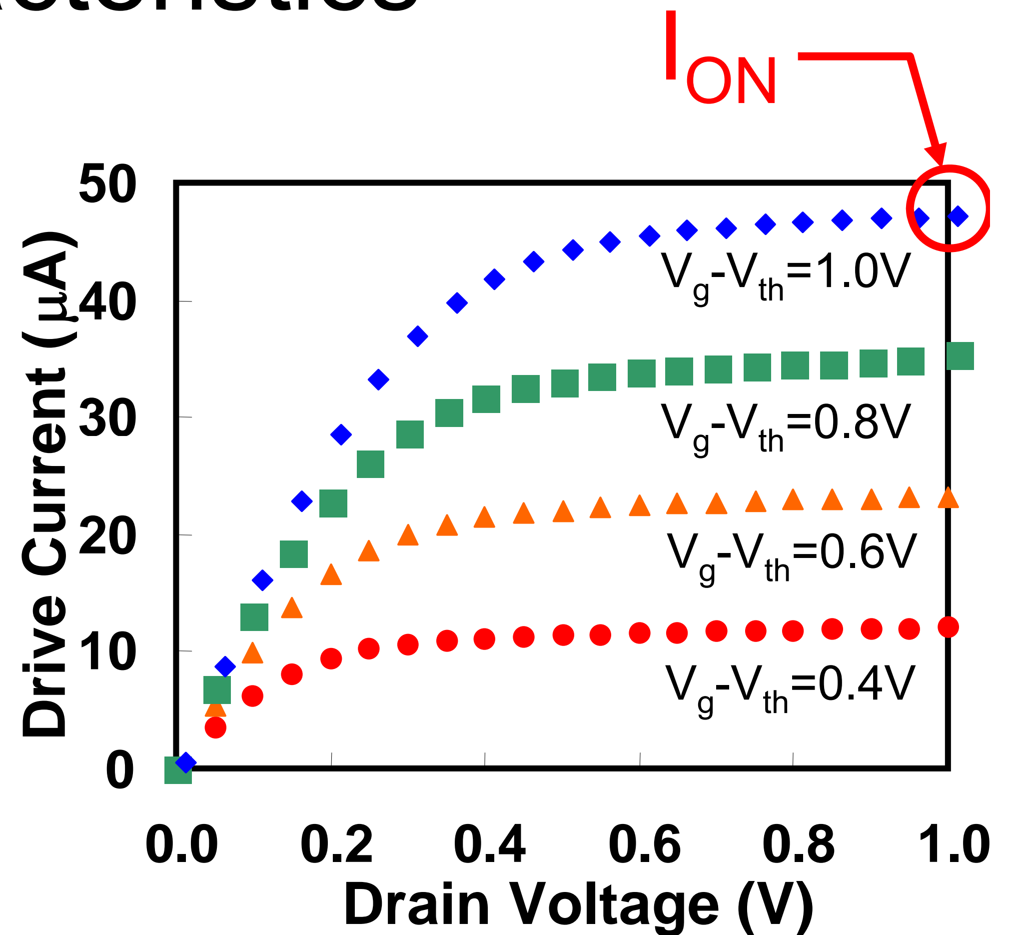
SiN support





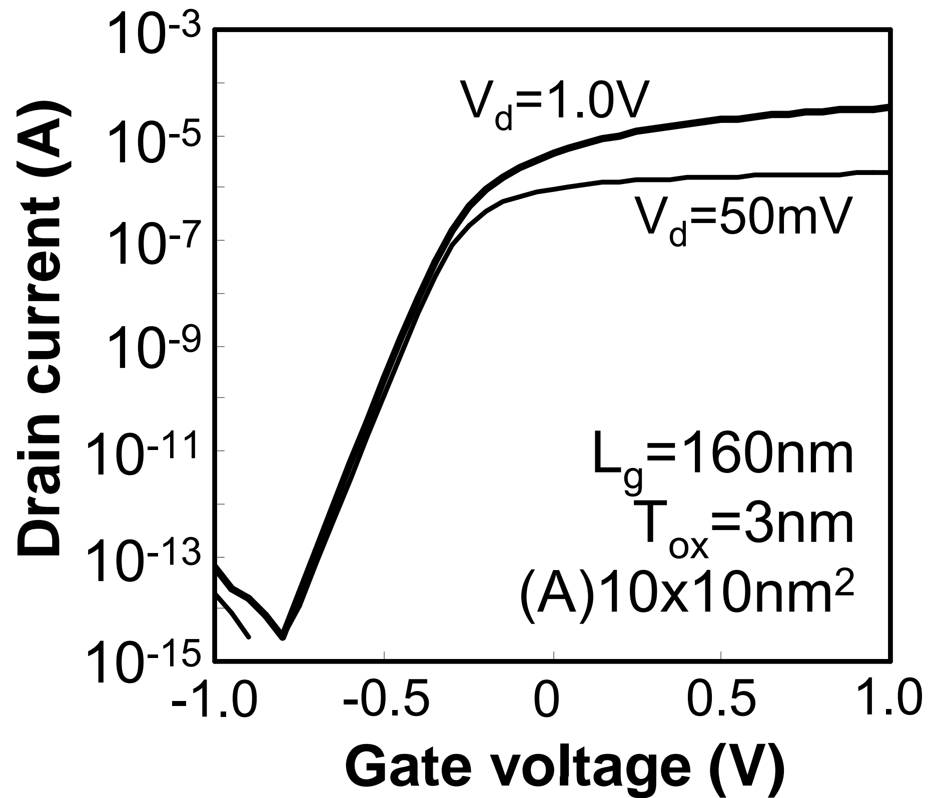
I_dV_g and I_dV_d Characteristics

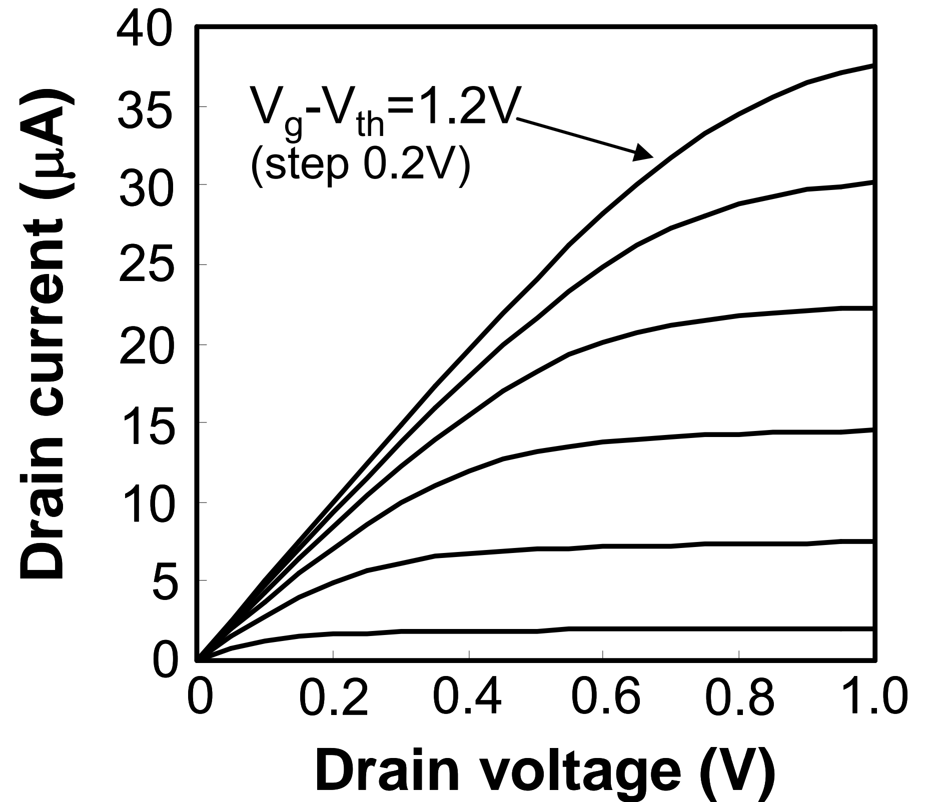


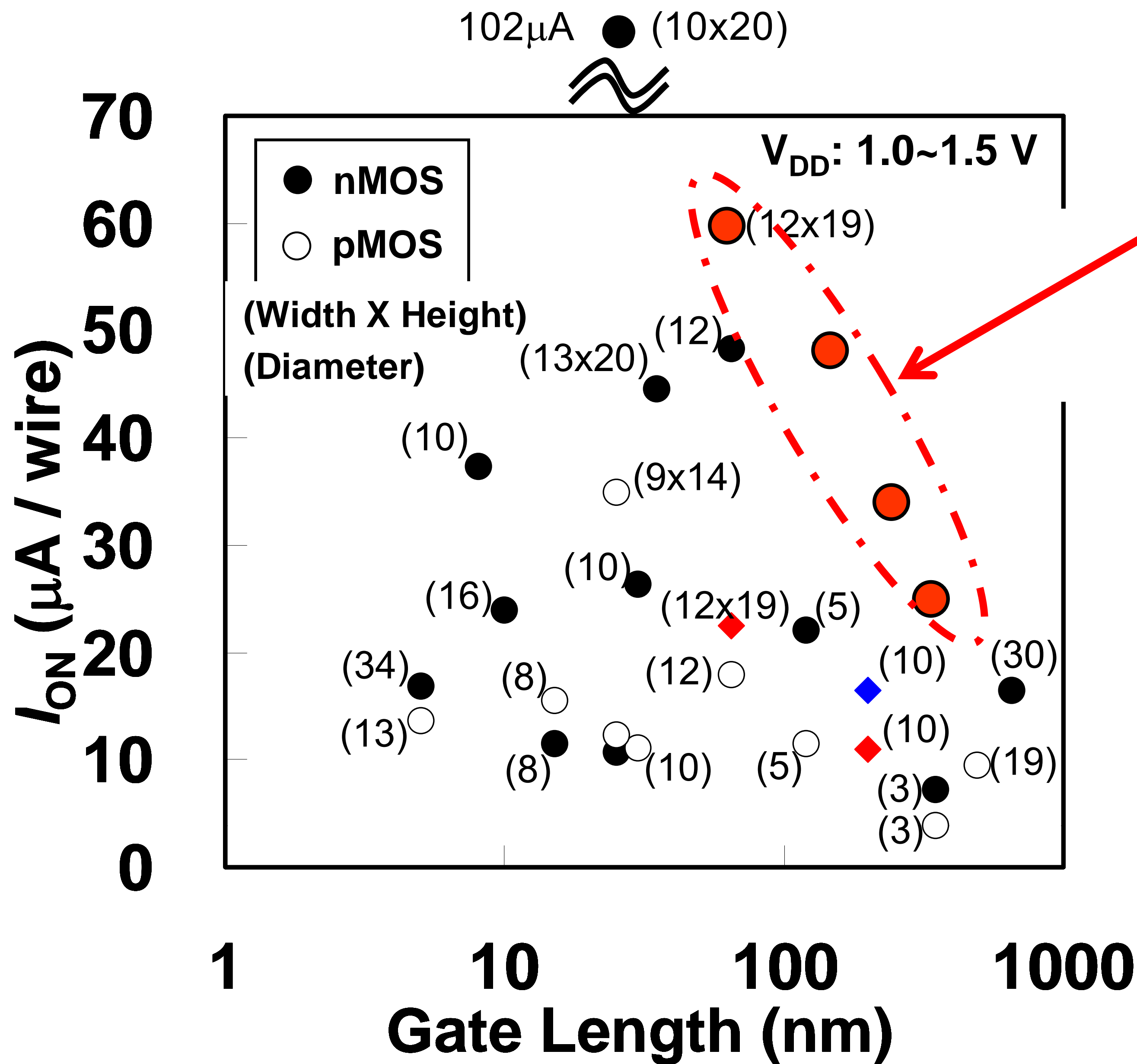


I_{on}/I_{off} ratio of $\sim 10^7$, high I_{on} of 49.6 μA/wire

Output characteristics of 10x10nm^2 SiNW FET



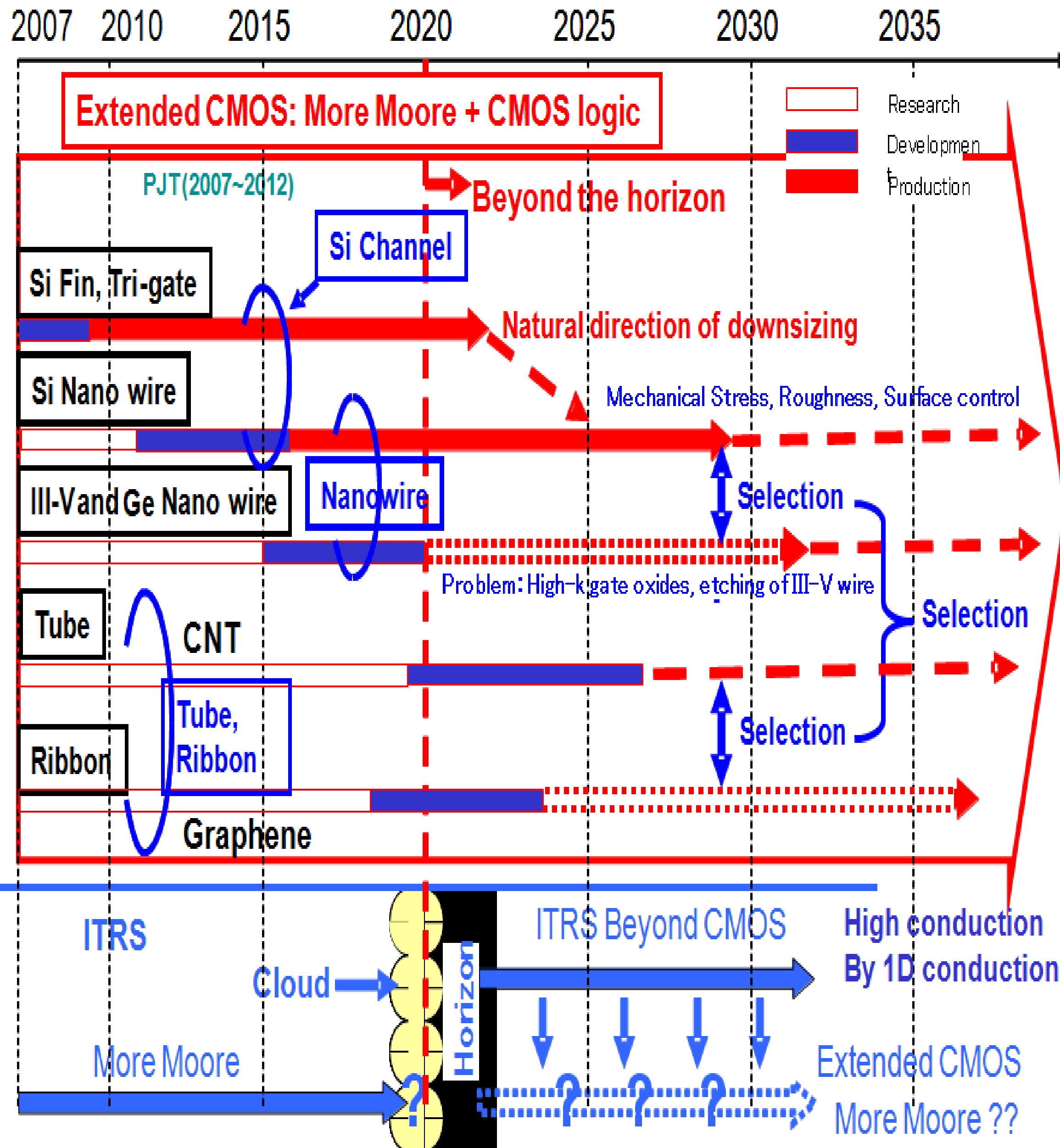




Our Work

Our roadmap for R &D

Source: H. Iwai, IWJT 2008



Current Issues

Si Nanowire

Control of wire surface property
Source Drain contact
Optimization of wire diameter
Compact I-V model

III-V & Ge Nanowire

High-k gate insulator
Wire formation technique

CNT:

Growth and integration of CNT
Width and Chirality control
Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique
Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

Thank you for your attention