Si Nanoelectronic Device Technology

Beyond the definition of classical devices & communication technology

@Siliguri Institute of Technology

March 29, 2010

Tokyo Institute of Technology

Frontier Research Center

Hiroshi Iwai
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
Institute Overview

Established in 1881 → 130th anniversary in 2011
3 undergraduate schools
   School of Science, School of Engineering, School of Bioscience and Biotechnology
7 graduate schools
   Science and Engineering Science, Science and Engineering Technology,
   Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
   Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

<table>
<thead>
<tr>
<th></th>
<th>Undergraduate</th>
<th>Graduate</th>
<th>Master's</th>
<th>Doctoral</th>
<th>Teaching Staff</th>
<th>Student/Instructor</th>
<th>Staff</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tokyo Inst.</td>
<td>5,000</td>
<td>5,000</td>
<td>3,500</td>
<td>1,500</td>
<td>1,200</td>
<td>8.3</td>
<td>550</td>
</tr>
<tr>
<td>Per Year</td>
<td>1,200</td>
<td>1,800</td>
<td>500</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Asia 847
Europe 78
North America 12
South America 24
Oceania 5
Africa 16

Total 982
(As of May. 1, 2005)
Tokyo Institute of Technology

Interdisciplinary Graduate School of Science and Engineering

Dept. of Electronics and Physics

Frontier Research Center

G CEO (Global Center of Excellence) for Photonics Nanodevice Integration Engineering

Other GCEO

Innovation Research Initiatives

5000 Undergraduate students
5000 Graduate Students

2 major campuses
Ookayama, Tokyo
Suzukakedai, Yokohama

5 other schools
4 Laboratories

10 other dept.

Consists of about 10 professor who have big projects

Consists of 5 EE Related departments

Consists of 5 EE Related departments
Interdisciplinary Graduate School of Science and Engineering
大学院総合理工学研究科

J2 Building:
Frontier Collaborative Research Center (FCRC)
先端創造共同研究中心
Iwai Lab. Equipment

MBE and Sputter Chamber

Sputter Chamber

MBE Chamber

RTA Furnace No.1

RTA Furnace No.2

RF measurement system; 8 inch wafer, 40 GHz

1/f noise measurement system; 6 inch wafer

RF measurement system; 8 inch wafer, 40 GHz

1/f noise measurement system; 6 inch wafer

Back Pressure:
10^-8 Pa
During Deposition:
10^-7 Pa
Deposition Rate:
0.1 to 1 nm/sec.
岩井研究室 ~Iwai Lab.~

Welcome to Iwai Lab.

次世代高性能半導体デバイスに向けた研究テーマ

Siデバイスの重要性

現代社会：産業、金融、運輸、医療、行政等の社会構造
インターネット、i-mode、Bluetooth、携帯電話、カーナビ、
ゲーム、自動車、航空機、製造装置などの全ての器、
CD、DVDなどの結果

ULTRALIM

Si集積回路による管理、制御無くてこれより有り得ない

近年のSiデバイスの驚異的な急増

数千万から数億個のトランジスタ集積
MPUのクロック周波数 3GHz
SiGeバイポラードの3,000GHz以上

微細化の重要性

量子の概念化（100年間に500万倍以上作）

Ion etch

プラズマエッチング

High-k/Metalゲートスパック

次世代ゲート絶縁膜材料として

LagO3に注目

High-kとSiの直接合成が必要

C_max = \frac{\varepsilon_s \varepsilon_0 \phi}{t_{ox}} \Rightarrow t_{ox} = \frac{\varepsilon_s \phi}{\varepsilon_0 EOT}

高性能・低消費電力化には

Lao3は特性の良い直接合成が可能

High-kとSiの直接合成が必要
Importance of Electronics

• There were many inventions in the 20th century: Airplane, Nuclear Power generation, Computer, Space aircraft, etc

• However, everything has to be controlled by electronics

• Electronics
  
  Most important invention in the 20th century

• What is Electronics: To use electrons, Electronic Circuits
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Same mechanism as that of transistor
4 wives of Lee De Forest

1906 Lucille Sheardown
1907 Nora Blatch
1912 Mary Mayo, singer
1930 Marie Mosquini, silent film actress
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928
**Capacitor structure with notch**

- **Negative bias**
  - Gate Electrode
  - Gate Insulator
  - Semiconductor
  - Electron
  - No current

- **Positive bias**
  - Electric field
  - Current flows
Today’s transistor: MOSFET for CMOS LSI

Surface Potential (Negative direction)

0 bias for gate

Positive bias for gate
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator

Drain Current was several orders of magnitude smaller than expected

Even Shockley!
However, they found amplification phenomenon when investigating Ge surface when putting needles. This is the 1st Transistor: Not Field Effect Transistor, But Bipolar Transistor (another mechanism)

1947: 1st transistor

J. Bardeen
W. Brattain
W. Shockley

Bipolar using Ge
1958: 1st Integrated Circuit

Connect 2 bipolar transistors in the Same substrate by bonding wire.

Jack S. Kilby
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

Al Gate

Si
Drain

Si/SiO₂ Interface is extraordinarily good
1970,71: 1st generation of LSIs

DRAM    Intel 1103

MPU     Intel 4004
MOS LSI experienced continuous progress for many years

<table>
<thead>
<tr>
<th>Name of Integrated Circuits</th>
<th>Number of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>1960s IC (Integrated Circuits)</td>
<td>~ 10</td>
</tr>
<tr>
<td>1970s LSI (Large Scale Integrated Circuit)</td>
<td>~1,000</td>
</tr>
<tr>
<td>1980s VLSI (Very Large Scale IC)</td>
<td>~10,000</td>
</tr>
<tr>
<td>1990s ULSI (Ultra Large Scale IC)</td>
<td>~1,000,000</td>
</tr>
<tr>
<td>2000s ?LSI (? Large Scale IC)</td>
<td>~1,000,000,000</td>
</tr>
</tbody>
</table>
Gate Electrode
Poly Si

Gate Insulator
SiO₂

Substrate
Si

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Use Gate Field Effect for switching

Gate Electrode
Poly Si

Gate Insulator
SiO₂

Source

Channel

N-MOS (N-type MOSFET)

Drain

Si Substrate
CMOS

Complementary MOS

Inverter

PMOS

NMOS

When NMOS is ON, PMOS is OFF

When PMOS is ON, NMOS is OFF
CMOS Technology: Indispensable for our human society

All the human activities are controlled by CMOS living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:
There is no computer in banks, and world economical activities immediately stop.

Cellarer phone dose not exists
Downsizing of the components has been the driving force for circuit evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>1900</th>
<th>1950</th>
<th>1960</th>
<th>1970</th>
<th>2000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>Vacuum Tube</td>
<td>Transistor</td>
<td>IC</td>
<td>LSI</td>
<td>ULSI</td>
</tr>
<tr>
<td>Size</td>
<td>10 cm</td>
<td>cm</td>
<td>mm</td>
<td>10 µm</td>
<td>100 nm</td>
</tr>
<tr>
<td></td>
<td>10⁻¹m</td>
<td>10⁻²m</td>
<td>10⁻³m</td>
<td>10⁻⁵m</td>
<td>10⁻⁷m</td>
</tr>
</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. Reduce Capacitance
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed
2. Increase number of Transistors
   - Parallel processing
     - Increase circuit operation speed

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.
Scaling Method: by R. Dennard in 1974

**Wdep**: Space Charge Region (or Depletion Region) Width

- Wdep has to be suppressed
- Otherwise, large leakage between S and D

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

\[ X, Y, Z : K, \quad V : K, \quad Na : 1/K \]

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

\[ W_{dep} \propto \sqrt{V/Na} : K \]

**K=0.7 for example**

Good scaled I-V characteristics
Downscaling merit: Beautiful!

<table>
<thead>
<tr>
<th>Geometry &amp; Supply voltage</th>
<th>L_g, W_g, T_{ox}, V_{dd}</th>
<th>K</th>
<th>Scaling K: K=0.7 for example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive current in saturation</td>
<td>I_d</td>
<td>K</td>
<td>I_d = v_{sat} W_g C_o (V_g - V_{th})</td>
</tr>
<tr>
<td></td>
<td>W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_d per unit W_g</td>
<td>I_d/μm</td>
<td>1</td>
<td>I_d per unit W_g = I_d / W_g = 1</td>
</tr>
<tr>
<td>Gate capacitance</td>
<td>C_g</td>
<td>K</td>
<td>C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox}</td>
</tr>
<tr>
<td>Switching speed</td>
<td>\tau</td>
<td>K</td>
<td>\tau = C_g V_{dd} / I_d</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>f</td>
<td>1/K</td>
<td>f = 1/\tau = 1/K</td>
</tr>
<tr>
<td>Chip area</td>
<td>A_{chip}</td>
<td>\alpha</td>
<td>\alpha: Scaling factor</td>
</tr>
<tr>
<td>Integration (# of Tr)</td>
<td>N</td>
<td>\alpha/K^2</td>
<td>N \rightarrow \alpha/K^2 = 1/K^2 , when \alpha=1</td>
</tr>
<tr>
<td>Power per chip</td>
<td>P</td>
<td>\alpha</td>
<td>fNCV^2/2 \rightarrow K^{-1}(\alphaK^{-2})K(K^1)^2 = \alpha = 1, when \alpha=1</td>
</tr>
<tr>
<td>Parameter</td>
<td>$k = 0.7$ and $\alpha = 1$</td>
<td>$k = 0.7^2 = 0.5$ and $\alpha = 1$</td>
<td></td>
</tr>
<tr>
<td>-----------------</td>
<td>-----------------------------</td>
<td>---------------------------------</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Single MOFET</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>$0.7$</td>
<td>$V_{dd}$</td>
<td></td>
</tr>
<tr>
<td>$L_g$</td>
<td>$0.7$</td>
<td>$L_g$</td>
<td></td>
</tr>
<tr>
<td>$I_d$</td>
<td>$0.7$</td>
<td>$I_d$</td>
<td></td>
</tr>
<tr>
<td>$C_g$</td>
<td>$0.7$</td>
<td>$C_g$</td>
<td></td>
</tr>
<tr>
<td>$P (\text{Power})/\text{Clock}$</td>
<td>$0.7^3 = 0.34$</td>
<td>$P (\text{Power})/\text{Clock}$</td>
<td>$0.5^3 = 0.125$</td>
</tr>
<tr>
<td>$\tau (\text{Switching time})$</td>
<td>$0.7$</td>
<td>$\tau (\text{Switching time})$</td>
<td>$0.5$</td>
</tr>
<tr>
<td><strong>Chip</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$N (# \text{of Tr})$</td>
<td>$1/0.7^2 = 2$</td>
<td>$N (# \text{of Tr})$</td>
<td>$1/0.5^2 = 4$</td>
</tr>
<tr>
<td>$f (\text{Clock})$</td>
<td>$1/0.7 = 1.4$</td>
<td>$f (\text{Clock})$</td>
<td>$1/0.5 = 2$</td>
</tr>
<tr>
<td>$P (\text{Power})$</td>
<td>$1$</td>
<td>$P (\text{Power})$</td>
<td>$1$</td>
</tr>
</tbody>
</table>
Actual past downscaling trend until year 2000

Change in 30 years

<table>
<thead>
<tr>
<th></th>
<th>Ideal scaling</th>
<th>Real Change</th>
<th></th>
<th>Ideal scaling</th>
<th>Real Change</th>
<th></th>
<th>Ideal scaling</th>
<th>Real Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_g ) ( t_{ox} )</td>
<td>( \frac{K}{K(10^{-2})} ) ( 10^{-2} ) ( 10^{-2} )</td>
<td>( I_d/\mu m ) ( 1 ) ( 10^1 )</td>
<td>( V_{dd} )</td>
<td>( K(10^{-2}) ) ( 10^{-1} )</td>
<td>( 1/K(10^2) ) ( 10^3 )</td>
<td>( P )</td>
<td>( \alpha(10^1) ) ( 10^5 )</td>
<td>( f \alpha N C V^2 )</td>
</tr>
</tbody>
</table>

Past 30 years scaling

Merit: N, f increase
Demerit: P increase

\( V_{dd} \) scaling insufficient
Additional significant increase in \( I_d, f, P \)

Vd scaling insufficient, \( \alpha \) increased \( \rightarrow \) N, Id, f, P increased significantly

Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1µm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5µm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25µm:</td>
<td>Direct-tunneling of gate SiO₂</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1µm:</td>
<td>‘0.1µm brick wall’(various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
Historically, many predictions of the limit of downsizing. VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.
C. Mead  L. Conway
Finally, there appears to be a fundamental limit of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide .... begin to make the devices of smaller dimension unworkable.
Direct-tunneling effect

PotentialBarrier

Gate Electrode

Gate Oxide

Potential Barrier

Si Substrate

Wave function

Direct tunneling current

Direct tunneling leakage current start to flow when the thickness is 3 nm.
Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide

- **Lg = 10 µm**
- **Lg = 5 µm**
- **Lg = 1.0 µm**
- **Lg = 0.1 µm**
Gate leakage: $I_g \propto $ Gate Area $\propto $ Gate length ($L_g$)

Drain current: $I_d \propto 1/$Gate length ($L_g$)

$L_g \rightarrow $ small, 
Then, $I_g \rightarrow $ small, $I_d \rightarrow $ large,    Thus, $I_g/I_d \rightarrow $ very small
Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!

Some one will think for you
Transistor Scaling Continues

90nm node
Lg=50nm

65nm node
Lg=35nm

45nm node
Lg=25nm

32nm node
Lg=15nm

22nm node
Lg=10nm

~30% every two years

ITRS 2003 (HP)

Qi Xinag, ECS 2004, AMD
Downsizing limit?  

Channel length?

Electron wave length

10 nm
5 nm gate length CMOS

Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC

IEDM, 2003
Electron wave length

10 nm

Tunneling distance

3 nm

Downsizing limit!
Channel length
Gate oxide thickness
**Prediction now!**

- **Electron wave length**: 10 nm
- **Tunneling distance**: 3 nm
- **Atom distance**: 0.3 nm

**MOSFET operation**

- **Lg = 2 ~ 1.5 nm?**
- Below this, no one knows future!
However, Gate oxide thickness 2 orders magnitude smaller Close to limitation!!

Lg: Gate length downsizing will continue to another 10-15 years
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
So, we are now in the limitation of downsizing?

Do you believe this or do not?
There is a solution! To use high-k dielectrics

Thin gate SiO₂  Thick gate high-k dielectrics

Almost the same electric characteristics

However, very difficult and big challenge!
Remember MOSFET had not been realized without Si/SiO₂!
Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>Unstable at Si interface</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
<th>He</th>
<th>B</th>
<th>C</th>
<th>N</th>
<th>O</th>
<th>F</th>
<th>Ne</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Si + MOX M + SiO₂</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Li Be</td>
<td>Si + MOX M + SiO₂</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Na Mg</td>
<td>Si + MOX M + MSiₓ + SiO₂</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| Ca Sc      | Si + MOX M + MSiₓ + SiO₂ |                         |              |    |   |   |   |   |   |    |
| Sr Y Zr    | Si + MOX M + MSiₓ + SiO₂ |                         |              |    |   |   |   |   |   |    |
| Cs Ba      | Si + MOX M + MSiₓ + SiO₂ |                         |              |    |   |   |   |   |   |    |

HfO₂ based dielectrics are selected as the first generation materials, because of their merit in 1) band-offset, 2) dielectric constant 3) thermal stability.

La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

R. Hauser, IEDM Short Course, 1999
Band Offsets

Calculates value

Dielectric constant

SiO₂; 4
Si₃N₄: ~ 7
Al₂O₃: ~ 9

Y₂O₃; ~10
Gd₂O₃: ~10
La₂O₃: ~27

HfO₂ was chosen for the 1ˢᵗ generation
La₂O₃ is more difficult material to treat
Dielectric constant value vs. Band offset (Measured)

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>3.9</td>
</tr>
<tr>
<td>AlₓSiᵧO₂</td>
<td></td>
</tr>
<tr>
<td>(Ba,Sr)TiO₃</td>
<td>200-300</td>
</tr>
<tr>
<td>BeAl₂O₄</td>
<td>8.3-9.43</td>
</tr>
<tr>
<td>CeO₂</td>
<td>16.6-26</td>
</tr>
<tr>
<td>CeHfO₄</td>
<td>10-20</td>
</tr>
<tr>
<td>CoTiO₃/Si₃N₄</td>
<td></td>
</tr>
<tr>
<td>EuAlO₃</td>
<td>22.5</td>
</tr>
<tr>
<td>HfO₂</td>
<td>26-30</td>
</tr>
<tr>
<td>Hf silicate</td>
<td>11</td>
</tr>
<tr>
<td>La₂O₃</td>
<td>20.8</td>
</tr>
<tr>
<td>LaScO₃</td>
<td>30</td>
</tr>
<tr>
<td>La₂SiO₅</td>
<td></td>
</tr>
<tr>
<td>MgAl₂O₄</td>
<td></td>
</tr>
<tr>
<td>NdAlO₃</td>
<td>22.5</td>
</tr>
<tr>
<td>PrAlO₃</td>
<td>25</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td>7</td>
</tr>
<tr>
<td>SmAlO₃</td>
<td>19</td>
</tr>
<tr>
<td>SrTiO₃</td>
<td>150-250</td>
</tr>
<tr>
<td>Ta₂O₅</td>
<td>25-24</td>
</tr>
<tr>
<td>Ta₂O₅-TiO₂</td>
<td></td>
</tr>
<tr>
<td>TiO₂</td>
<td>86-95</td>
</tr>
<tr>
<td>TiO₂/Si₃N₄</td>
<td></td>
</tr>
<tr>
<td>Y₂O₃</td>
<td>8-11.6</td>
</tr>
<tr>
<td>YₓSiᵧO₂z</td>
<td></td>
</tr>
<tr>
<td>ZrO₂</td>
<td>22.2-28</td>
</tr>
<tr>
<td>Zr-Al-O</td>
<td></td>
</tr>
<tr>
<td>Zr silicate</td>
<td></td>
</tr>
<tr>
<td>(Zr,Sn)TiO₄</td>
<td>40-60</td>
</tr>
</tbody>
</table>

√φ_B * k : Figure of Merit of High-k

C.A. Billmann et al., MRS Spring Symp., 1999
S. De Gebdt, IEDM Short Coyuse, 2004

T. Hattori, INFOS , 2003
Absorption of moisture and CO₂

The oxides become hydroxide and carbonate in H₂O and CO₂ ambient.

\[
Ln_2O_3 + H_2O \rightarrow Ln_2(OH)_3 + H_2O
\]

\[
Ln_2O_3 + H_2O \rightarrow 2(LnOOH)
\]

\[
2Ln(OH) + H_2O \rightarrow 3Ln_2(OH)_3
\]

\[
Ln_2O_3 + CO_2 \rightarrow Ln_2O_2(CO_3)
\]
Hygroscopic Properties of La$_2$O$_3$

After 30 hours in clean room (temperature & humidity controlled)
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O$^*$ $\rightarrow$ HfO$_2$ + SiO$_2$

Oxygen supplied from W gate electrode

SiO$_x$-IL is formed after annealing

Oxygen control is required for optimizing the reaction

D.J. Lichtenwalner, Trans. ECS 11, 319

H. Shimizu, JJAP, 44, pp. 6131
La-Silicate Reaction at $\text{La}_2\text{O}_3$/Si

Direct contact high-k/Si is possible

$\text{La}_2\text{O}_3 + \text{Si} + n\text{O}_2$

- $\text{La}_2\text{SiO}_5$, $\text{La}_2\text{Si}_2\text{O}_7$
- $\text{La}_{9.33}\text{Si}_6\text{O}_{26}$, $\text{La}_{10}\text{(SiO}_4)_6\text{O}_3$, etc.

$\text{La}_2\text{O}_3$ can achieve direct contact of high-k/Si
EOT<0.5nm with Gain in Drive Current

14% of $I_d$ increase is observed even at saturation region

EOT below 0.4nm is still useful for scaling
- There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

- Even after reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

- Two candidates have emerged for R & D
  1. Nanowire/tube MOSFETs
  2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.
FinFET to Nanowire

Double-Gate FinFET
\((T_{si} = \frac{2}{3} L_g)\)

Omega FinFET
\((T_{si} = L_g)\)

Nanowire FinFET
\((T_{si} = 2L_g)\)

Channel conductance is well controlled by Gate even at \(L=5\text{nm}\)

F.-L. Yang, VLSI2004
Si nanowire FET as a strong candidate after CMOS limitation

1. Compatibility with current CMOS process
2. Good controllability of $I_{OFF}$
3. High drive current

---

1D ballistic conduction

Multi quantum Channel

High integration of wires
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

300 K

\(E_g = 1.12 \text{ eV}\)
\(E_{L} = 2.0 \text{ eV}\)
\(E_{X} = 1.2 \text{ eV}\)
\(E_{e} = 0.044 \text{ eV}\)
\(E_{T1} = 3.4 \text{ eV}\)
\(E_{T2} = 4.2 \text{ eV}\)

4 channels can be used

Energy band of 3 x 3 Si wire

Energy (eV)
Maximum number of wires per 1 µm

Front gate type MOS 165 wires /µm

Surrounded gate type MOS 33 wires/µm

6nm pitch
By nano-imprint method

30nm pitch:
EUV lithography

Metal gate electrode (10nm)
High-k gate insulator (4nm)
Si Nano wire (Diameter 2nm)
Increase the number of wires towards vertical dimension
Landauer Formalism for Ballistic FET

Potential Energy

\[ dU_L(x)/dx \approx 0 \]

From \( x_{\text{max}} \) to \( x_{\text{min}} \)

\[
I_D = \frac{q}{\pi \hbar} \sum_i \int [f(E, \mu_S) - f(E, \mu_D)] T_i(E) dE
\]

From \( x_{\text{max}} \) to \( x_{\text{min}} \) \( T_i(E) \approx 1 \)

\[
I_D = G_0 \left( \frac{k_B T}{q} \right) \sum_i g_i \ln \left\{ \frac{1 + \exp \left[ \left( \frac{\mu_S - E_{i0}}{k_B T} \right) \right]}{1 + \exp \left[ \left( \frac{\mu_D - E_{i0}}{k_B T} \right) \right]} \right\}
\]
Carrier Density obtained from E-k Band

\[ |Q| = |Q_f| + |Q_b| \]

\[
\begin{align*}
|Q| &= \left| \int \sum_{i} g_i \int_{k_{i_{\text{min}}}}^{\infty} \frac{dk}{1 + \exp\left(\frac{E_i(k) - \mu_S}{k_B T}\right)} \right| \\
&\quad + \left| \int \sum_{i} g_i \int_{-\infty}^{k_{i_{\text{min}}}} \frac{dk}{1 + \exp\left(\frac{E_i(k) - \mu_D}{k_B T}\right)} \right|
\end{align*}
\]
Carrier Density obtained from Band Diagram

\[
\frac{|Q|}{C_G} = (V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q}
\]

\[
\alpha = 1 + \frac{C_P}{C_G}
\]
IV Characteristics of Ballistic SiNW FET

Small temperature dependency
35μA/wire for 4 quantum channels
Model of Carrier Scattering

Linear Potential Approx. : Electric Field $E$

Transmission Probability to Drain

$T(\varepsilon) = \frac{F(0) - G(0)}{F(0)}$ (Injection from Drain = 0)
Résumé of the Compact Model

\[ I = \frac{q}{\pi \hbar} \sum_i g_i \int [f(\varepsilon, \mu_s) - f(\varepsilon, \mu_D)] T_i \, d\varepsilon \]

\[ (V_G - V_t) - \alpha \frac{\mu_s - \mu_0}{q} = \frac{|Q_f + Q_b|}{C_G}. \]

\[ \mu_s - \mu_D = qV_D \]

\[ C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left( \frac{\sqrt{2r + t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r + t_{ox}} - \sqrt{t_{ox}}} \right)}. \]

\[ \sum_i \int_{-\infty}^{\infty} \frac{dk}{1 + \exp \left\{ \frac{\varepsilon_i(k) - \mu_s}{k_BT} \right\} - \int_{-\infty}^{0} \frac{1}{1 + \exp \left\{ \frac{\varepsilon_i(k) - \mu_s}{k_BT} \right\} - \int_{0}^{\infty} \frac{1}{1 + \exp \left\{ \frac{\varepsilon_i(k) - \mu_D}{k_BT} \right\} } T_i(\varepsilon_i(k)) \, dk \]

\[ T(\varepsilon) = \frac{\sqrt{2D_0} \, qE}{\left( \sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0B_0} \ln \left( \frac{qEx_0 + \varepsilon}{\varepsilon} \right)} \]

Unknowns are \( I_D, (\mu_s-\mu_0), (\mu_D-\mu_0), \) および \( (Q_f+Q_b) \)
I-V\textsubscript{D} Characteristics (RT)

- Electric current: 20\textendash25 \(\mu\text{A}\)
- No saturation at large \(V_{\text{D}}\)
Cross section of Si NW

First principal calculation, TAPP

D=1.96nm [001]
D=1.94nm [011]
D=1.93nm [111]
Si nanowire FET with 1D Transport

Small mass with [011]

Large number of quantum channels with [001]
SiNW FET Fabrication
Brief process flow of Si Nanowire FET

- S/D&Fin Patterining (ArF Lithography and RIE Etching)
- Sacrificial Oxidation & Oxide Removal (not completely released from BOX layer)
- Nanowire Sidewall Formation (oxide support protector)
- Gate Oxidation (5nm) & Poly-Si Deposition (75nm)
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process
(a) Fin structure formed on BOX layer. (b) XTEM image of fin shown in (a) (c) XTEM image after sacrificial oxidation (d) Cross sectional SEM image after partial removal of sacrificial oxide (e) XTEM after nanowire sidewall formation
SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oxide etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
  - Gate Lithography & RIE Etching
  - Gate Sidewall Formation
  - Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

Standard recipe for gate stack formation
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.
Fabricated SiNW FET
$I_d V_g$ and $I_d V_d$ Characteristics

$V_D=1.0V$

$V_D=0.05V$

S.S. = 71mV/dec

$V_{th}=-0.36V$

$L_g=200nm$

$V_{g-V_th}=1.0V$

$V_{g-V_th}=0.8V$

$V_{g-V_th}=0.6V$

$V_{g-V_th}=0.4V$

$I_{on}/I_{off}$ ratio of $\sim 10^7$, high $I_{on}$ of 49.6 $\mu A/wire$
Output characteristics of 10x10cm$^2$ SiNW FET

- Gate voltage (V): -1.0, -0.5, 0, 0.5, 1.0
- Drain voltage (V): 0, 0.2, 0.4, 0.6, 0.8, 1.0

$V_d=1.0V$  
$V_d=50mV$

$L_g=160nm$  
$T_{ox}=3nm$  
$(A)10x10nm^2$

$V_g-V_{th}=1.2V$ (step 0.2V)
Our roadmap for R & D
Source: H. Iwai, IWJT 2008

Current Issues
Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
  - Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap

Extended CMOS: More Moore + CMOS logic

Beyond the horizon

Si Fin, Tri-gate
Si Nano wire
III-V and Ge Nano wire
Nanowire
CNT
Tube, Ribbon
Graphene

ITRS
More Moore

Cloud
Horizon
ITRS Beyond CMOS
High conduction
By 1D conduction
Extended CMOS
More Moore ??

Research Development Production
Brain

Ultra small volume
Small number of neuron cells
Extremely low power

Real time image processing
(Artificial) Intelligence
3D flight control

Sensor

Infrared
Humidity
CO₂

Mosquito

System and Algorism becomes more important!

But do not know how?

Dragonfly is further high performance