Si Nanoelectronic Device Technology

IEEE EDS WIMNACT 23

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Tokyo Institute of Technology

Frontier Research Center

Hiroshi Iwai
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
Institute Overview

Established in 1881 → 130th anniversary in 2011
3 undergraduate schools
   School of Science, School of Engineering, School of Bioscience and Biotechnology
7 graduate schools
   Science and Engineering Science, Science and Engineering Technology, Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering, Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

<table>
<thead>
<tr>
<th></th>
<th>Undergraduate</th>
<th>Graduate</th>
<th>Master’s</th>
<th>Doctoral</th>
<th>Teaching Staff</th>
<th>Student/Instructor</th>
<th>Staff</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tokyo Inst.</td>
<td>5,000</td>
<td>5,000</td>
<td>3,500</td>
<td>1,500</td>
<td>1,200</td>
<td>8.3</td>
<td>550</td>
</tr>
<tr>
<td>Per Year</td>
<td>1,200</td>
<td></td>
<td>1,800</td>
<td></td>
<td>500</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Asia 847
Europe 78
Africa 16
North America 12
South America 24
Oceania 5
Total 982
(As of May. 1, 2005)
Tokyo Institute of Technology

Interdisciplinary Graduate School of Science and Engineering

- 5 other schools
- 4 Laboratories

Frontier Research Center

- Consists of about 10 professor who have big projects

G CEO (Global Center of Excellence) for Photonics Nanodevice Integration Engineering

- Other GCEO

Dept. of Electronics and Physics

- 10 other dept.

2 major campuses
Ookayama, Tokyo
5000 Undergraduate students
Suzukakedai, Yokohama
5000 Graduate Students

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2 major campuses
Ookayama, Tokyo
5000 Graduate Students
Suzukakedai, Yokohama

Innovation Research Initiatives (革新的研究集団)
Interdisciplinary Graduate School of Science and Engineering
大学院総合理工学研究科

J2 Building:
Frontier Collaborative Research Center (FCRC)
先端創造共同研究中心
**Iwai Lab. Equipment**

- **MBE and Sputter Chamber**
- **Sputter Chamber**
- **MBE Chamber**
- **RTA Furnace No.1**
- **RTA Furnace No.2**
- **RF measurement system; 8 inch wafer, 40 GHz**
- **1/f noise measurement system; 6 inch wafer**

**Back Pressure:**
- During Deposition: $10^{-7}$ Pa
- Deposition rate: 0.1 to 1 nm/min

**Deposition rate:** 0.1 to 1 nm/min
Importance of Electronics

• There were many inventions in the 20\textsuperscript{th} century: Airplane, Nuclear Power generation, Computer, Space aircraft, etc

• However, everything has to be controlled by electronics

• Electronics
  Most important invention in the 20\textsuperscript{th} century

• What is Electronics: To use electrons, Electronic Circuits
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Same mechanism as that of transistor
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power consumption
J.E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928

J.E. LILIENFELD
Capacitor structure with notch

Negative bias

Gate Electrode
Gate Insulator
Semiconductor
Electron
No current

Positive bias

Electric field
Current flows
Today’s transistor: MOSFET for CMOS LSI

Surface Potential (Negative direction)

0 bias for gate

Positive bias for gate

Electron flow
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator. Even Shockley!

Drain Current was several orders of magnitude smaller than expected.

Even Shockley!
However, they found amplification phenomenon when investigating Ge surface when putting needles. This is the 1st Transistor:

Not Field Effect Transistor, But Bipolar Transistor (another mechanism)

1947: 1st transistor

Bipolar using Ge

J. Bardeen

W. Bratten,

W. Shockley
1958: 1st Integrated Circuit

Connect 2 bipolar transistors in the Same substrate by bonding wire.

Jack S. Kilby
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source
Drain
Al Gate
Si
SiO₂
Al
Si

Si/SiO₂ Interface is extraordinarily good
1970,71: 1st generation of LSIs

DRAM Intel 1103

MPU Intel 4004
MOS LSI experienced continuous progress for many years

<table>
<thead>
<tr>
<th>Name of Integrated Circuits</th>
<th>Number of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>1960s IC (Integrated Circuits)</td>
<td>~10</td>
</tr>
<tr>
<td>1970s LSI (Large Scale Integrated Circuit)</td>
<td>~1,000</td>
</tr>
<tr>
<td>1980s VLSI (Very Large Scale IC)</td>
<td>~10,000</td>
</tr>
<tr>
<td>1990s ULSI (Ultra Large Scale IC)</td>
<td>~1,000,000</td>
</tr>
<tr>
<td>2000s ?LSI (? Large Scale IC)</td>
<td>~1,000,000,000</td>
</tr>
</tbody>
</table>
MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Use Gate Field Effect for switching

Gate Electrode
Poly Si

Gate Insulator
SiO₂

Substrate
Si

Source

Channel

N-MOS (N-type MOSFET)

Drain

Si Substrate
Complimentary MOS

When NMOS is ON, PMOS is OFF
When PMOS is ON, NMOS is OFF
CMOS Technology:  
Indispensable for our human society

All the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:
There is no computer in banks, and
world economical activities immediately stop.

Cellarer phone dose not exists
Downsizing of the components has been the driving force for circuit evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Vacuum Tube</th>
<th>Transistor</th>
<th>IC</th>
<th>LSI</th>
<th>ULSI</th>
</tr>
</thead>
<tbody>
<tr>
<td>1900</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1950</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1960</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1970</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

10 cm  cm  mm  10 µm  100 nm

10^{-1}m  10^{-2}m  10^{-3}m  10^{-5}m  10^{-7}m

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. **Reduce Capacitance**
   - ➔ Reduce switching time of MOSFETs
   - ➔ Increase clock frequency
     - ➔ Increase circuit operation speed

2. **Increase number of Transistors**
   - ➔ Parallel processing
     - ➔ Increase circuit operation speed

Thus, downsizing of Si devices is the most important and critical issue.
Scaling Method: by R. Dennard in 1974

**Wdep**: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed. Otherwise, large leakage between S and D.

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

**K=0.7 for example**

\[ \begin{align*}
X, Y, Z &: K, \\
V &: K, \\
\text{Na} &: 1/K
\end{align*} \]

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

Good scaled I-V characteristics

\[ \text{Wdep} \propto \sqrt{V/\text{Na}} : K \]
### Downscaling merit: Beautiful!

<table>
<thead>
<tr>
<th>Geometry &amp; Supply voltage</th>
<th>( L_g, W_g, T_{ox}, V_{dd} )</th>
<th>( K )</th>
<th><strong>Scaling</strong> ( K : K=0.7 ) for example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive current in saturation</td>
<td>( I_d )</td>
<td>( K )</td>
<td>( I_d = v_{sat} W_g C_o (V_g - V_{th}) ) ( C_o ): gate C per unit area</td>
</tr>
<tr>
<td>( I_d ) per unit ( W_g )</td>
<td>( I_d / \mu m )</td>
<td>1</td>
<td>( I_d ) per unit ( W_g = I_d / W_g = 1 )</td>
</tr>
<tr>
<td>Gate capacitance</td>
<td>( C_g )</td>
<td>( K )</td>
<td>( C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox} ) ( \rightarrow ) KK/K = K</td>
</tr>
<tr>
<td>Switching speed</td>
<td>( \tau )</td>
<td>( K )</td>
<td>( \tau = C_g V_{dd} / I_d ) ( \rightarrow ) KK/K = K</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>( f )</td>
<td>1/K</td>
<td>( f = 1/\tau = 1/K )</td>
</tr>
<tr>
<td>Chip area</td>
<td>( A_{chip} )</td>
<td>( \alpha )</td>
<td>( \alpha ): Scaling factor ( \rightarrow ) In the past, ( \alpha&gt;1 ) for most cases</td>
</tr>
<tr>
<td>Integration (# of Tr)</td>
<td>( N )</td>
<td>( \alpha/K^2 )</td>
<td>( N ) ( \rightarrow ) ( \alpha/K^2 ) ( = 1/K^2 ), when ( \alpha=1 )</td>
</tr>
<tr>
<td>Power per chip</td>
<td>( P )</td>
<td>( \alpha )</td>
<td>( fNCV^2/2 ) ( \rightarrow ) ( K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha ) ( = 1 ), when ( \alpha=1 )</td>
</tr>
<tr>
<td></td>
<td>( k = 0.7 ) and ( \alpha = 1 )</td>
<td>( k = 0.7^2 = 0.5 ) and ( \alpha = 1 )</td>
<td></td>
</tr>
<tr>
<td>----------------------</td>
<td>-------------------------------------</td>
<td>------------------------------------------</td>
<td></td>
</tr>
<tr>
<td><strong>Single MOFET</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{dd} \rightarrow 0.7 )</td>
<td></td>
<td>( V_{dd} \rightarrow 0.5 )</td>
<td></td>
</tr>
<tr>
<td>( L_g \rightarrow 0.7 )</td>
<td></td>
<td>( L_g \rightarrow 0.5 )</td>
<td></td>
</tr>
<tr>
<td>( I_d \rightarrow 0.7 )</td>
<td></td>
<td>( I_d \rightarrow 0.5 )</td>
<td></td>
</tr>
<tr>
<td>( C_g \rightarrow 0.7 )</td>
<td></td>
<td>( C_g \rightarrow 0.5 )</td>
<td></td>
</tr>
<tr>
<td>( P ) (Power)/Clock</td>
<td>( 0.7^3 = 0.34 )</td>
<td>( 0.5^3 = 0.125 )</td>
<td></td>
</tr>
<tr>
<td>( \tau ) (Switching time)</td>
<td>0.7</td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td><strong>Chip</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( N ) (# of Tr)</td>
<td>( 1/0.7^2 = 2 )</td>
<td>( 1/0.5^2 = 4 )</td>
<td></td>
</tr>
<tr>
<td>( f ) (Clock)</td>
<td>( 1/0.7 = 1.4 )</td>
<td>( 1/0.5 = 2 )</td>
<td></td>
</tr>
<tr>
<td>( P ) (Power)</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>
Actual past downscaling trend until year 2000

Change in 30 years

<table>
<thead>
<tr>
<th>Ideal scaling</th>
<th>Real Change</th>
<th>Ideal scaling</th>
<th>Real Change</th>
<th>Ideal scaling</th>
<th>Real Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$</td>
<td>$K$</td>
<td>$10^{-2}$</td>
<td>$10^{-2}$</td>
<td>$I_d$</td>
<td>$K(10^{-2})$</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-1}$</td>
<td></td>
<td>$I_d/\mu m$</td>
<td>$1$</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-1}$</td>
<td></td>
<td>$N$</td>
<td>$\alpha/K^2(10^5)$</td>
</tr>
<tr>
<td>$A_{chip}$</td>
<td>$\alpha$</td>
<td>$10^1$</td>
<td></td>
<td>$P$</td>
<td>$\alpha(10^1)$</td>
</tr>
</tbody>
</table>

Past 30 years scaling
Merit: $N$, $f$ increase
Demerit: $P$ increase

$V_{dd}$ scaling insufficient
Additional significant increase in $I_d$, $f$, $P$

Vd scaling insufficient, $\alpha$ increased $\rightarrow$ $N$, $I_d$, $f$, $P$ increased significantly

Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1µm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5µm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25µm:</td>
<td>Direct-tunneling of gate SiO₂</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1µm:</td>
<td>‘0.1µm brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
Historically, many predictions of the limit of downsizing. VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.
Finally, there appears to be a fundamental limit of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide begin to make the devices of smaller dimension unworkable.
Direct-tunneling effect

Gate Electrode  Gate Oxide  Potential Barrier  Si Substrate

Wave function  Direct tunneling current

Direct tunneling leakage current start to flow when the thickness is 3 nm.
Direct tunneling leakage was found to be OK! In 1994!
Gate leakage: $I_g \propto \text{Gate Area} \propto \text{Gate length (Lg)}$

Drain current: $I_d \propto 1/\text{Gate length (Lg)}$

$L_g \to \text{small},$

Then, $I_g \to \text{small}, I_d \to \text{large},$ Thus, $I_g/I_d \to \text{very small}$
Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!

Some one will think for you
Transistor Scaling Continues

Qi Xinag, ECS 2004, AMD
Downsizing limit?

Electron wave length

Channel length?

10 nm
5 nm gate length CMOS
Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et. al, NEC
IEDM, 2003
Electron wave length
10 nm

Tunneling distance
3 nm

Downsizing limit!
Channel length
Gate oxide thickness
Prediction now!

Electron wave length
10 nm

Tunneling distance
3 nm

Atom distance
0.3 nm

MOSFET operation
Lg = 3 nm?

Below this, no one knows future!
However, Gate oxide thickness 2 orders magnitude smaller Close to limitation!!

Lg: Gate length downsizing will continue to another 10-15 years
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
So, we are now in the limitation of downsizing?

Do you believe this or do not?
There is a solution! To use high-k dielectrics

K: Dielectric Constant

Thin gate SiO₂

Almost the same electric characteristics

Thick gate high-k dielectrics

Thick
Small leakage Current

However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO₂!
Candidates □

Unstable at Si interface

- Si + MO\textsubscript{X} M + SiO\textsubscript{2}
- Si + MO\textsubscript{X} MSi\textsubscript{X} + SiO\textsubscript{2}
- Si + MO\textsubscript{X} M + MSi\textsubscript{X}O\textsubscript{Y}

Gas or liquid at 1000 K

Radio active

He

B C N O F Ne

Al Si P S Cl Ar

K Ca Sc Ti V Cr Mn Fe Co Ni Cu Zn Ga Ge As Se Br Kr

Sr Y Zr Nb Mo Tc Ru Rh Pd Ag Cd In Sn Sb Te I Xe

Cs Ba Hf Ta W Re Os Ir Pt Au Hg Ti Pb Bi Po At Rn

Fr Ra Ac Th Pa U Np Pu Am Cm Bk Cf Es Fm Md No Lr

HfO\textsubscript{2} based dielectrics are selected as the first generation materials, because of their merit in 1) band-offset, 2) dielectric constant, 3) thermal stability.

La\textsubscript{2}O\textsubscript{3} based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

R. Hauser, IEDM Short Course, 1999
**Dielectric constant**

- SiO$_2$: 4
- Si$_3$N$_4$: ~7
- Al$_2$O$_3$: ~9
- Y$_2$O$_3$: ~10
- Gd$_2$O$_3$: ~10
- HfO$_2$: ~23
- La$_2$O$_3$: ~27

HfO$_2$ was chosen for the 1st generation
La$_2$O$_3$ is more difficult material to treat

Dielectric constant value vs. Band offset (Measured)

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>3.9</td>
</tr>
<tr>
<td>Al$_x$Si$_y$O$_z$</td>
<td></td>
</tr>
<tr>
<td>(Ba,Sr)TiO$_3$</td>
<td>200-300</td>
</tr>
<tr>
<td>BeAl$_2$O$_4$</td>
<td>8.3-9.43</td>
</tr>
<tr>
<td>CeO$_2$</td>
<td>16.6-26</td>
</tr>
<tr>
<td>CeHfO$_4$</td>
<td>10-20</td>
</tr>
<tr>
<td>CoTiO$_3$/Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>EuAlO$_3$</td>
<td>22.5</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>26-30</td>
</tr>
<tr>
<td>Hf silicate</td>
<td>11</td>
</tr>
<tr>
<td>La$_2$O$_3$</td>
<td>20.8</td>
</tr>
<tr>
<td>LaScO$_3$</td>
<td>30</td>
</tr>
<tr>
<td>La$_2$SiO$_5$</td>
<td></td>
</tr>
<tr>
<td>MgAl$_2$O$_4$</td>
<td></td>
</tr>
<tr>
<td>NdAlO$_3$</td>
<td>22.5</td>
</tr>
<tr>
<td>PrAlO$_3$</td>
<td>25</td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
<td>7</td>
</tr>
<tr>
<td>SmAlO$_3$</td>
<td>19</td>
</tr>
<tr>
<td>SrTiO$_3$</td>
<td>150-250</td>
</tr>
<tr>
<td>Ta$_2$O$_5$</td>
<td>25-24</td>
</tr>
<tr>
<td>Ta$_2$O$_5$-TiO$_2$</td>
<td></td>
</tr>
<tr>
<td>TiO$_2$</td>
<td>86-95</td>
</tr>
<tr>
<td>TiO$_2$/Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>Y$_2$O$_3$</td>
<td>8-11.6</td>
</tr>
<tr>
<td>Y$_x$Si$_y$O$_z$</td>
<td></td>
</tr>
<tr>
<td>ZrO$_2$</td>
<td>22.2-28</td>
</tr>
<tr>
<td>Zr-Al-O</td>
<td></td>
</tr>
<tr>
<td>Zr silicate</td>
<td></td>
</tr>
<tr>
<td>(Zr,Sn)TiO$_4$</td>
<td>40-60</td>
</tr>
</tbody>
</table>

\[ \sqrt{\phi_B} \ast k \] : Figure of Merit of High-k

C.A. Billmann et al., MRS Spring Symp., 1999
S. De Gebdt, IEDM Short Coyuse, 2004
T. Hattori, INFOS, 2003
Absorption of moisture and CO$_2$

The oxides become hydroxide and carbonate in H$_2$O and CO$_2$ ambient.

$\text{Ln}_2\text{O}_3 + \text{H}_2\text{O} \rightleftharpoons \text{Ln}_2\text{O}_3 \cdot \text{H}_2\text{O}$

$\text{Ln}_2\text{O}_3 + \text{H}_2\text{O} \rightleftharpoons 2(\text{LnOOH})$

$2\text{Ln} (\text{OH}) + \text{H}_2\text{O} \rightleftharpoons 3\text{Ln}_2 (\text{OH})_3$

$\text{Ln}_2\text{O}_3 + \text{CO}_2 \rightleftharpoons \text{Ln}_2\text{O}_2(\text{CO}_3)$

$\text{Ln}$: Lanthanide
Hygroscopic Properties of $\text{La}_2\text{O}_3$

After 30 hours in clean room (temperature & humidity controlled)
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O* $\rightarrow$ HfO$_2$ + SiO$_2$

H. Shimizu, JJAP, 44, pp. 6131

SiO$_x$-IL is formed after annealing
Oxygen control is required for optimizing the reaction

D.J. Lichtenwalner, Trans. ECS 11, 319
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

$\text{La}_2\text{O}_3 + \text{Si} + n\text{O}_2 \rightarrow \text{La}_9.33\text{Si}_6\text{O}_{26}, \text{La}_{10}(\text{SiO}_4)_6\text{O}_3, \text{etc.}$

La$_2$O$_3$ can achieve direct contact of high-k/Si
EOT<0.5nm with Gain in Drive Current

14% of $I_d$ increase is observed even at saturation region

EOT below 0.4nm is still useful for scaling
- There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

- Even after reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher $I_d$-sat under low $V_{dd}$.

- Two candidates have emerged for R & D
  1. Nanowire/tube MOSFETs
  2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.

*5.5nm? was added by Iwai*
FinFET to Nanowire

Channel conductance is well controlled by Gate even at L=5nm

F.-L.Yang, VLSI2004
Si nanowire FET as a strong candidate

1. Compatibility with current CMOS process

2. Good controllability of $I_{OFF}$

3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Maximum number of wires per 1 µm

Front gate type MOS  165 wires /µm

Surrounded gate type MOS  33 wires/µm

6nm pitch
By nano-imprint method

6nm pitch
Metal gate electrode(10nm)
High-k gate insulator (4nm)
Si Nano wire (Diameter 2nm)

30nm pitch: EUV lithograpy

Surrounded gate MOS
Increase the number of wires towards vertical dimension
Landauer Formalism for Ballistic FET

Potential Energy

\[
dU_L(x) / dx \approx 0
\]

\[
I_D = \frac{q}{\pi \hbar} \sum_i \int [f(E, \mu_S) - f(E, \mu_D)] T_i(E) dE
\]

From \(x_{\text{max}}\) to \(x_{\text{min}}\) \(T_i(E) \approx 1\)

\[
I_D = G_0 \left( \frac{k_B T}{q} \right) \sum_i g_i \ln \left\{ \frac{1 + \exp\left[ (\mu_S - E_{i0}) / k_B T \right]}{1 + \exp\left[ (\mu_D - E_{i0}) / k_B T \right]} \right\}
\]
Carrier Density obtained from E-k Band

\[ |Q| = |Q_f| + |Q_b| \]

\[ = \frac{q}{\pi} \sum_i g_i \left[ \int_{k_{i_{\text{min}}}}^{\infty} \frac{dk}{1 + \exp\left(\frac{E_i(k) - \mu_S}{k_B T}\right)} + \int_{-\infty}^{k_{i_{\text{min}}}} \frac{dk}{1 + \exp\left(\frac{E_i(k) - \mu_D}{k_B T}\right)} \right] \]
Carrier Density obtained from Band Diagram

\[ \frac{|Q|}{C_G} = (V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} \]

\[ \alpha = 1 + \frac{C_P}{C_G} \]
IV Characteristics of Ballistic SiNW FET

Small temperature dependency
35\(\mu\)A/wire for 4 quantum channels
Model of Carrier Scattering

Linear Potential Approx. : Electric Field \( E \)

\[ T(\varepsilon) = \frac{F(0) - G(0)}{F(0)} \]

Transmission Probability to Drain

Injection from Drain = 0
Résumé of the Compact Model

\[
I = \frac{q}{\pi \hbar} \sum_i g_i \int \left[ f(\varepsilon, \mu_s) - f(\varepsilon, \mu_D) \right] T_i d\varepsilon
\]

\[
(V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{Q_f + Q_b}{C_G}.
\]

\[
\mu_S - \mu_D = qV_D
\]

\[
I = \frac{q}{\pi \hbar} \sum_i g_i \int \left[ f(\varepsilon, \mu_s) - f(\varepsilon, \mu_D) \right] T_i d\varepsilon
\]

\[
C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left( \frac{\sqrt{2r + t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r + t_{ox}} - \sqrt{t_{ox}}} \right)}.
\]

Planar Gate

\[
(Carrier distribution in Subbands)
\]

\[
T(\varepsilon) = \frac{\sqrt{2D_0} qE}{\left( \sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0} B_0 \ln \left( \frac{qEx_0 + \varepsilon}{\varepsilon} \right)}
\]

Unknowns are \(I_D, (\mu_S - \mu_0), (\mu_D - \mu_0), \) および \((Q_f + Q_b)\)
I-V_D Characteristics (RT)

- Electric current: 20~25 µA
- No saturation at Large V_D
Cross section of Si NW

First principal calculation, TAPP

D=1.96nm [001]  D=1.94nm [011]  D=1.93nm [111]
Si nanowire FET with 1D Transport

Orientation  [001]  [011]  [111]
Diameter (nm) 0.86 0.94 0.89

Energy (eV)

(a)

Small mass with [011]

Large number of quantum channels with [001]
SiNW FET Fabrication
Brief process flow of Si Nanowire FET

1. S/D&Fin Patterining (ArF Lithography and RIE Etching)
2. Sacrificial Oxidation & Oxide Removal (not completely released from BOX layer)
3. Nanowire Sidewall Formation (oxide support protector)
4. Gate Oxidation (5nm) & Poly-Si Deposition (75nm)
5. Gate Lithography & RIE Etching
6. Gate Sidewall Formation
7. Ni SALISIDE Process
(a) Fin structure formed on BOX layer. (b) XTEM image of fin shown in (a). (c) XTEM image after sacrificial oxidation. (d) Cross-sectional SEM image after partial removal of sacrificial oxide. (e) XTEM after nanowire sidewall formation.
SiNW FET Fabrication

1. S/D & Fin Patterning
2. Sacrificial Oxidation
3. Oxide etch back
4. SiN sidewall support formation
5. Gate Oxidation & Poly-Si Deposition
6. Gate Lithography & RIE Etching
7. Gate Sidewall Formation
8. Ni SALISIDE Process (Ni 9nm / TiN 10nm)
9. Backend

Standard recipe for gate stack formation
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.
Fabricated SiNW FET

SiNW

SiN support

30nm

Poly-Si

500nm
IdVg and IdVd Characteristics

I_{on}/I_{off} ratio of \sim 10^7, high I_{on} of 49.6 \mu A/wire
Output characteristics of 10x10cm² SiNW FET

- Gate voltage (V): -1.0 -0.5 0 0.5 1.0
- Vd=1.0V
- Vd=50mV
- Lg=160nm
- Tox=3nm
- (A)10x10nm²

Drain current (A) vs gate voltage (V)

Drain current (µA) vs drain voltage (V)

Vg-Vth=1.2V (step 0.2V)
Our roadmap for R & D

Source: H. Iwai, IWJT 2008

Current Issues

Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
  - Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Brain
Ultra small volume
Small number of neuron cells
Extremely low power
Real time image processing
(Artificial) Intelligence
3D flight control

System and Algorism becomes more important!
But do not know how?

Sensor
Infrared
Humidity
CO$_2$

Dragonfly is further high performance
Thank you for your attention