Past and Future of Integrated Circuits Technology

@Jiangxi University of Finance & Economics

江西財経大学、南昌

March 15, 2010

東京工業大学
Tokyo Institute of Technology

先端研究中心
Frontier Research Center

岩井　洋　Hiroshi Iwai

Tokyo Institute of Technology

Founded in 1881, Promoted to Univ. 1929

Institute Overview

Einstein Visit

Established in 1881→ 130th anniversary in 2011

3 undergraduate schools

School of Science, School of Engineering, School of Bioscience and Biotechnology

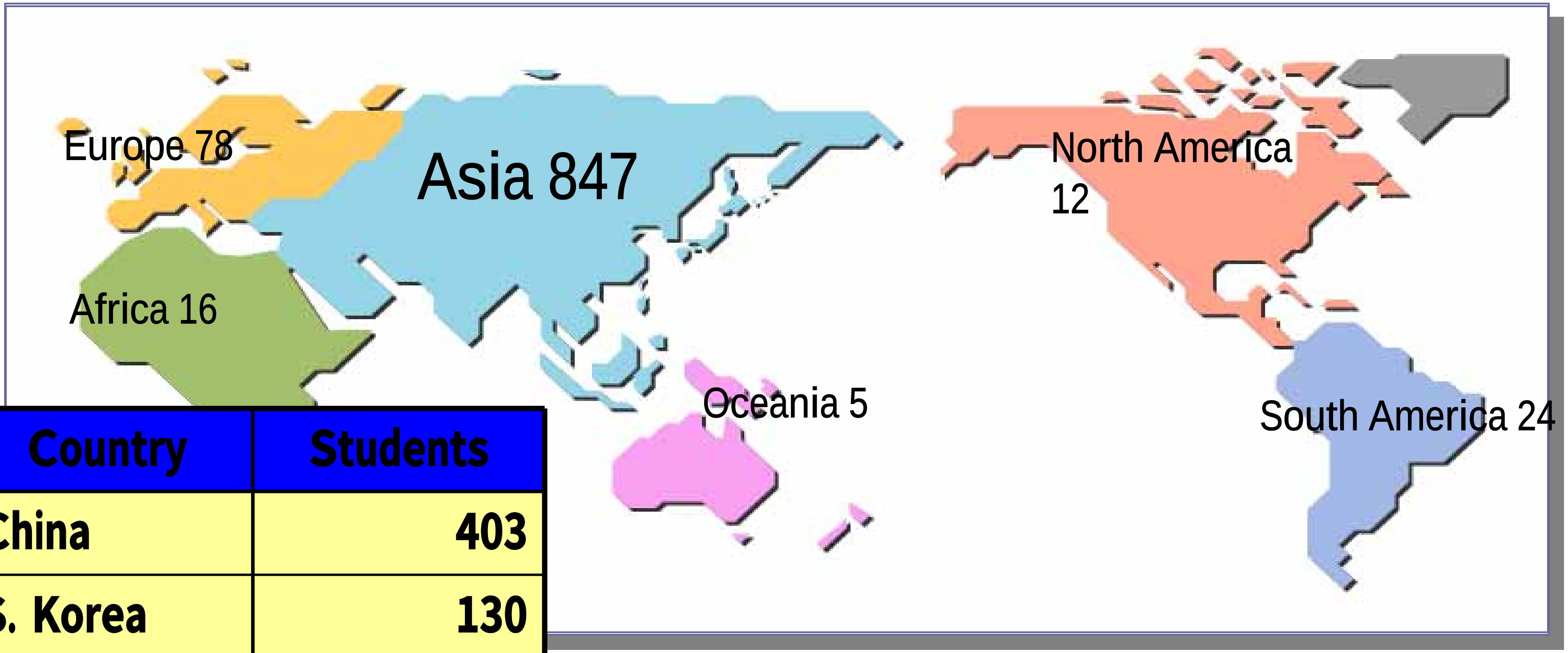
7 graduate schools

Science and Engineering Science, Science and Engineering Technology,
Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

	Undergraduate	Graduate	Master's	Doctoral	Teaching Staff	Student/Instructor	Staff
Tokyo Inst.	**5,000**	**5,000**	**3,500**	**1,500**	**1,200**	**8.3**	**550**
Per Year	**1,200**		**1,800**	**500**			

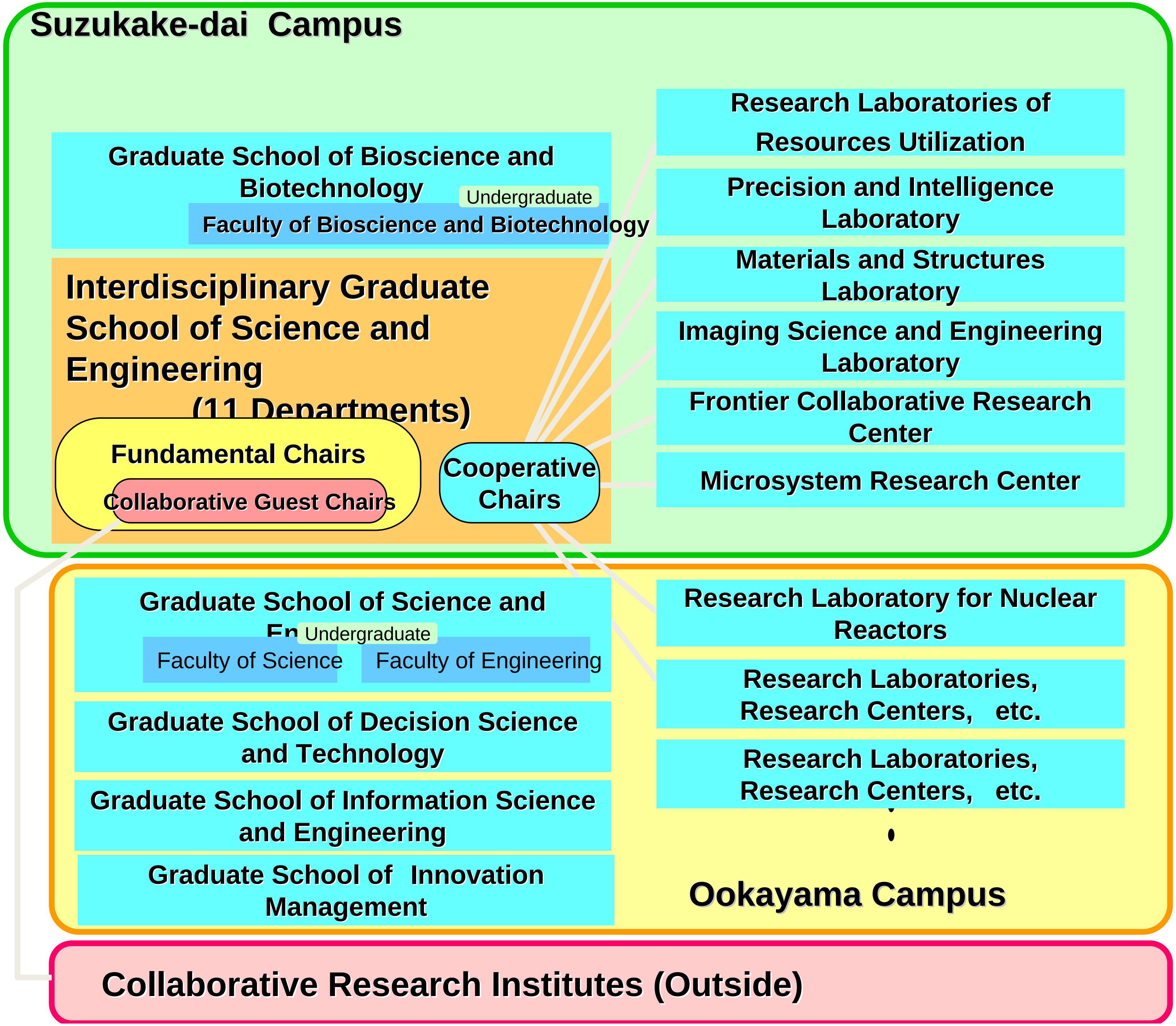
International Students



Country	Students
China	403
S. Korea	130
Indonesia	64
Thailand	55
Vietnam	60
Malaysia	28

Total 982

(As of May. 1, 2005)



Suzukake-dai Campus

Graduate School of Bioscience and Biotechnology

Undergraduate

Faculty of Bioscience and Biotechnology

Interdisciplinary Graduate School of Science and Engineering
(11 Departments)

Fundamental Chairs

Collaborative Guest Chairs

Cooperative Chairs

Research Laboratories of Resources Utilization

Precision and Intelligence Laboratory

Materials and Structures Laboratory

Imaging Science and Engineering Laboratory

Frontier Collaborative Research Center

Microsystem Research Center

Graduate School of Science and En

Undergraduate

Faculty of Science

Faculty of Engineering

Graduate School of Decision Science and Technology

Graduate School of Information Science and Engineering

Graduate School of Innovation Management

Research Laboratory for Nuclear Reactors

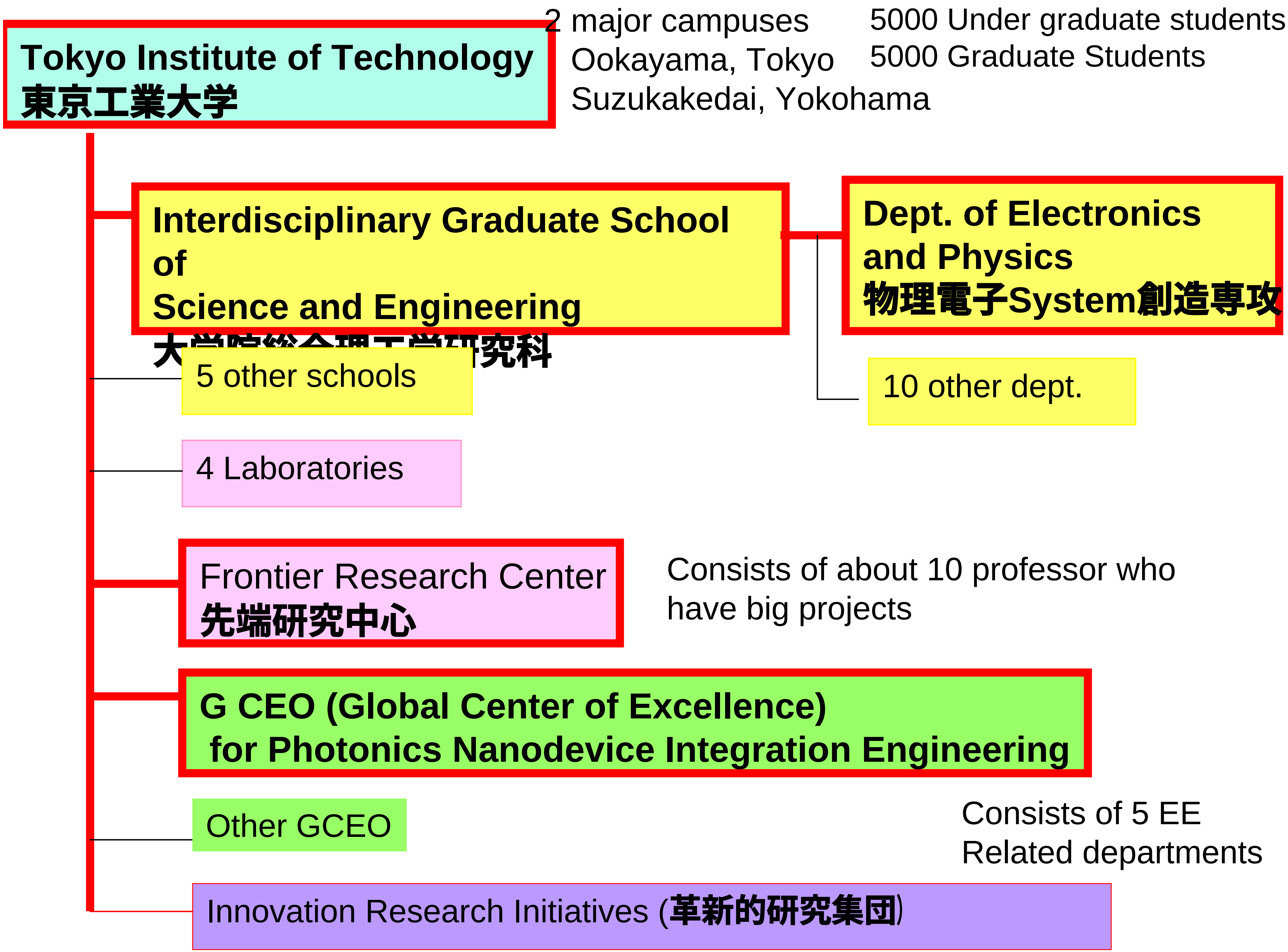
Research Laboratories, Research Centers, etc.

Research Laboratories, Research Centers, etc.

⋮

Ookayama Campus

Collaborative Research Institutes (Outside)



Tokyo Institute of Technology
東京工業大学

2 major campuses
Ookayama, Tokyo
Suzukakedai, Yokohama

5000 Under graduate students
5000 Graduate Students

Interdisciplinary Graduate School of Science and Engineering
大学院総合理工学研究科

Dept. of Electronics and Physics
物理電子System創造専攻

5 other schools

10 other dept.

4 Laboratories

Frontier Research Center
先端研究中心

Consists of about 10 professor who have big projects

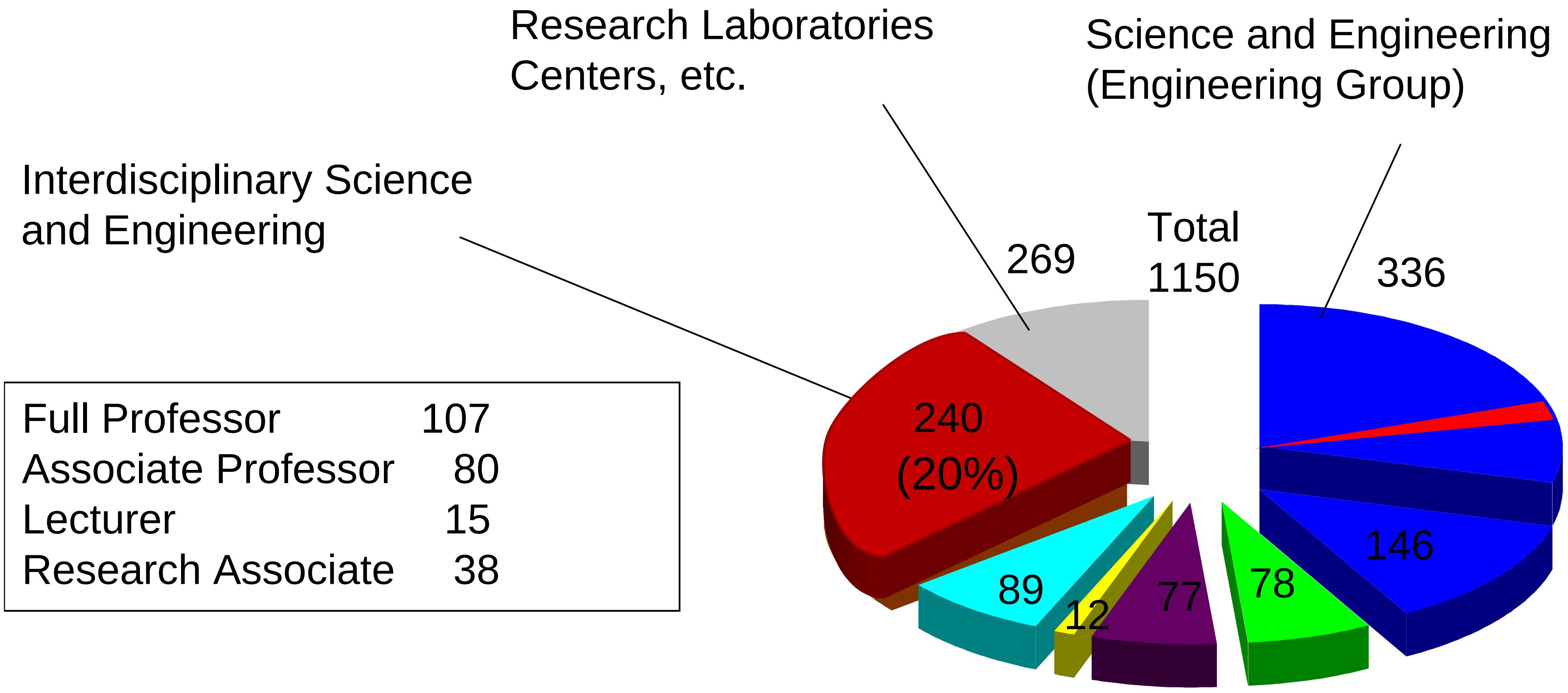
G CEO (Global Center of Excellence)
for Photonics Nanodevice Integration Engineering

Other GCEO

Consists of 5 EE
Related departments

Innovation Research Initiatives (**革新的研究集団**)

Number of Teaching Staffs



Full Professor	107
Associate Professor	80
Lecturer	15
Research Associate	38

(Spring, 2006)

Students

 # Students

	in IGS	in Titech
Undergraduate Course		5001 (307)
Master’s Course	1125 (48)	3547 (249)
Doctoral Course	482 (80)	1533 (322)

() : # students from overseas

Enrollment

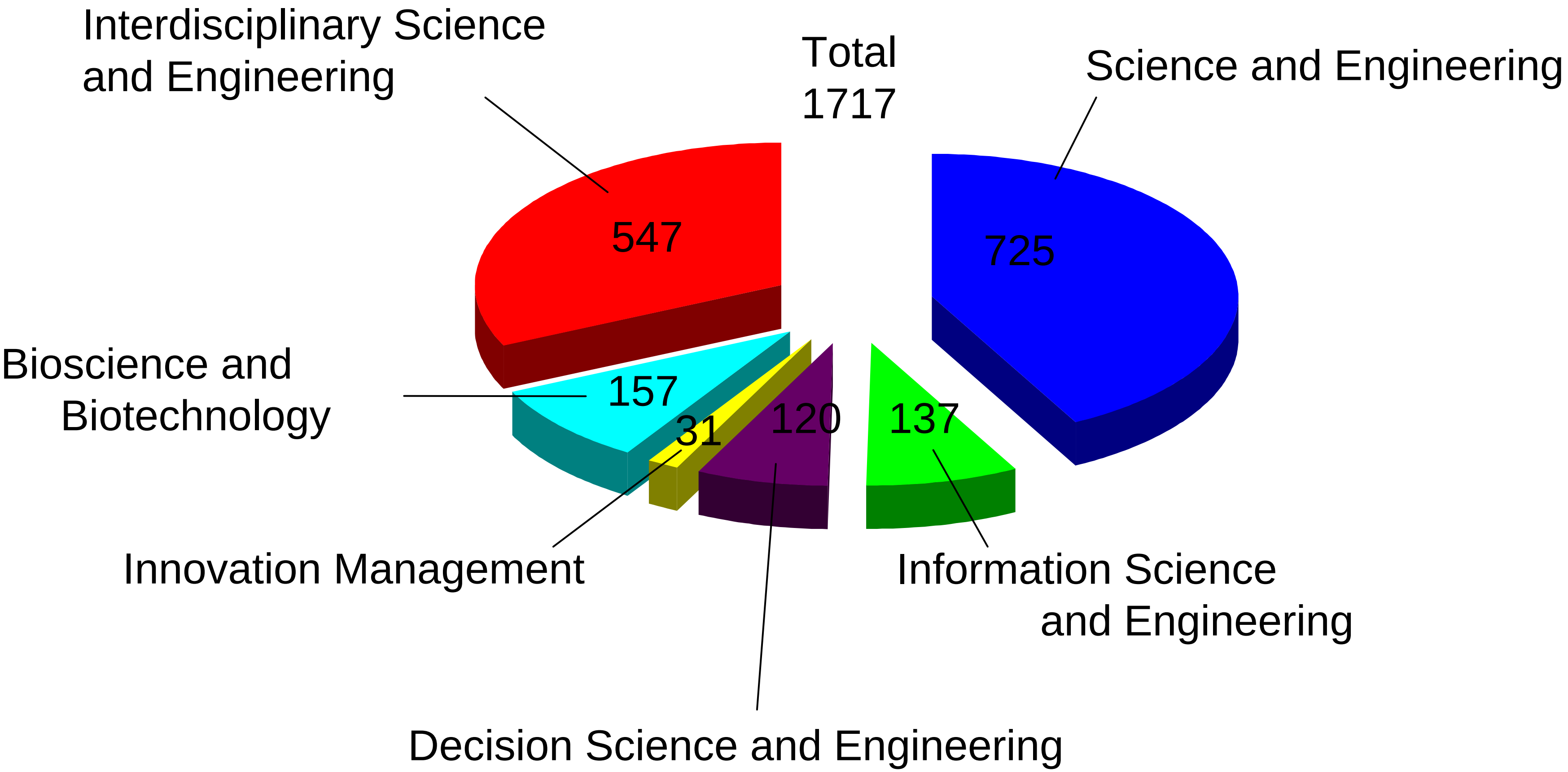
Master’s Course 5≃50, Doctoral Course 140 ≃

Master’s course : enrolled from other universities.
students of various backgrounds
Doctoral course : increase in # working students

(Spring, 2006)

Number of Students (Enrolled in Oct., 2005-Apr.,2006)

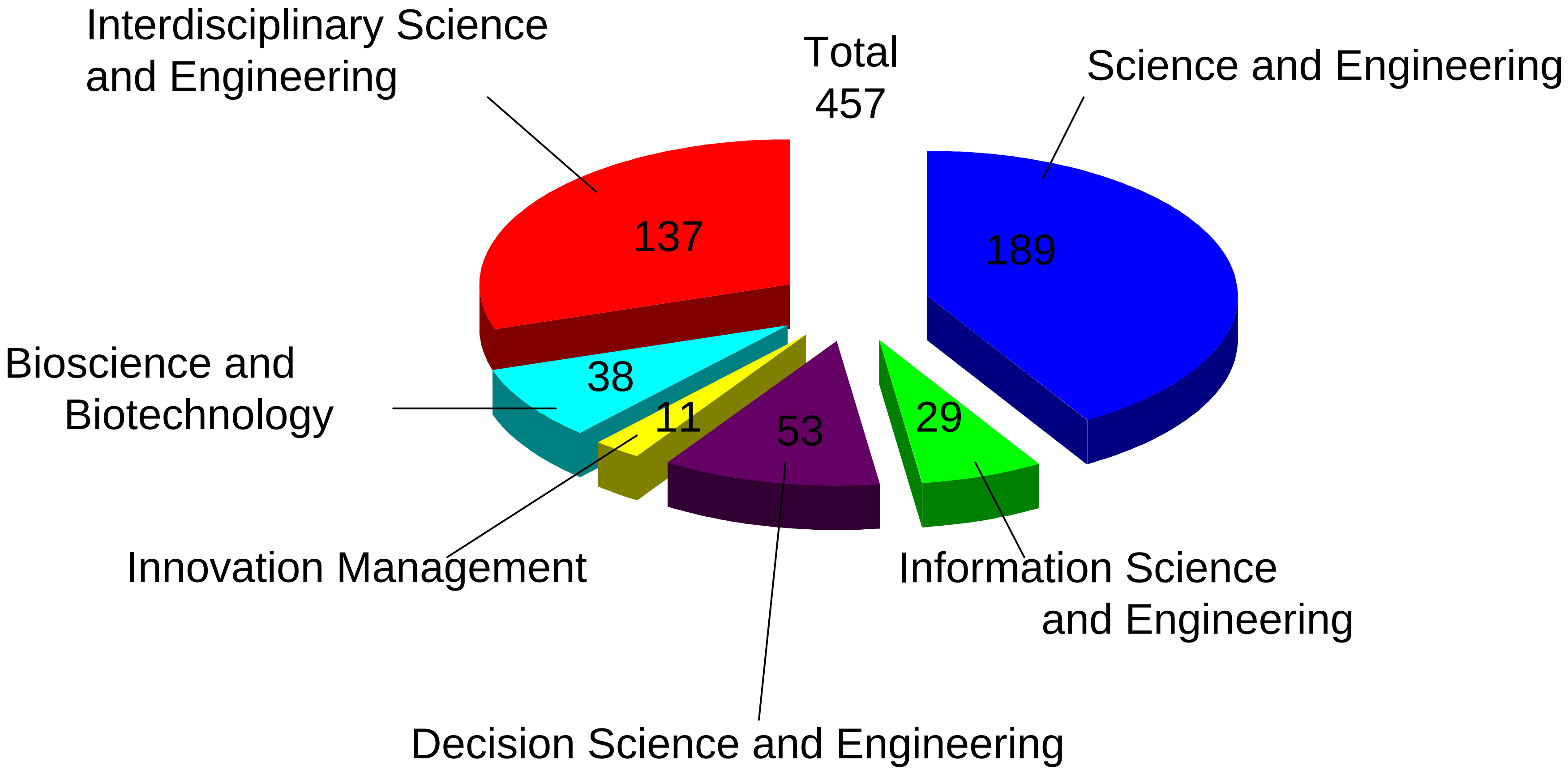
Master's Course



(Spring, 2006)

Number of Students (Enrolled in Oct., 2005-Apr.,2006)

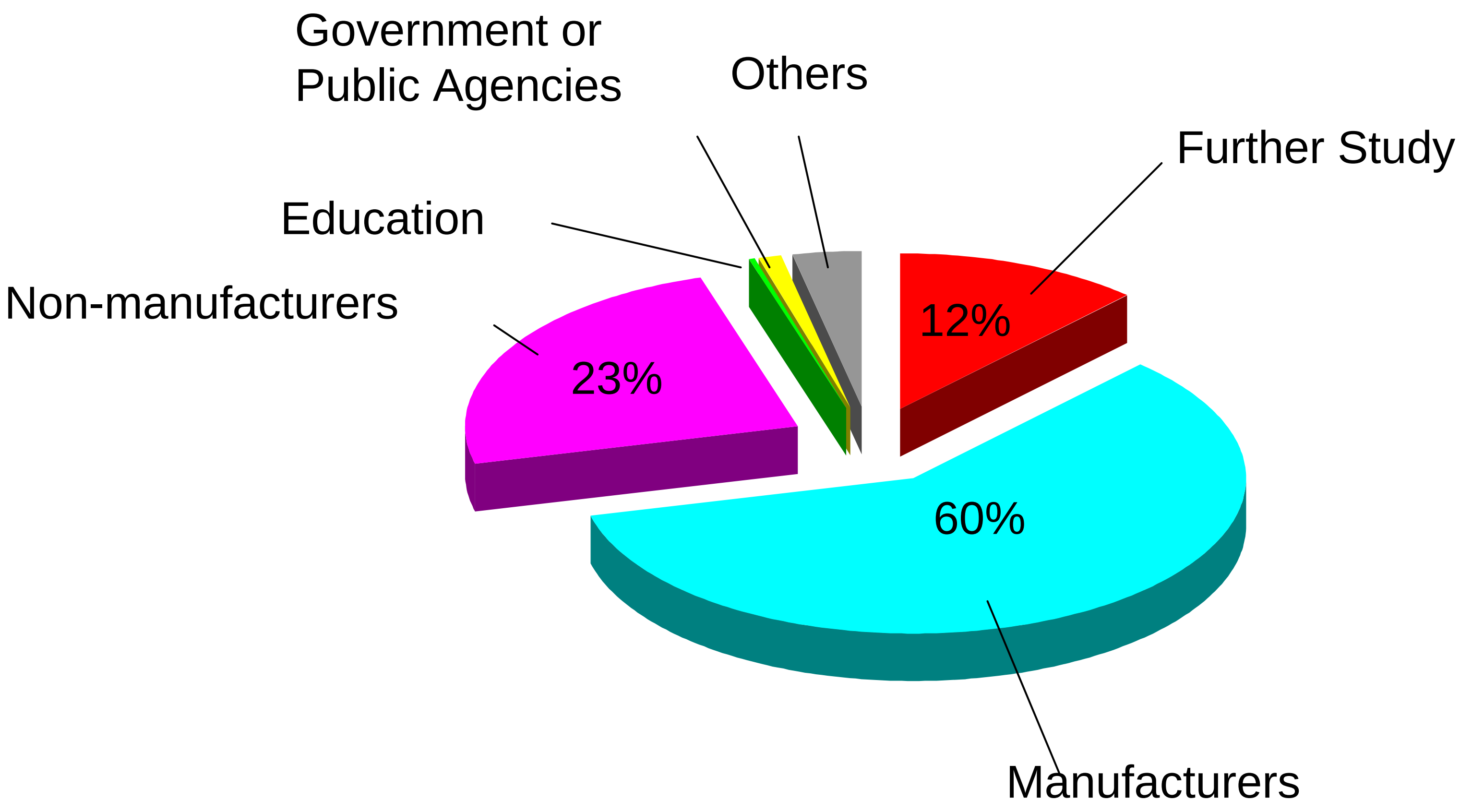
Doctoral Course



(Spring, 2006)

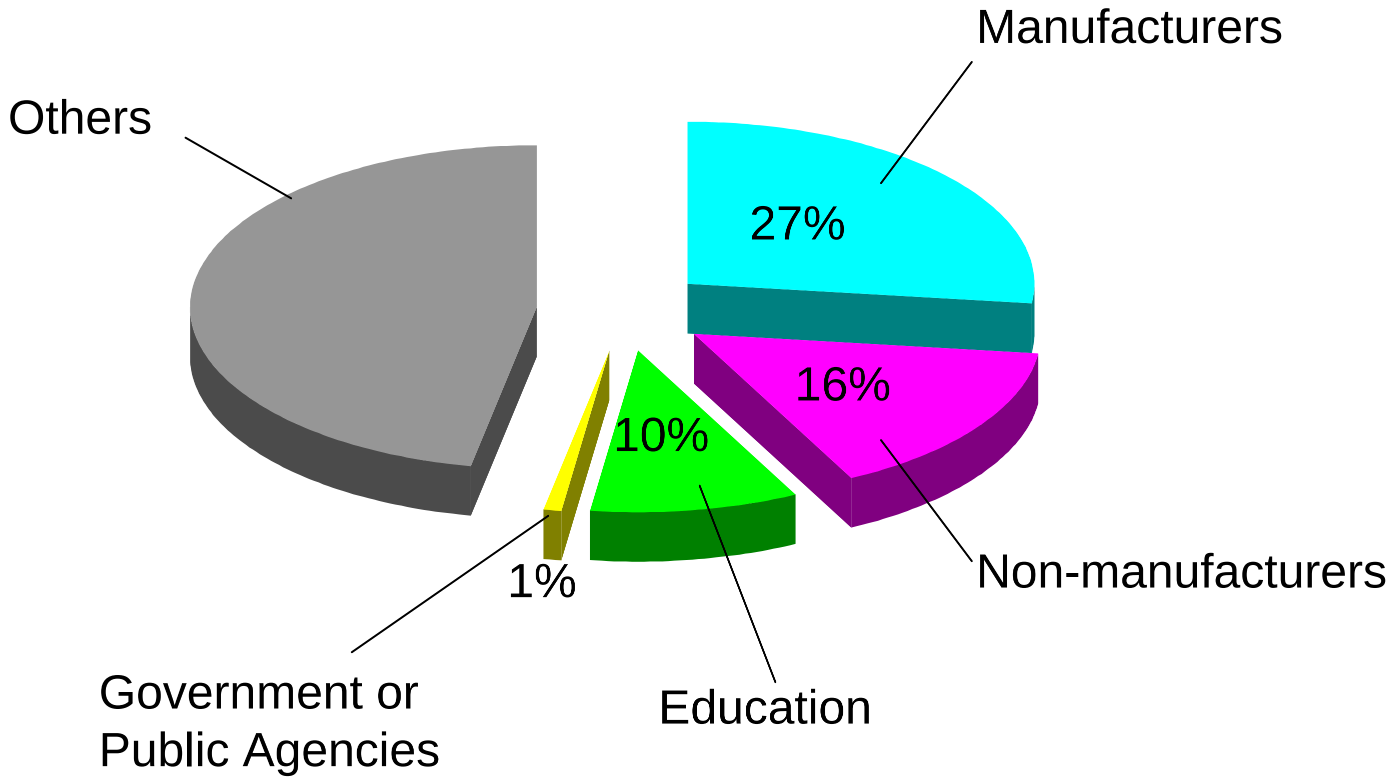
After Graduation

Master's degree (IGS)

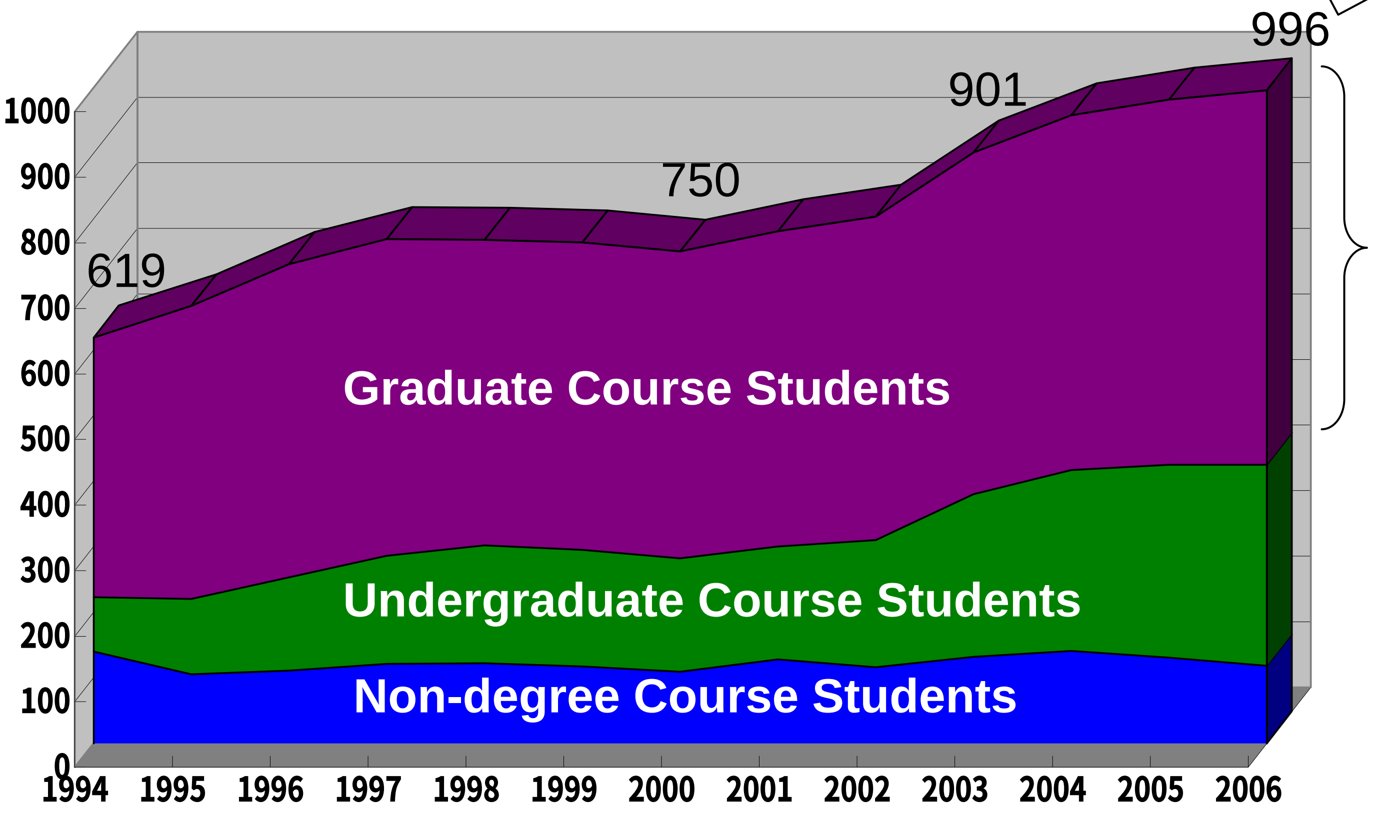


After Graduation

Doctoral degree (IGS)



Students from Abroad



Oct.,2006:1051

Apr. 2006: 571
128 in IGS.

China	407
Korea	122
Vietnam	67
Indonesia	64
Thailand	49
Malaysia	33
Bangladesh	24
:	:

岩井研メンバー

（2009年11月1日現在）


教授
岩井洋


准教授(共同研究)
筒井一生


客員教授
Simon Min Sze


客員教授
服部健雄


特任教授
名取研二


連携教授
杉井信之


連携教授
西山彰


特任准教授
Parhat Ahmet


助教
角嶋邦之

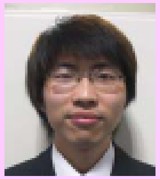
博士研究員


Milan Kumar Bera

博士課程


D3
佐々木雄一朗


D3
下村浩


D3
宋在烈


D3
舘喜一


D2
川那子高暢


D2
佐藤創志


D2
冨田隆治


D2
Maimaitirexiati Maimaiti


D2
Abudukelimu Abudureheman


D1
幸田みゆき


D1
李映勲


筒井研 D3
小林勇介

修士課程

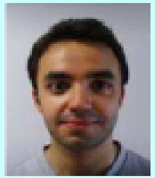

M2
新井英朗


M2
中山寛人


M2
船水清永


M2
細田亘


M2
又野克哉


M2
ダリウス・ハサンザデ


M2
Mokhammad Sholihul Hadi


M1
小柳友常


M1
小澤健児


M1
神田高志


M1
澤田剛伸


M1
茂森直登


M1
向井弘樹


M1
呉研


M1
Dou Chunmeng


筒井研 M2
横田知之


筒井研 M2
星野憲文


筒井研 M1
田中正興

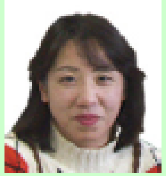
学部


B4
来山大祐

研究生


Rena Saimaiti

スタッフ


松本昭子


辛川美琴


西澤　正子

Interdisciplinary Graduate School of Science and Engineering
大学院総合理工学研究科

J2 Building:

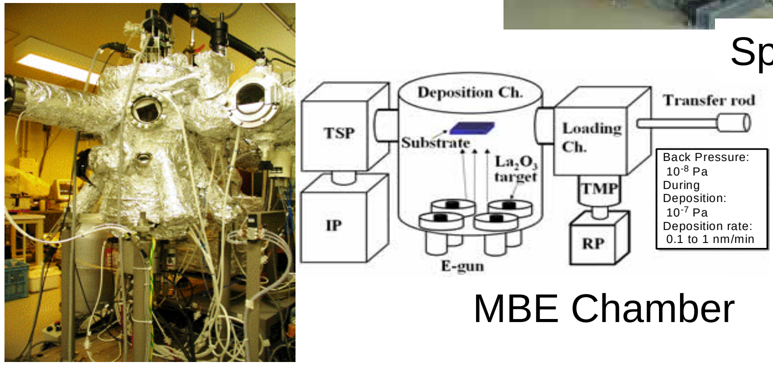
Frontier Collaborative Research Center（FCRC）
先端創造共同研究中心

Iwai Lab. Equipment

MBE and Sputter Chamber

Sputter Chamber

1/f noise measurement system; 6 inch wafer



MBE Chamber

RTA Furnace No.1

RTA Furnace No.2

RF measurement system; 8 inch wafer, 40 GHz

岩井研究室 ~Iwai Lab.~

● ご挨拶

Welcome to Iwai Lab.

総合理工学研究科　物理電子システム創造専攻　岩井研究室

当研究室では、シリコンをベースとした集積回路のデバイス技術、特に素子超微細化や集積回路限界の探査、研究や、新材料や三次元トランジスタ構造のシリコン集積回路への導入を行っています。さらにエマージング技術としてゲルマニウムやⅢ-Ⅴ族半導体チャネル材料の検討などを行っています。

LSI（Large scale Integrated Circuit,大規模集積回路）の最初の製品とみなされるIntelの1k bit DRAMが製造されてから30年近くになりますが、この間にLSIは実に長足の発展を遂げ、高度な計算を行い動作や情報を制御する中枢部品としてありとあらゆる機器に用いられるようになってきました。

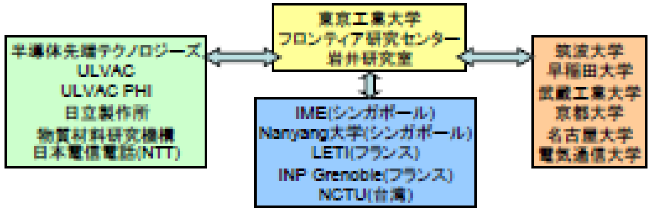
最近のMobile Telephone, Mobile PC, ひいてはインターネットの爆発的な普及も軽量、小型、低消費電力で極めてきたことによるものです。
今後更にこの文明飛躍的な発展を遂げて、近い将来人間の知性、感性の機能を代行する機器が出現することが大いに期待されます。

これはこれからの高齢化社会で予想される労働人口不足、老人介護人口不足などの状況のもとで、各人が平等にある程度以上の生活レベルを教授できるためには行く行くは越えなければならないハードルであると考えますが、何れにせよこれを実現するためには現状のものから何桁も性能の高い機器の実現が必要であると考えられており、まずはハードとしてのLSIの発展が今後何十年かにわたって継続していくことが必要条件のひとつとも考えられています。

さて、LSIの発展はトランジスタを中心としたLSI中の素子の縮小化によってなされてきましたが、トランジスタの縮小化の限界がどこにあるかが重要な課題としてクローズアップされてきます。この流れが今後も続くとすると2005年頃にはゲート長が30nmとなり、更に今世紀の半ばにはゲート長はシリコン結晶中の原子の間隔である0.0003μm(即ち3Å)となる計算となります。この寸法辺りが原子を用いてトランジスタを形成する限りにおいて究極的な限界と考えられますが、このようなゲート長のトランジスタが動作するかどうかは甚だ疑問であると思われており、経済的要因からはもう少し大きいところとも言われています。

研究テーマとしてはCMOS　LSIの素子微細化の限界を見据えて、今後のLSIがハード、ソフトの両面から継続して発展していくためにはどういう技術を開発していくべきかを考えつつ、まずは微細シリコントランジスタ微細の特性研究、微細化限界とその打破（高誘電体ゲート絶縁膜などの新材料の導入、構造の改良等など）の研究などから手を染めていきたいと考えています。またその後のポストスケーリング時代に対応した、エマージング技術として、ゲルマニウムやⅢ-Ⅴ族半導体チャネル材料、シリコンナノワイヤートランジスタの研究を行っていこうと思っています。また、成果をできるだけ広く産業界に使っていただき、社会に貢献すること目指しており、産学連携と国際協力を研究の基本としています。

外部機関との連携研究



東京工業大学
フロンティア研究センター
岩井研究室

半導体先端テクノロジーズ
ULVAC
ULVAC PHI
日立製作所
物質材料研究機構
日本電信電話(NTT)

IME(シンガポール)
Nanyang大学(シンガポール)
LETI(フランス)
INP Grenoble(フランス)
NCTU(台湾)

筑波大学
早稲田大学
武蔵工業大学
京都大学
名古屋大学
電気通信大学

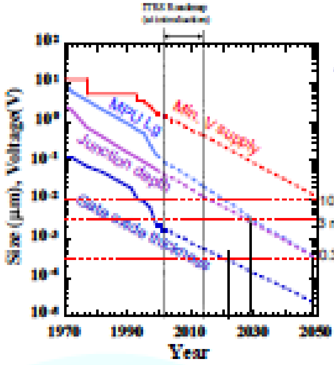
● 次世代高性能半導体デバイスに向けた研究テーマ

Siデバイスの重要性

現代社会：生産、金融、運輸、医療、行政などの社会機構
インターネット、i-mode、Bluetooth、携帯電話、カーナビ、
ゲーム、自動車、航空機、製造装置などの全ての機器、
CD、DVDなどの娯楽

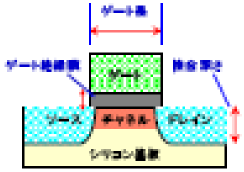
Si集積回路による管理・制御無くしてこれらは有り得ない

近年のSiデバイスの驚異的な発展
数千万個ー数億個のトランジスタ集積
MPUのクロック周波数　3GHz
SiGeバイポーラのf_T300GHz以上



10 nm Wave length of electron
3 nm Direct-tunneling limit in SiO_2
0.3 nm Distance between Si atoms

ULTIMATE LIMIT

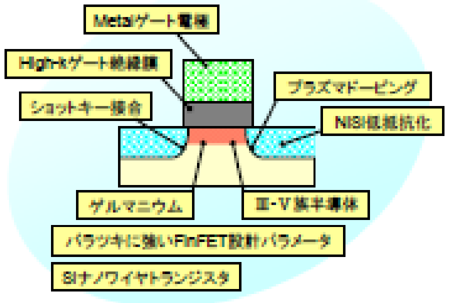


微細化の重要性

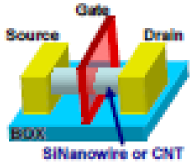
素子の微細化（100年間で100万分の1に！）

1900	1950	1960	1970	2000
真空管	トランジスタ	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm

微細化：
キャパシタンス減少 → 消費電力減少、高速化
高集積化 → 多機能化、並列処理 → 高速化
→ 機能、速度あたりのコスト、電力削減

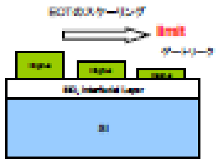


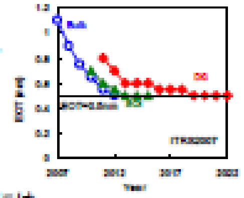
○低消費電力化
○高速性
○集積化
○バラツキ低減



High-k/Metalゲートスタック

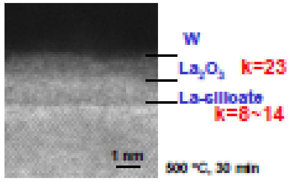
次世代ゲート絶縁膜材料として　La_2O_3に注目





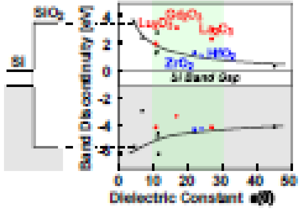
高性能化・低消費電力化には
EOT=0.5nmが必須

High-kとSiの直接接合が必要



La_2O_3は特性の良い直接接合が可能

XPS measurement by
Prof. T. Hattori, INFOS 2003

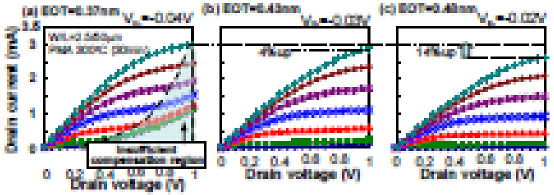


$$C_{ox} = \frac{\varepsilon_d \varepsilon_0}{t_{ox}} = \frac{\varepsilon_{SiO_2} \varepsilon_0}{EOT} \Rightarrow t_{ox} = \frac{\varepsilon_d}{\varepsilon_{SiO_2}} EOT$$

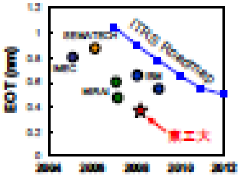
EOT：SiO_2等価換算膜厚

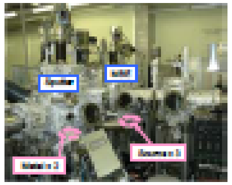
High-kゲート絶縁膜

EOT<0.4nmを達成



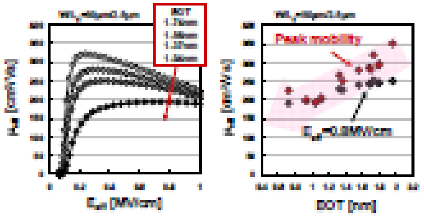
EOTの更なるスケーリングでドレイン電流増加を確認





低EOTにおける移動度劣化

W/La_2O_3/nFET, 500°C anneal, 30min in FG



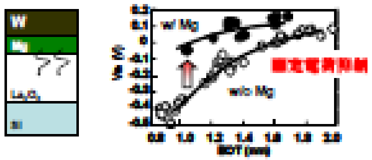
直接接合で高い移動度を実現

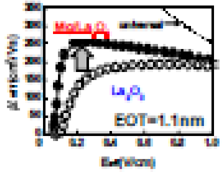
ゲートメタル電極に起因する
Coulomb散乱源の影響

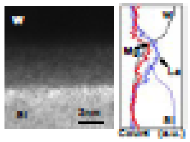
低EOTの移動度向上技術

異種材料導入による低いEOTの移動度改善が可能

Mg(マグネシウム)の導入





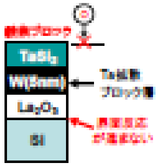


極限EOTに向けた材料選択

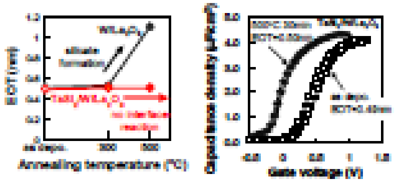
Metal Gate

$TaSi_2$を積層することで
酸素の侵入を抑制

→ 界面反応の抑制

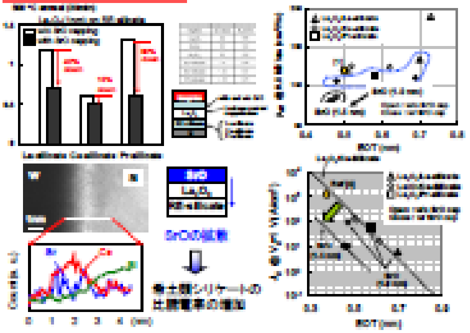


500°CでEOT=0.5nmを達成



k-value boosting

Ce-silicateとSrO-capping
によって0.5nm EOTを達成



SrOの拡散

希土類シリケートの比誘電率の増加

ゲルマニウムMOSFET

デバイスの更なる高速化のためにCMOSデバイスのチャネル材料としてGeが注目

ゲート長縮小の限界

L_g<5nm?

ソース・ドレイン間の漏れ電流増加

$$I_{ds}=\frac{W}{L}\mu_{eff}C_{ox}\frac{1}{2}(V_g-V_{th})^2$$

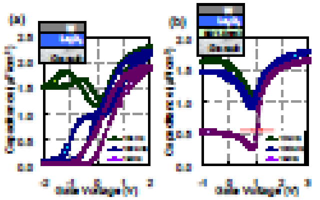
	μ_e[cm²/Vs]	μ_h[cm²/Vs]
Si	1400	450
Ge	3900	1900
GaAs	8500	400
InP	4600	650

Geトランジスタのゲート絶縁膜

GeO_2は
①高温熱処理で分解
②水溶性(ウェットプロセス不可能)
③比誘電率が低い
→良好なトランジスタ特性が得られない

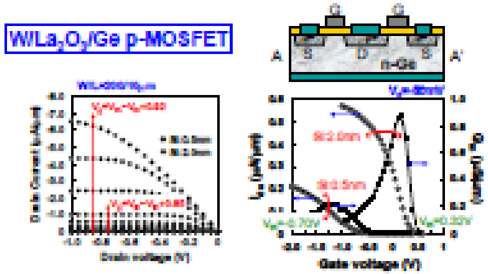
high-kをGeトランジスタの
ゲート絶縁膜として使おう!

High-k/Ge界面の制御が重要



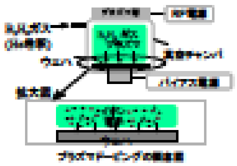
極薄Si挿入によりヒステリシスの低減が可能

W/La_2O_3/Ge p-MOSFET



High-k/Geトランジスタの動作を確認

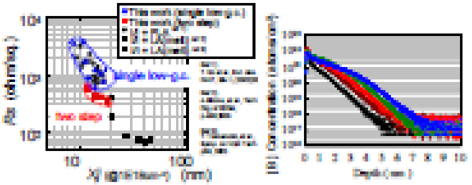
極浅接合用プラズマドーピング技術



Bの場合とAsの場合

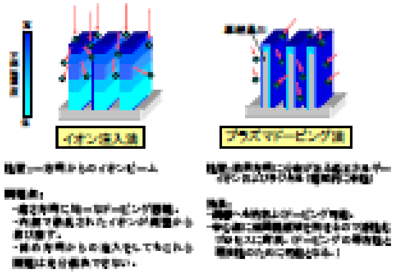
○低エネルギー注入(~100V)
○高いスループット(10^{15}cm^{-2}を30sec以内で注入可能)
○チャネリング無し→立体MOSFETに適用可能

極浅接合と高活性化の実現



4nmの接合深さを実現
30%以上の高活性化率

Fin構造へのプラズマドーピング



SiNanowireトランジスタ

Off電流抑制の要求からナノワイヤ系FETへ

スケーリングによらない低消費電力化・高性能化

オフ電流

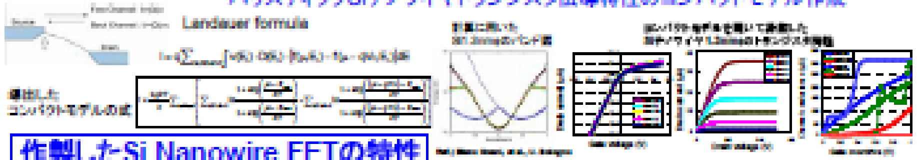
・サブシュレッショルドリーク電流の抑制

オン電流

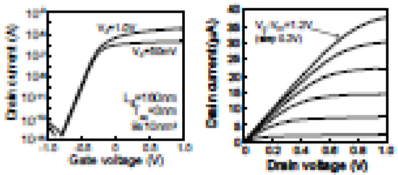
・短チャネル濃度によるドレイン電流増加

・一次元構造による量子効果

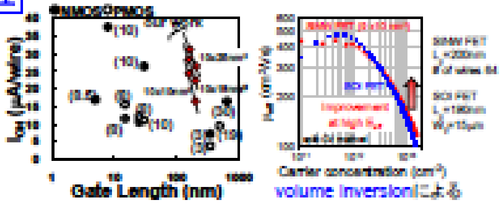
バリスティックSiナノワイヤトランジスタ伝導特性のコンパクトモデル作成



作製したSi Nanowire FETの特性



SS=65mV/dec., I_{ON}/I_{OFF} over 10^5



他報告との比較：高いI_{ON}電流を確認

volume inversionによる高電界移動度の増加を確認

Si Nanowire のNiシリサイド化

Si Nanowire FETのSource/Drain領域の寄生抵抗

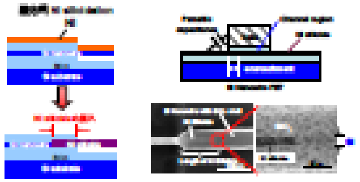
⇨ I_{ON}電流の減少

Ni silicideが有効

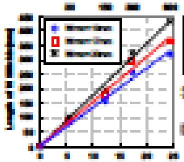
Si Nanowire

Ni Silicide形成機構の理解

Ni Silicideの侵入の制御



Si Nanowire内への過剰なNi silicideの侵入が問題

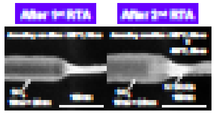


Diffusion equation

$\lambda \propto A\sqrt{t}$

Si Nanowire内へのNi silicideの侵入

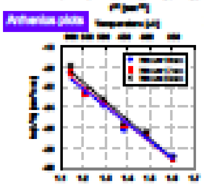
⇨ silicide へのNiの拡散が支配的



- 6nm Ni deposition
- 1st RTA
- Un-reacted Ni removal
- 2nd RTA
- Observation by SEM

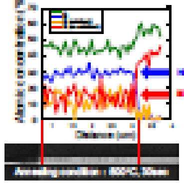
2-Step annealingによる侵入長の制御

Arrhenius plots

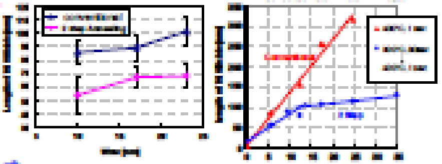


活性化エネルギーはNi_2Siとほぼ一致

オージェ電子分光から均一なNi_2Siを確認



2-Step annealingによってワイヤ内への過剰なNi silicideの侵入を抑制



Activation energy

W_{Si} [nm]	10	17	23
E_a [eV]	1.48	1.52	1.60

Activation energy on bulk Si

Ni silicide	NiSi	Ni_2Si
Activation energy [eV]	1.4	1.5

600 °C熱処理

⇩

NiリッチなSilicideが形成

ショットキー障壁トランジスタ

● Source/Drain領域のスケーリング

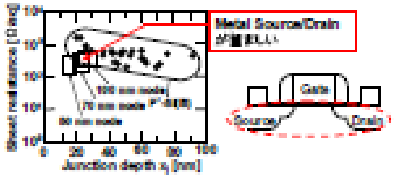


Fig.1 Sheet resistance vs.junction depth.

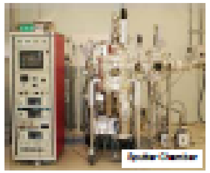
利点

- 浅い接合形成が容易
- ソース/ドレイン低抵抗
- 短チャネル効果耐性が高い

欠点

- ショットキー障壁による駆動電流の劣化

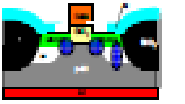
Schottky障壁の制御が必要



異種金属界面挿入

n-channel SB-MOSFETにはErまたはHfの界面挿入が有効

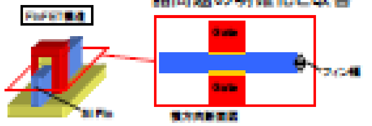
p-channel SB-MOSFETにはPtの界面挿入が有効



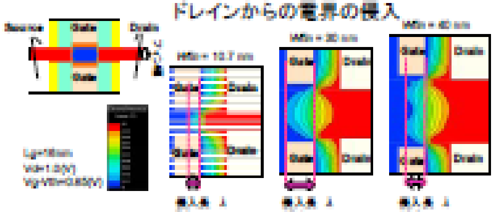
ショットキー障壁トランジスタの概念図

ロバスト3次元トランジスタ

FinFETの微細化により生じる諸問題の明確化と改善



ドレインからの電界の侵入



DIBLと侵入長のフィン幅依存性

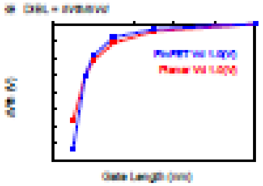
プレーナ型MOSFETとFinFETの短チャネル効果の比較

ITRS2006updateの構造でのシミュレーション

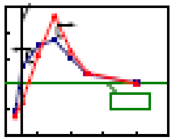
	Planar MOSFET	FinFET
DIBL [mV/V]	40.2	71.5
S [mV/dec]	79.6	83.7

デバイスシミュレーションにて評価

シミュレーション例



FinFETの方が短チャネル効果に弱い！ 何故！？



フィン幅と共に侵入長が増加し、それに伴いDIBLが変化している。また、侵入長は中性領域がなくなるフィン幅で最大となる。

フィン幅をゲート長の2/3よりも薄くしないと短チャネル効果を十分抑えられない。

Ⅲ-Ⅴ族半導体

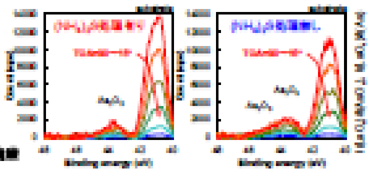
更なる高速化のためには新たなチャネル材料が必要

	μ_e(cm²/Vs)	μ_h(cm²/Vs)
Si	[illegible]	[illegible]
Ge	[illegible]	[illegible]
GaAs	[illegible]	[illegible]
InP	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]

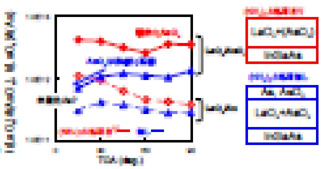
電子移動度の高いInGaAsに注目

- アセトン、エタノールに続きHF処理により洗浄
- $(NH_4)_2S$による中間層の自然酸化物除去
- 電子線蒸着中電子線照射によりHigh-k絶縁膜堆積
- Post Deposition Annealing

X線光電子分光



$(NH_4)_2S$処理により僅かなAs拡散の抑制効果



$(NH_4)_2S$処理によりAs酸化物形成を少なくできる

Importance of Electronics

- There were many inventions in the 20th century:

  Airplane, Nuclear Power generation, Computer,

  Space aircraft, etc

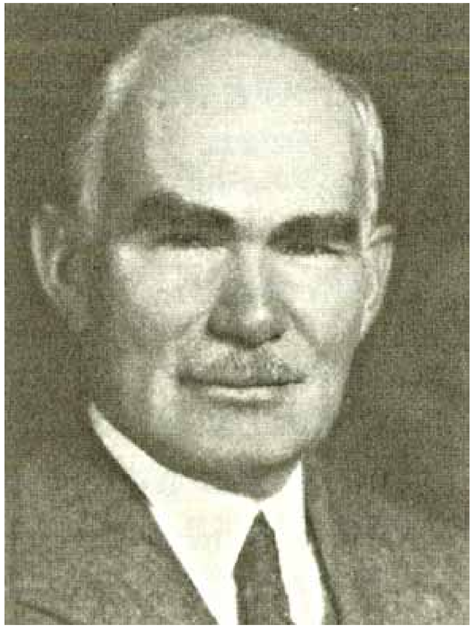
- However, everything has to be controlled by electronics
- Electronics

  Most important invention in the 20th century

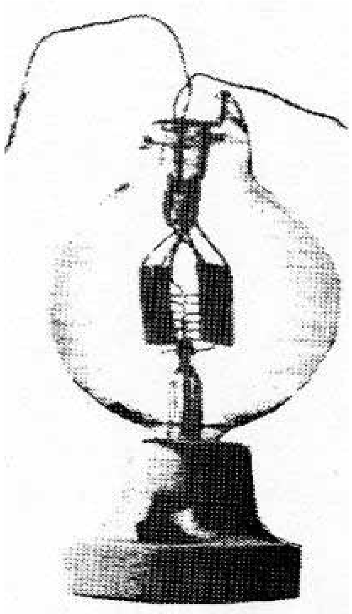
- What is Electronics: To use electrons,

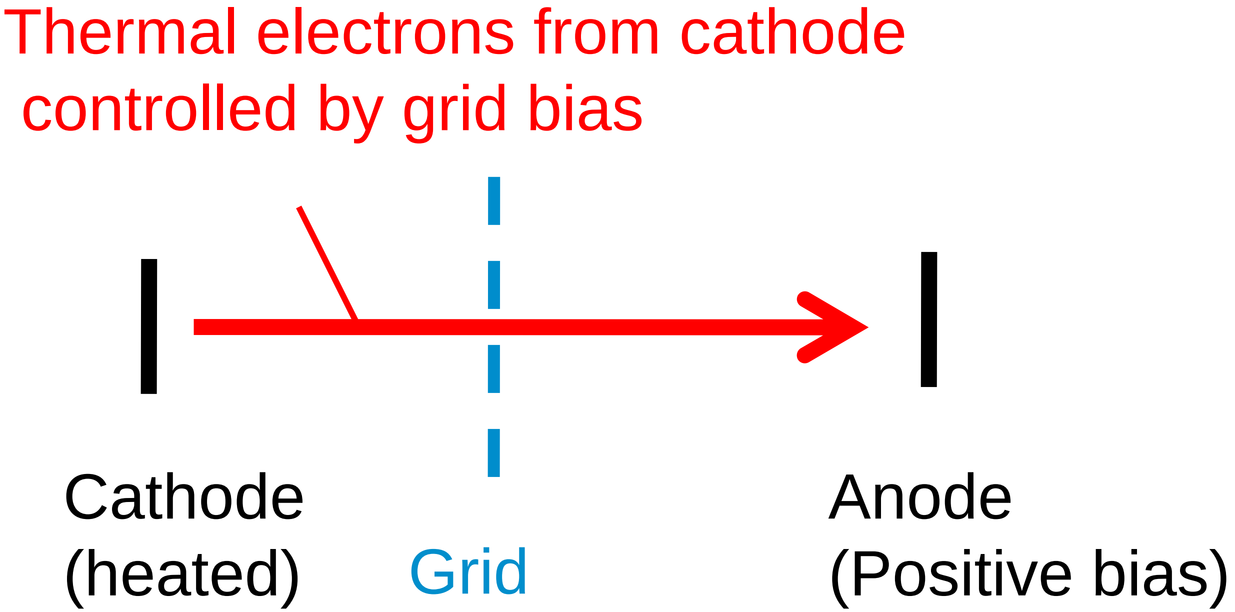
  Electronic Circuits

Electronic Circuits started by the invention of vacuum tube (Triode) in 1906



Lee De Forest





Thermal electrons from cathode controlled by grid bias

Cathode (heated)

Grid

Anode (Positive bias)

Same mechanism as that of transistor

4 wives of Lee De Forest

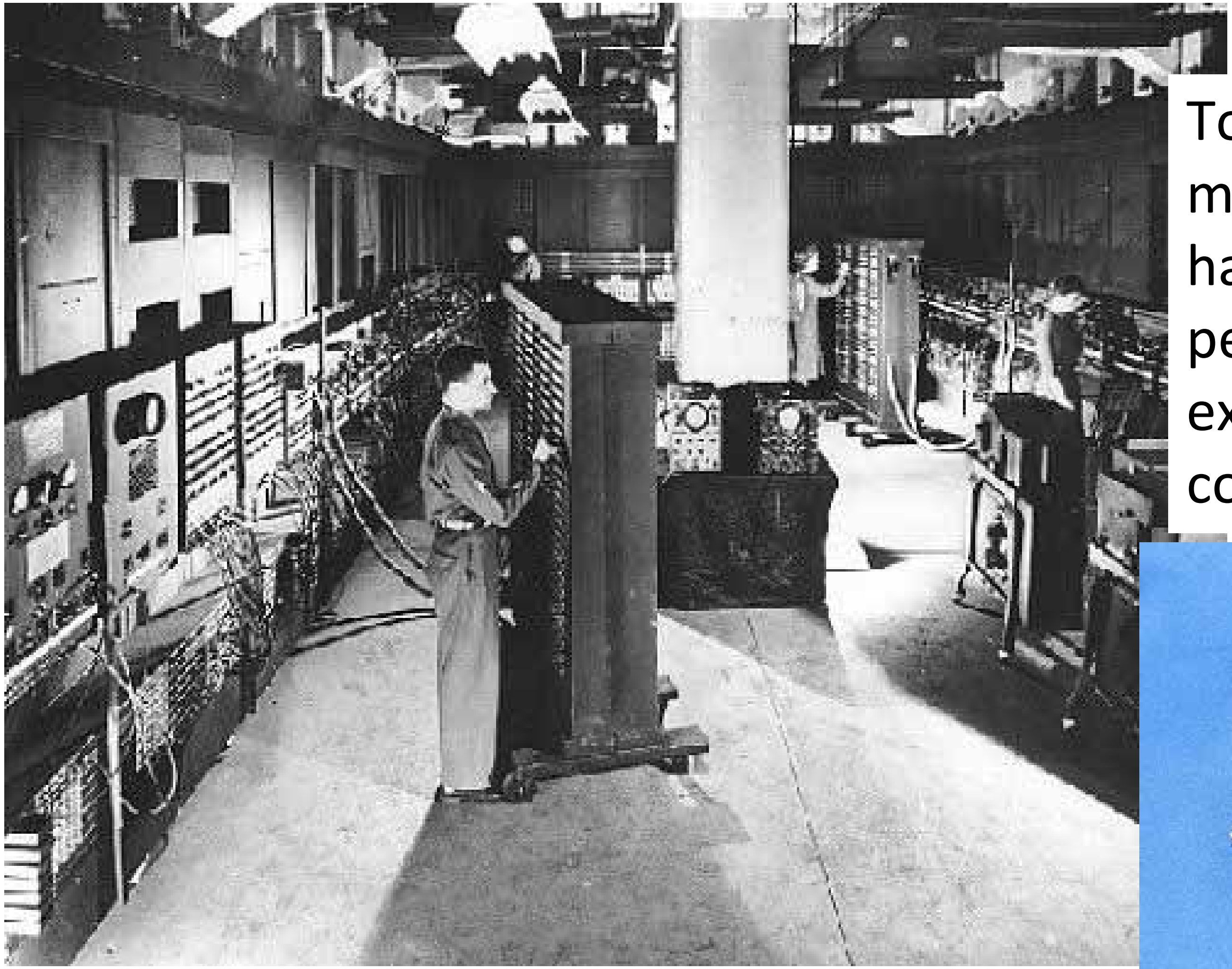
1906 Lucille Sheardown
1907 Nora Blatch
1912 Mary Mayo, singer
1930 Marie Mosquini, silent film actress

Mary

Marie

First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

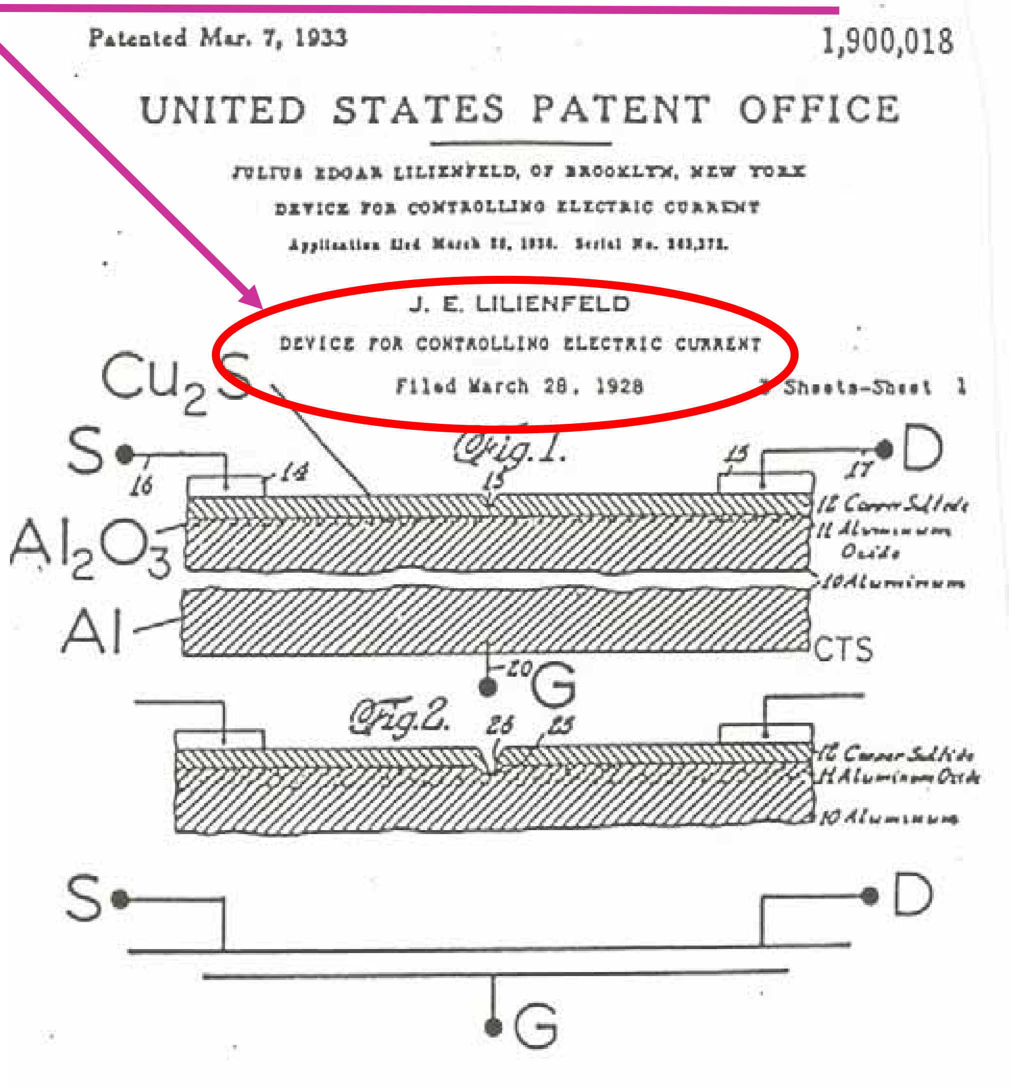


Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928



Patented Mar. 7, 1933

1,900,018

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Application filed March 28, 1928. Serial No. 265,372.

J. E. LILIENFELD

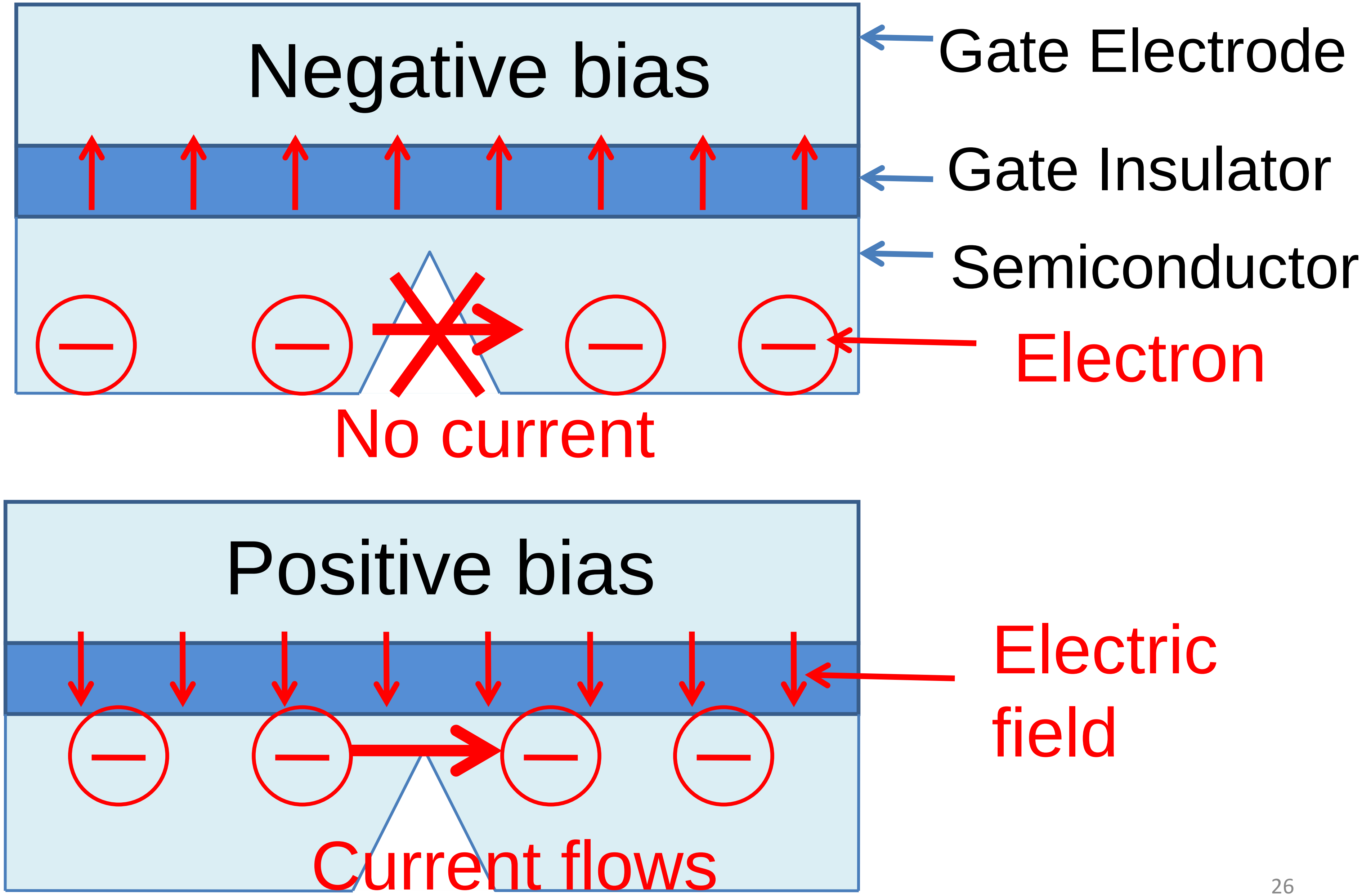
DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928

2 Sheets-Sheet 1

J.E.LILIENFELD

Capacitor structure with notch



Negative bias

Gate Electrode

Gate Insulator

Semiconductor

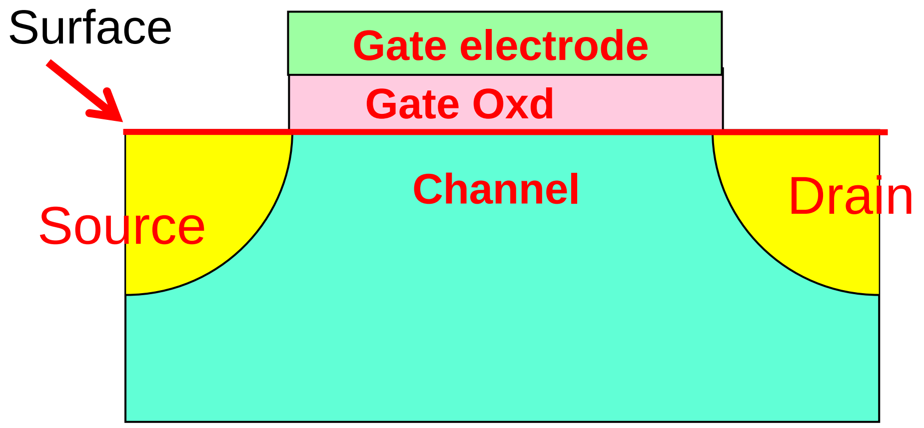
Electron

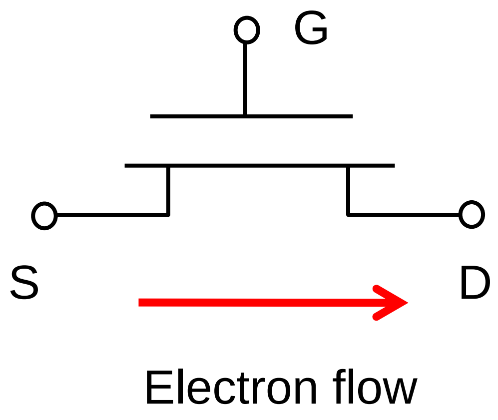
No current

Positive bias

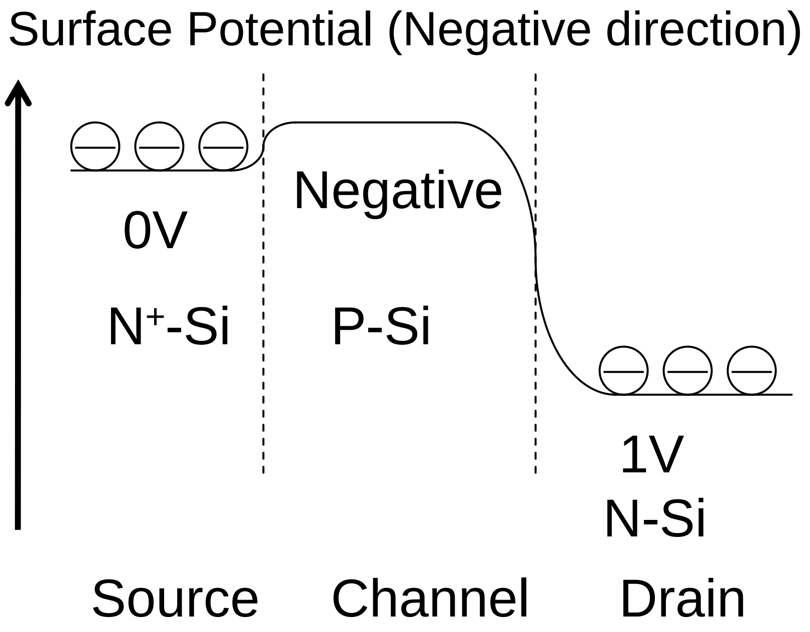
Electric field

Current flows

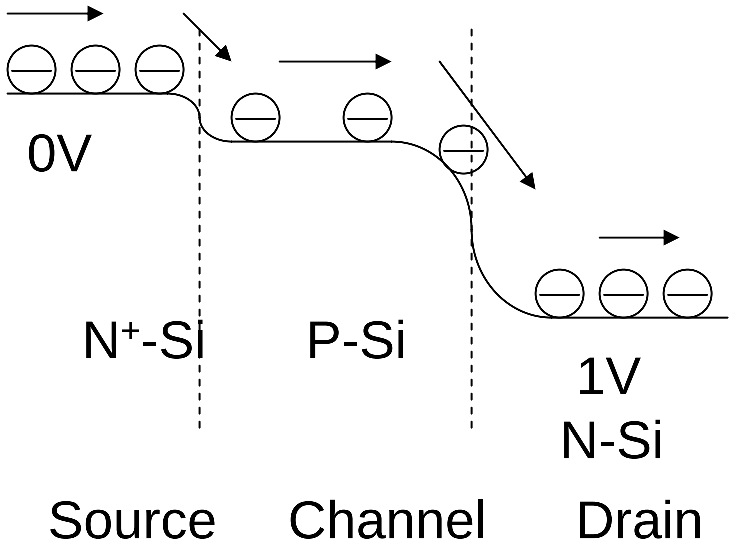




<u>0 bias for gate</u>



<u>Positive bias for gate</u>

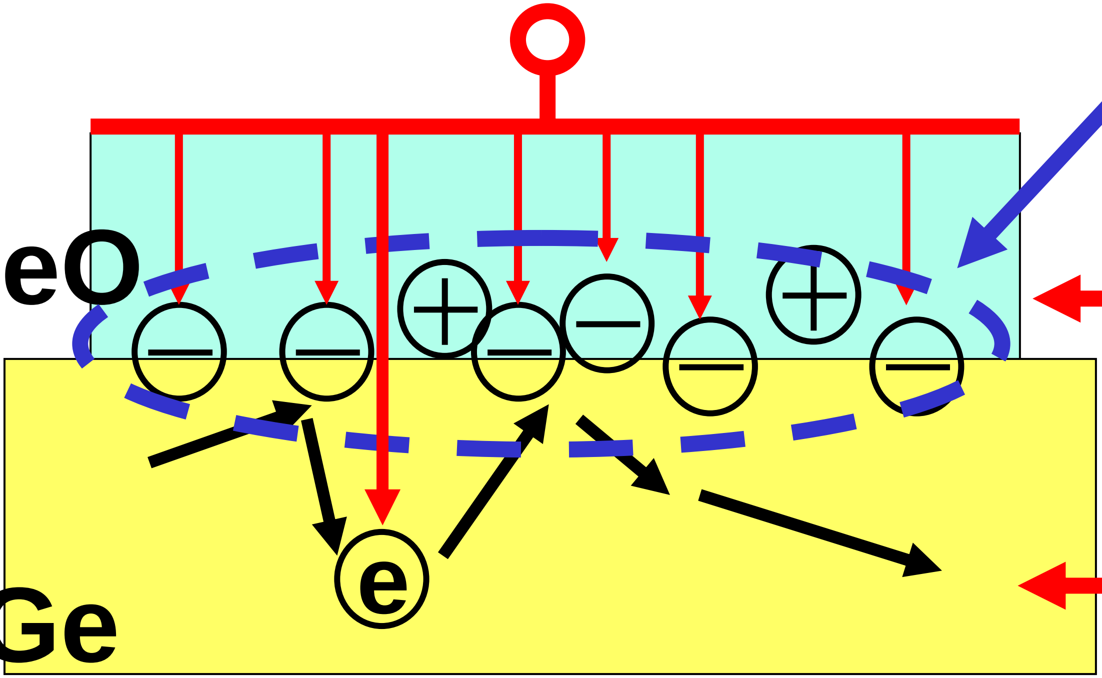


However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!

Very bad interface property between the semiconductor and gate insulator



Interfacial Charges

Electric Shielding

Carrier Scattering

Drain Current was several orders of magnitude smaller than expected

Even Shockley!

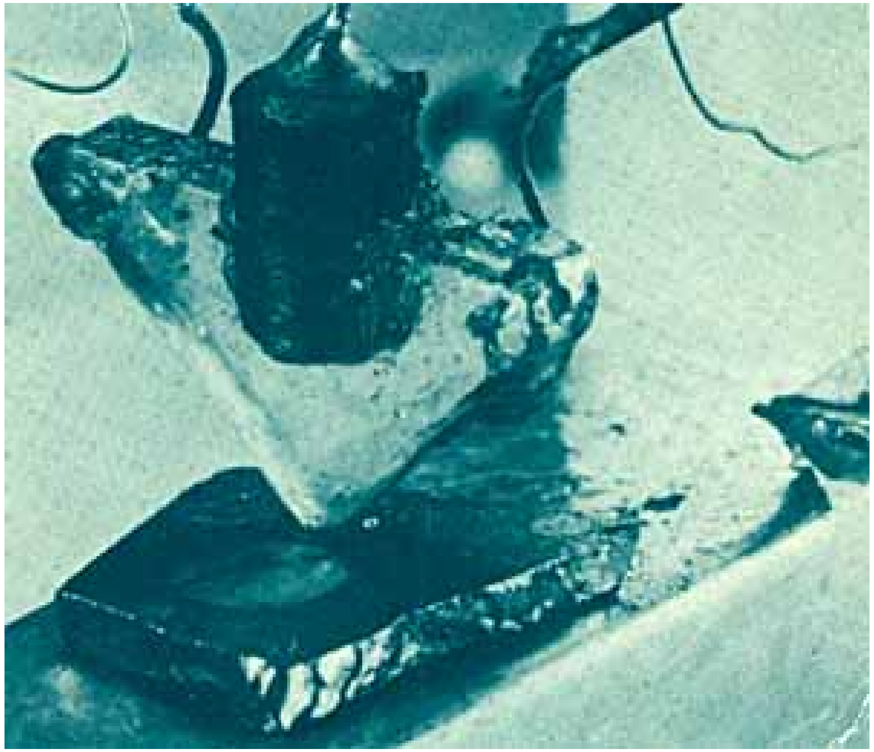
However, they found amplification phenomenon when investigating Ge surface when putting needles.

This is the 1^{st} Transistor:

Not Field Effect Transistor,

But Bipolar Transistor (another mechanism)

1947: 1^{st} transistor



Bipolar using Ge

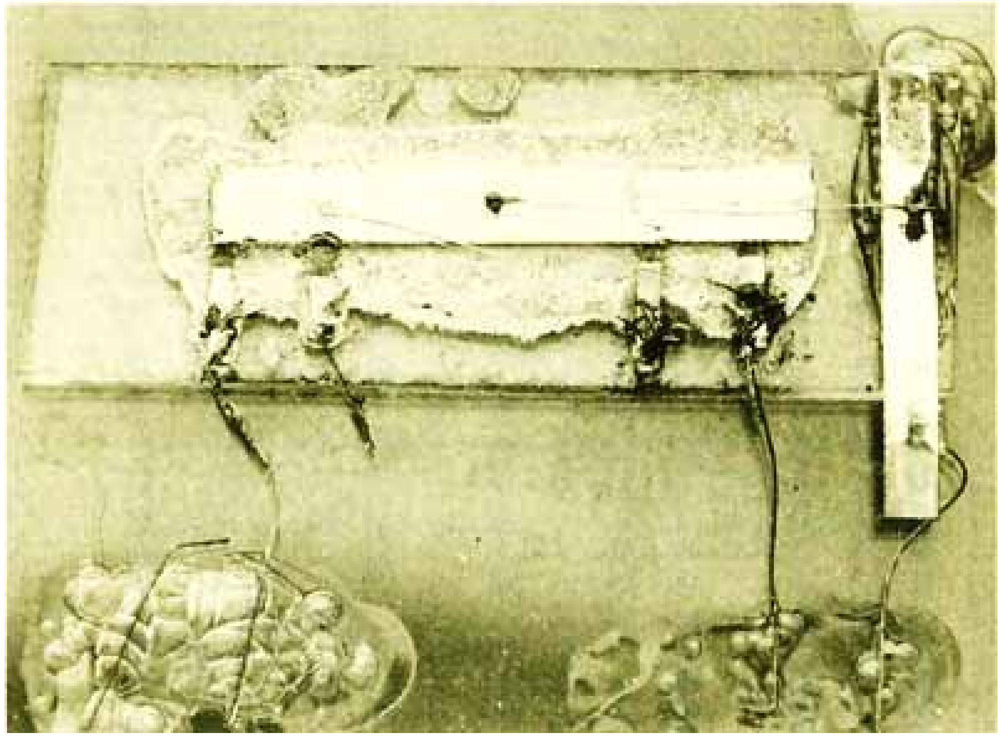
J. Bardeen W. Bratten,

W. Shockley

1958: 1st Integrated Circuit

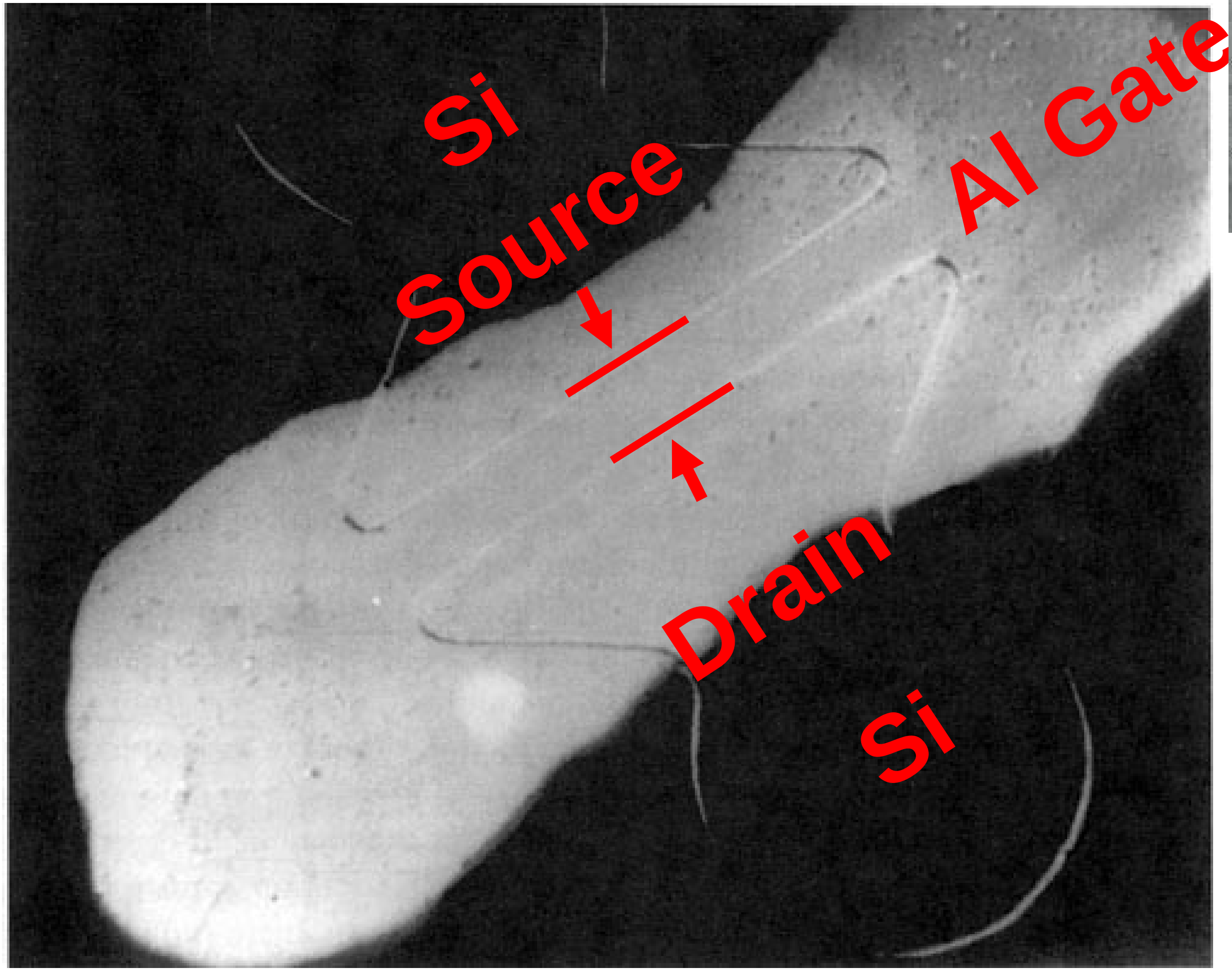
Jack S. Kilby

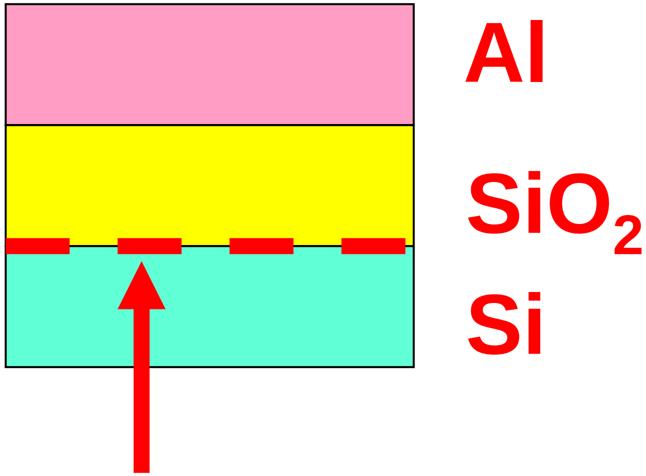
Connect 2 bipolar transistors in the
Same substrate by bonding wire.



1960: First MOSFET
by D. Kahng and M. Atalla

Top View

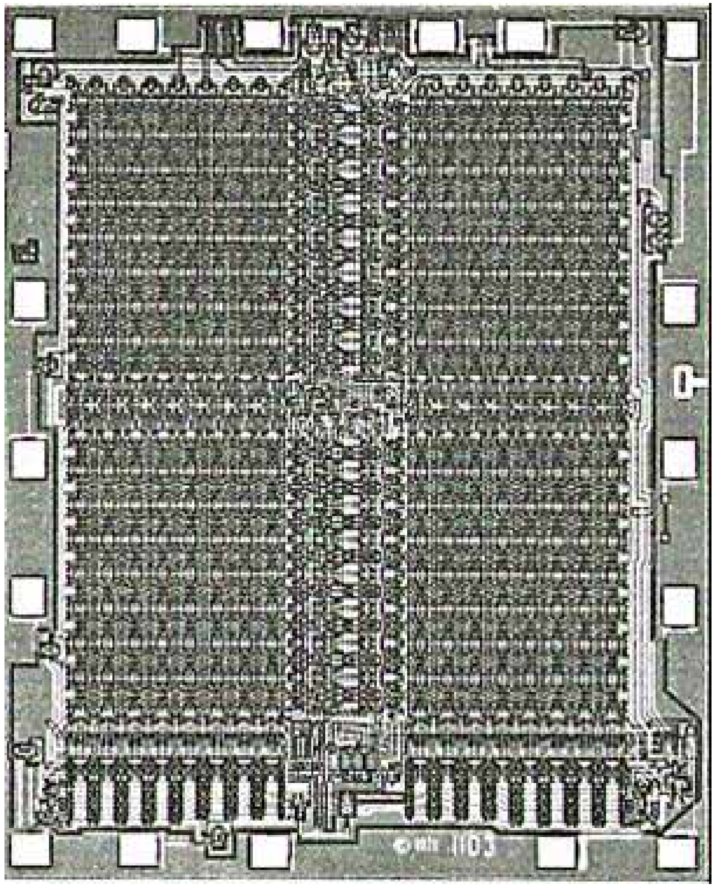




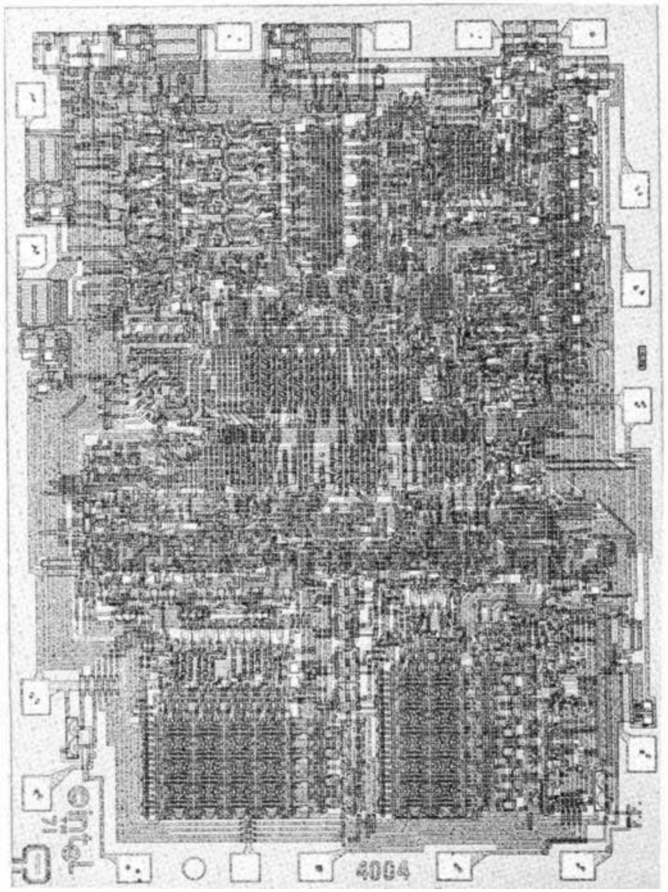
Si/SiO2 Interface is extraordinarily good

1970,71: 1st generation of LSIs

DRAM Intel 1103



MPU Intel 4004



MOS LSI experienced continuous progress for many years

	Name of Integrated Circuits	Number of Transistors
1960s	IC (Integrated Circuits)	~ 10
1970s	LSI (Large Scale Integrated Circuit)	~1,000
1980s	VLSI (Very Large Scale IC)	~10,000
1990s	ULSI (Ultra Large Scale IC)	~1,000,000
2000s	?LSI (? Large Scale IC)	~1000,000,000

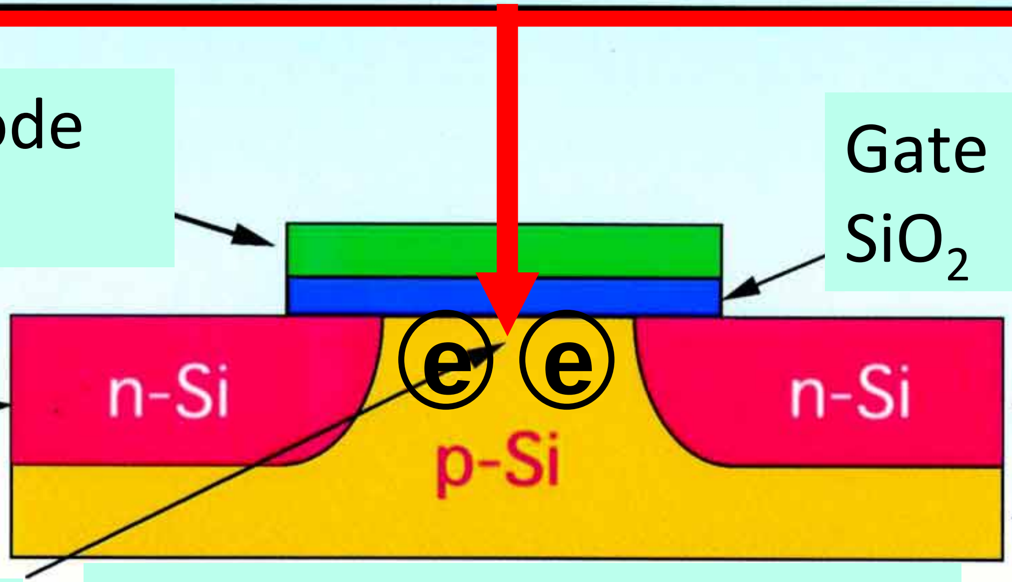
Gate Electrode
Poly Si

Gate Insulator
SiO_2

Substrate
Si

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Use Gate Field Effect for switching



Gate Electrode
Poly Si

Gate Insulator
SiO_2

Source

Drain

Si
Substrate

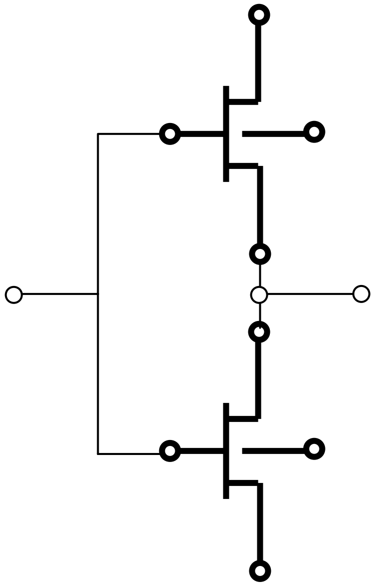
Channel

N-MOS (N-type MOSFET)

CMOS

Complimentary MOS

Inverter



PMOS

NMOS

When NMOS is ON, PMOS is OFF

When PMOS is ON, NMOS is OFF

Needless to say, but….

CMOS Technology:

Indispensible for our human society

Al the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:

There is no computer in banks, and

world economical activities immediately stop.

Cellarer phone dose not exists

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 µm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

→ **Increase clock frequency**

→ **Increase circuit operation speed**

2. **Increase number of Transistors**

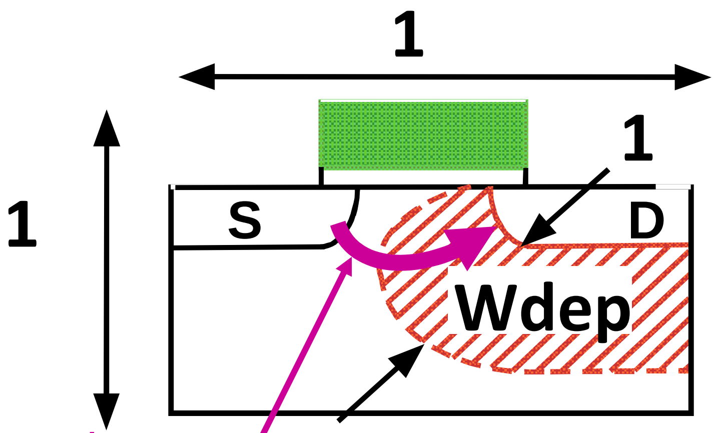
→ **Parallel processing**

→ **Increase circuit operation speed**

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.

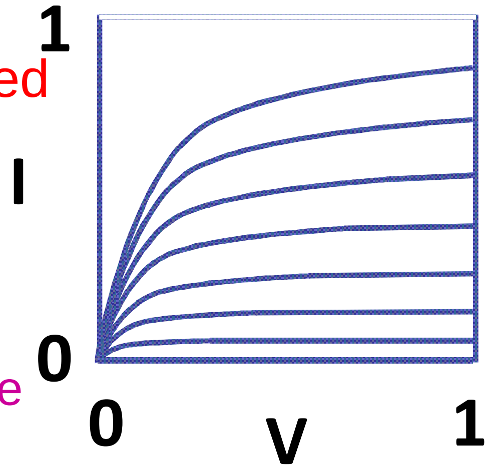
Scaling Method: by R. Dennard in 1974



Leakage current

Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage
between S and D



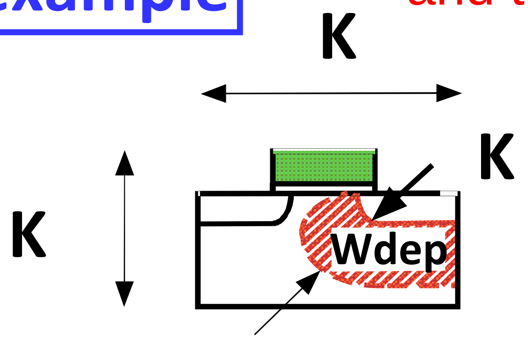
Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

K=0.7 for example

X , Y , Z : K, V : K, Na : 1/K

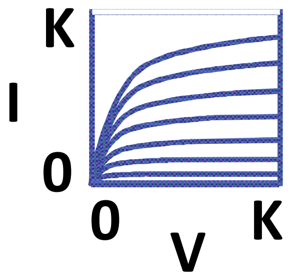
By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$\text{Wdep} \propto \sqrt{V/Na}$$

$$: \ K$$



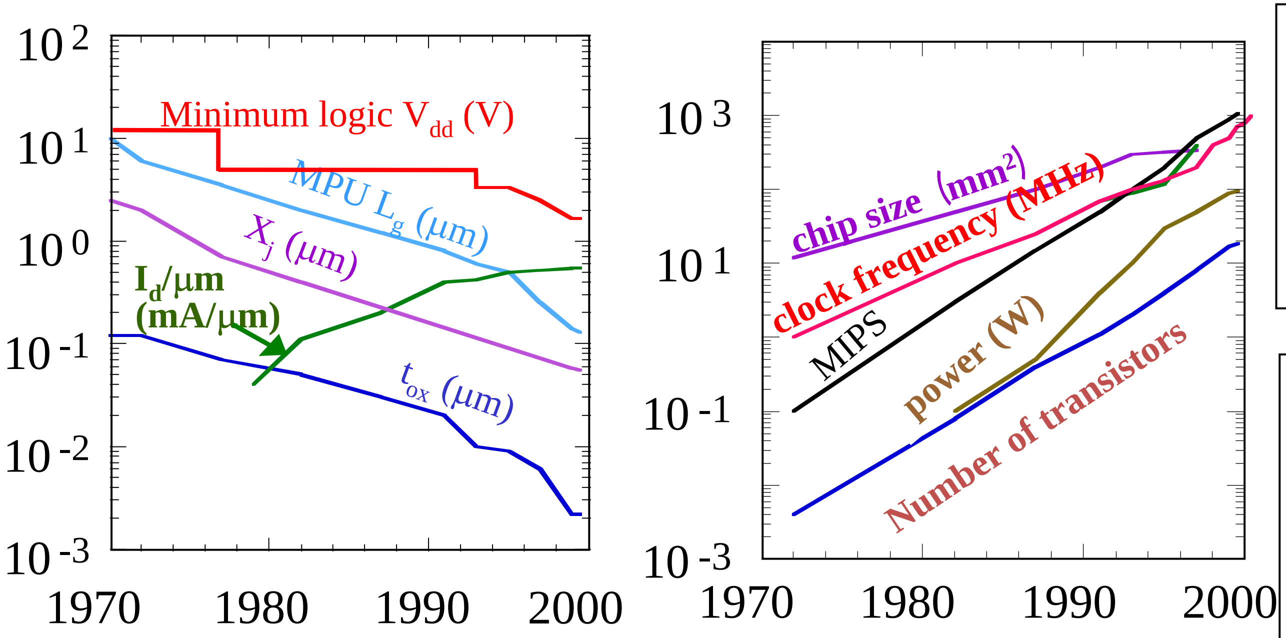
I : K

Downscaling merit: Beautiful!

Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	**Scaling K : K=0.7 for example**
Drive current in saturation	I_d	K	$I_d = v_{sat}W_gC_o(V_g-V_{th})$ C_o: gate C per unit area $\rightarrow W_g(t_{ox}^{-1})(V_g-V_{th}) = W_g t_{ox}^{-1}(V_g-V_{th}) = KK^{-1}K=K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o\varepsilon_{ox}L_gW_g/t_{ox} \rightarrow KK/K = K$
Switching speed	τ	K	$\tau = C_gV_{dd}/I_d \rightarrow KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α: Scaling factor → **In the past, $\alpha>1$ for most cases**
Integration (# of Tr)	N	α/K^2	$N \rightarrow \alpha/K^2$ **$= 1/K^2$, when $\alpha=1$**
Power per chip	P	α	$fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha$ **$= 1$, when $\alpha=1$**

k= 0.7 and α =1	k= 0.7^2 =0.5 and α =1
Single MOFET	
Vdd → 0.7	Vdd → 0.5
Lg → 0.7	Lg → 0.5
Id → 0.7	Id → 0.5
Cg → 0.7	Cg → 0.5
P (Power)/Clock → $0.7^3 = 0.34$	P (Power)/Clock → $0.5^3 = 0.125$
τ (Switching time) → 0.7	τ (Switching time) → 0.5
Chip	
N (# of Tr) → $1/0.7^2 = 2$	N (# of Tr) → $1/0.5^2 = 4$
f (Clock) → 1/0.7 = 1.4	f (Clock) → 1/0.5 = 2
P (Power) → 1	P (Power) → 1

Actual past downscaling trend until year 2000



Source. Iwai and S. Ohmi, Microelectronics Reliability 42 (2002), pp.1251-1268

Past 30 years scaling

Merit: N, f increase

Demerit: P increase

V_{dd} scaling insufficient

⇩

Additional significant increase in I_d, f, P

Change in 30 years

	Ideal scaling	Real Change		Ideal scaling	Real Change		Ideal scaling	Real Change
L_g	K	10^{-2}	I_d	K (10^{-2})	10^{-1}	f	$1/K(10^2)$	10^3
t_{ox}	$K(10^{-2})$	10^{-2}						
V_{dd}	$K(10^{-2})$	10^{-1}	I_d/μm	1	10^1	P	$\alpha(10^1)$	10^5
A_{chip}	α	10^1	N	$\alpha/K^2(10^5)$	10^4	$= f\alpha NCV^2$		

Vd scaling insufficient, α increased → N, Id, f, P increased significantly

Microprocessors Trend??

Increase in Power and Heat ?

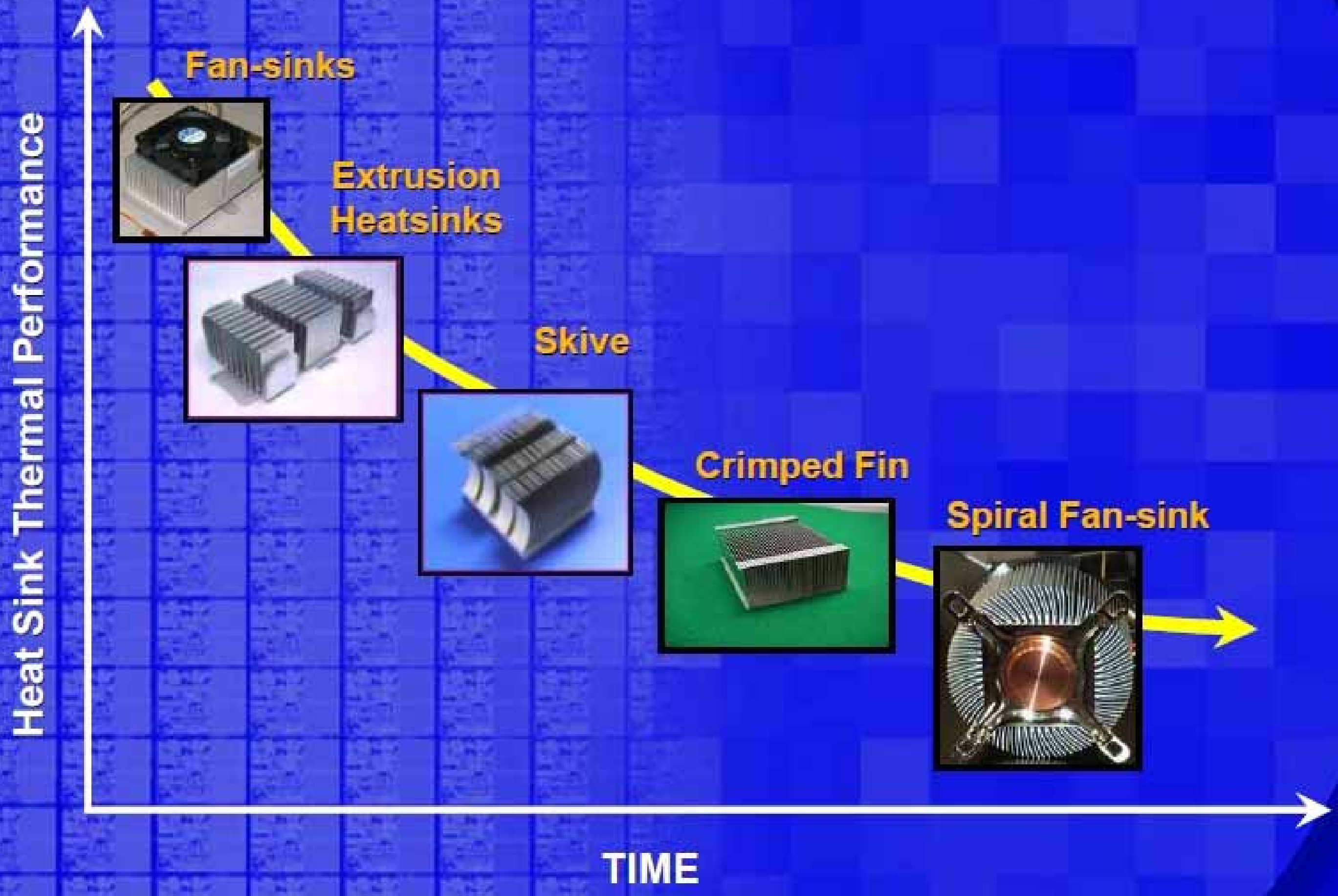
Past: 1972 (Intel)	Today: 2002 (Intel)	2008 (Intel)
Lg 10,000 nm	Lg sub-70 nm	Lg sub-25 nm
Tox 1200 nm	Tox 1.4 nm	Tox 0.7 nm
f 0.00075 GHz	f 2.53 GHz	f 30 GHz
P a few 100 mW	P several 10 W	P 10 kW
N 2.25k	N 50 M	N 1.8B
		MIPS 1M MIPS (TIPS)

Heat generation

2002	**10W/cm^2**	**Hot plate**
2006	**100W/cm^2**	**Surface of nuclear reactor**
2010	**1000W/cm^2**	**rocket nozzle**
2016	**10000W/cm^2**	**Sun surface**

P. P. Gelsinger, “Microprocessor for the New Millennium: Challenges, Opportunities, and New Frontiers,” Dig. Tech. 2001 ISSCC, San Francisco, pp.22-23, February, 2001

Heat Sink Technology

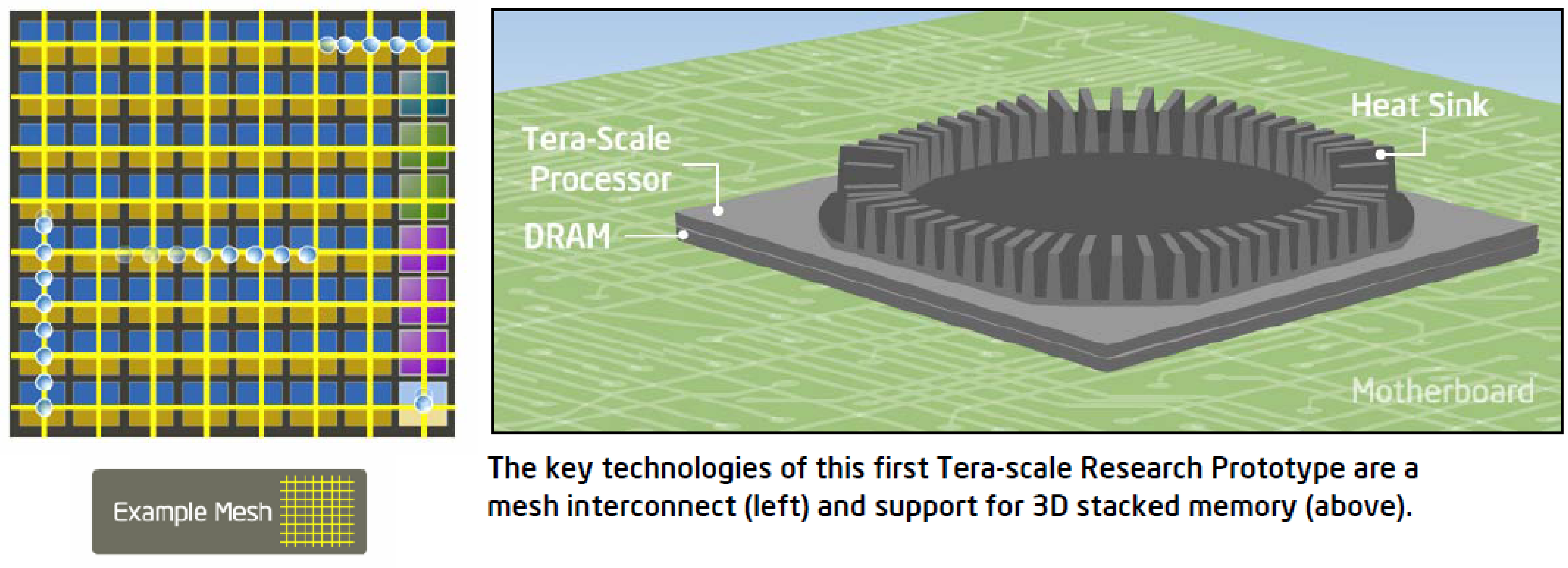


Tera-scale Research Prototype

Connecting 80 simple cores on a single test chip

Intel processors with two cores are here now and quad-core processors are right around the corner. In the coming years, the number of cores on a chip will continue to grow, launching an era of vastly more powerful computers. These are the machines that will deliver efficient teraflop performance with the capabilities needed to handle tomorrow's emerging applications. They must also scale to an increasing number of cores – perhaps 10s or even 100s of them.

This test chip represents Intel's first tera-scale research prototype silicon. The purpose of the prototype is to develop a design methodology appropriate for tera-scale computing by using a tiled approach. Each tile includes a small core, or compute element, with a few simple instructions that can generate data, and a router that connects each tile to adjacent tiles and to 3D stacked memory that will be added in the future. The prototype consists of 80 tiles in an 8x10 array with an on-chip interconnect fabric.



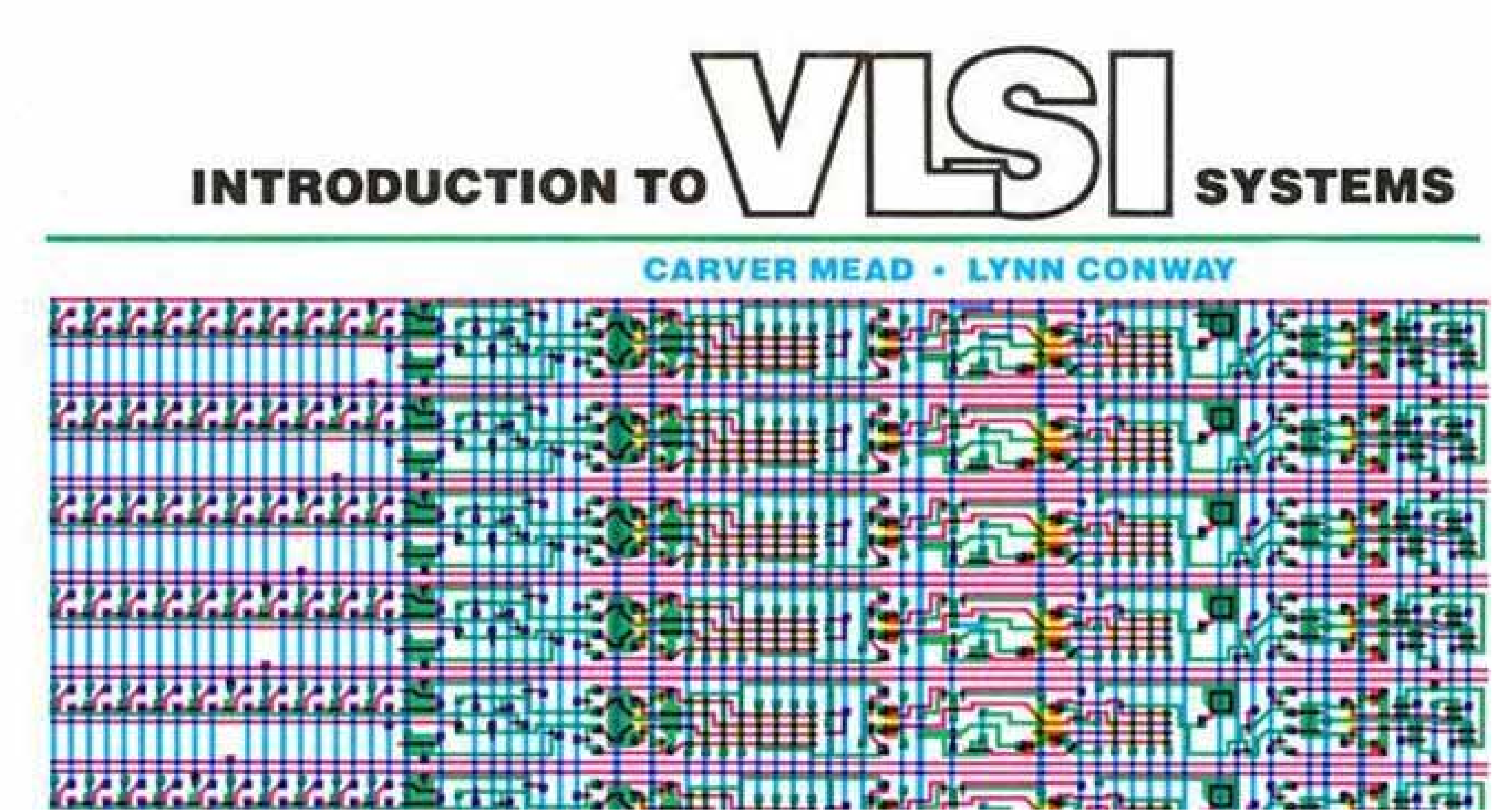
The key technologies of this first Tera-scale Research Prototype are a mesh interconnect (left) and support for 3D stacked memory (above).

Many people wanted to say about the limit.
Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.



INTRODUCTION TO VLSI SYSTEMS

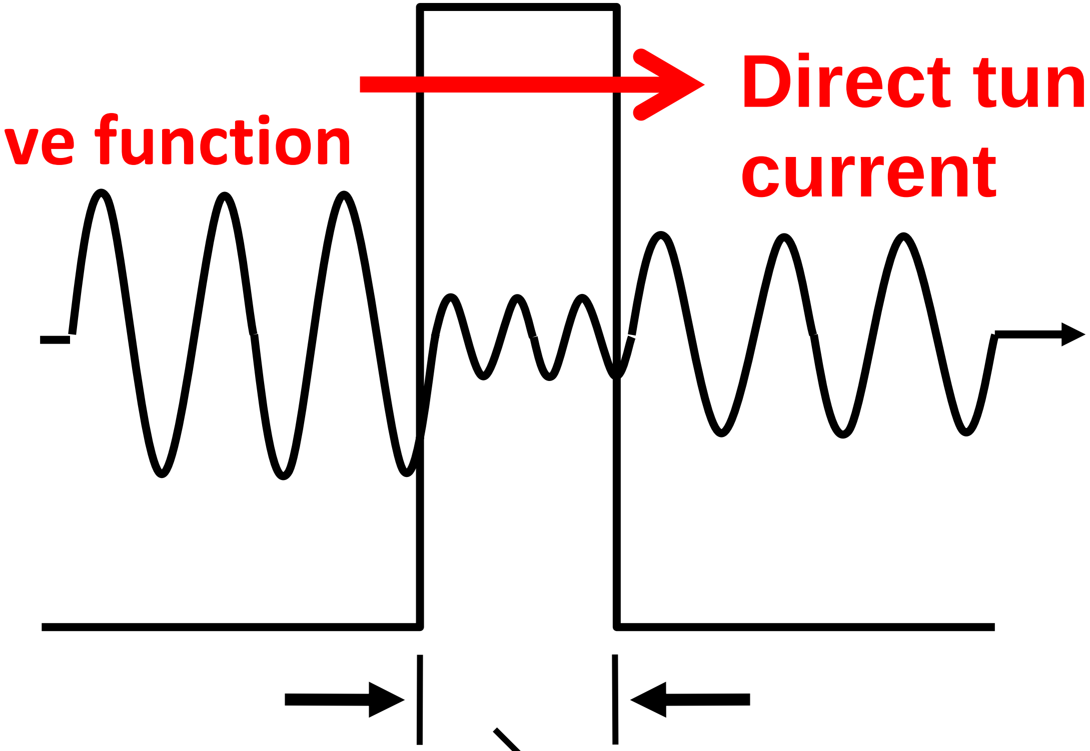
CARVER MEAD • LYNN CONWAY

C. Mead L. Conway

VLSI textbook

Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.

Direct-tunneling effect



Gate Electrode

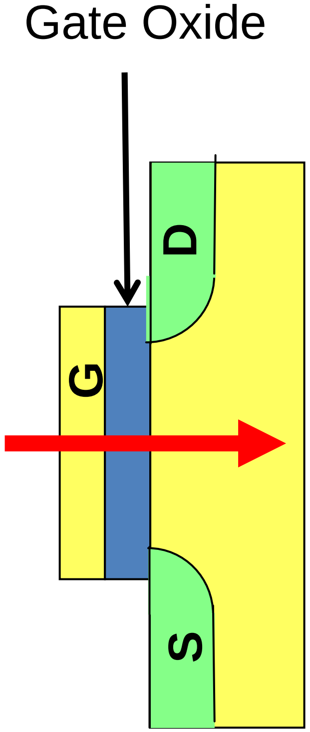
Gate Oxide

Si Substrate

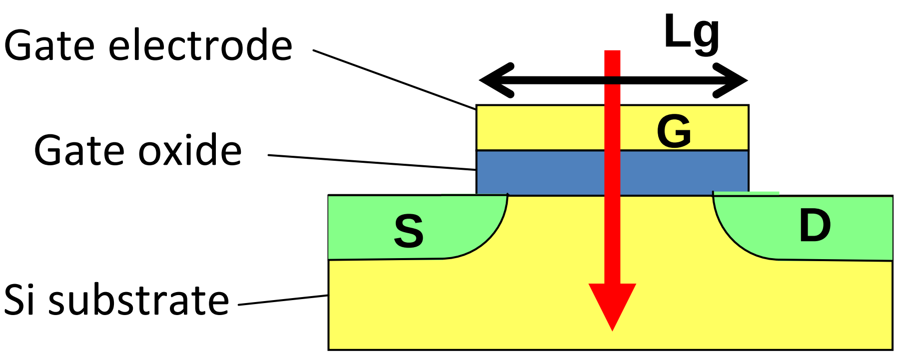
Potential Barrier

Wave function

Direct tunneling current

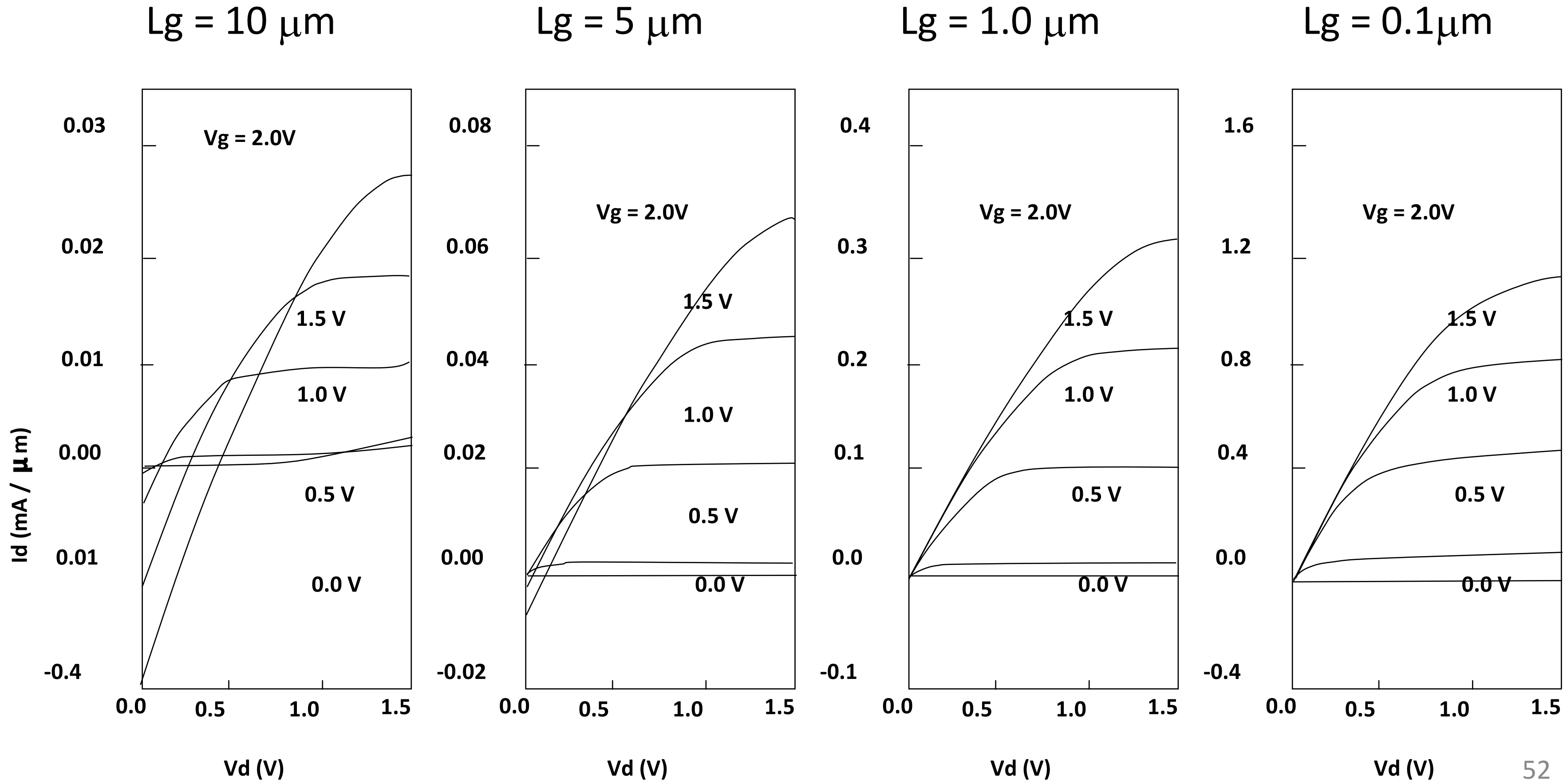


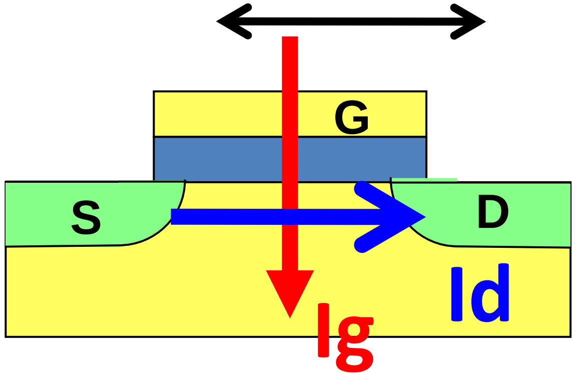
Direct tunneling leakage current start to flow when the thickness is 3 nm.



Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide

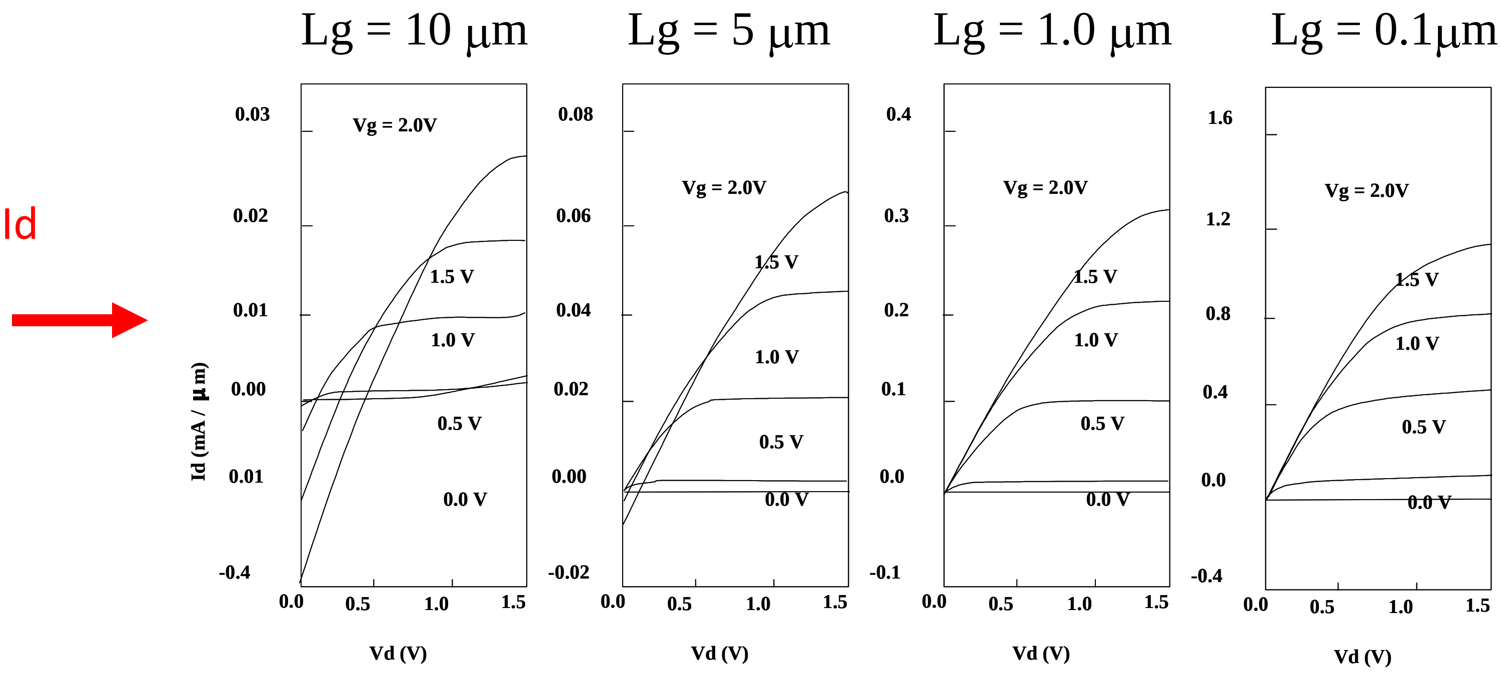




Gate leakage: Ig ∝ Gate Area ∝ Gate length (Lg)

Drain current: Id ∝ 1/Gate length (Lg)

Lg → small,
Then, Ig → small, Id → large, Thus, Ig/Id → very small


Lg = 10 μm Lg = 5 μm Lg = 1.0 μm Lg = 0.1μm

Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!
Some one will think for you

Transistor Scaling Continues

90nm node

Lg=50nm

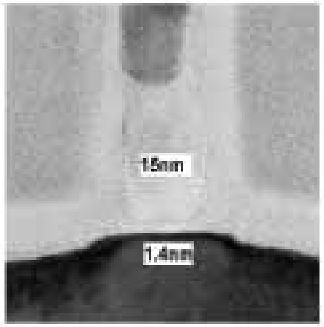
65nm node

Lg=35nm

45nm node

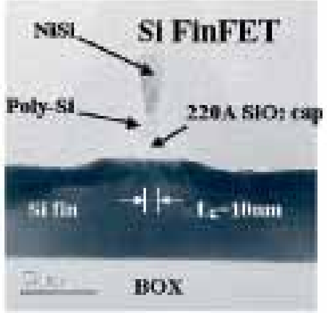
Lg=25nm

32nm node

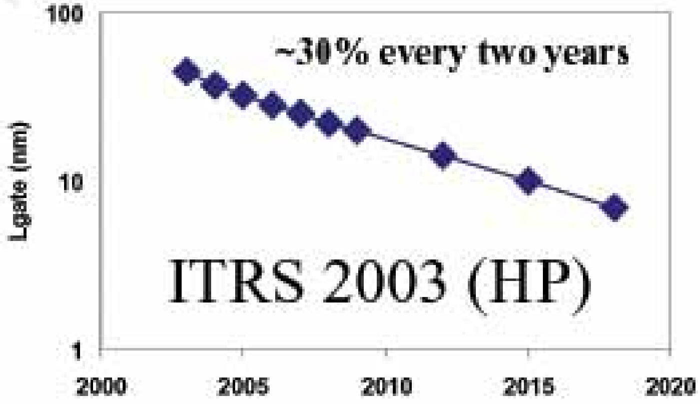


Lg=15nm

22nm node



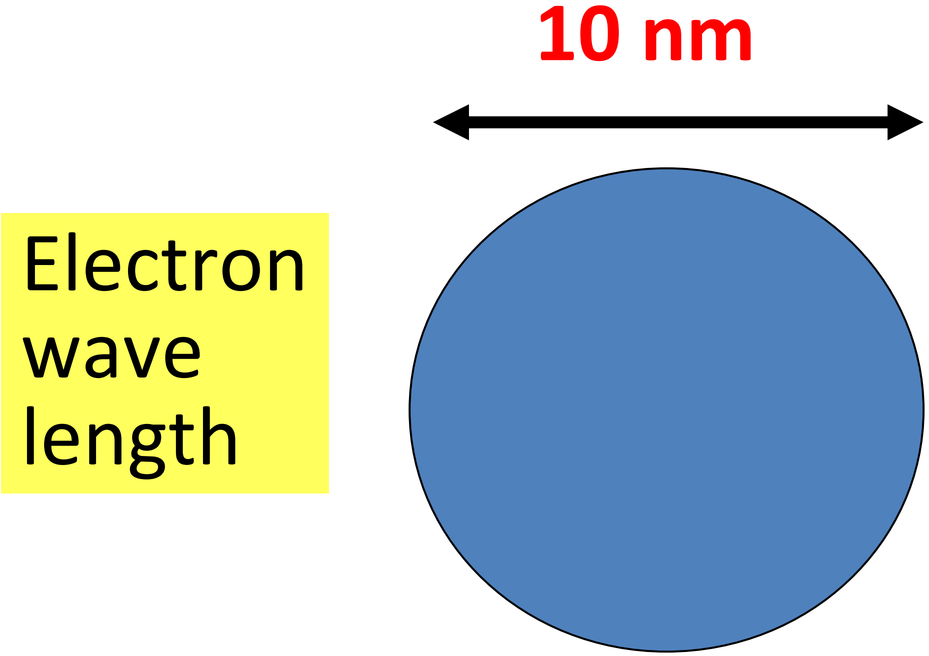
Lg=10nm

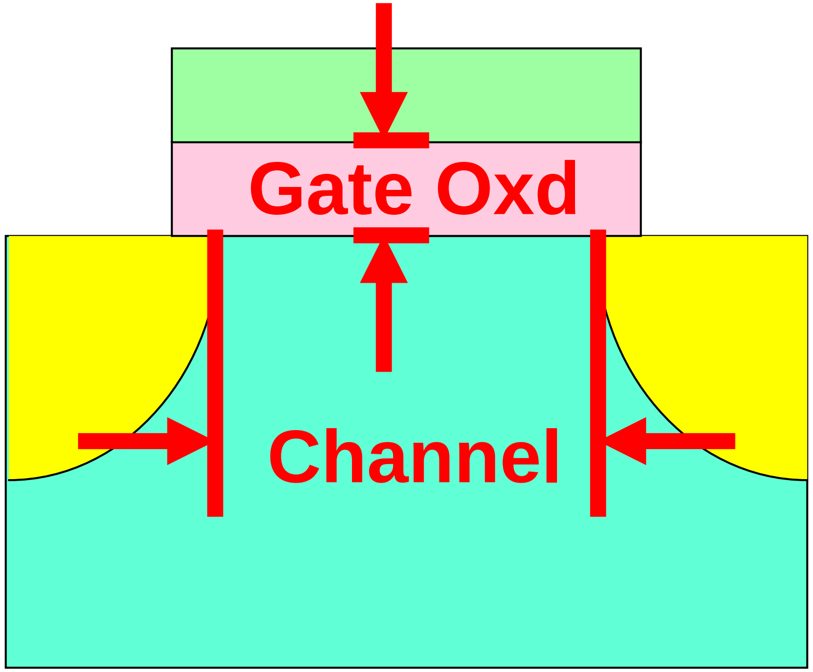


Qi Xinag, ECS 2004, AMD

Downsizing limit?

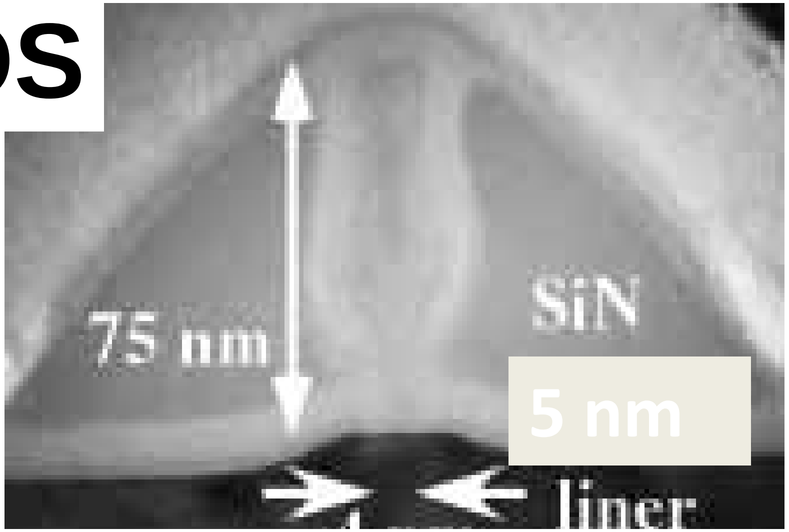
Channel length?



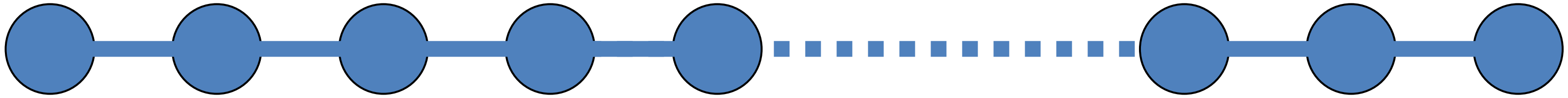


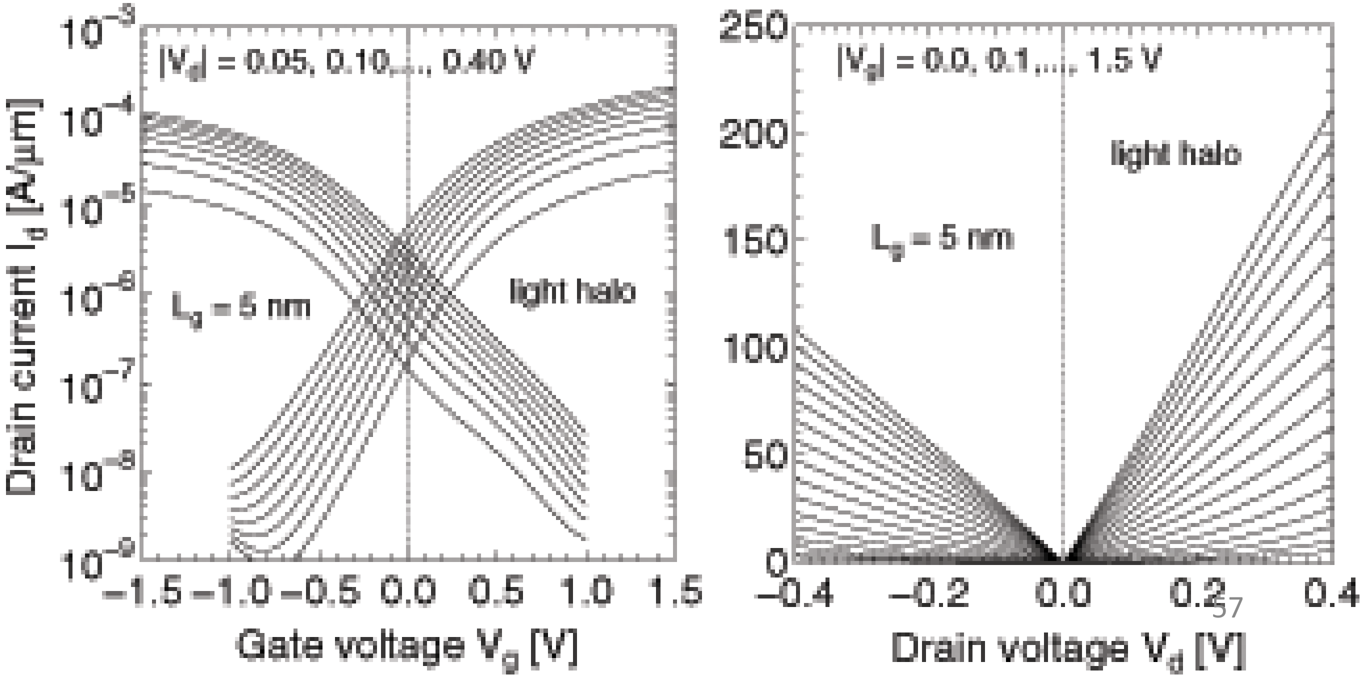
5 nm gate length CMOS

Is a Real Nano Device!!



Length of 18 Si atoms



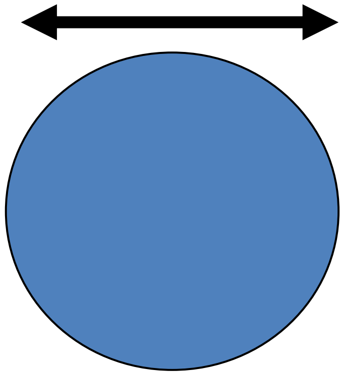


H. Wakabayashi et.al, NEC

IEDM, 2003

Electron wave length

10 nm



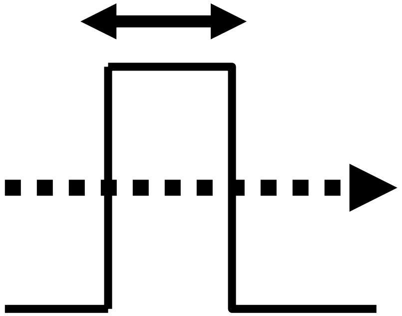
Downsizing limit!

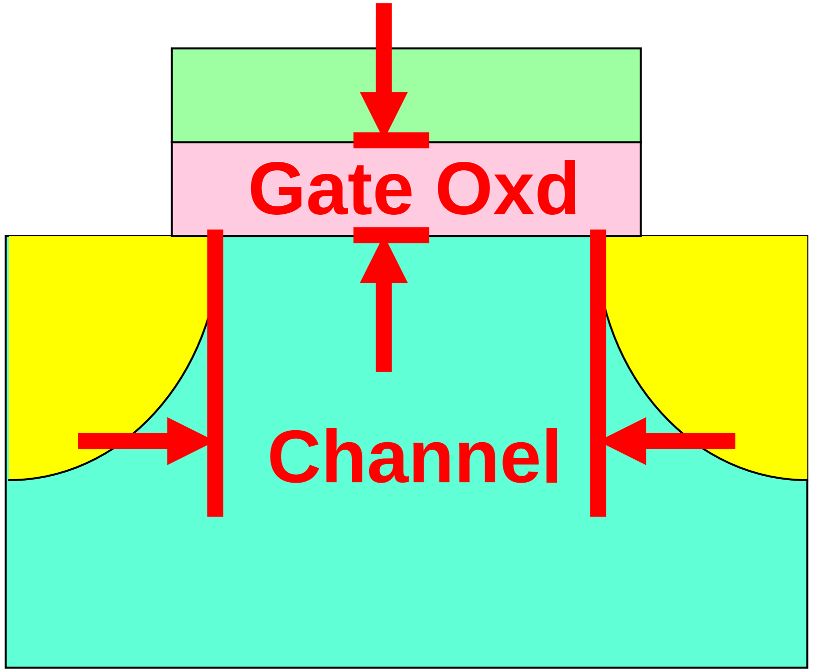
Channel length

Gate oxide thickness

Tunneling distance

3 nm

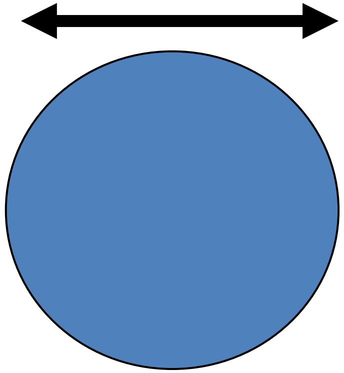




Prediction now!

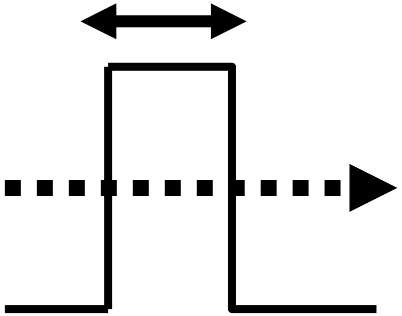
Electron wave length

10 nm



Tunneling distance

3 nm

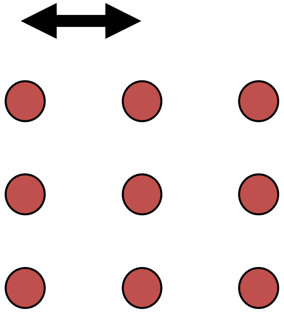


MOSFET operation

Lg = 2 ~ 1.5 nm?

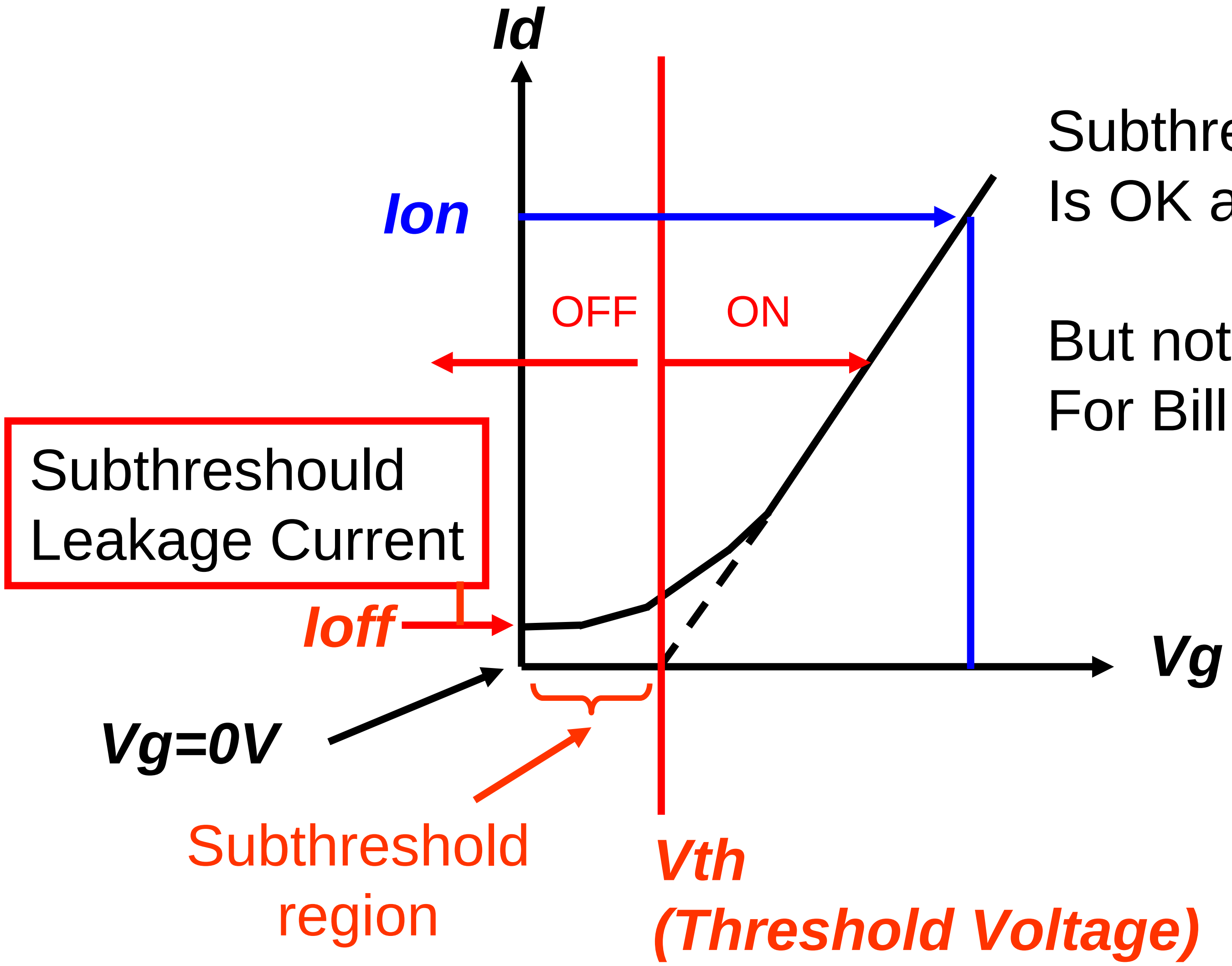
Atom distance

0.3 nm



Below this,
no one knows future!

Subtheshold leakage current of MOSFET



Subthreshold Current
Is OK at Single Tr. level

But not OK
For Billions of Trs.

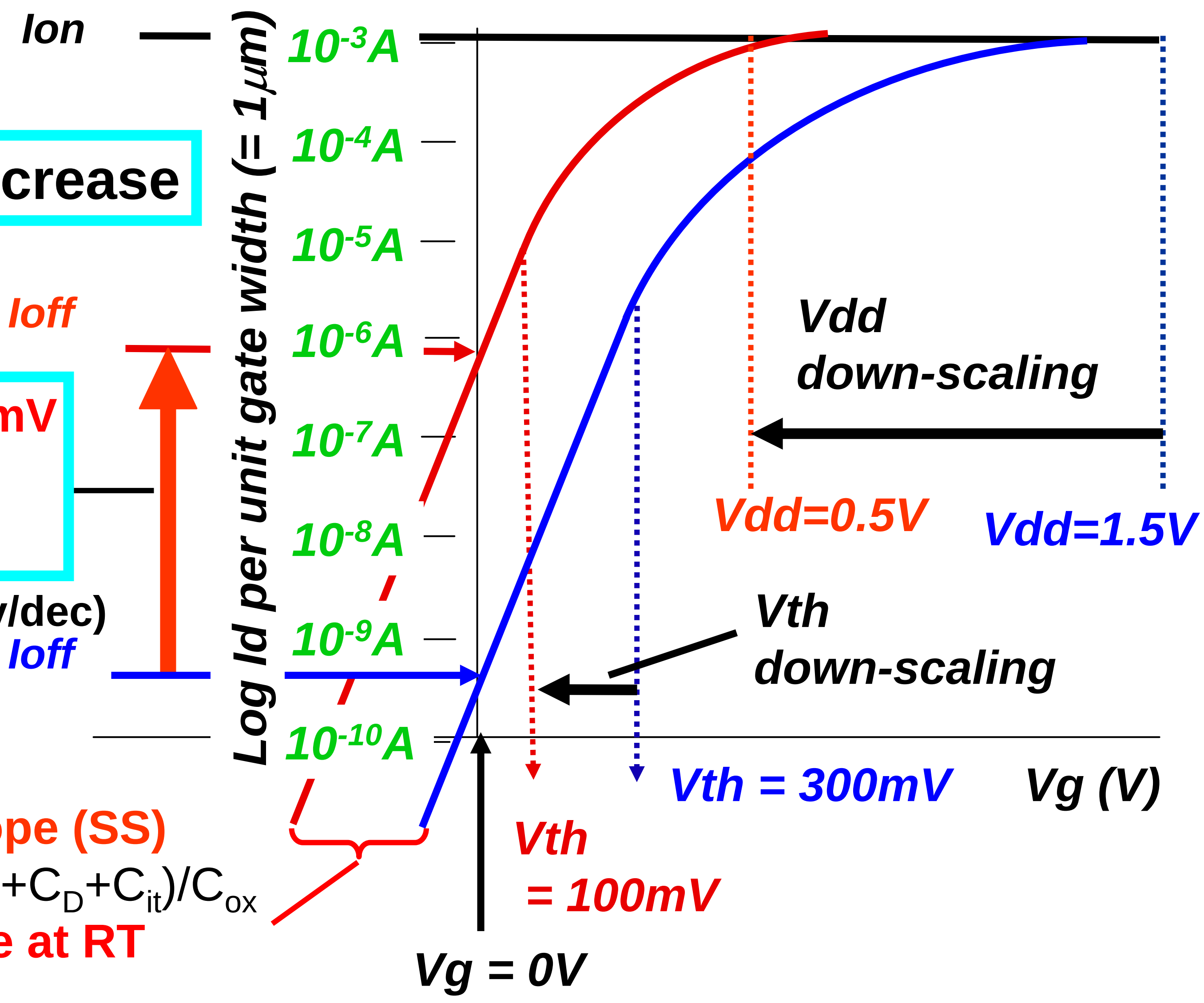
Vth cannot be decreased anymore

significant Ioff increase

Vth: 300mV → 100mV

Ioff increases with 3.3 decades

(300 – 100)mV/(60mv/dec) = 3.3 dec



Subthreshold slope (SS)

= (Ln10)(kT/q)(C_{ox}+C_D+C_{it})/C_{ox}

> **~ 60 mV/decade at RT**

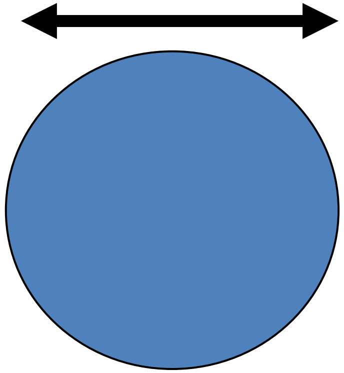
SS value:

Constant and does not become small with down-scaling

Prediction now!

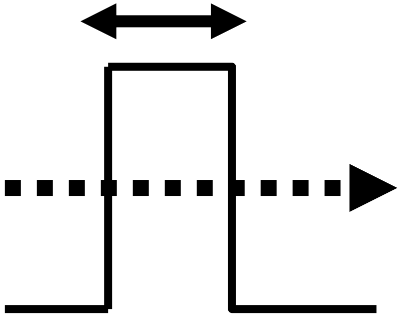
Electron wave length

10 nm



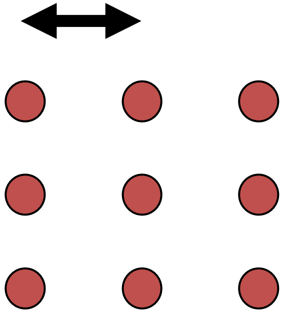
Tunneling distance

3 nm



Atom distance

0.3 nm



Practical limit for integration

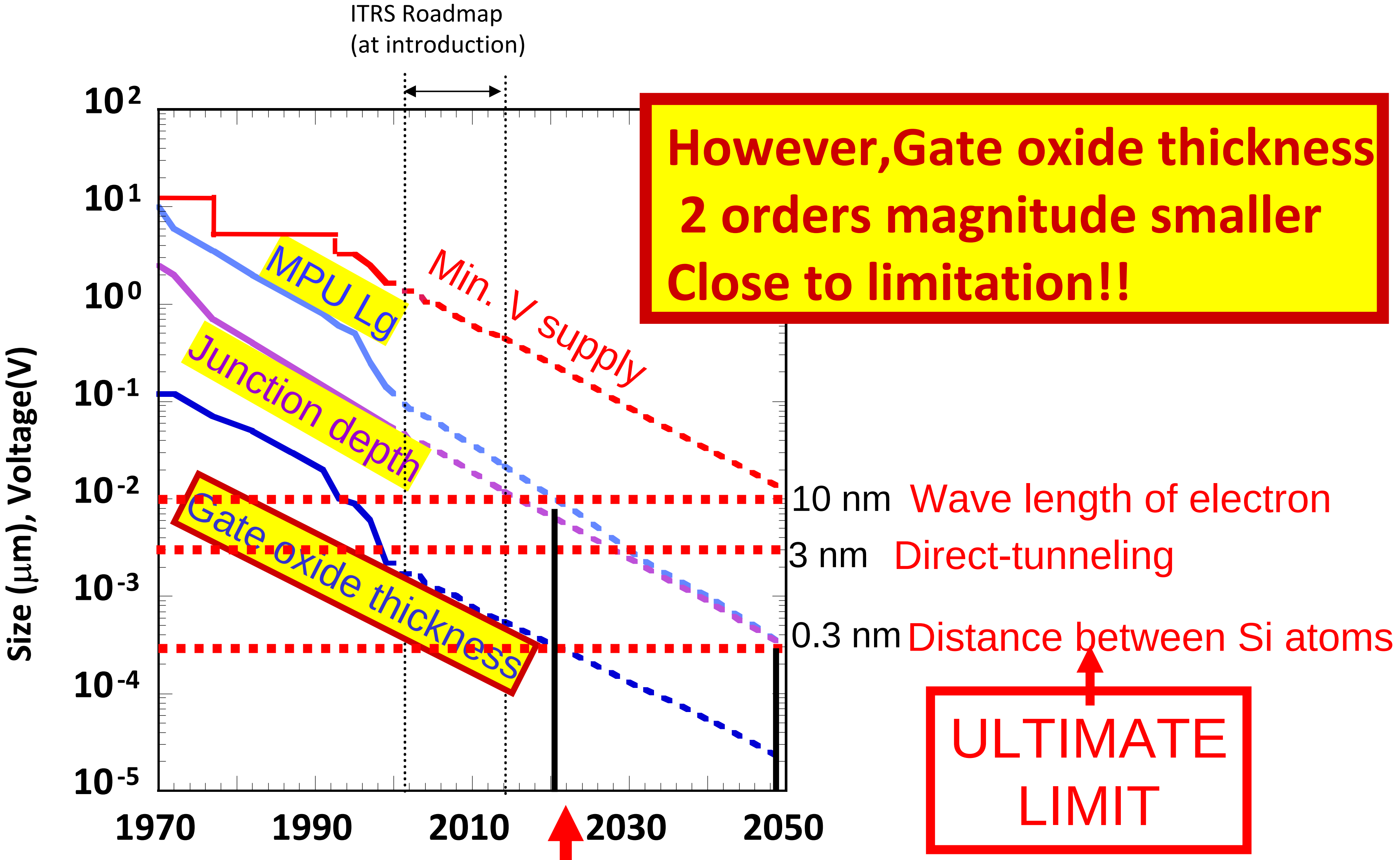
Lg = 5 nm?

MOSFET operation

Lg = 2 ~ 1.5 nm?

Below this,
no one knows future!

Ultimate limitation



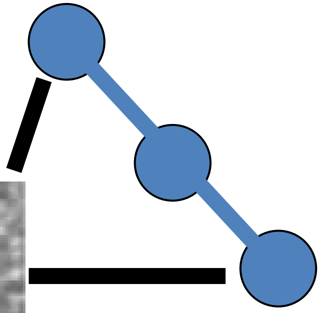
However,Gate oxide thickness 2 orders magnitude smaller Close to limitation!!

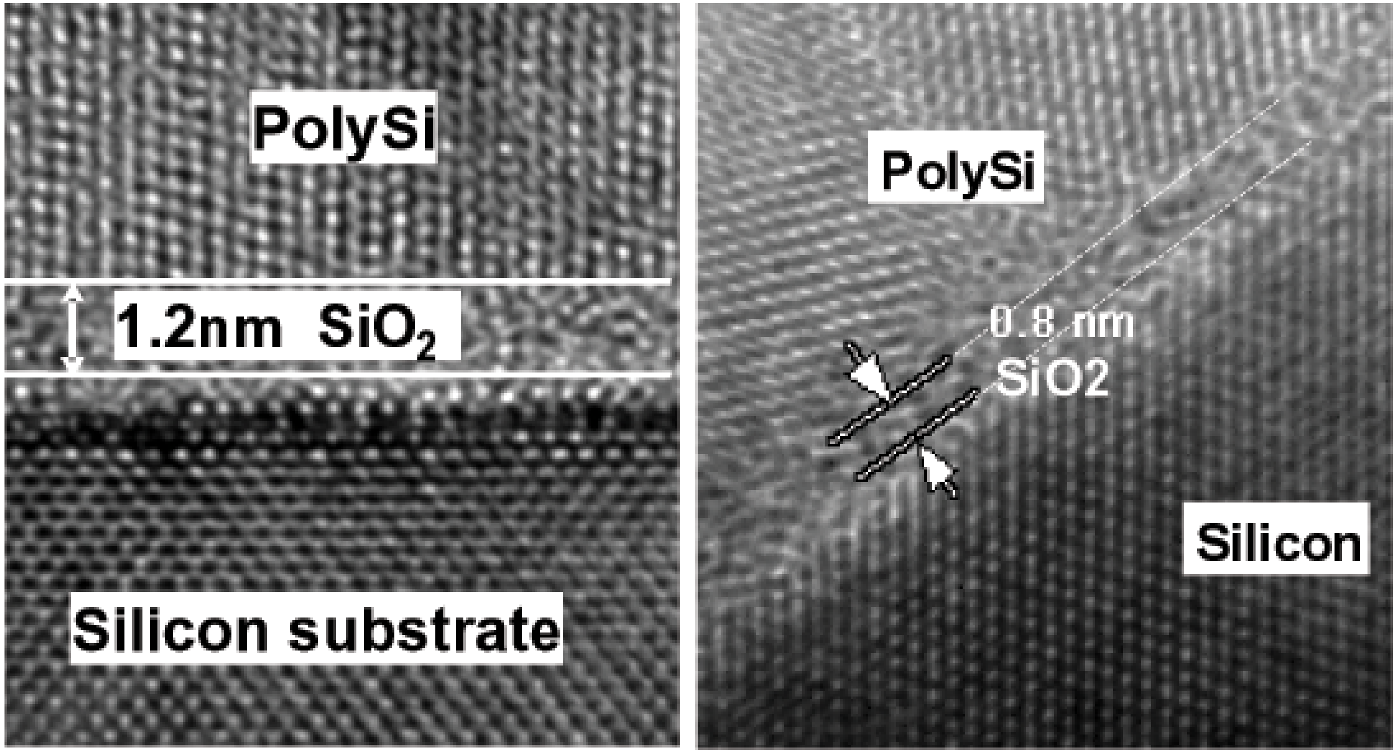
ULTIMATE LIMIT

Lg: Gate length downsizing will continue to another 10-15 years

0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!





- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003

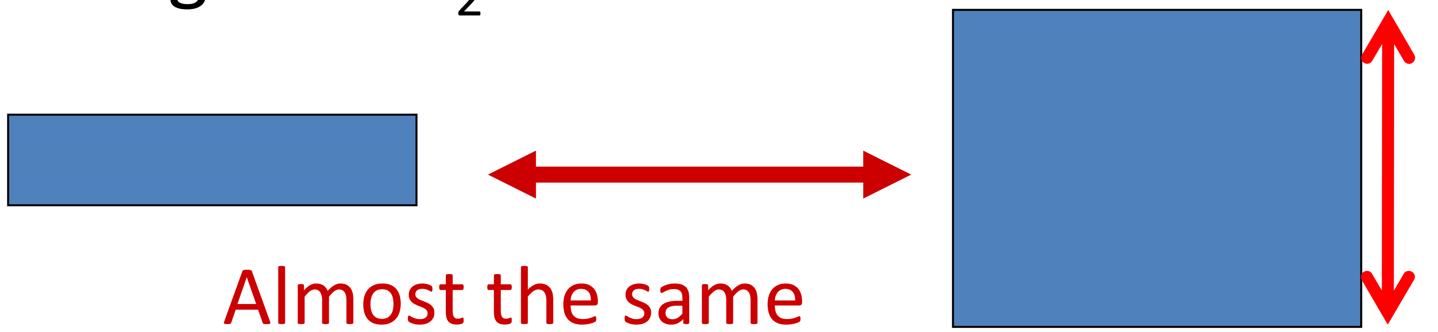
So, we are now in the limitation of downsizing?

Do you believe this or do not?

There is a solution!

K: Dielectric Constant

To use high-k dielectrics



Thin gate SiO_2

Thick gate high-k dielectrics

Thick ↓ Small leakage Current

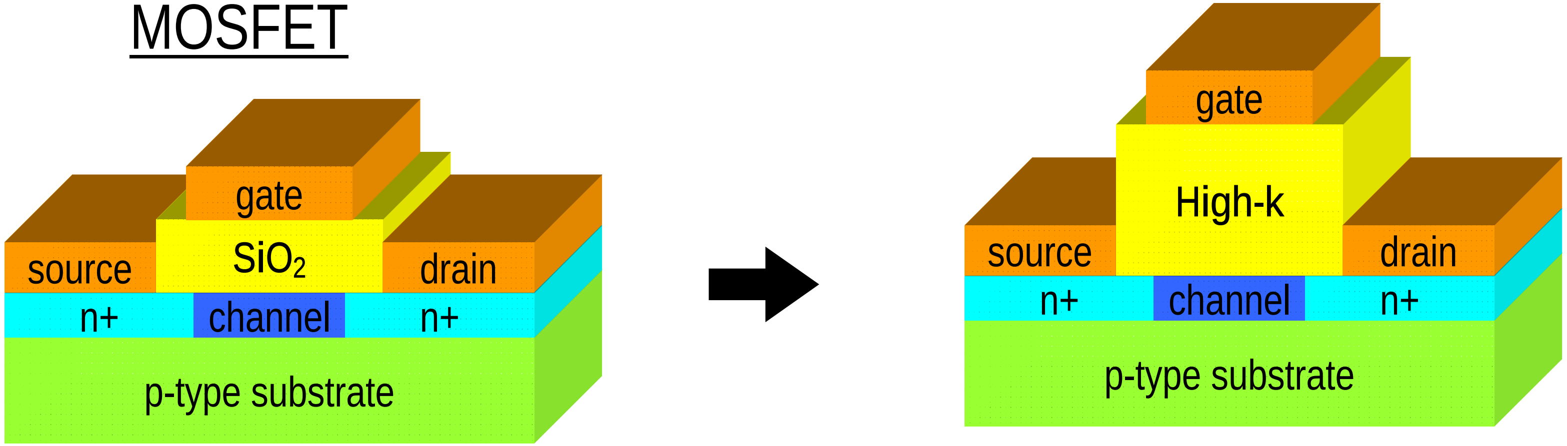
Almost the same electric characteristics

However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO_2!

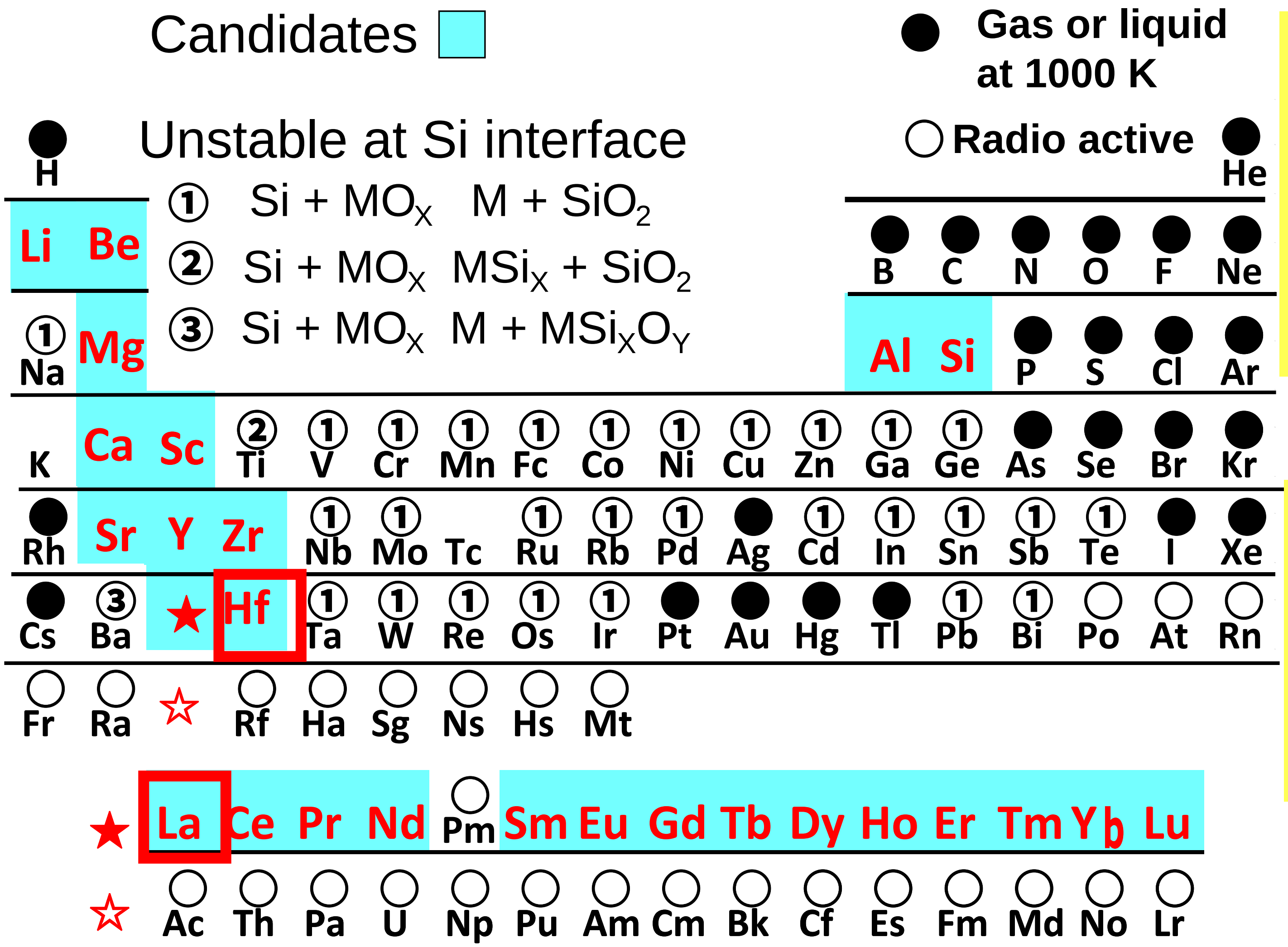
High-k Thin Film for Gate Insulator

MOSFET



	2005	2008	2010	2015
Physical Gate Length (nm)	**32**	**22**	**18**	**10**
Equivalent Oxide Thickness (nm)	**1.1**	**0.8**	**0.7**	**0.6**

Choice of High-k elements for oxide



Candidates 🟦

● **Gas or liquid at 1000 K**

○ **Radio active**

Unstable at Si interface

① Si + MO_X M + SiO_2

② Si + MO_X MSi_X + SiO_2

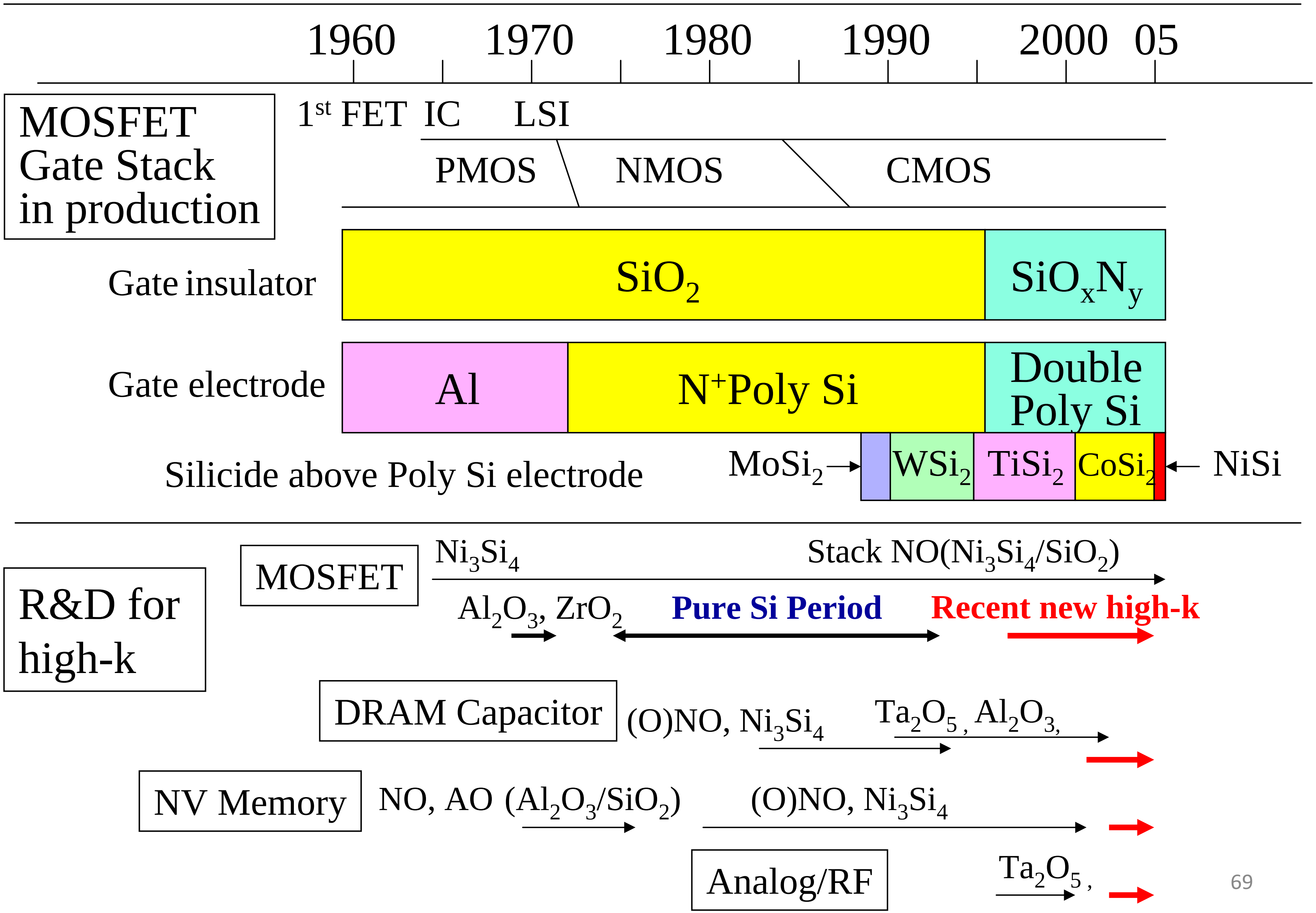
③ Si + MO_X M + MSi_XO_Y

HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

Historical trend of high-k R& D



1960 1970 1980 1990 2000 05

MOSFET Gate Stack in production

1^{st} FET IC LSI

PMOS NMOS CMOS

Gate insulator: SiO_2 | SiO_xN_y

Gate electrode: Al | N^+Poly Si | Double Poly Si

Silicide above Poly Si electrode: $MoSi_2$ → | WSi_2 | $TiSi_2$ | $CoSi_2$ | ← NiSi

R&D for high-k

MOSFET: Ni_3Si_4 Stack NO(Ni_3Si_4/SiO_2)

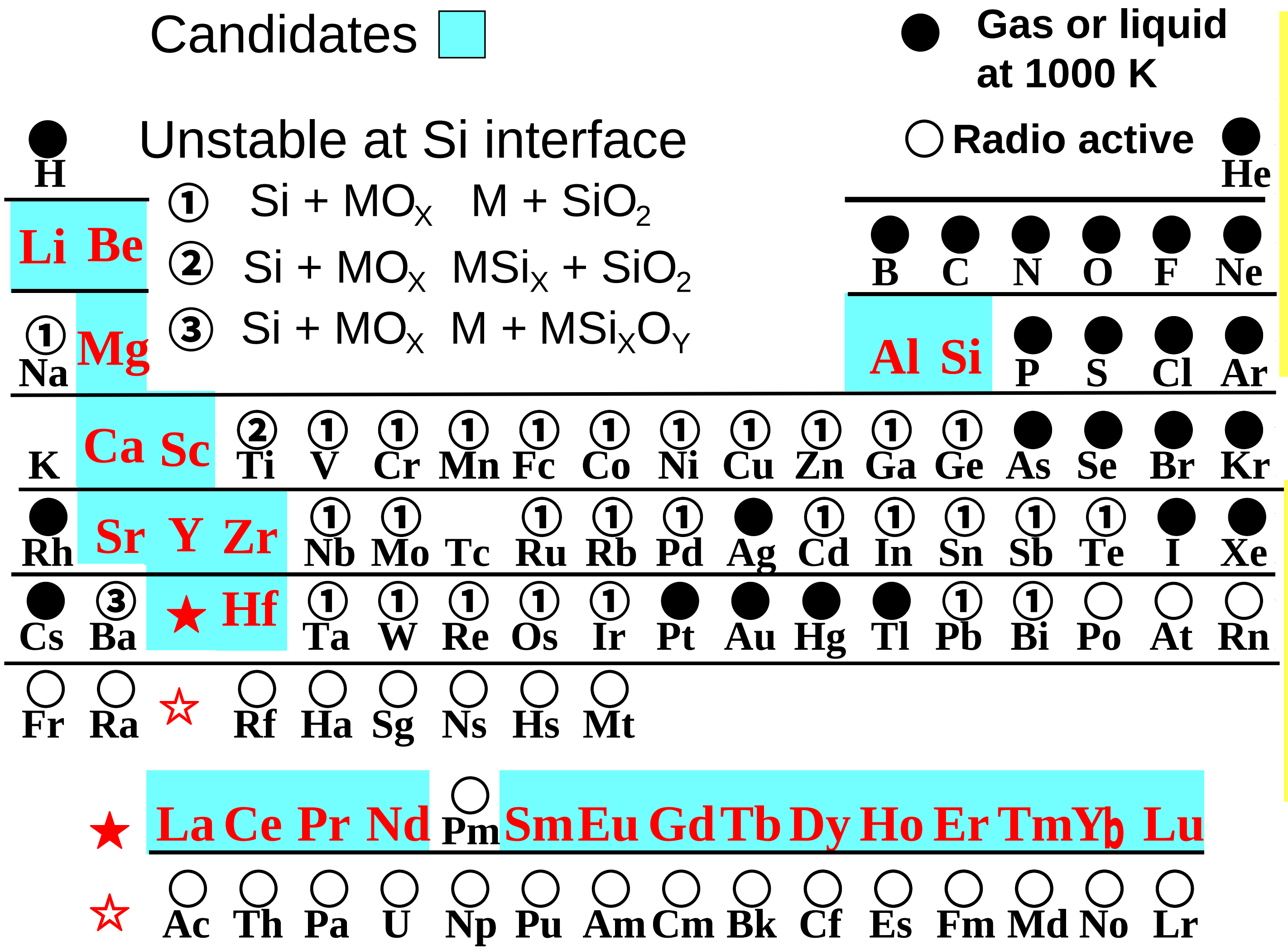
Al_2O_3, ZrO_2 **Pure Si Period** **Recent new high-k**

DRAM Capacitor: (O)NO, Ni_3Si_4 Ta_2O_5, Al_2O_3,

NV Memory: NO, AO (Al_2O_3/SiO_2) (O)NO, Ni_3Si_4

Analog/RF: Ta_2O_5,

Choice of High-k



Candidates 🟦

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② Si + MO_X MSi_X + SiO_2

③ Si + MO_X M + MSi_XO_Y

● H																	● He
🟦 Li	🟦 Be											● B	● C	● N	● O	● F	● Ne
① Na	🟦 Mg											🟦 Al	🟦 Si	● P	● S	● Cl	● Ar
K	🟦 Ca	🟦 Sc	② Ti	① V	① Cr	① Mn	① Fc	① Co	① Ni	① Cu	① Zn	① Ga	① Ge	● As	● Se	● Br	● Kr
● Rh	🟦 Sr	🟦 Y	🟦 Zr	① Nb	① Mo	Tc	① Ru	① Rb	① Pd	● Ag	① Cd	① In	① Sn	① Sb	① Te	● I	● Xe
● Cs	③ Ba	🟦 ★	🟦 Hf	① Ta	① W	① Re	① Os	① Ir	● Pt	● Au	● Hg	● Tl	① Pb	① Bi	○ Po	○ At	○ Rn
○ Fr	○ Ra	☆	○ Rf	○ Ha	○ Sg	○ Ns	○ Hs	○ Mt									

★	🟦 La	🟦 Ce	🟦 Pr	🟦 Nd	○ Pm	🟦 Sm	🟦 Eu	🟦 Gd	🟦 Tb	🟦 Dy	🟦 Ho	🟦 Er	🟦 Tm	🟦 Yb	🟦 Lu
☆	○ Ac	○ Th	○ Pa	○ U	○ Np	○ Pu	○ Am	○ Cm	○ Bk	○ Cf	○ Es	○ Fm	○ Md	○ No	○ Lr

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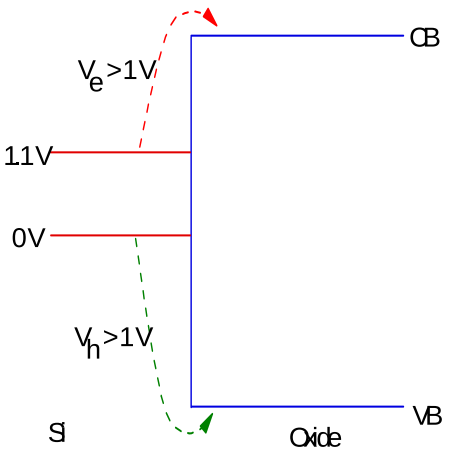
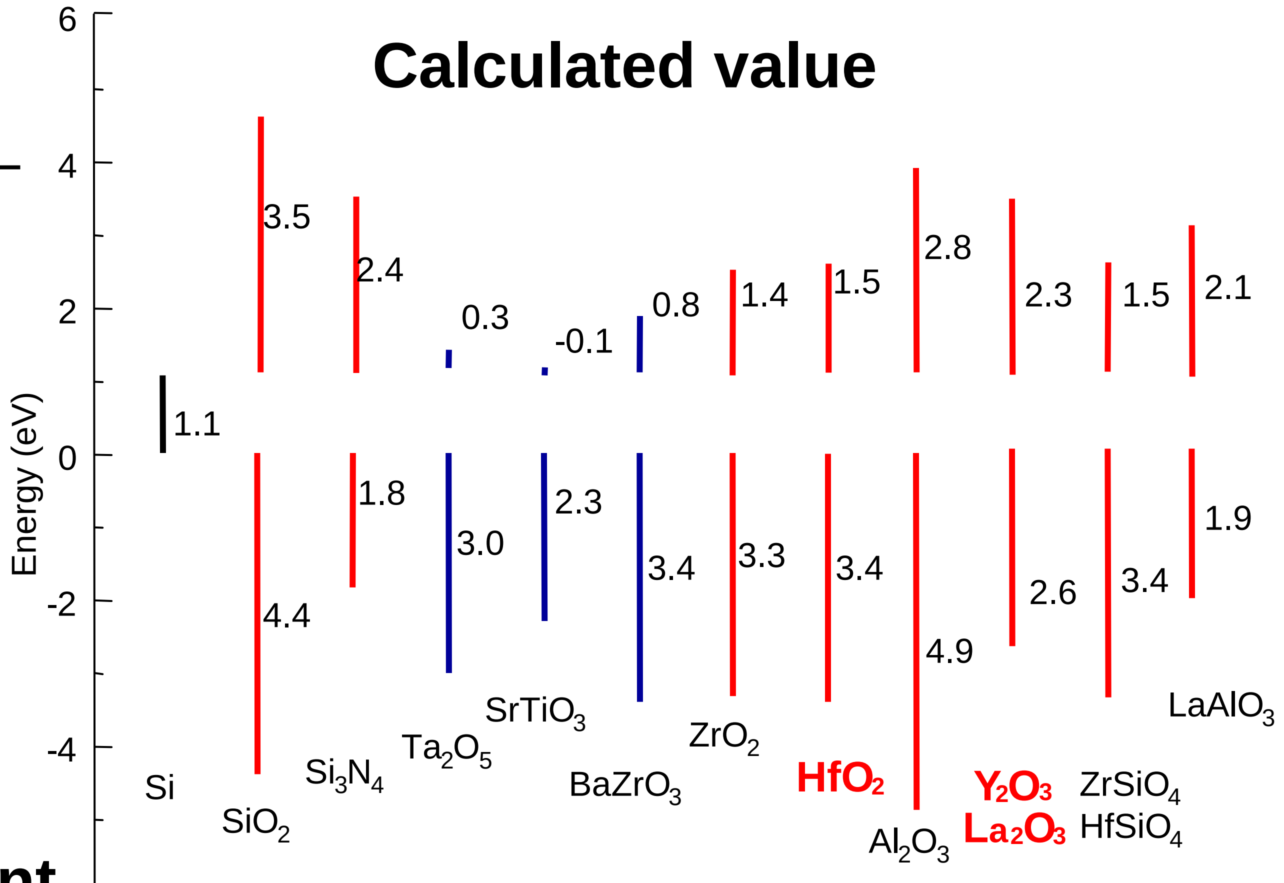
R. Hauser, IEDM Short Course, 1999

Hubbard and Schlom, J Mater Res 11 2757 (1996)

Band Offsets





Calculated value

J Robertson, J Vac Sci Technol B **18** 1785 (2000)

Dielectric constant

SiO2; 4
Si3N4: ~ 7
Al2O3: ~ 9

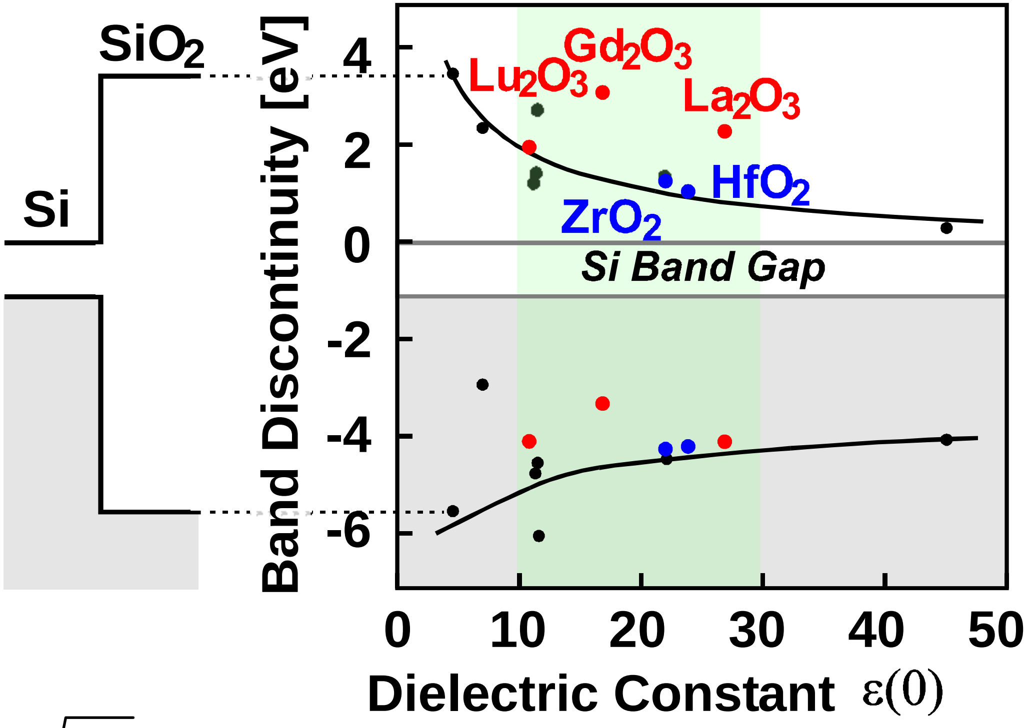
Y2O3; ~10
Gd2O3: ~10

HfO2; ~23
La2O3: ~27

HfO2 was chosen for the 1st generation
La2O3 is more difficult material to treat

Dielectric constant value vs. Band offset (Measured)

SiO_2	3.9
Al_xSi_yOz	
$(Ba,Sr)TiO_3$	200-300
$BeAl_2O4$	8.3-9.43
CeO_2	16.6-26
$CeHfO_4$	10-20
$CoTiO_3/Si_3N_4$	
$EuAlO_3$	22.5
HfO_2	26-30
Hf silicate	11
La_2O_3	20.8
$LaScO_3$	30
La_2SiO_5	
$MgAl_2O_4$	
$NdAlO_3$	22.5
$PrAlO_3$	25
Si_3N_4	7
$SmAlO_3$	19
$SrTiO_3$	150-250
Ta_2O_5	25-24
Ta_2O_5-TiO_2	
TiO_2	86-95
TiO_2/Si_3N_4	
Y_2O_3	8-11.6
$Y_xSi_yO_z$	
ZrO_2	22.2-28
Zr-Al-O	
Zr silicate	
$(Zr,Sn)TiO_4$	40-60

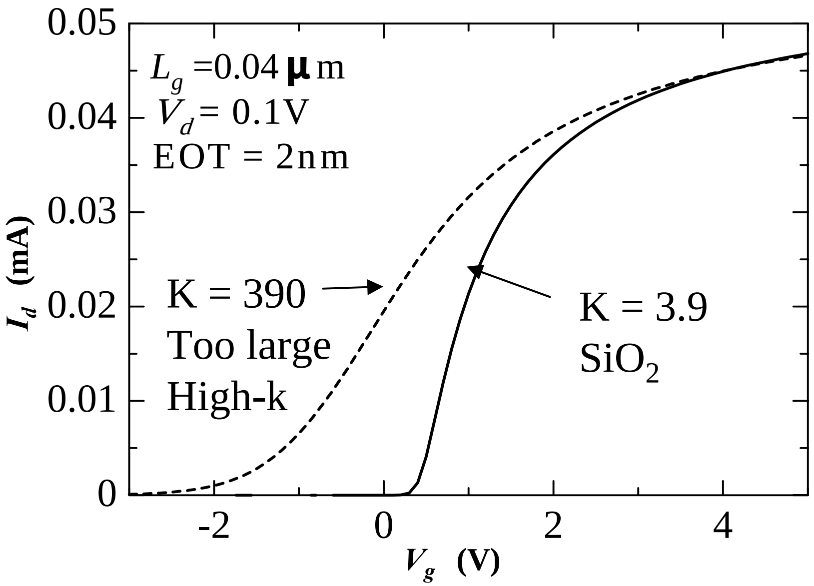


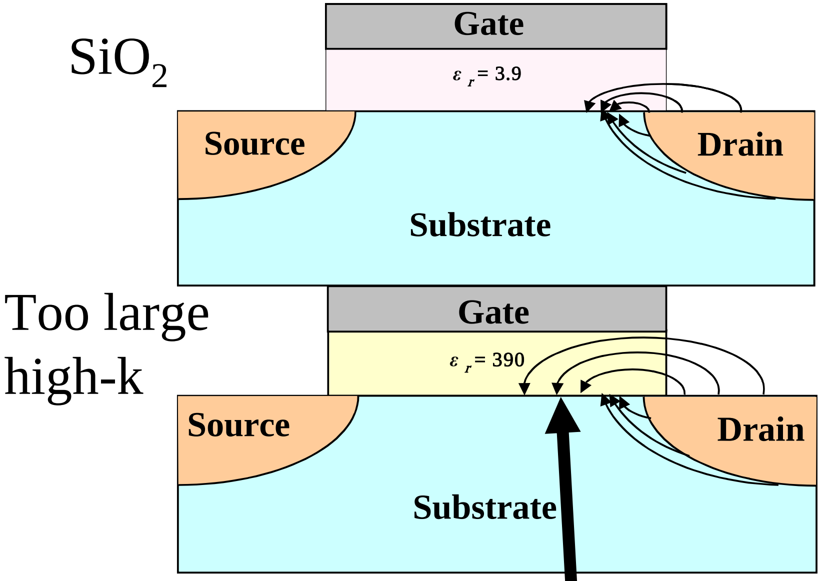
$\sqrt{\phi_B} * k$: Figure of Merit of High-k

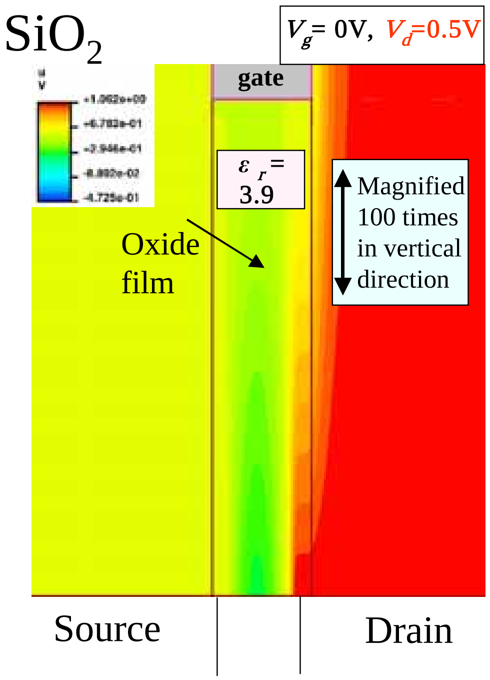
C.A. Billmann et al.,, MRS Spring Symp., 1999,
R.D.Shannon, J. Appl. Phys., 73, 348, 1993
S. De Gebdt, IEDM Short Coyuse, 2004

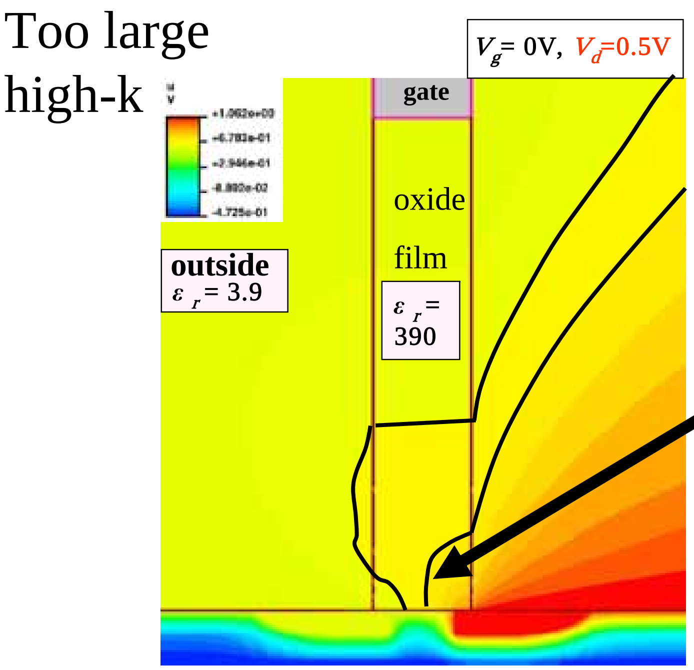
T. Hattori, INFOS , 2003

Too large high-k cause significant short channel effect







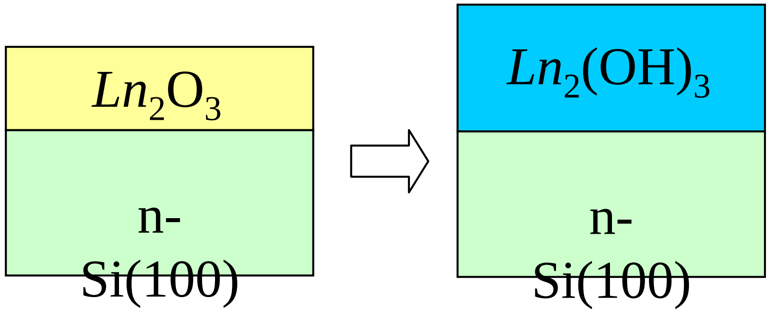


Penetration of lateral field from Drain through high-k causes significant short channel effects

Absorption of moisture and CO_2

The oxides become hydroxide and carbonate in H_2O and CO_2 ambient.

hydroxide

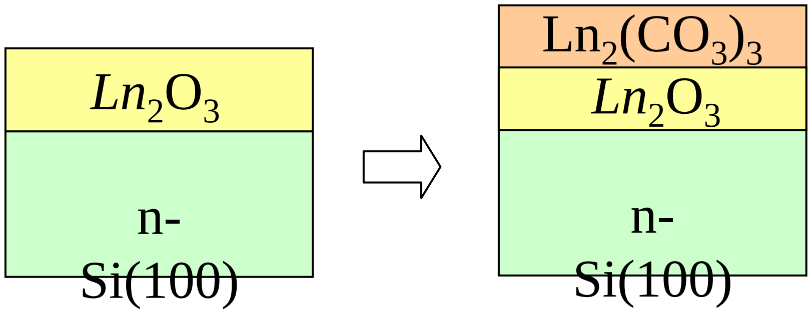


$$Ln_2O_3 + H_2O \rightarrow Ln_2O_3 \cdot H_2O$$

$$Ln_2O_3 + H_2O \rightarrow 2(LnOOH)$$

$$2Ln(OH) + H_2O \rightarrow 3Ln_2(OH)_3$$

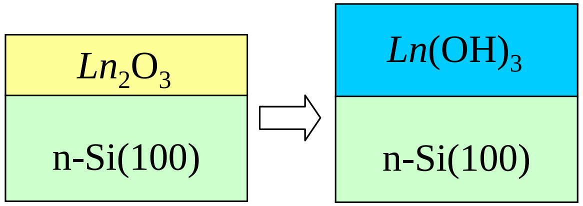
carbonate



$$Ln_2O_3 + CO_2 \rightarrow Ln_{2O2}(CO_3)$$

※*Ln*：Lanthanide

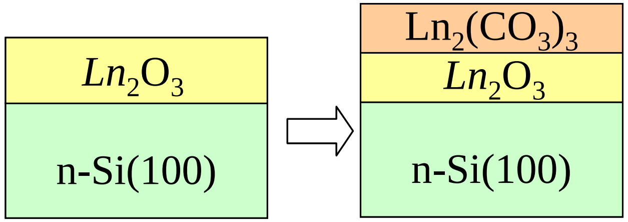
Hygroscopic Properties of La_2O_3



$Ln_2O_3 + H_2O \rightarrow Ln_2O_3 \cdot H_2O$

$Ln_2O_3 \cdot H_2O \rightarrow 2(LnOOH)$

$LnOOH + H_2O \rightarrow Ln(OH)_3$

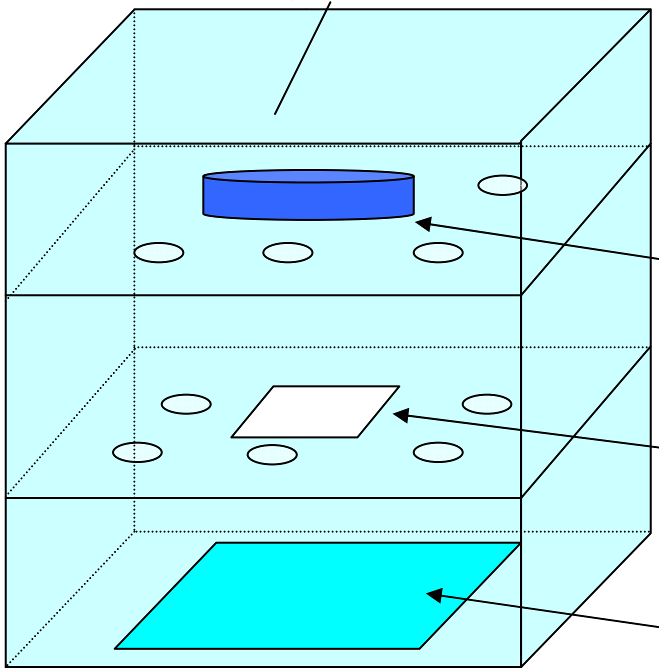


$Ln_2O_3 + 2CO_2 \rightarrow Ln_2(CO_3)_3$

After 30 hours in clean room (temperature & humidity controlled)

Experimental apparatus

Temperature: ~20°C
Humidity: 80%
Humidification time:
0 ~120 hrs



acryl(PMMA)
or glass(PYREX)

Thermometer
Hygrometer

Samples

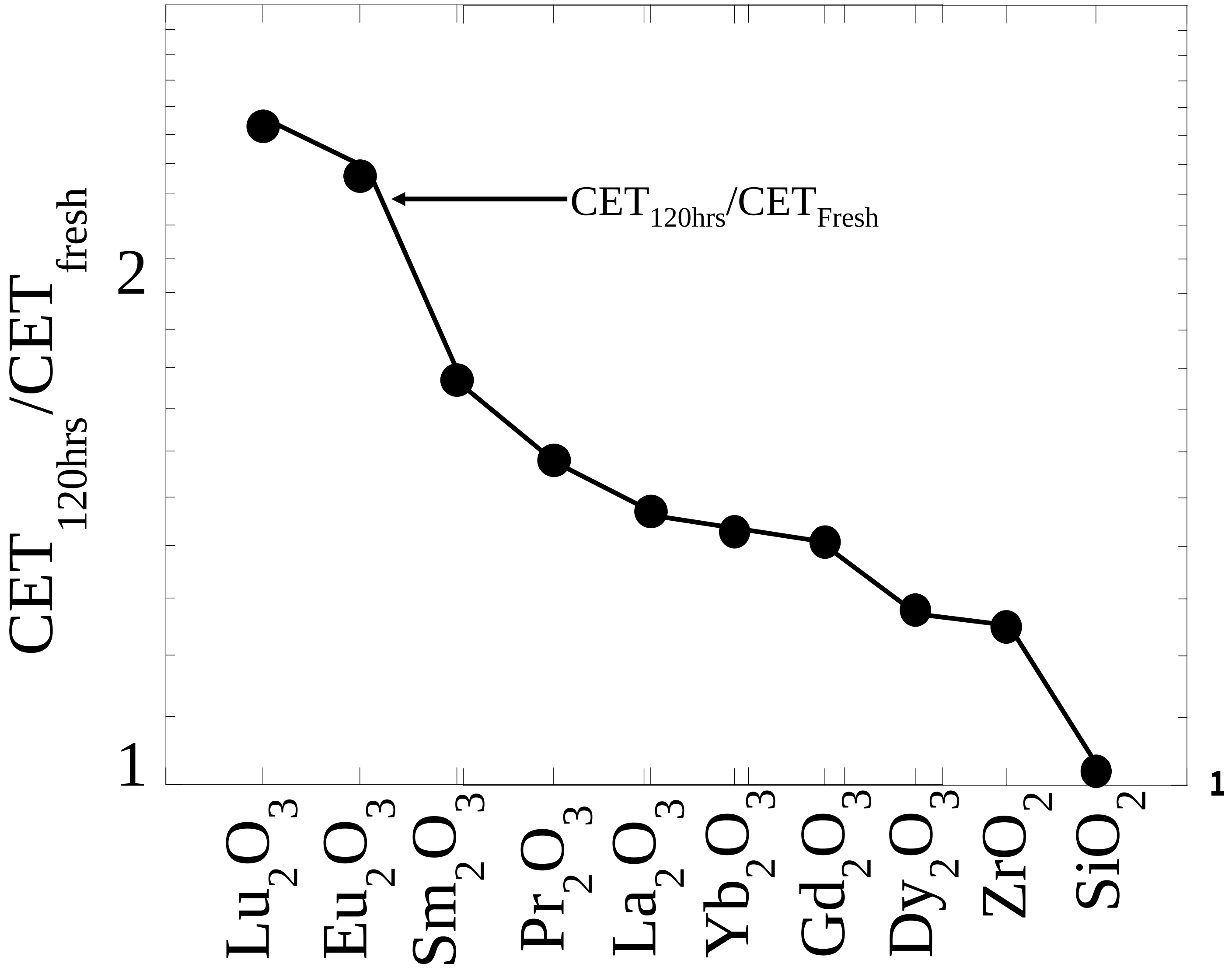
Ultra pure
water

glass
(PYREX)

acryl
(PMMA)

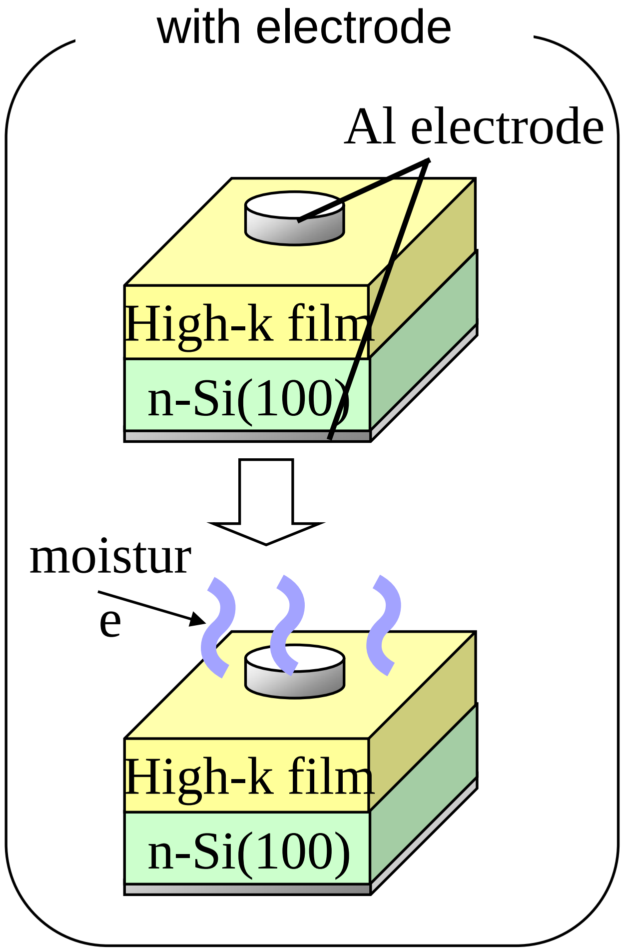
*PMMA :
$CH_2C(CH)_3COOCH_3$

Change of CET for all studied

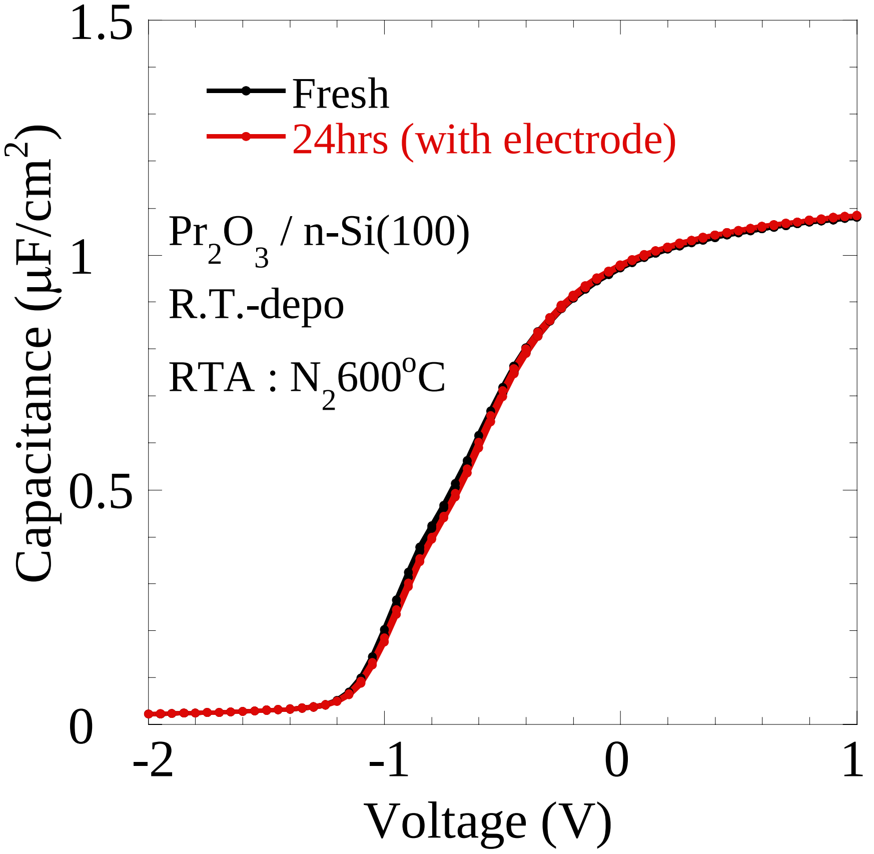


Absorption test in case of acryl apparatus after the Al electrode formation

→ Moisture absorption is protected

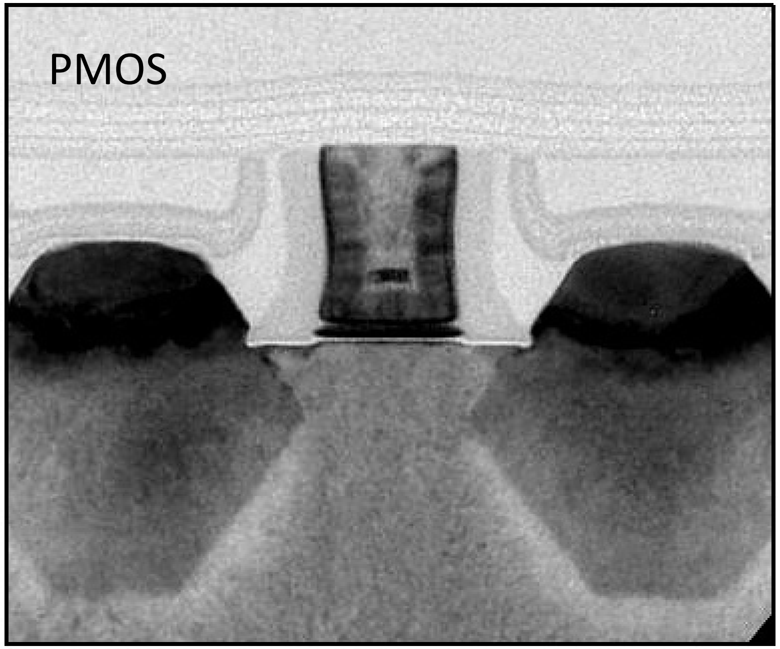


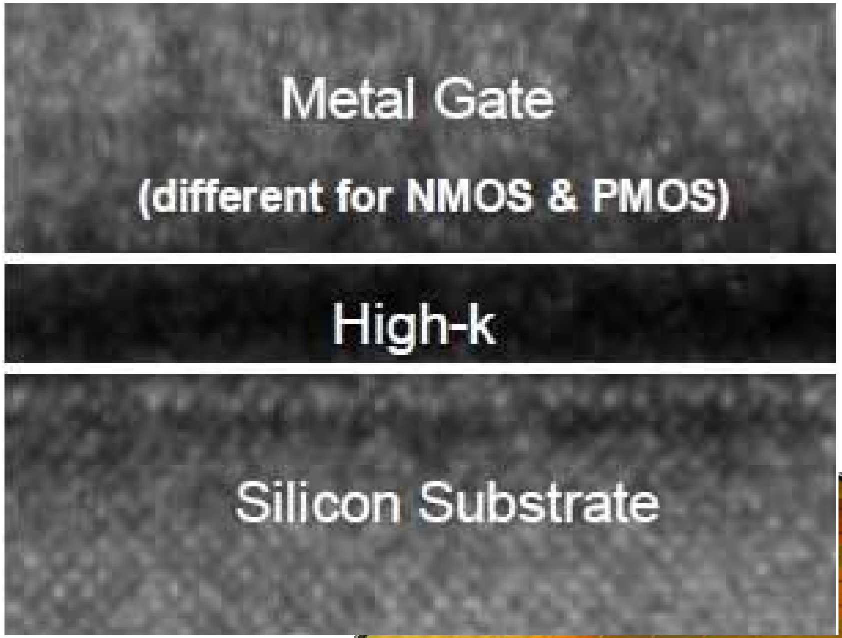
C-V

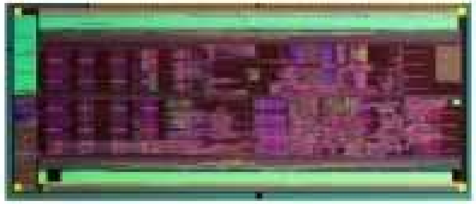


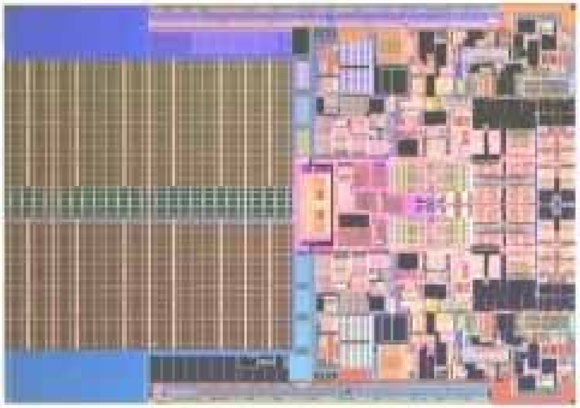
High-k gate insulator MOSFETs for Intel: EOT=1nm

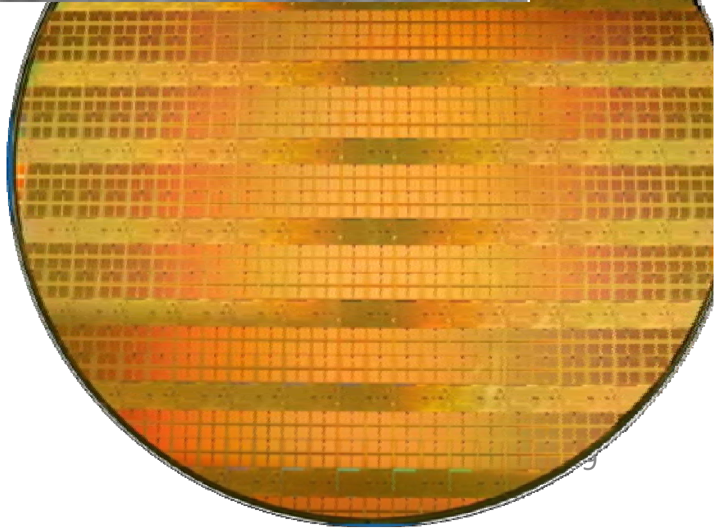
EOT: Equivalent Oxide Thickness



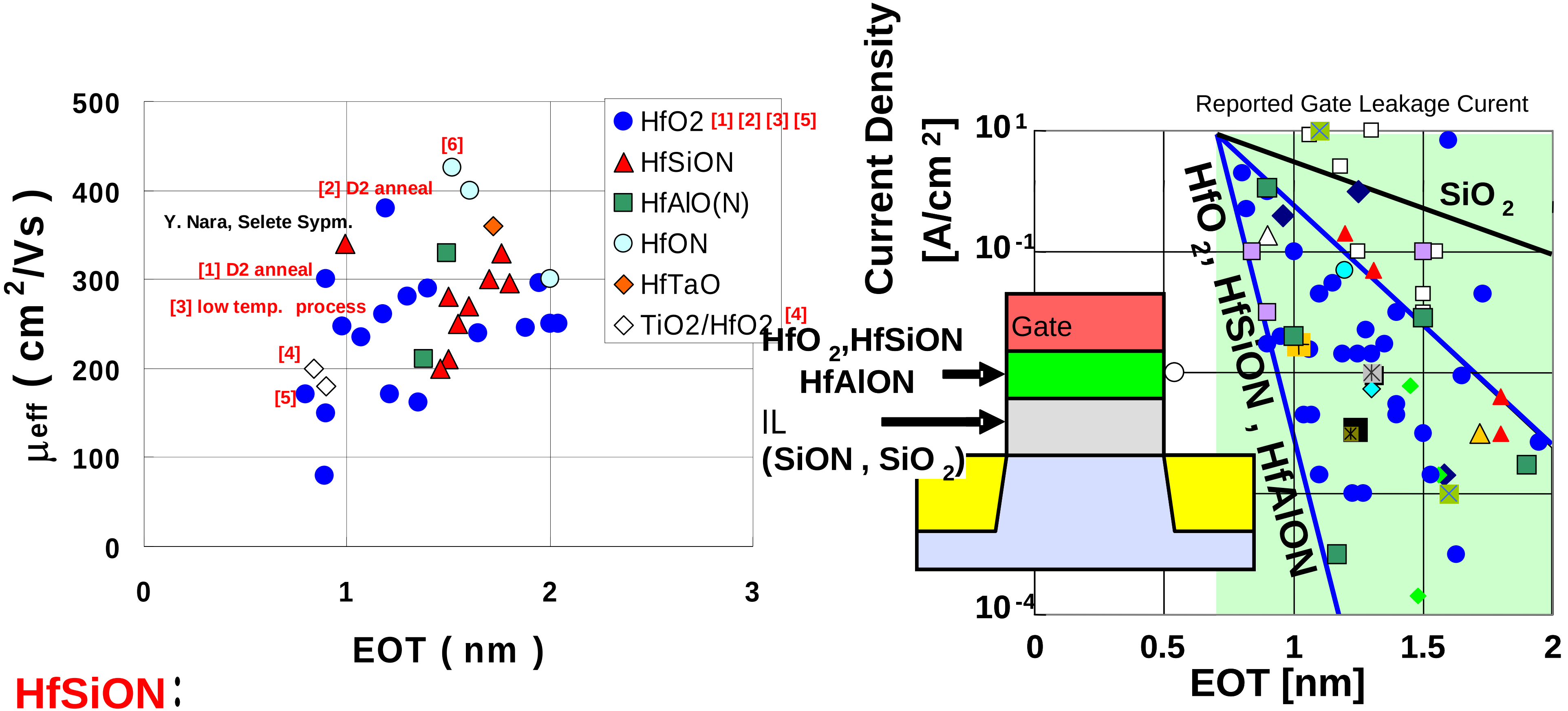








Present Status of high-k Research



HfSiON：

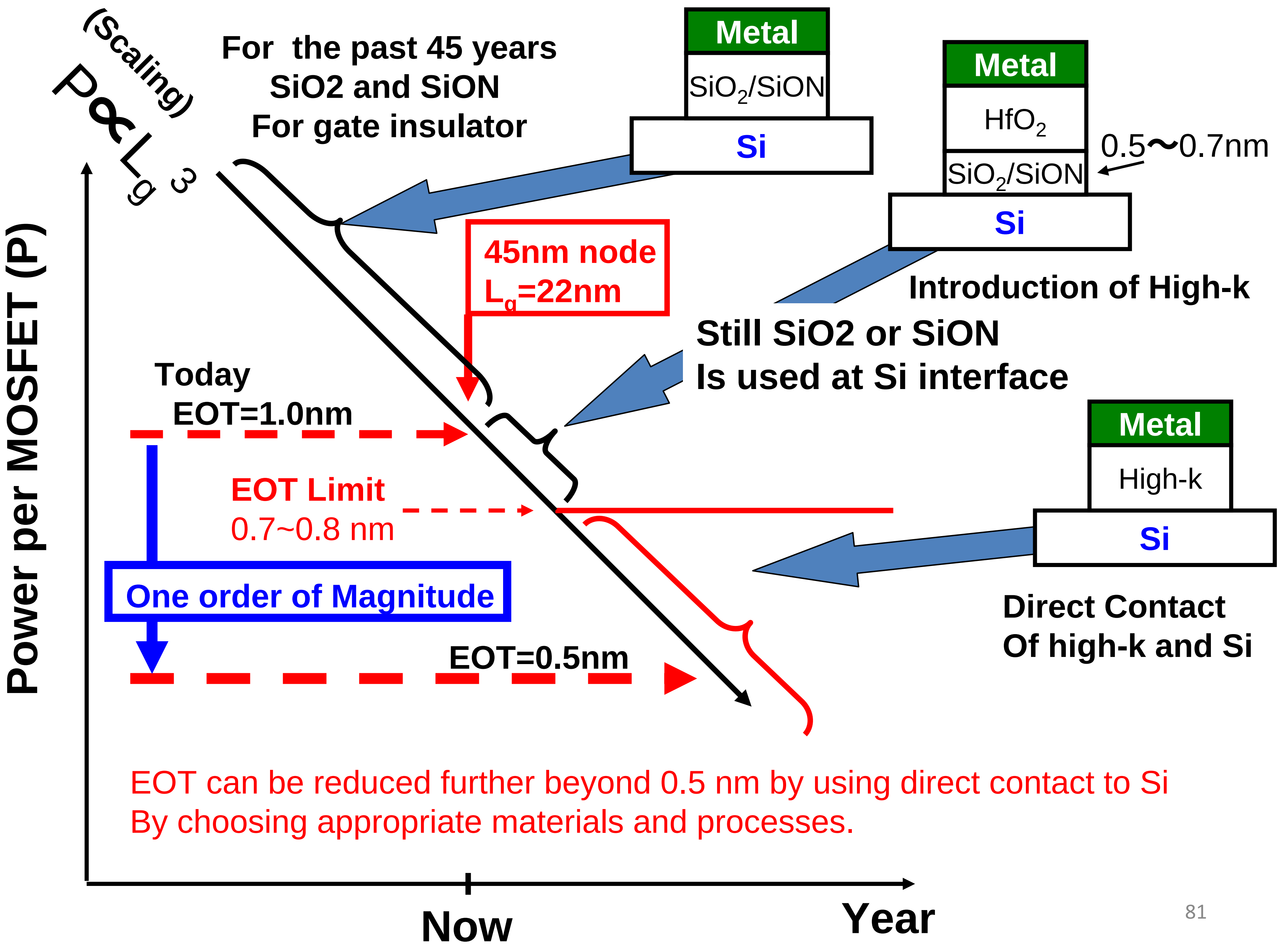
- High effective mobility even at EOT=1nm

- Thermal stability

- IL of 0.5~0.7nm is essential for high μ

- Difficult to achieve EOT<0.7nm ?

[1]C. Choi, VLSI05
[2]R. Choi, IEDM02
[3]Y. Akasaka, VLSI05
[4]S. J. Rhee, IEDM04
[5] L. A. Rangersson, VLSI05
[6]C. H. Choi, IEDM02
[7]S. J. Rhee, VLSI05



For the past 45 years
SiO2 and SiON
For gate insulator

Metal
$SiO_2/SiON$
Si

Metal
HfO_2
$SiO_2/SiON$
Si
0.5〜0.7nm

Introduction of High-k

45nm node
L_g=22nm

Still SiO2 or SiON
Is used at Si interface

Today
EOT=1.0nm

EOT Limit
0.7~0.8 nm

One order of Magnitude

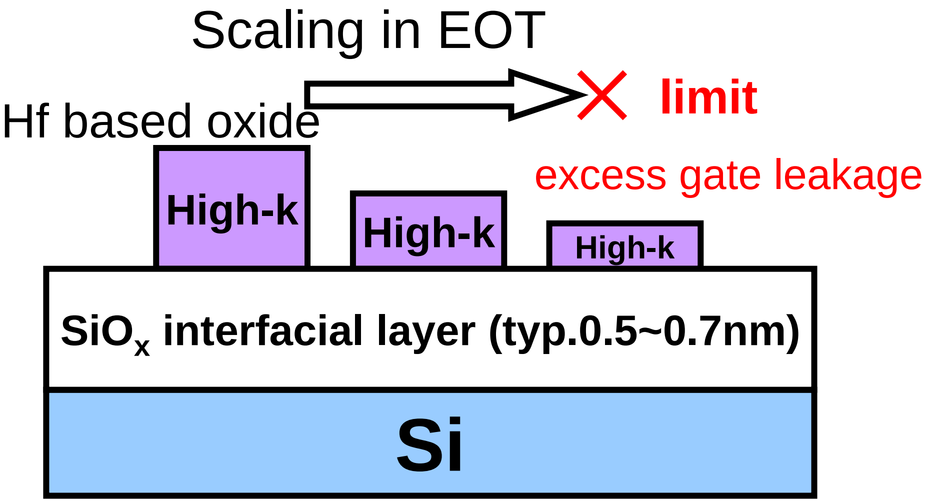
EOT=0.5nm

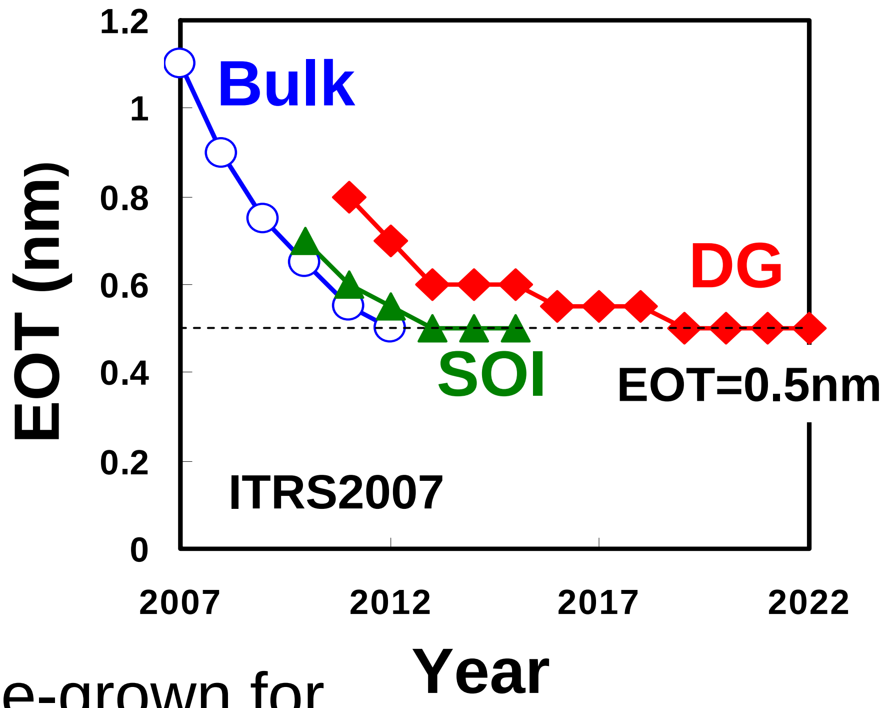
Metal
High-k
Si

Direct Contact
Of high-k and Si

EOT can be reduced further beyond 0.5 nm by using direct contact to Si
By choosing appropriate materials and processes.

High-k for Further Scaling



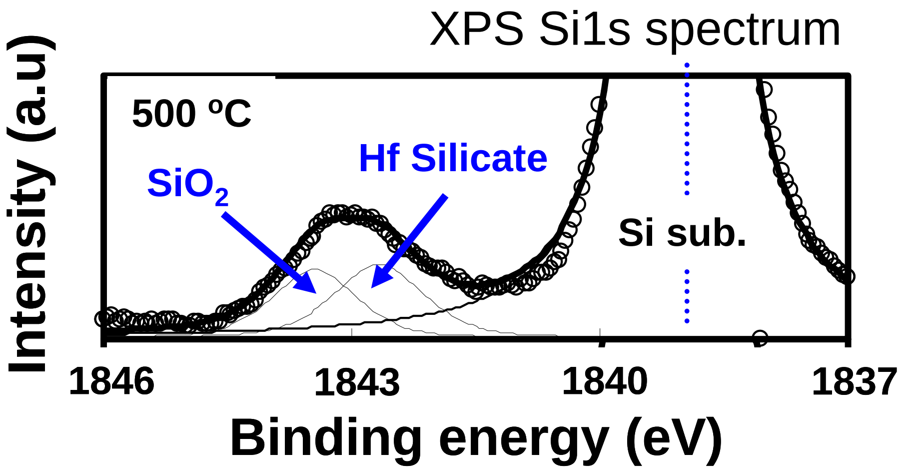


SiO_2 interfacial layer inserted or re-grown for

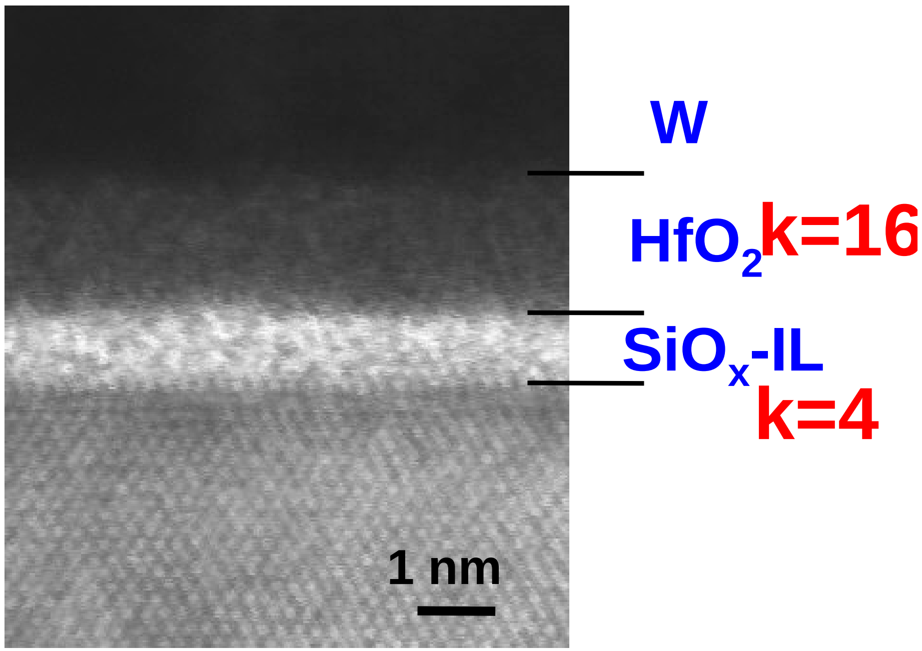
- recovery of degraded mobility
- interface state, reliability (TDDB, BTI), etc.

- **SiO_2-IL free structure (direct contact of high-k/Si) is required for EOT=0.5nm**
- **EOT scaling is expected down to 0.5 nm in ITRS**

SiO_x-IL growth at HfO_2/Si Interface



TEM image 500 ºC 30min



Phase separator

$$HfO_2 + Si + O_2 \rightarrow HfO_2 + Si + 2O^* \rightarrow HfO_2 + SiO_2$$

H. Shimizu, JJAP, 44, pp. 6131

Oxygen supplied from W gate electrode

D.J.Lichtenwalner, Tans. ECS 11, 319

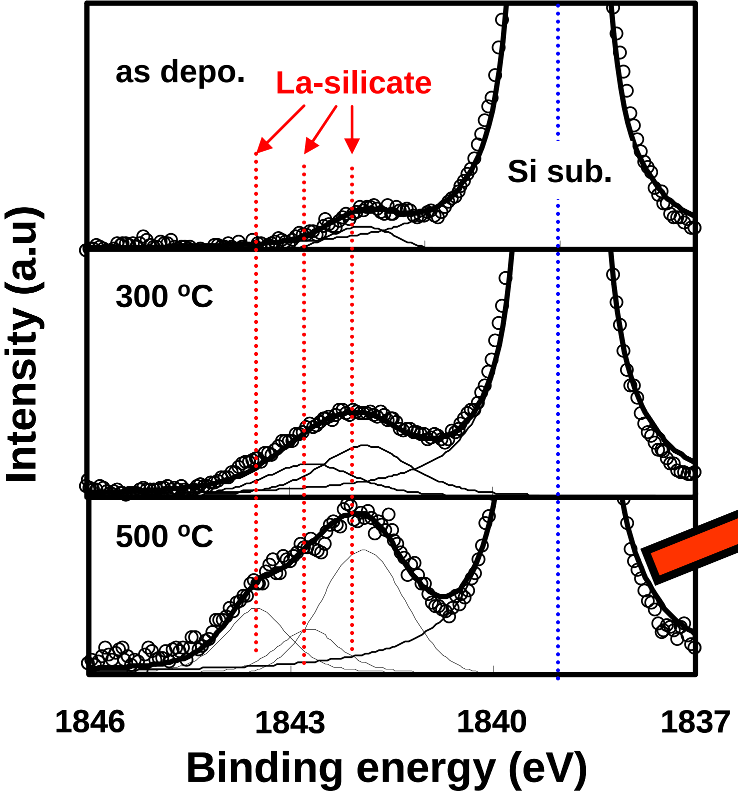
SiO_x-IL is formed after annealing

Oxygen control is required for optimizing the reaction

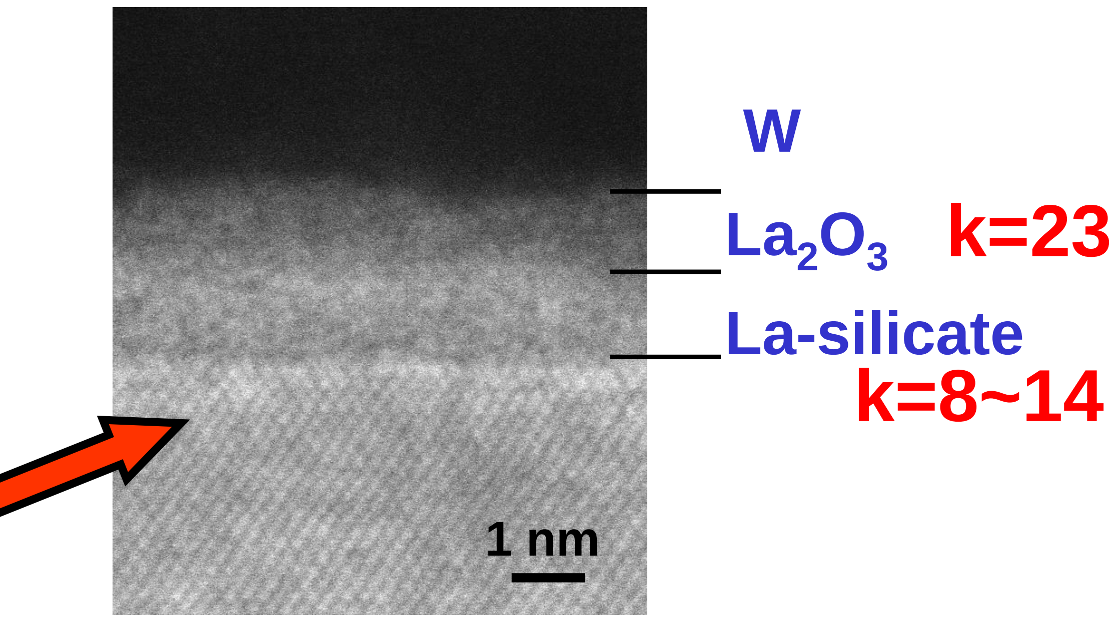
La-Silicate Reaction at La_2O_3/Si

Direct contact high-k/Si is possible

XPS Si1s spectra



TEM image **500 ºC, 30 min**



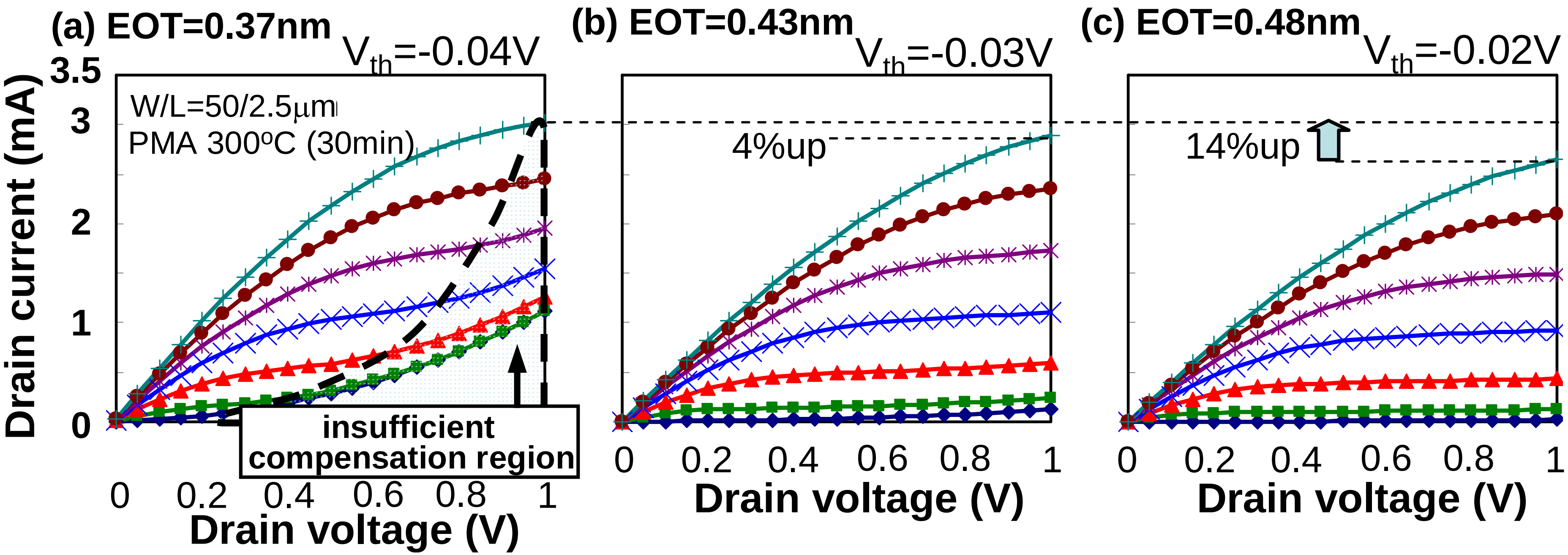
La_2O_3 + Si + nO_2

→ La_2SiO_5, $La_2Si_2O_7$,

$La_{9.33}Si_6O_{26}$, $La_{10}(SiO_4)_6O_3$, etc.

La_2O_3 can achieve direct contact of high-k/Si

EOT<0.5nm with Gain in Drive Current

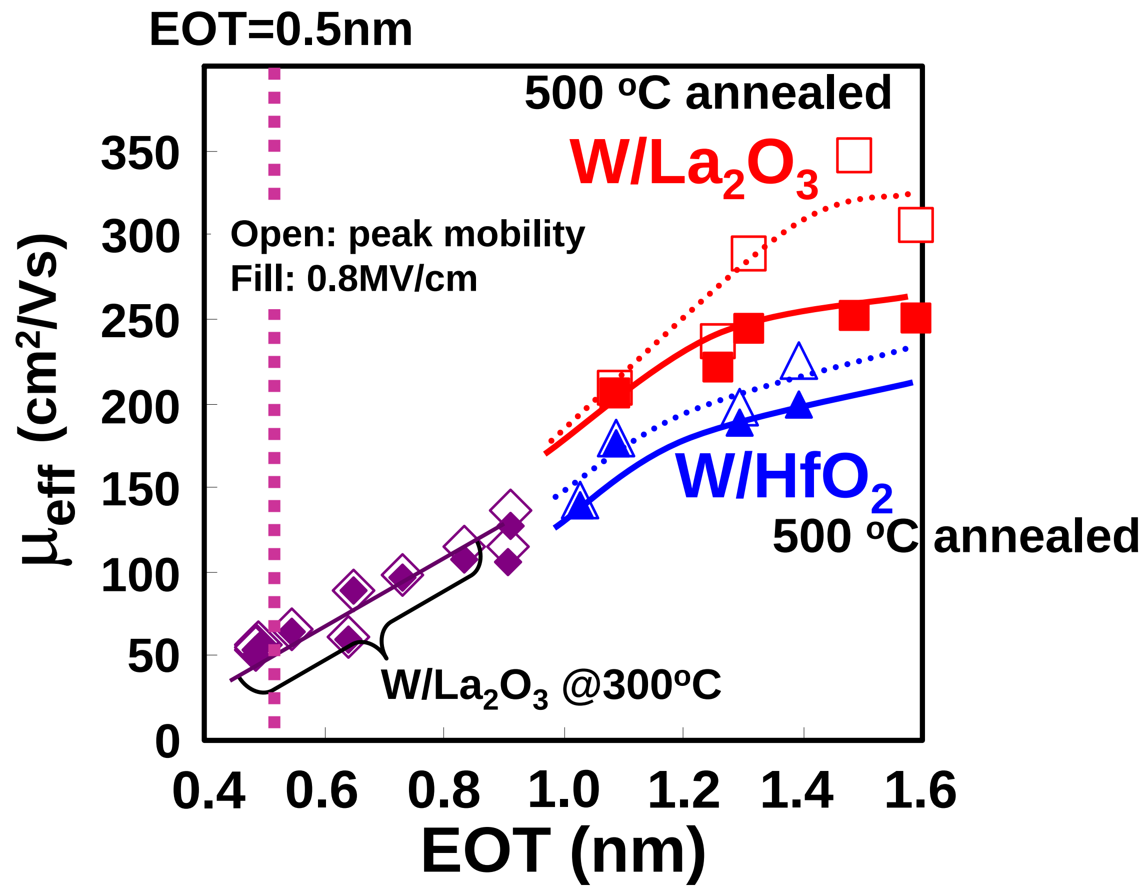


14% of I_d increase is observed even at saturation region

⇩

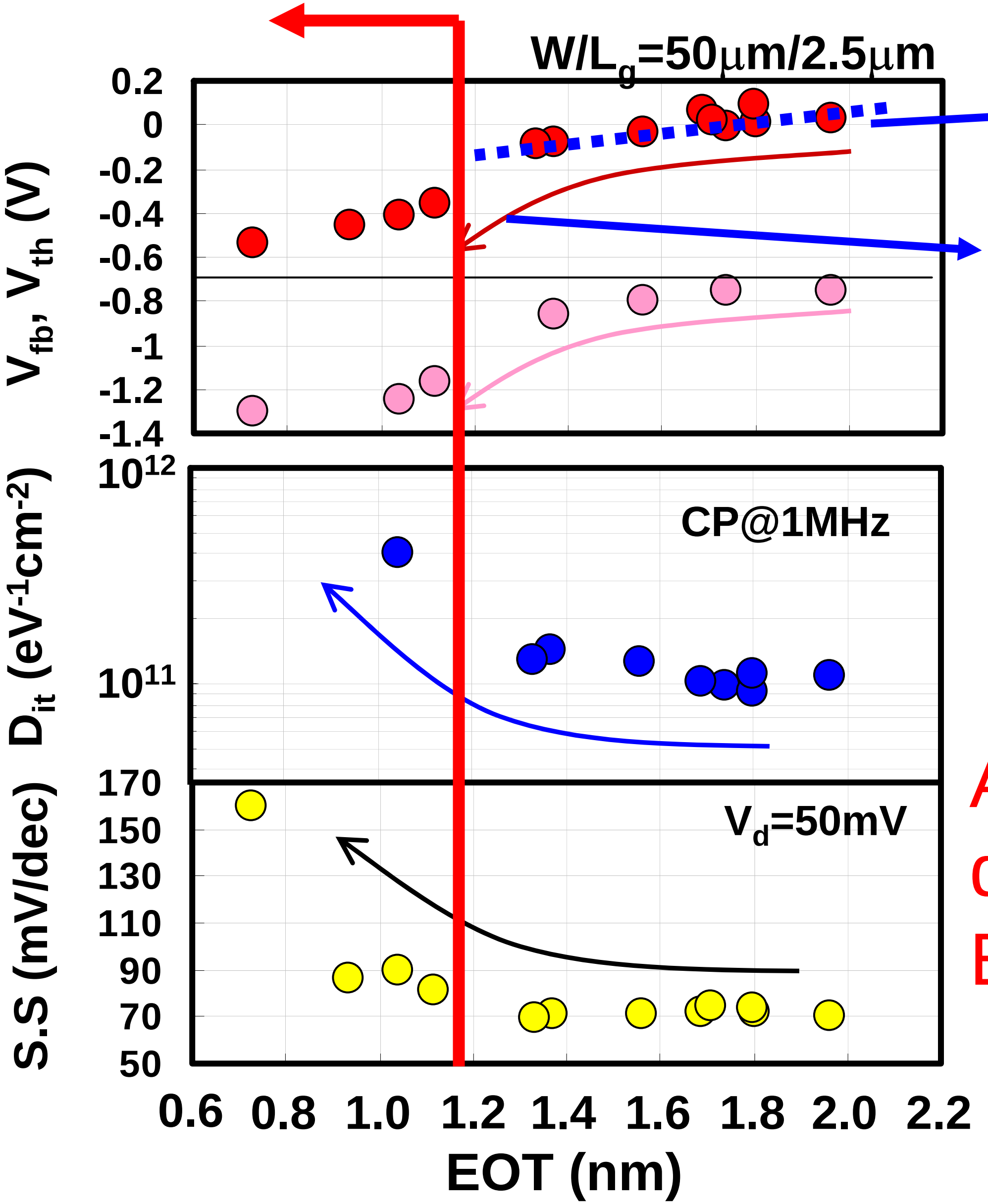
EOT below 0.4nm is still useful for scaling

μ_{eff} of W/La_2O_3 and W/HfO_2 nFET on EOT



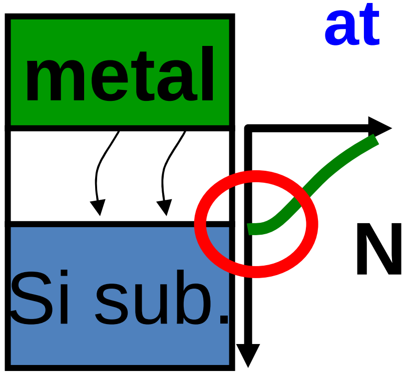
- W/La_2O_3 exhibits higher μ_{eff} than W/HfO_2
- μ_{eff} start degrades below EOT=1.4nm

FET characteristics of W/La_2O_3 on EOT



N_{fix}=7x10^{12} cm^{-2}

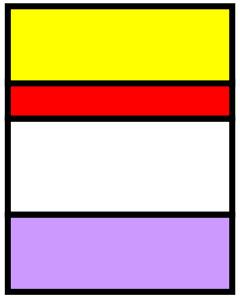
Aggressive N_{fix} generation at EOT<1.2nm



N_{fix} and D_{it}

All characteristics start to degrade or shift below EOT=1.4nm

Gate Metal Induced Defects Compensation

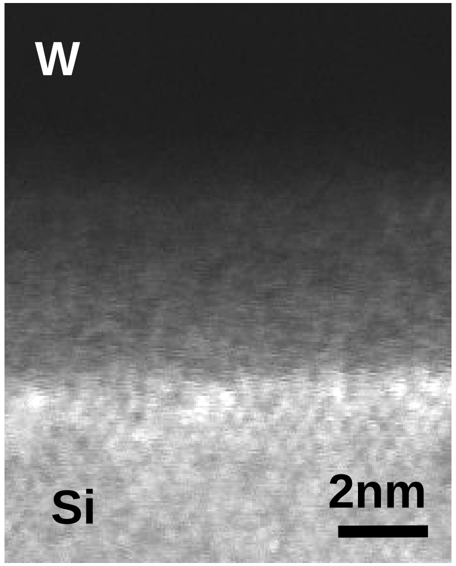


Metal Gate

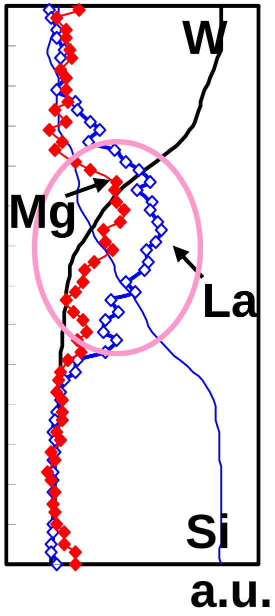
MgO

La2O3

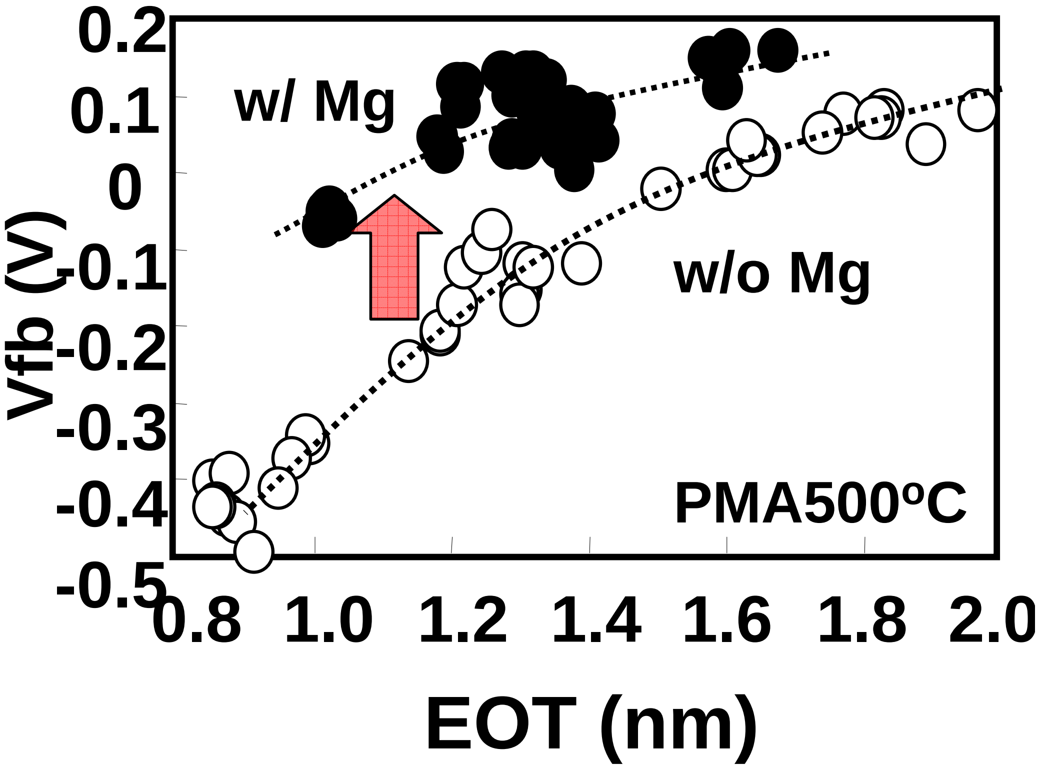
Si



TEM

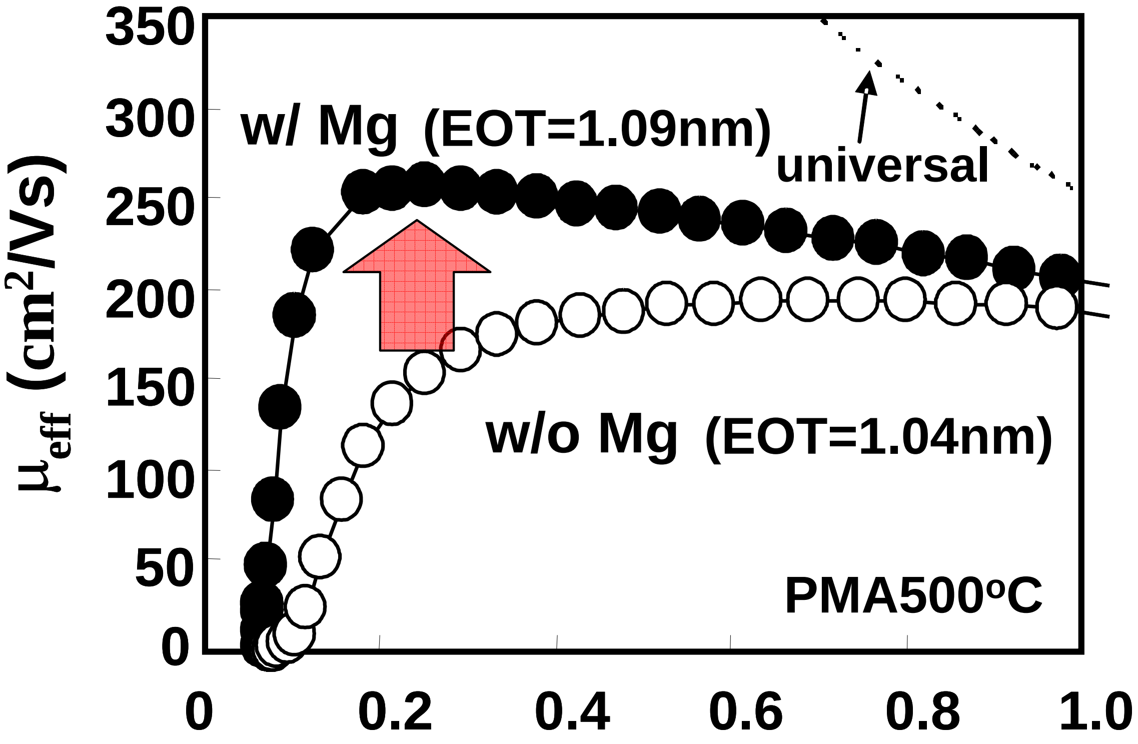


EDX



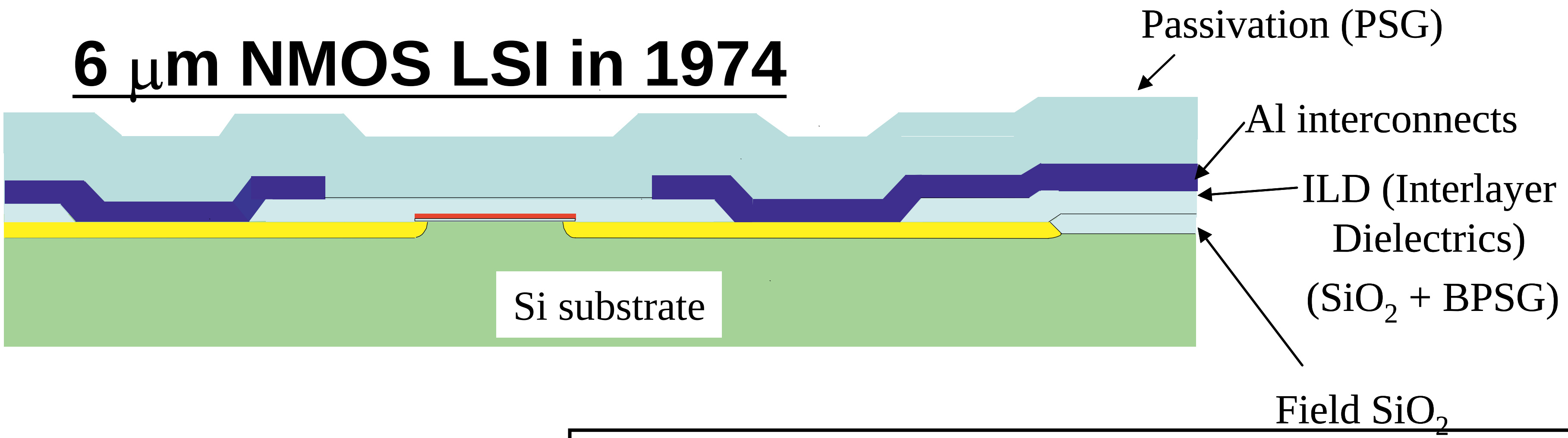
Suppression of aggressive shift in V_{fb}

Mobility Improvement with Mg Incorporation

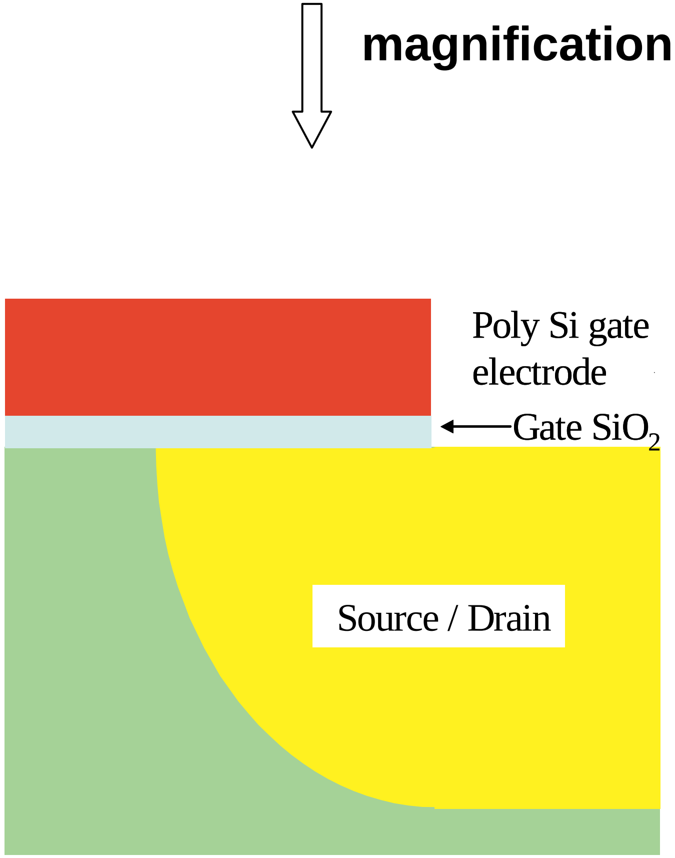


Recovery of μ_{eff} mainly at low E_{eff}

6 μm NMOS LSI in 1974



magnification



Layers

1. Si substrate
2. Field oxide
3. Gate oxide
4. Poly Si
5. S/D
6. Interlayer
7. Aluminum
8. Passivation

Materials

1. Si
2. SiO_2
3. BPSG
4. Al
5. PSG

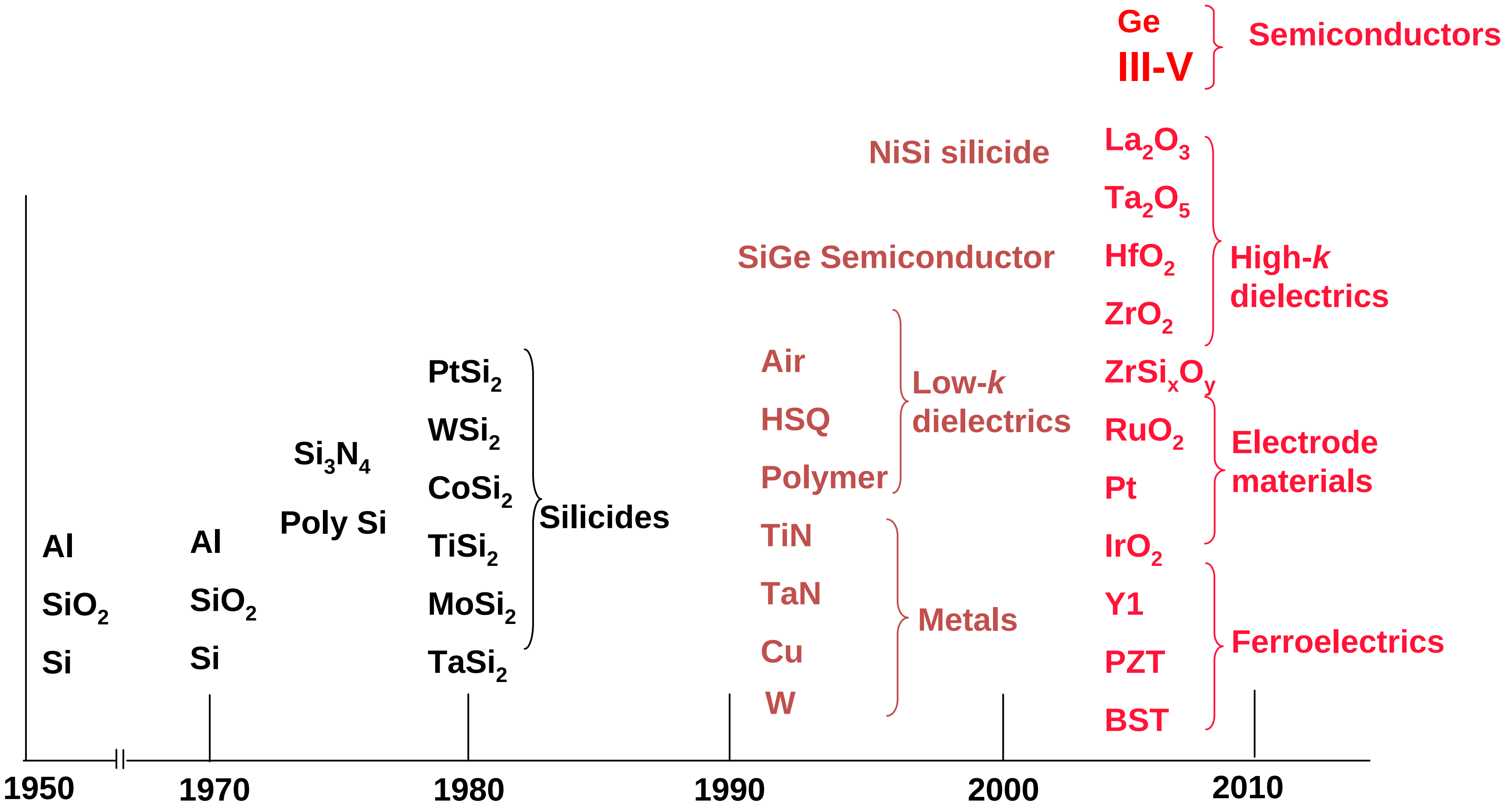
Atoms

1. **Si**
2. **O**
3. **P**
4. **B**
5. **Al**

(H, N, Cl)

New materials

Just examples!
Many other candidates



Al
SiO_2
Si

Al
SiO_2
Si

Si_3N_4
Poly Si

$PtSi_2$
WSi_2
$CoSi_2$
$TiSi_2$
$MoSi_2$
$TaSi_2$
Silicides

NiSi silicide
SiGe Semiconductor

Air
HSQ
Polymer
Low-*k* dielectrics

TiN
TaN
Cu
W
Metals

Ge
III-V
Semiconductors

La_2O_3
Ta_2O_5
HfO_2
ZrO_2
High-*k* dielectrics

$ZrSi_xO_y$
RuO_2
Pt
IrO_2
Electrode materials

Y1
PZT
BST
Ferroelectrics

Y. Nishi, Si Nano Workshop, 2006,

(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)

1970’s

Toshiba Corporation

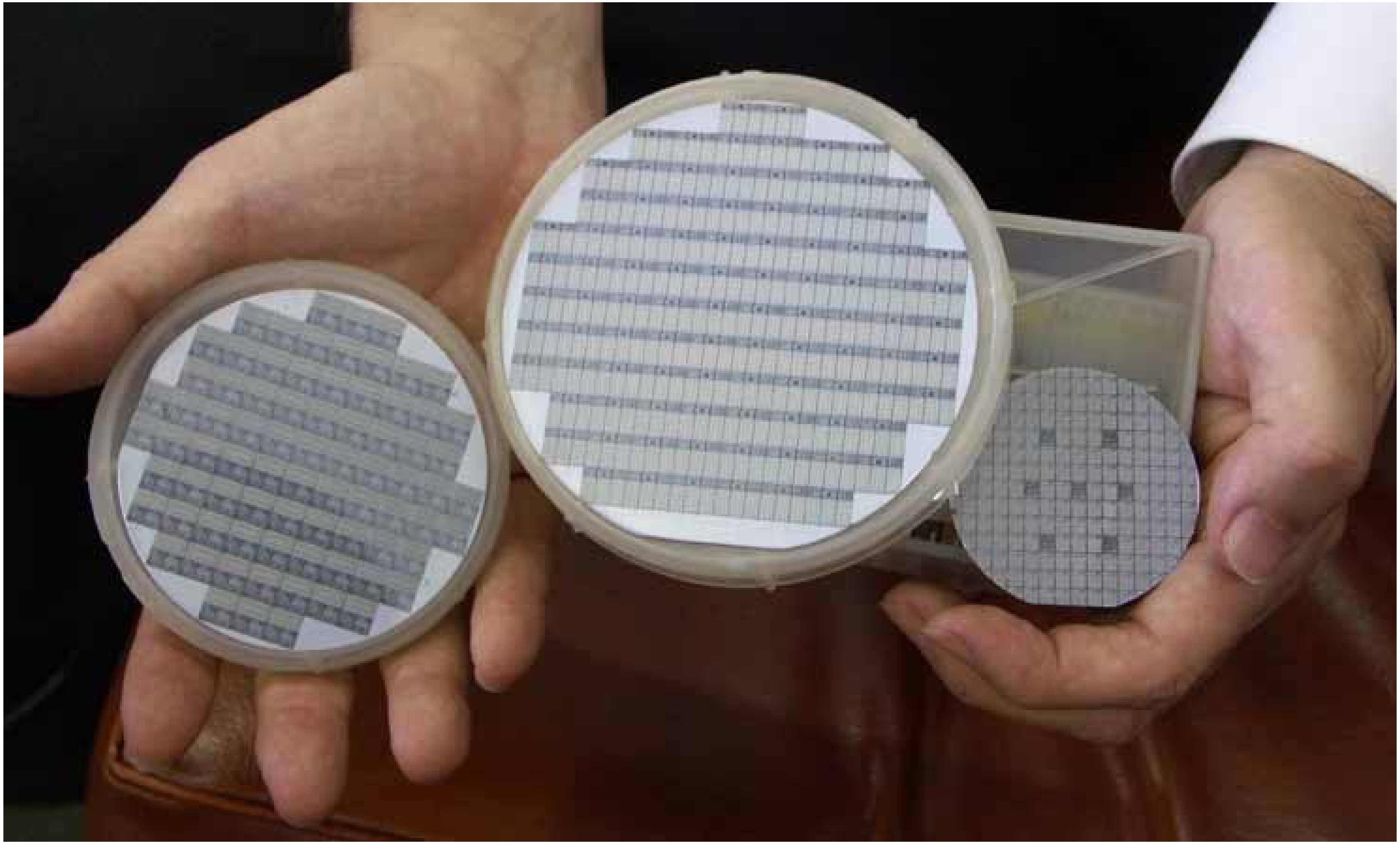
Now

300 mm Fab TSMC

Toshiba Oita Works

300 mm Super clean room in Tsukuba,Selete

In a future
No person is necessary!



64k DRAM
3 inch
wafer

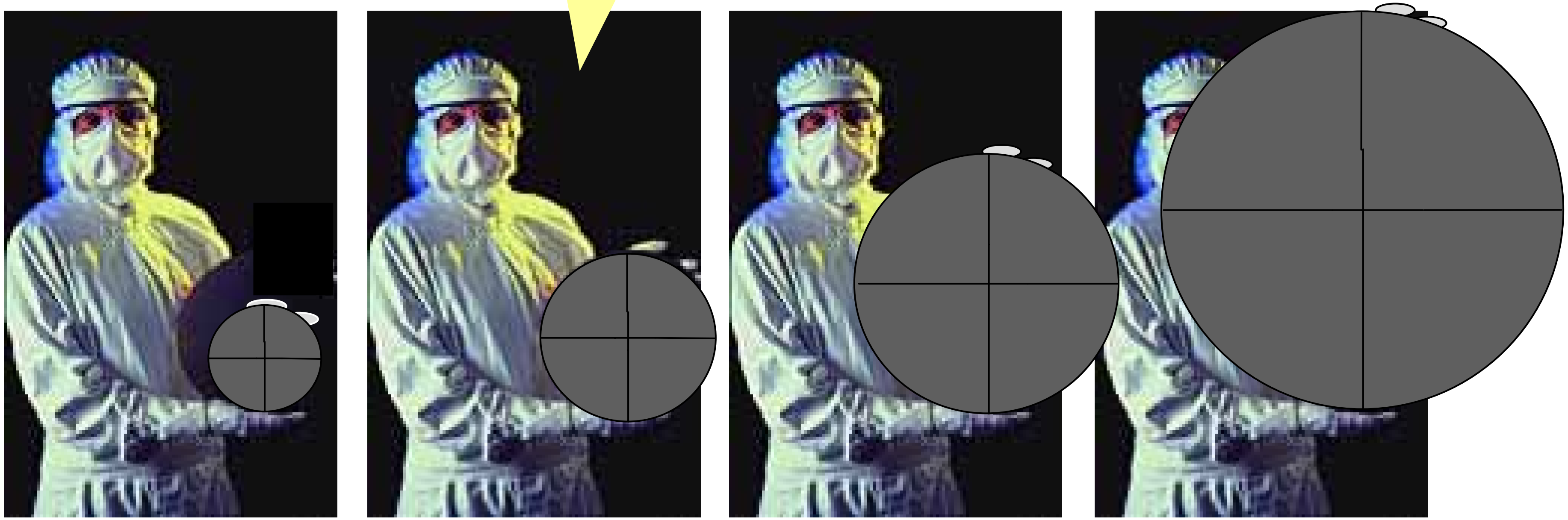
64k DRAM
4 inch wafer
1980

1k SRAM
2 inch wafer
1974

When do we start planning for next wafer size transition?

We are here

When does this happen?



200mm/1990

300mm/2001

450mm/2012 ?

675mm/2021 ?

(125/150mm - 1981)

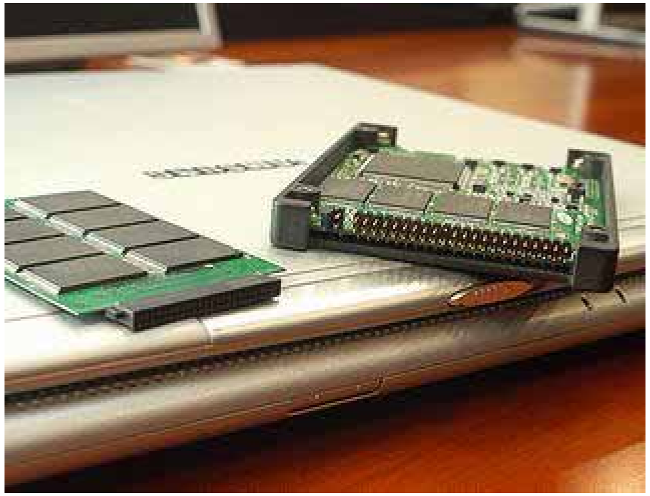
9 yrs + 2 yrs delay*

9 yrs? + 2 yrs delay?

9 yrs + ?yrs delay

Now: After 50 Years from the 1st single MOSFETs

64Gbit, 32 Gb and 16Gb NAND, SAMSUNG

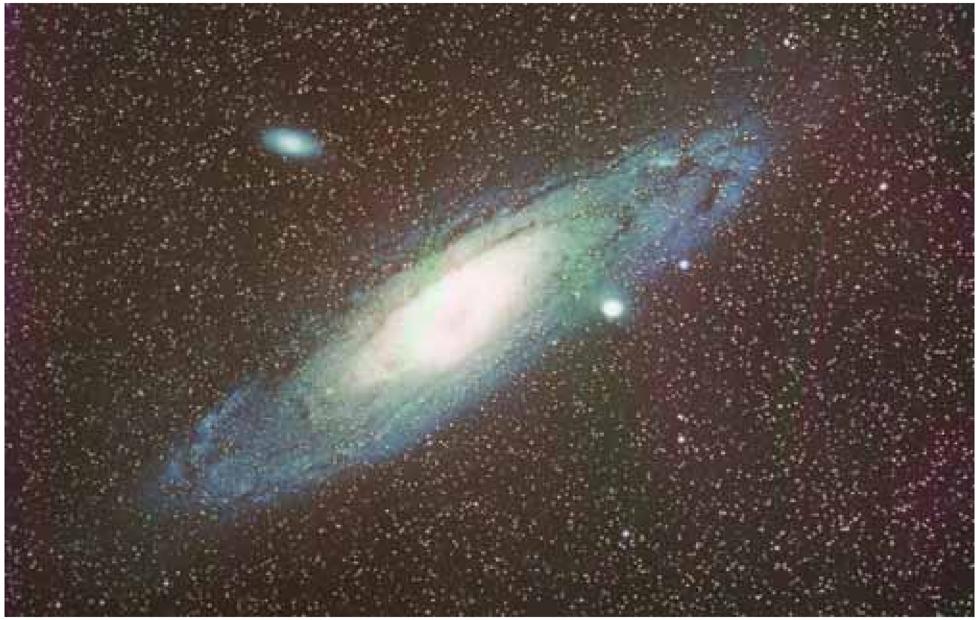


Already 64 Gbit:

larger than that of world population
comparable for the numbers of neurons
in human brain

Samsung announced 256 Gbit will be produced

256Gbit: larger than those of # of stars in galaxies



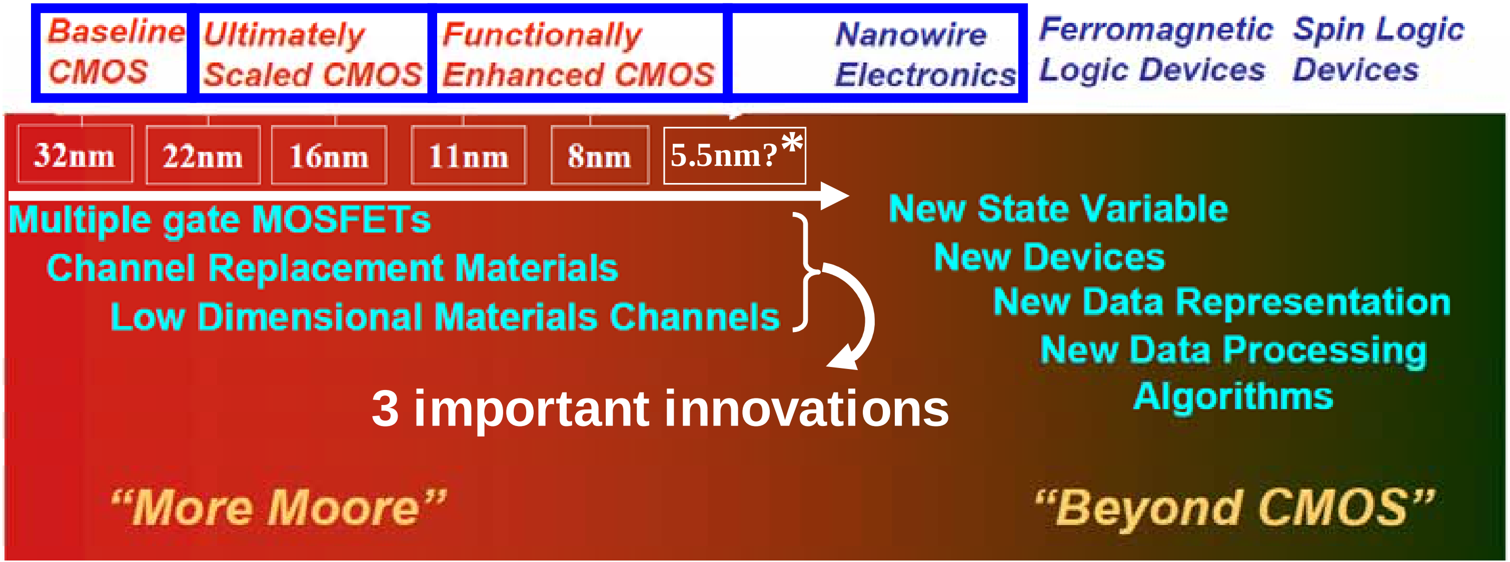
-There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

-Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

-Two candidates have emerged for R & D

1. Nanowire/tube MOSFETs
2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.

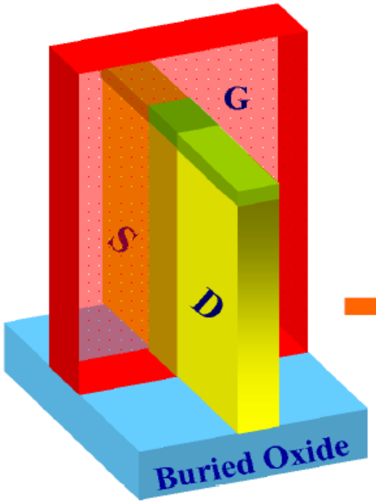


ITRS figure edited by Iwai

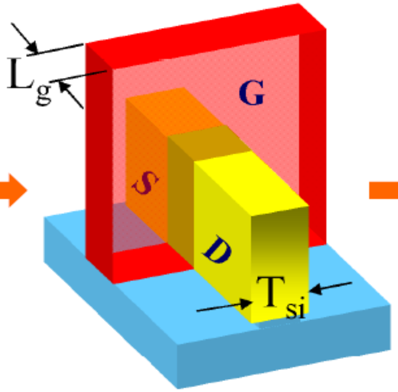
Source: 2008 ITRS Summer Public Conf.

***5.5nm? was added by Iwai**

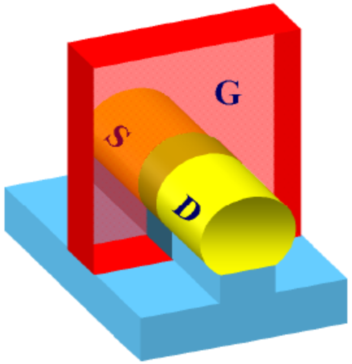
FinFET to Nanowire



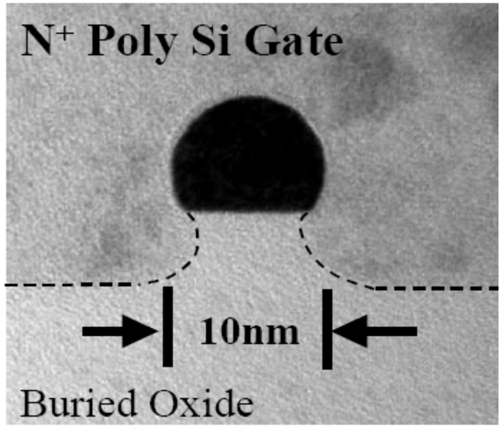
Double-Gate
FinFET
($T_{si} = {}^{2}/_{3} L_g$)

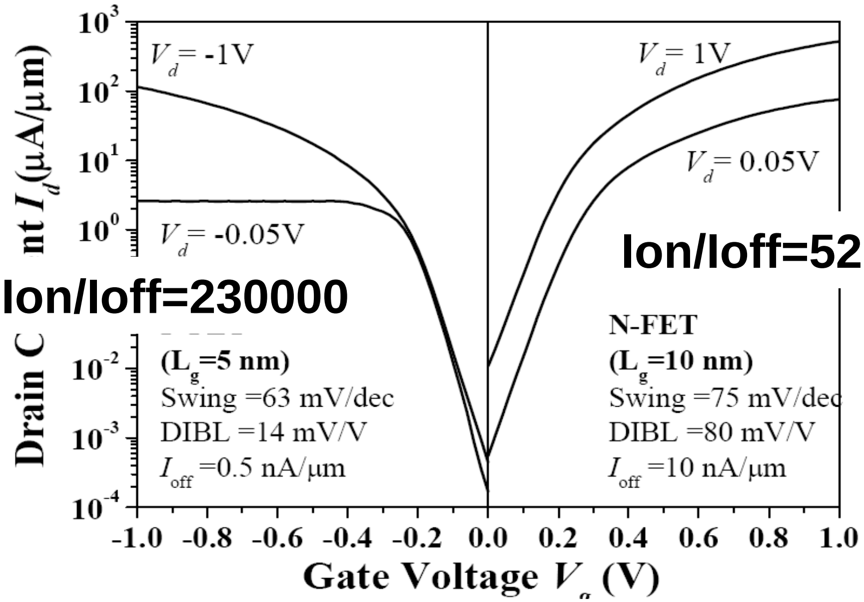


Omega
FinFET
($T_{si} = L_g$)



Nanowire
FinFET
($T_{si} = 2L_g$)





Ion/Ioff=52200

Ion/Ioff=230000

Channel conductance is well controlled by Gate even at L=5nm

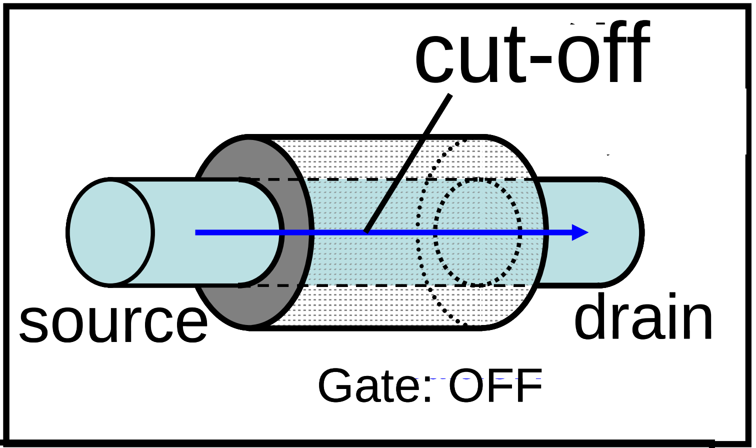
F.-L.Yang, VLSI2004

Si nanowire FET as a strong candidate after CMOS limitation

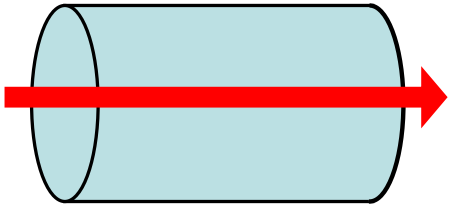
1. Compatibility with current CMOS process

2. Good controllability of I_{OFF}

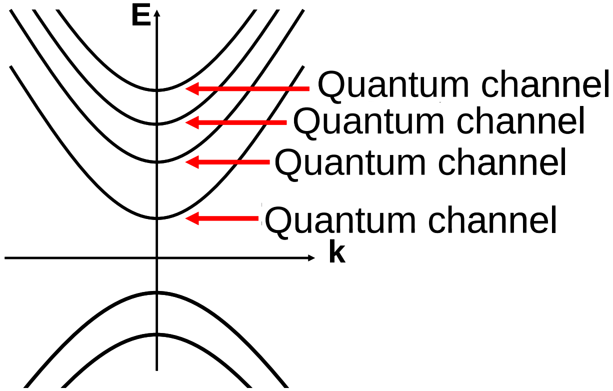
3. High drive current



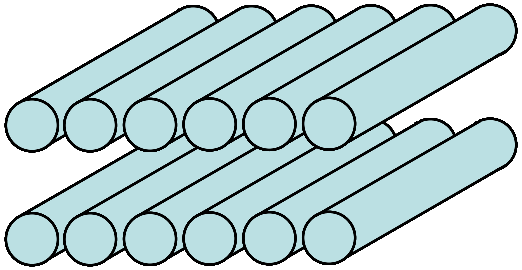
1D ballistic conduction



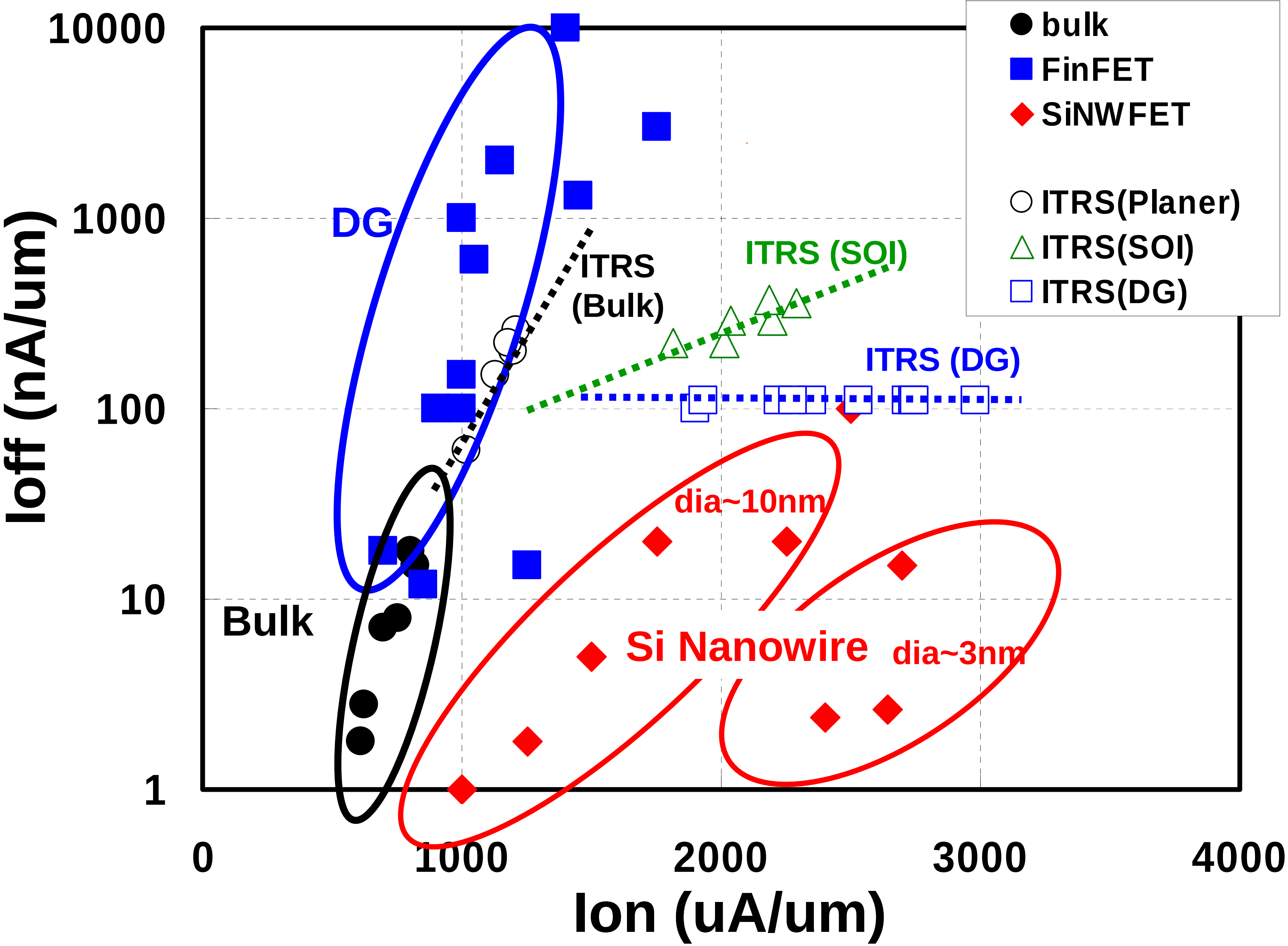
Multi quantum Channel



High integration of wires

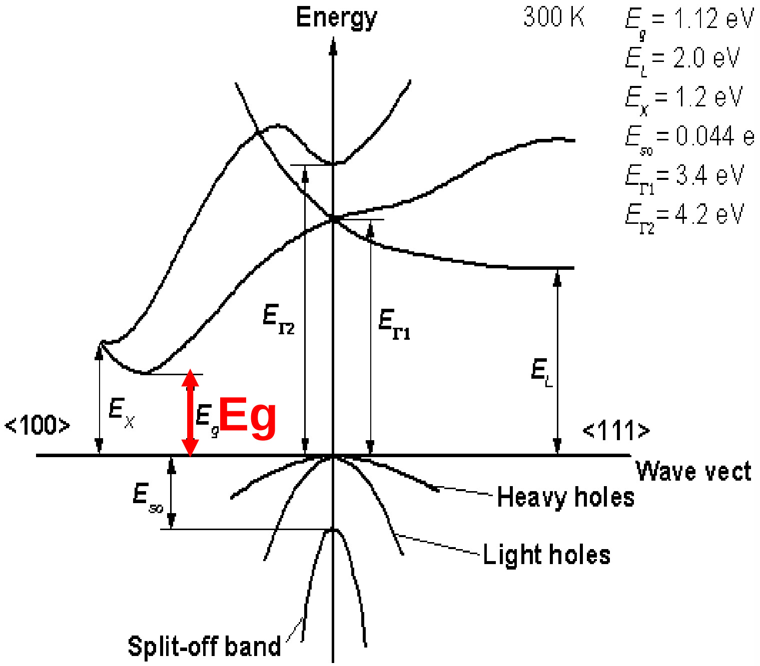


Off Current

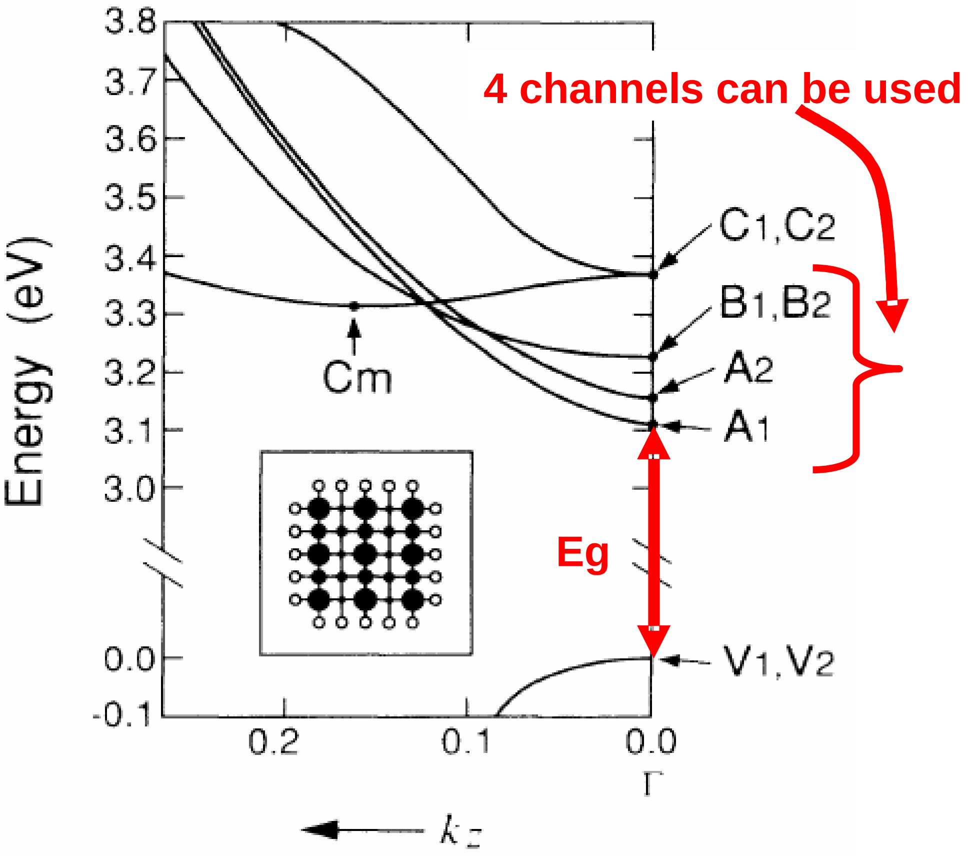

10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
● bulk
■ FinFET
◆ SiNWFET
○ ITRS(Planer)
△ ITRS(SOI)
□ ITRS(DG)
DG
Bulk
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Si Nanowire
dia~3nm

Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



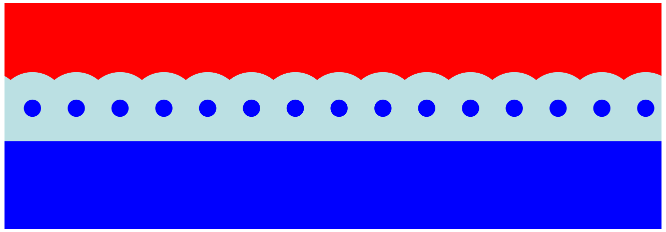
Energy band of Bulk Si



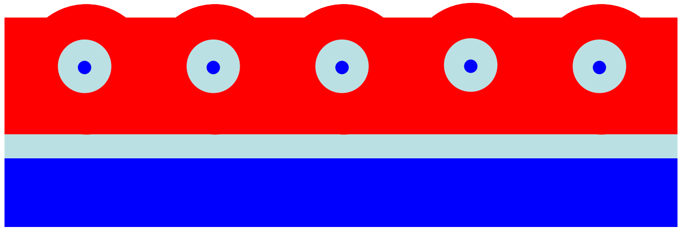
Energy band of 3 x 3 Si wire

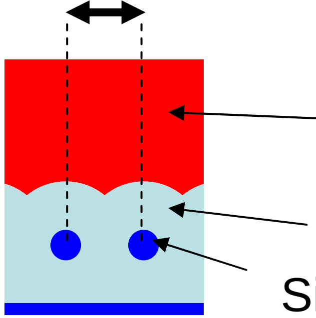
Maximum number of wires per 1 μm

Front gate type MOS 165 wires /μm



Surrounded gate type MOS 33 wires/μm



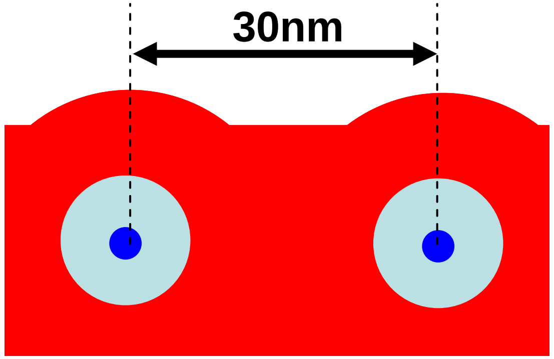


6nm pitch
By nano-imprint method

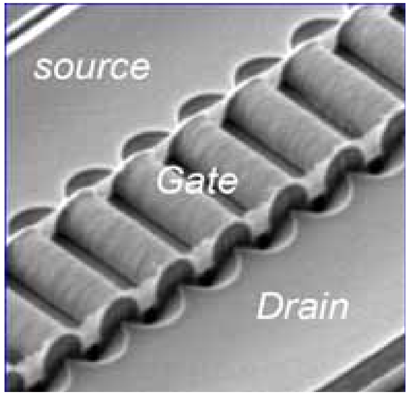
Metal gate electrode(10nm)

High-k gate insulator (4nm)

Si Nano wire (Diameter 2nm)

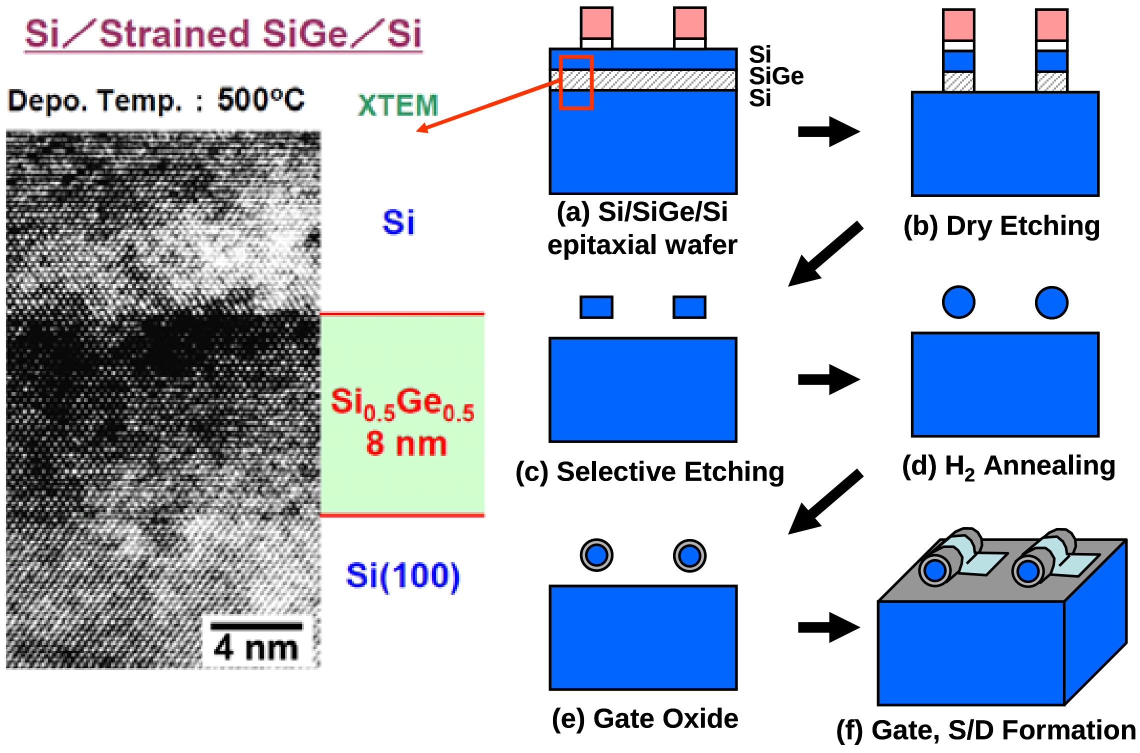


30nm pitch:
EUV lithograpy



Surrounded gate MOS

Increase the number of wires towards vertical dimension



(a) Si/SiGe/Si epitaxial wafer

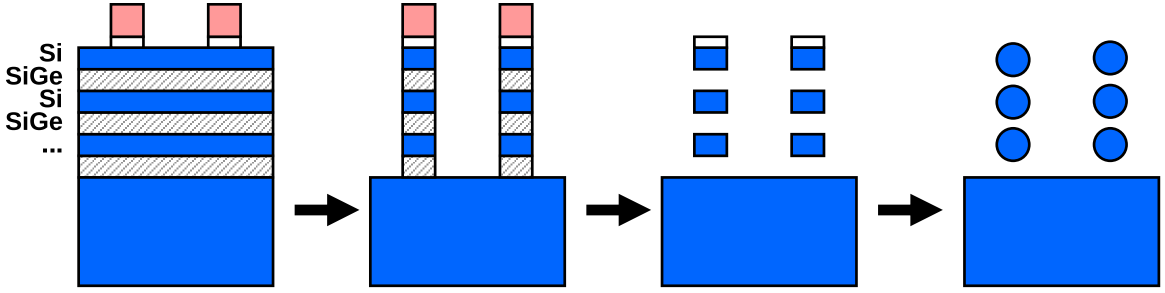
(b) Dry Etching

(c) Selective Etching

(d) H_2 Annealing

(e) Gate Oxide

(f) Gate, S/D Formation



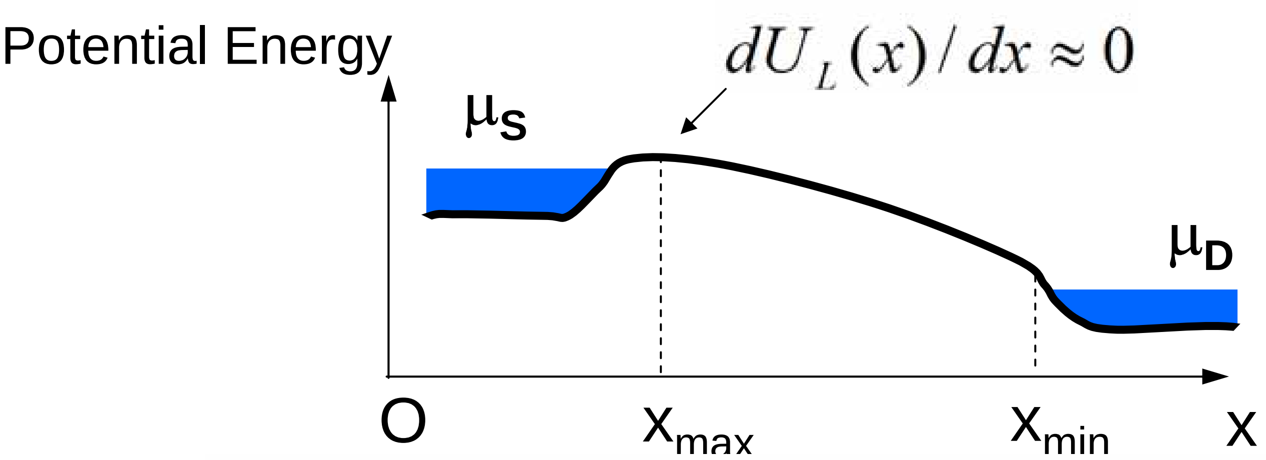
Si/SiGe multi stacked wafer

Dry Etching

Selective Etching

H_2 Annealing

Landauer Formalism for Ballistic FET

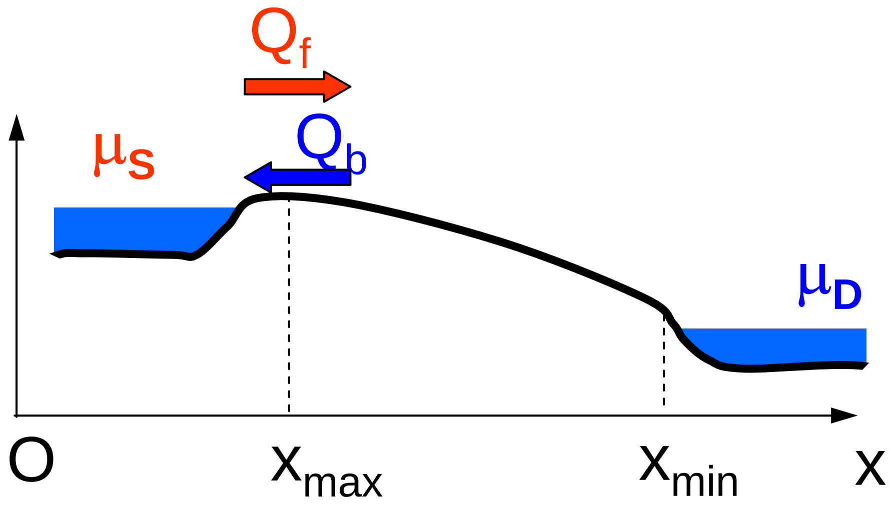


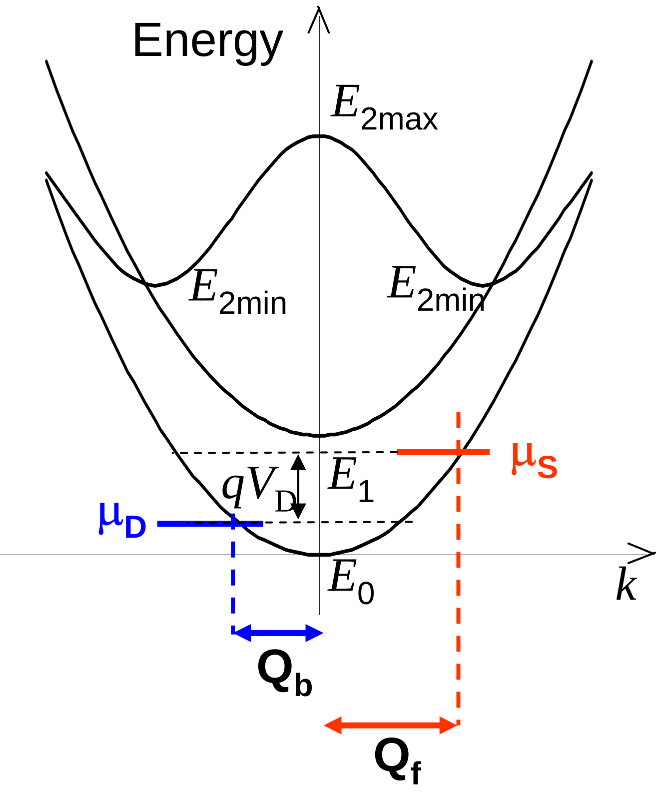
$$I_D = \frac{q}{\pi\hbar}\sum_i \int \left[f(E,\mu_S) - f(E,\mu_D) \right] T_i(E)\,dE$$

From x_{max} to x_{min} $T_i(E) \approx 1$

$$\boxed{I_D = G_0 \left(\frac{k_B T}{q} \right) \sum_i g_i \ln \left\{ \frac{1 + \exp\left[(\mu_S - E_{i0}) / k_B T \right]}{1 + \exp\left[(\mu_D - E_{i0}) / k_B T \right]} \right\}}$$

Carrier Density obtained from E-k Band

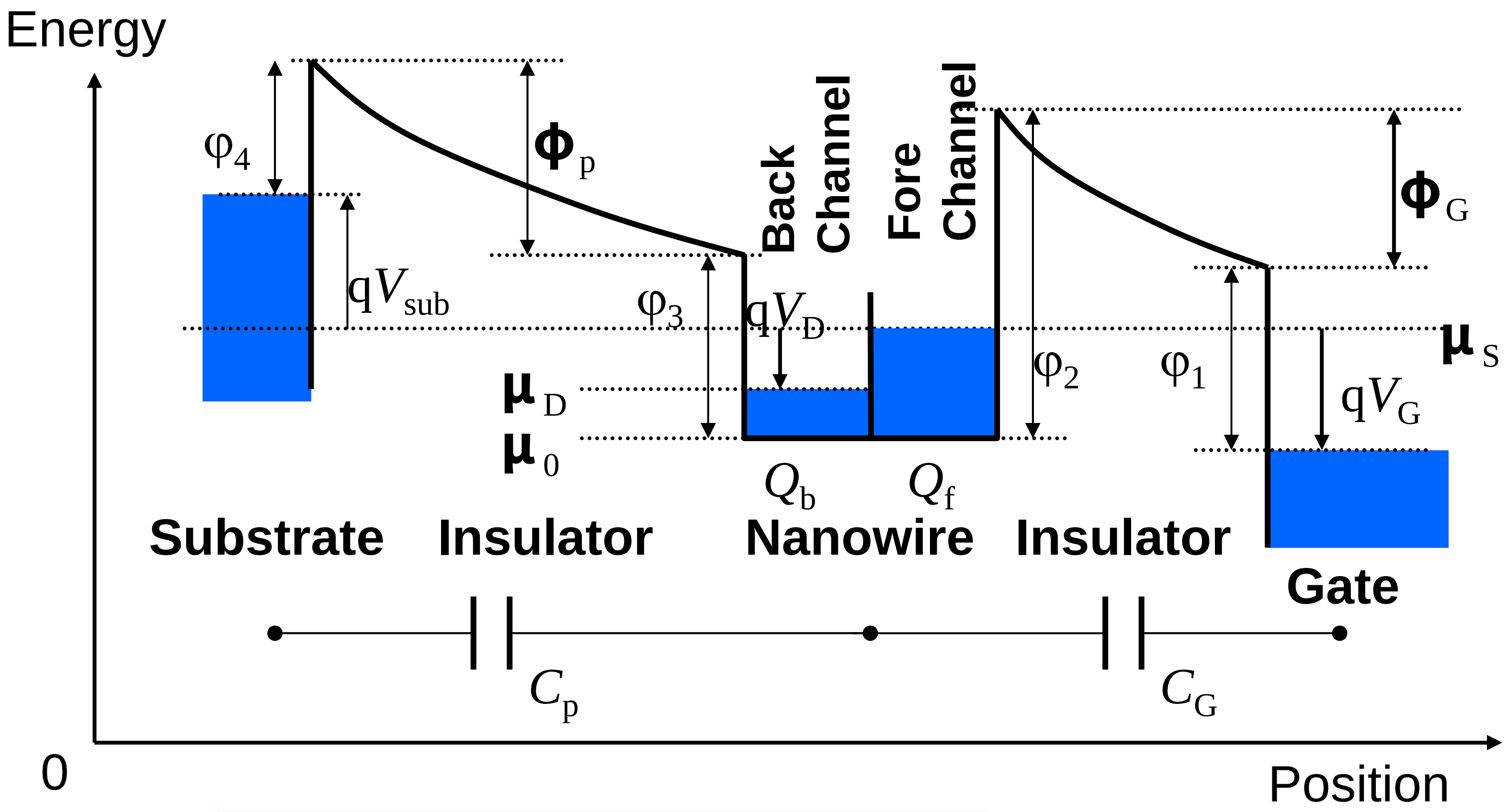




$$|Q| = |Q_f| + |Q_b|$$

$$= \frac{q}{\pi}\sum_i g_i \left[\int_{k_{i\,\min}}^{\infty} \frac{dk}{1+\exp\left\{\dfrac{E_i(k)-\mu_S}{k_B T}\right\}} + \int_{-\infty}^{k_{i\,\min}} \frac{dk}{1+\exp\left\{\dfrac{E_i(k)-\mu_D}{k_B T}\right\}} \right]$$

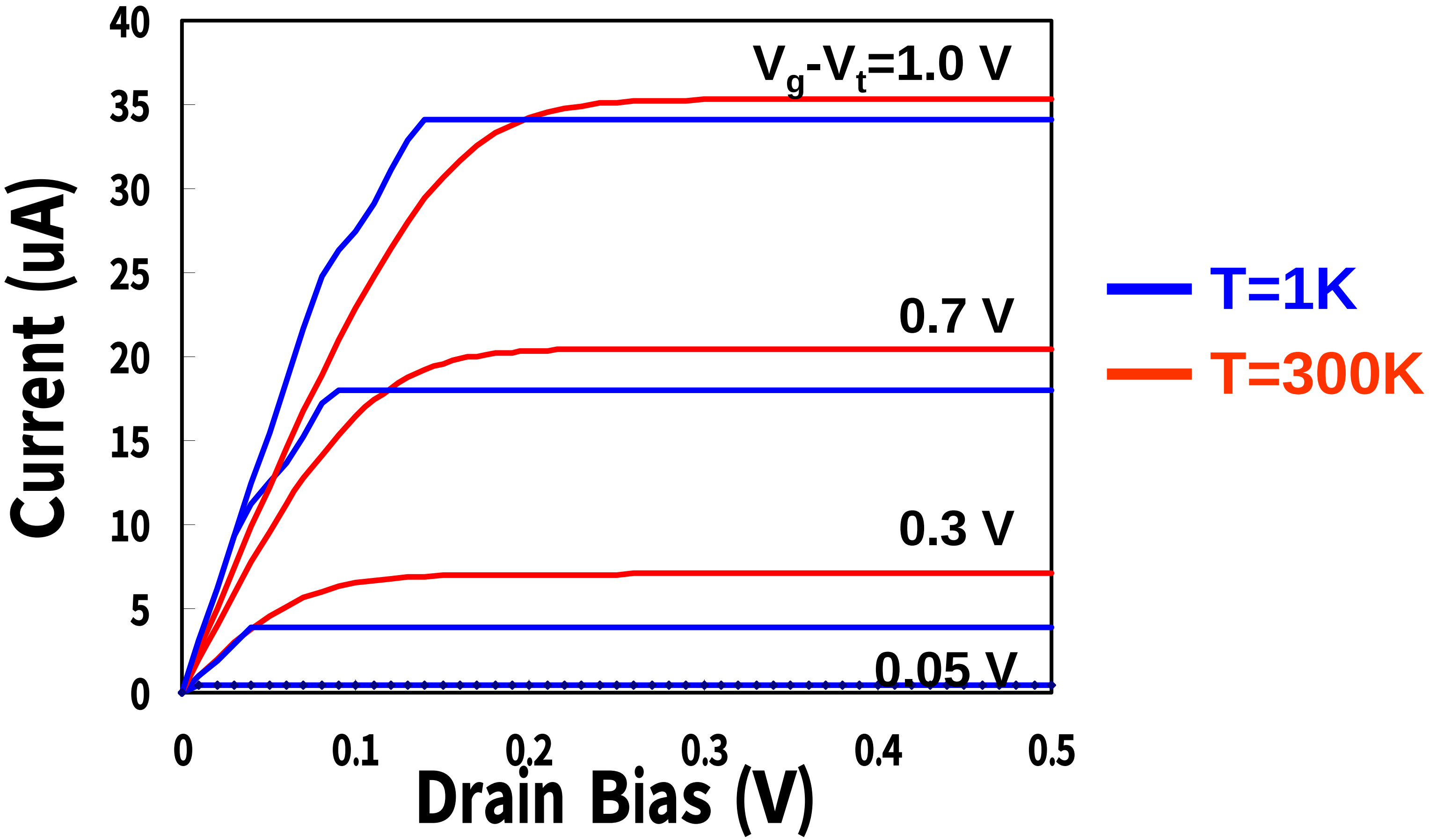
Carrier Density obtained from Band Diagram



$$\frac{|Q|}{C_G} = (V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q}$$

$$\alpha = 1 + \frac{C_P}{C_G}$$

IV Characteristics of Ballistic SiNW FET

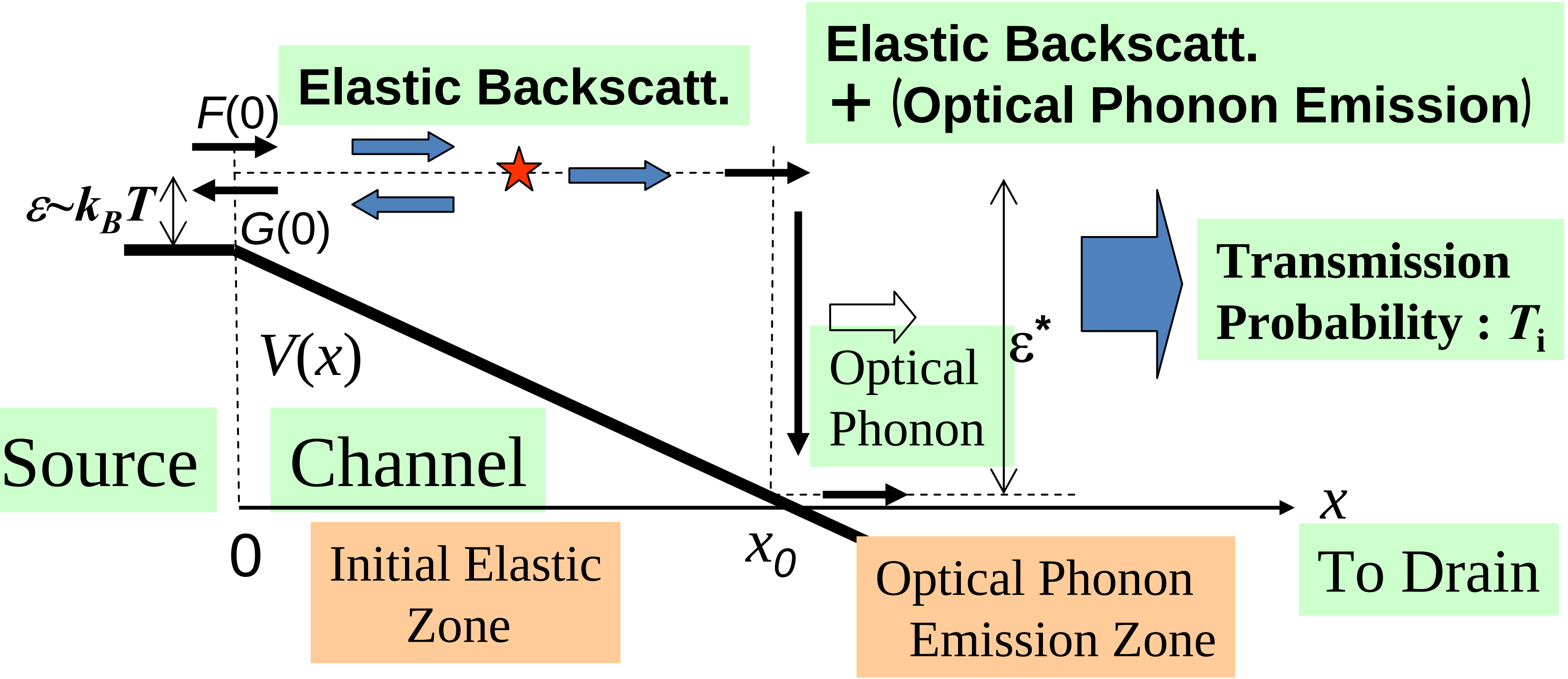


Small temperature dependency

35μA/wire for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx.： Electric Field E



Elastic Backscatt.

Elastic Backscatt.
+ (Optical Phonon Emission)

Transmission Probability : T_i

Source

Channel

To Drain

Initial Elastic Zone

Optical Phonon Emission Zone

Transmission Probability to Drain

$$T(\varepsilon) = \left.\frac{F(0)-G(0)}{F(0)}\right)_{\text{Injection from Drain}=0}$$

Résumé of the Compact Model

$$I=\frac{q}{\pi\hbar}\sum_i g_i\int\left[f(\varepsilon,\mu_s)-f(\varepsilon,\mu_D)\right]T_i\,d\varepsilon$$

$$C_G=\frac{2\pi\varepsilon_{ox}}{\ln\left\{\dfrac{\sqrt{2r+t_{ox}}+\sqrt{t_{ox}}}{\sqrt{2r+t_{ox}}-\sqrt{t_{ox}}}\right\}}.$$

Planar Gate

$$(V_G-V_t)-\alpha\frac{\mu_S-\mu_0}{q}=\frac{\left|Q_f+Q_b\right|}{C_G}.$$

$$\mu_S-\mu_D=qV_D$$

$$C_G=\frac{2\pi\varepsilon_{ox}}{\ln\left(\dfrac{r+t_{ox}}{r}\right)}.$$

GAA

(Electrostatics requirement)

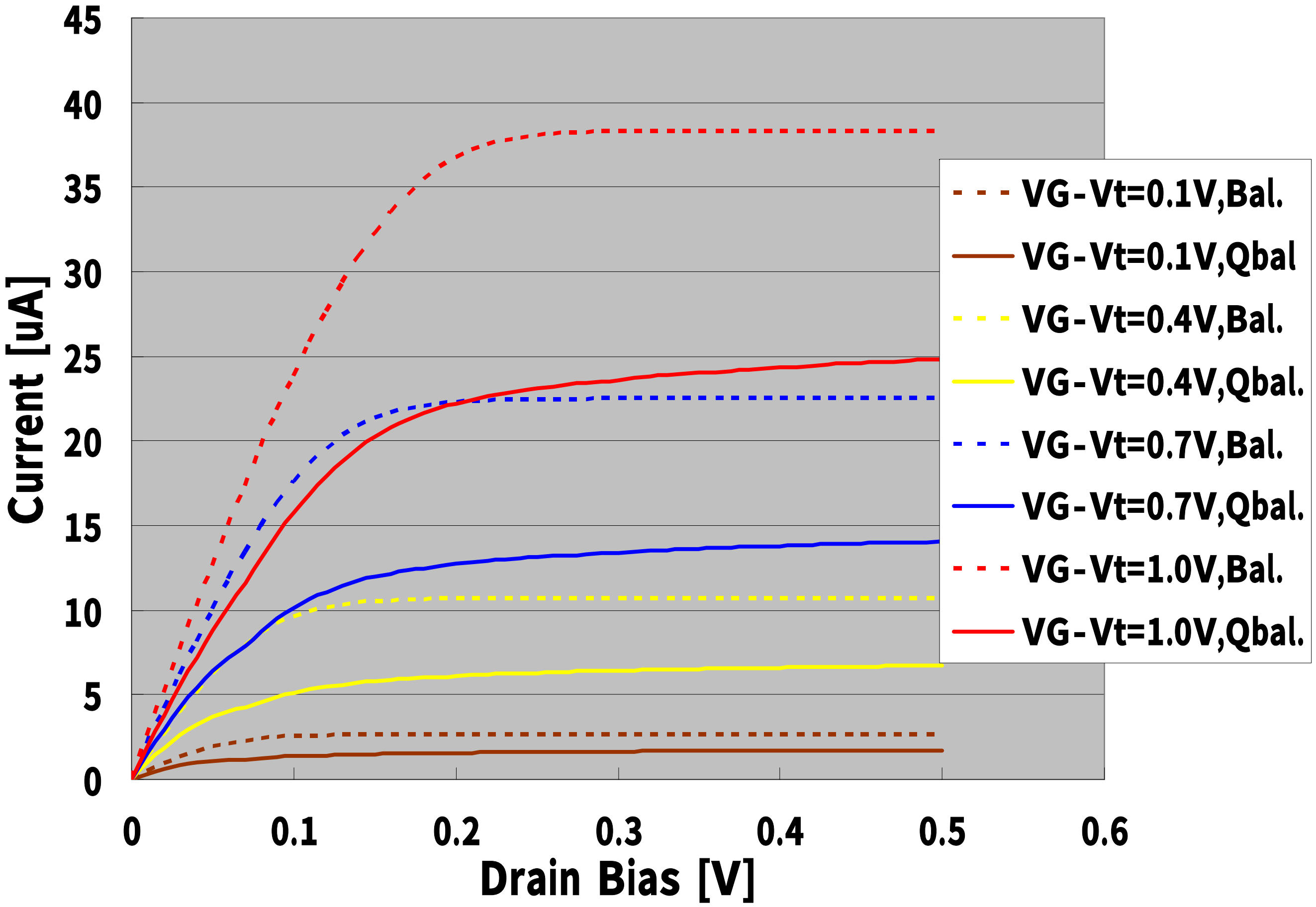
$$\left|Q_f+Q_b\right|=\frac{q}{\pi}\sum_i g_i\left[\int_{-\infty}^{\infty}\frac{dk}{1+\exp\left\{\dfrac{\varepsilon_i(k)-\mu_S}{k_BT}\right\}}-\int_{-\infty}^{0}\left\{\frac{1}{1+\exp\left\{\dfrac{\varepsilon_i(k)-\mu_S}{k_BT}\right\}}-\frac{1}{1+\exp\left\{\dfrac{\varepsilon_i(k)-\mu_D}{k_BT}\right\}}\right\}T_i(\varepsilon_i(k))\,dk\right]$$

$$T(\varepsilon)=\frac{\sqrt{2D_0qE}}{\left(\sqrt{B_0+D_0}+\sqrt{D_0}\right)qE+\sqrt{2mD_0}B_0\ln\left(\dfrac{qEx_0+\varepsilon}{\varepsilon}\right)}$$

(Carrier distribution
in Subbands)

Unknowns are I_D, $(\mu_S-\mu_0)$, $(\mu_D-\mu_0)$, および (Q_f+Q_b)

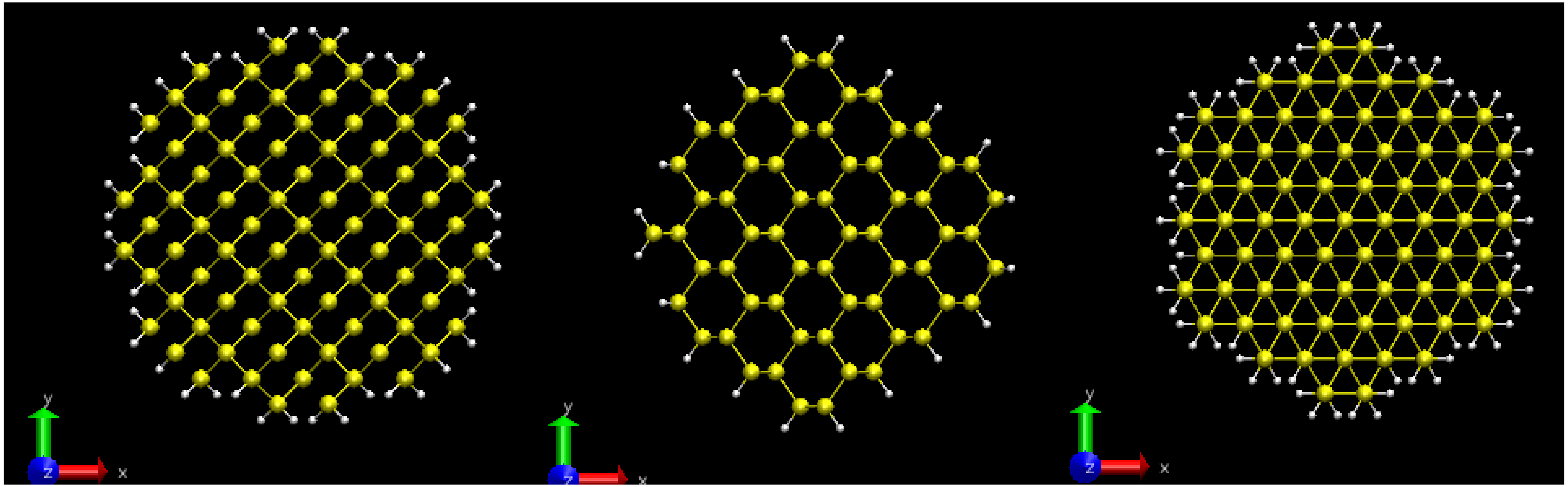
I-V_D Characteritics (RT)



- ☐ **Electric current ２０～25 μA**
- ☐ **No satruration at Large V_D**

Cross section of Si NW

First principal calculation, TAPP

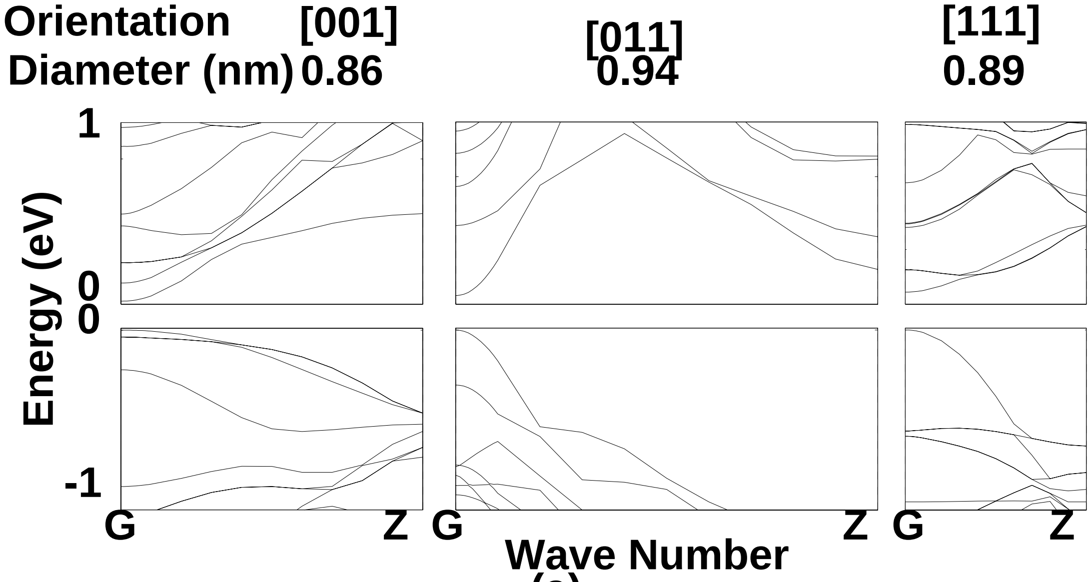


D=1.96nm
[001]

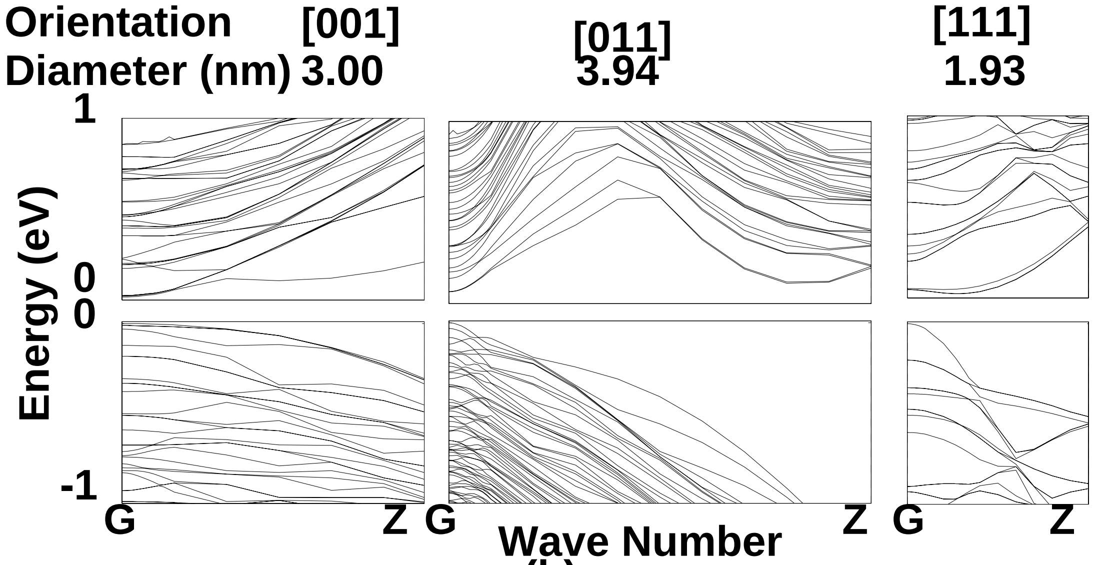
D=1.94nm
[011]

D=1.93nm
[111]

Si nanowire FET with 1D Transport



(a)



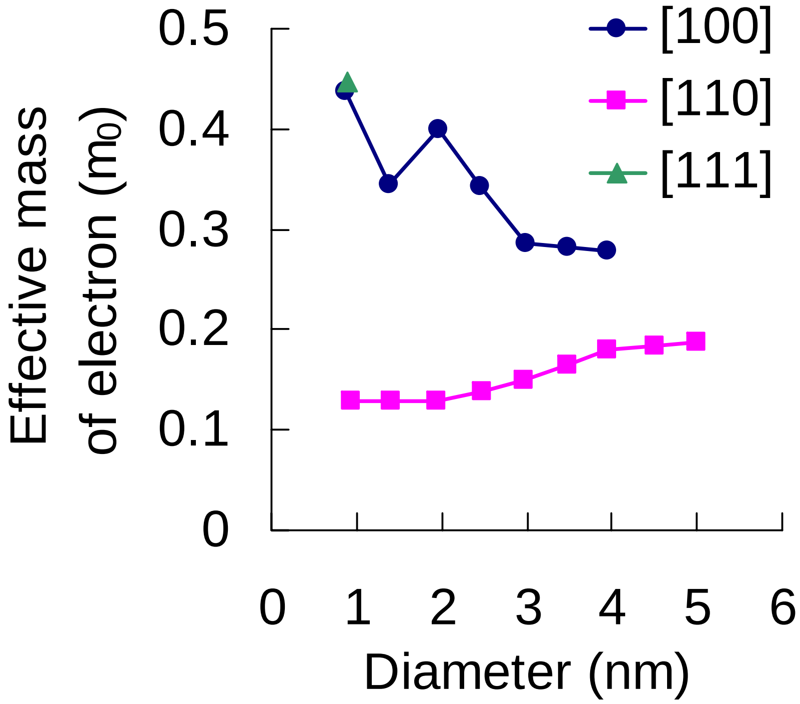
(b)

Small mass with [011]

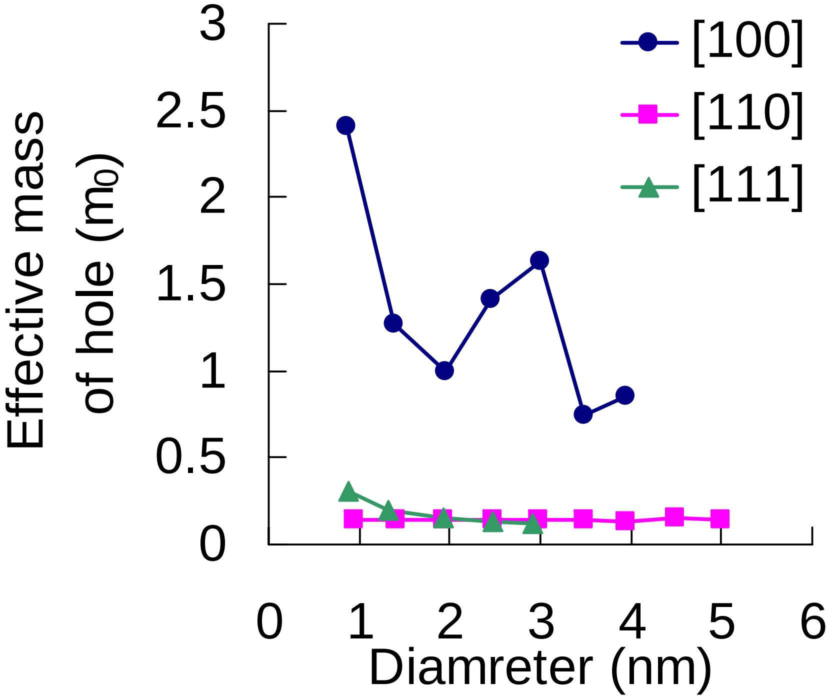
Large number of quantum channels with [001]

Effective mass

Electron



Hole



Lighter effective masses make conductance higher

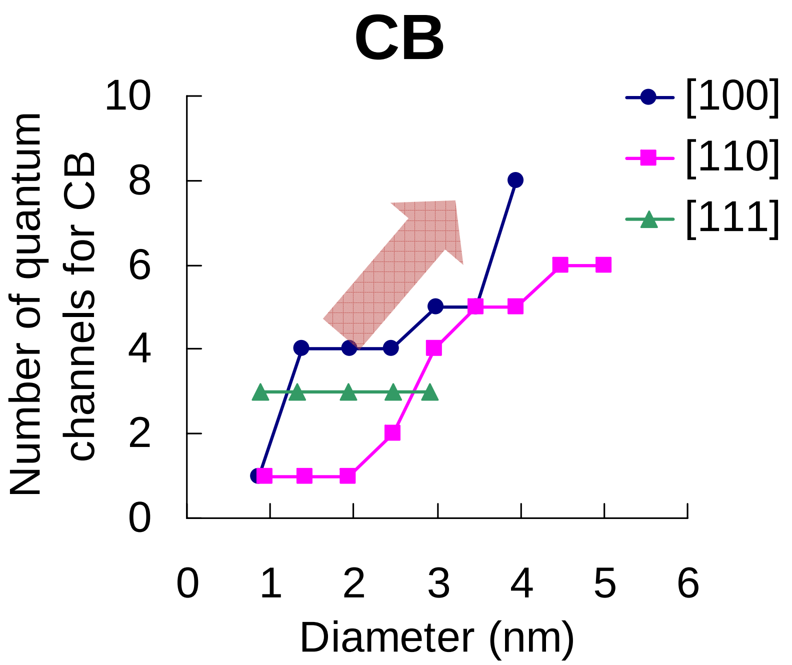
→ lighter

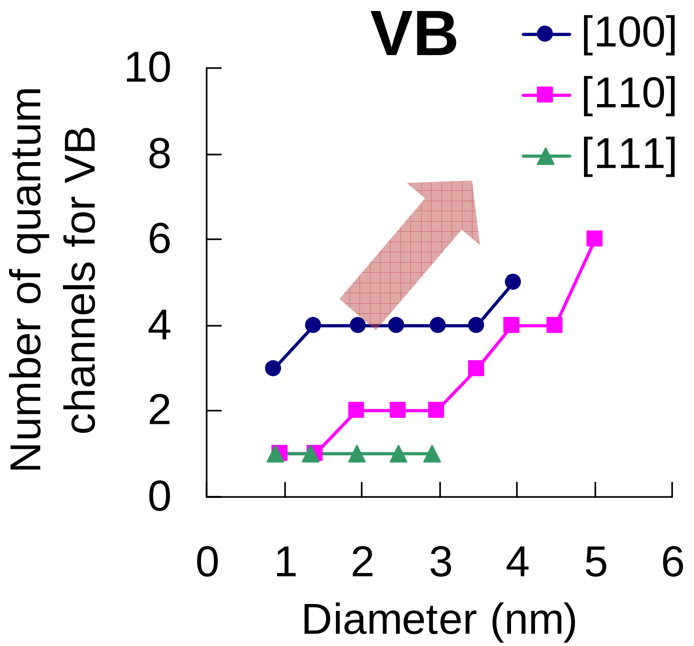
Electron [100] [111] > [110]

Hole [100] >> [110] [111]

Numbers of Quantum Channels

Quantum channels denote subband edges within 0.1 eV from CBM and VBM





Quantum channels increase in large wire

Quantum channel ➡ Passage for transport

→ **more**

CB [110] [111] **<** [100]

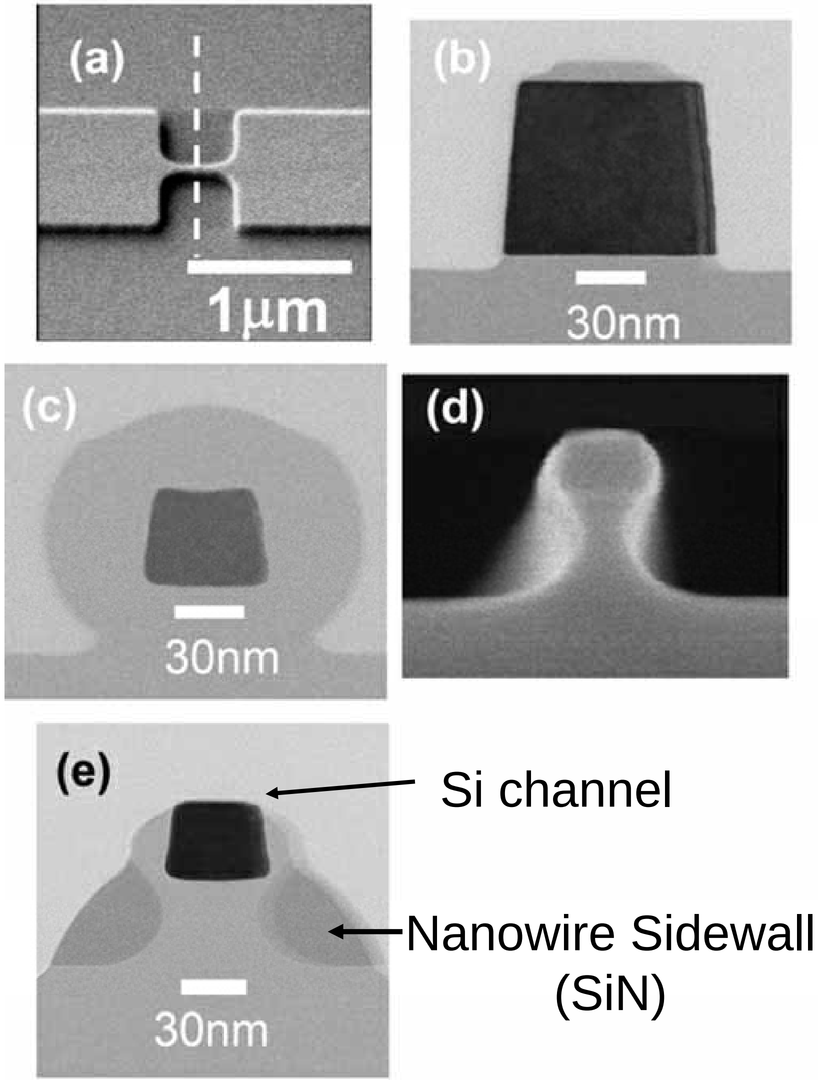
VB [111] **<** [110] **<** [100]

SiNW FET Fabrication

Brief process flow of Si Nanowire FET

- S/D&Fin Patterining
  (ArF Lithography and RIE Etching)
- Sacrificial Oxidation & Oxide Removal
  (not completely released from BOX layer)
- Nanowire Sidewall Formation (oxide support protector)
- Gate Oxidation (5nm) & Poly-Si Deposition (75nm)
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process

(a) Fin structure formed on BOX layer. (b)XTEM image of fin shown in (a) (c) XTEM image after sacrificial oxidation (d) Cross sectional SEM image after partial removal of sacrificial oxide (e) XTEM after nanowire sidewall formation

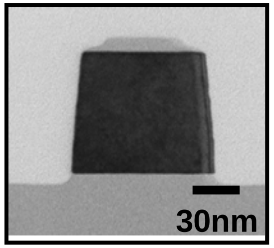


Si channel

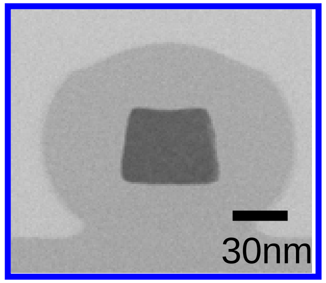
Nanowire Sidewall
(SiN)

SiNW FET Fabrication

S/D & Fin Patterning

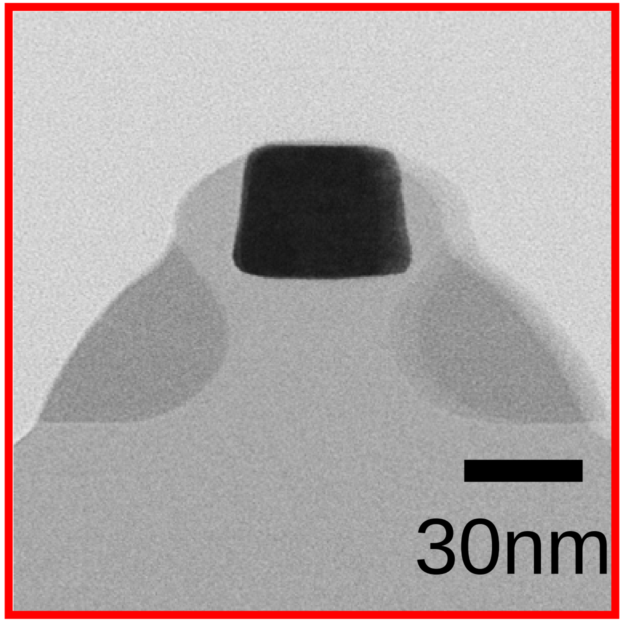


Sacrificial Oxidation



Oixde etch back

SiN sidewall support formation



Gate Oxidation & Poly-Si Deposition

Gate Lithography & RIE Etching

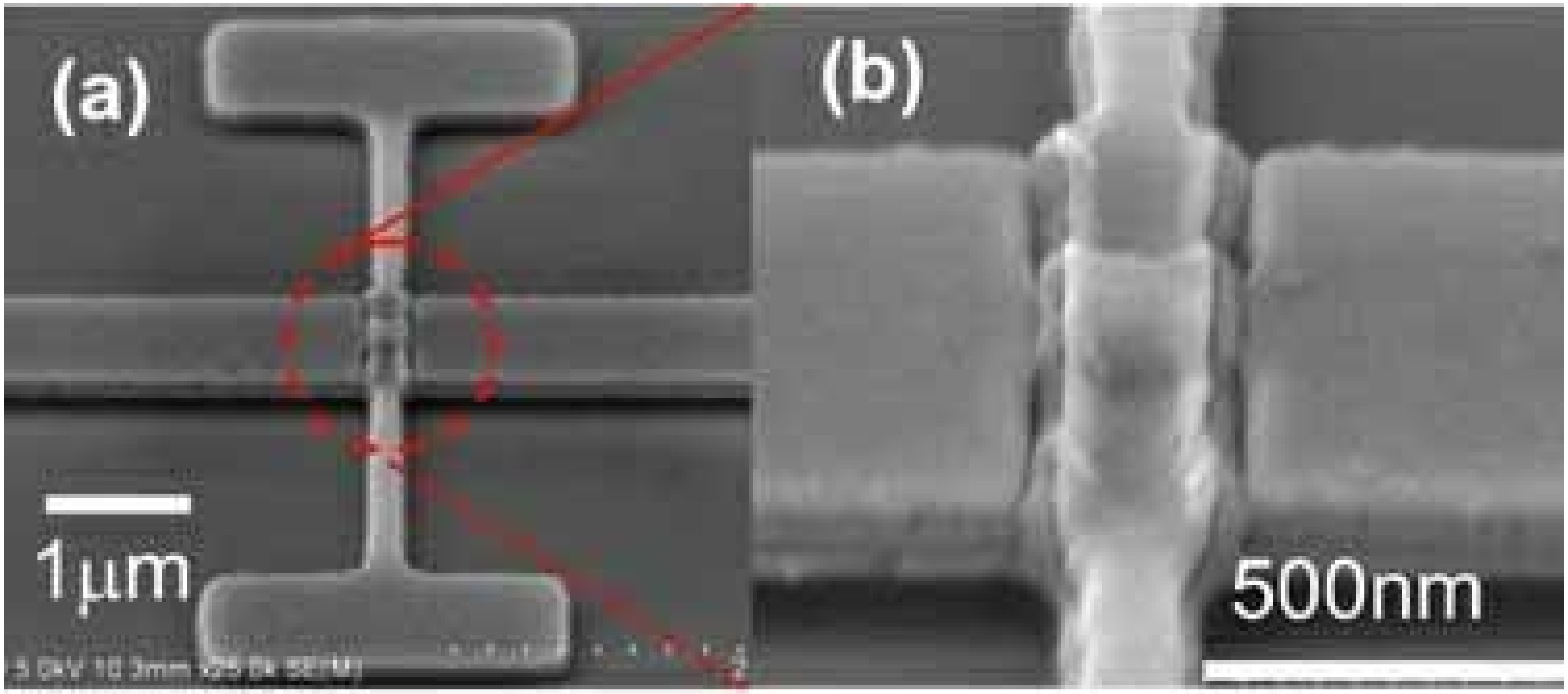
Gate Sidewall Formation

Ni SALISIDE Process (Ni 9nm / TiN 10nm)

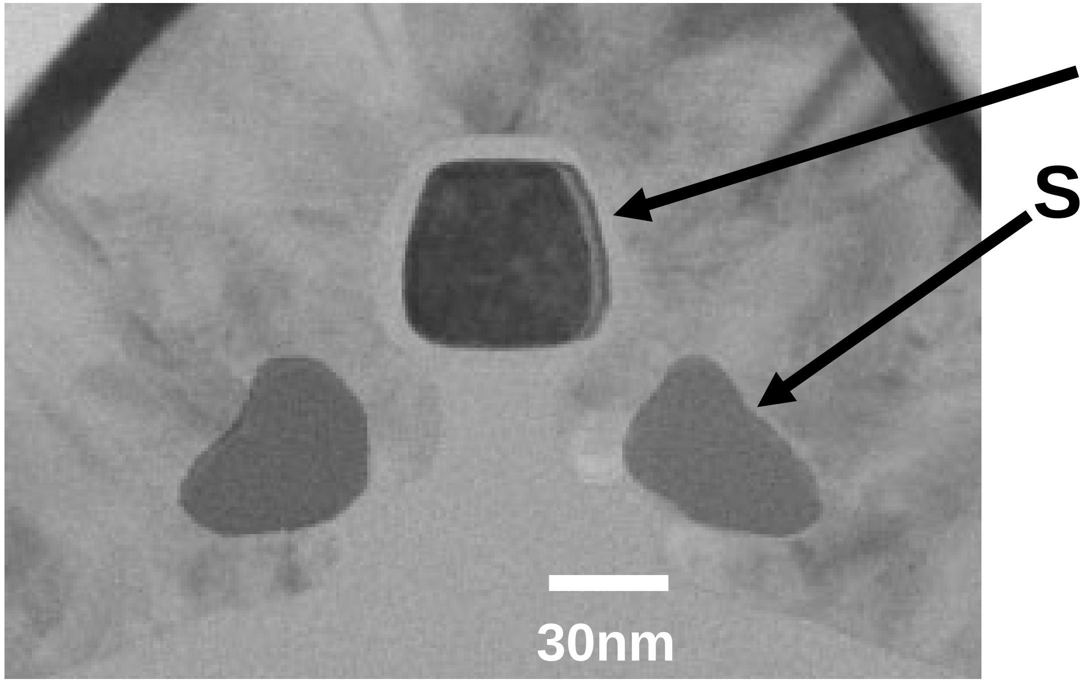
Backend

Standard recipe for gate stack formation

(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.

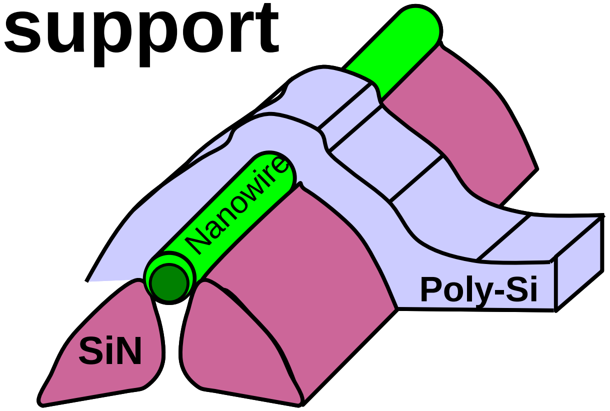


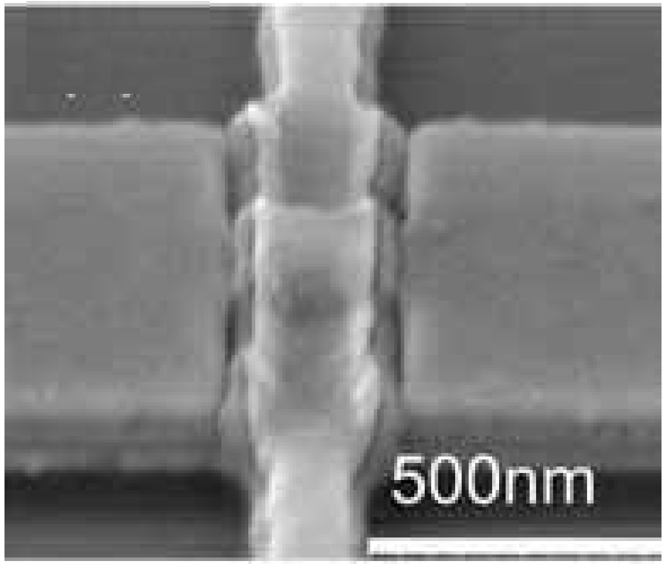
Fabricated SiNW FET



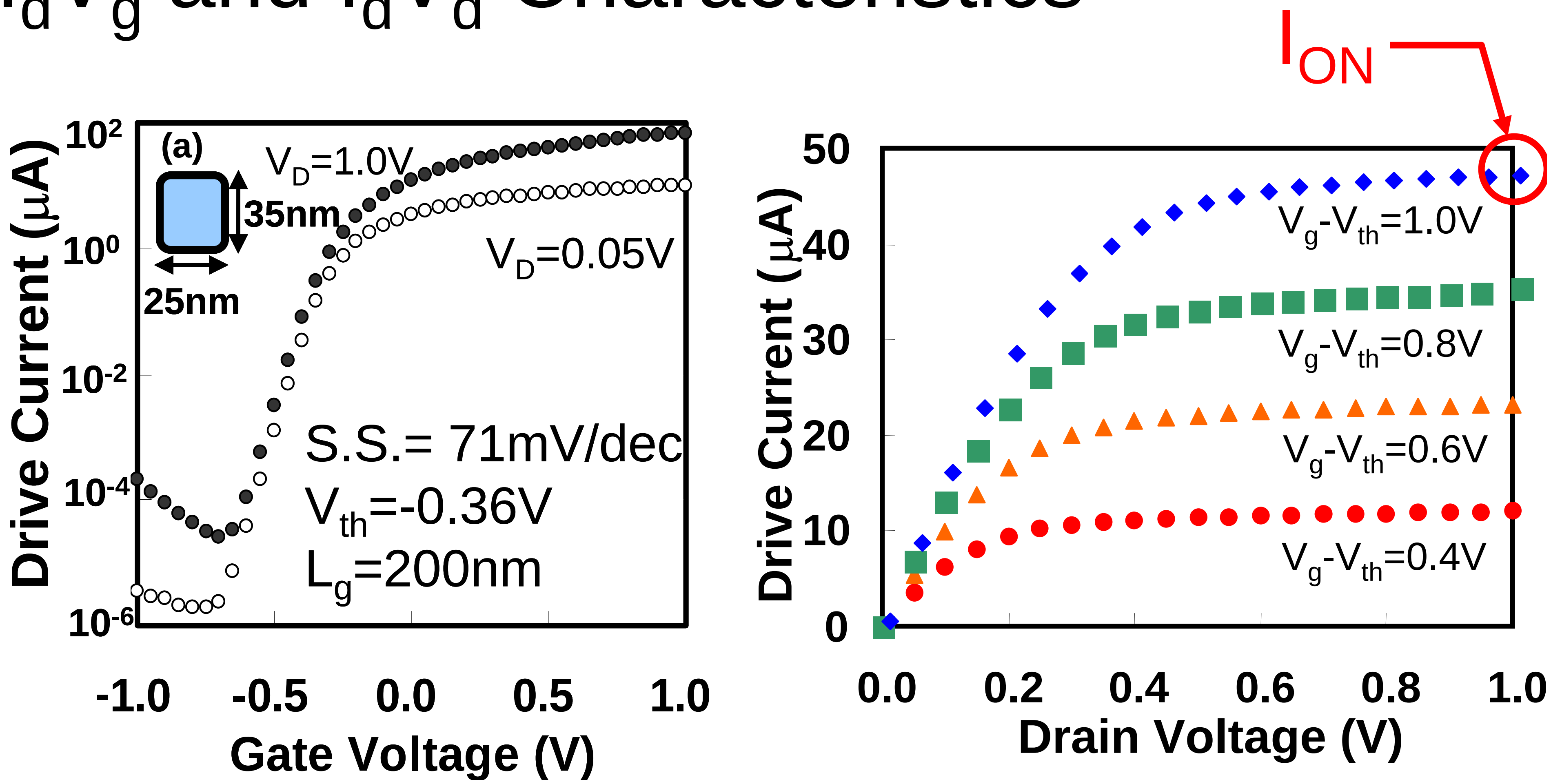
SiNW

SiN support



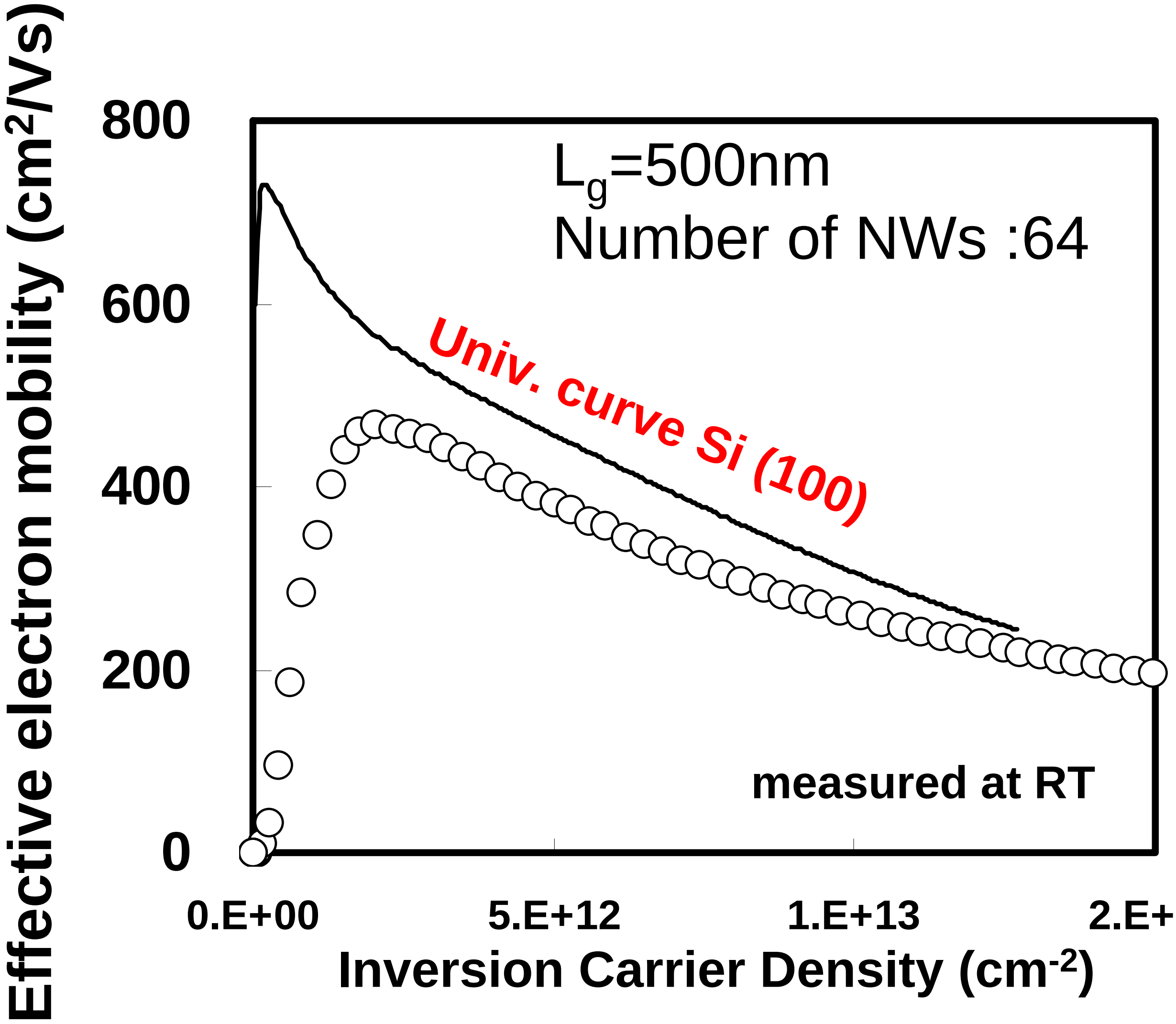


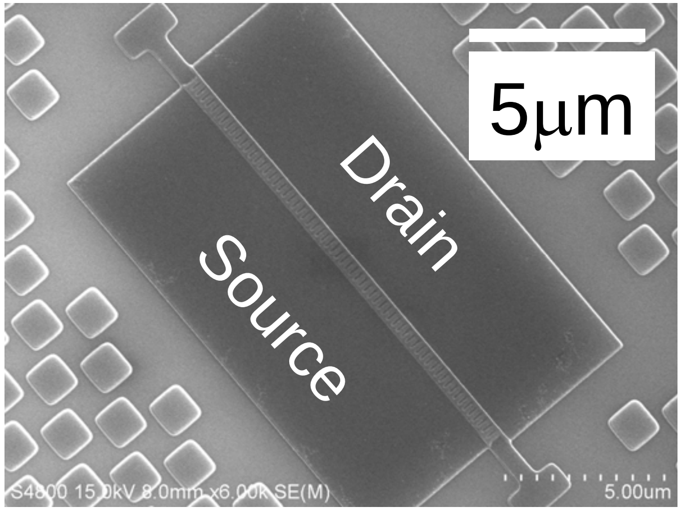
I_dV_g and I_dV_d Characteristics



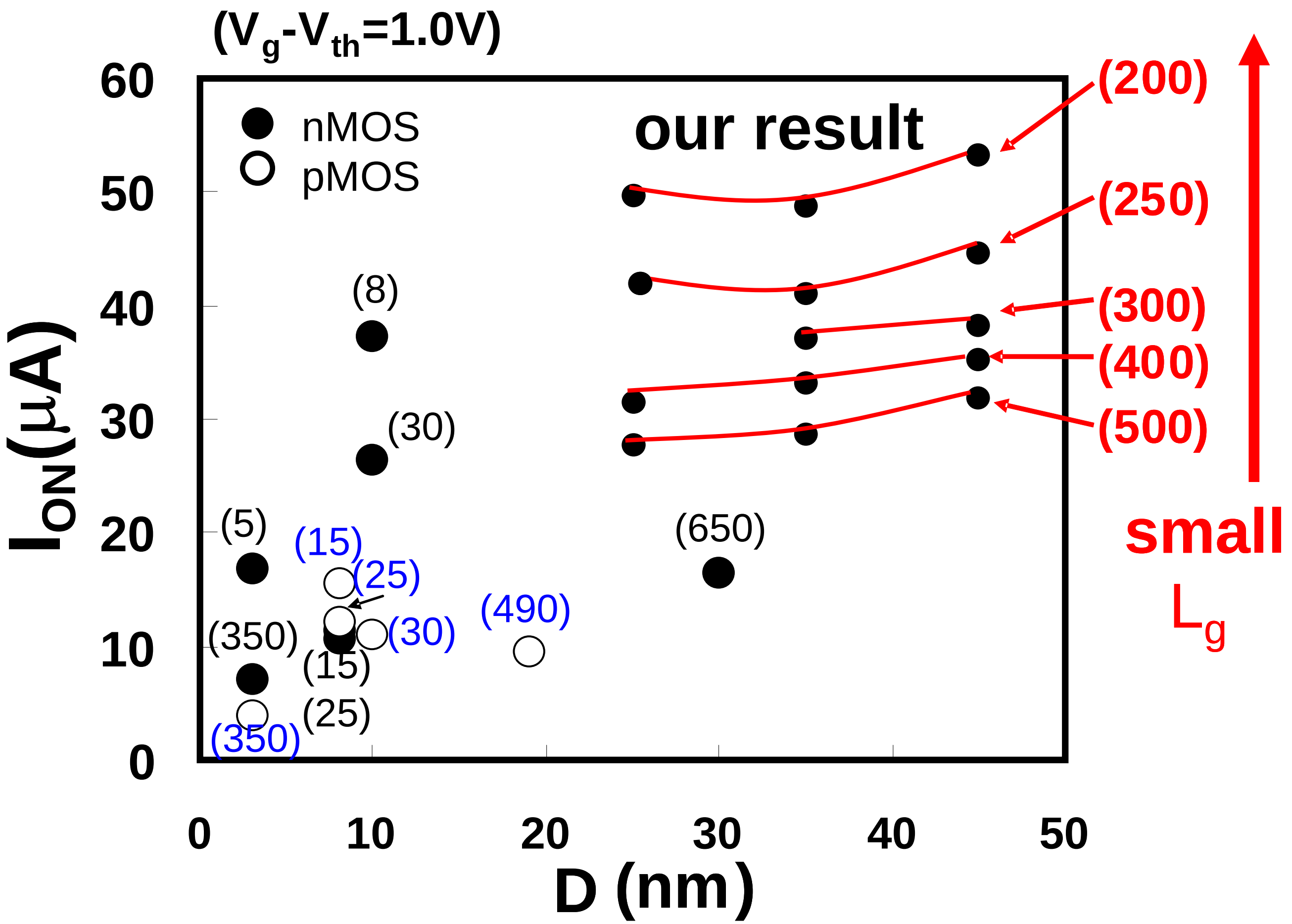
I_{on}/I_{off} ratio of ~10^7, high I_{on} of 49.6 μA/wire

Effective mobility extraction

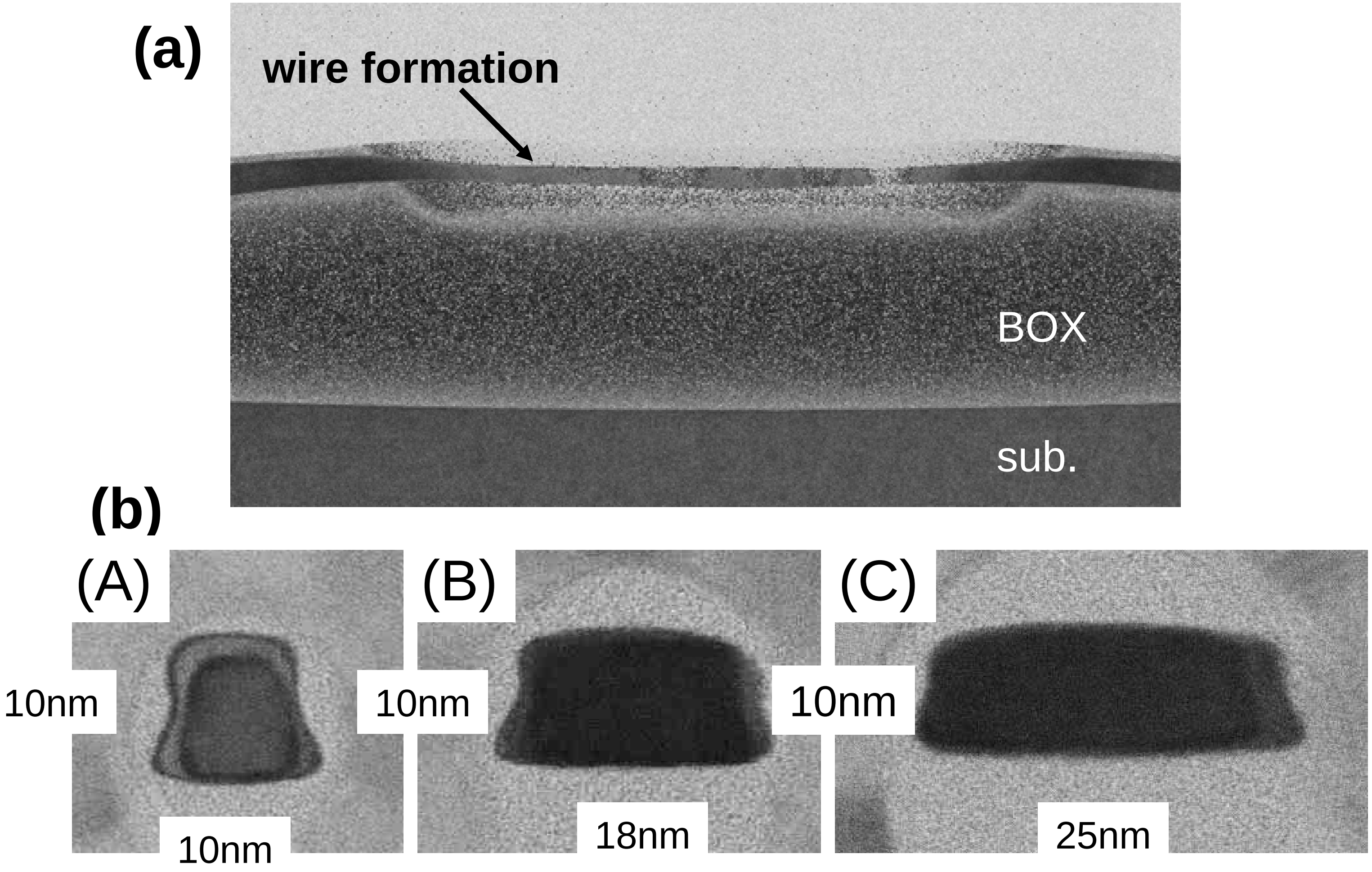




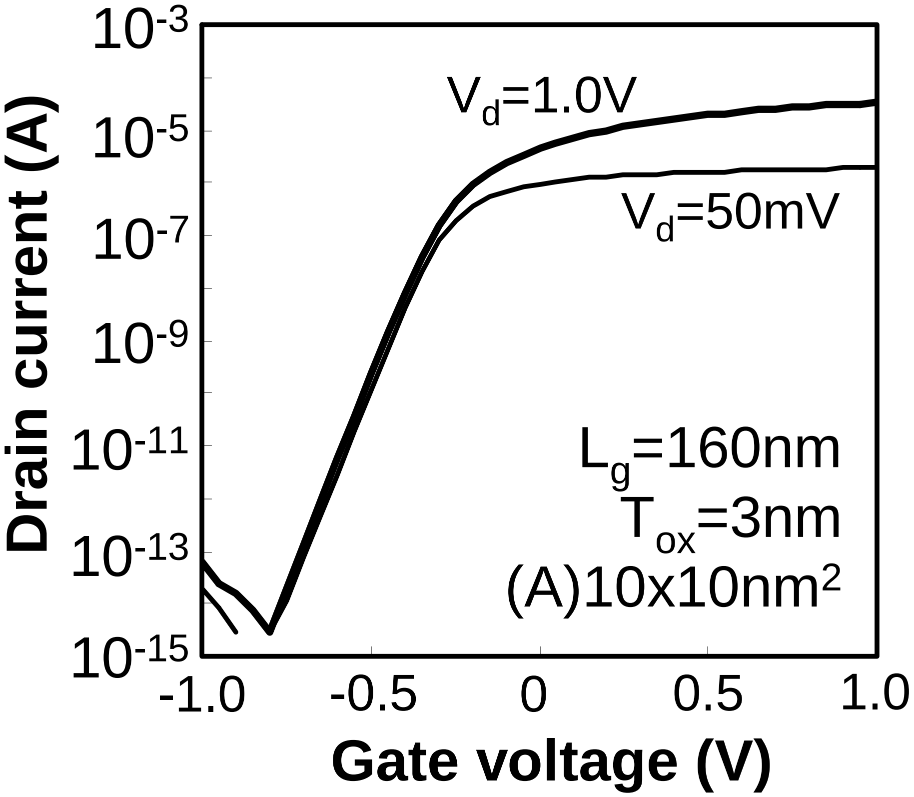
Comparison of Si NW FET being already reported with Si NW FETs in this work

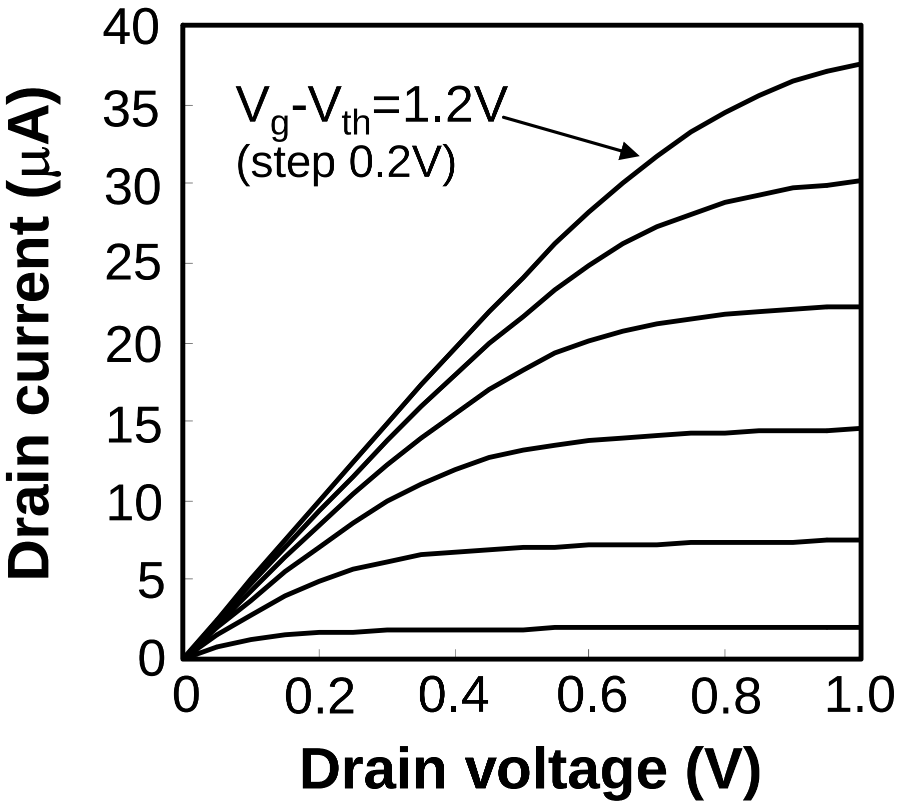


??

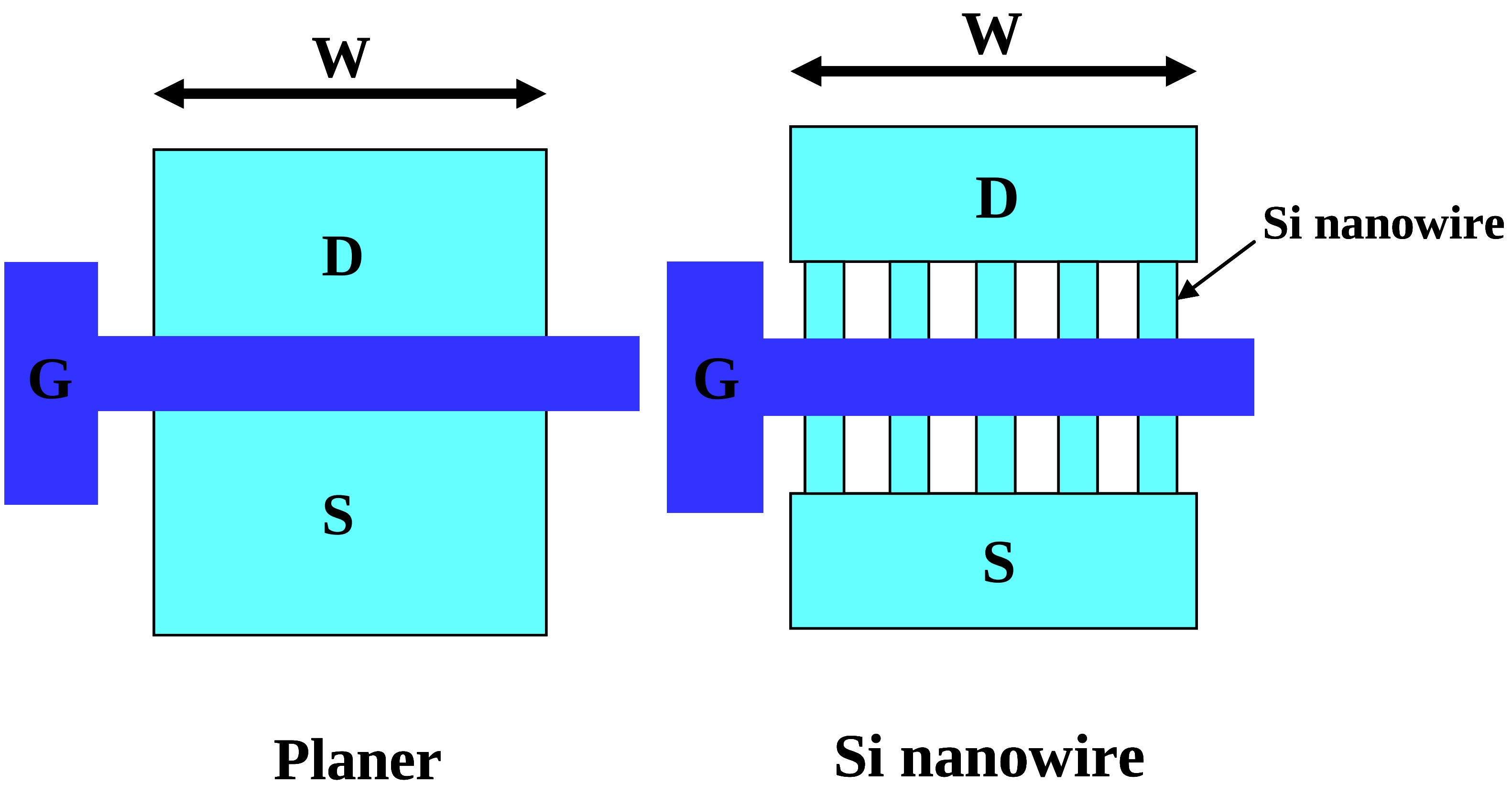

(a)
wire formation
BOX
sub.
(b)
(A)
10nm
10nm
(B)
10nm
18nm
(C)
10nm
25nm

Output characteristics of 10x10cm^2 SiNW FET

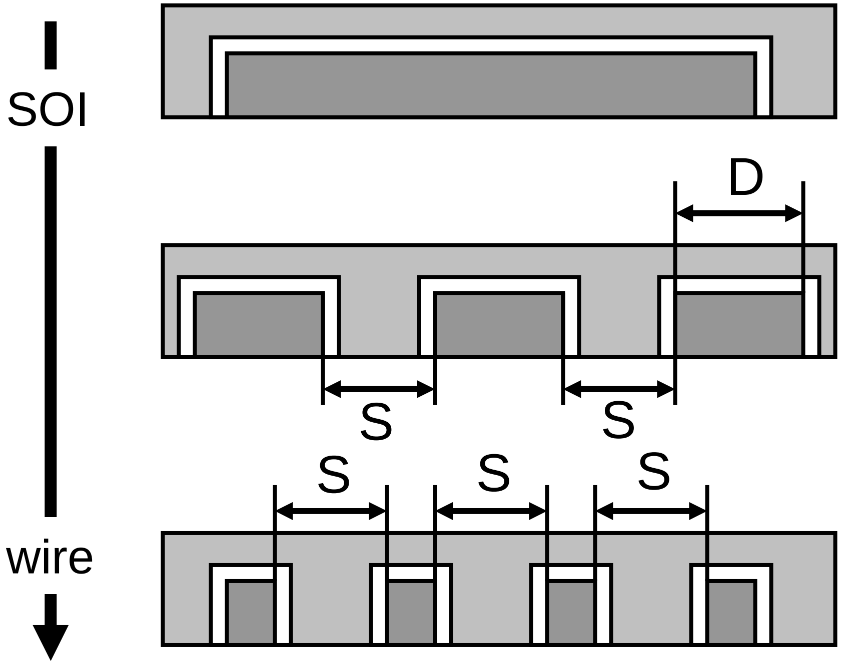




Occupying area of Si bulk planar FET and Si NW FET.
Drive current should be compared with the same width, W



On current evaluation base on gate width



Year	half-pitch (nm), P
2010	45
2014	28
2018	18
2022	11

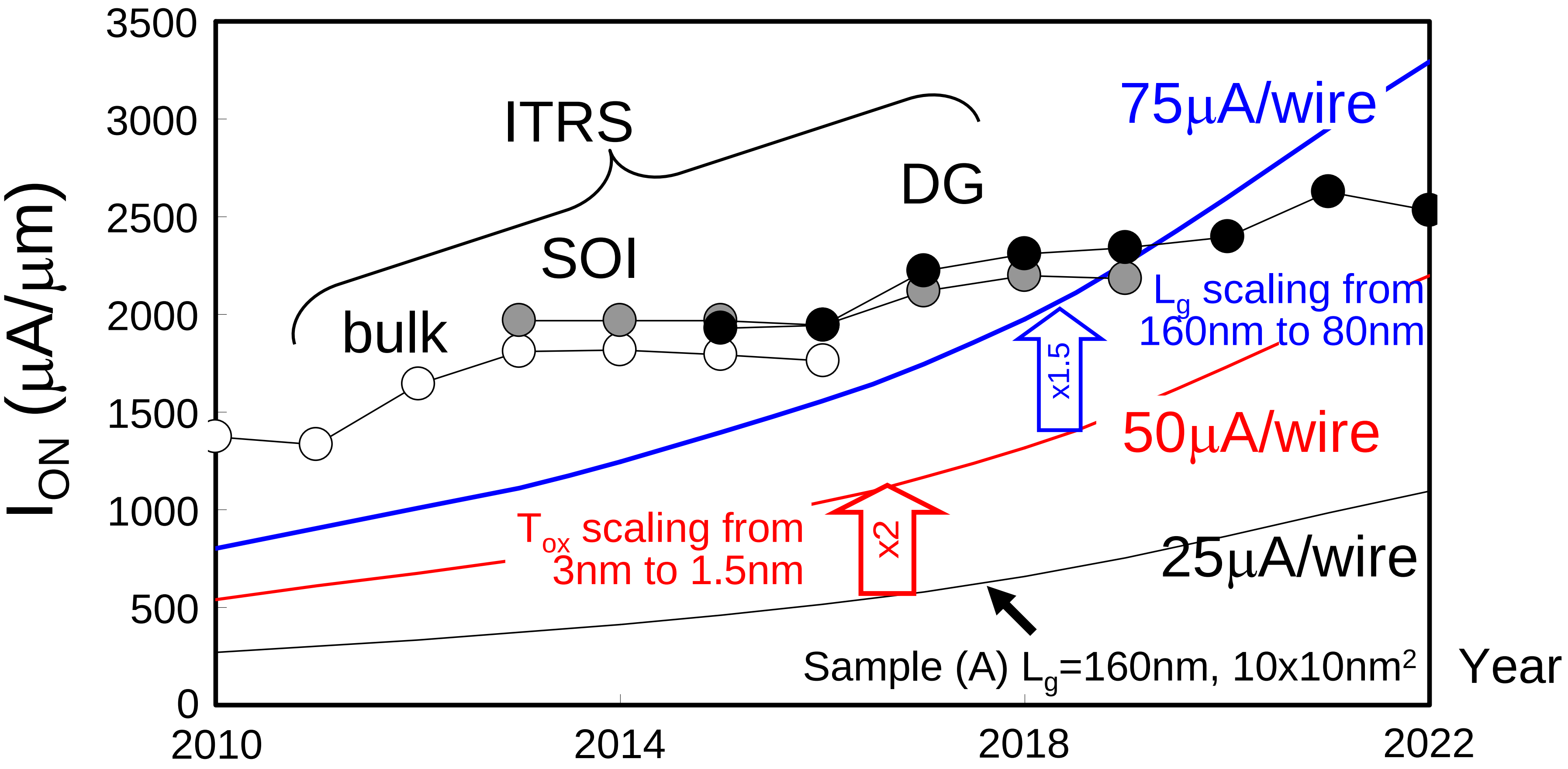
(based on ITRS2008update)

Numbers of wires are determined by the lithographic technology

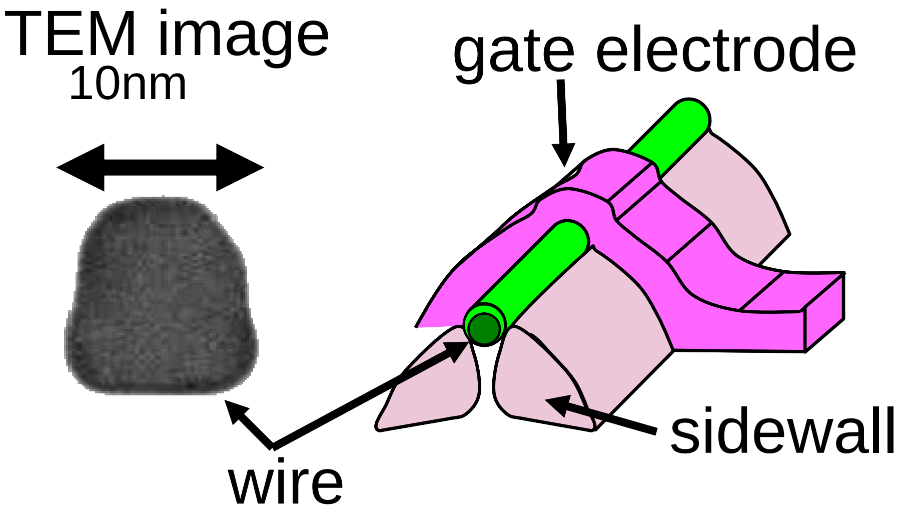
$$\#N = \frac{1000(\mathrm{nm})}{P} \quad \text{or} \quad \frac{1000(\mathrm{nm})}{D+P/2}$$

(at D<P/2) (at D>P/2)

Performance of SiNW FET in ITRS



With device scaling in T_{ox} and L_g, SiNW FET can exceed the required performance in ITRS



Advantage of Si nanowire

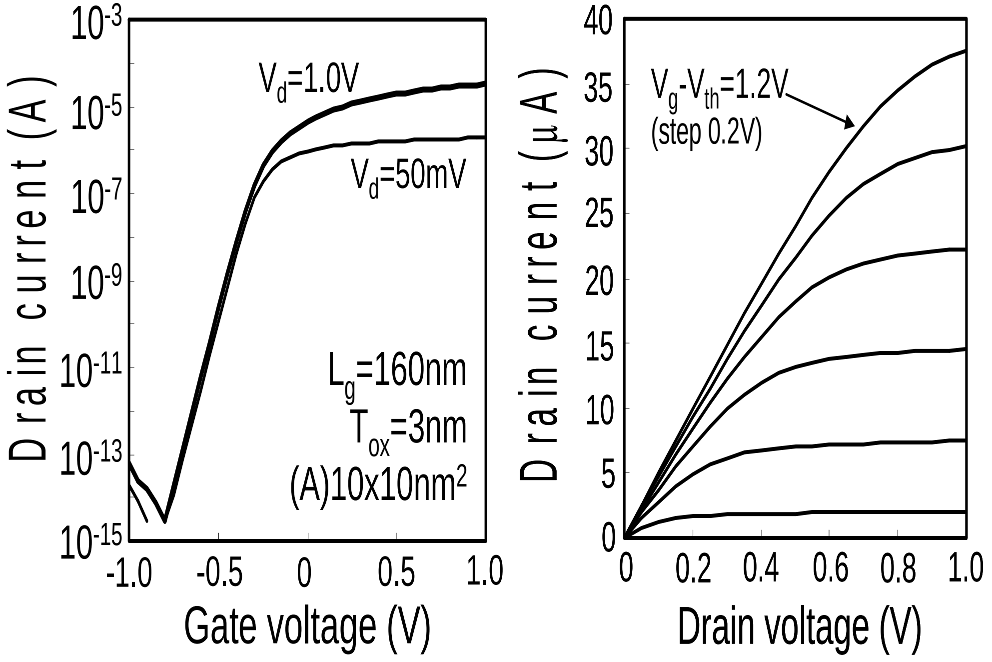
Large drive current

Spec. in 2019 by ITRS

I_{ON}=2.3mA/μm

L_g=11nm, T_{ox}=0.6nm

L_g=160nm, T_{ox}=3nm



Nice cut-off High drive

Our nanowire FET (with 2010 Litho. tech.)

I_{ON}=0.25mA/μm

L_g=160nm

T_{ox}=3.0nm

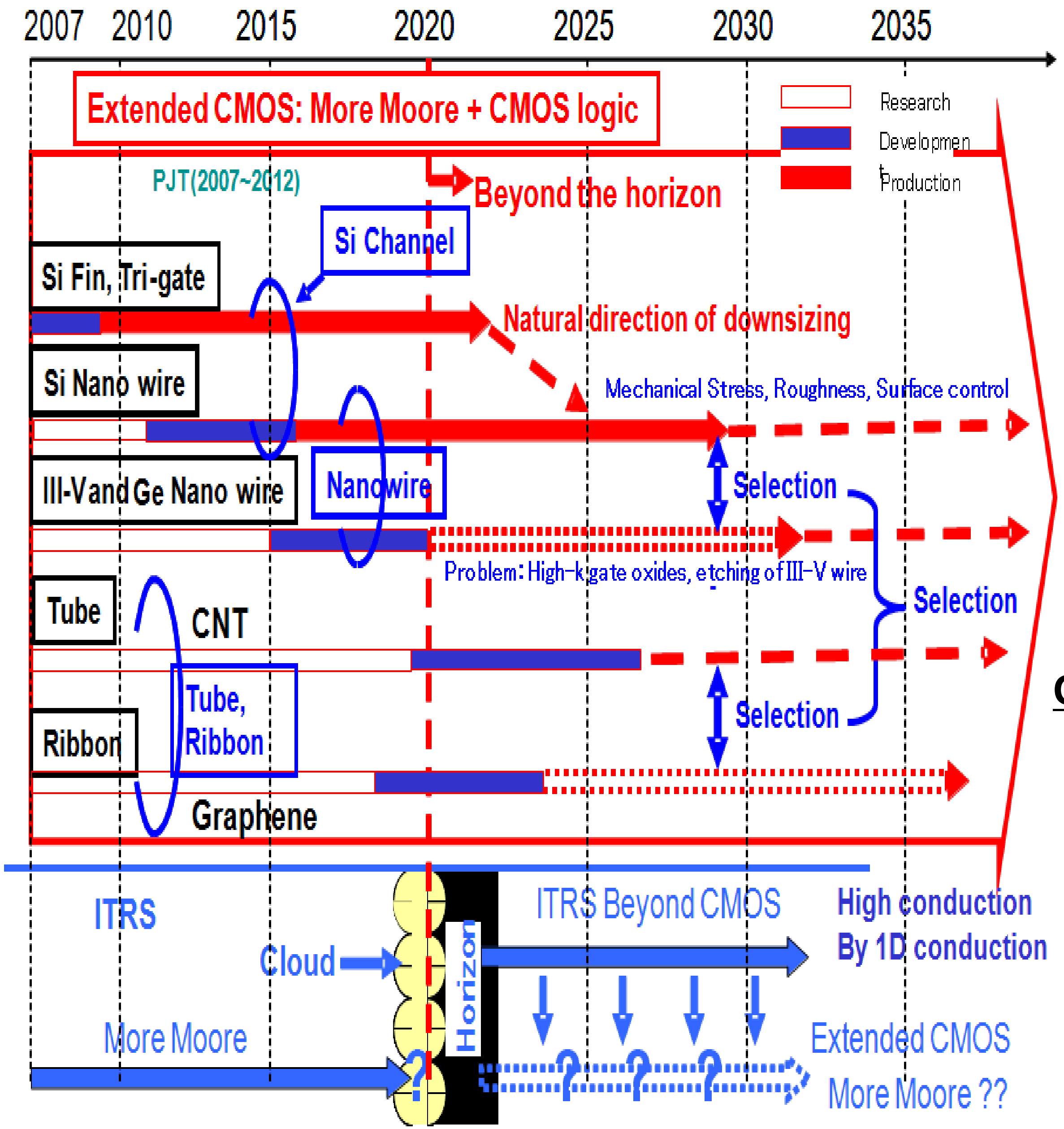
With 2019 litho. tech.

I_{ON}=2.3mA/μm will be obtained even with L_g=80nm and T_{ox}=1.5nm

by the courtesy of Professor H.Iwai

Our roadmap for R &D

Source: H. Iwai, IWJT 2008



Current Issues

Si Nanowire

Control of wire surface property

Source Drain contact

Optimization of wire diameter

Compact I-V model

III-V & Ge Nanowire

High-k gate insulator

Wire formation technique

CNT:

Growth and integration of CNT

Width and Chirality control

Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique

Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

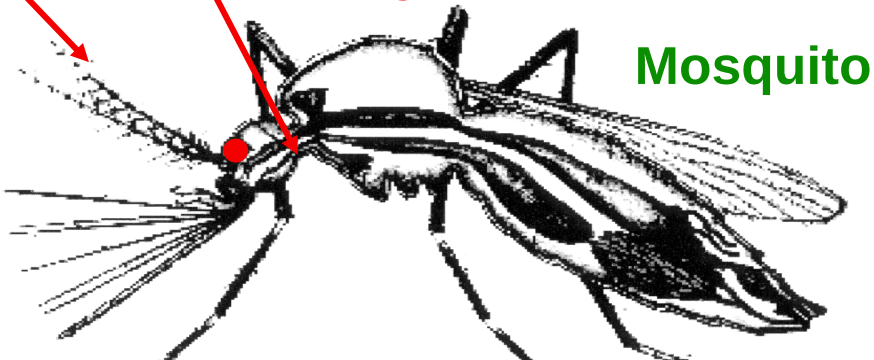
Sensor

Infrared
Humidity
CO_2

Brain

Ultra small volume
Small number of neuron cells
Extremely low power

Real time image processing
(Artificial) Intelligence
3D flight control



Mosquito

System and Algorism becomes more important !

But do not know how?

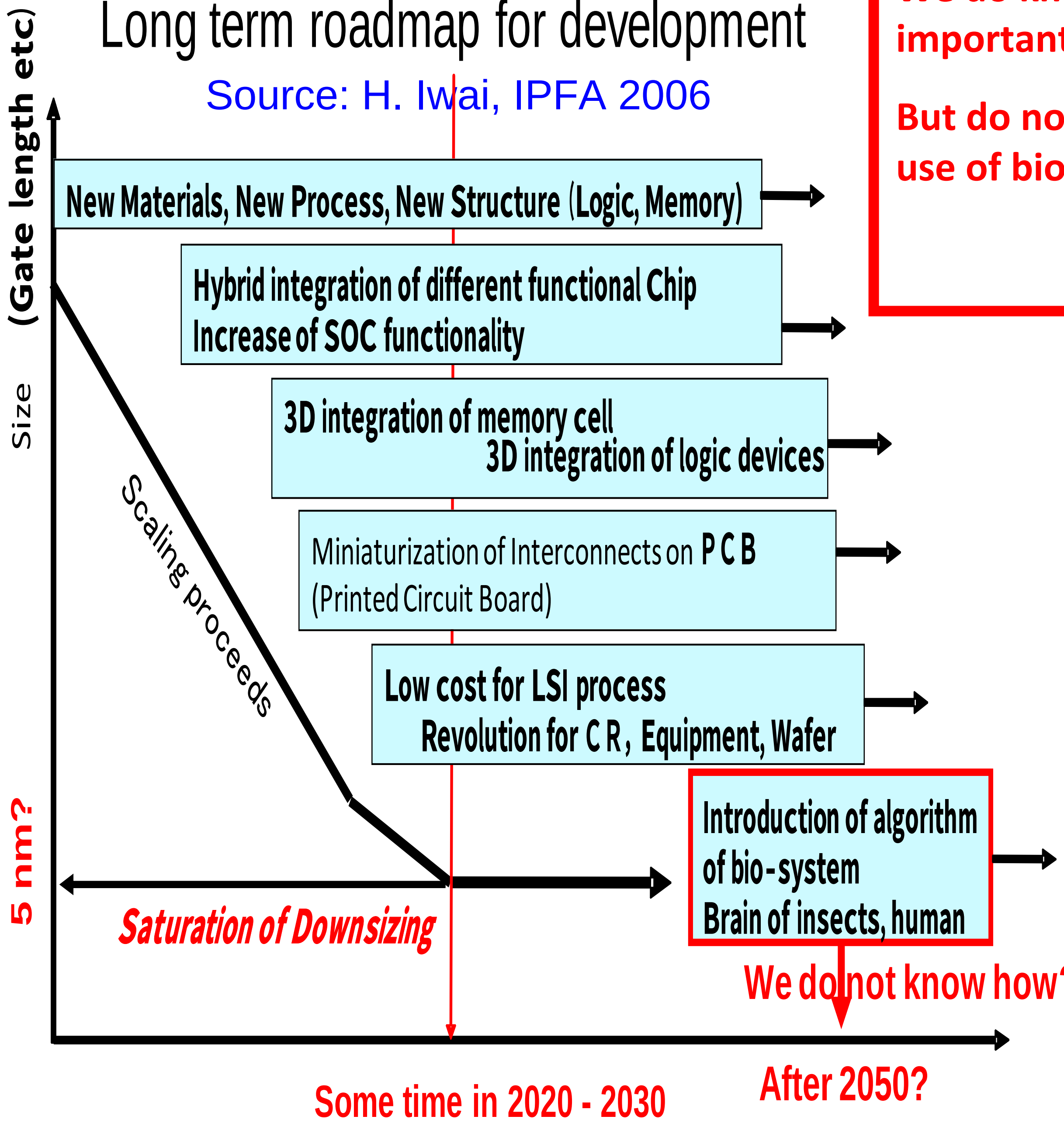
Dragonfly is further high performance

Long term roadmap for development

Source: H. Iwai, IPFA 2006

We do know system and algorithms are important!

But do not know how it can be by us for use of bio?



New Materials, New Process, New Structure (Logic, Memory)

Hybrid integration of different functional Chip
Increase of SOC functionality

3D integration of memory cell
3D integration of logic devices

Miniaturization of Interconnects on PCB
(Printed Circuit Board)

Low cost for LSI process
Revolution for CR, Equipment, Wafer

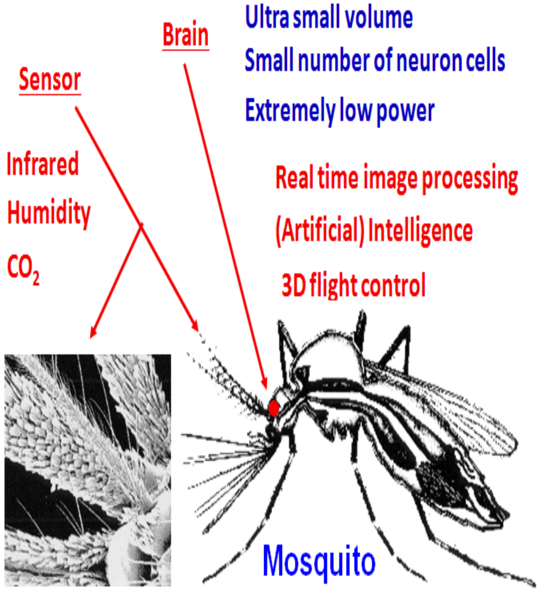
Introduction of algorithm
of bio-system
Brain of insects, human

Saturation of Downsizing

We do not know how?

Some time in 2020 - 2030

After 2050?



Ultra small volume

Small number of neuron cells

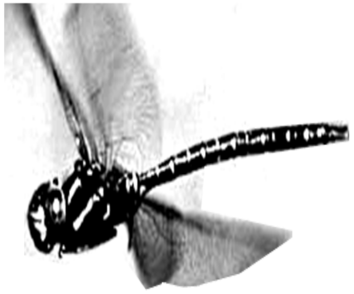
Extremely low power

Real time image processing

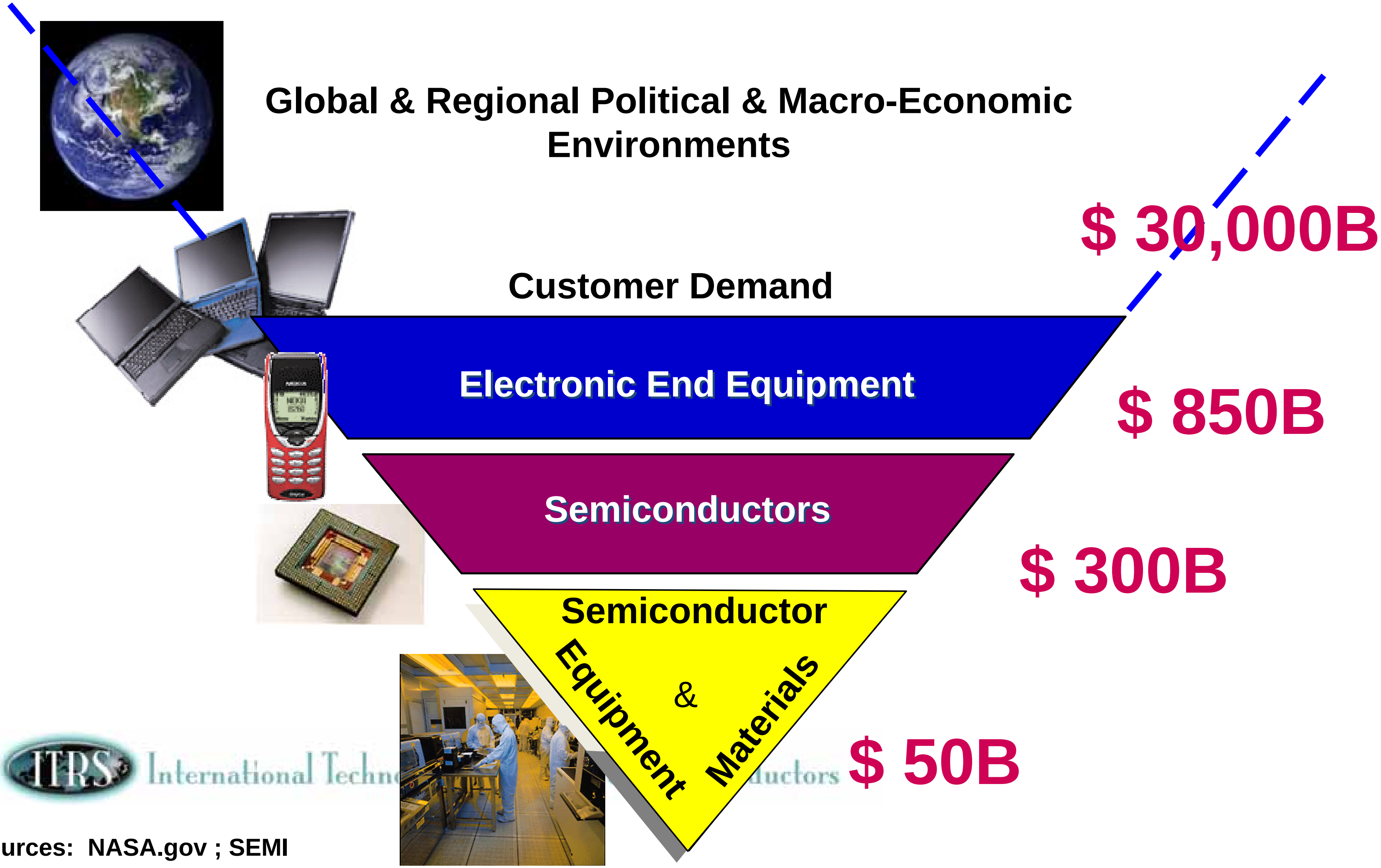
(Artificial) Intelligence

3D flight control

Dragonfly brain has even further higher performance



Wanted: CUSTOMERS, who breathe, eat, and live in…..



Global & Regional Political & Macro-Economic Environments

$ 30,000B

Customer Demand

Electronic End Equipment

$ 850B

Semiconductors

$ 300B

Semiconductor Equipment & Materials

$ 50B

Sources: NASA.gov ; SEMI

Data Source: UN

population in million people