Si Nanoelectronic Device Technology

@East China Jiaotong University,

華東交通大学、南昌

March 16, 2010

東京工業大学
Tokyo Institute of Technology

先端研究中心
Frontier Research Center

岩井　洋　Hiroshi Iwai

Tokyo Institute of Technology

Founded in 1881, Promoted to Univ. 1929

Institute Overview

Einstein Visit

Established in 1881→ 130th anniversary in 2011

3 undergraduate schools

School of Science, School of Engineering, School of Bioscience and Biotechnology

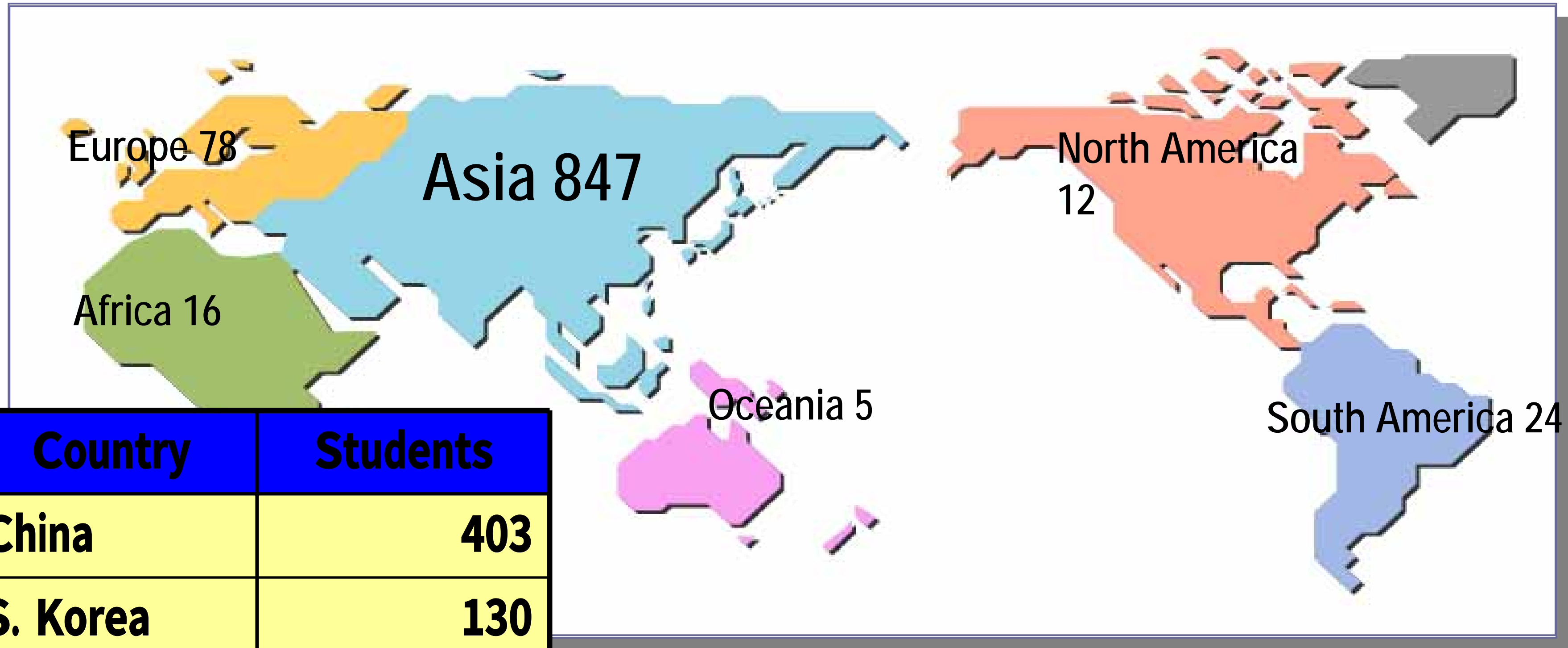
7 graduate schools

Science and Engineering Science, Science and Engineering Technology,
Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

	Undergraduate	Graduate	Master's	Doctoral	Teaching Staff	Student/Instructor	Staff
Tokyo Inst.	**5,000**	**5,000**	**3,500**	**1,500**	**1,200**	**8.3**	**550**
Per Year	**1,200**		**1,800**	**500**			

International Students



Country	Students
China	403
S. Korea	130
Indonesia	64
Thailand	55
Vietnam	60
Malaysia	28

Total 982

(As of May. 1, 2005)

Importance of Electronics

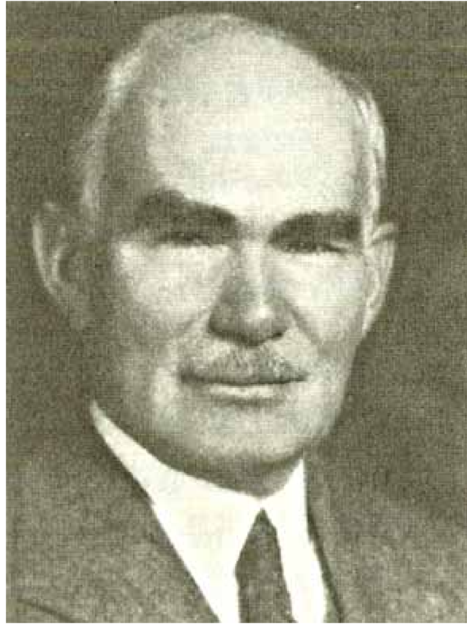
- There were many inventions in the 20th century:

  Airplane, Nuclear Power generation, Computer,

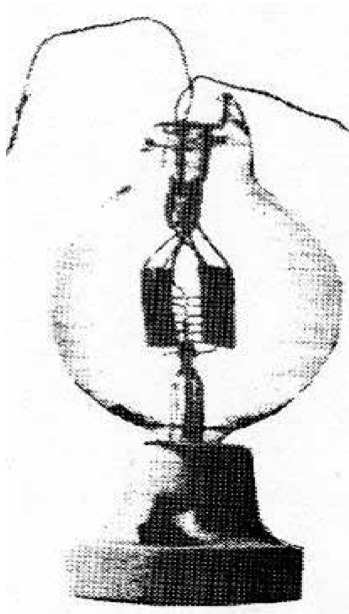
  Space aircraft, etc
- However, everything has to be controlled by electronics
- Electronics

  Most important invention in the 20th century
- What is Electronics: To use electrons,

  Electronic Circuits

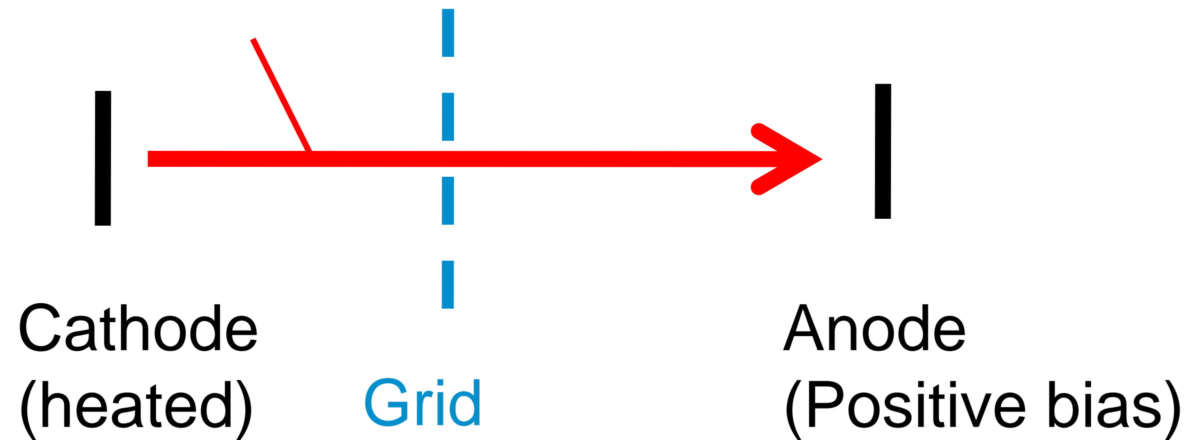


Lee De Forest



Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias



Same mechanism as that of transistor

First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

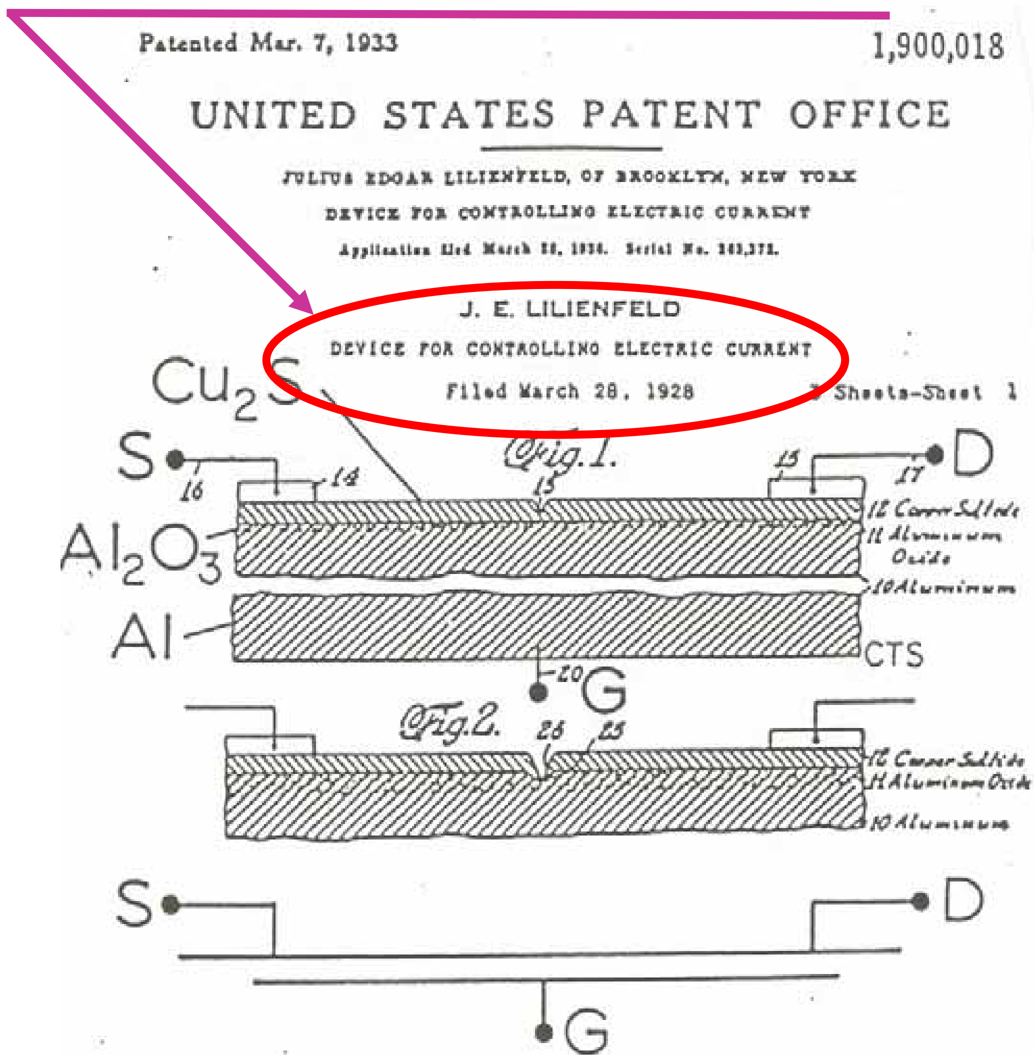
→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

J. E. LILIENFELD

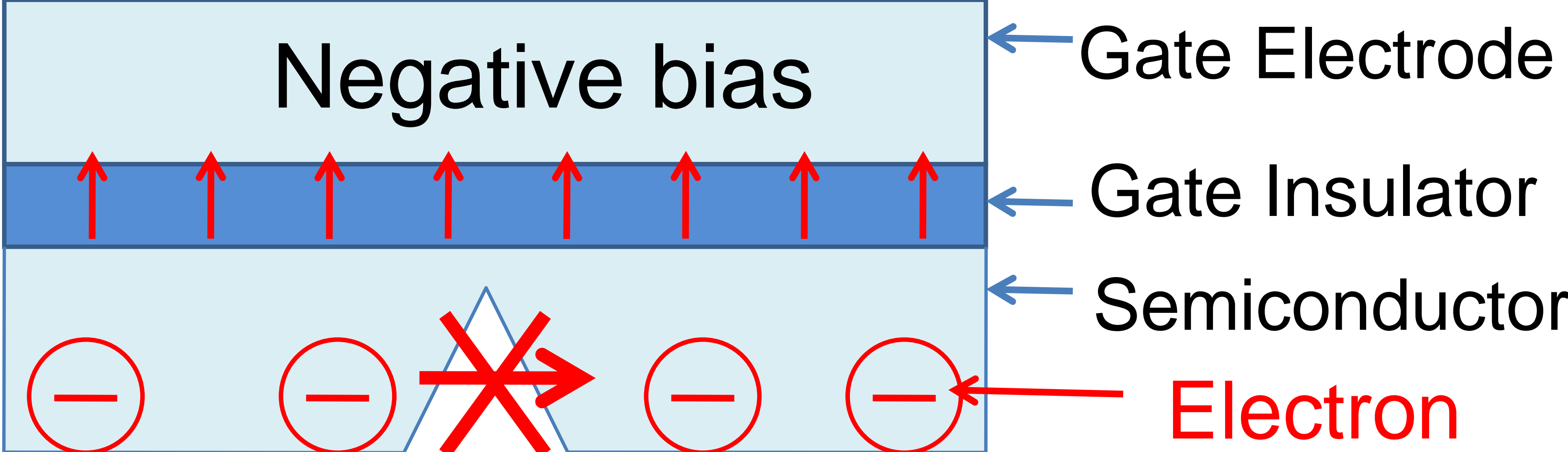
DEVICES FOR CONTROLLED ELECTRIC CURRENT

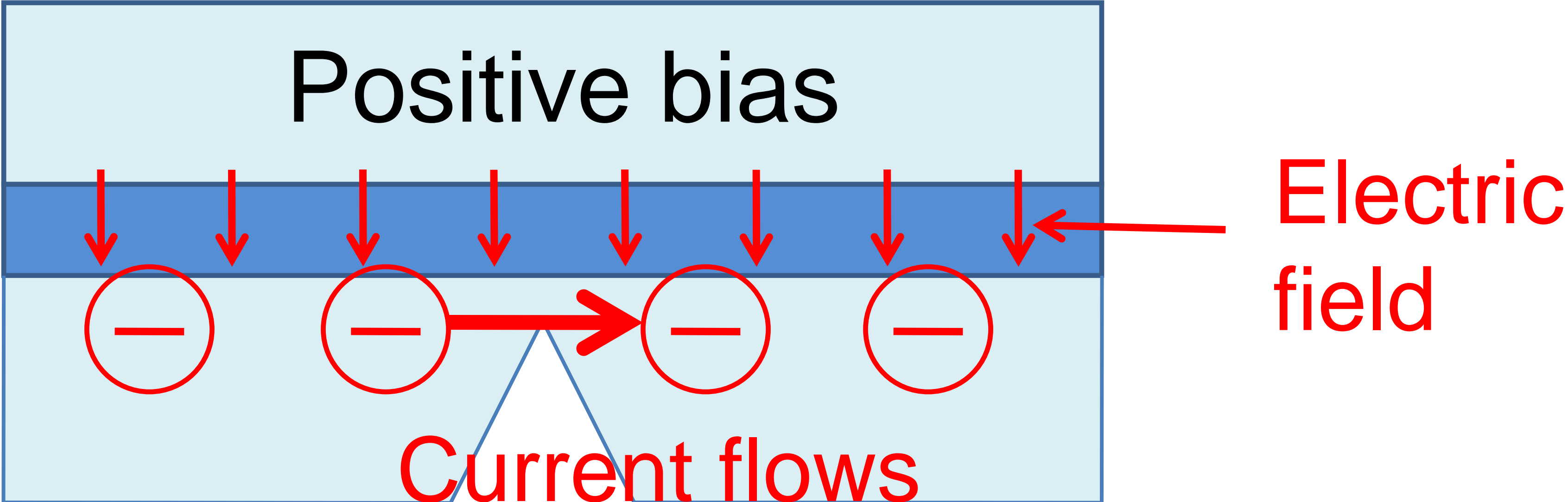
Filed March 28, 1928



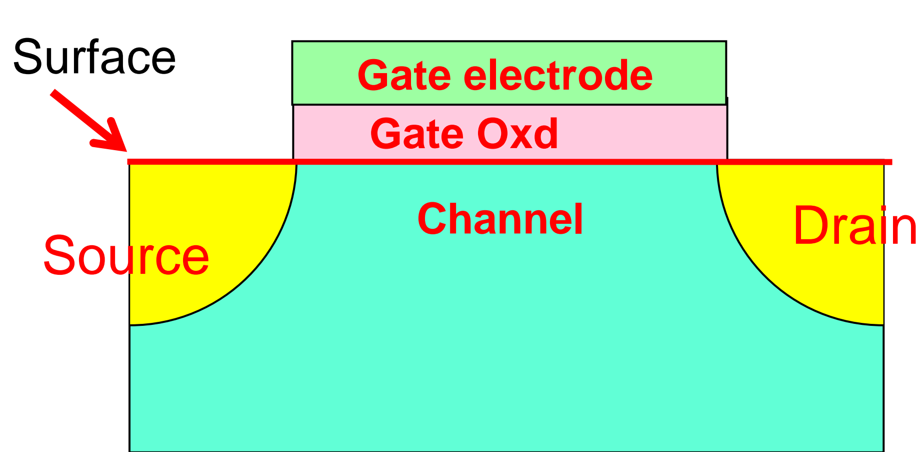
J.E.LILIENFELD

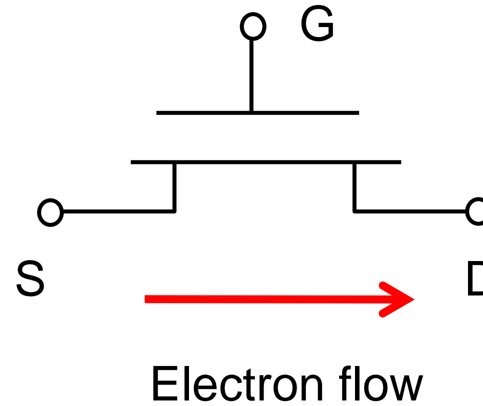
Capacitor structure with notch



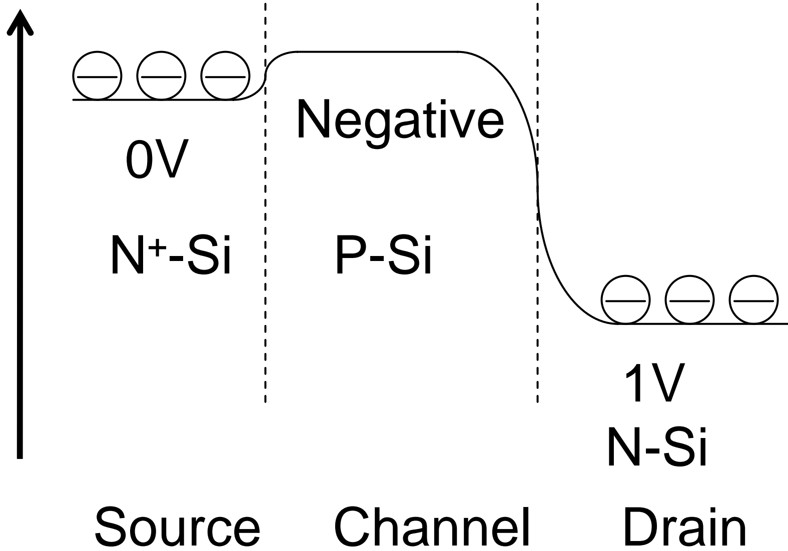


Today’s transistor: MOSFET for CMOS LSI

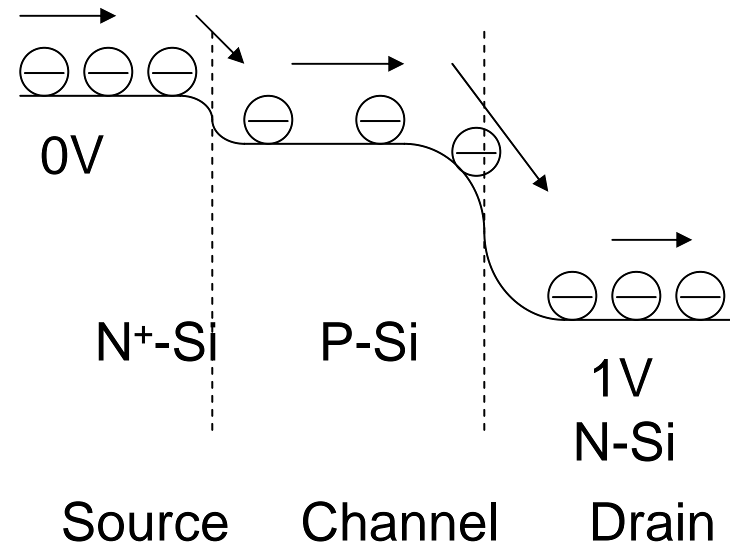




0 bias for gate



Positive bias for gate

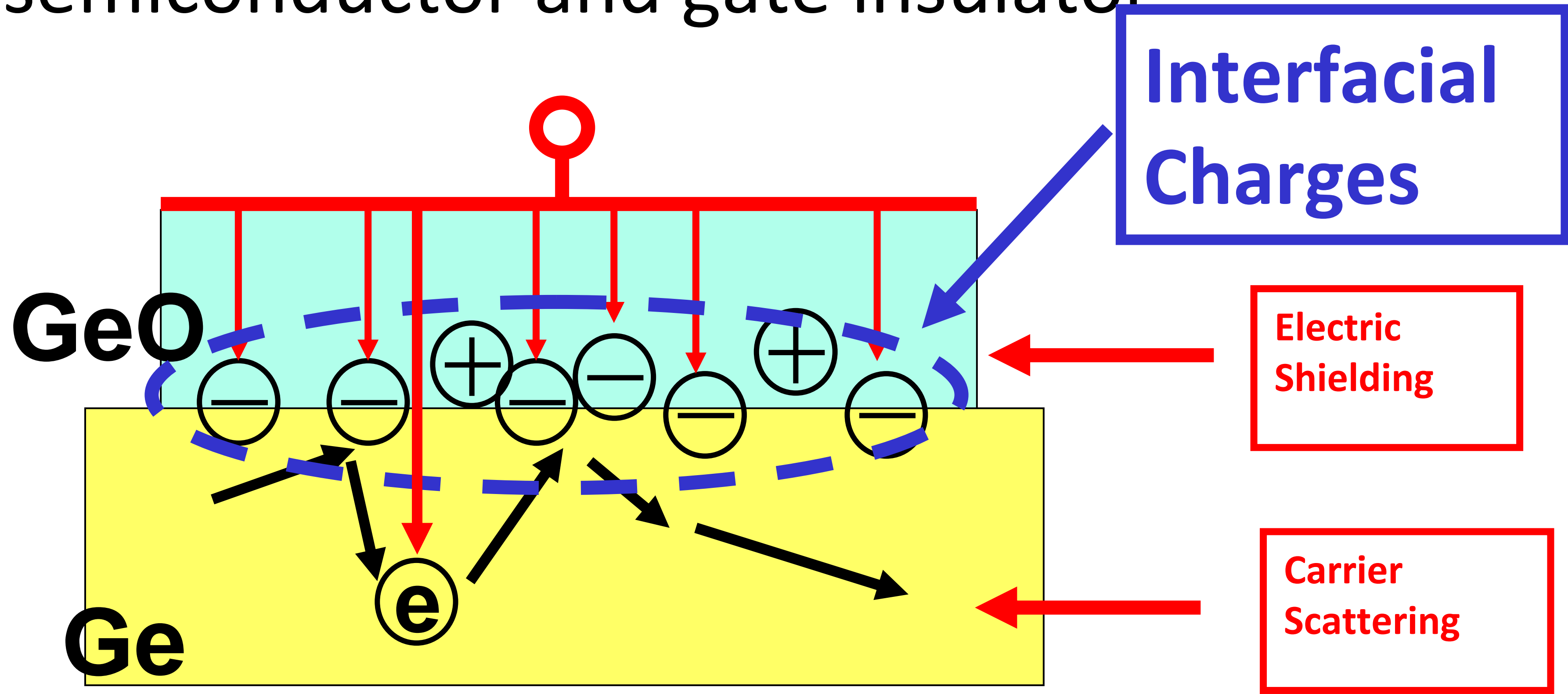


However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!

Very bad interface property between the semiconductor and gate insulator

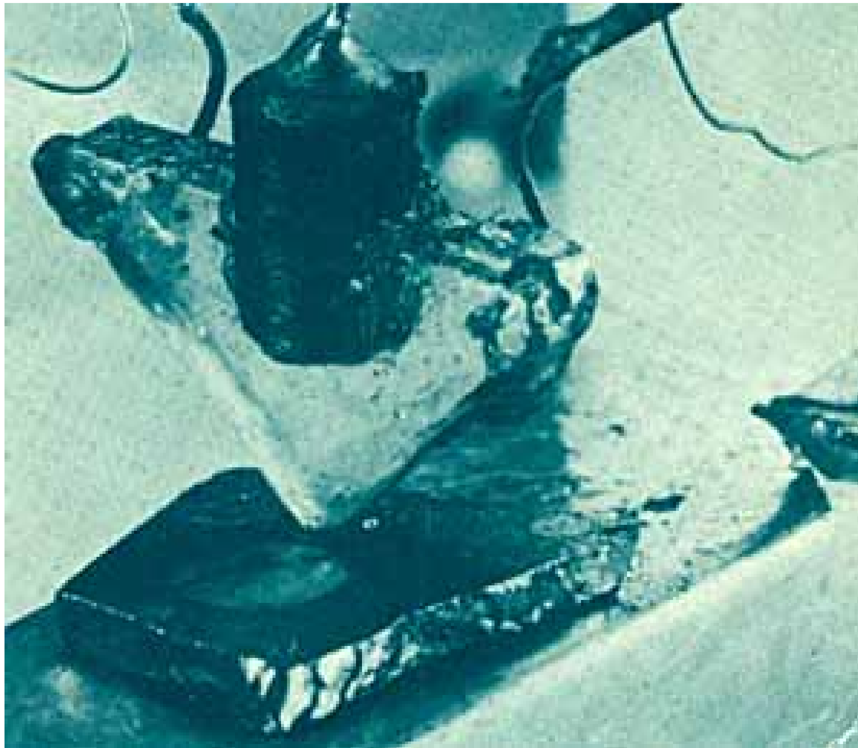


Drain Current was several orders of magnitude smaller than expected

Even Shockley!

However, they found amplification phenomenon when investigating Ge surface when putting needles.
This is the 1st Transistor:
Not Field Effect Transistor,
But Bipolar Transistor (another mechanism)

1947: 1st transistor



Bipolar using Ge

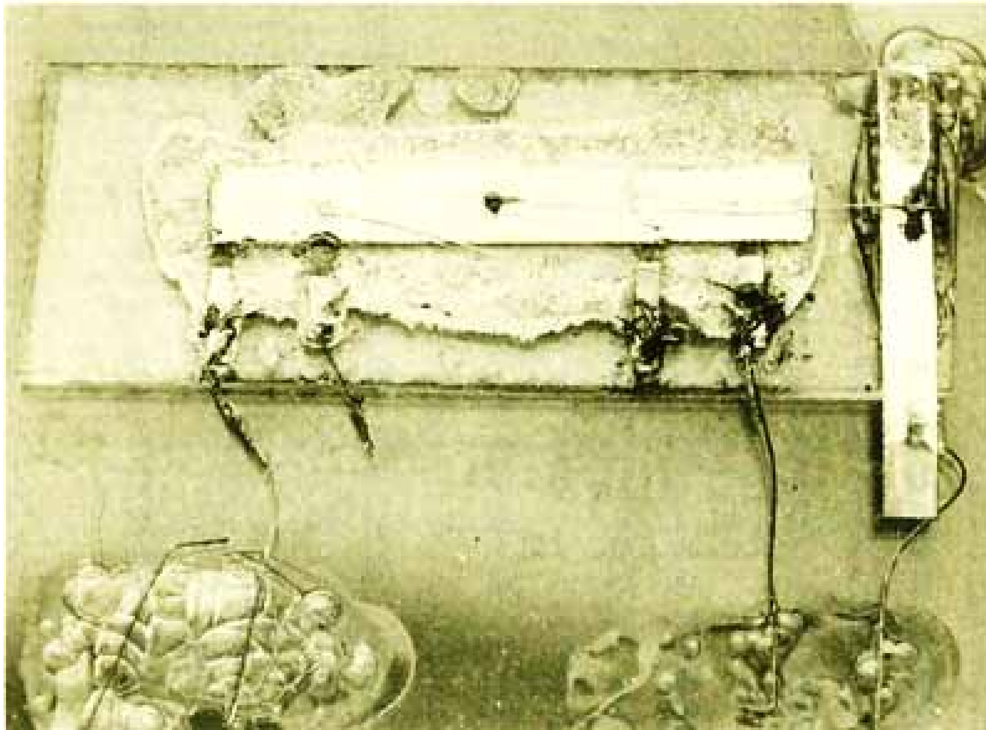
J. Bardeen W. Bratten,

W. Shockley

1958: 1st Integrated Circuit

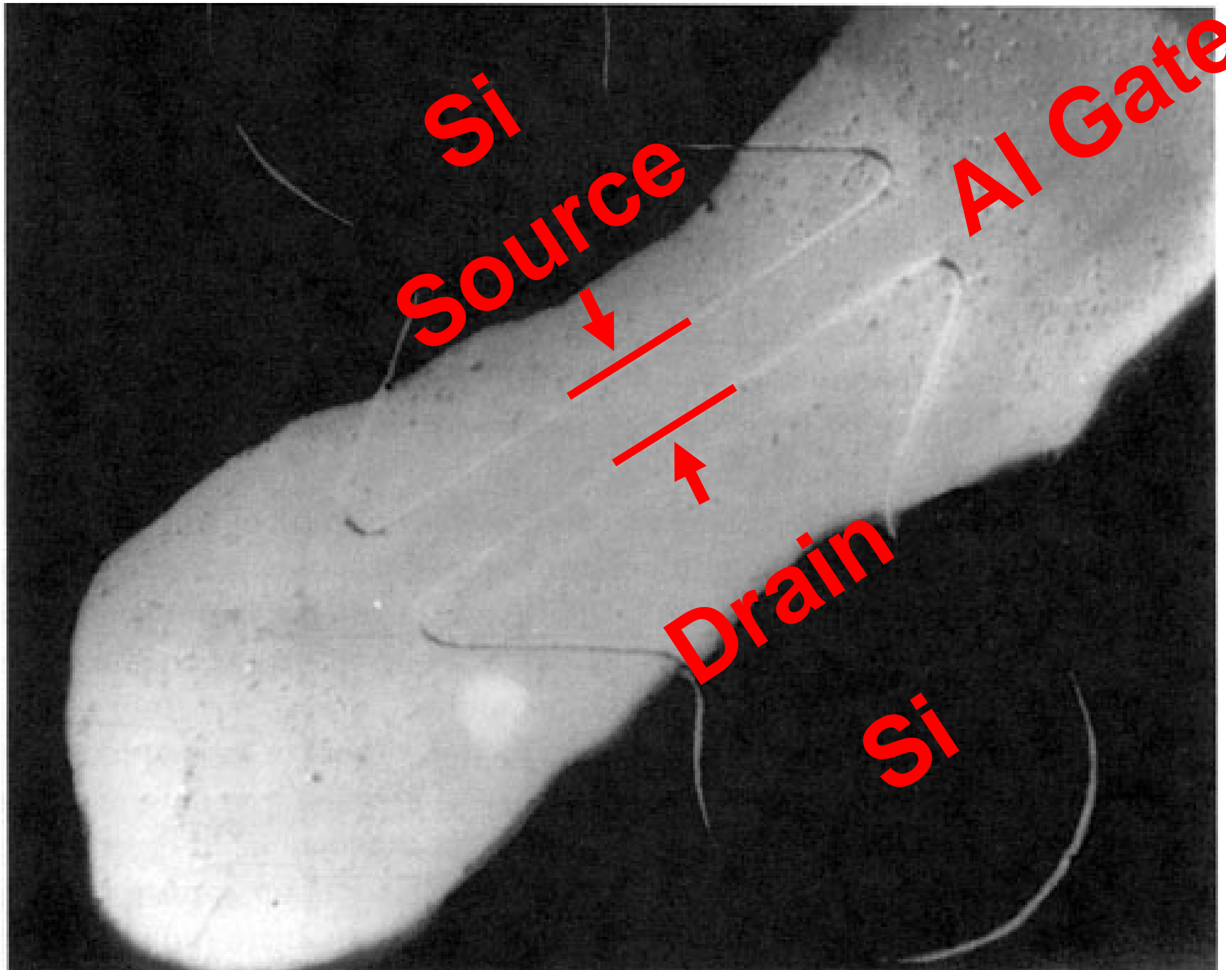
Jack S. Kilby

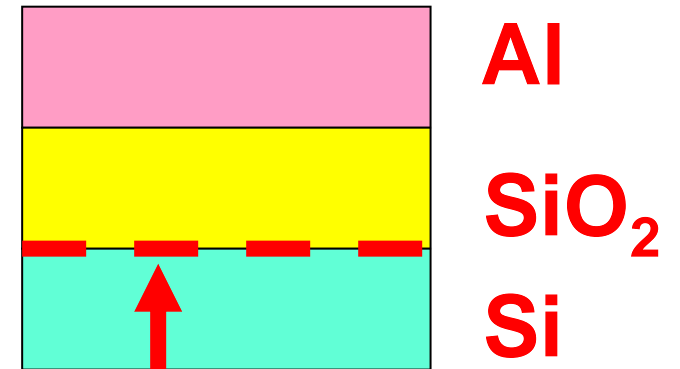
Connect 2 bipolar transistors in the Same substrate by bonding wire.



1960: First MOSFET
by D. Kahng and M. Atalla

Top View

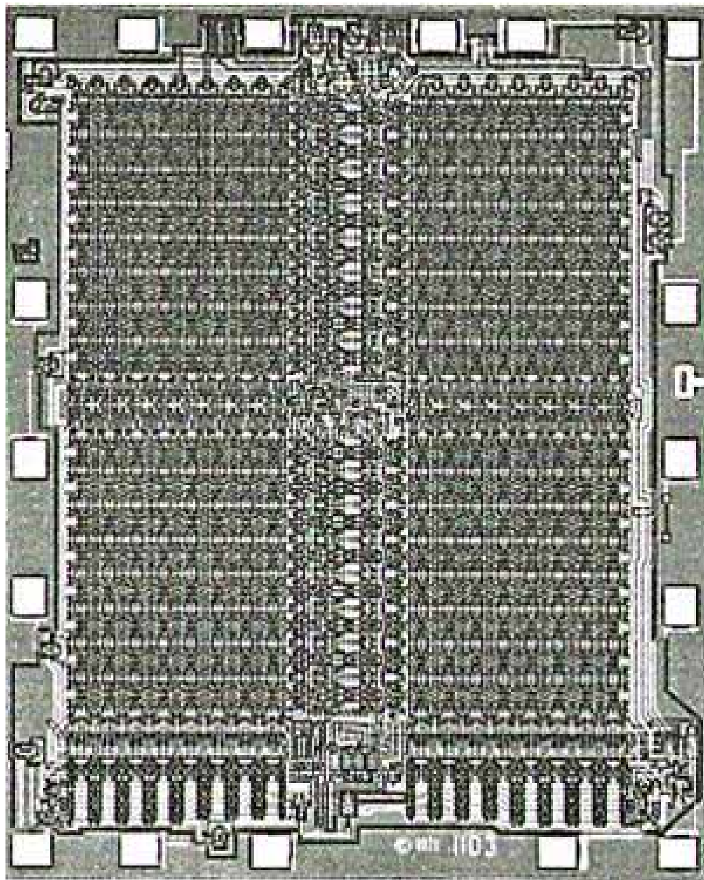




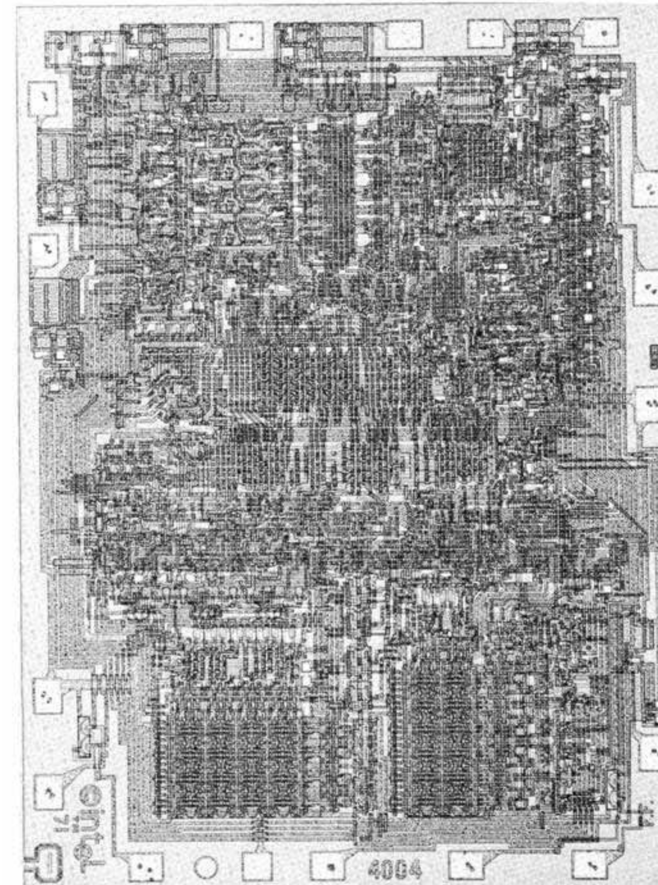
Si/SiO2 Interface is extraordinarily good

1970,71: 1st generation of LSIs

DRAM Intel 1103



MPU Intel 4004



MOS LSI experienced continuous progress for many years

	Name of Integrated Circuits	Number of Transistors
1960s	IC (Integrated Circuits)	~ 10
1970s	LSI (Large Scale Integrated Circuit)	~1,000
1980s	VLSI (Very Large Scale IC)	~10,000
1990s	ULSI (Ultra Large Scale IC)	~1,000,000
2000s	?LSI (? Large Scale IC)	~1000,000,000

Gate Electrode
Poly Si

Gate Insulator
SiO_2

Substrate
Si

MOSFET: Metal Oxide Semiconductor
Field Effect Transistor

Use Gate Field Effect for switching

Gate Electrode
Poly Si

Gate Insulator
SiO_2

Source

n-Si

n-Si

Drain

p-Si

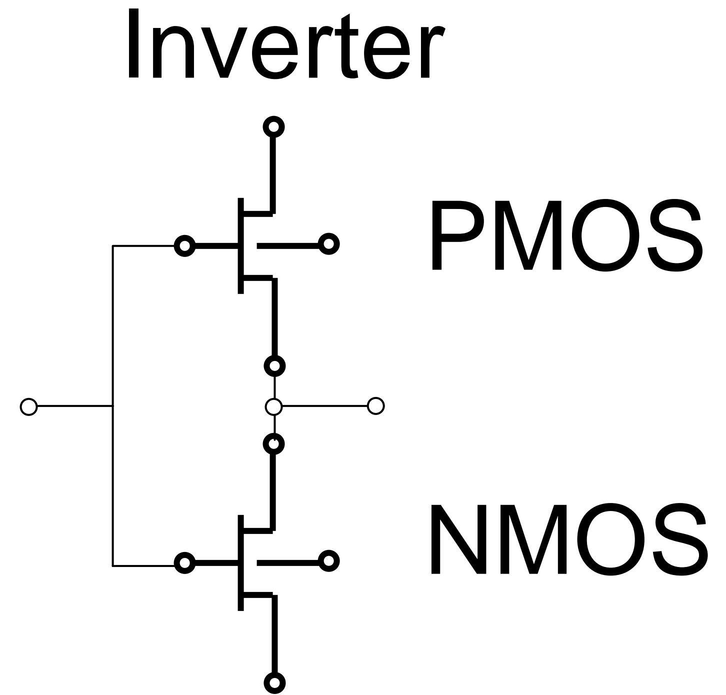
Si
Substrate

Channel

N-MOS (N-type MOSFET)

CMOS

Complimentary MOS



When NMOS is ON, PMOS is OFF

When PMOS is ON, NMOS is OFF

Needless to say, but….

CMOS Technology:

Indispensible for our human society

Al the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:

There is no computer in banks, and

world economical activities immediately stop.

Cellarer phone dose not exists

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

→ **Increase clock frequency**

→ **Increase circuit operation speed**

2. **Increase number of Transistors**

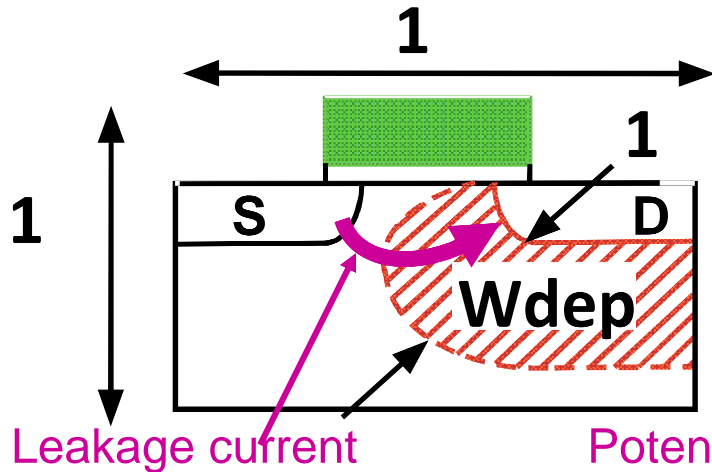
→ **Parallel processing**

→ **Increase circuit operation speed**

Downsizing contribute to the performance increase in double ways

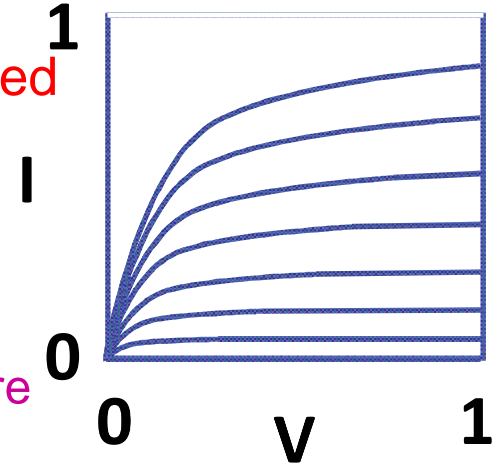
Thus, downsizing of Si devices is the most important and critical issue.

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

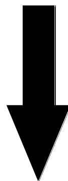
Wdep has to be suppressed
Otherwise, large leakage between S and D



Leakage current

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

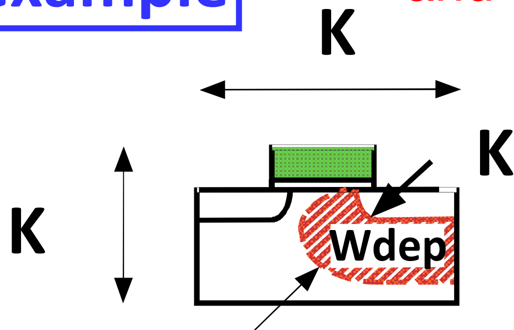
K=0.7 for example



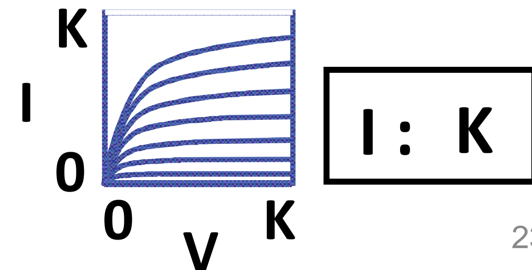
X , Y , Z : K,   V : K,   Na : 1/K

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$\text{Wdep} \propto \sqrt{V/Na}$$
: K



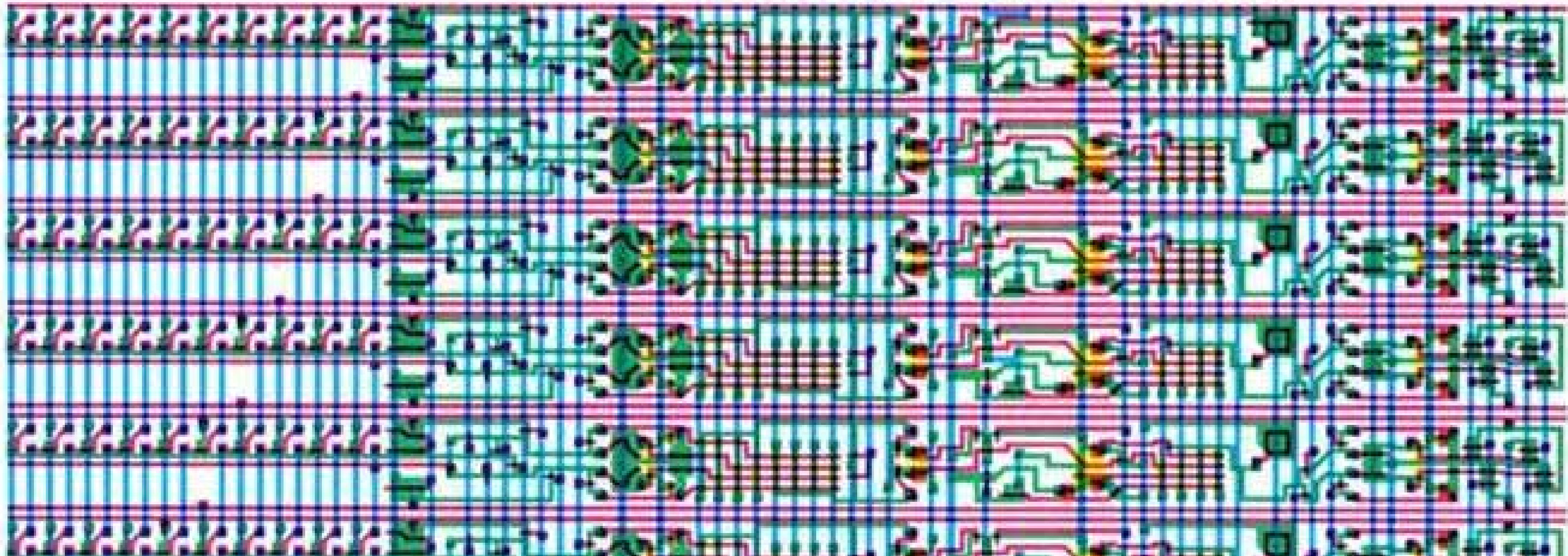
I : K

Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.

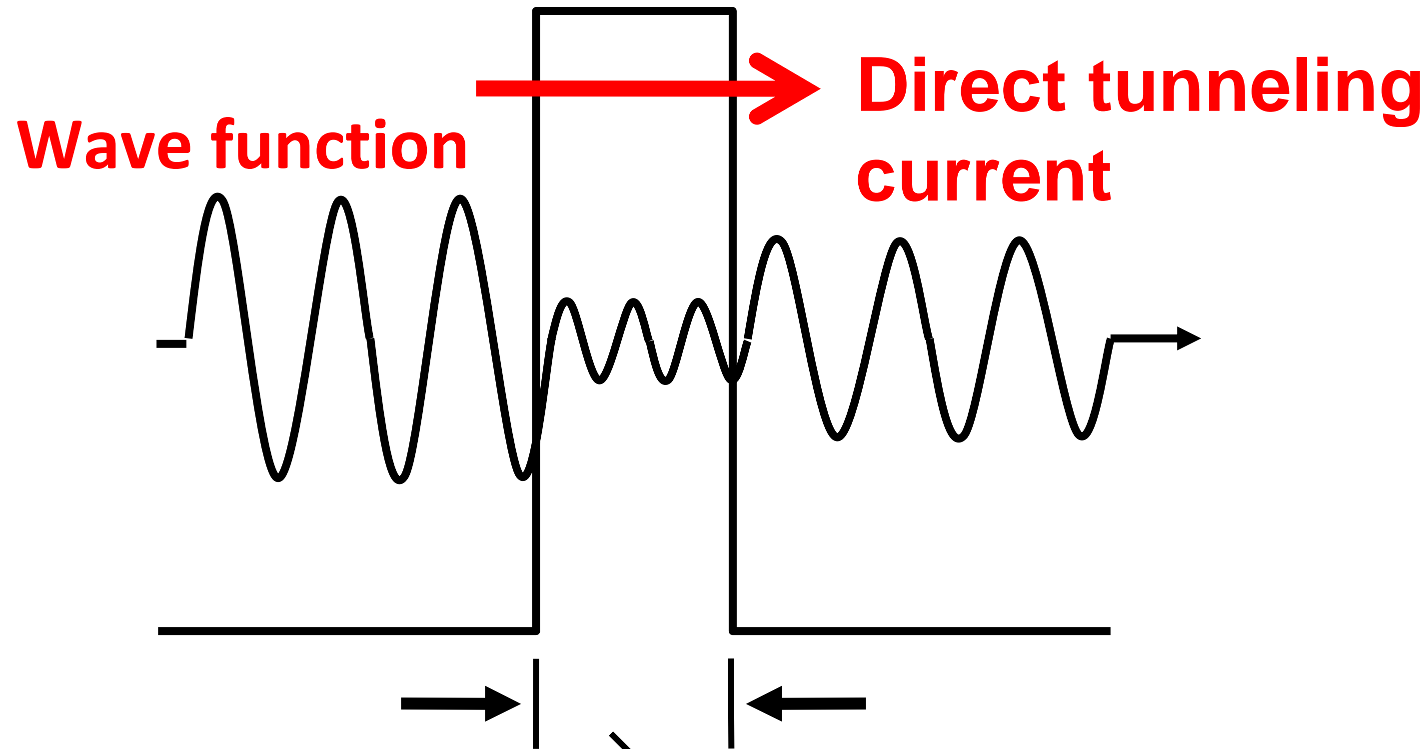


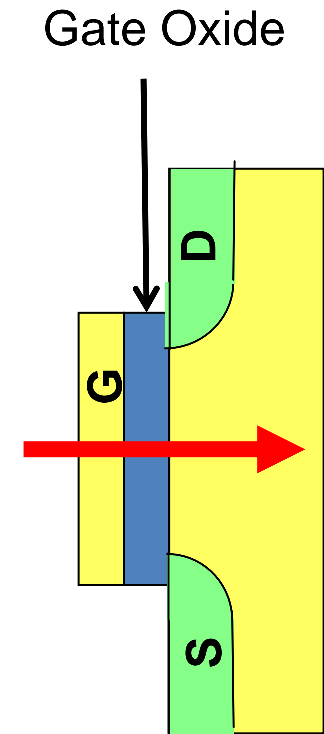
C. Mead L. Conway

VLSI textbook

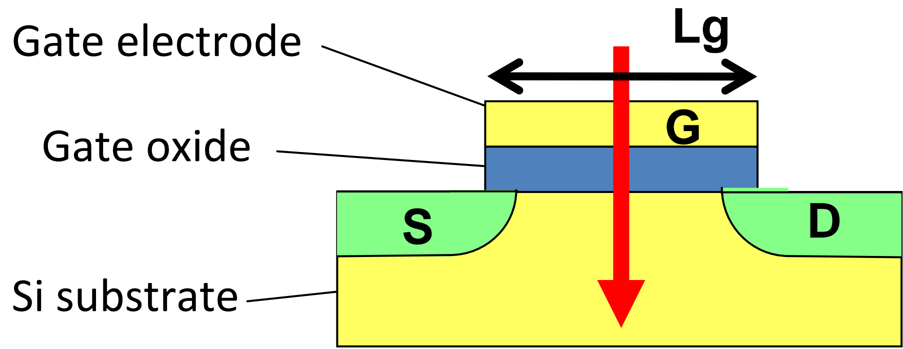
Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.

Direct-tunneling effect





Direct tunneling leakage current start to flow when the thickness is 3 nm.



Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide

Lg = 10 μm

0.03
0.02
0.01
0.00
0.01
-0.4
Id (mA / μm)
Vg = 2.0V
1.5 V
1.0 V
0.5 V
0.0 V
0.0 0.5 1.0 1.5
Vd (V)

Lg = 5 μm

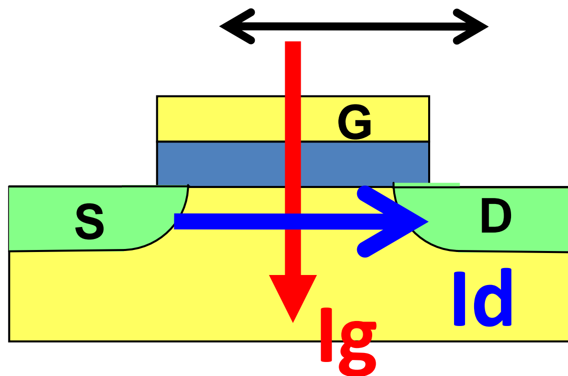
0.08
0.06
0.04
0.02
0.00
-0.02
Vg = 2.0V
1.5 V
1.0 V
0.5 V
0.0 V
0.0 0.5 1.0 1.5
Vd (V)

Lg = 1.0 μm

0.4
0.3
0.2
0.1
0.0
-0.1
Vg = 2.0V
1.5 V
1.0 V
0.5 V
0.0 V
0.0 0.5 1.0 1.5
Vd (V)

Lg = 0.1μm

1.6
1.2
0.8
0.4
0.0
-0.4
Vg = 2.0V
1.5 V
1.0 V
0.5 V
0.0 V
0.0 0.5 1.0 1.5
Vd (V)



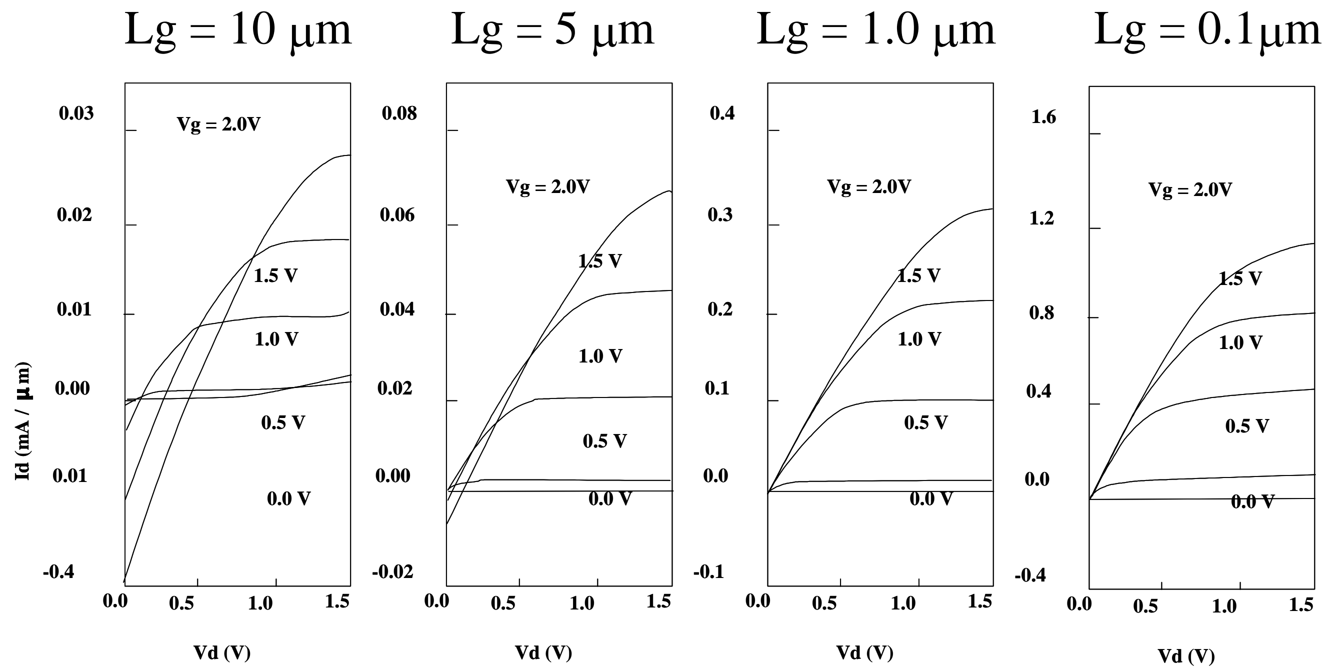
Gate leakage: Ig $\propto$ Gate Area $\propto$ Gate length (Lg)

Drain current: Id $\propto$ 1/Gate length (Lg)

Lg → small,

Then, Ig → small, Id → large, Thus, Ig/Id → very small

Id



Do not believe a text book statement, blindly!

Never Give Up!

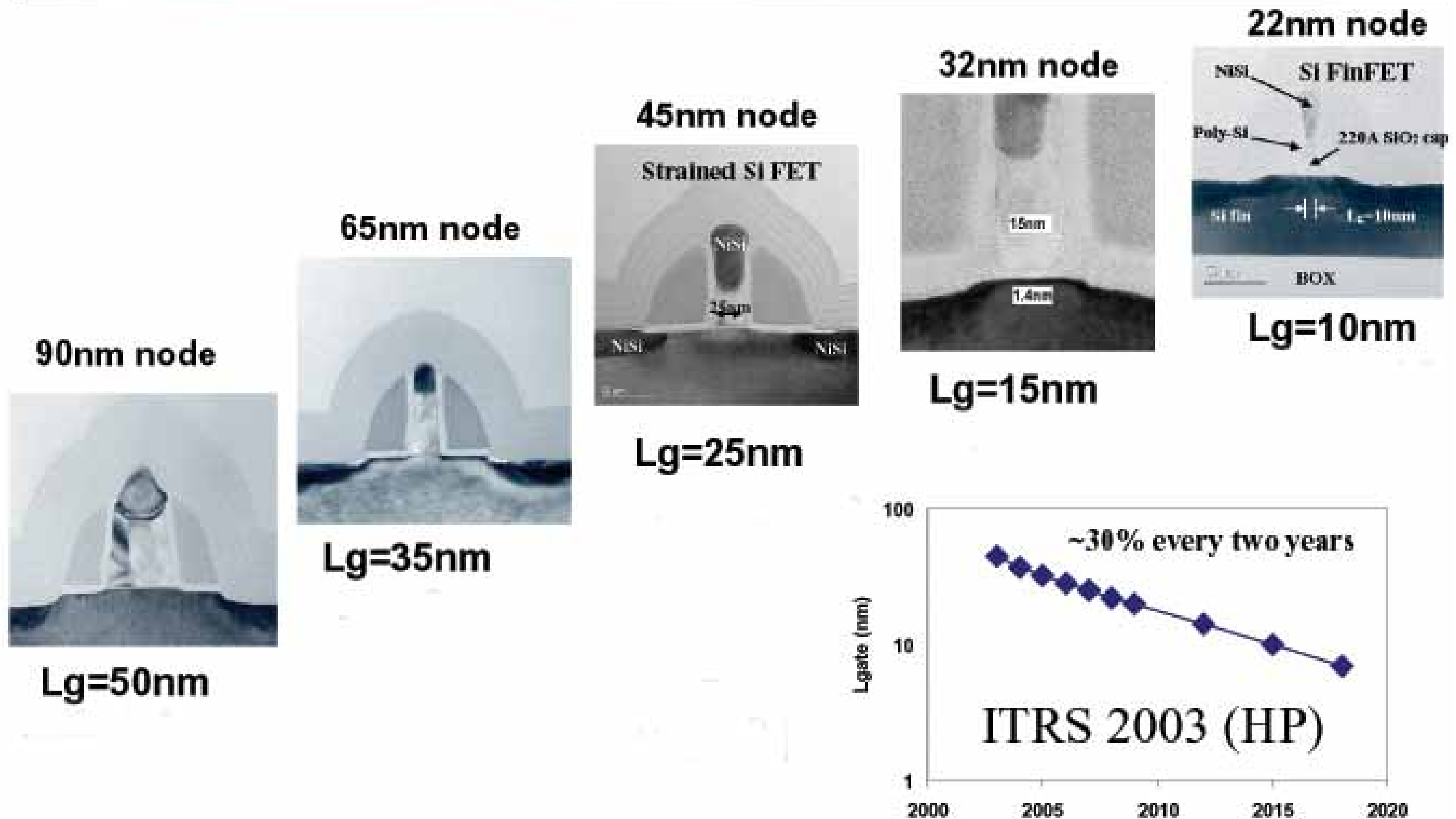
No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!
Some one will think for you

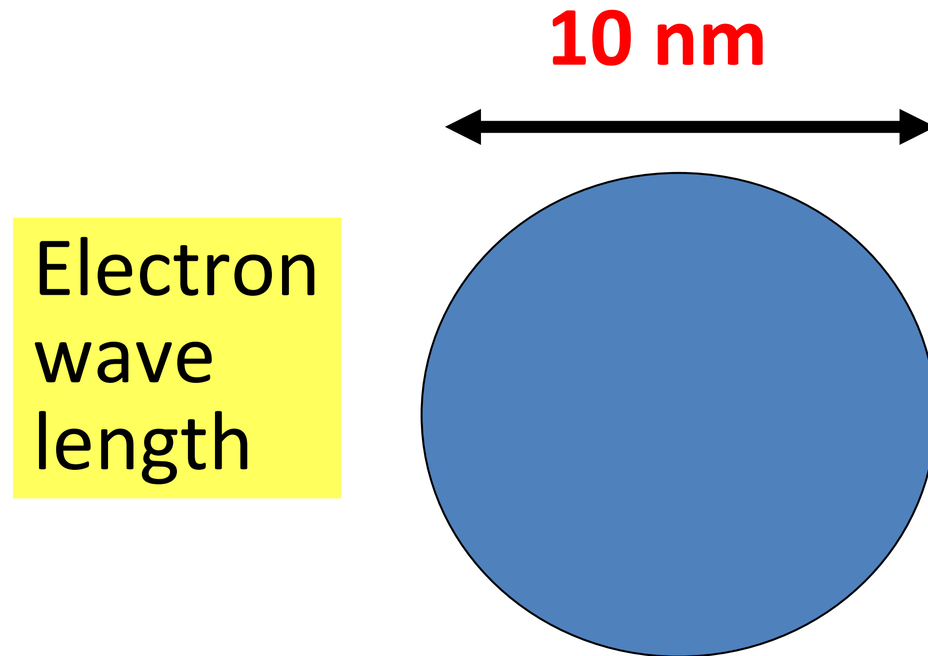
Transistor Scaling Continues

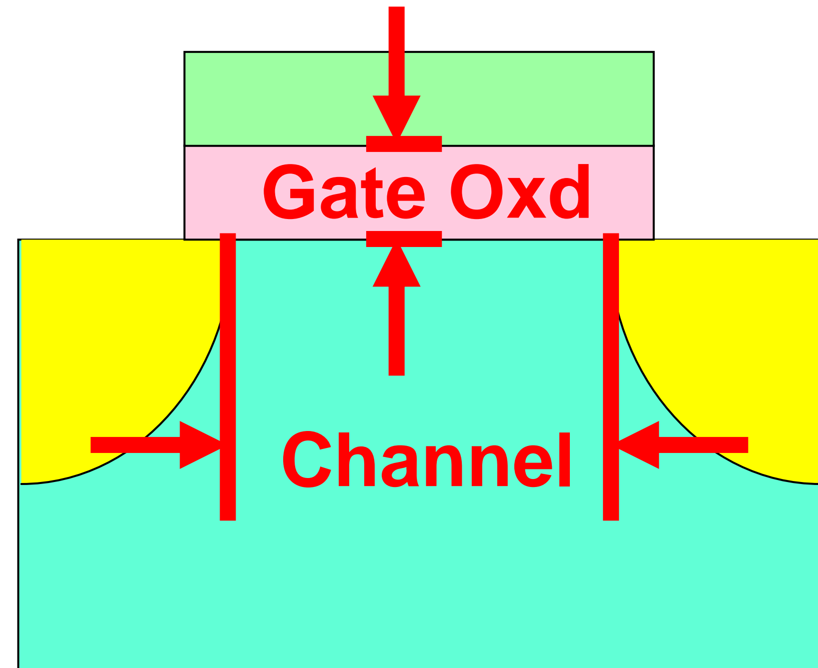


Qi Xinag, ECS 2004, AMD

<u>Downsizing limit?</u>

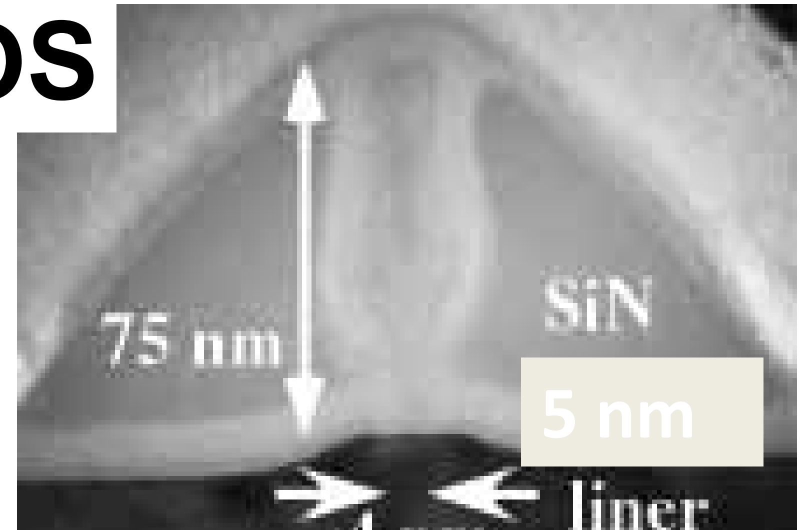
Channel length?



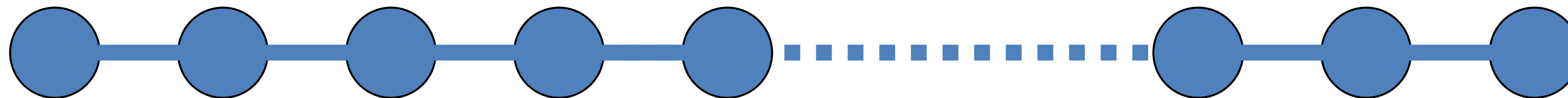


5 nm gate length CMOS

Is a Real Nano Device!!

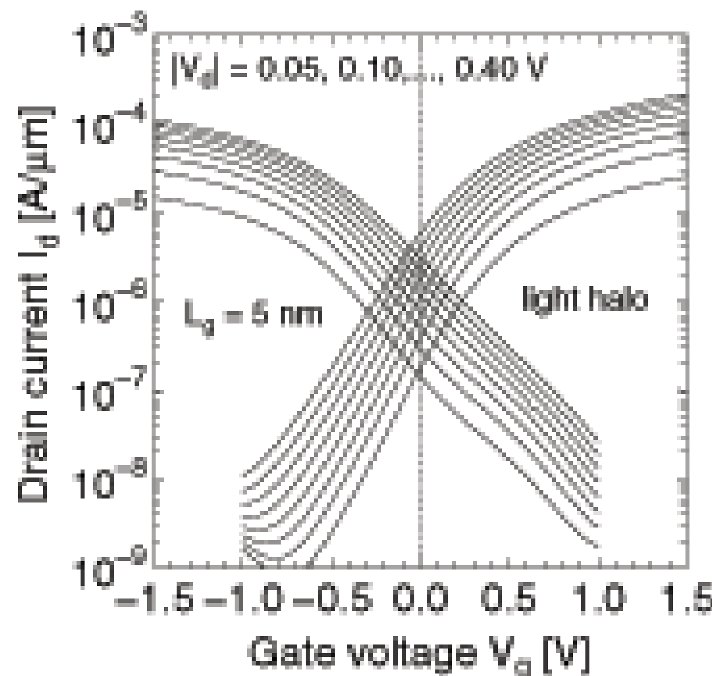


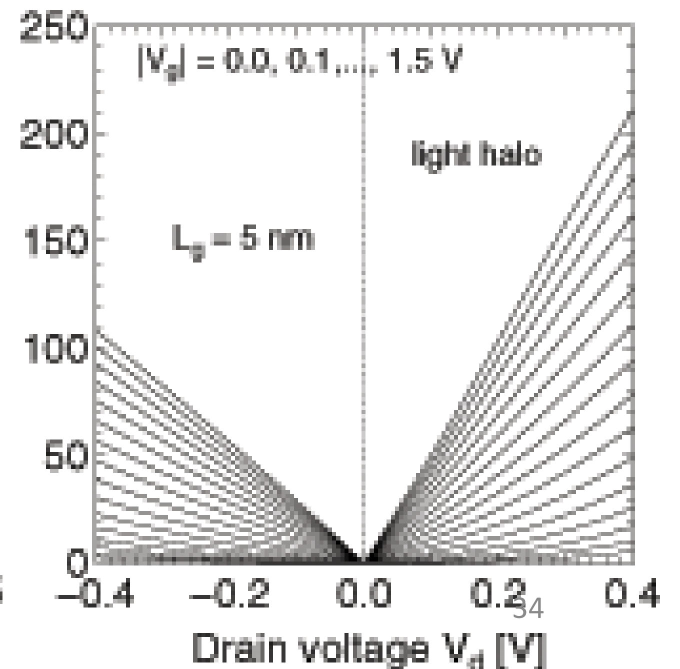
Length of 18 Si atoms



H. Wakabayashi
et.al, NEC

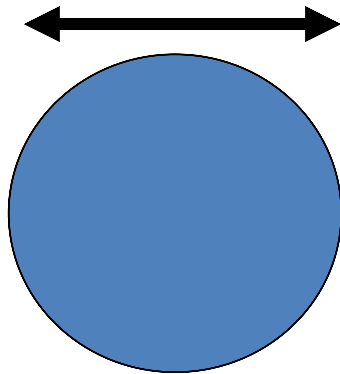
IEDM, 2003





Electron wave length

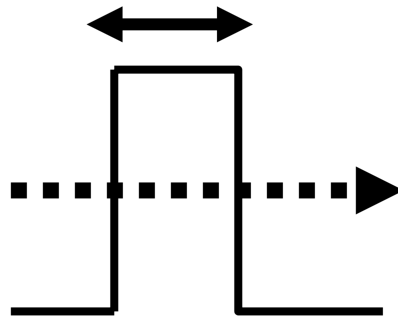
10 nm



Downsizing limit!

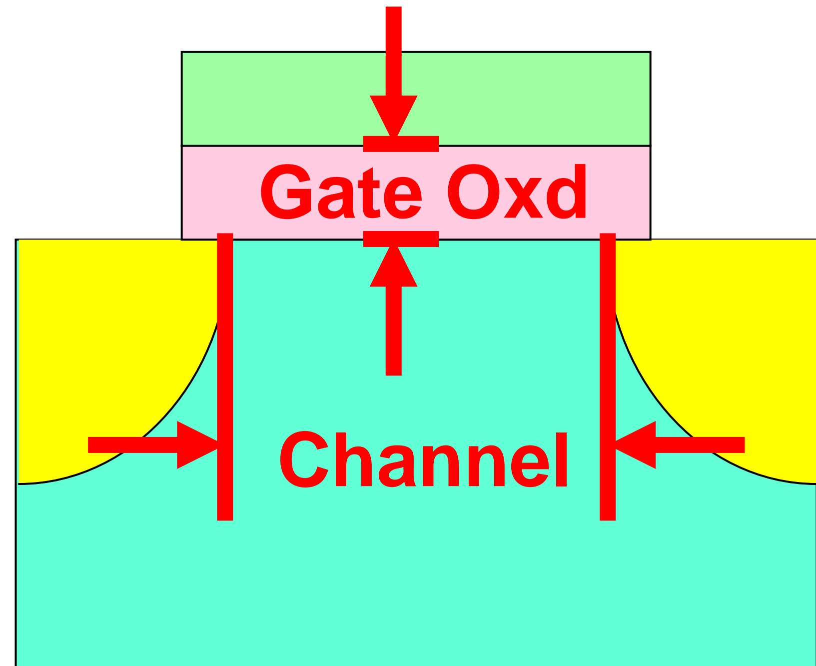
Channel length

Gate oxide thickness



Tunneling distance

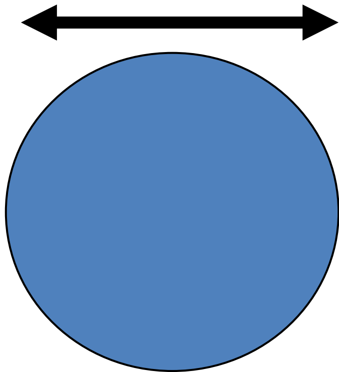
3 nm



Prediction now!

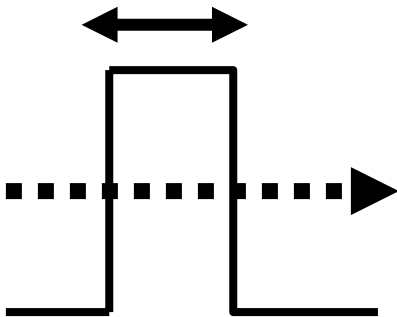
Electron wave length

10 nm



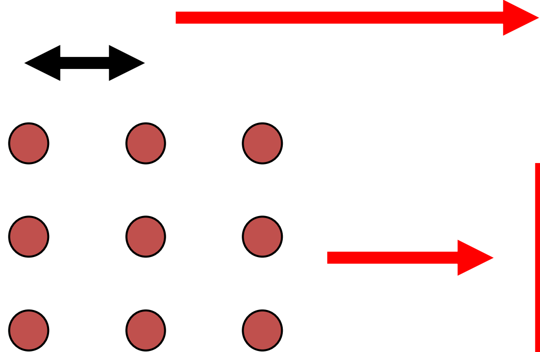
Tunneling distance

3 nm



Atom distance

0.3 nm

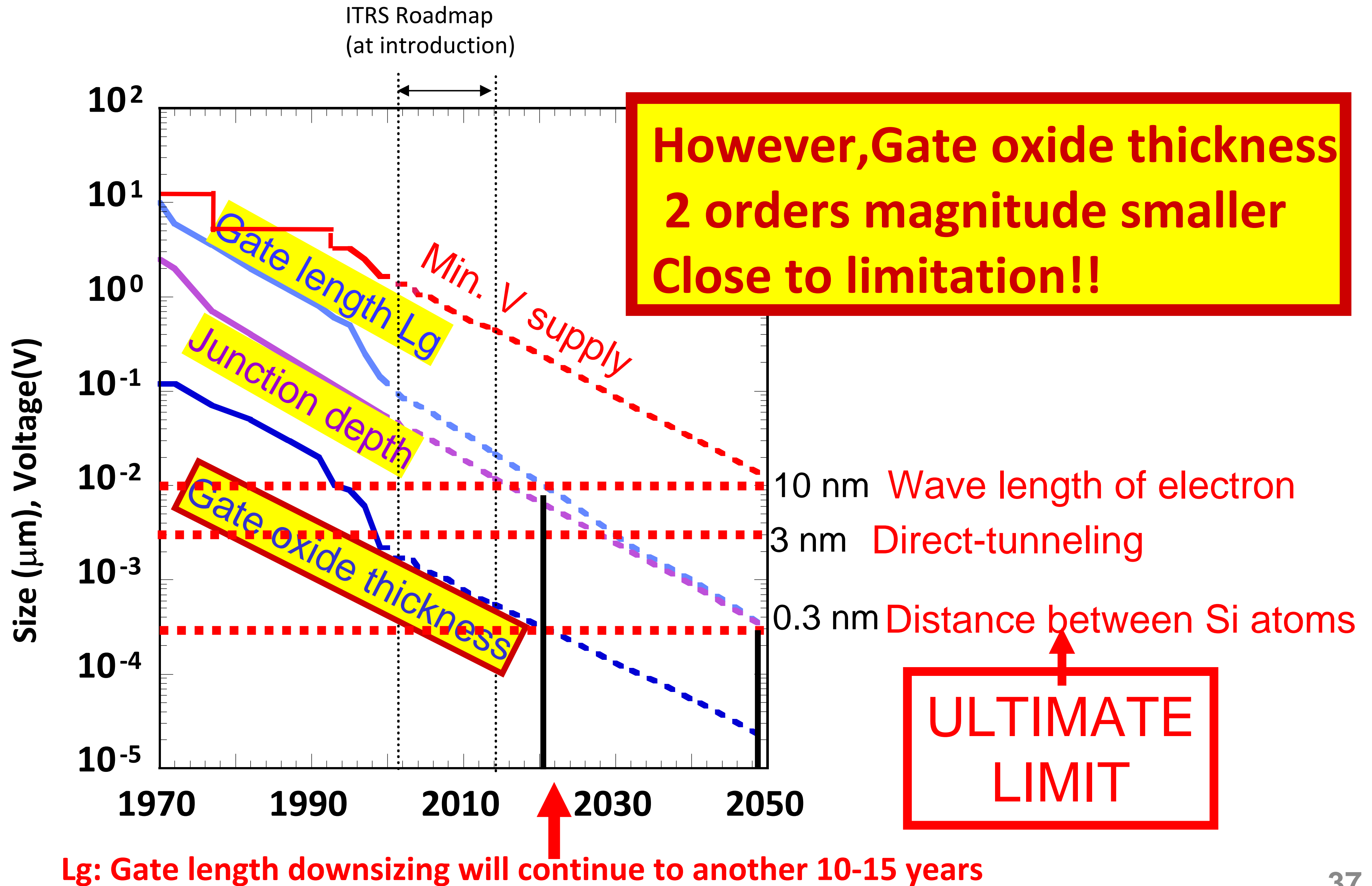


MOSFET operation

Lg = 2 ~ 1.5 nm?

Below this, no one knows future!

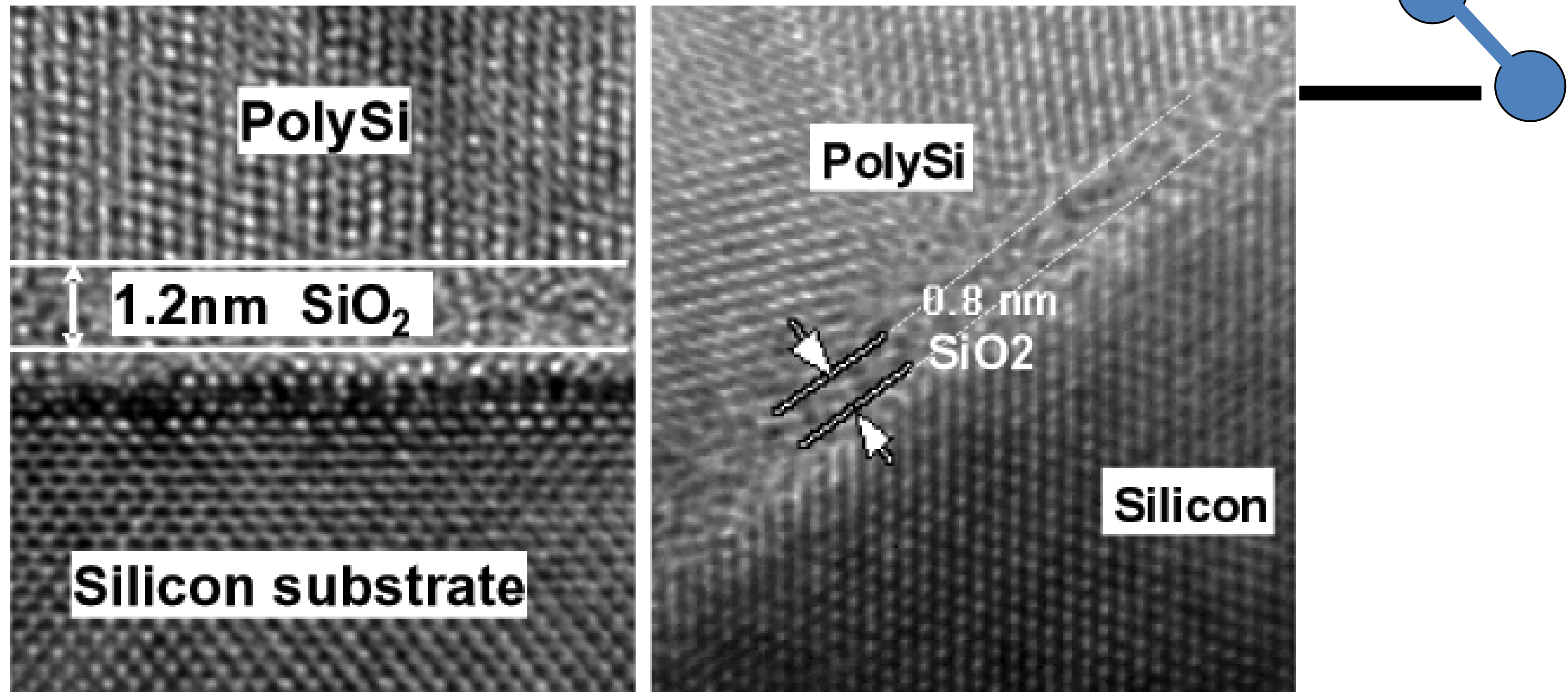
Ultimate limitation



Lg: Gate length downsizing will continue to another 10-15 years

0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!



- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

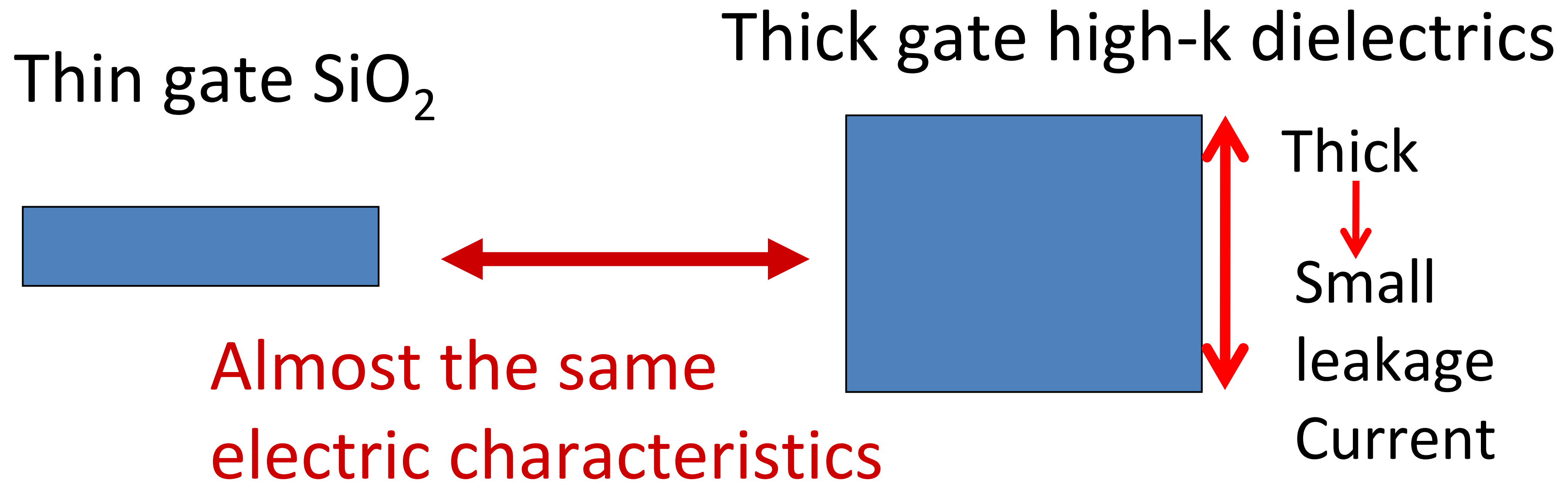
By Robert Chau, IWGI 2003

So, we are now in the limitation of downsizing?

Do you believe this or do not?

There is a solution! K: Dielectric Constant

To use high-k dielectrics



However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO_2!

Choice of High-k elements for oxide

Candidates (shaded)

● Gas or liquid at 1000 K

○ Radio active

Unstable at Si interface

① Si + MO_X M + SiO_2

② Si + MO_X MSi_X + SiO_2

③ Si + MO_X M + MSi_XO_Y

● H   ● He

Li Be   ● B ● C ● N ● O ● F ● Ne

① Na Mg   Al Si ● P ● S ● Cl ● Ar

K Ca Sc ② Ti ① V ① Cr ① Mn ① Fc ① Co ① Ni ① Cu ① Zn ① Ga ① Ge ● As ● Se ● Br ● Kr

● Rh Sr Y Zr ① Nb ① Mo Tc ① Ru ① Rb ① Pd ● Ag ① Cd ① In ① Sn ① Sb ① Te ● I ● Xe

● Cs ③ Ba ★ Hf ① Ta ① W ① Re ① Os ① Ir ● Pt ● Au ● Hg ● Tl ① Pb ① Bi ○ Po ○ At ○ Rn

○ Fr ○ Ra ☆ ○ Rf ○ Ha ○ Sg ○ Ns ○ Hs ○ Mt

★ La Ce Pr Nd ○ Pm Sm Eu Gd Tb Dy Ho Er Tm Yb Lu

☆ ○ Ac ○ Th ○ Pa ○ U ○ Np ○ Pu ○ Am ○ Cm ○ Bk ○ Cf ○ Es ○ Fm ○ Md ○ No ○ Lr

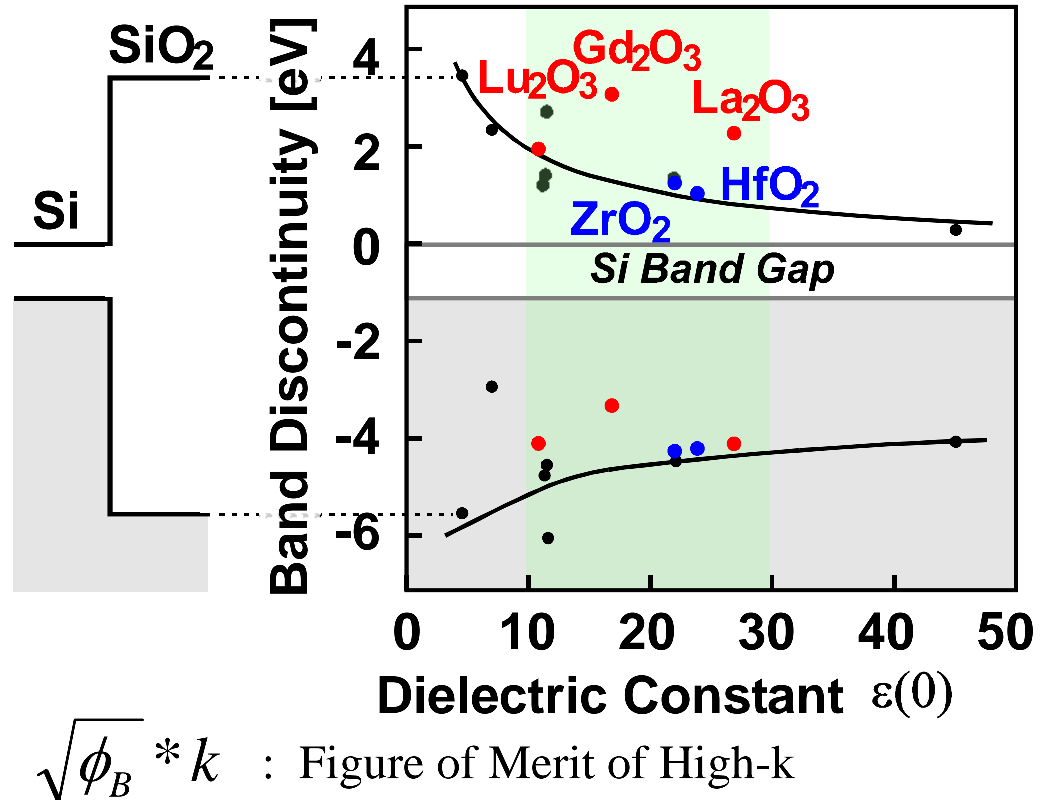
HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

Dielectric constant value vs. Band offset (Measured)

Material	Dielectric constant
SiO_2	3.9
Al_xSi_yOz	
$(Ba,Sr)TiO_3$	200-300
$BeAl_2O4$	8.3-9.43
CeO_2	16.6-26
$CeHfO_4$	10-20
$CoTiO_3/Si_3N_4$	
$EuAlO_3$	22.5
HfO_2	26-30
Hf silicate	11
La_2O_3	20.8
$LaScO_3$	30
La_2SiO_5	
$MgAl_2O_4$	
$NdAlO_3$	22.5
$PrAlO_3$	25
Si_3N_4	7
$SmAlO_3$	19
$SrTiO_3$	150-250
Ta_2O_5	25-24
$Ta_2O_5-TiO_2$	
TiO_2	86-95
TiO_2/Si_3N_4	
Y_2O_3	8-11.6
$Y_xSi_yO_z$	
ZrO_2	22.2-28
Zr-Al-O	
Zr silicate	
$(Zr,Sn)TiO_4$	40-60



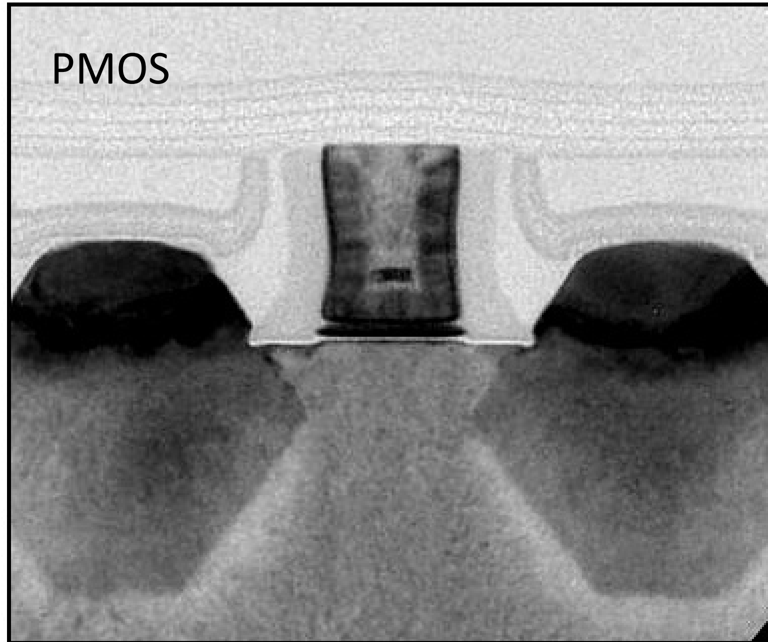
$\sqrt{\phi_B} * k$: Figure of Merit of High-k

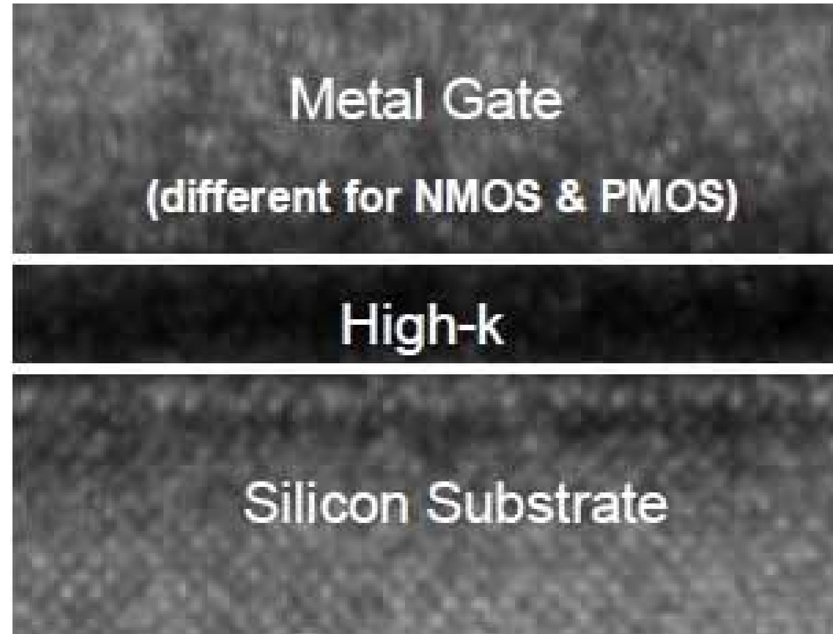
C.A. Billmann et al.,, MRS Spring Symp., 1999,
R.D.Shannon, J. Appl. Phys., 73, 348, 1993
S. De Gebdt, IEDM Short Coyuse, 2004

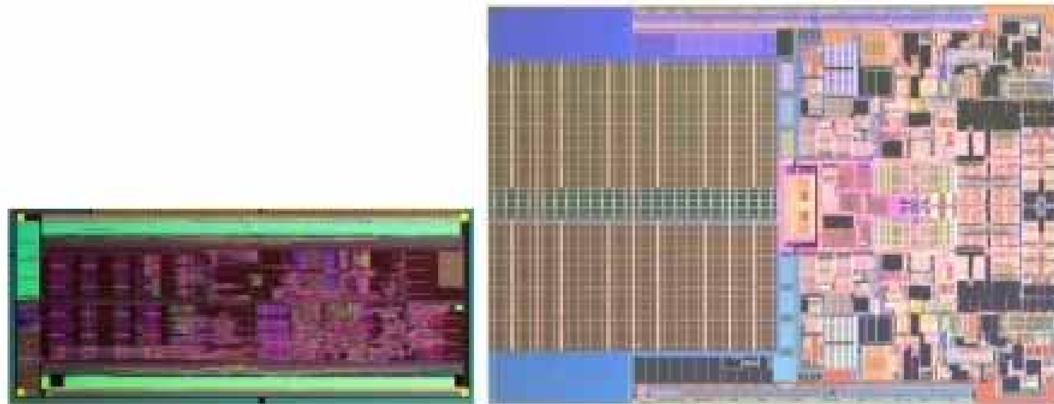
T. Hattori, INFOS , 2003

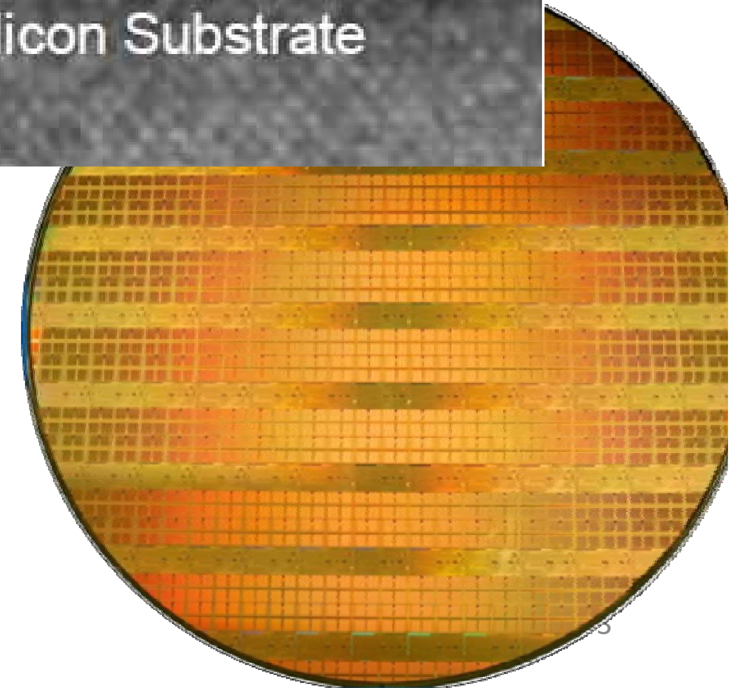
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness

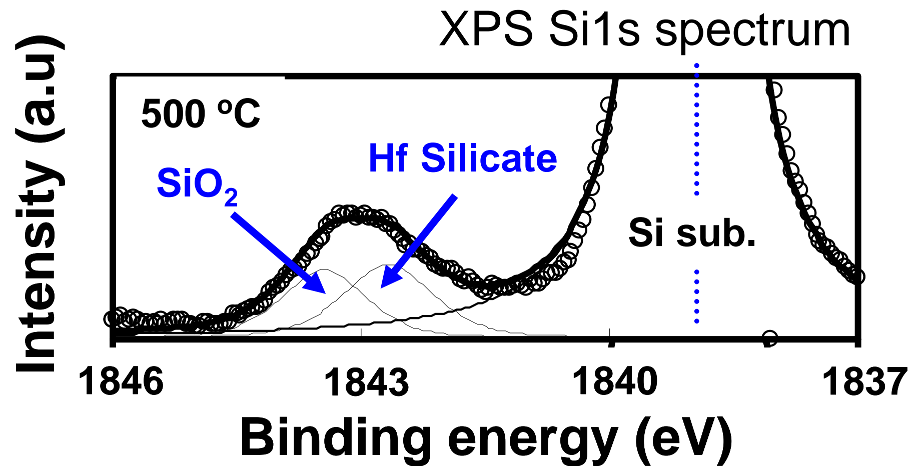




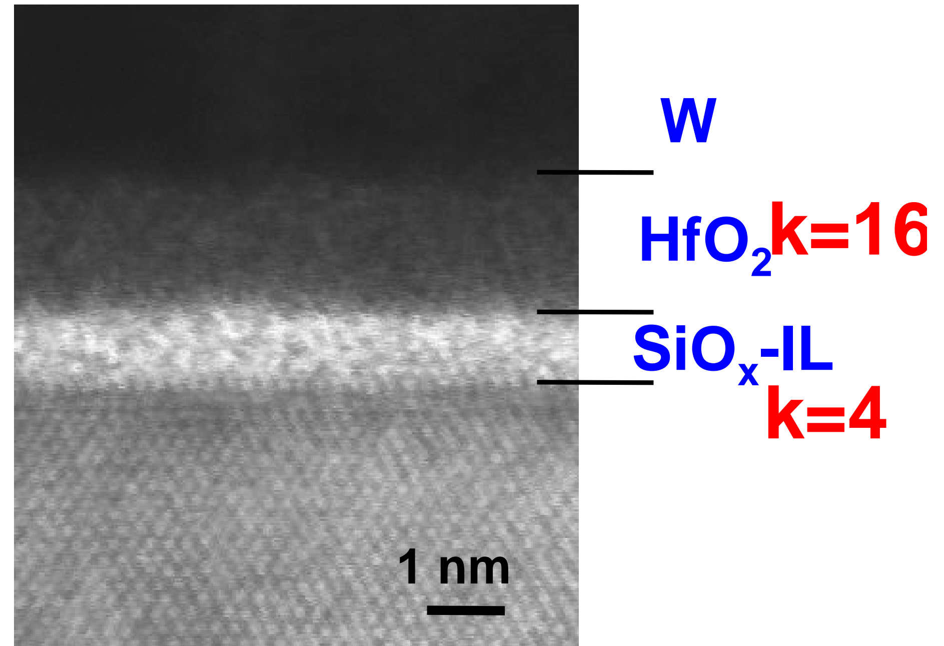




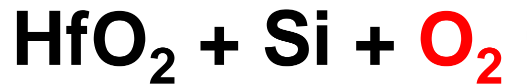
SiO_x-IL growth at HfO_2/Si Interface

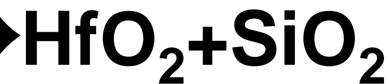


TEM image 500 °C 30min



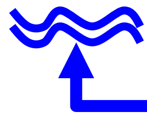
Phase separator





$$HfO_2 + Si + O_2 \rightarrow HfO_2 + Si + 2O^* \rightarrow HfO_2 + SiO_2$$

H. Shimizu, JJAP, 44, pp. 6131



Oxygen supplied from W gate electrode

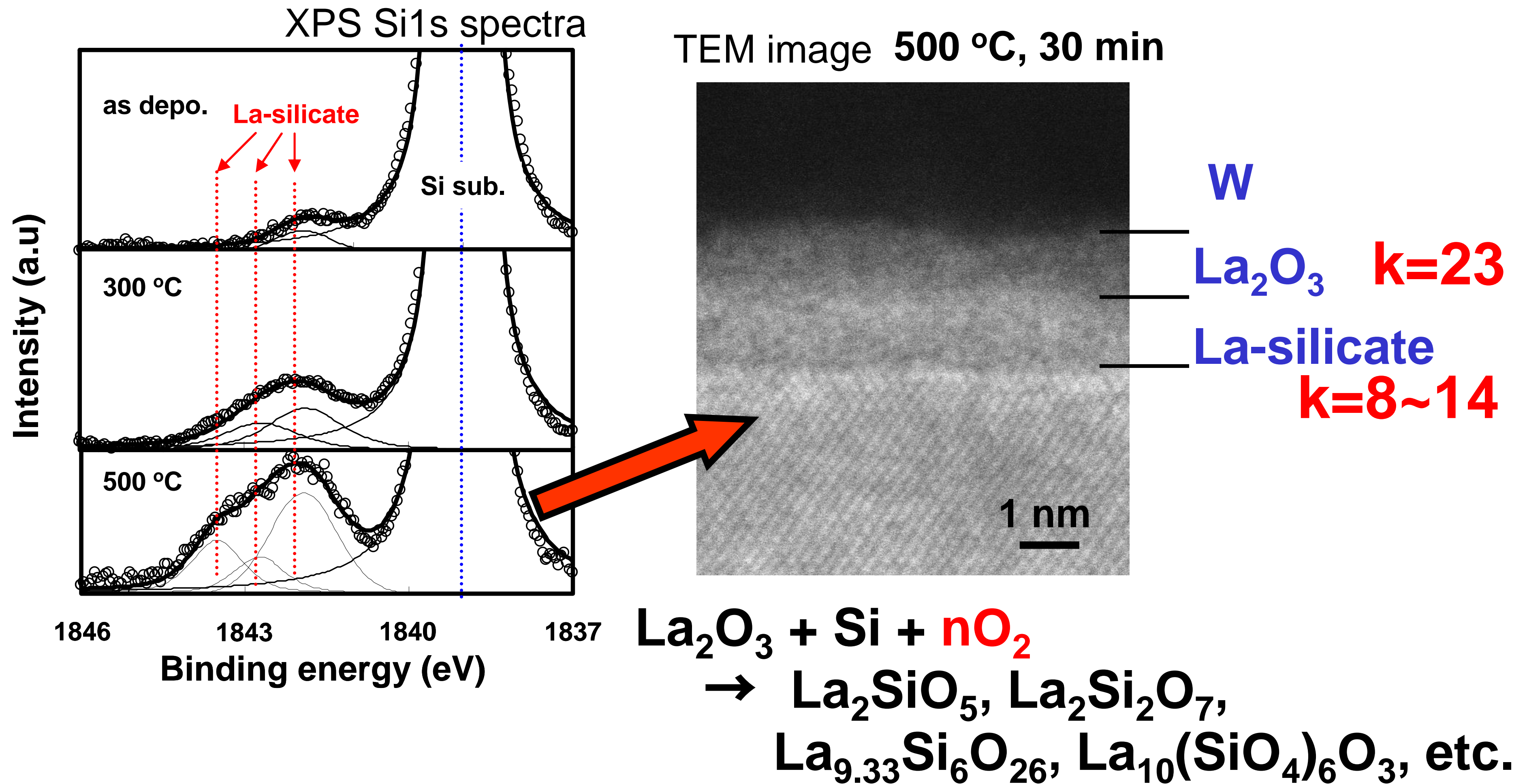
D.J.Lichtenwalner, Tans. ECS 11, 319

SiO_x-IL is formed after annealing

Oxygen control is required for optimizing the reaction

La-Silicate Reaction at La_2O_3/Si

Direct contact high-k/Si is possible

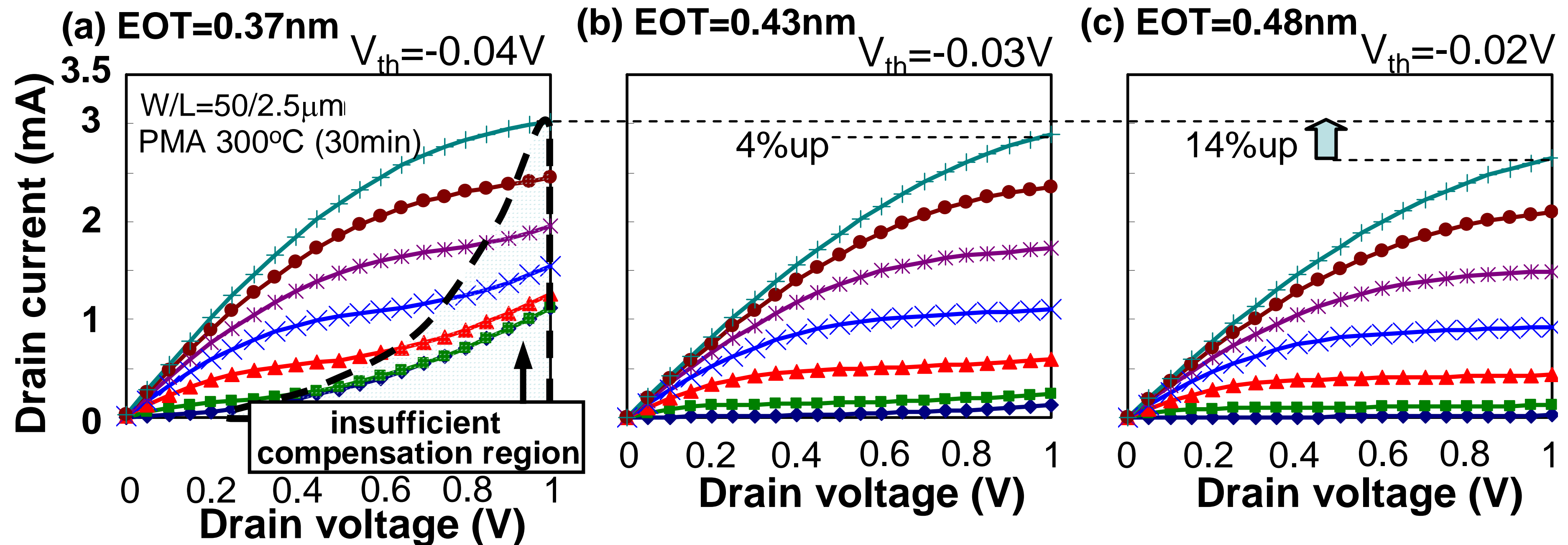


La_2O_3 + Si + nO_2

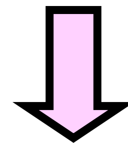
→ La_2SiO_5, $La_2Si_2O_7$, $La_{9.33}Si_6O_{26}$, $La_{10}(SiO_4)_6O_3$, etc.

La_2O_3 can achieve direct contact of high-k/Si

EOT<0.5nm with Gain in Drive Current



14% of I_d increase is observed even at saturation region



EOT below 0.4nm is still useful for scaling

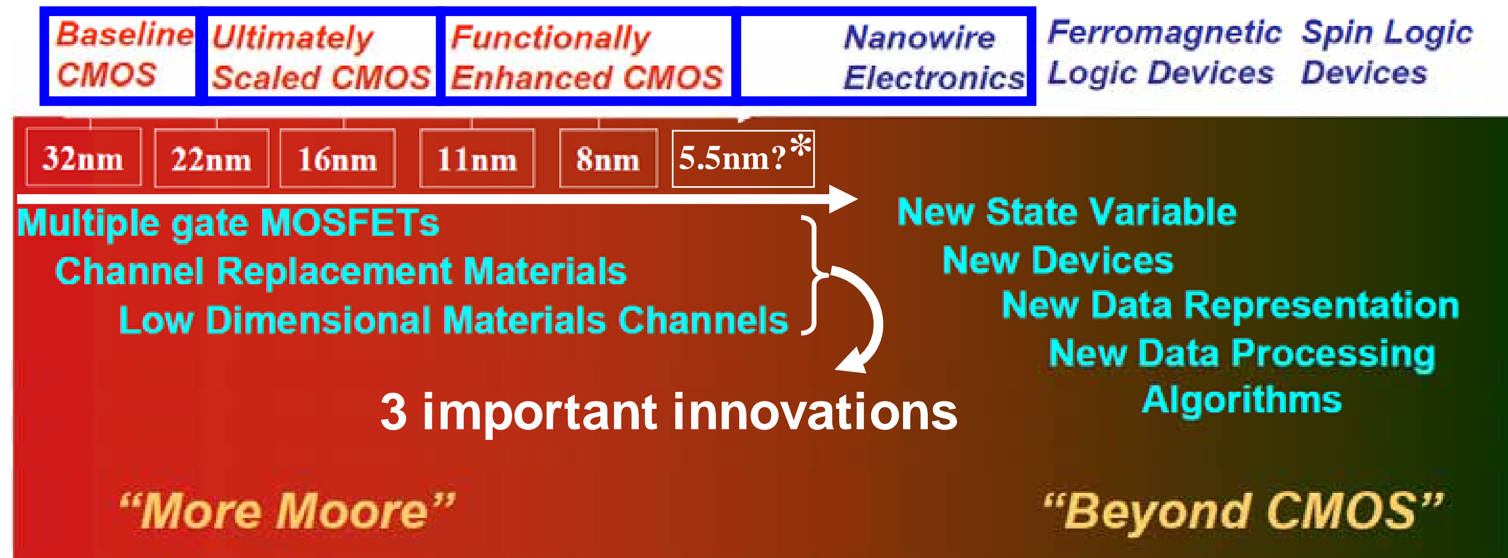
-There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

-Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

-Two candidates have emerged for R & D

1. Nanowire/tube MOSFETs
2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.

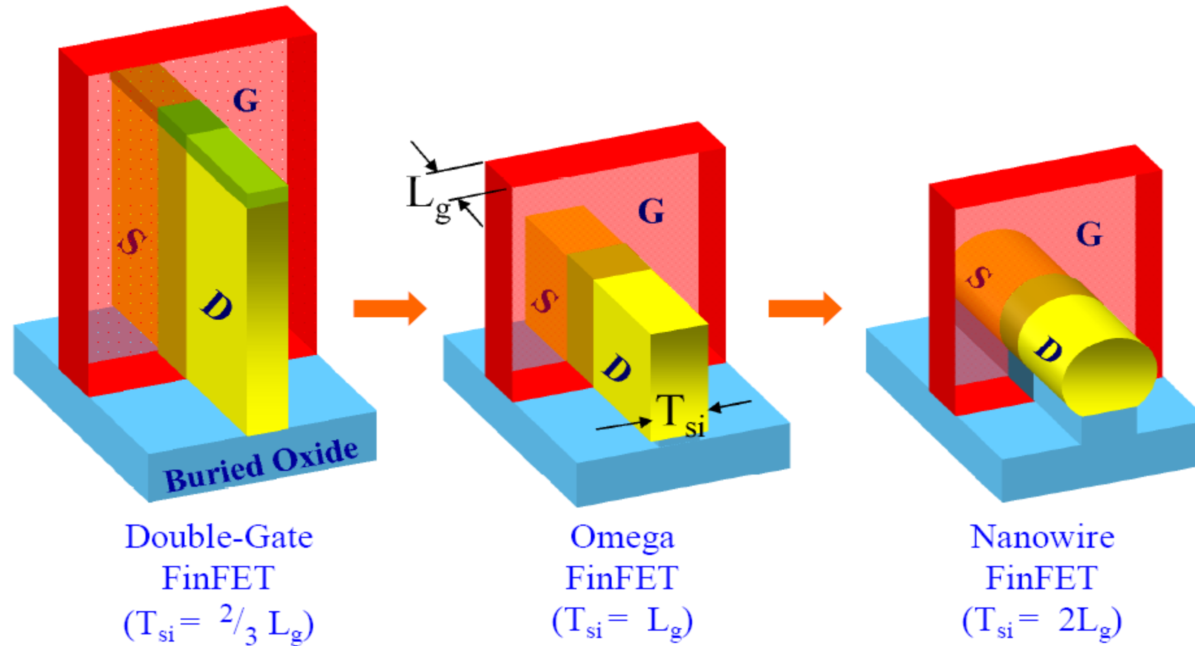


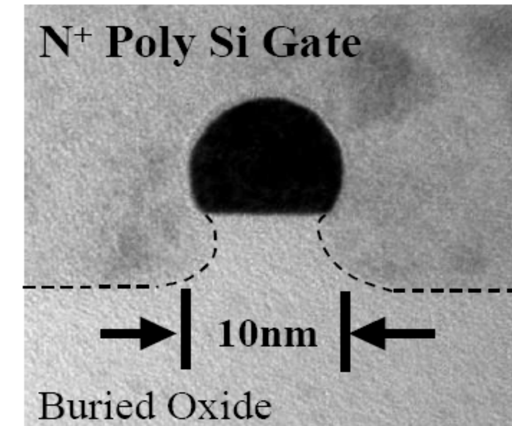
ITRS figure edited by Iwai

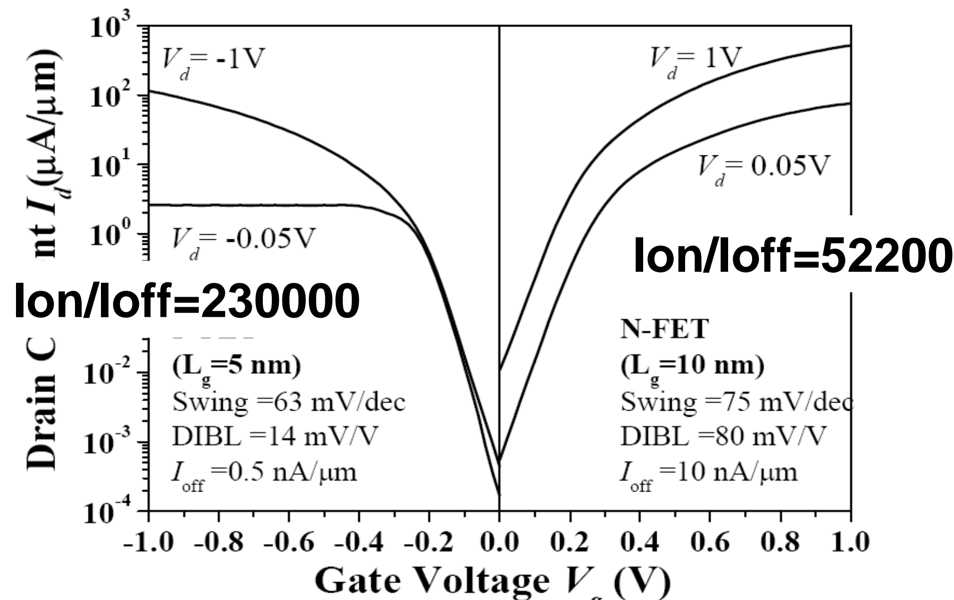
Source: 2008 ITRS Summer Public Conf.

*5.5nm? was added by Iwai

FinFET to Nanowire







Ion/Ioff=230000

Ion/Ioff=52200

Channel conductance is well controlled by Gate even at L=5nm

F.-L.Yang, VLSI2004

Si nanowire FET as a strong candidate after CMOS limitation

1. Compatibility with current CMOS process

2. Good controllability of I_{OFF}

3. High drive current