Future nanoelectronic device technologies - high-k, nanowire and alternative channel

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Tokyo Institute of Technology
Frontier Research Center

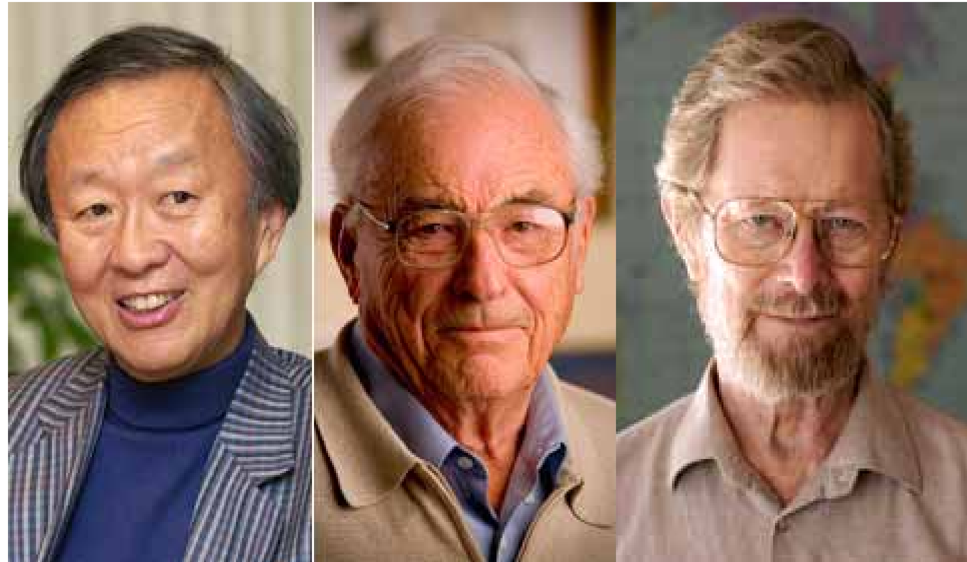
Hiroshi Iwai

Last year is a great year for Electron/Opt Devices!

By Dr. Lu Terman, at IEDM 2009

Three IEEE Fellows Win 2009 Nobel Prize in Physics

"... for breakthroughs involving the transmission of light in fiber optics and inventing an imaging semiconductor circuit, the three scientists created the technology behind digital photography and helped link the world through fiber-optic networks."



(l-r)
Dr. Charles K. Kao
Dr. Willard S. Boyle
Dr. George E. Smith

Nobel Prizes in Electron Devices

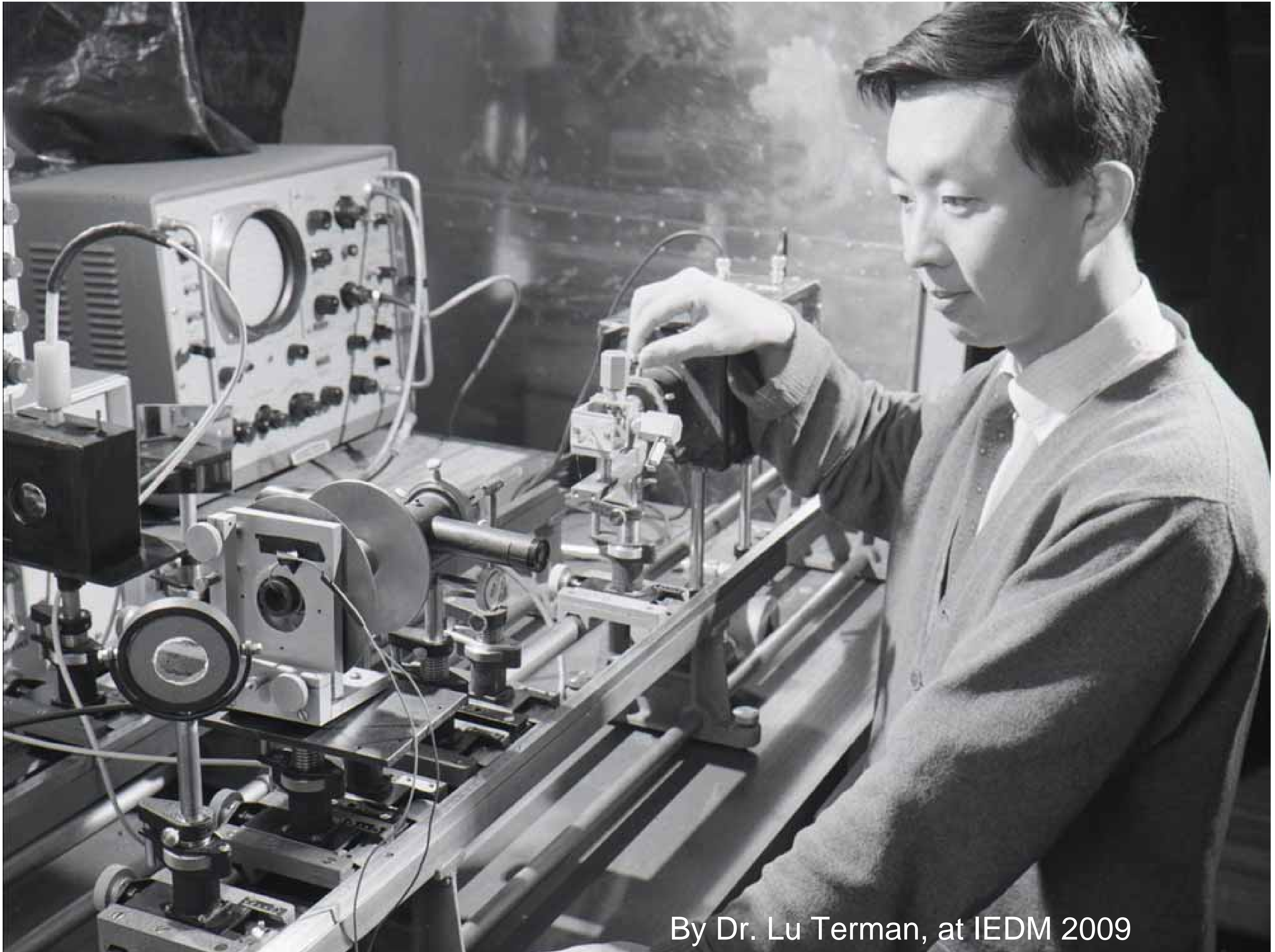
- **1956 – The Transistor**
  William Shockley, John Bardeen, and Walter Brattain
- **1973 – Tunneling Diode**
  Leo Esaki, Ivar Giaever

  – Josephson Junction
  Brian David Josephson
- **2000 – Integrated Circuit**
  Jack Kilby

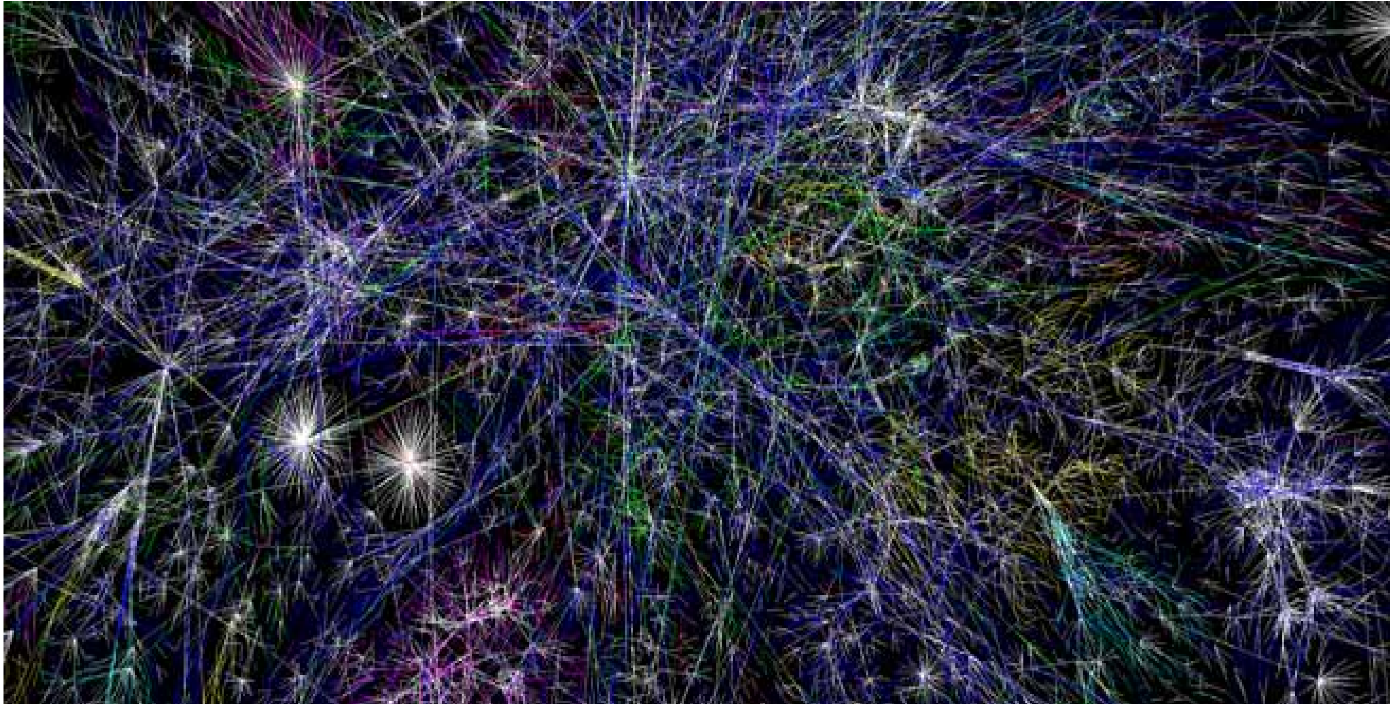
  – Semiconductor Heterojunction Devices
  Zohres Alferov and Herbert Kroemer
- **2007 – Giant Magnetoresistive Effect (GMR)**
  Albert Fert and Peter Grunberg
- **2009 – Charge Coupled Devices**
  George Smith and Willard Boyle

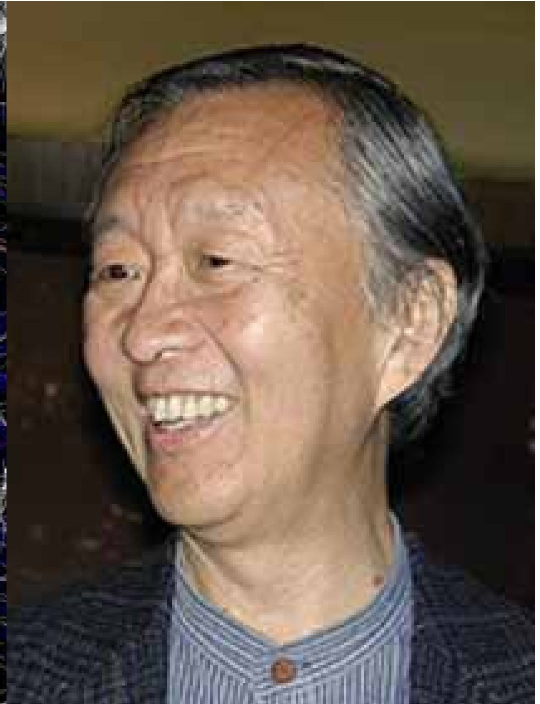
  – Fiber Optic Technology
  Charles Kao

By Dr. Lu Terman, at IEDM 2009

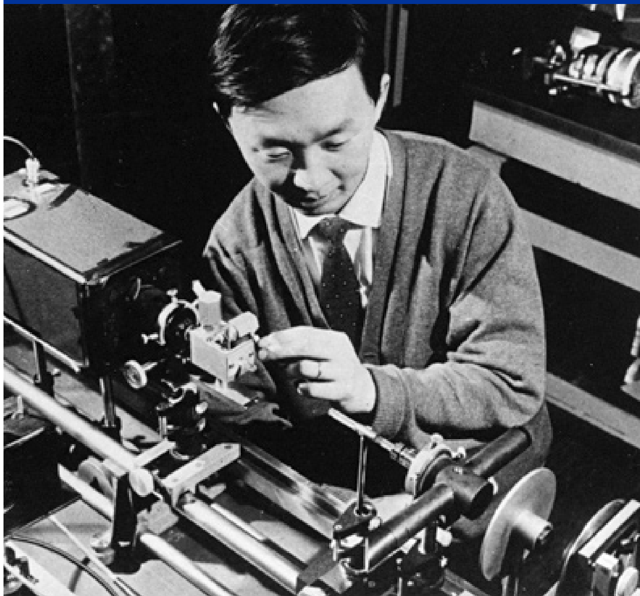


By Dr. Lu Terman, at IEDM 2009





Global Internet 2009



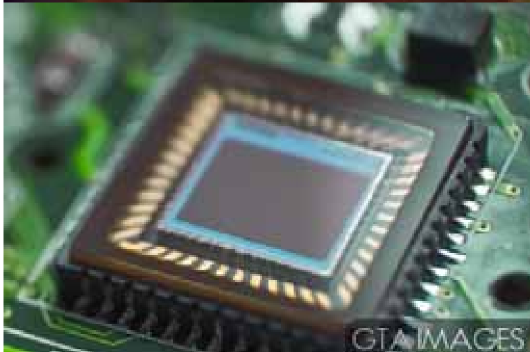
The Father of Fiber Optic Communication

By Dr. Lu Terman, at IEDM 2009

By Dr. Lu Terman, at IEDM 2009

Willard S. Boyle
Bell Laboratories
Murray Hill, NJ, USA

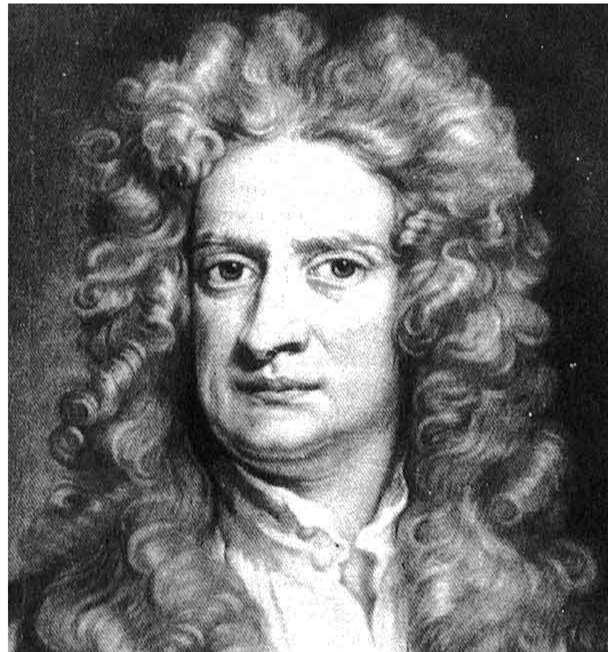
George E. Smith
Bell Laboratories
Murray Hill, NJ, USA



By Dr. Lu Terman, at IEDM 2009

Sir Isaac Newton

"If I can see so far, it is because I stand on the shoulders of giants"



By Dr. Lu Terman, at IEDM 2009

1. Scaling

10

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

→ **Increase clock frequency**

→ **Increase circuit operation speed**

2. **Increase number of Transistors**

→ **Parallel processing**

→ **Increase circuit operation speed**

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.

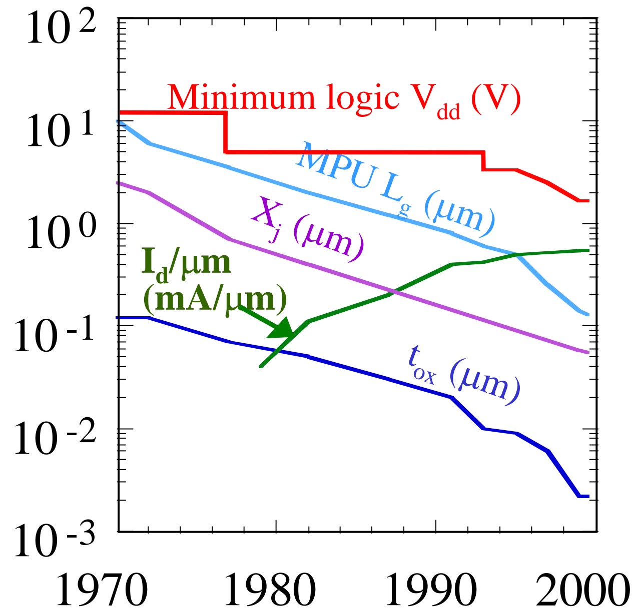
Downscaling merit: Beautiful!

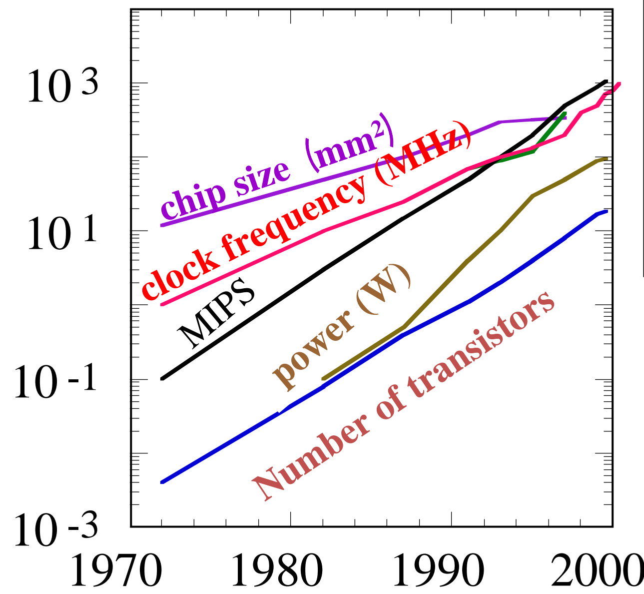
Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	**Scaling K : K=0.7 for example**
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o: gate C per unit area $\rightarrow W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox} \rightarrow KK/K = K$
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d \rightarrow KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α: Scaling factor $\rightarrow$ **In the past, $\alpha > 1$ for most cases**
Integration (# of Tr)	N	α/K^2	$N \rightarrow \alpha/K^2$ **$= 1/K^2$, when $\alpha=1$**
Power per chip	P	α	$fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha$ **= 1, when $\alpha=1$**

Scaling down approach is very beautiful and imprtant

2 Generations scaling	$k = 0.7^2 = 0.5$ if we keep the chip area the same for scaling
Single MOFET	Vdd → 0.5 Lg → 0.5 Id → 0.5 Cg → 0.5 P (Power)/Clock → $0.5^3 = 0.125$ τ (Switching time) → 0.5
Chip	N (# of Tr) → $1/0.5^2 = 4$ f (Clock) → $1/0.5 = 2$ P (Power) → 1

Actual past downscaling trend until year 2000





Source. Iwai and S. Ohmi, Microelectronics Reliability 42 (2002), pp.1251-1268

Past 30 years scaling

Merit: N, f increase

Demerit: P increase

V_{dd} scaling insufficient

⇩

Additional significant increase in I_d, f, P

Change in 30 years

	Ideal scaling	Real Change		Ideal scaling	Real Change		Ideal scaling	Real Change
L_g	K	10^{-2}	I_d	K (10^{-2})	10^{-1}	f	1/K(10^{2})	10^{3}
t_{ox}	K(10^{-2})	10^{-2}	I_d/μm	1	10^{1}	P = fαNCV²	α(10^{1})	10^{5}
V_{dd}	K(10^{-2})	10^{-1}	N	α/K²(10^{5})	10^{4}			
A_{chip}	α	10^{1}						

Vd scaling insufficient, α increased → N, Id, f, P increased significantly

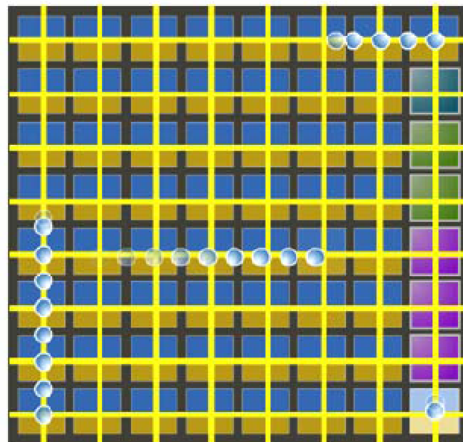
intel Leap ahead

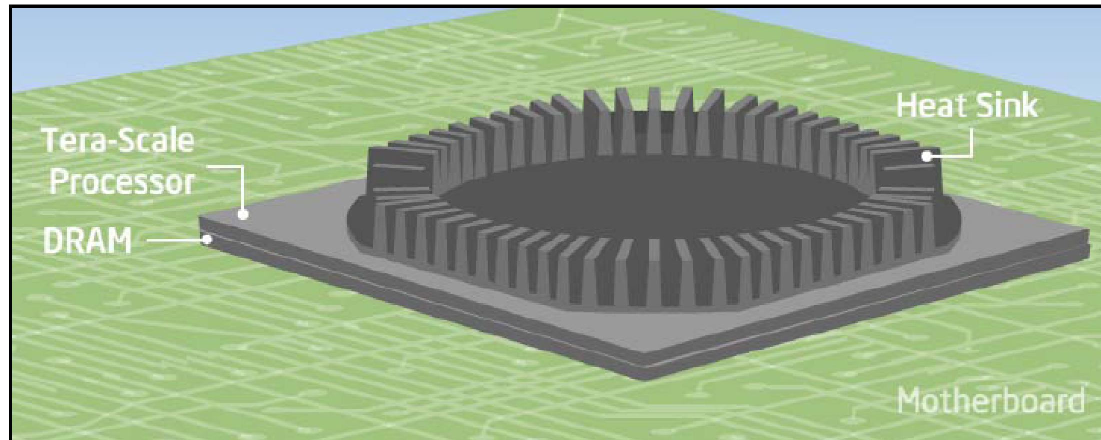
Tera-scale Research Prototype

Connecting 80 simple cores on a single test chip

Intel processors with two cores are here now and quad-core processors are right around the corner. In the coming years, the number of cores on a chip will continue to grow, launching an era of vastly more powerful computers. These are the machines that will deliver efficient teraflop performance with the capabilities needed to handle tomorrow's emerging applications. They must also scale to an increasing number of cores – perhaps 10s or even 100s of them.

This test chip represents Intel's first tera-scale research prototype silicon. The purpose of the prototype is to develop a design methodology appropriate for tera-scale computing by using a tiled approach. Each tile includes a small core, or compute element, with a few simple instructions that can generate data, and a router that connects each tile to adjacent tiles and to 3D stacked memory that will be added in the future. The prototype consists of 80 tiles in an 8x10 array with an on-chip interconnect fabric.





The key technologies of this first Tera-scale Research Prototype are a mesh interconnect (left) and support for 3D stacked memory (above).

- The concerns for limits of down-scaling have been announced for every generation.

- However, down-scaling of CMOS is still the 'royal road'* for high performance and low power.

- Effort for the down-scaling has to be continued by all means.

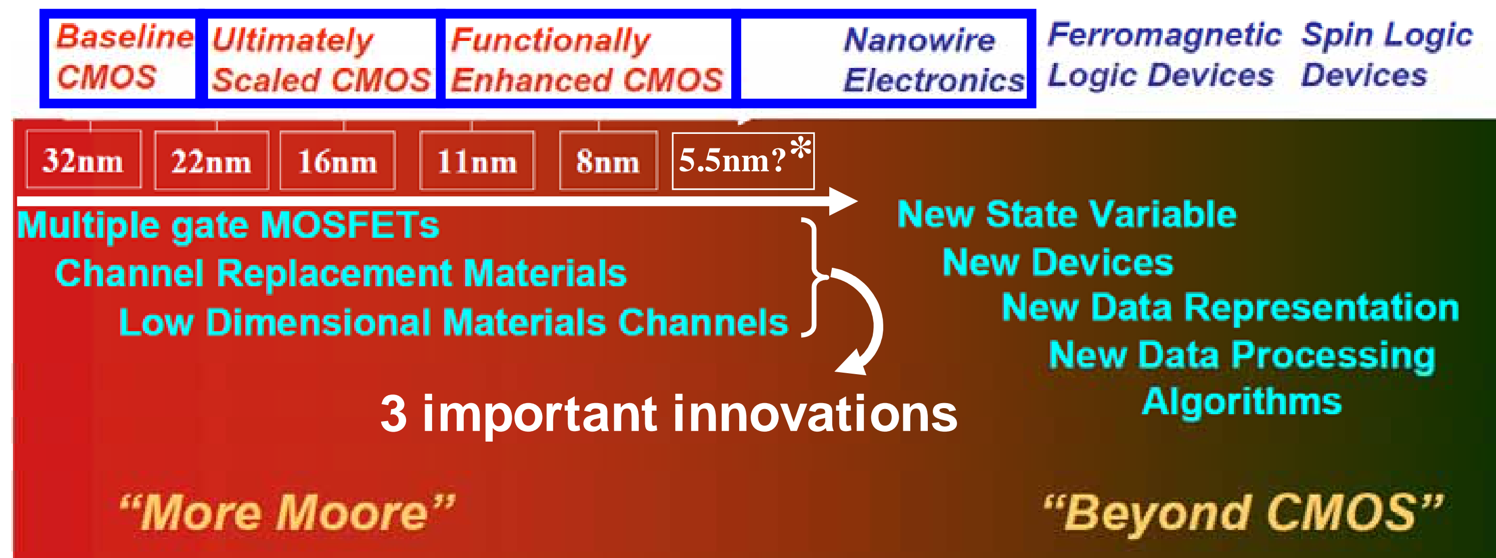
-There will be still 4~6 generations left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

-Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

-Three important technologies

1. High-k/metal gate stack with <0.5nm EOT, Silcide S/D
2. Si Nanowire MOSFETs
3. Alternative channel MOSFETs (III-V, Ge), maybe nanowire

- Other Beyond CMOS devices are still in the cloud.



ITRS figure edited by Iwai

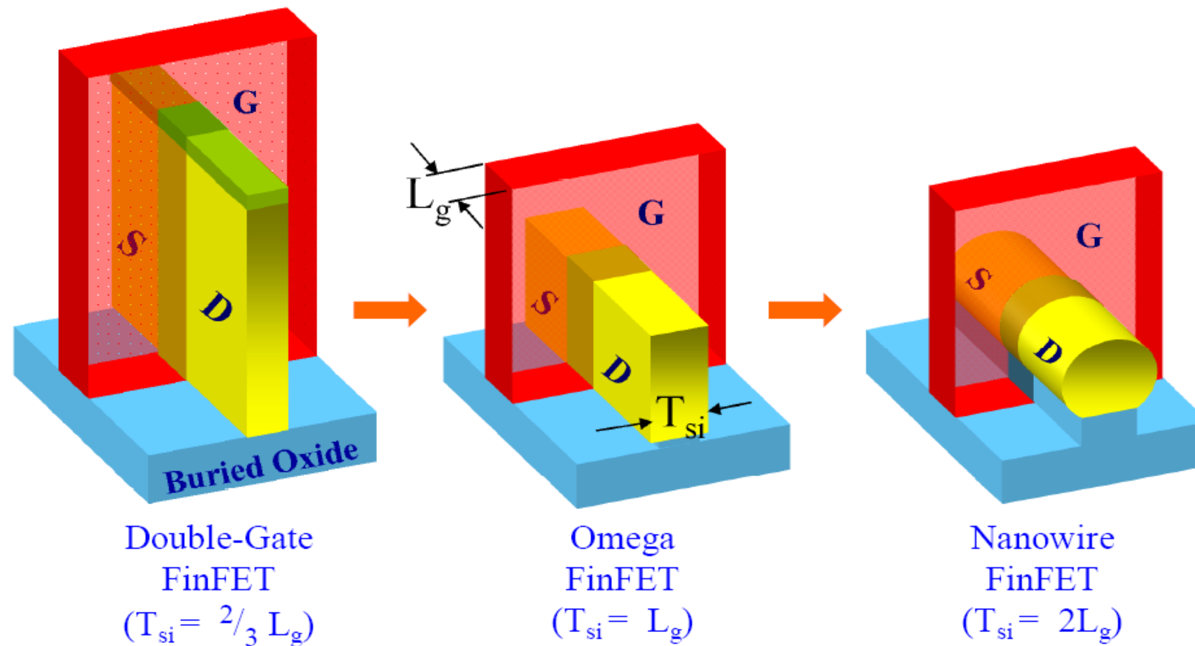
Before reaching the scaling limit, we need to pursuit the down scaling limit with conventional planar, or FINFET, introducing new materials such as
(1) high-k/metal gate <0.5 nm EOT, and silicide S/D.

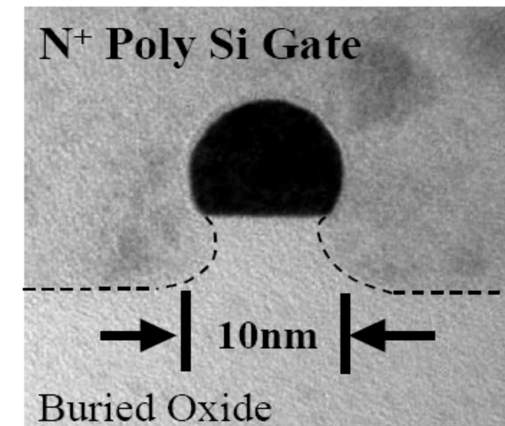
Then, (2) Si-nanowire FET

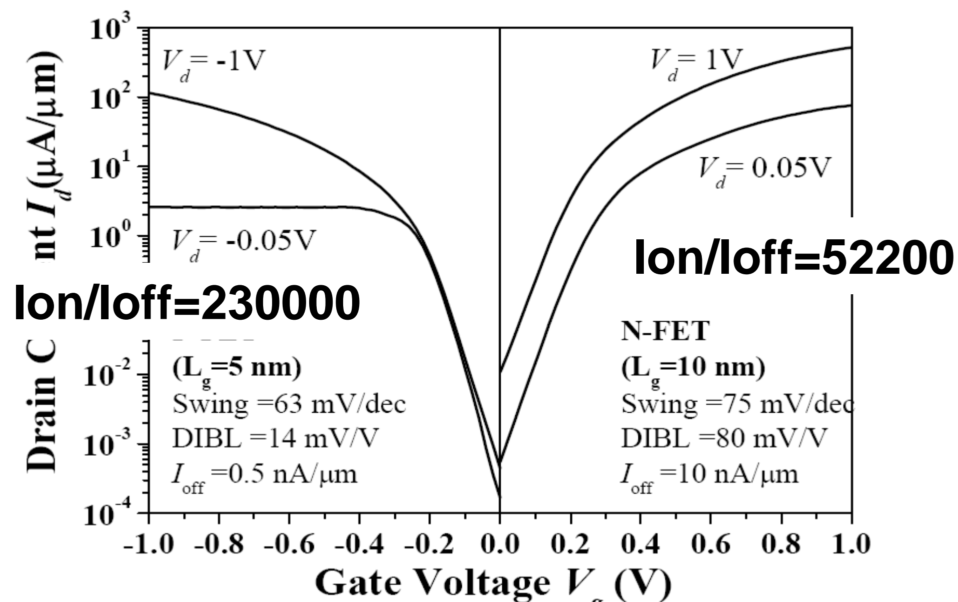
and then, (3) Alternative channel (III-V and Ge) .

Si Nanowire FET

FinFET to Nanowire





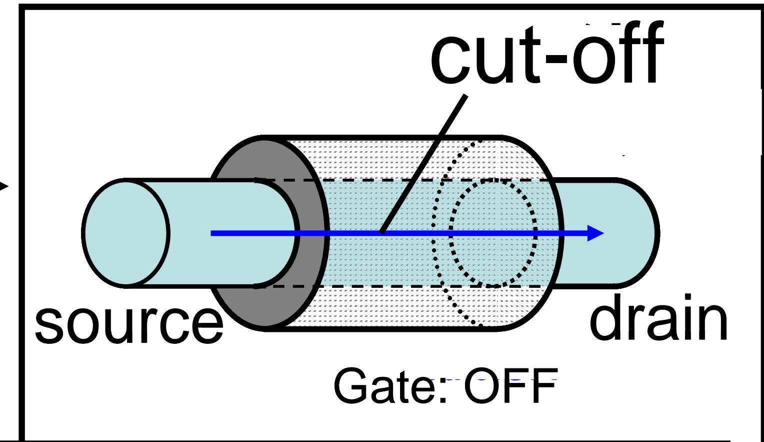


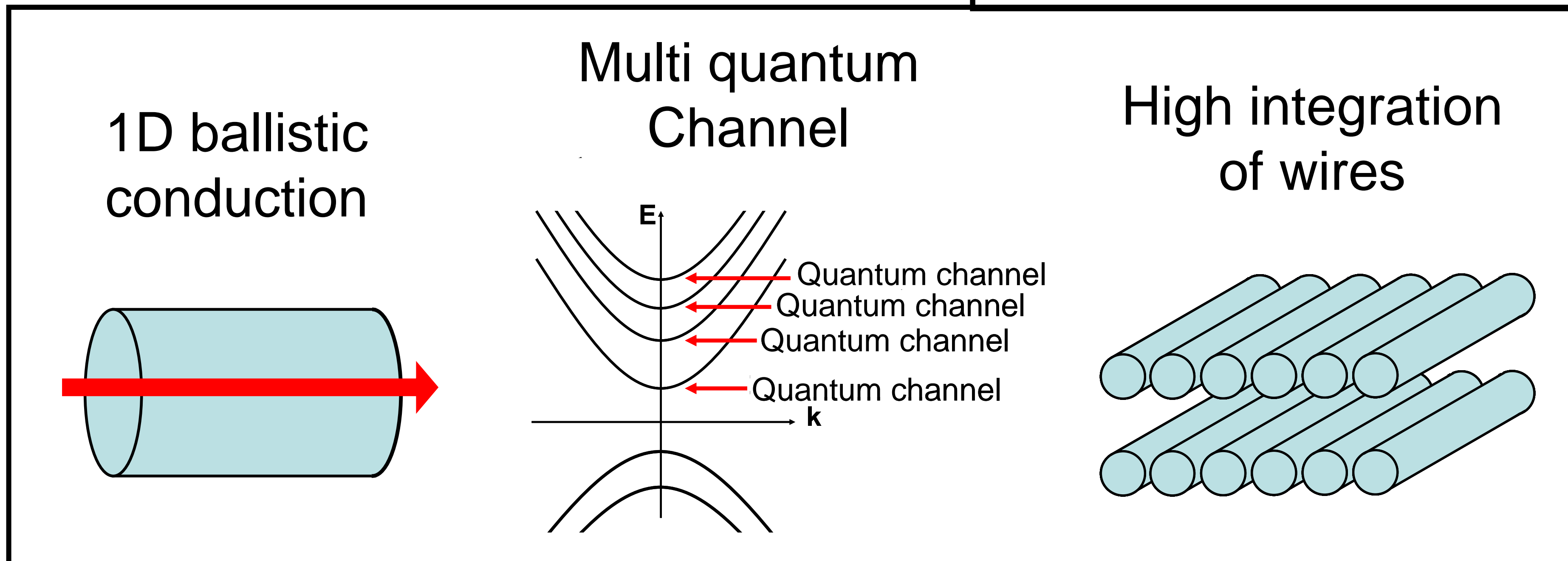
Channel conductance is well controlled by Gate even at L=5nm

F.-L.Yang, VLSI2004

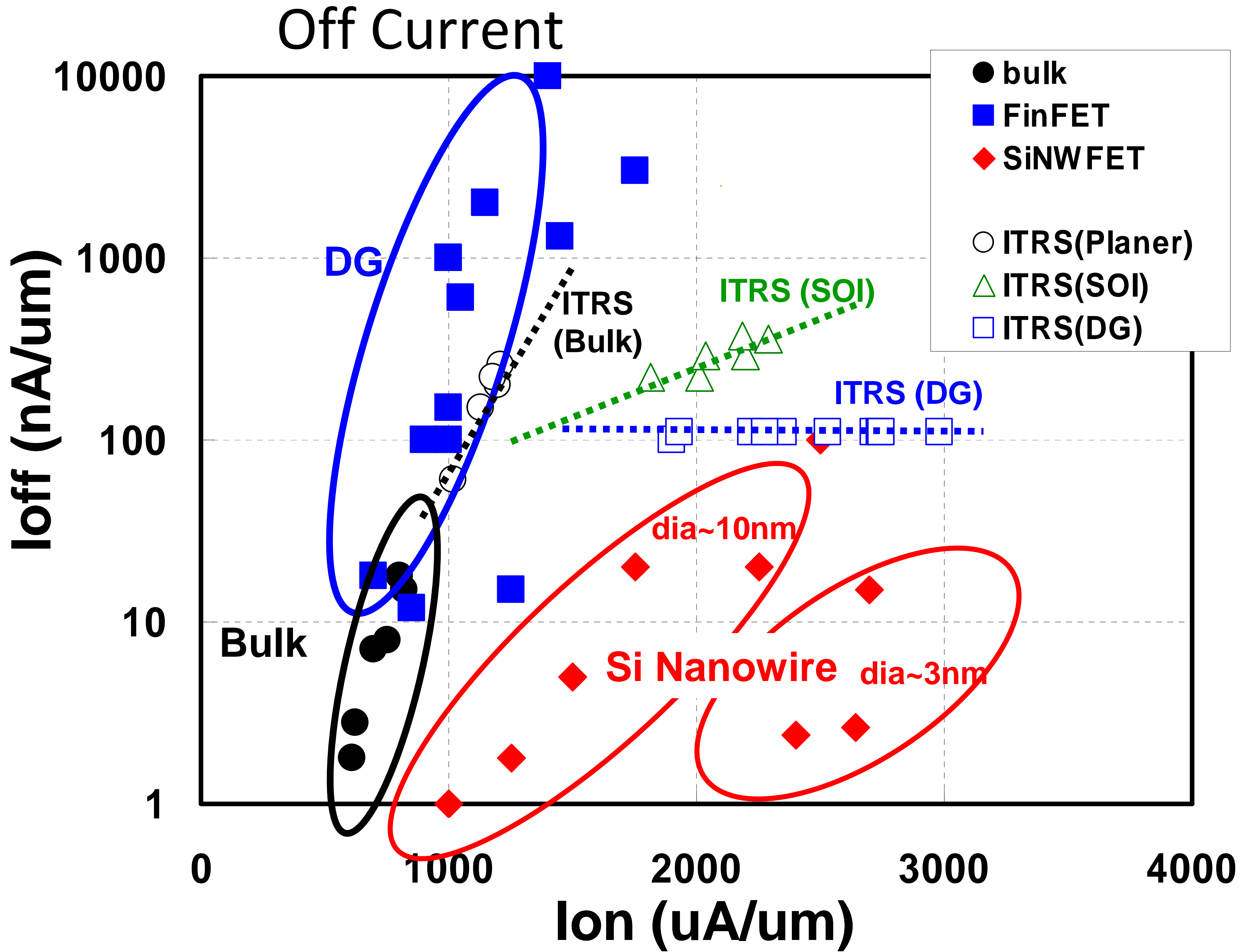
Si nanowire FET as a strong candidate after CMOS limitation

1. Compatibility with current CMOS process
2. Good controllability of I_{OFF}
3. High drive current





by the courtesy of Professor H. Iwai



Off Current
10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

1D conduction per one quantum channel:

$G = 2e^2/h = 77.8\ \mu S$/wire or tube

regardless of gate length and channel material

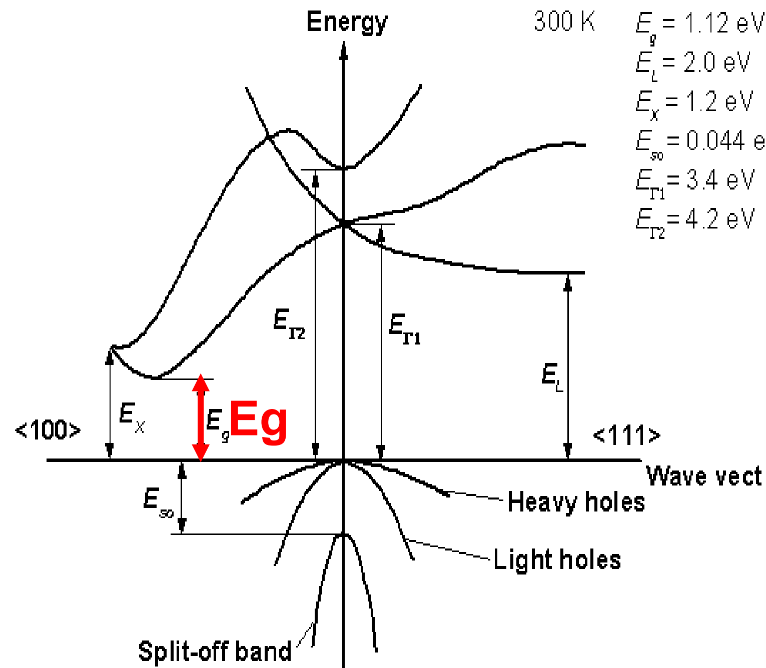
That is 77.8 microA/wire at 1V supply

This an extremely high value

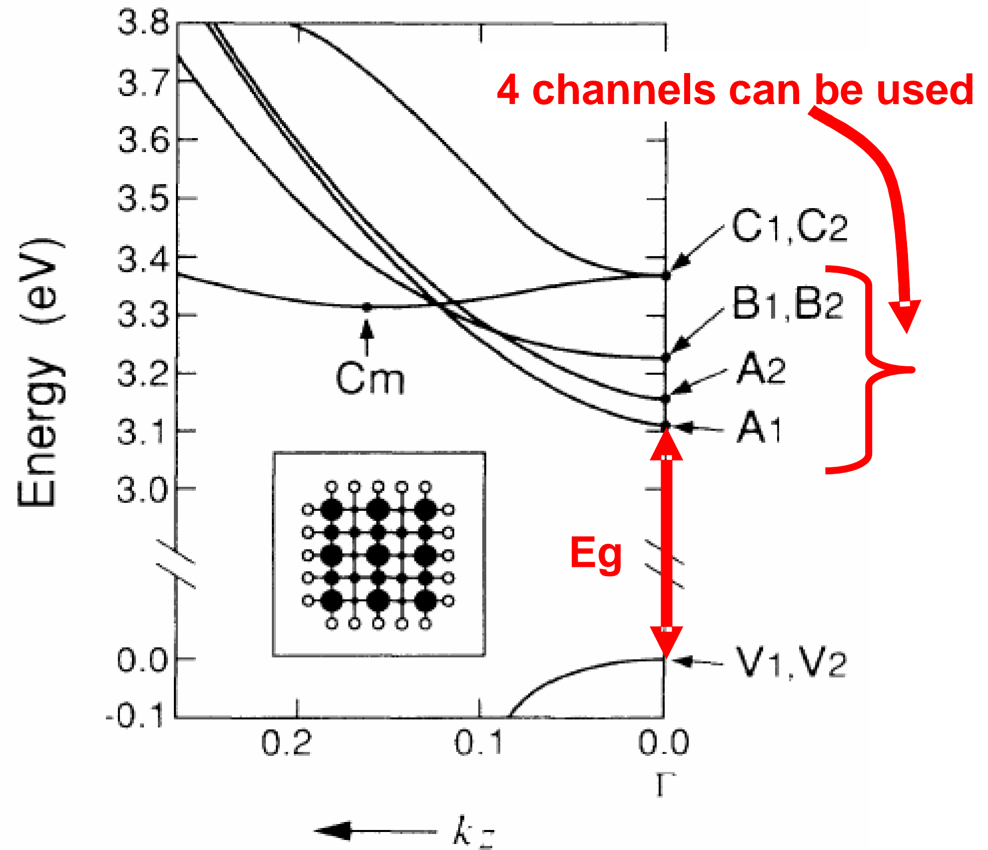
However, already 40-50 micro A/wire was obtained by our experiments

Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



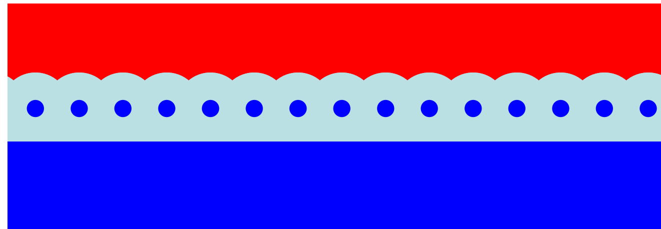
Energy band of Bulk Si



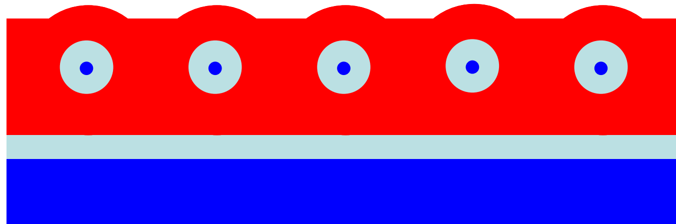
Energy band of 3 x 3 Si wire

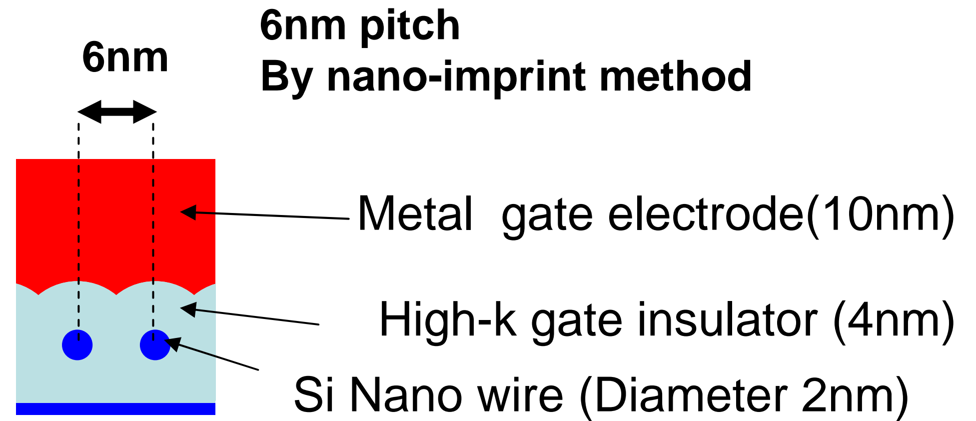
Maximum number of wires per 1 µm

Front gate type MOS 165 wires /µm

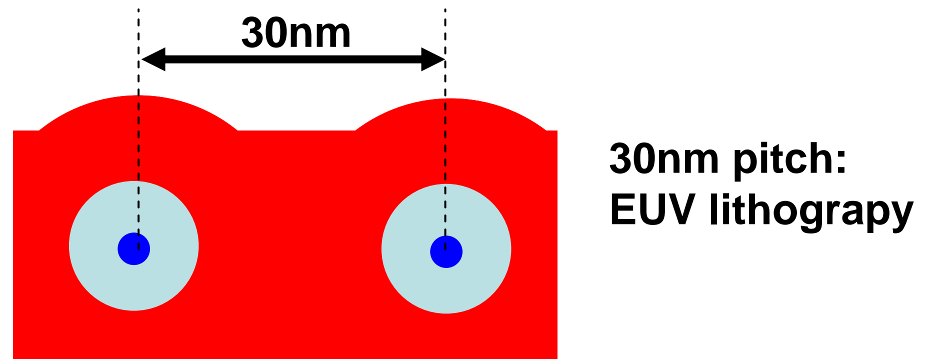


Surrounded gate type MOS 33 wires/µm

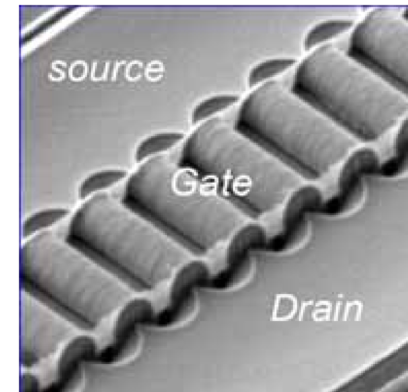




6nm pitch
By nano-imprint method

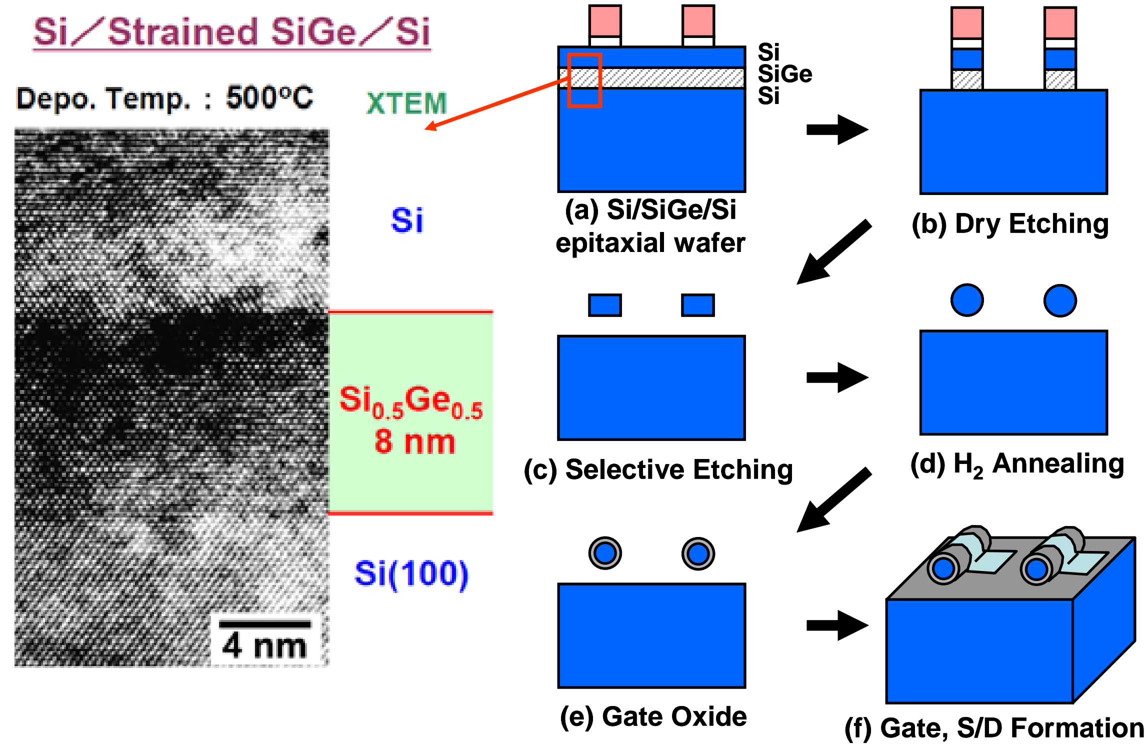


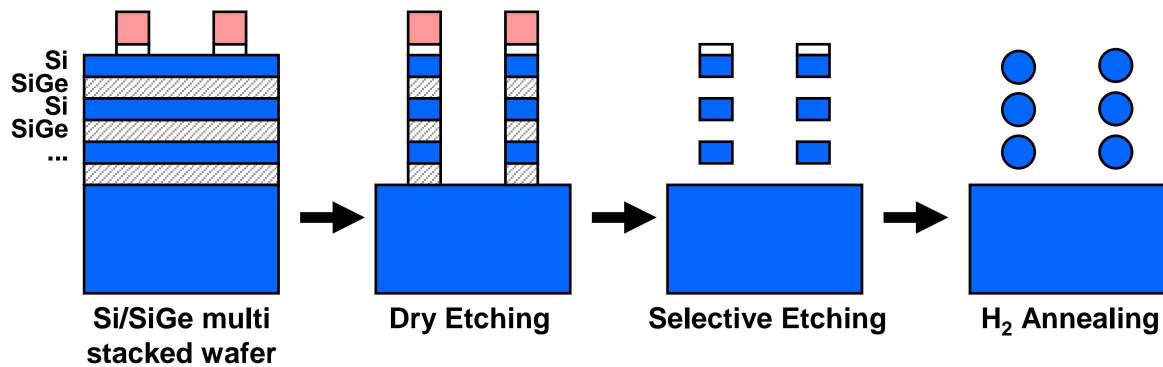
30nm pitch:
EUV lithograpy



Surrounded gate MOS

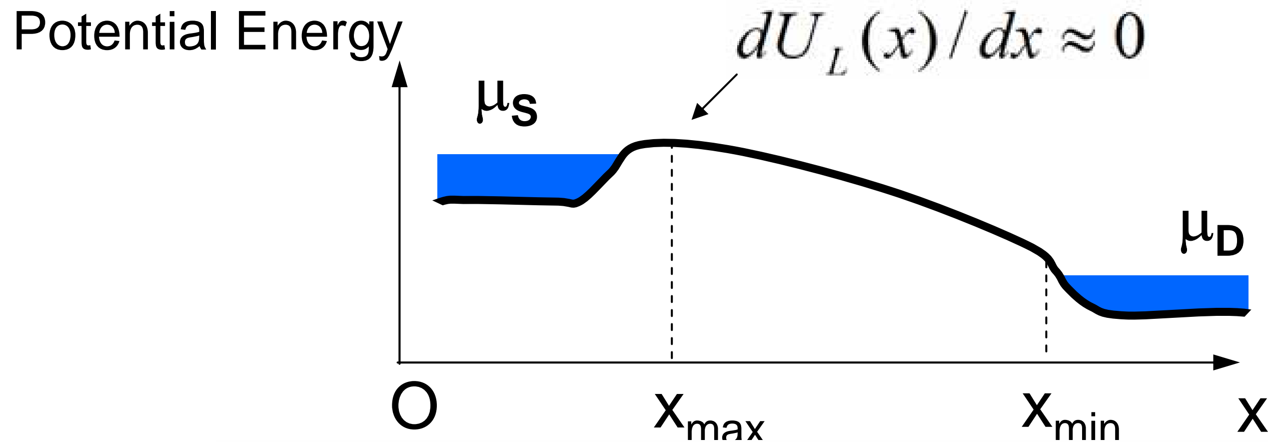
Increase the number of wires towards vertical dimension





Theoretical model of SiNW FET

Landauer Formalism for Ballistic FET

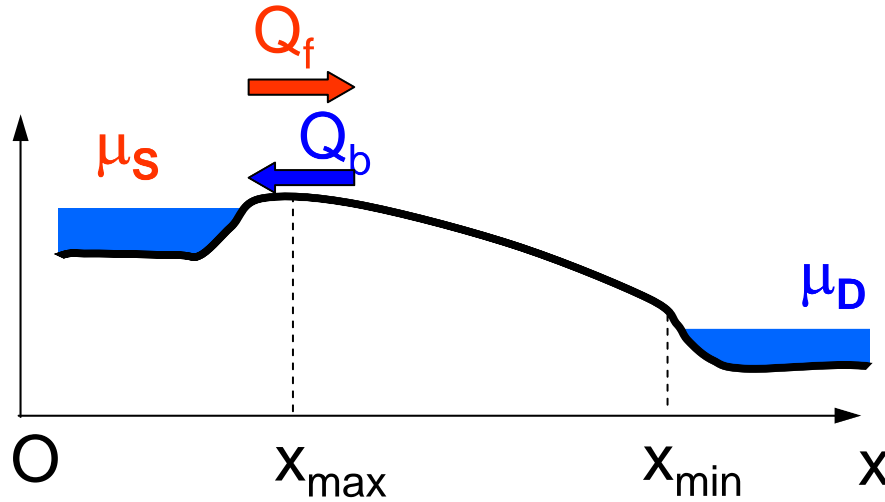


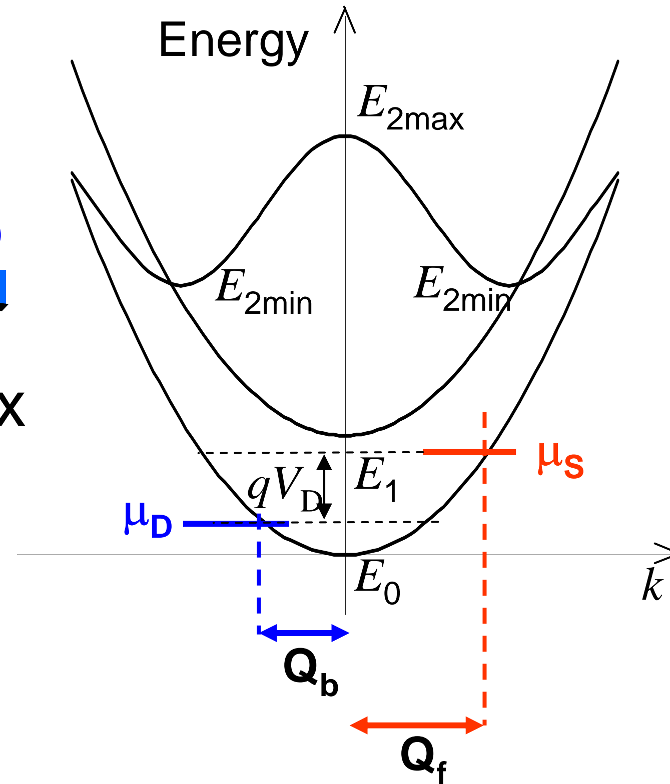
$$I_D = \frac{q}{\pi\hbar}\sum_i \int [f(E,\mu_S) - f(E,\mu_D)] T_i(E) dE$$

From x_{max} to x_{min} $\quad T_i(E) \approx 1$

$$I_D = G_0\left(\frac{k_B T}{q}\right)\sum_i g_i \ln\left\{\frac{1+\exp[(\mu_S - E_{i0})/k_B T]}{1+\exp[(\mu_D - E_{i0})/k_B T]}\right\}$$

Carrier Density obtained from E-k Band

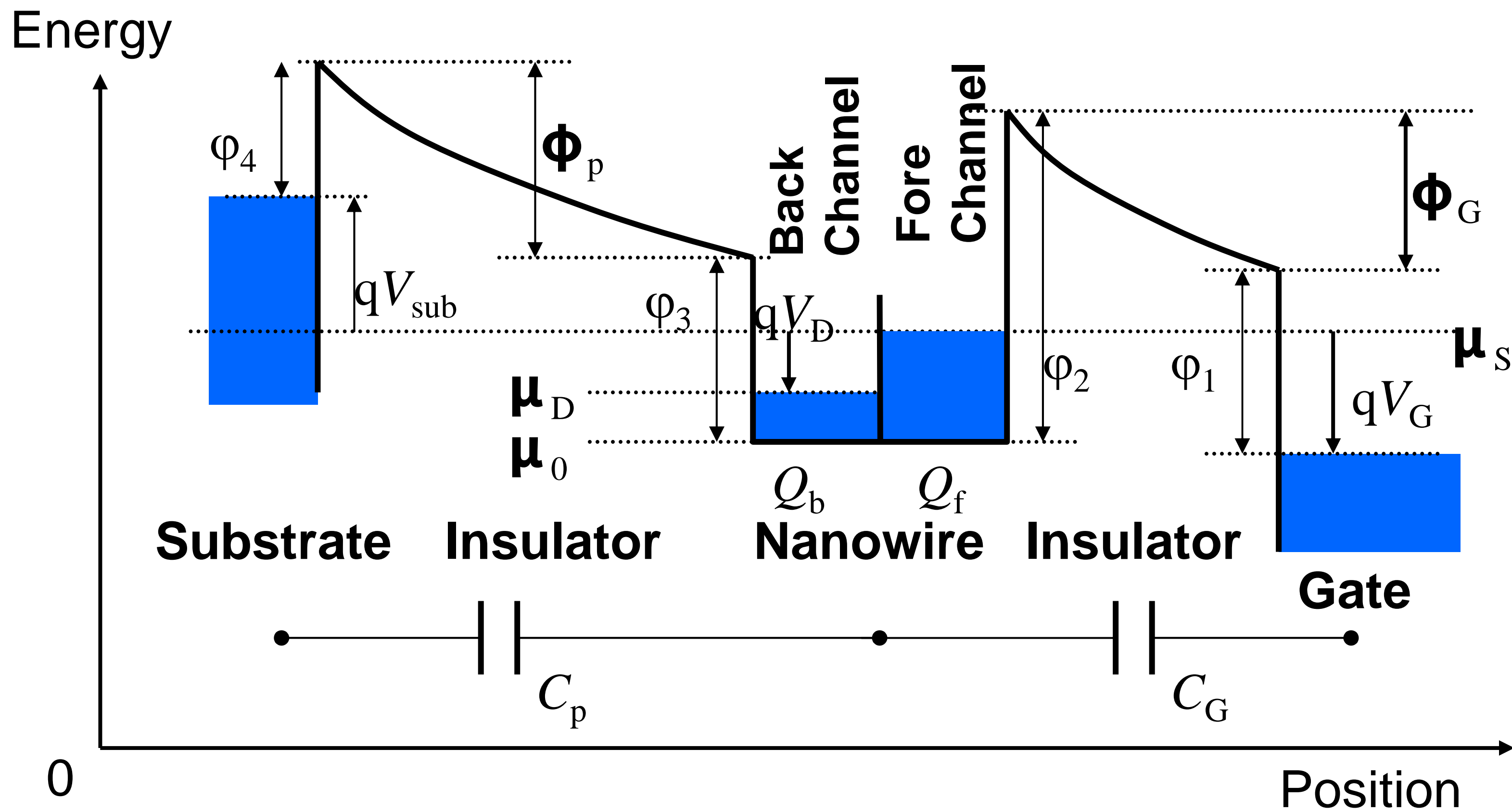




$$|Q| = |Q_f| + |Q_b|$$

$$= \frac{q}{\pi} \sum_i g_i \left[\int_{k_{i\min}}^{\infty} \frac{dk}{1 + \exp\left\{ \frac{E_i(k) - \mu_S}{k_B T} \right\}} + \int_{-\infty}^{k_{i\min}} \frac{dk}{1 + \exp\left\{ \frac{E_i(k) - \mu_D}{k_B T} \right\}} \right]$$

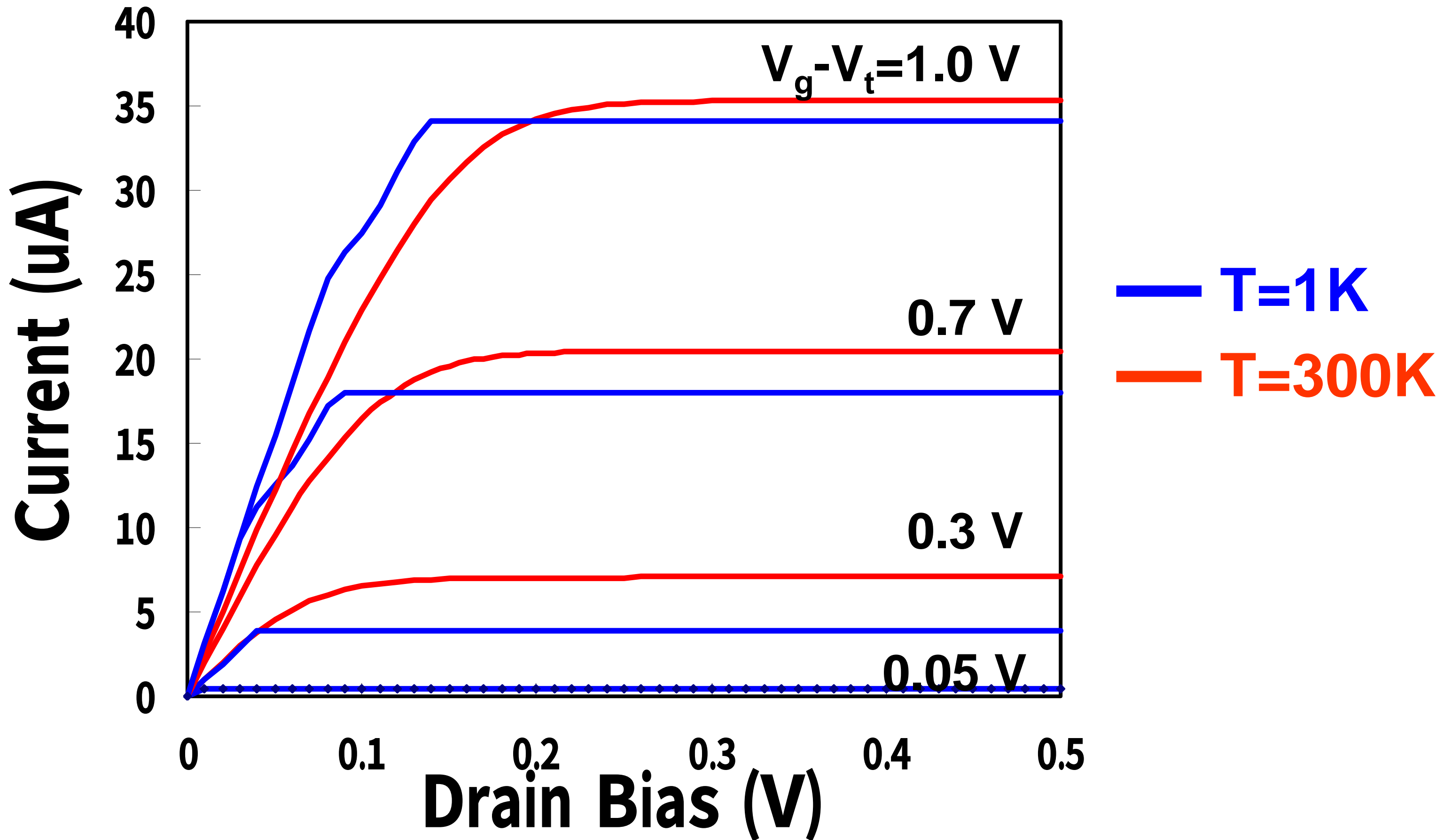
Carrier Density obtained from Band Diagram



$$\frac{|Q|}{C_G} = (V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q}$$

$$\alpha = 1 + \frac{C_P}{C_G}$$

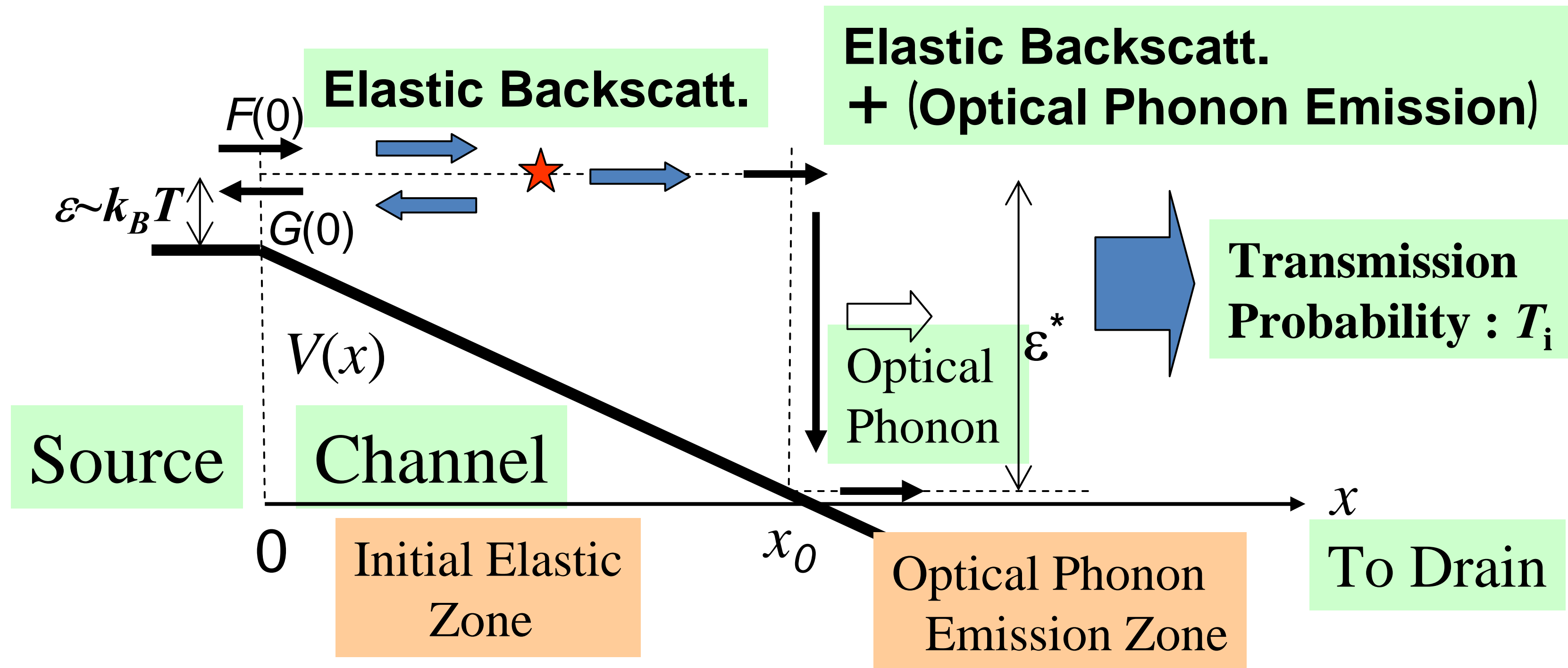
IV Characteristics of Ballistic SiNW FET



Small temperature dependency
35μA/wire for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx.： Electric Field *E*



Transmission Probability to Drain

$$T(\varepsilon) = \left.\frac{F(0) - G(0)}{F(0)}\right)_{\text{Injection from Drain}=0}$$

Résumé of the Compact Model

$$I = \frac{q}{\pi\hbar}\sum_i g_i \int \left[f(\varepsilon,\mu_s) - f(\varepsilon,\mu_D) \right] T_i \, d\varepsilon$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left\{ \dfrac{\sqrt{2r+t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r+t_{ox}} - \sqrt{t_{ox}}} \right\}}.$$

Planar Gate

$$(V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{\left| Q_f + Q_b \right|}{C_G}.$$

$$\mu_S - \mu_D = qV_D$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left(\dfrac{r + t_{ox}}{r} \right)}.$$

GAA

(Electrostatics requirement)

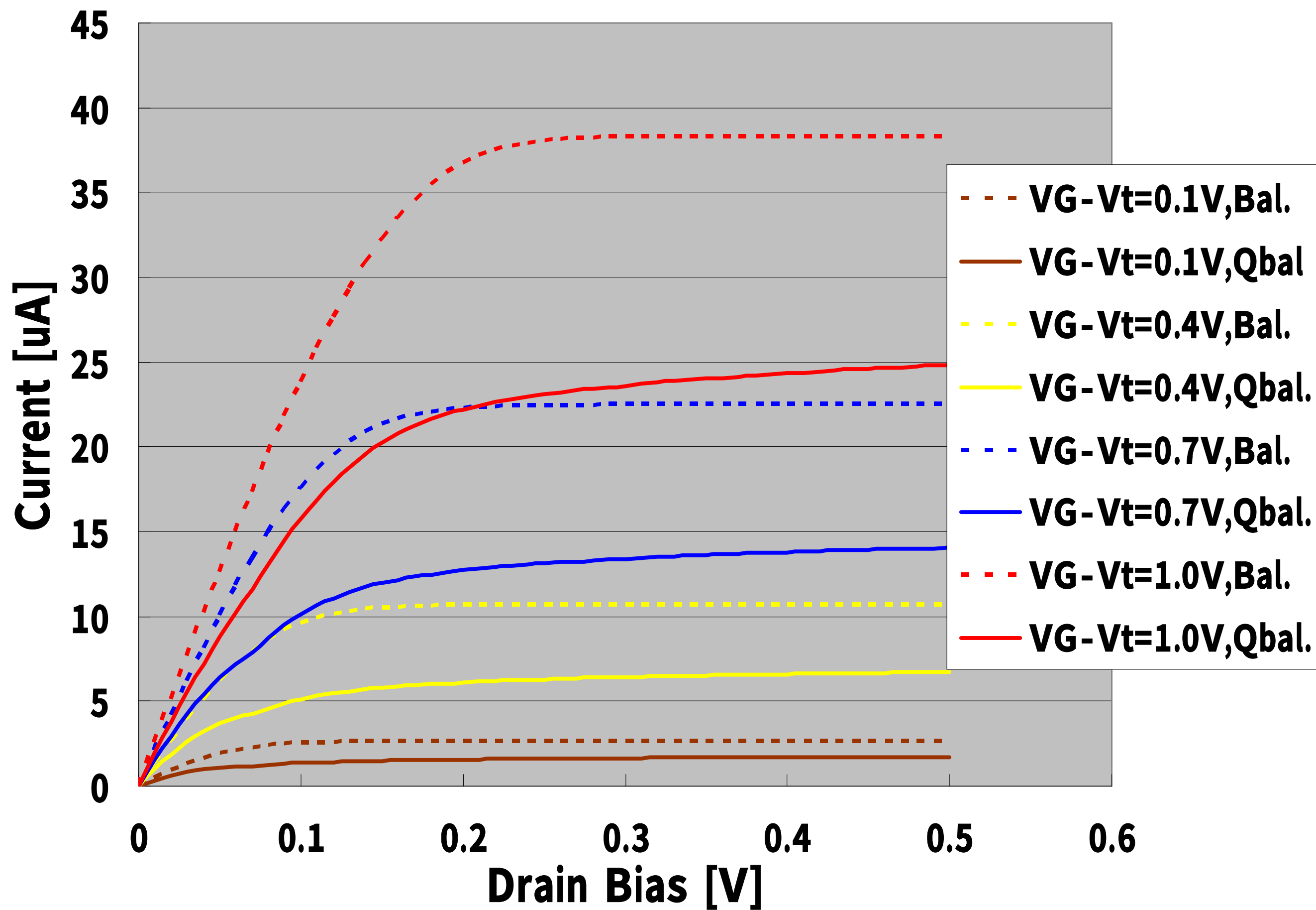
$$\left| Q_f + Q_b \right| = \frac{q}{\pi}\sum_i g_i \left[\int_{-\infty}^{\infty} \frac{dk}{1+\exp\left\{ \dfrac{\varepsilon_i(k) - \mu_S}{k_B T} \right\}} - \int_{-\infty}^{0} \left\{ \frac{1}{1+\exp\left\{ \dfrac{\varepsilon_i(k) - \mu_S}{k_B T} \right\}} - \frac{1}{1+\exp\left\{ \dfrac{\varepsilon_i(k) - \mu_D}{k_B T} \right\}} \right\} T_i(\varepsilon_i(k)) dk \right]$$

$$T(\varepsilon) = \frac{\sqrt{2D_0}\, qE}{\left(\sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0}\, B_0 \ln\left(\dfrac{qEx_0 + \varepsilon}{\varepsilon} \right)}$$

(Carrier distribution in Subbands)

Unknowns are I_D, $(\mu_S - \mu_0)$, $(\mu_D - \mu_0)$, および $(Q_f + Q_b)$

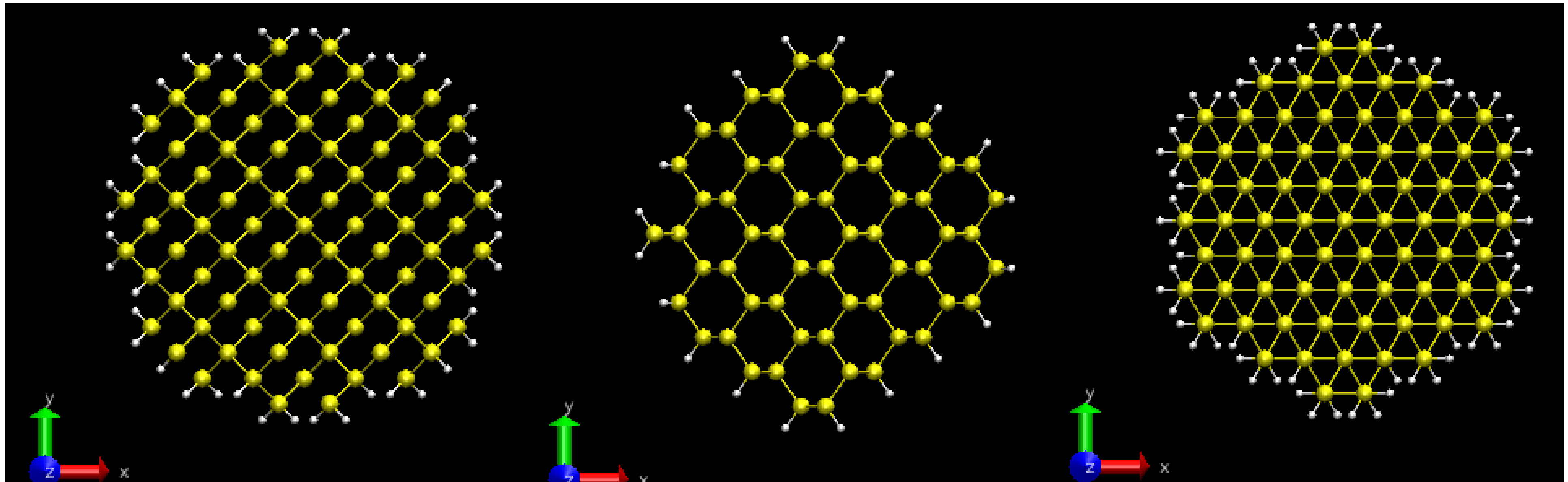
I-V_D Characteritics (RT)



- Electric current 20～25 μA
- No satruration at Large V_D

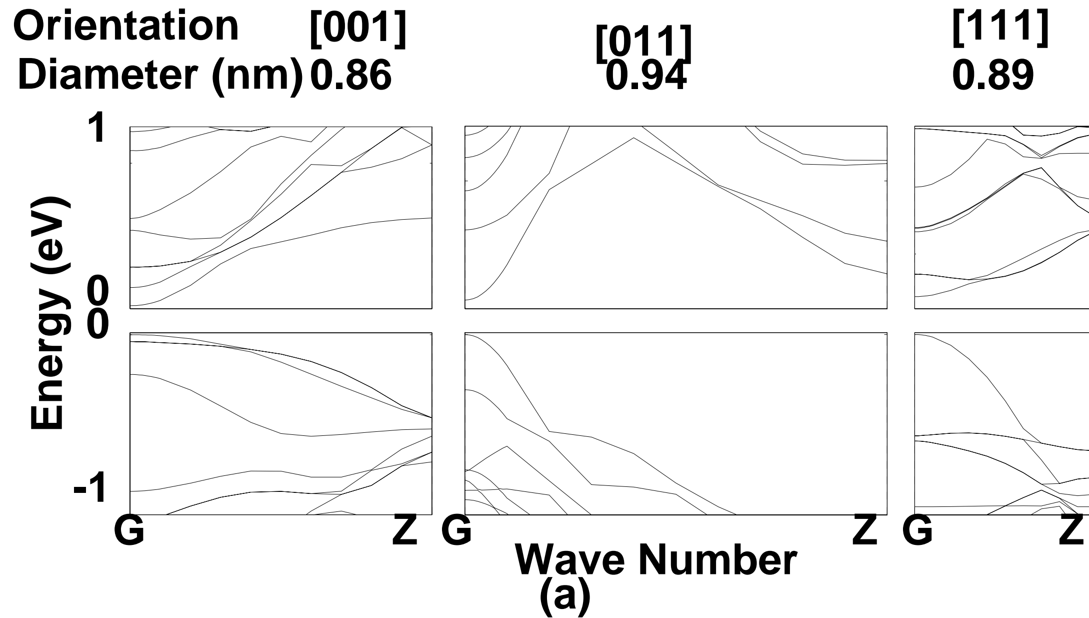
Cross section of Si NW

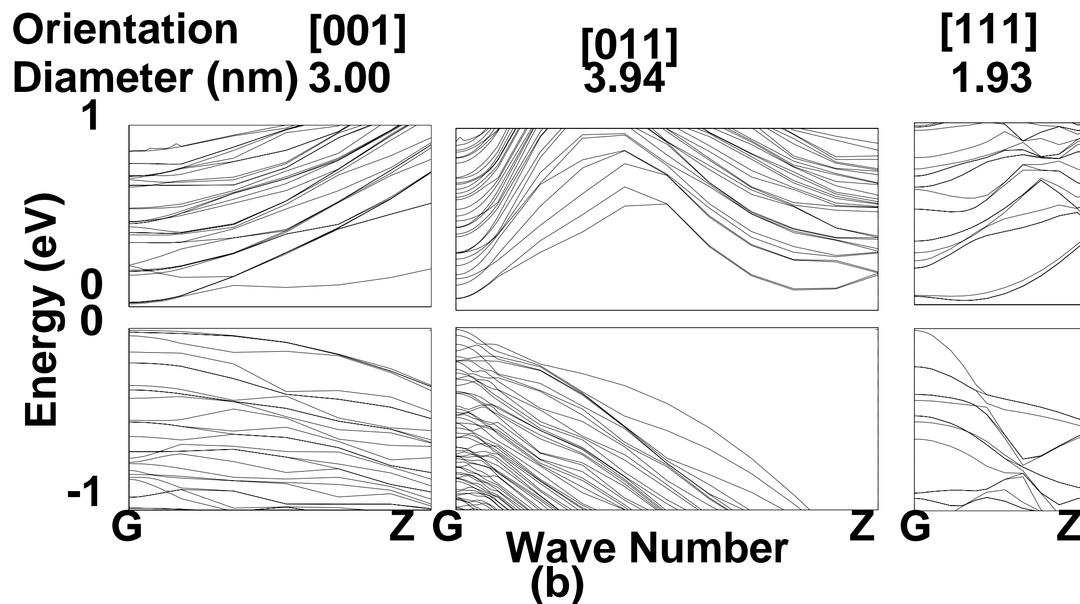
First principal calculation, TAPP



D=1.96nm	D=1.94nm	D=1.93nm
[001]	[011]	[111]

Si nanowire FET with 1D Transport

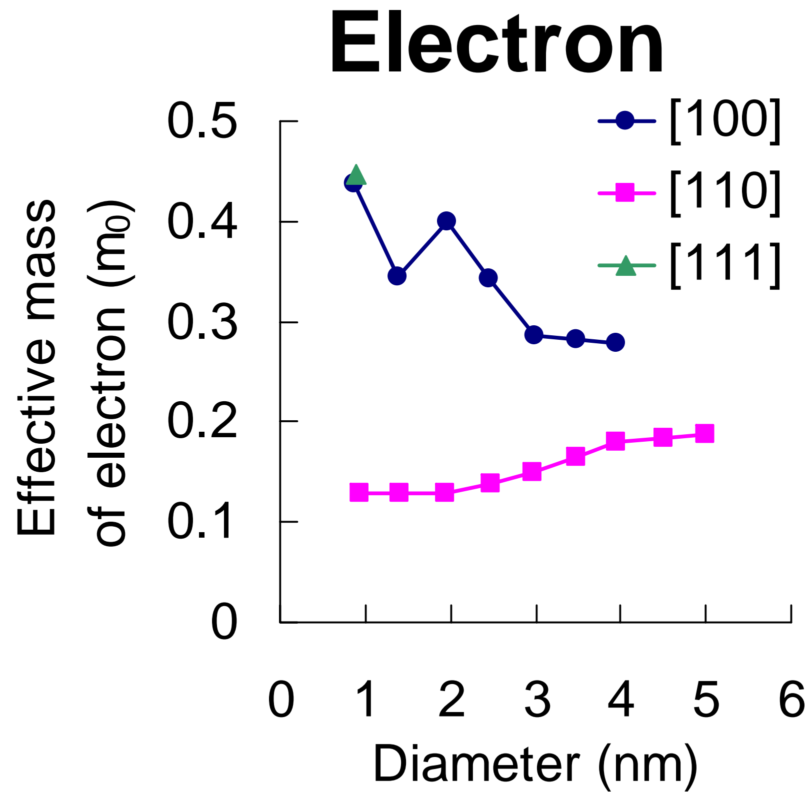


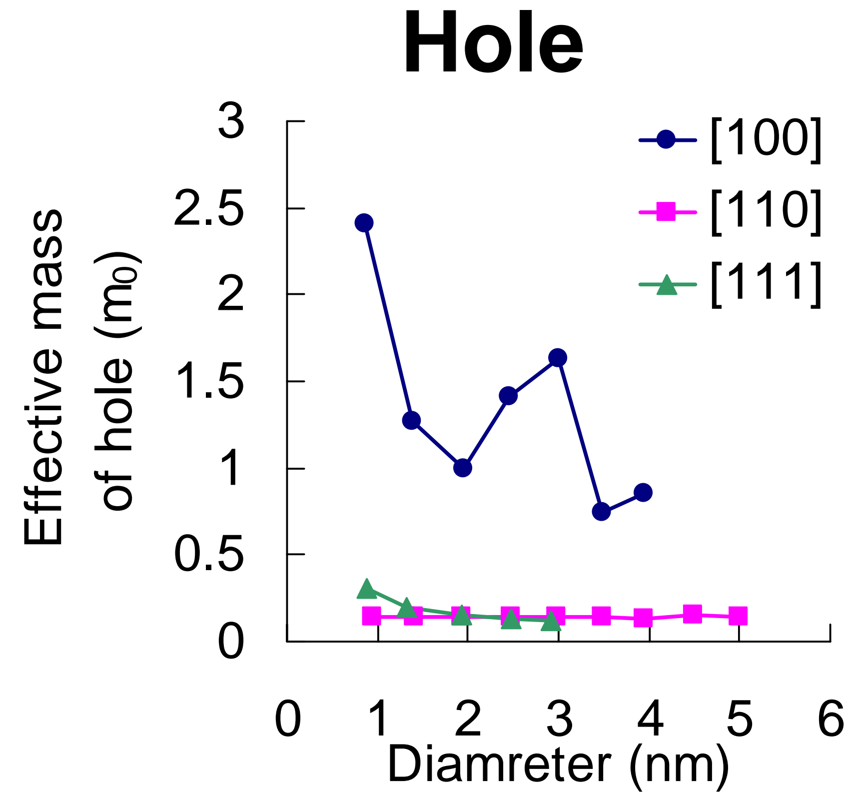


Small mass with [011]

Large number of quantum channels with [001]

Effective mass





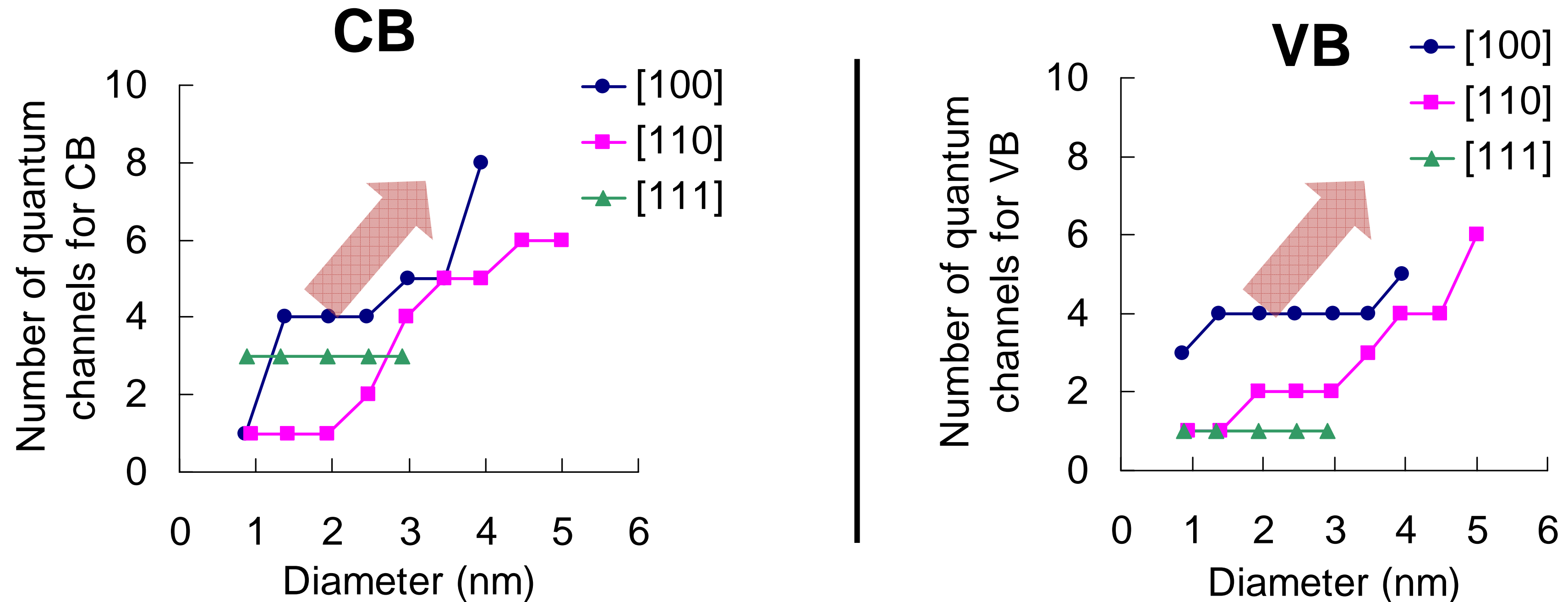
Lighter effective masses make conductance higher

→ lighter

Electron	**[100] [111] > [110]**	**lighter**
Hole	**[100] >> [110] [111]**	

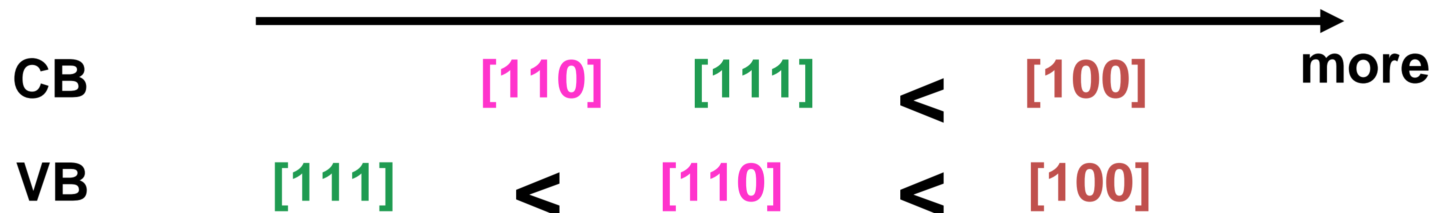
Numbers of Quantum Channels

Quantum channels denote subband edges within 0.1 eV from CBM and VBM



Quantum channels increase in large wire

Quantum channel ➡ **Passage for transport**

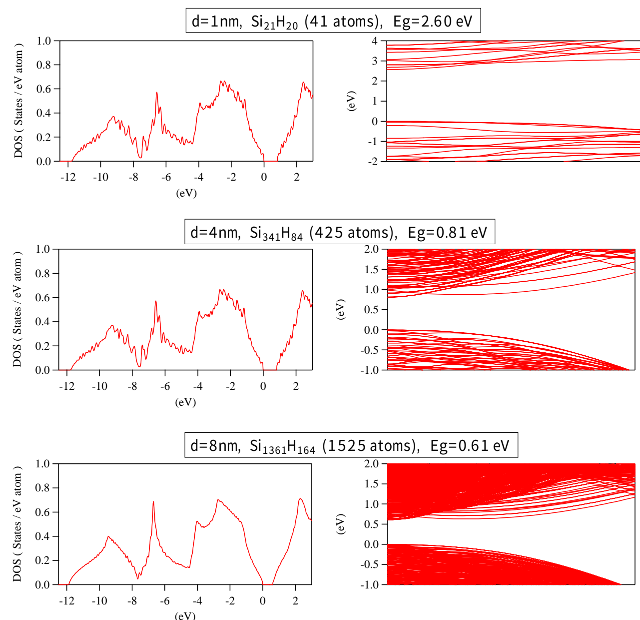


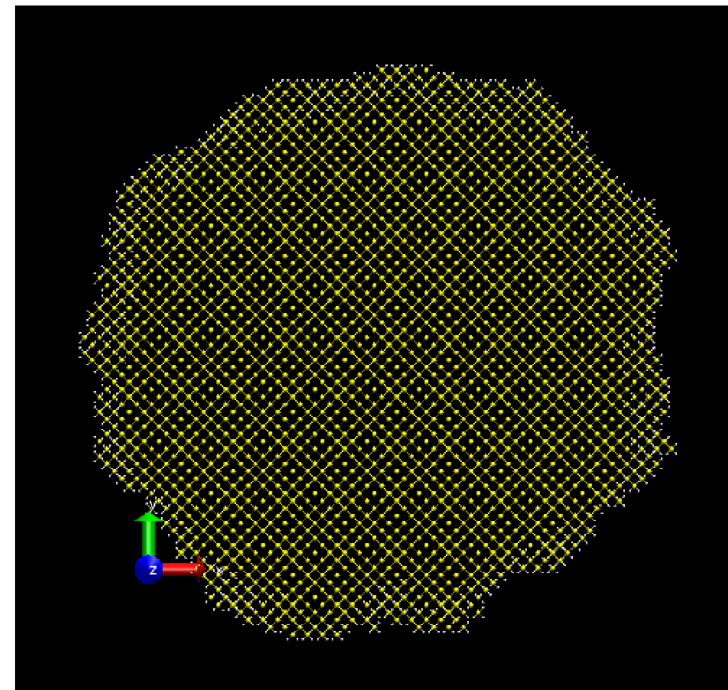
Collboration with Prof. Oshiyama and Iwata of Univ. of Tokyo

PACS-CS
Theoretical Peak Performance : 14 TFLOPS
CPU : LV Xeon 2.8GHz (✕1 CPU✕2560 nodes)

T2K-Tsukuba
Theoretical Peak Performance : 95 TFLOPS
CPU : Quad-core Opteron 2.3GHz (✕4 CPUs✕648 nodes)

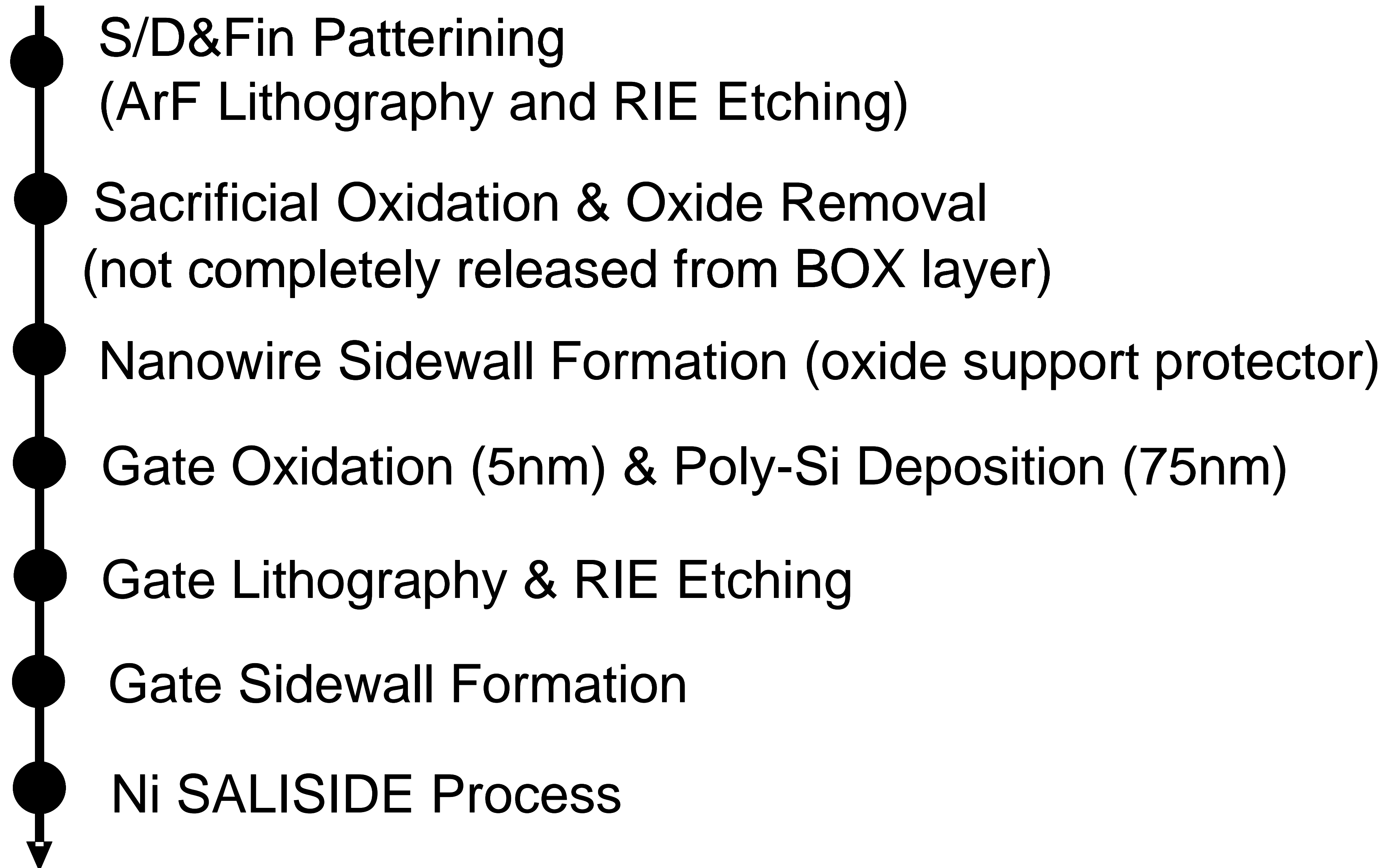
10 nm diameter Si nanowired with 14,366-atom model



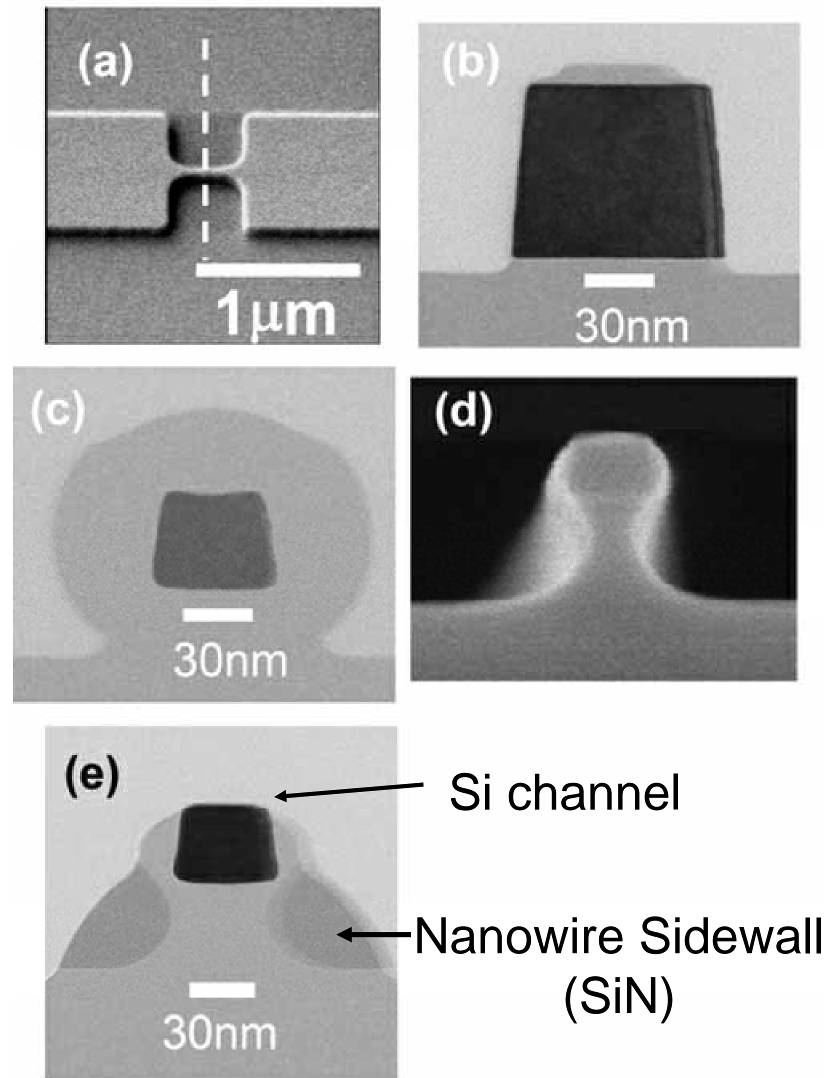


SiNW FET Fabrication

Brief process flow of Si Nanowire FET

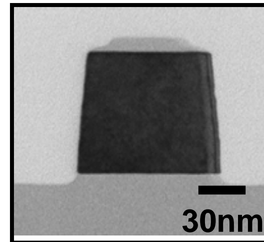


(a) Fin structure formed on BOX layer. (b)XTEM image of fin shown in (a) (c) XTEM image after sacrificial oxidation (d) Cross sectional SEM image after partial removal of sacrificial oxide (e) XTEM after nanowire sidewall formation

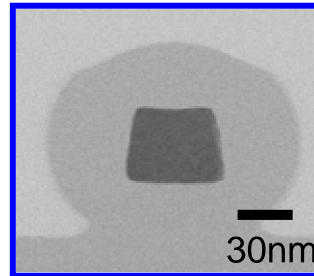


SiNW FET Fabrication

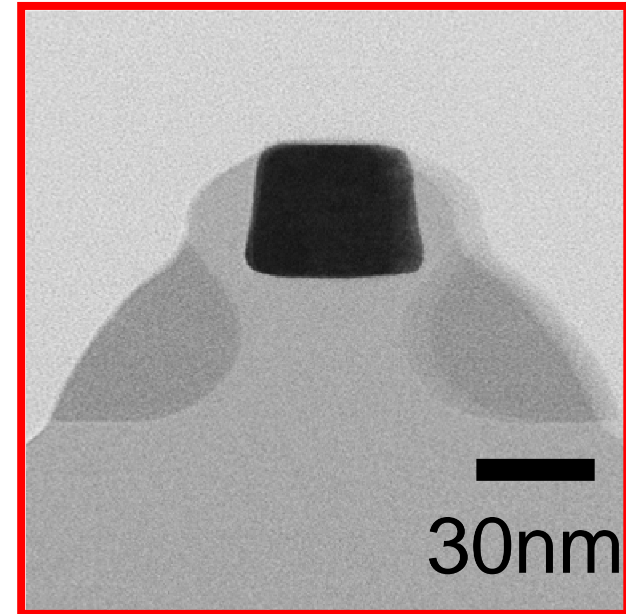
- S/D & Fin Patterning



- Sacrificial Oxidation



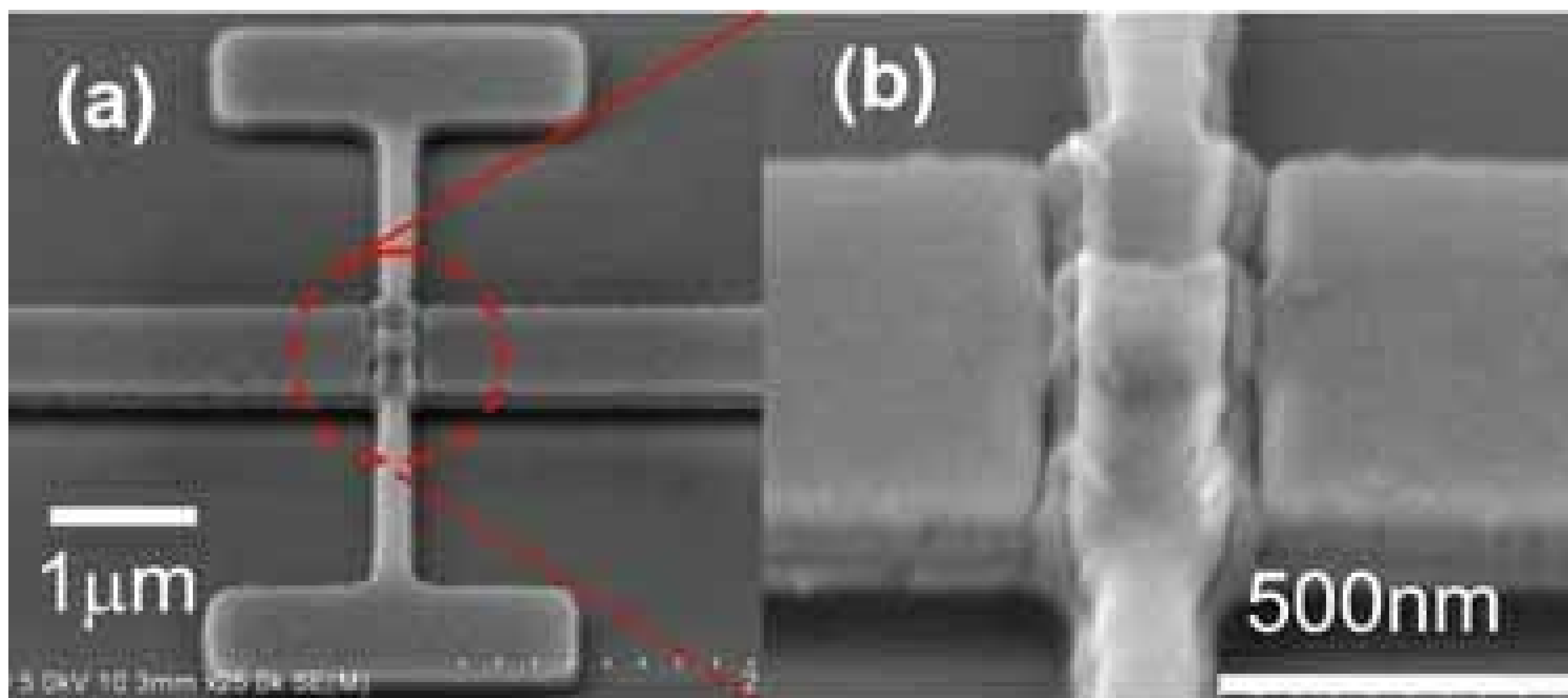
- Oixde etch back
- SiN sidewall support formation



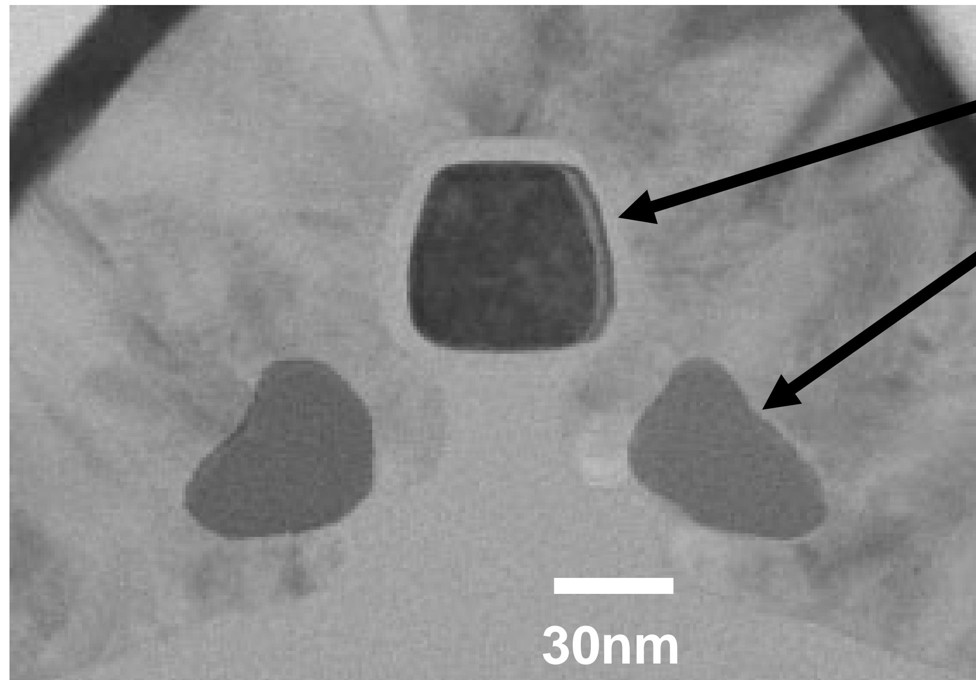
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

Standard recipe for gate stack formation

(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.

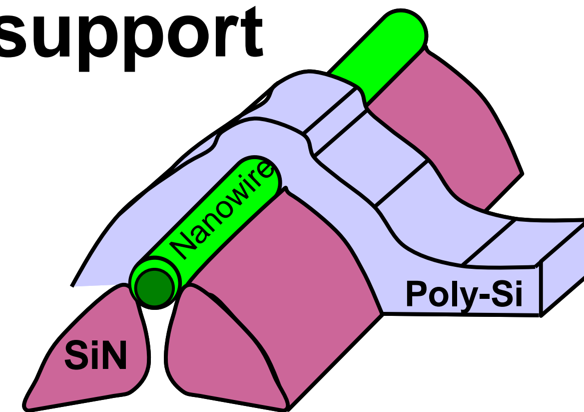


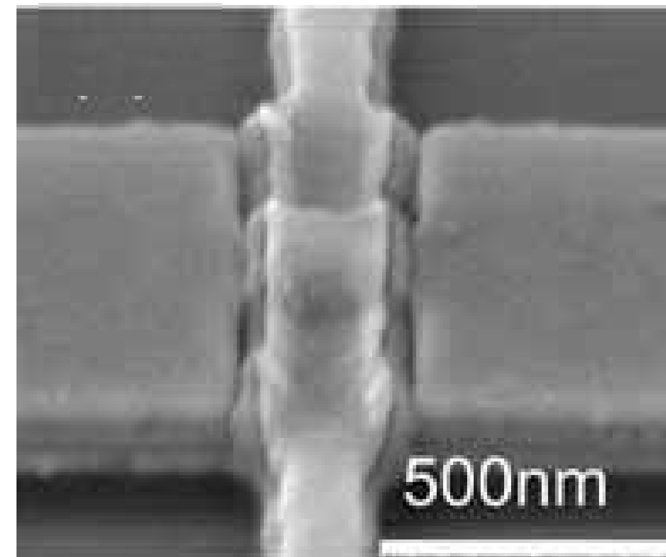
Fabricated SiNW FET



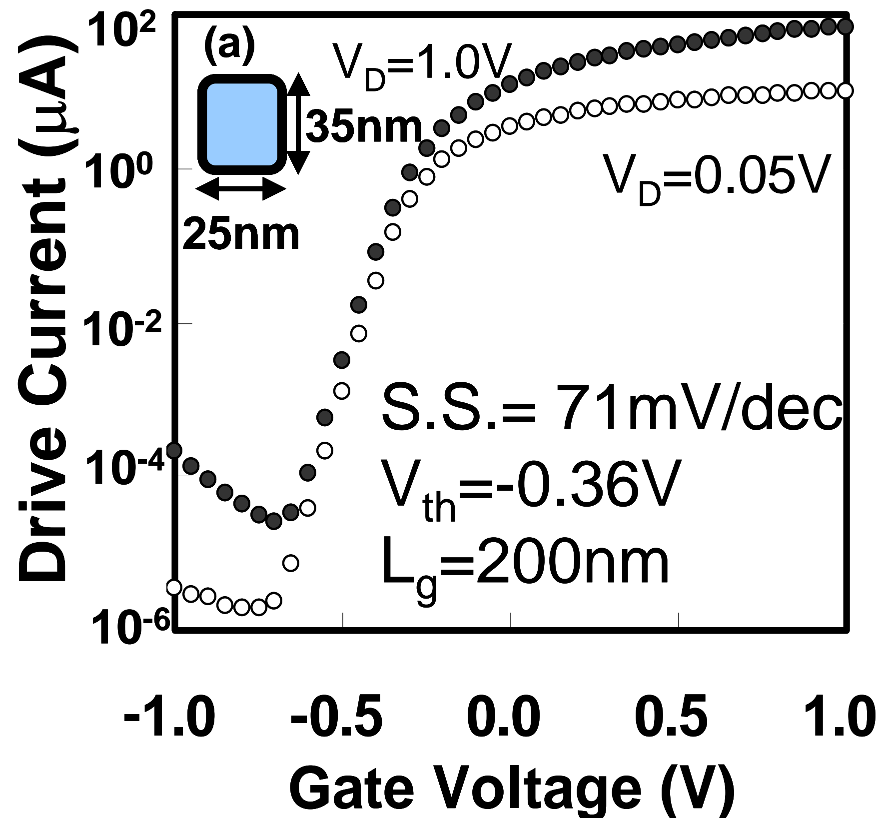
SiNW

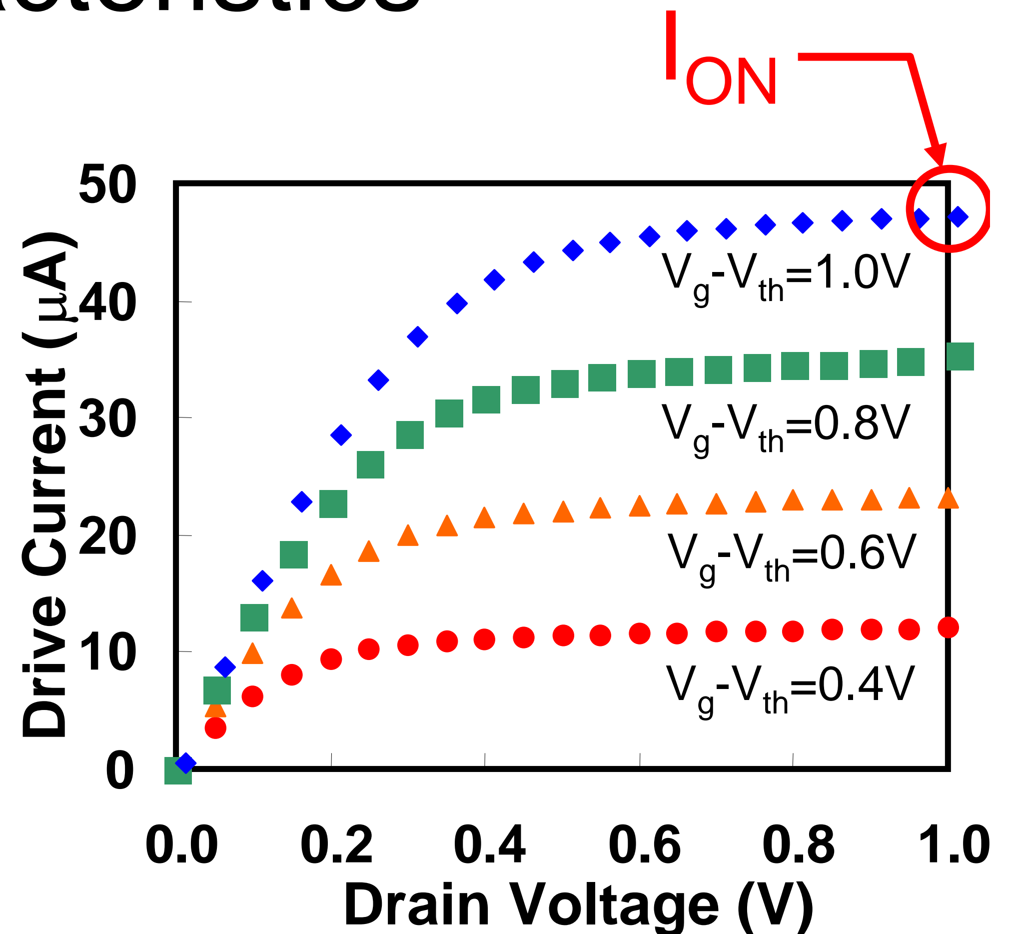
SiN support





I_dV_g and I_dV_d Characteristics





I_{on}/I_{off} ratio of ~10^7, high I_{on} of 49.6 μA/wire

Effective mobility extraction

Effective electron mobility (cm^2/Vs)

800
600
400
200
0

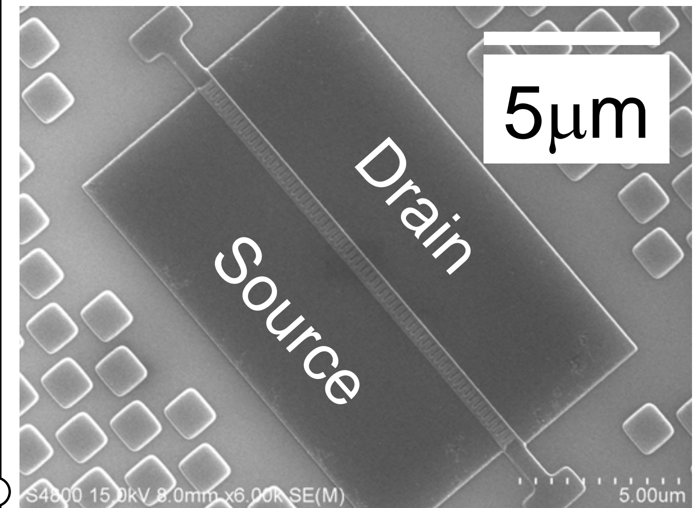
L_g=500nm
Number of NWs :64

Univ. curve Si (100)

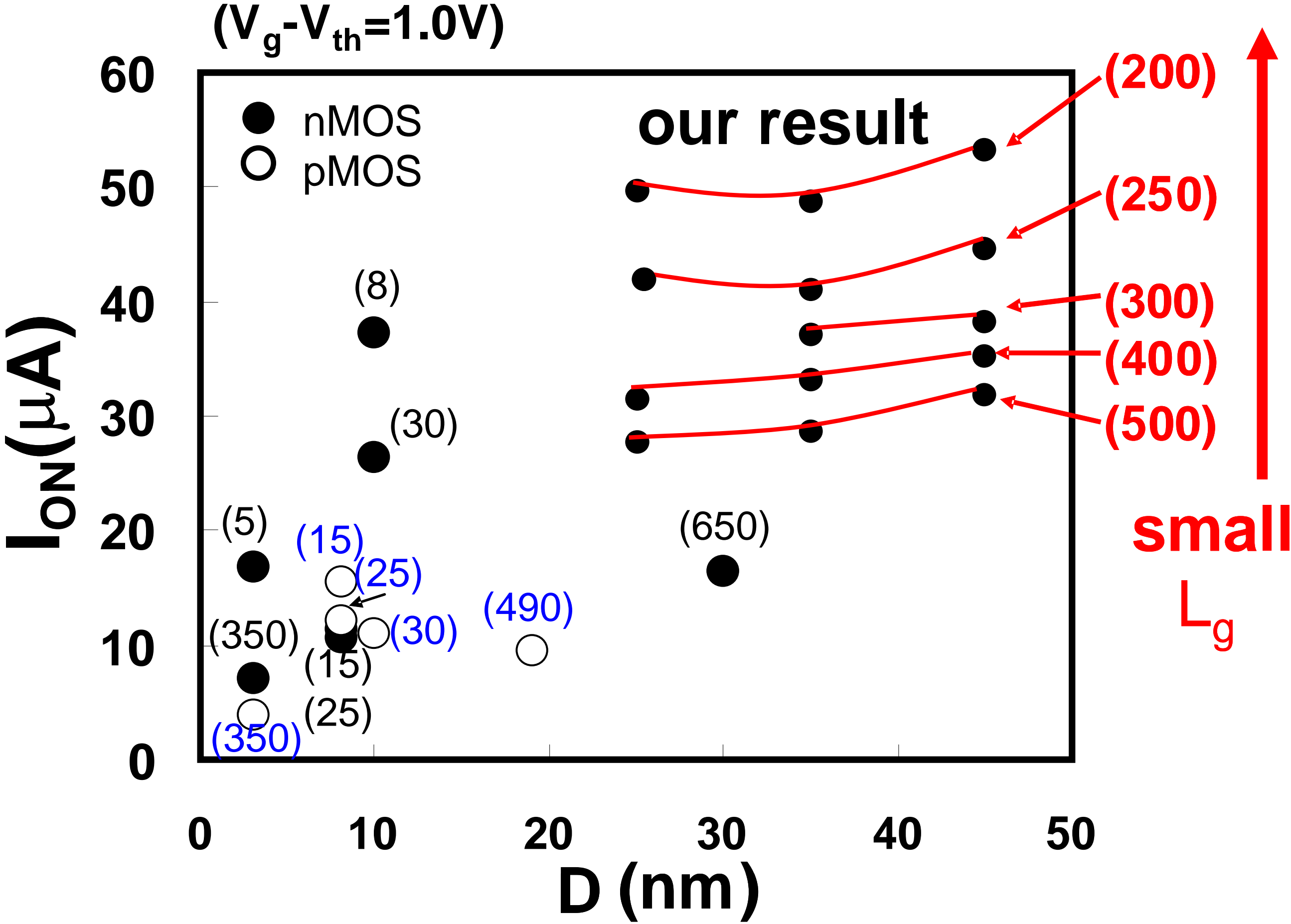
measured at RT

0.E+00
5.E+12
1.E+13
2.E+13

Inversion Carrier Density (cm^{-2})

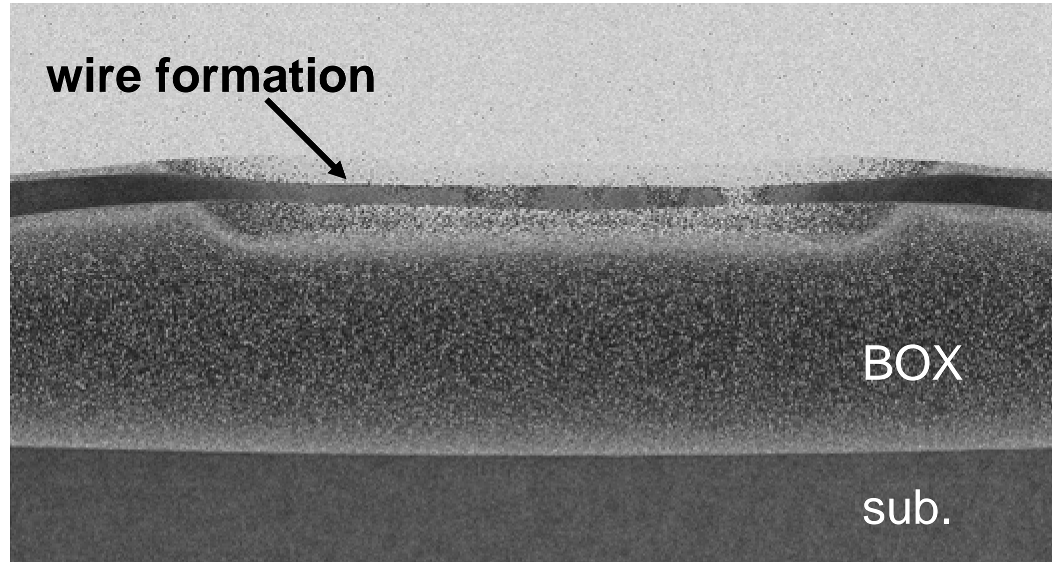


Comparison of Si NW FET being already reported with Si NW FETs in this work

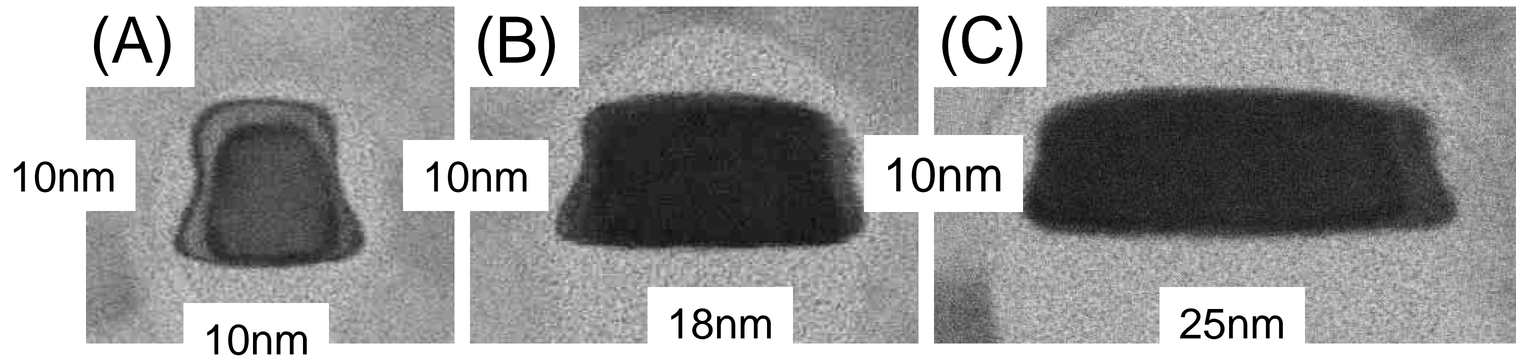


??

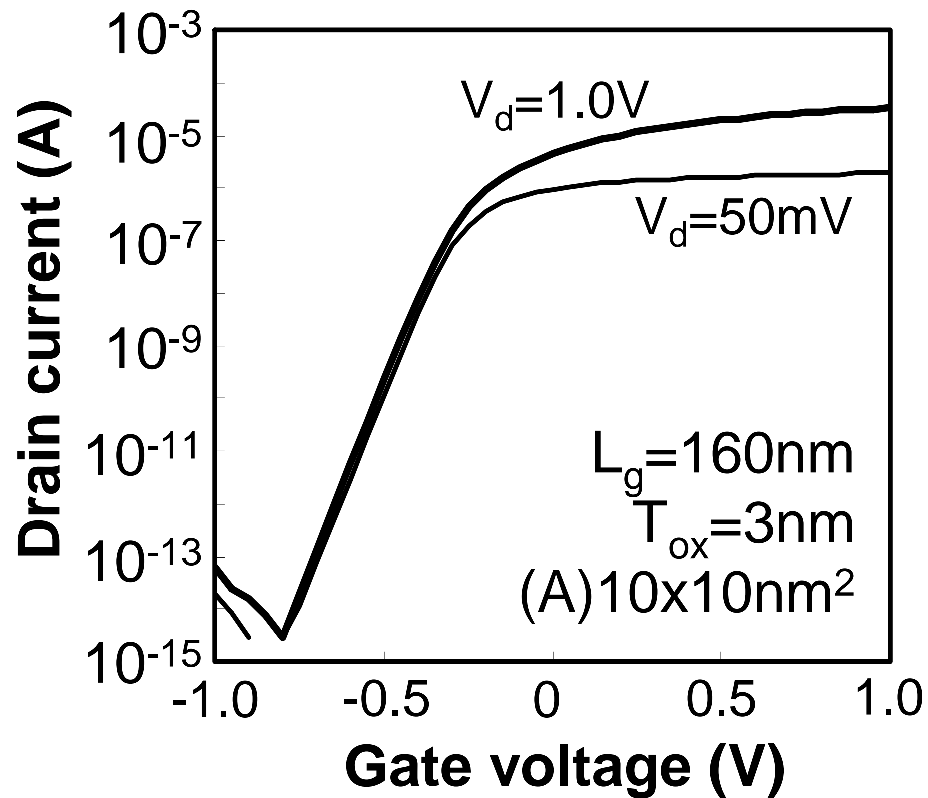
(a)

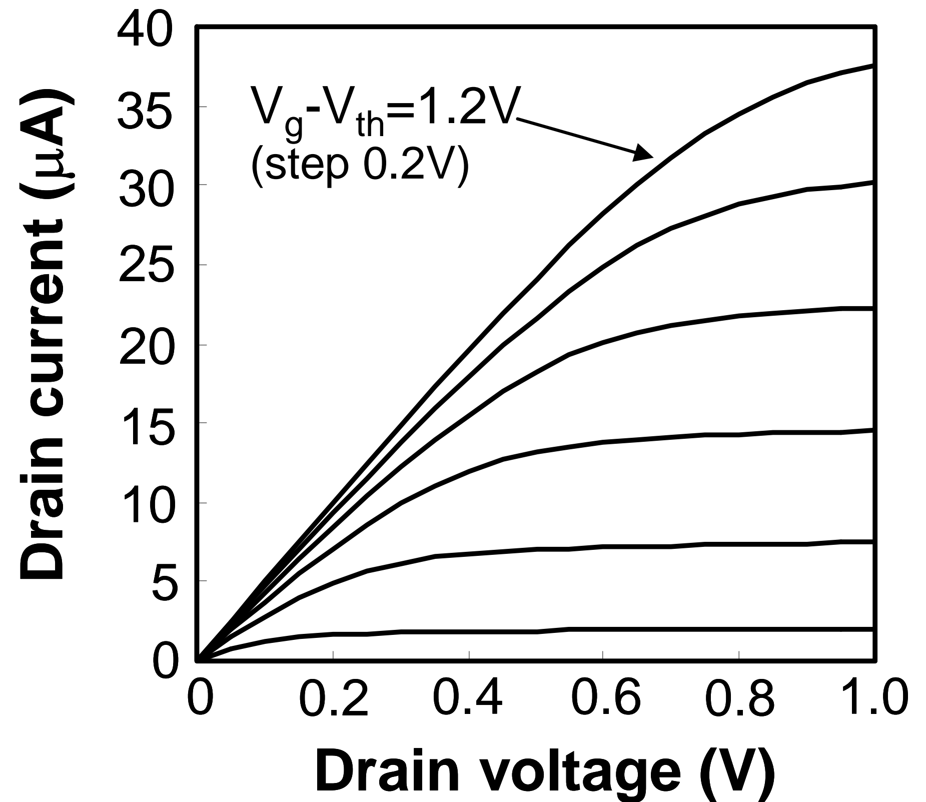


(b)

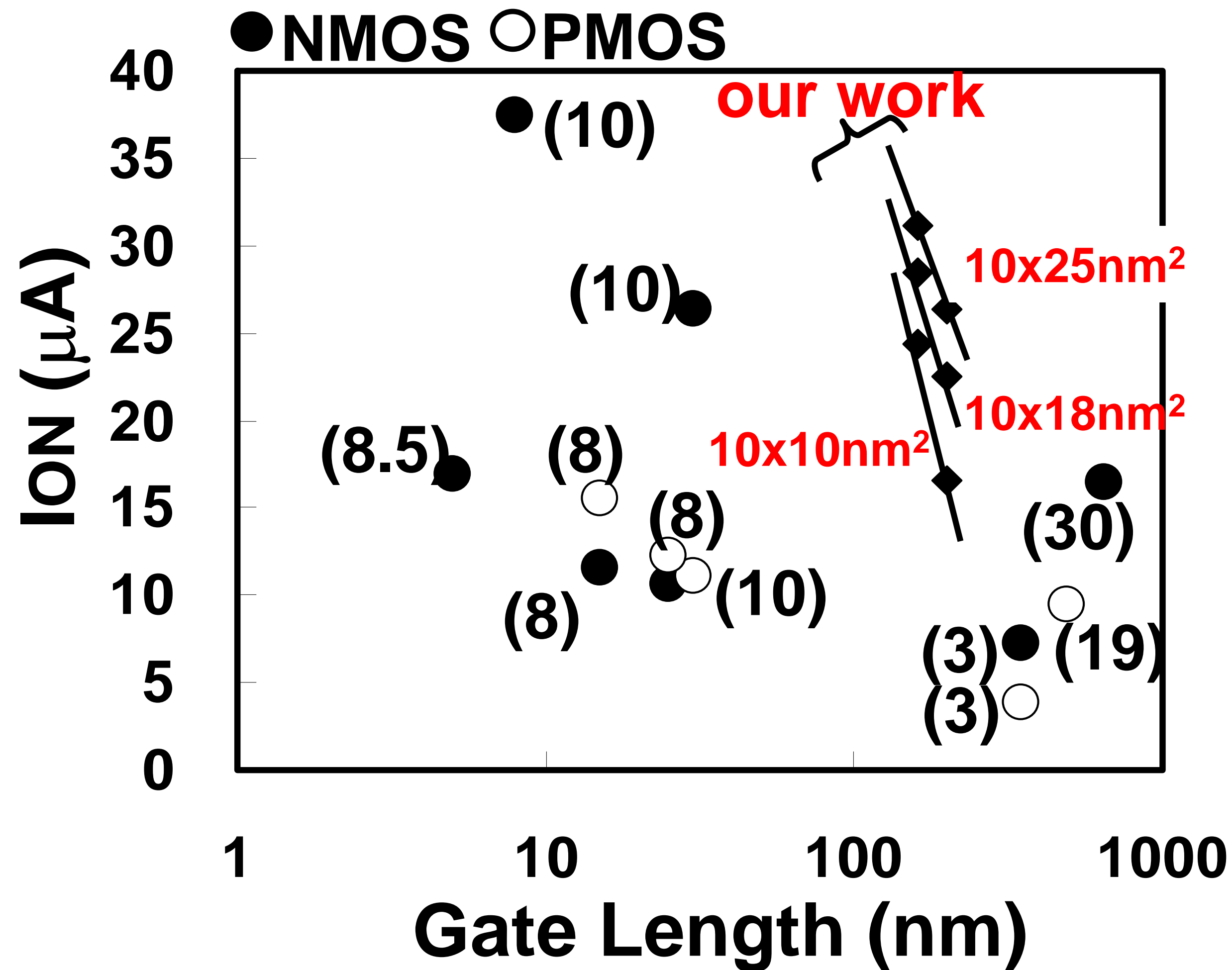


Output characteristics of 10x10cm^2 SiNW FET



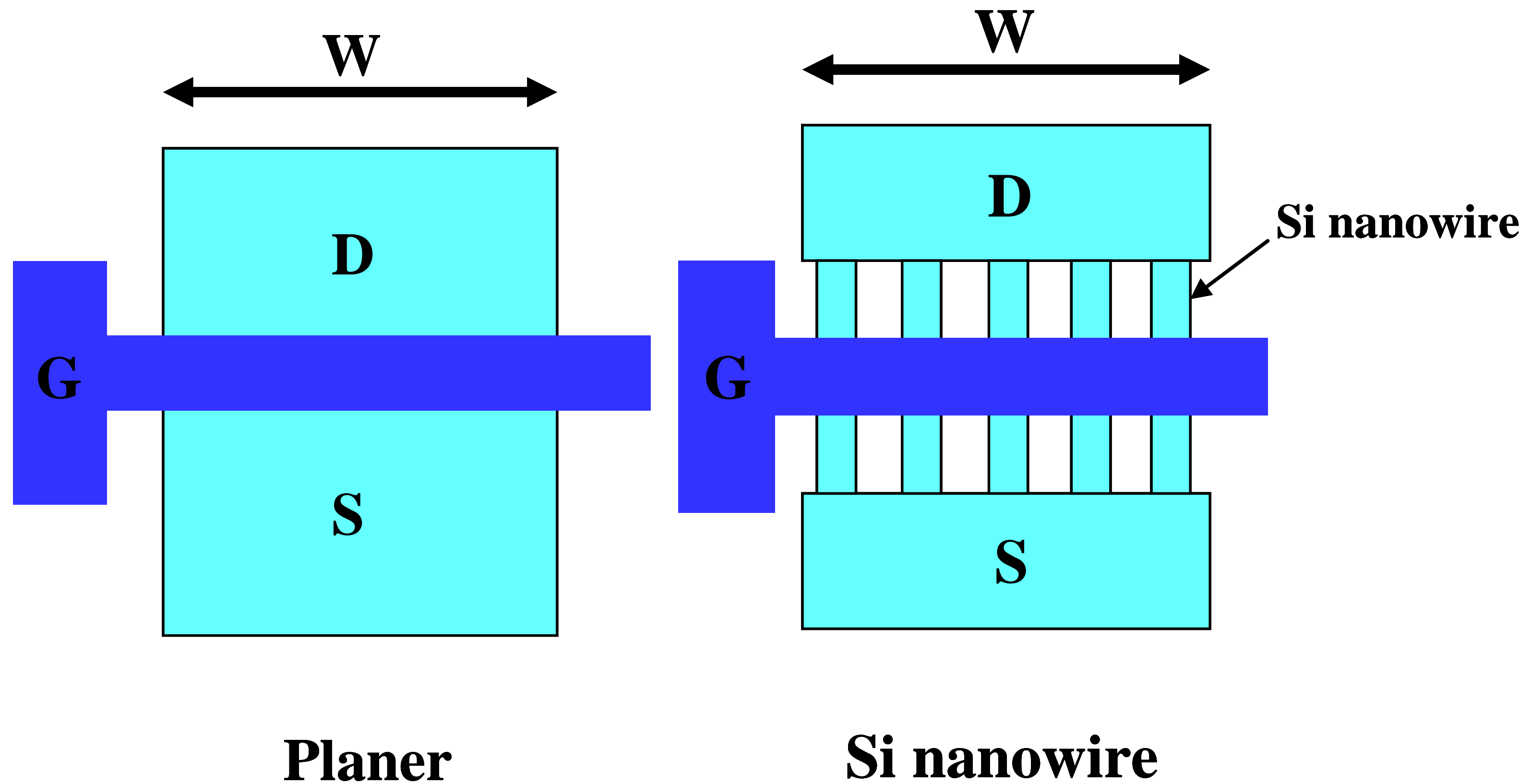


Obtained Ion with reported data

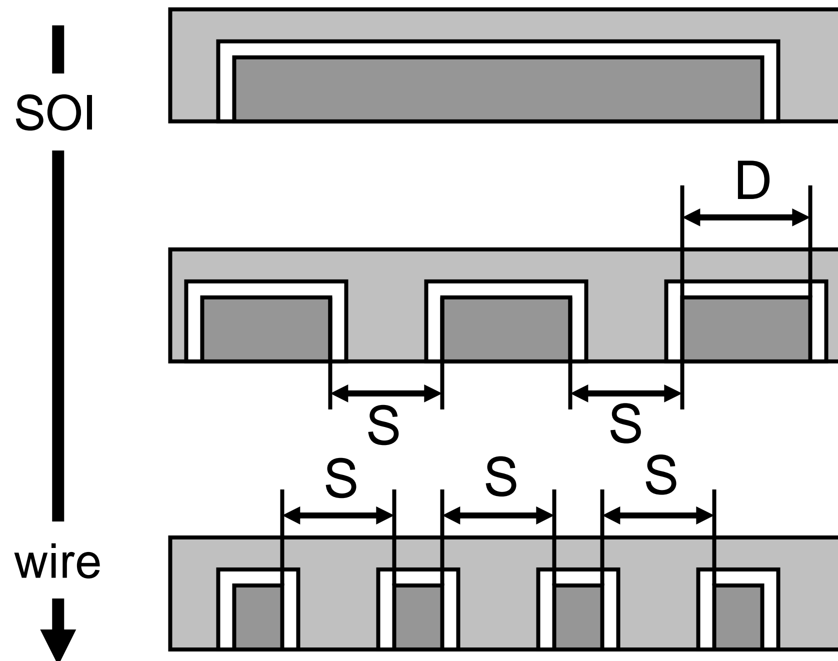


Even with large L_g, fairly nice I_{ON} have been achieved

Occupying area of Si bulk planar FET and Si NW FET.
Drive current should be compared with the same width, W



On current evaluation base on gate width



Year	half-pitch (nm), P
2010	45
2014	28
2018	18
2022	11

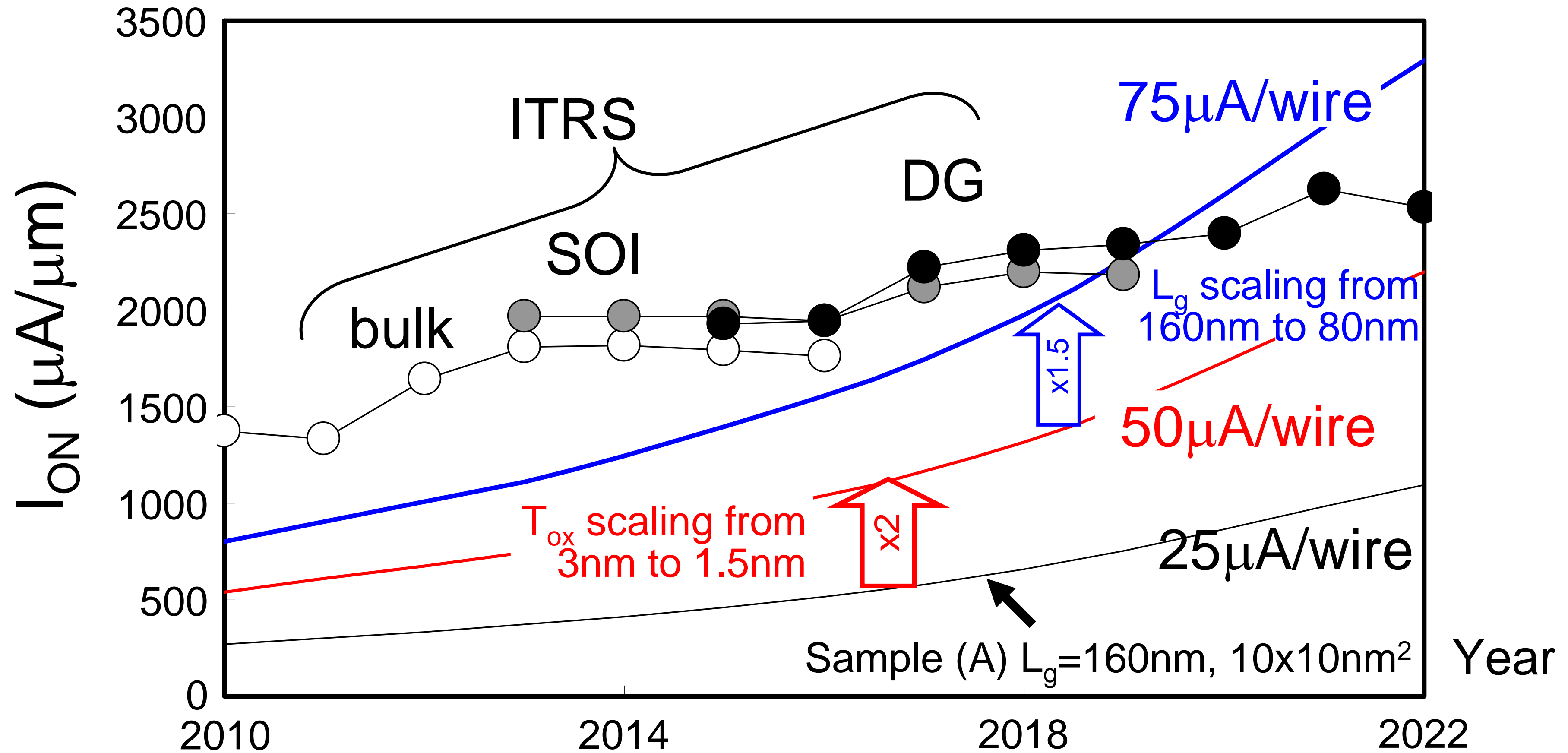
(based on ITRS2008update)

Numbers of wires are determined by the lithographic technology

$$\#N = \frac{1000(nm)}{P} \quad \text{or} \quad \frac{1000(nm)}{D+P/2}$$

(at D<P/2) (at D>P/2)

Performance of SiNW FET in ITRS

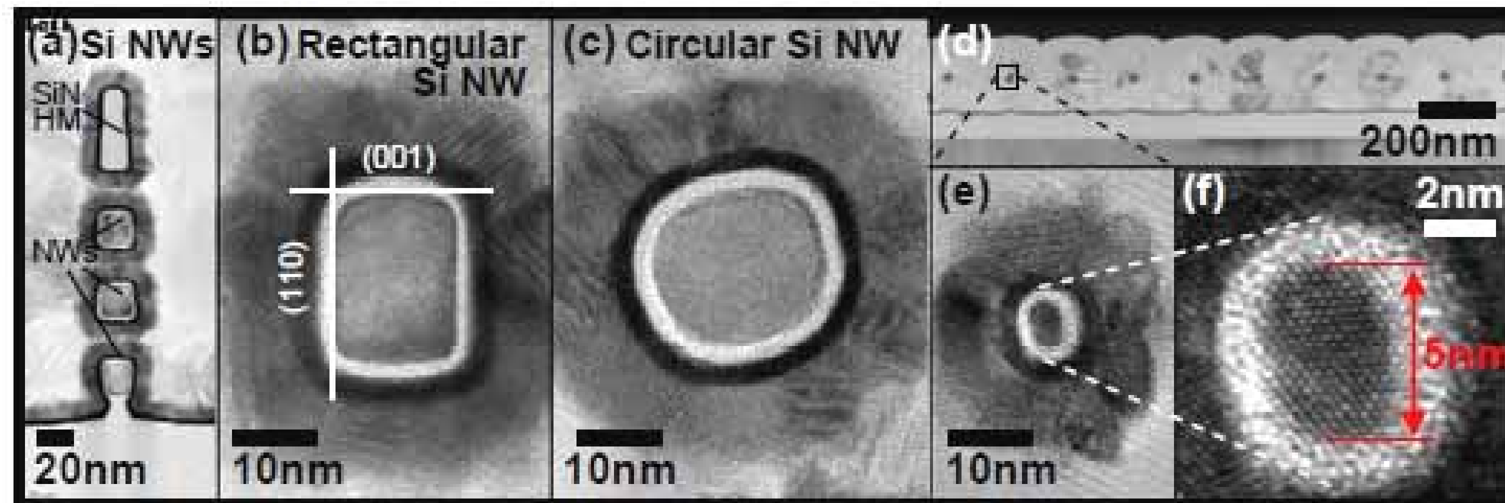


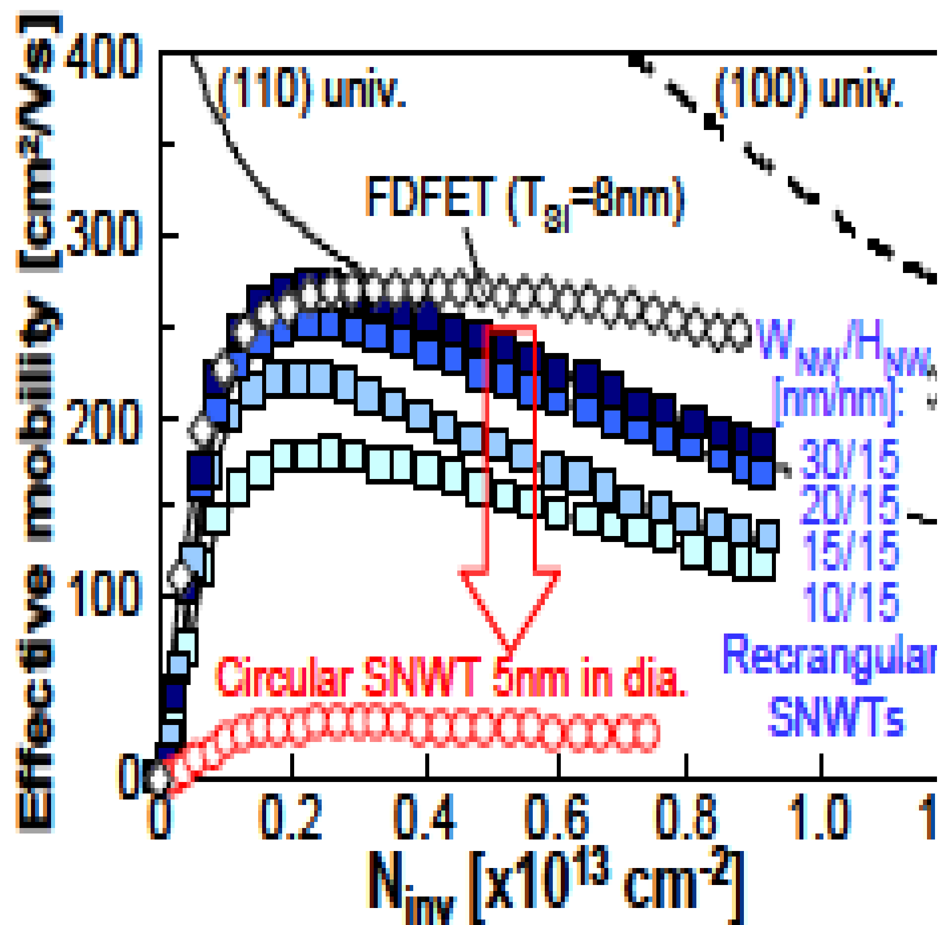
With device scaling in T_{ox} and L_g, SiNW FET can exceed the required performance in ITRS

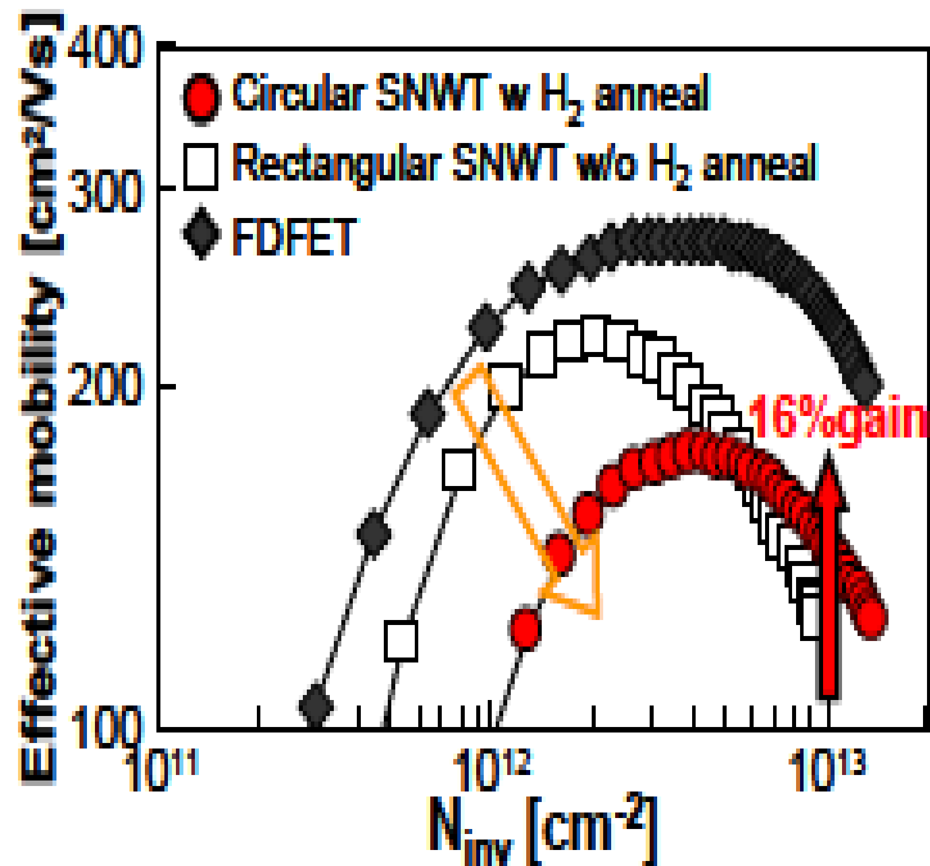
Joint work with LETI

Relationship between mobility and high-*k interface properties*
in advanced Si and SiGe nanowires

K. Tachi,, M. Casse, D. Jang2, C. Dupré, A. Hubert, N. Vulliet, V. Maffini-Alvaro,
C. Vizioz1,C. Carabasse1, V. Delaye, J. M. Hartmann, G. Ghibaudo,
H. Iwai4, S. Cristoloveanu, O. Faynot, and T. Ernst1

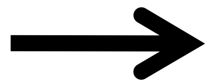



(110) univ.
(100) univ.
FDFET (T_{SI}=8nm)
W_{NW}/H_{NW} [nm/nm]:
30/15
20/15
15/15
10/15
Recrangular SNWTs
Circular SNWT 5nm in dia.
Effective mobility [cm²/Vs]
N_{inv} [x10¹³ cm⁻²]


Circular SNWT w H_2 anneal
Rectangular SNWT w/o H_2 anneal
FDFET
16%gain
Effective mobility [cm²/Vs]
N_{inv} [cm⁻²]

Si Nanowire FET

1. Good I-off control
2. High I-on
3. Fully compatible to Si-LSI process



Most promising candidate for
16 or 11 nm CMOS and beyond

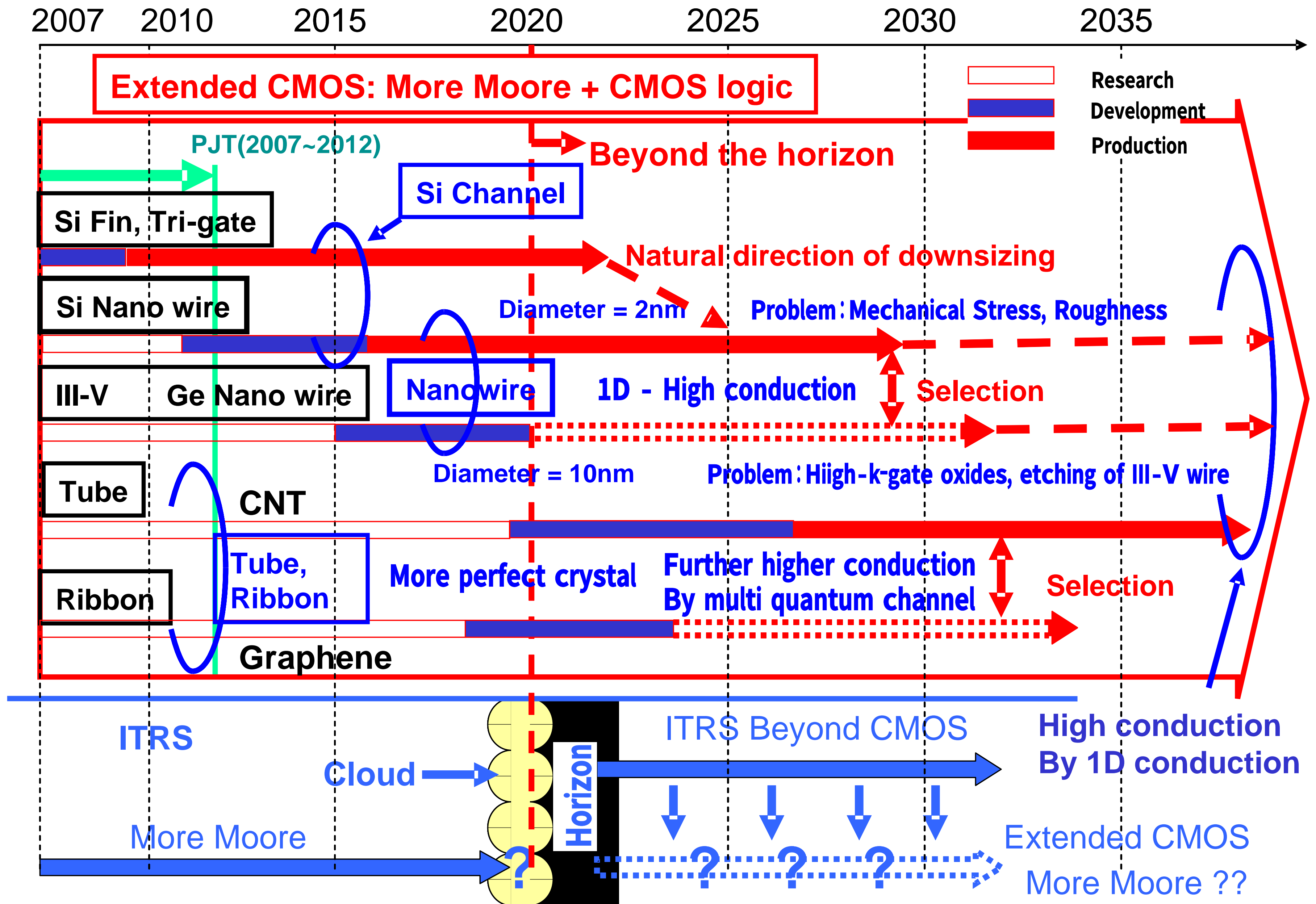
Many things to do for Si nanowire FETs

1. No optimum diameter/orientation/, cross-section shape are known, both from theory and experiments

2. No compact model for I-V exists, with diameter, orientation, cross-section shape, gate length as a parameter.

3. So many unknown things;

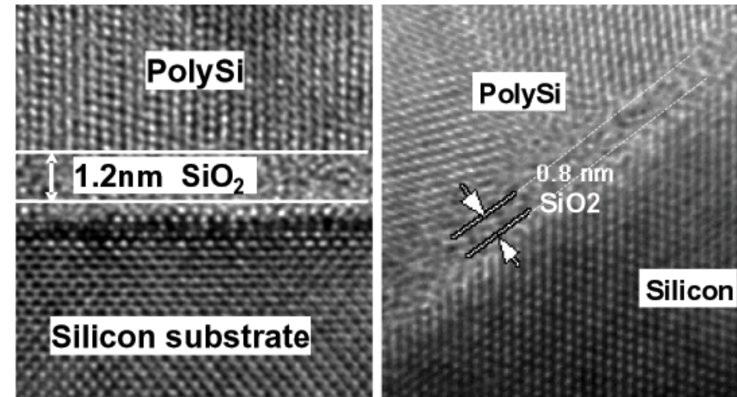
   Mobility, Oxidation, Strain, etc.



Our new roadmap
2007
2010
2015
2020
2025
2030
2035
Extended CMOS: More Moore + CMOS logic
Research
Development
Production
PJT(2007~2012)
Beyond the horizon
Si Channel
Si Fin, Tri-gate
Natural direction of downsizing
Si Nano wire
Diameter = 2nm
Problem：Mechanical Stress, Roughness
III-V
Ge Nano wire
Nanowire
1D - High conduction
Selection
Diameter = 10nm
Problem：Hiigh-k-gate oxides, etching of III-V wire
Tube
CNT
Tube,
Ribbon
More perfect crystal
Further higher conduction
By multi quantum channel
Selection
Ribbon
Graphene
ITRS
ITRS Beyond CMOS
High conduction
By 1D conduction
Cloud
Horizon
More Moore
Extended CMOS
More Moore ??

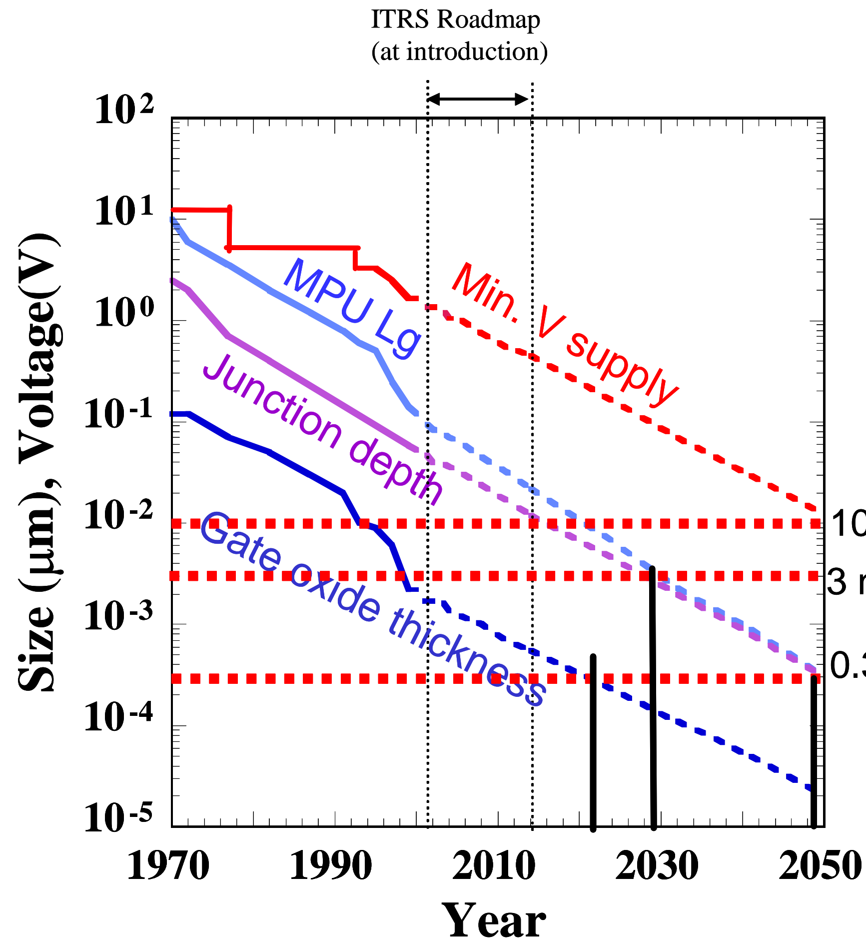
Scaling Limit in MOSFET

SiO2 Scaling



- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

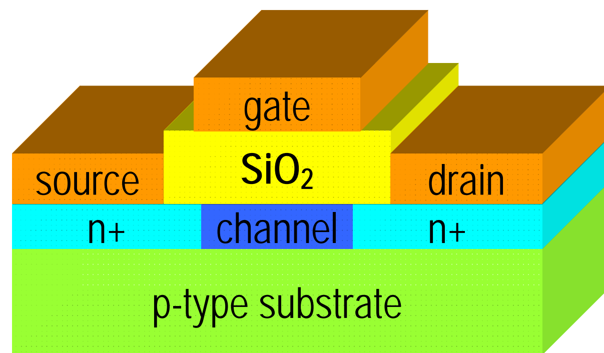
By Robert Chau, IWGI 2003

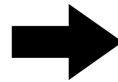


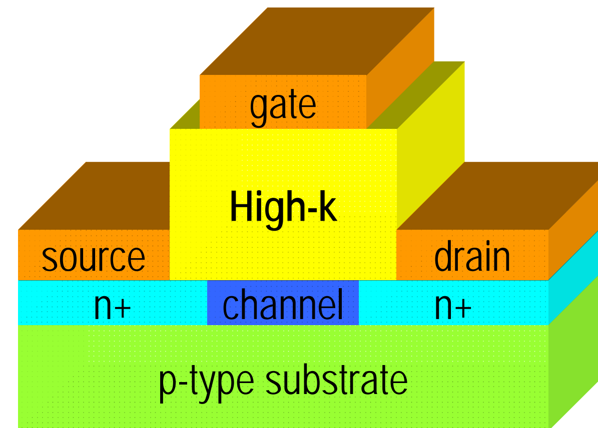
ULTIMATE LIMIT

High-k Thin Film for Gate Insulator

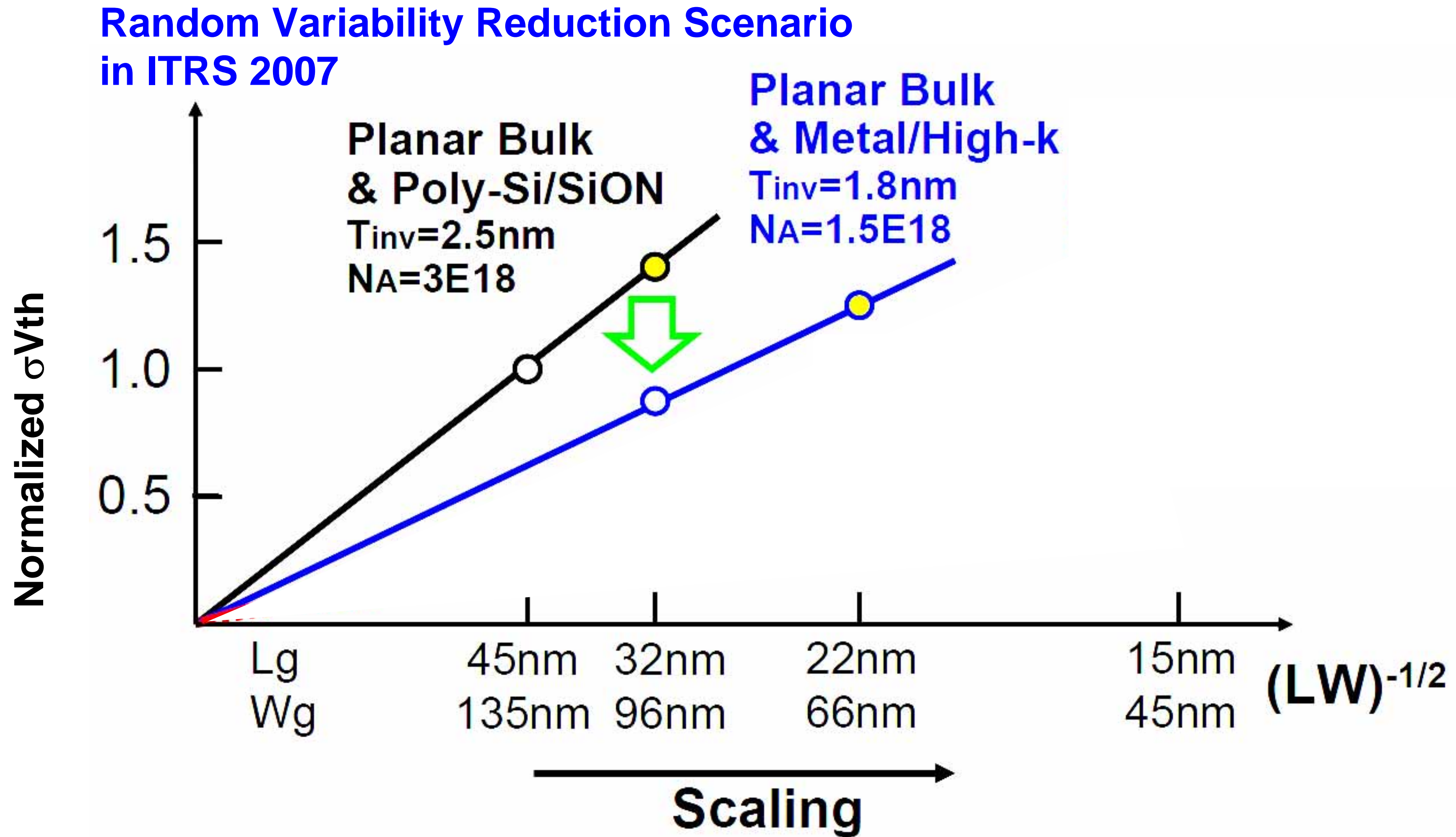
<u>MOSFET</u>







Gate oxide scaling is very important also for suppressing the variation.



Source: 2007 ITRS Winter Public Conf.

Historical trend of high-k R& D

1960 1970 1980 1990 2000 05

MOSFET Gate Stack in production

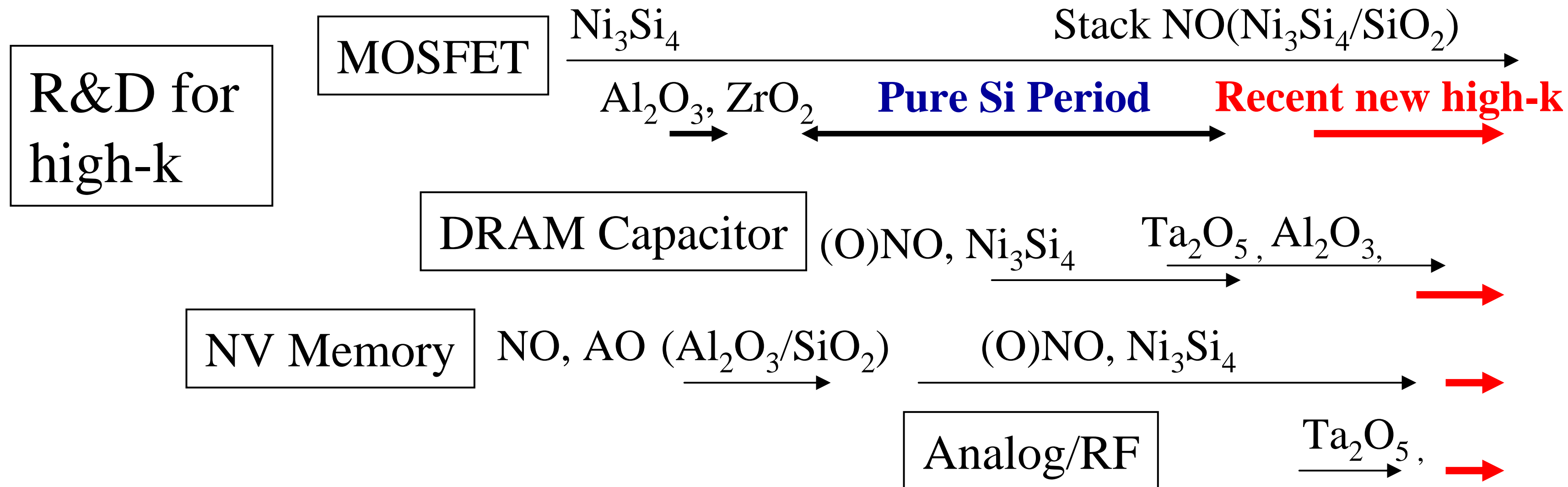
1st FET IC LSI

PMOS NMOS CMOS

Gate insulator: SiO_2 | SiO_xN_y

Gate electrode: Al | N^+Poly Si | Double Poly Si

Silicide above Poly Si electrode: $MoSi_2$ → | WSi_2 | $TiSi_2$ | $CoSi_2$ | ← NiSi



Choice of High-k

Candidates (cyan)

● Gas or liquid at 1000 K

Unstable at Si interface

① $Si + MO_X$ $M + SiO_2$

② $Si + MO_X$ $MSi_X + SiO_2$

③ $Si + MO_X$ $M + MSi_XO_Y$

○ Radio active

● H																	● He
Li	Be											● B	● C	● N	● O	● F	● Ne
① Na	Mg											Al	Si	● P	● S	● Cl	● Ar
K	Ca	Sc	② Ti	① V	① Cr	① Mn	① Fc	① Co	① Ni	① Cu	① Zn	① Ga	① Ge	● As	● Se	● Br	● Kr
● Rh	Sr	Y	Zr	① Nb	① Mo	Tc	① Ru	① Rb	① Pd	● Ag	① Cd	① In	① Sn	① Sb	① Te	● I	● Xe
● Cs	③ Ba	★	Hf	① Ta	① W	① Re	① Os	① Ir	● Pt	● Au	● Hg	● Tl	① Pb	① Bi	○ Po	○ At	○ Rn
○ Fr	○ Ra	☆	○ Rf	○ Ha	○ Sg	○ Ns	○ Hs	○ Mt									

★	La	Ce	Pr	Nd	○ Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
☆	○ Ac	○ Th	○ Pa	○ U	○ Np	○ Pu	○ Am	○ Cm	○ Bk	○ Cf	○ Es	○ Fm	○ Md	○ No	○ Lr

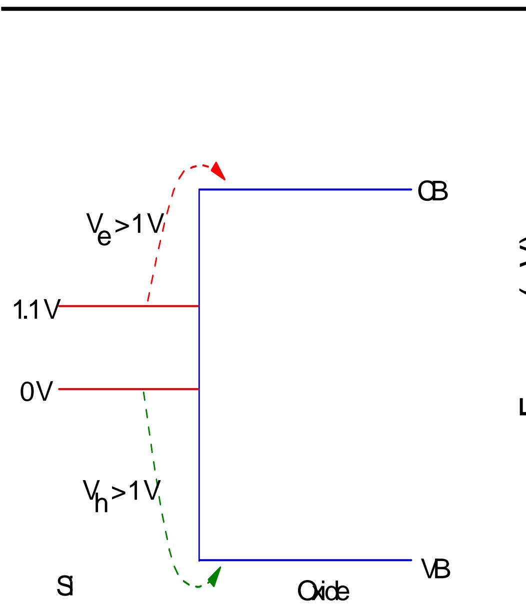
HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

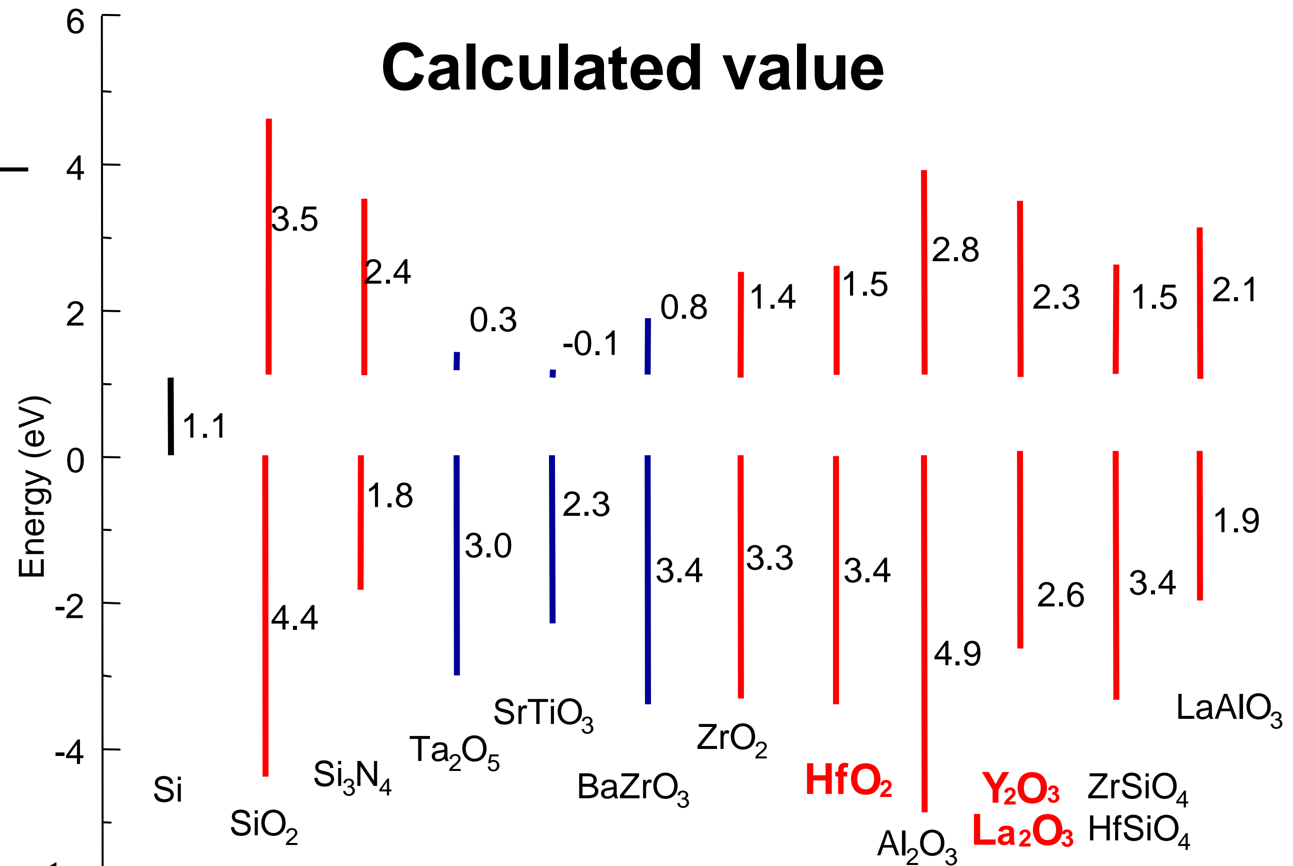
La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999

Hubbard and Schlom, J Mater Res 11 2757 (1996)

Band Offsets





J Robertson, J Vac Sci Technol B **18** 1785 (2000)

Dielectric constant

SiO2; 4
Si3N4: ~ 7
Al2O3: ~ 9

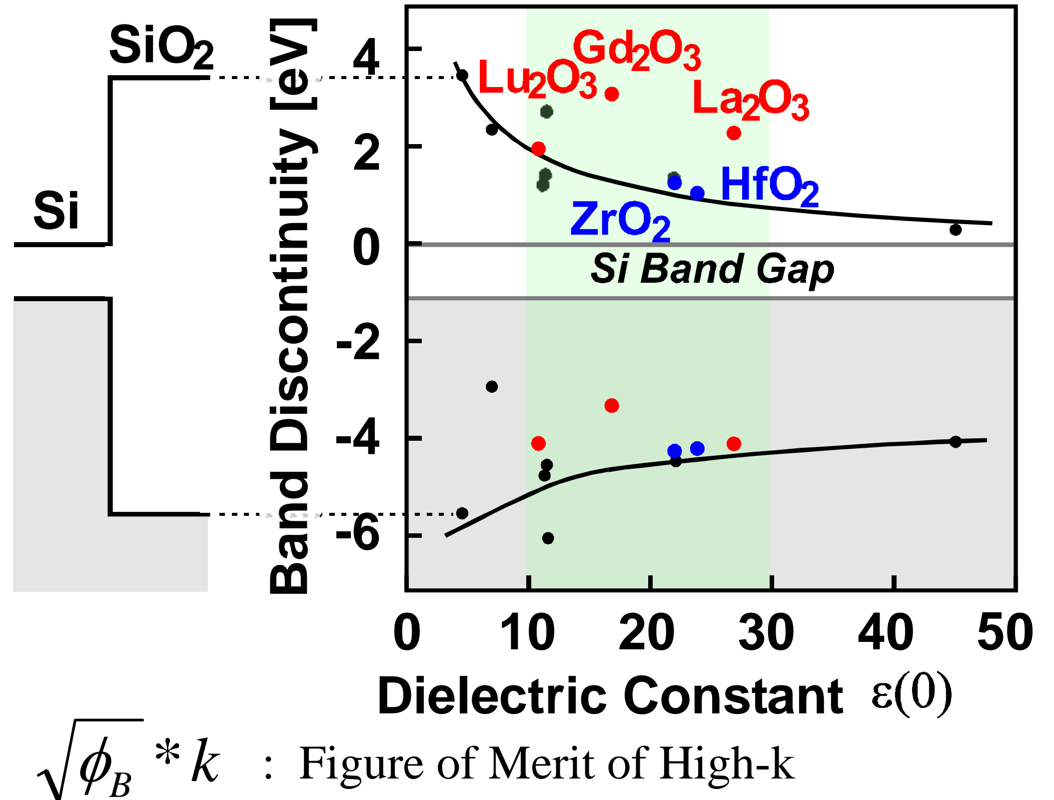
Y2O3; ~10
Gd2O3: ~10

HfO2; ~23
La2O3: ~27

HfO2 was chosen for the 1st generation
La2O3 is more difficult material to treat

Dielectric constant value vs. Band offset (Measured)

SiO_2	3.9
Al_xSi_yOz	
$(Ba,Sr)TiO_3$	200-300
$BeAl_2O4$	8.3-9.43
CeO_2	16.6-26
$CeHfO_4$	10-20
$CoTiO_3/Si_3N_4$	
$EuAlO_3$	22.5
HfO_2	26-30
Hf silicate	11
La_2O_3	20.8
$LaScO_3$	30
La_2SiO_5	
$MgAl_2O_4$	
$NdAlO_3$	22.5
$PrAlO_3$	25
Si_3N_4	7
$SmAlO_3$	19
$SrTiO_3$	150-250
Ta_2O_5	25-24
Ta_2O_5-TiO_2	
TiO_2	86-95
TiO_2/Si_3N_4	
Y_2O_3	8-11.6
$Y_xSi_yO_z$	
ZrO_2	22.2-28
Zr-Al-O	
Zr silicate	
$(Zr,Sn)TiO_4$	40-60

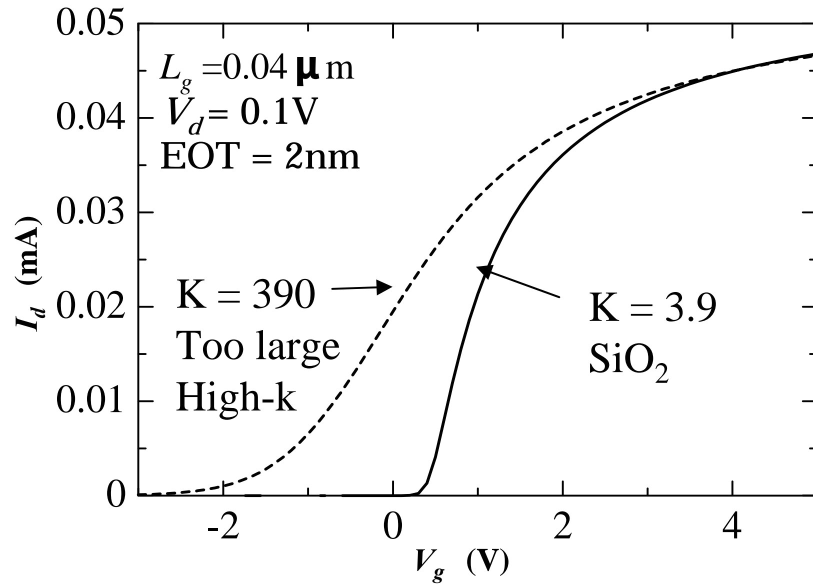


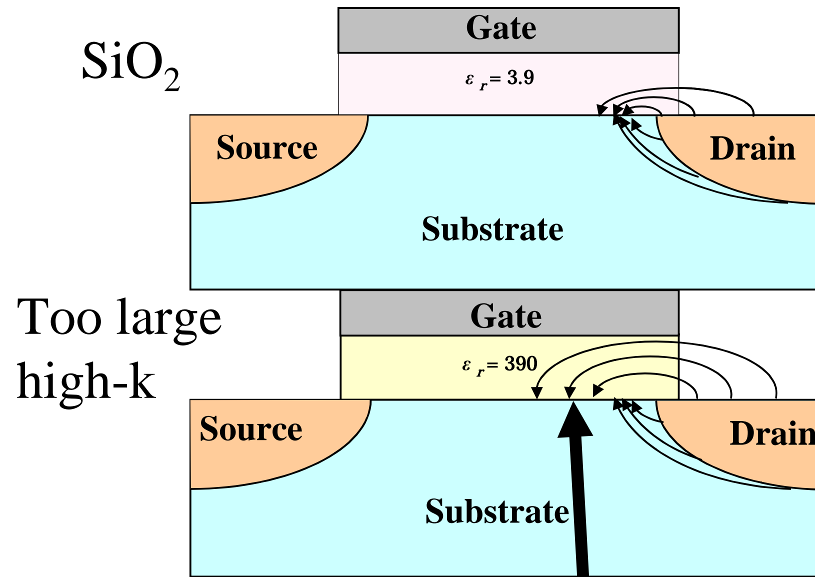
$\sqrt{\phi_B} * k$: Figure of Merit of High-k

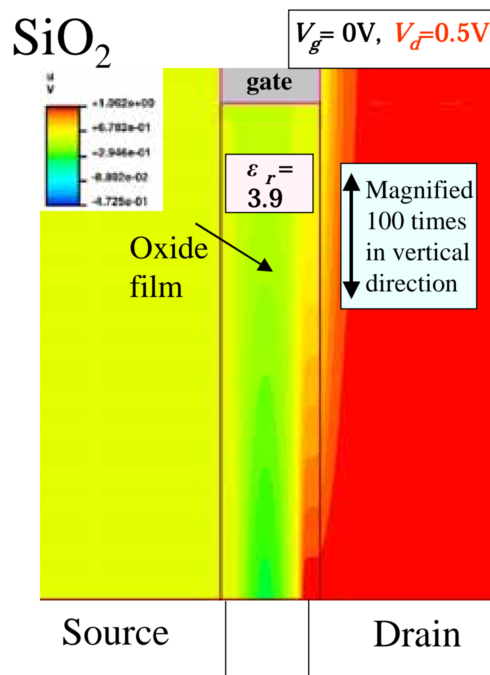
C.A. Billmann et al.,, MRS Spring Symp., 1999,
R.D.Shannon, J. Appl. Phys., 73, 348, 1993
S. De Gebdt, IEDM Short Coyuse, 2004

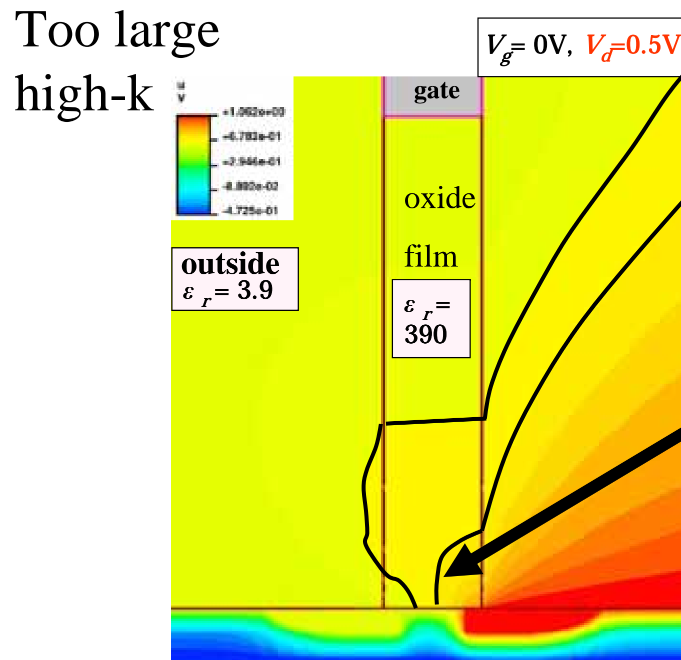
T. Hattori, INFOS , 2003

Too large high-k cause significant short channel effect





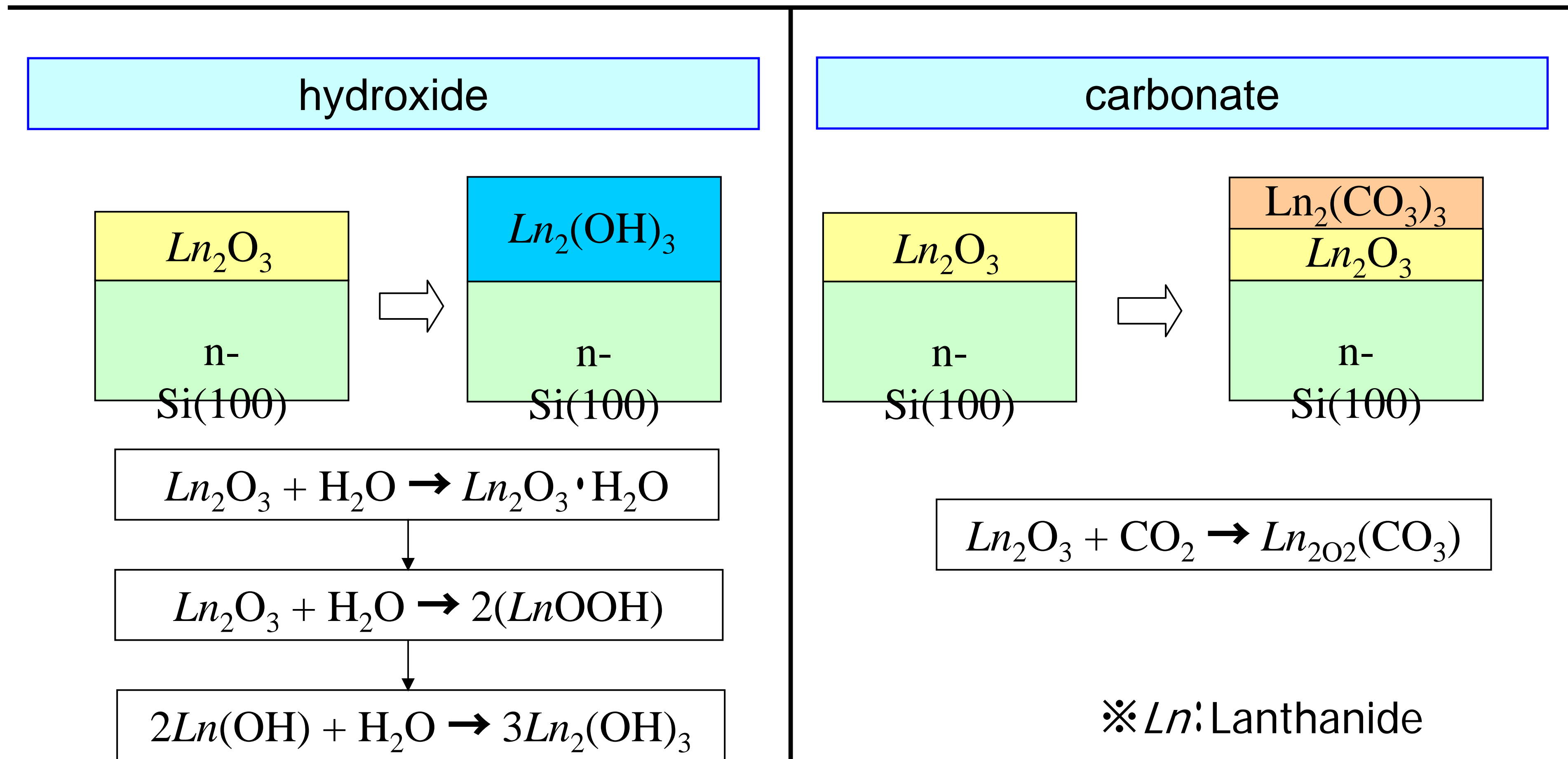




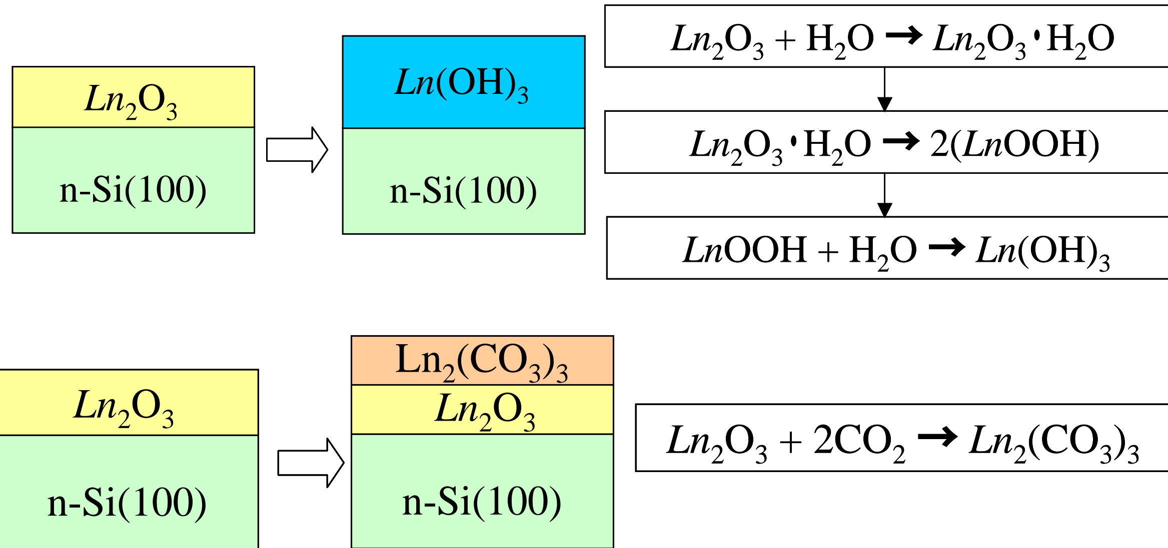
Penetration of lateral field from Drain through high-k causes significant short channel effects

Absorption of moisture and CO_2

The oxides become hydroxide and carbonate in H_2O and CO_2 ambient.



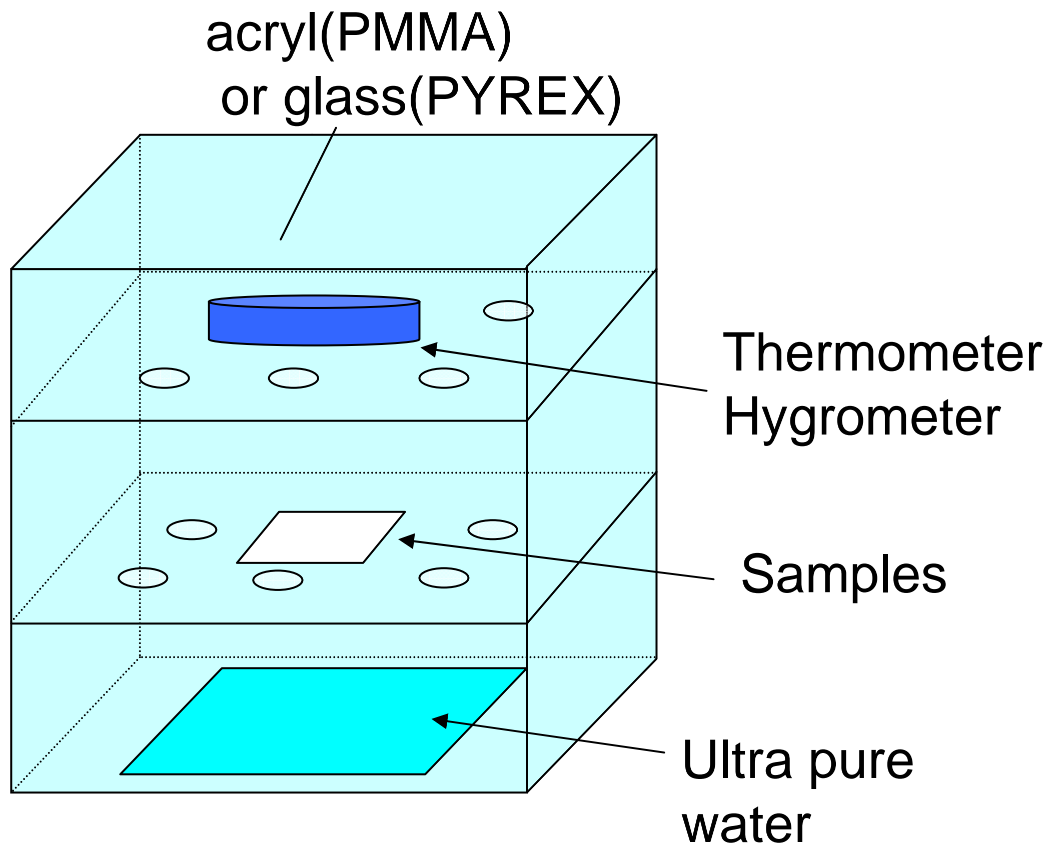
Hygroscopic Properties of La_2O_3



After 30 hours in clean room (temperature & humidity controlled)

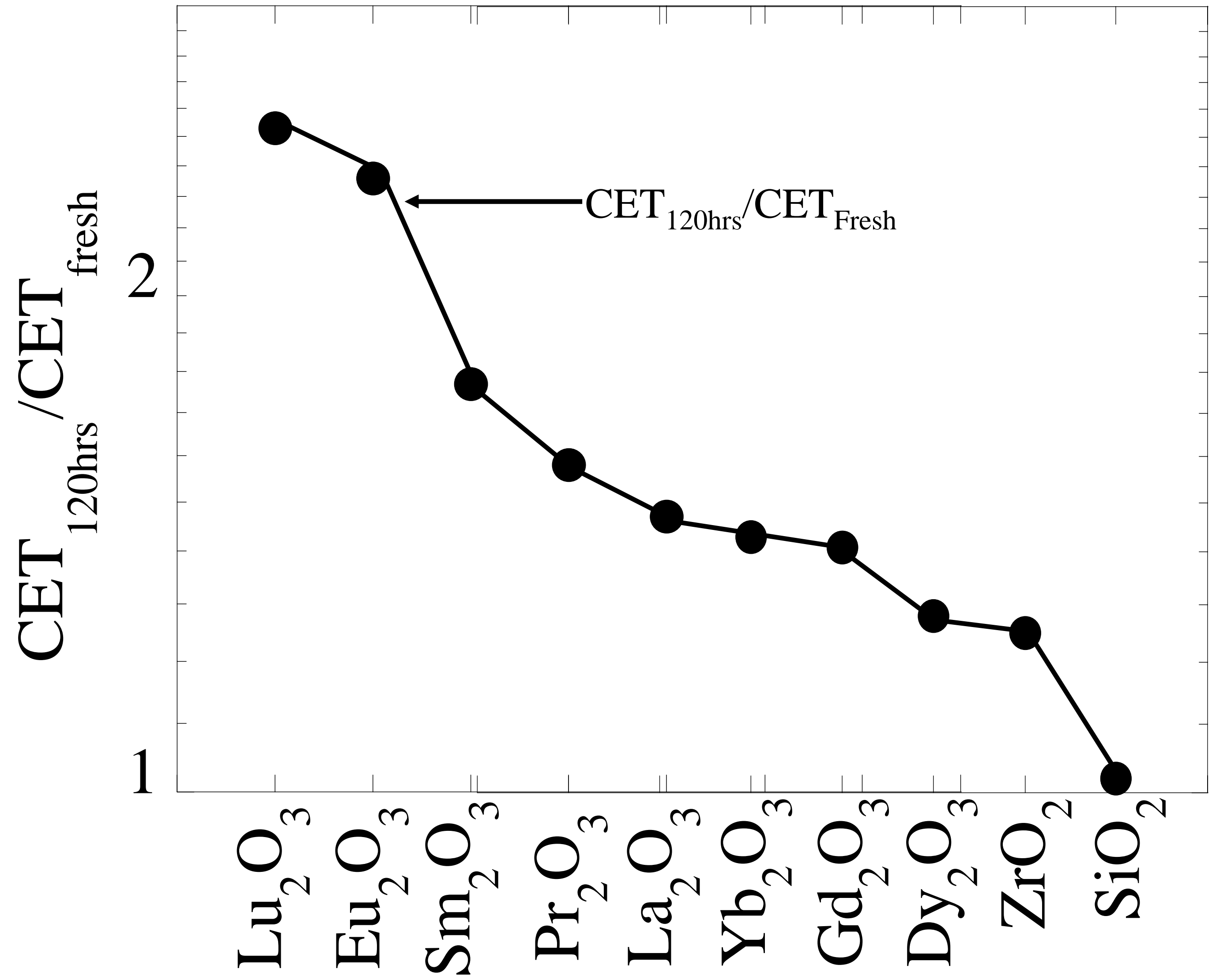
Experimental apparatus

Temperature: ~20°C
Humidity: 80%
Humidification time:
0 ~120 hrs



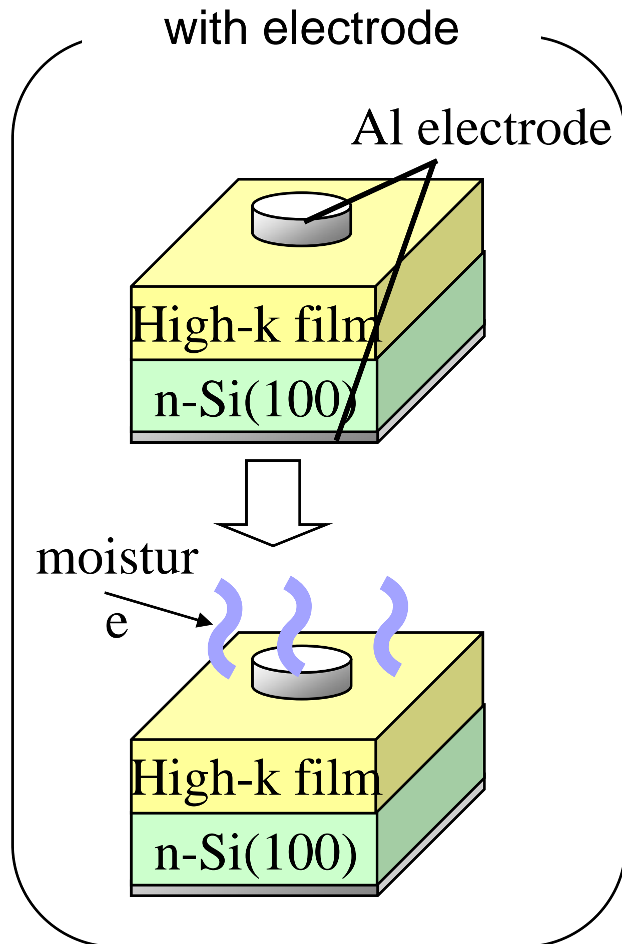
*PMMA :
$CH_2C(CH)_3COOCH_3$

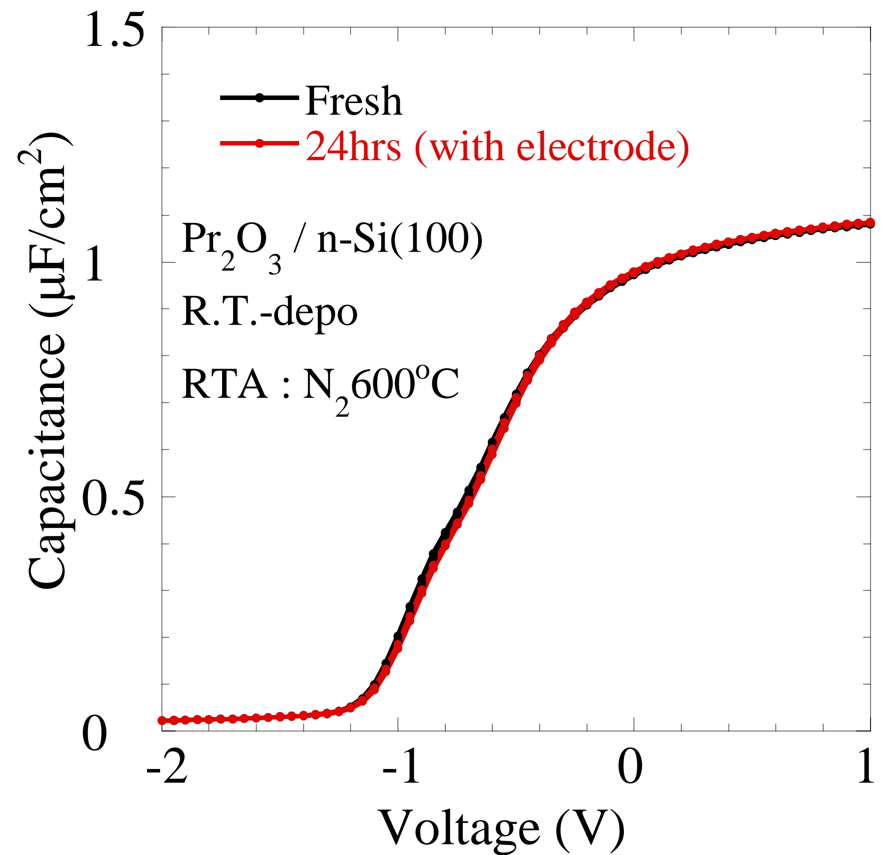
Change of CET for all studied



Absorption test in case of acryl apparatus
after the Al electrode formation

→ Moisture absorption is protected





Choice of High-k

Candidates (shaded)

● Gas or liquid at 1000 K

○ Radio active

Unstable at Si interface

① $Si + MO_X \quad M + SiO_2$

② $Si + MO_X \quad MSi_X + SiO_2$

③ $Si + MO_X \quad M + MSi_XO_Y$

● H ● He

Li Be ● B ● C ● N ● O ● F ● Ne

① Na Mg Al Si ● P ● S ● Cl ● Ar

K Ca Sc ② Ti ① V ① Cr ① Mn ① Fc ① Co ① Ni ① Cu ① Zn ① Ga ① Ge ● As ● Se ● Br ● Kr

● Rh Sr Y Zr ① Nb ① Mo Tc ① Ru ① Rb ① Pd ● Ag ① Cd ① In ① Sn ① Sb ① Te ● I ● Xe

● Cs ③ Ba ★ Hf ① Ta ① W ① Re ① Os ① Ir ● Pt ● Au ● Hg ● Tl ① Pb ① Bi ○ Po ○ At ○ Rn

○ Fr ○ Ra ☆ ○ Rf ○ Ha ○ Sg ○ Ns ○ Hs ○ Mt

★ La Ce Pr Nd ○ Pm Sm Eu Gd Tb Dy Ho Er Tm Yb Lu

☆ ○ Ac ○ Th ○ Pa ○ U ○ Np ○ Pu ○ Am ○ Cm ○ Bk ○ Cf ○ Es ○ Fm ○ Md ○ No ○ Lr

HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

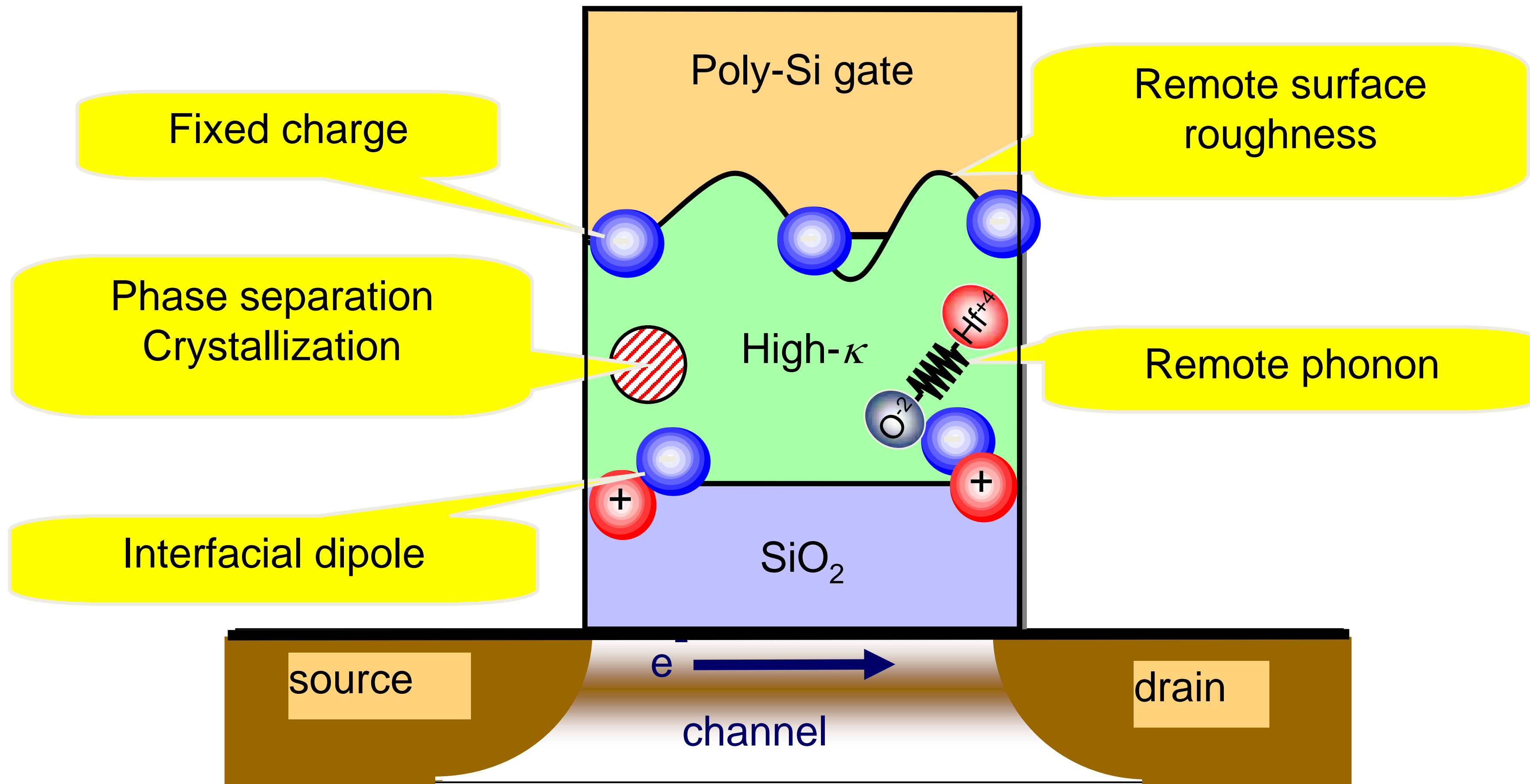
La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999

Hubbard and Schlom, J Mater Res 11 2757 (1996)

Mobility degradation causes for High-k MOSFETs (HfO_2, Al_2O_3 based oxide)

Remote scattering is dominant

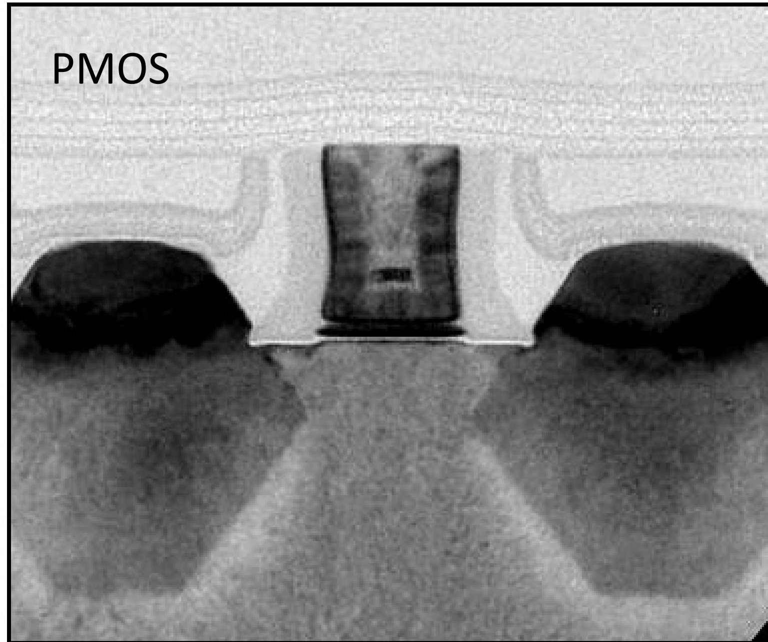


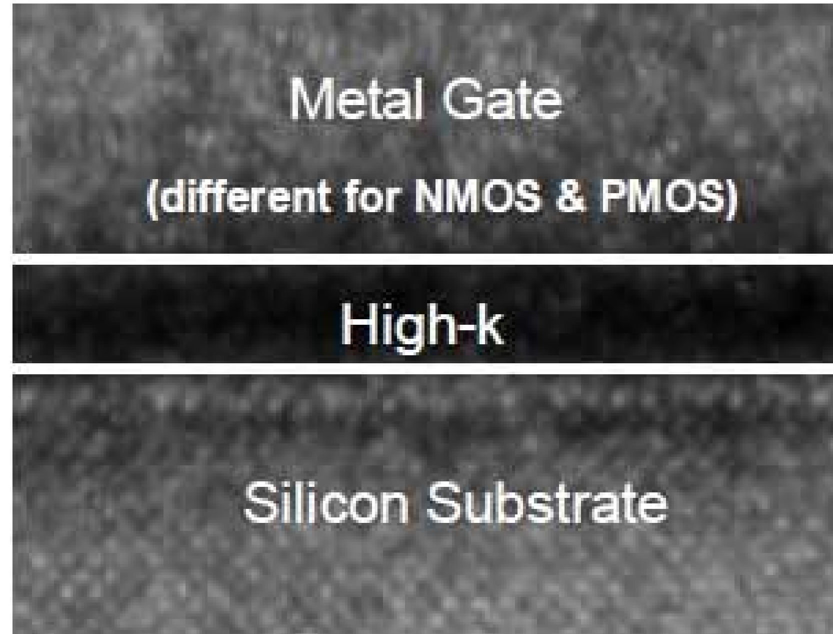
S. Saito et al., IEDM 2003,

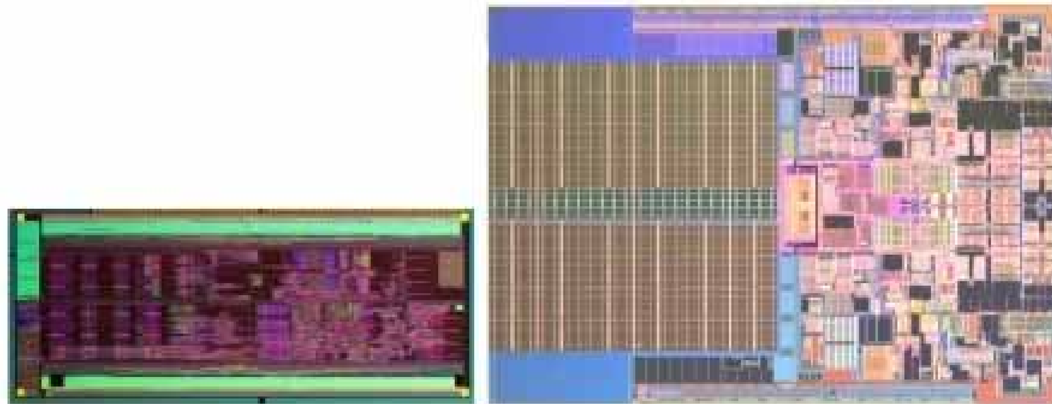
S. Saito et al., ECS Symp. on ULSI Process Integration

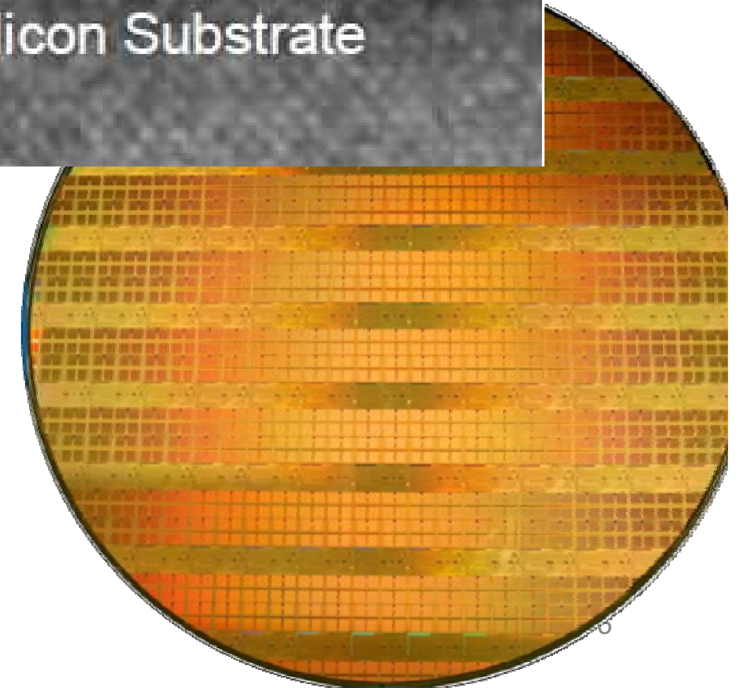
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness

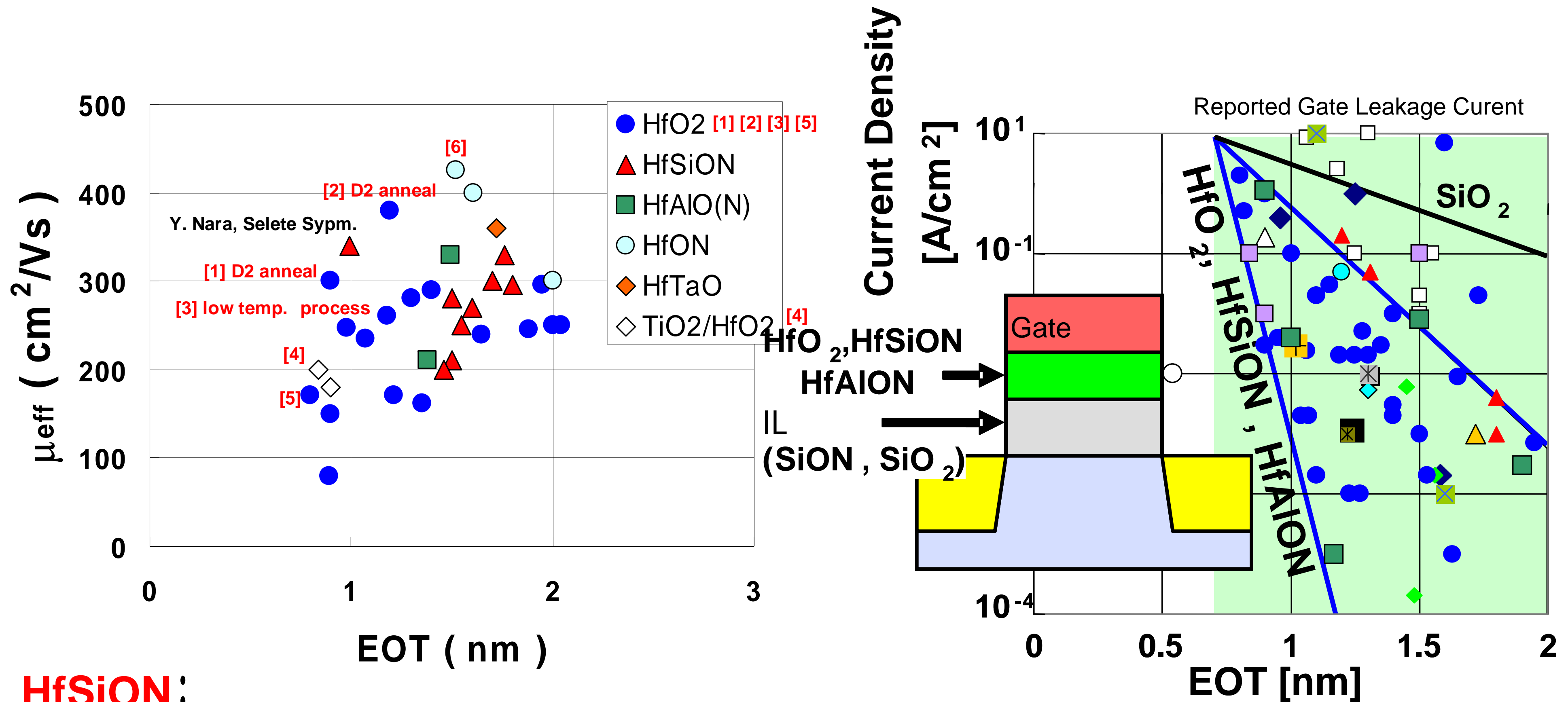








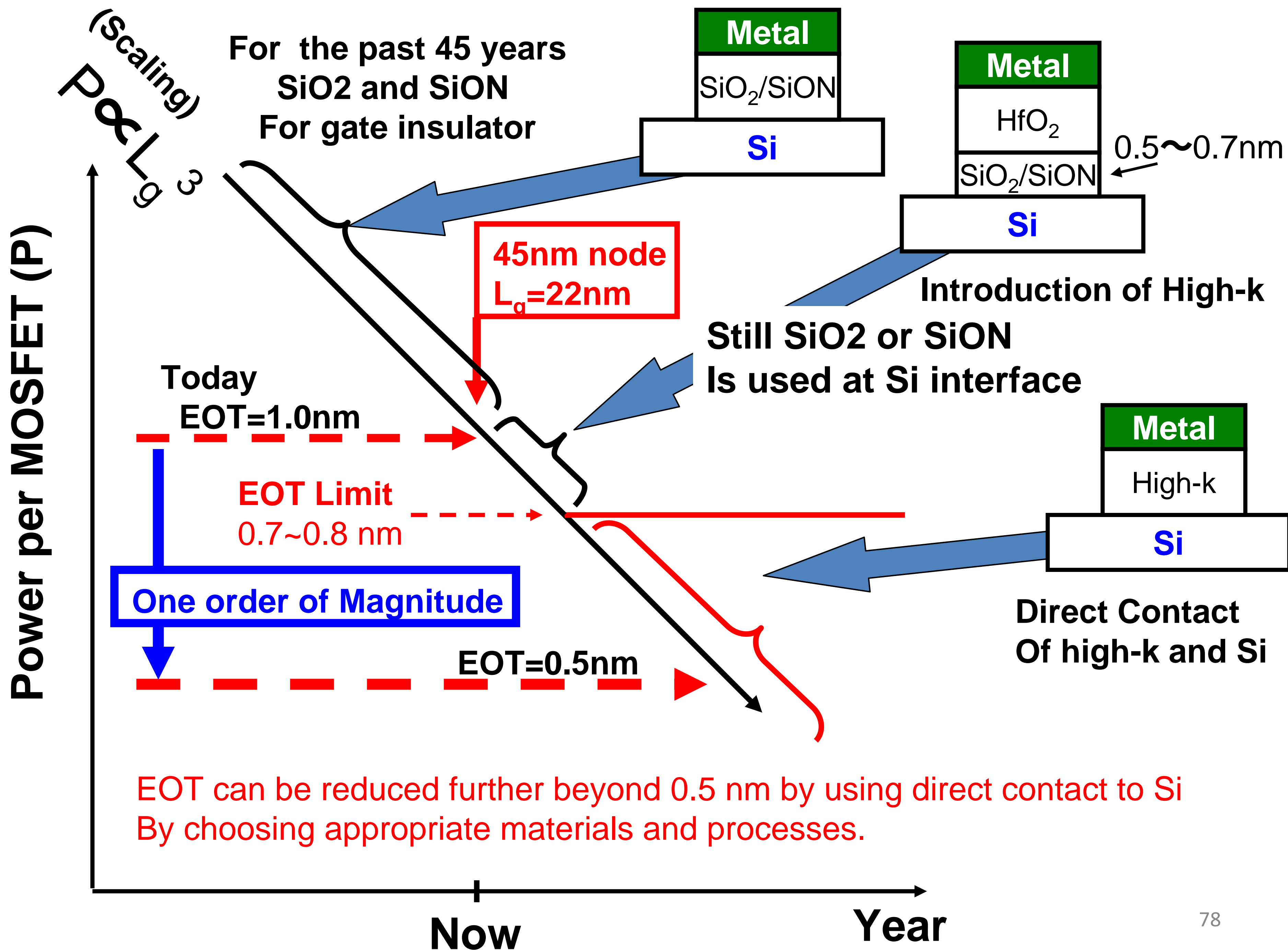
Present Status of high-k Research



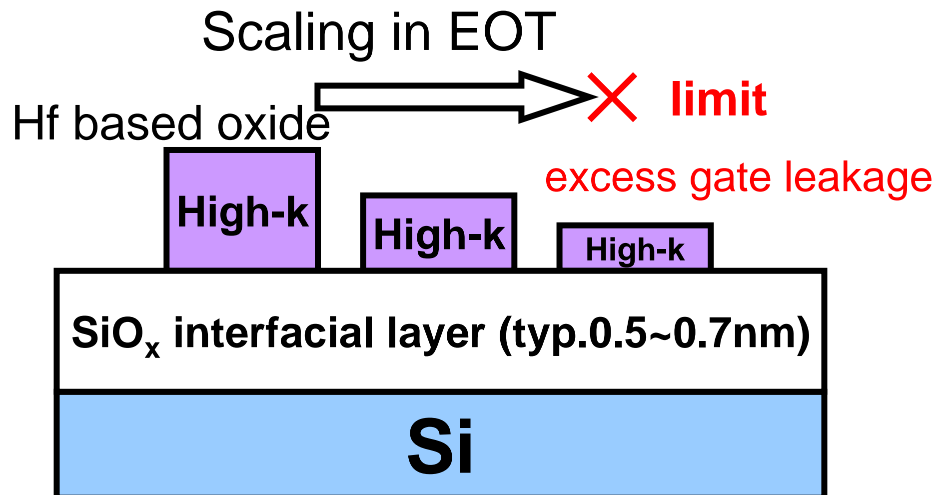
HfSiON:

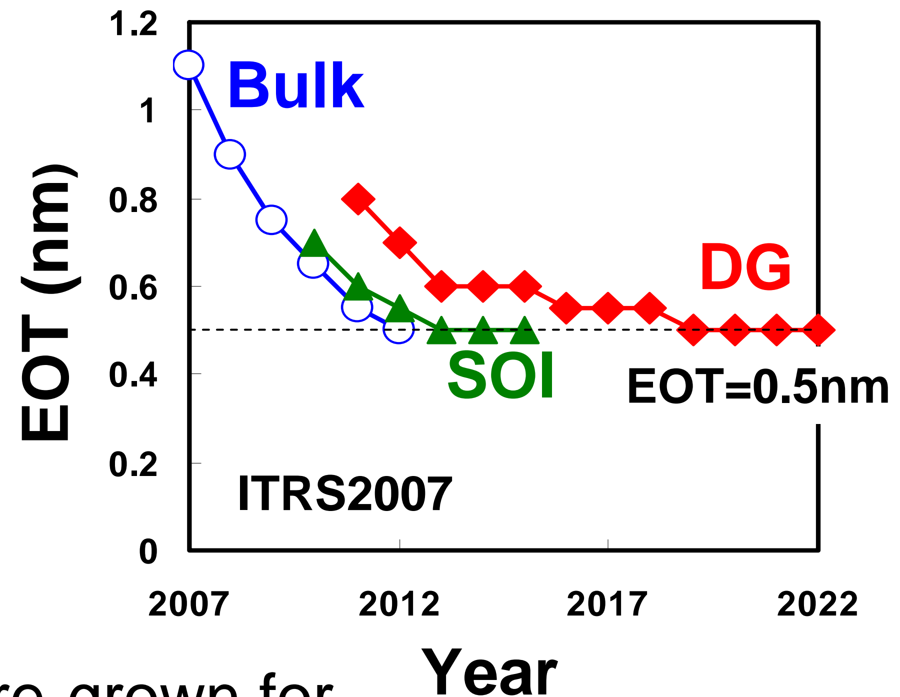
- **High effective mobility even at EOT=1nm**
- **Thermal stability**
- **IL of 0.5~0.7nm is essential for high μ**
- **Difficult to achieve EOT<0.7nm ?**

[1]C. Choi, VLSI05
[2]R. Choi, IEDM02
[3]Y. Akasaka, VLSI05
[4]S. J. Rhee, IEDM04
[5] L. A. Rangersson, VLSI05
[6]C. H. Choi, IEDM02
[7]S. J. Rhee, VLSI05


(Scaling)
P ∝ Lg 3
For the past 45 years
SiO2 and SiON
For gate insulator
Metal
SiO2/SiON
Si
Metal
HfO2
0.5~0.7nm
SiO2/SiON
Si
Introduction of High-k
45nm node
Lg=22nm
Still SiO2 or SiON
Is used at Si interface
Power per MOSFET (P)
Today
EOT=1.0nm
EOT Limit
0.7~0.8 nm
Metal
High-k
Si
One order of Magnitude
EOT=0.5nm
Direct Contact
Of high-k and Si
EOT can be reduced further beyond 0.5 nm by using direct contact to Si
By choosing appropriate materials and processes.
Now
Year

High-k for Further Scaling

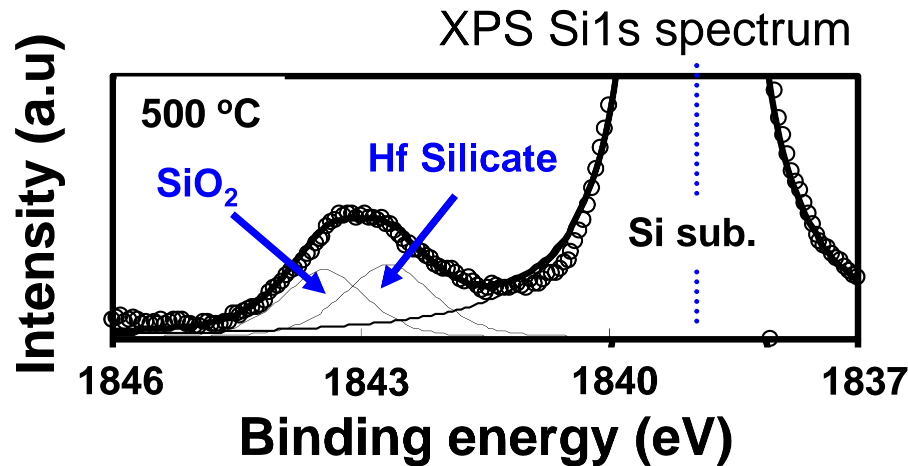


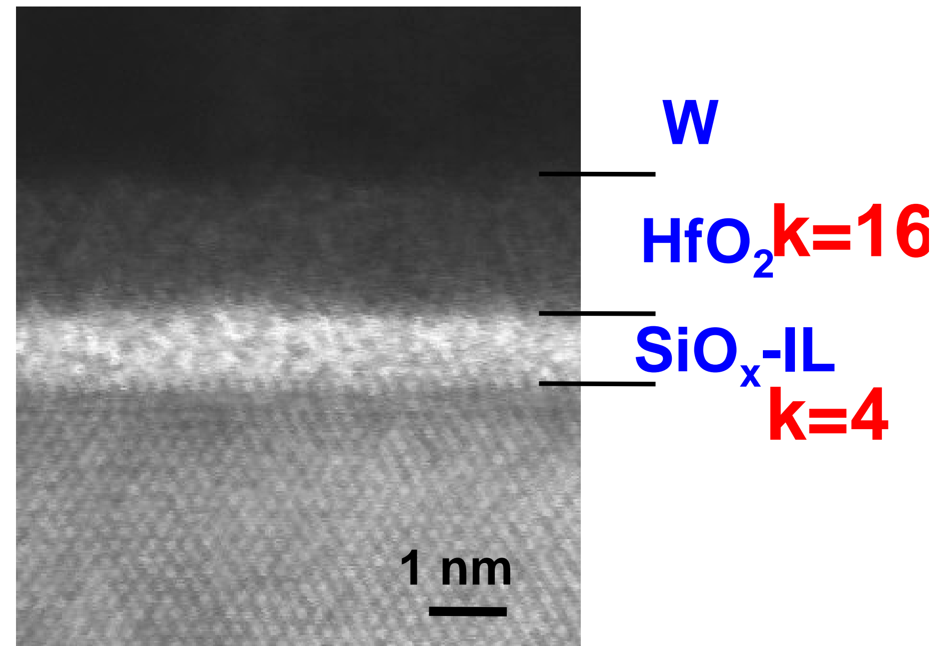


SiO_2 interfacial layer inserted or re-grown for
- recovery of degraded mobility
- interface state, reliability (TDDB, BTI), etc.

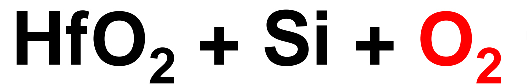
- **SiO_2-IL free structure (direct contact of high-k/Si) is required for EOT=0.5nm**
- **EOT scaling is expected down to 0.5 nm in ITRS**

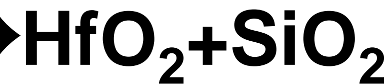
SiO_x-IL growth at HfO_2/Si Interface





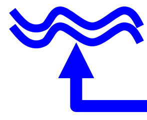
Phase separator





$$HfO_2 + Si + O_2 \rightarrow HfO_2 + Si + 2O^* \rightarrow HfO_2 + SiO_2$$

H. Shimizu, JJAP, 44, pp. 6131



Oxygen supplied from W gate electrode

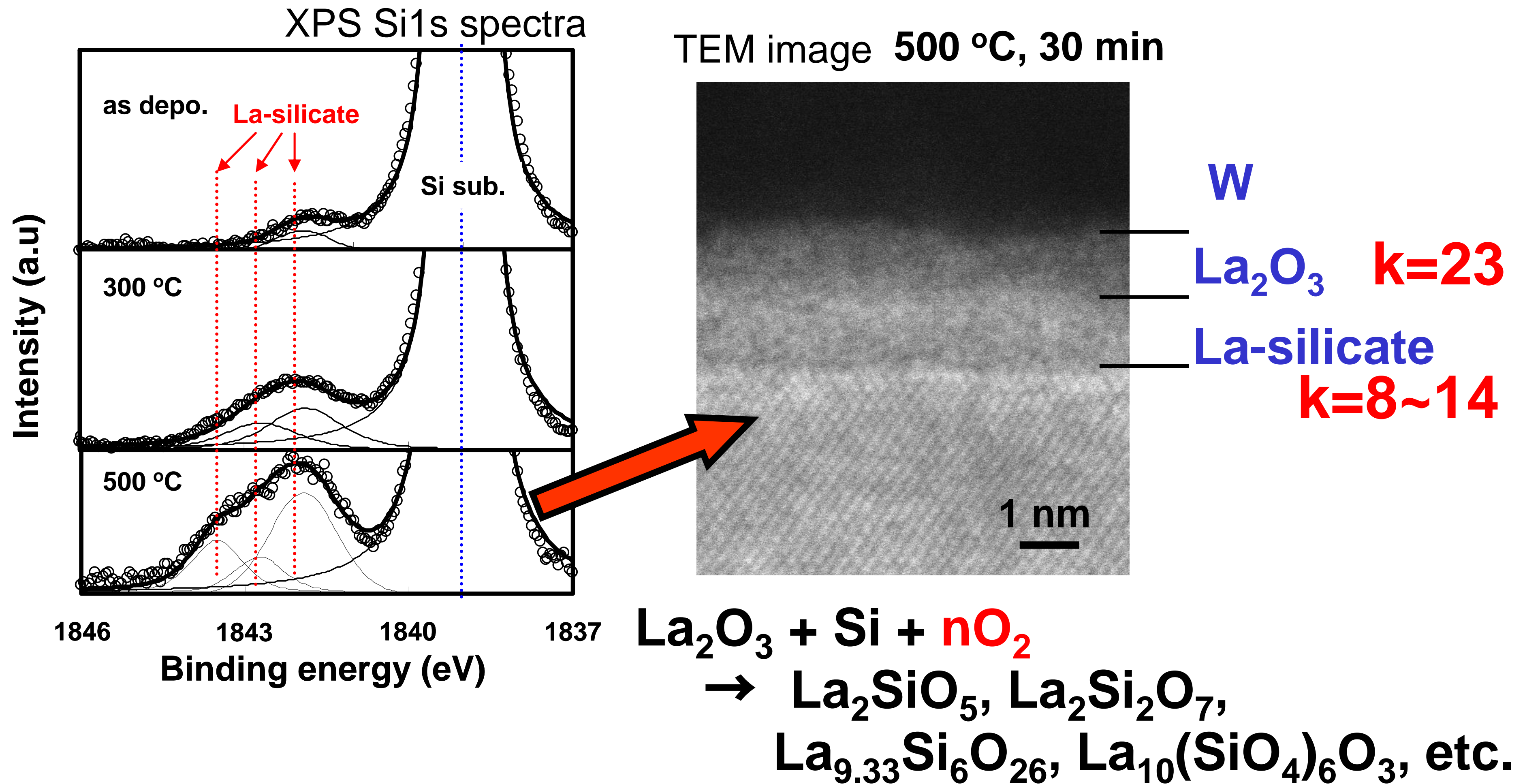
D.J.Lichtenwalner, Tans. ECS 11, 319

SiO_x-IL is formed after annealing

Oxygen control is required for optimizing the reaction

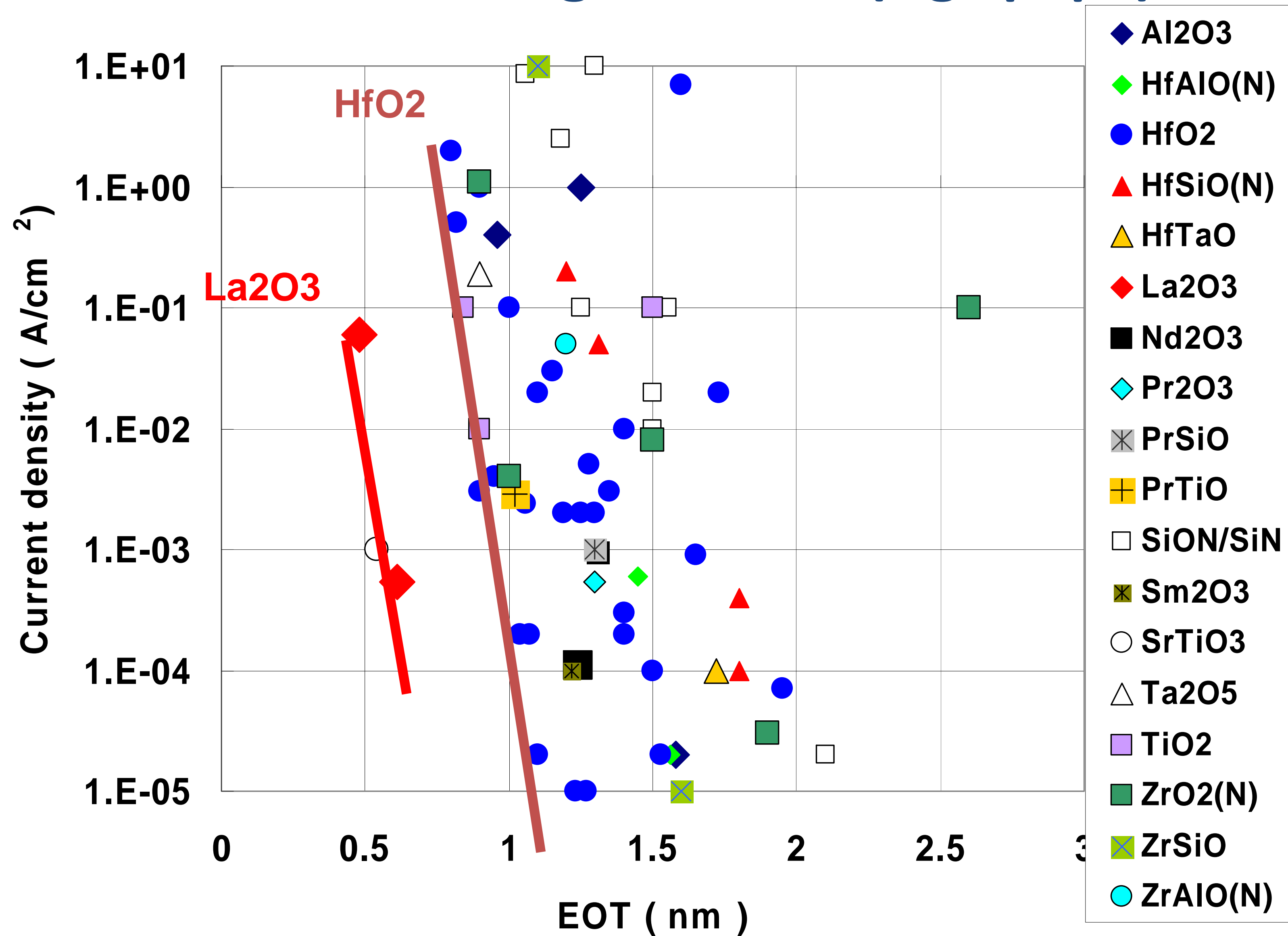
La-Silicate Reaction at La_2O_3/Si

Direct contact high-k/Si is possible

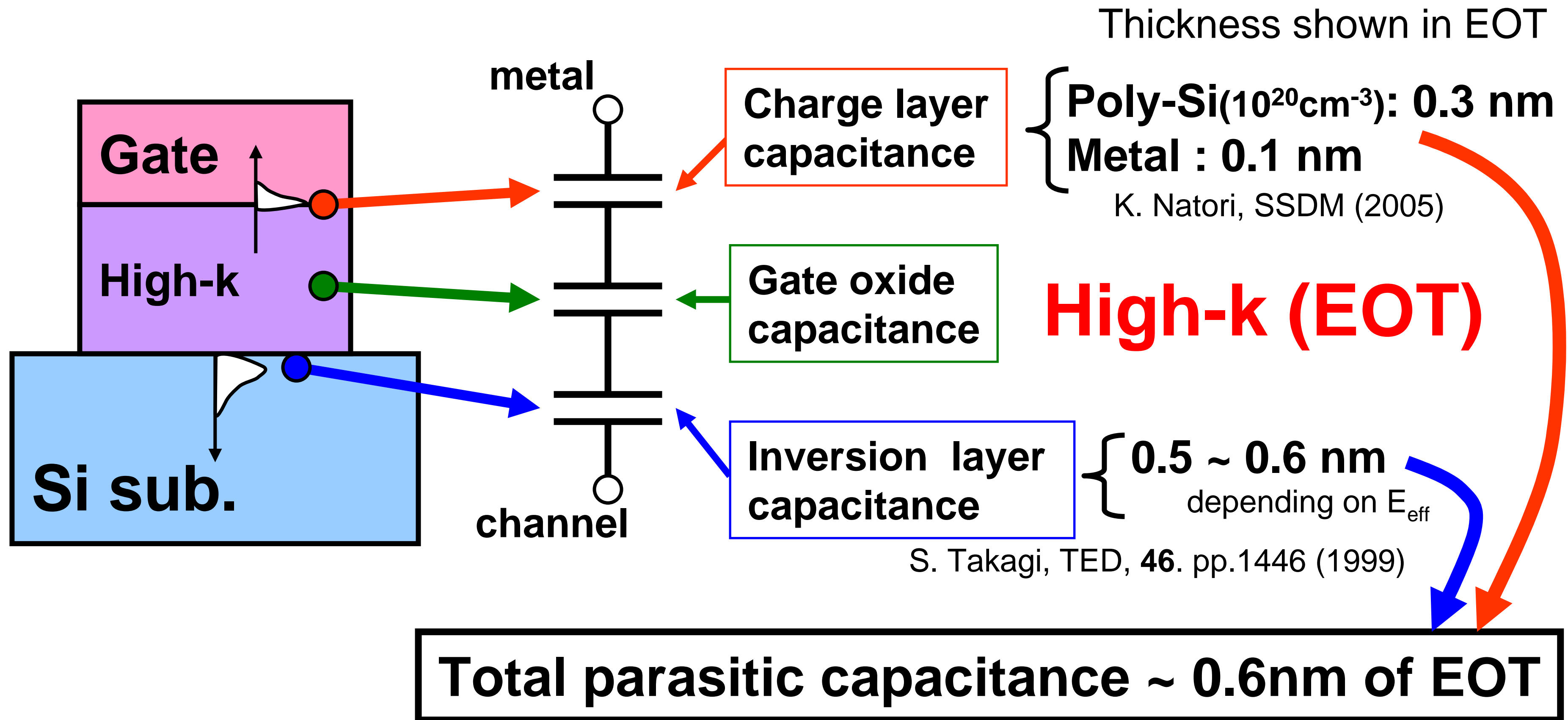


La_2O_3 can achieve direct contact of high-k/Si

Gate Leakage vs EOT, (Vg=|1|V)



Quantum Effect in Gate Stack

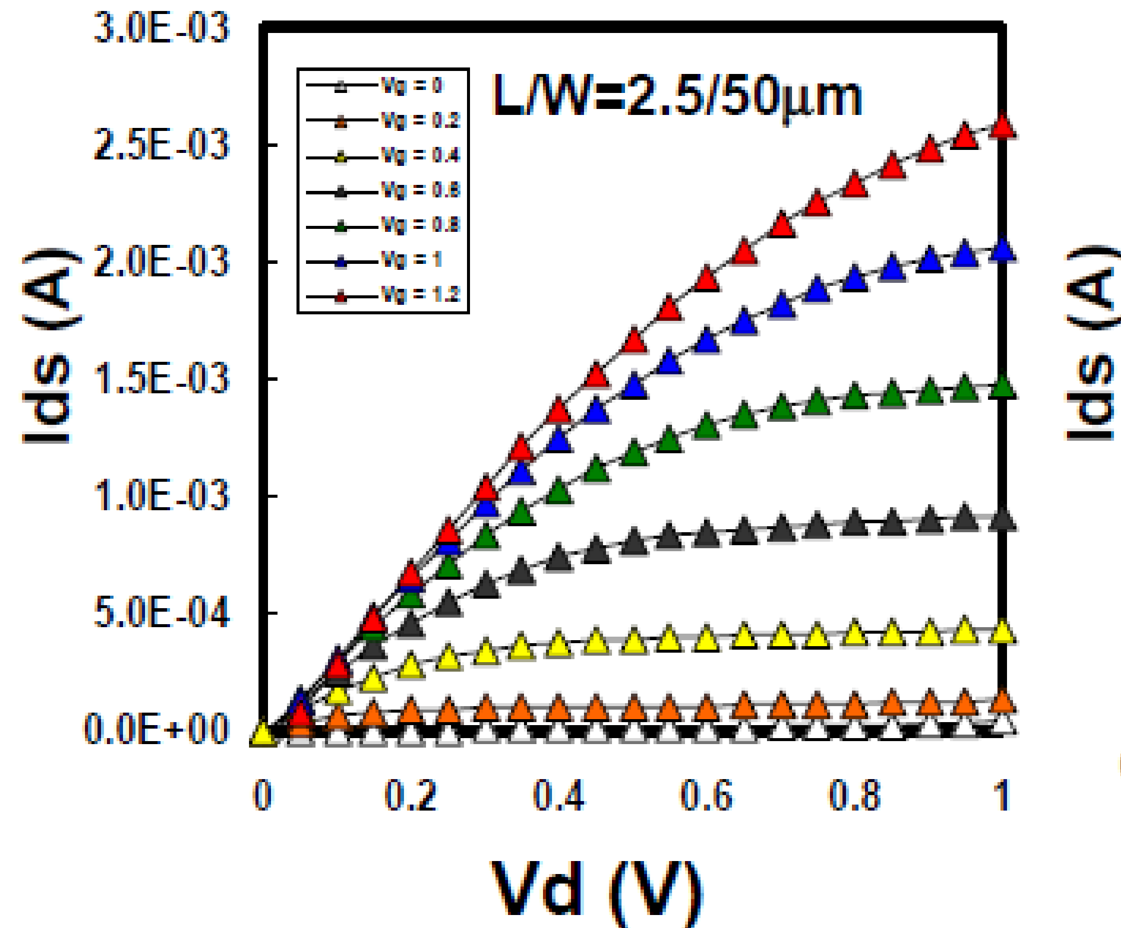


- A question if the performance improvement can be obtained with EOT<0.5nm
- Is EOT<0.5nm achievable?

EOT = 0.48 nm

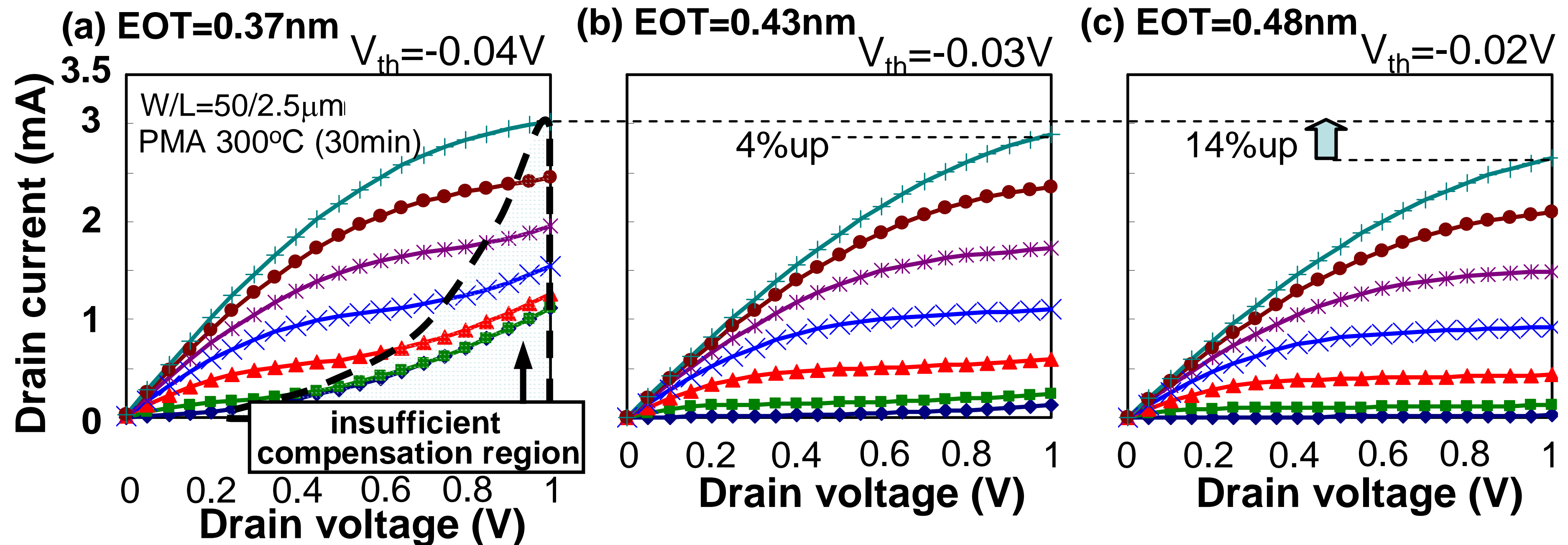
Our results

Transistor with La_2O_3 gate insulator

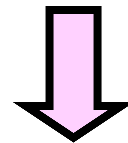


Electrical Characterization of thin La_2O_3 MOSFET EOT<0.5nm

EOT<0.5nm with Gain in Drive Current



14% of I_d increase is observed even at saturation region

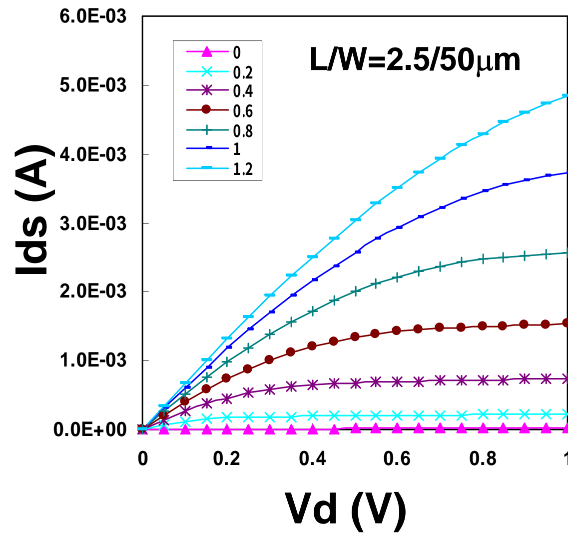


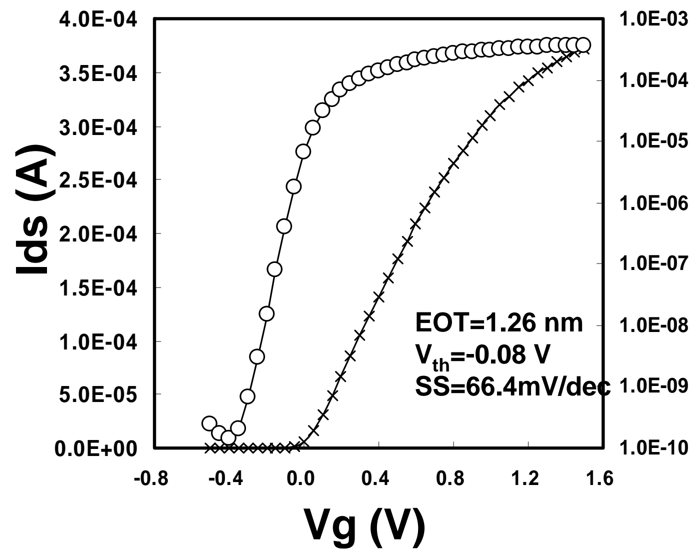
EOT below 0.4nm is still useful for scaling

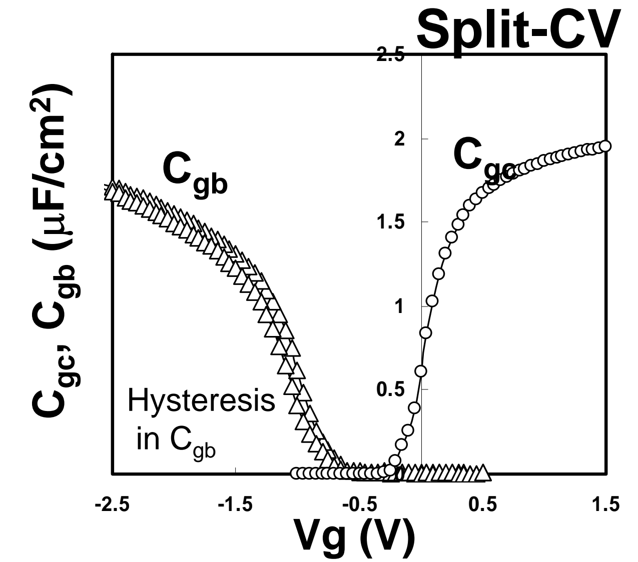
Mobility concerns

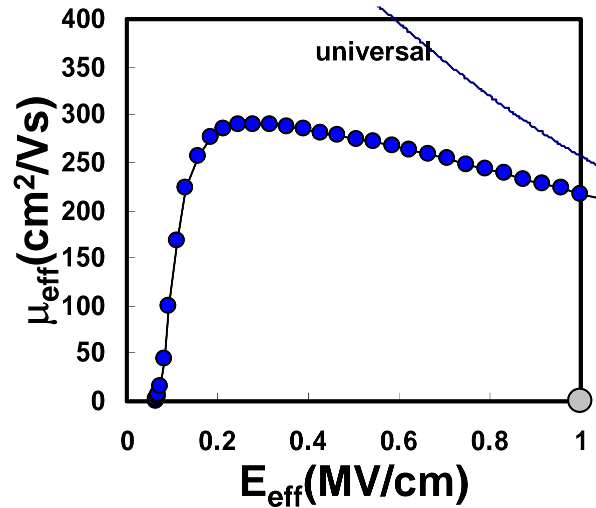
Electrical characteristics of W/La_2O_3 nFET annealed at 500 °C

W/La_2O_3/nFET, 500°C anneal





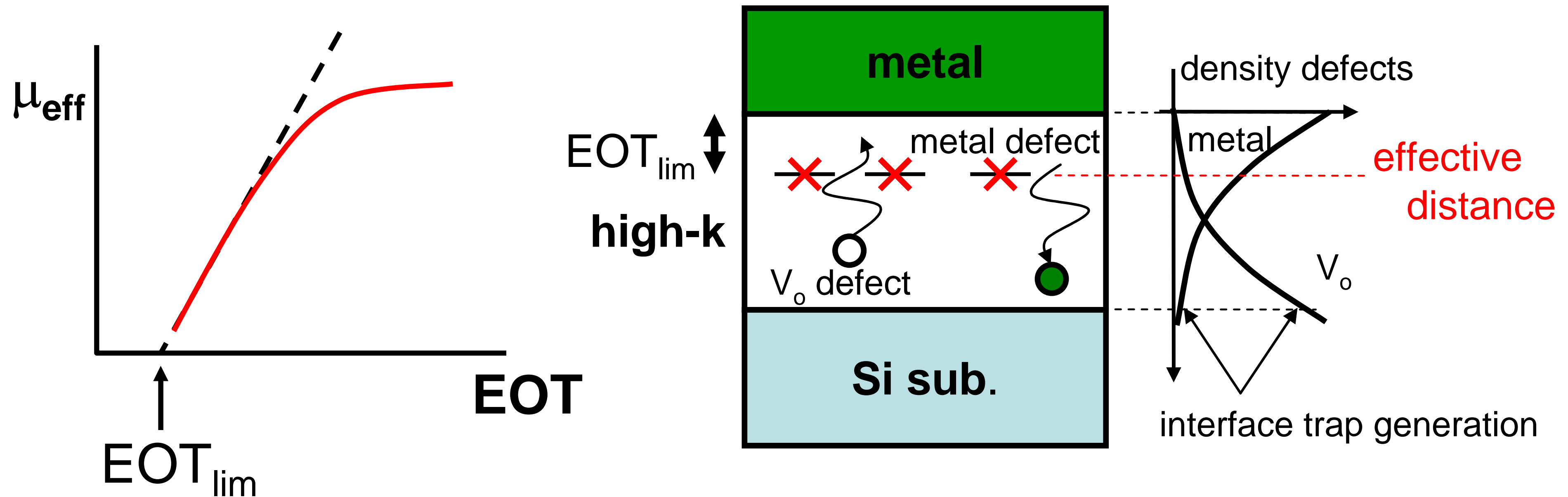




Improvement in electrical characteristics
SS=66mV/dec, μ_{eff}=300cm^2/Vs

EOT grows from 0.5 to 1.3nm

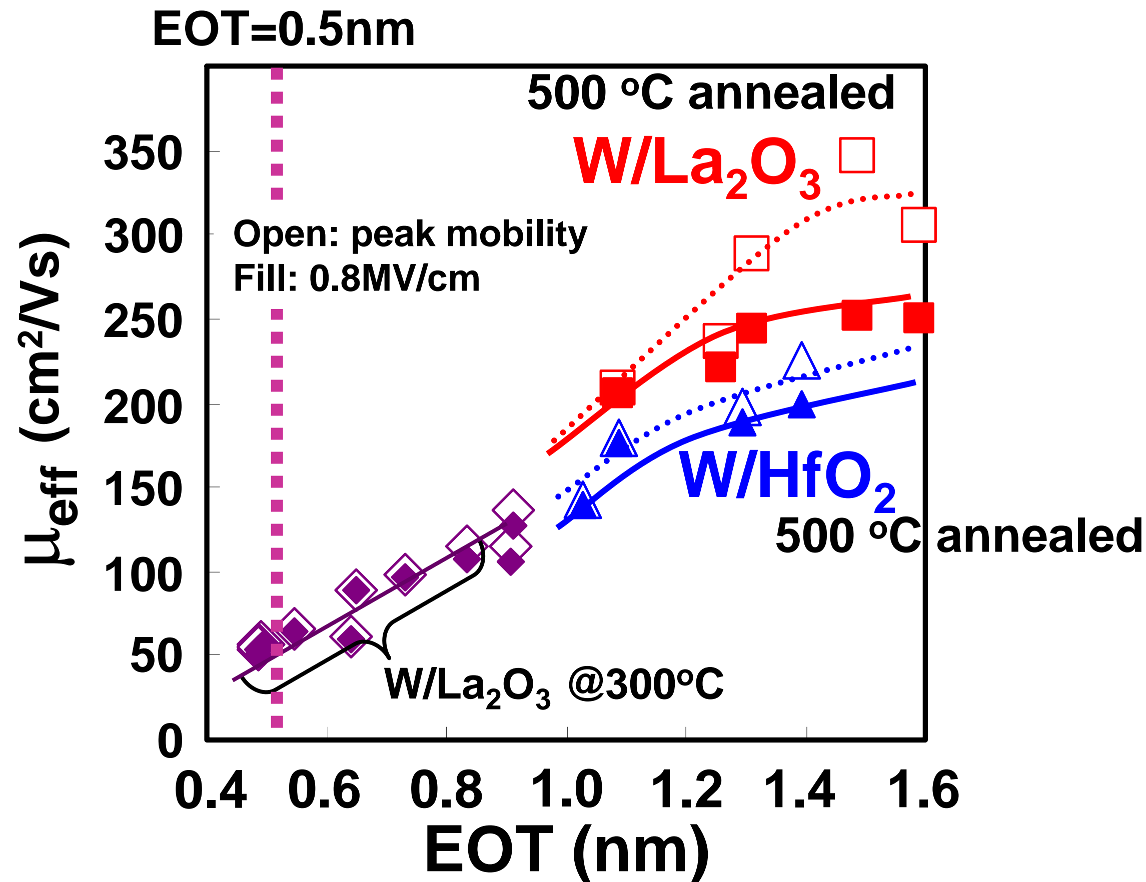
Schematic illustration of μ_{eff} reduction at small EOT



Spatial distribution of metal gate induced defects approaches to high-k/Si interface with small EOT

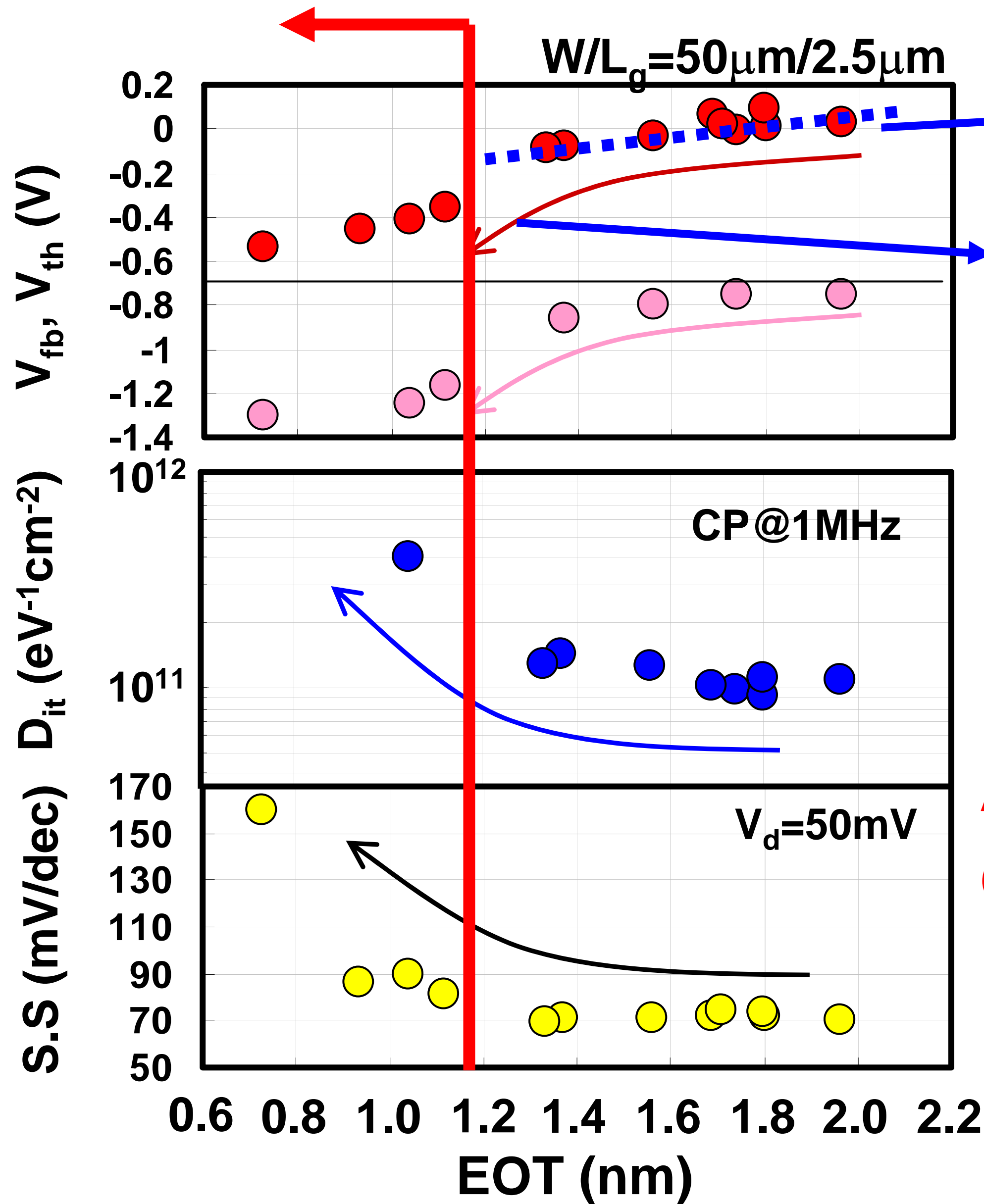
Some of the defects generates interfacial states

μ_{eff} of W/La_2O_3 and W/HfO_2 nFET on EOT



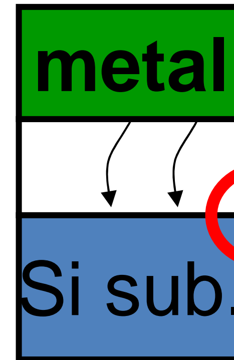
- W/La_2O_3 exhibits higher μ_{eff} than W/HfO_2
- μ_{eff} start degrades below EOT=1.4nm

FET characteristics of W/La_2O_3 on EOT



N_{fix}=7x10^{12} cm^{-2}

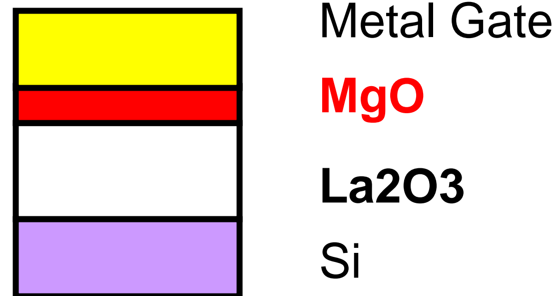
Aggressive N_{fix} generation at EOT<1.2nm

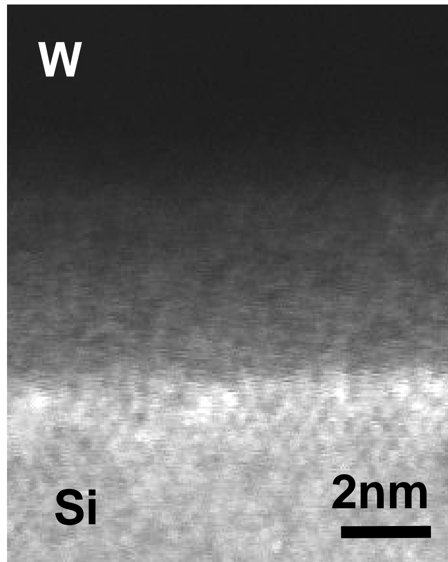


N_{fix} and D_{it}

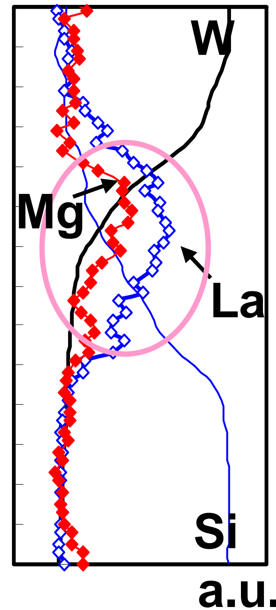
All characteristics start to degrade or shift below EOT=1.4nm

Gate Metal Induced Defects Compensation

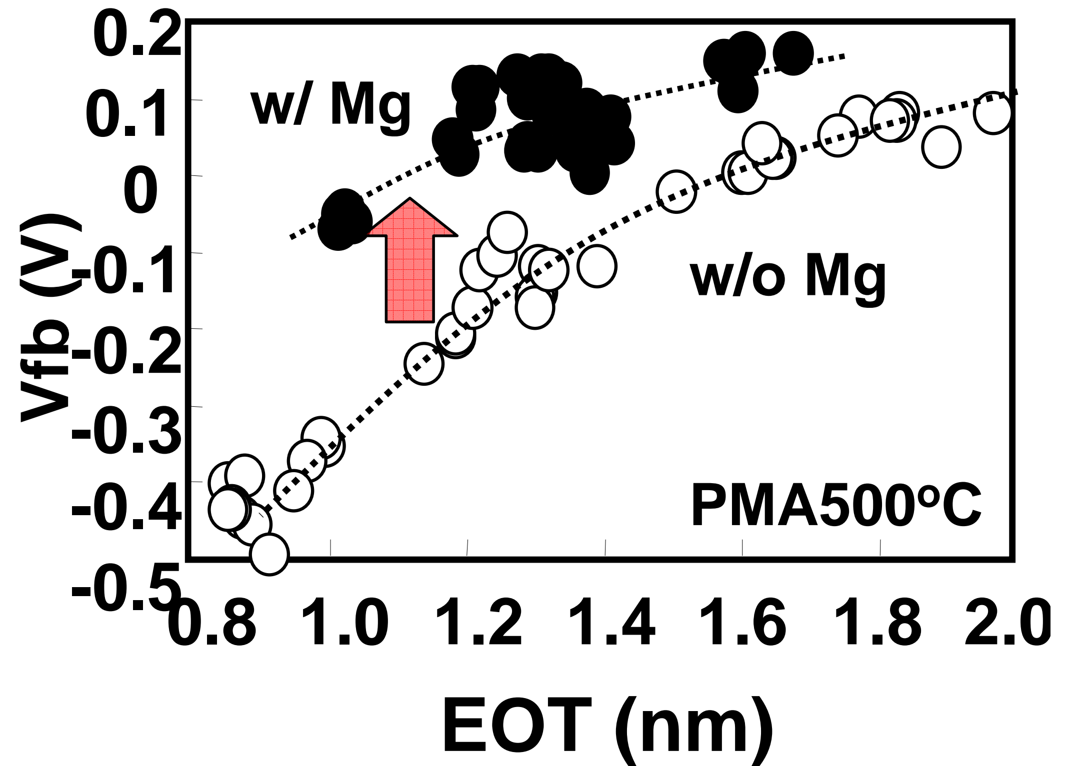




TEM

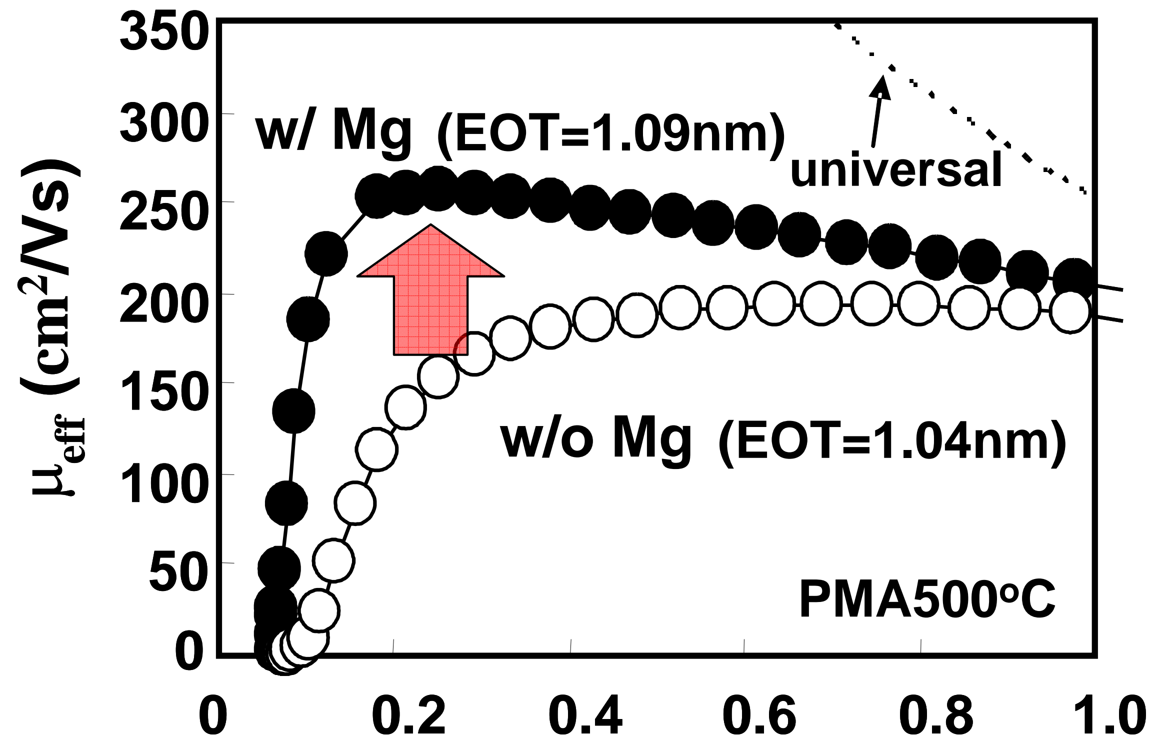


EDX



Suppression of aggressive shift in V_{fb}

Mobility Improvement with Mg Incorporation



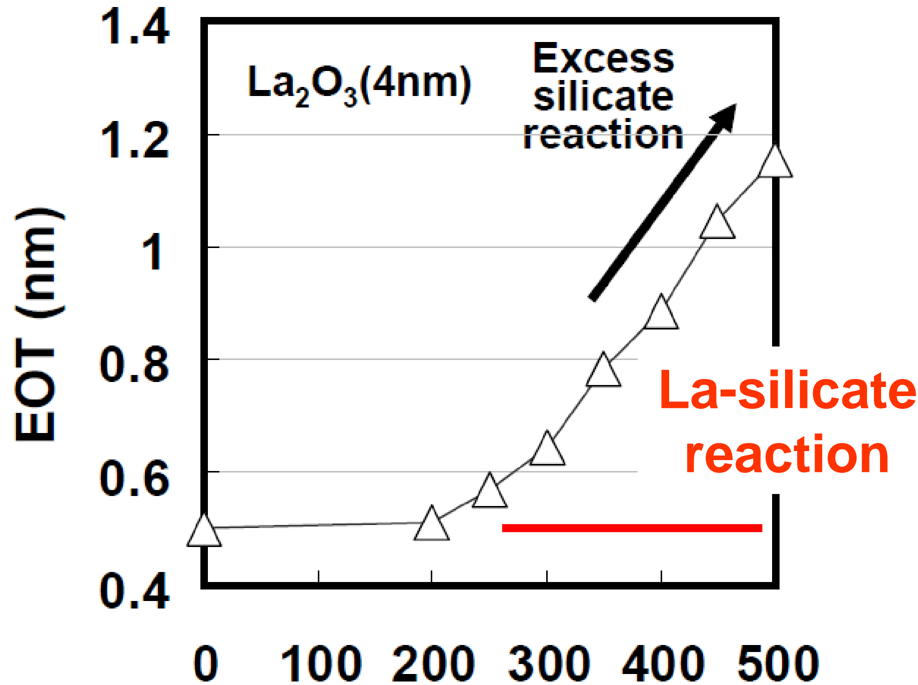
Recovery of μ_{eff} mainly at low E_{eff}

Material selection against EOT growth

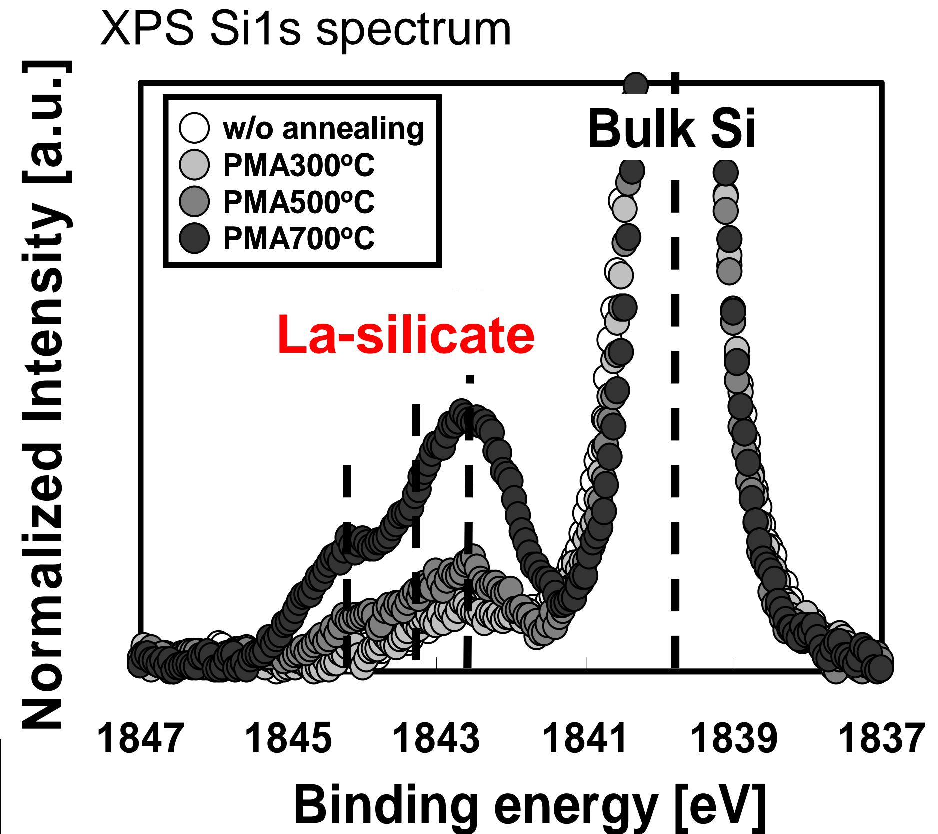
1. metal selection
2. high-k selection

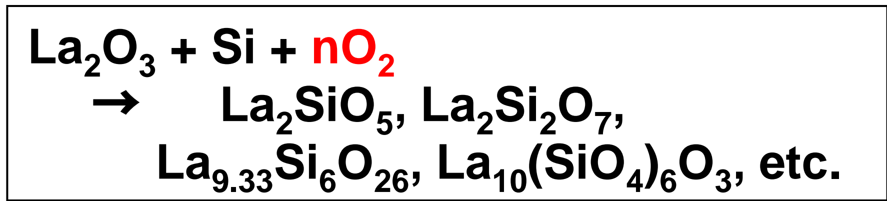
EOT growth of W/La_2O_3 on annealing temperature

30min in F.G.



XPS Si1s spectrum

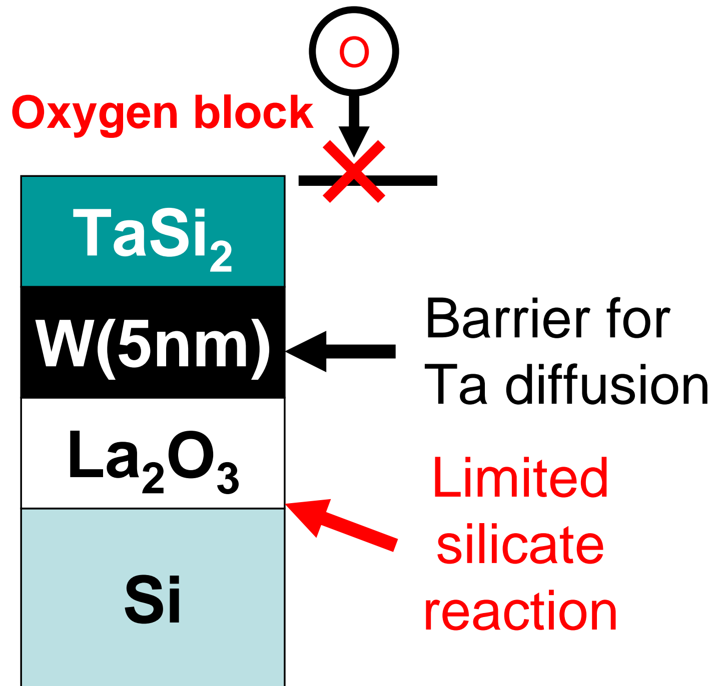


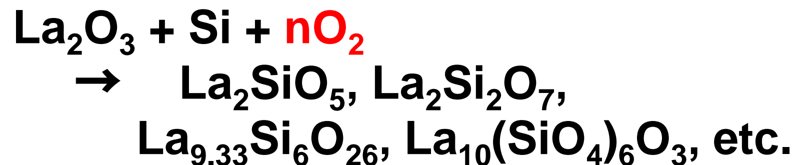


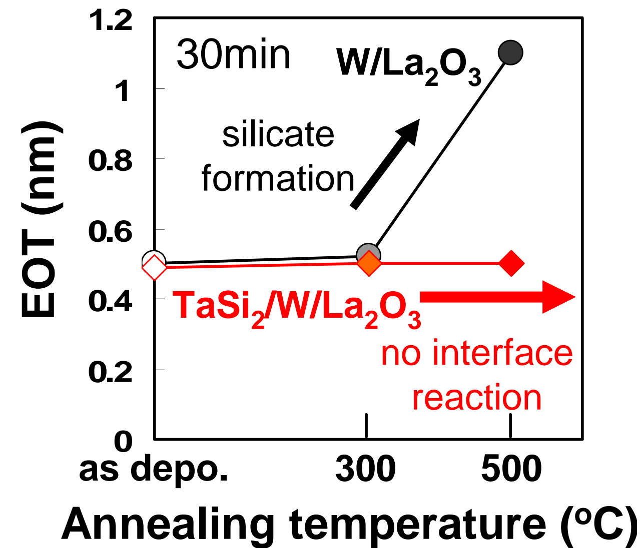
La_2O_3 + Si + nO_2
→ La_2SiO_5, $La_2Si_2O_7$, $La_{9.33}Si_6O_{26}$, $La_{10}(SiO_4)_6O_3$, etc.

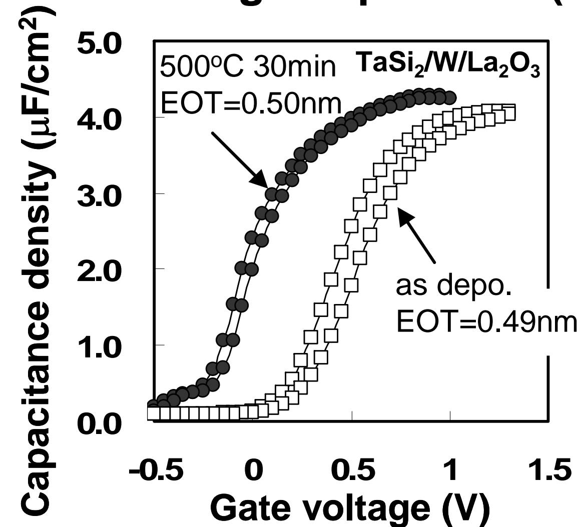
Silicate reaction further proceeds with the annealing temperature

Suppression of Silicate Reaction



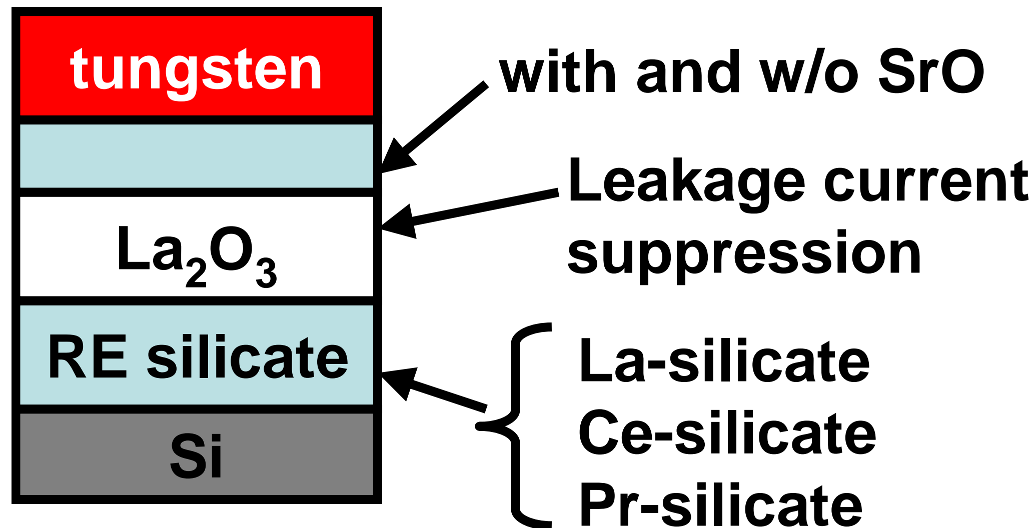






Oxygen control is the key technology in achieving small EOT with high temperature annealing

Cap effect of SrO

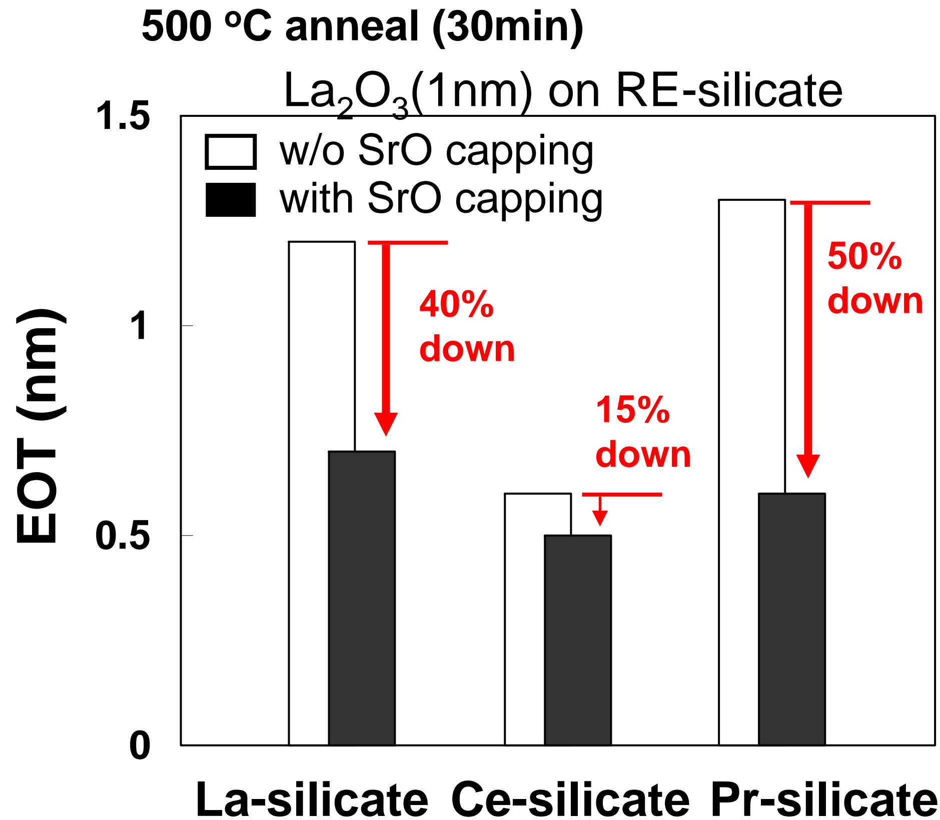


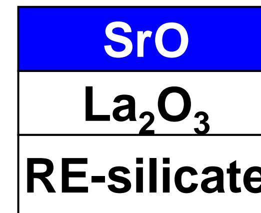
high-k	k-value	E_g (eV)
La_2O_3	24	5.5
CeO_2	32	3.2
Pr_6O_{11}	32	5.5
La-silicate	~ 9	6.4
Ce-silicate	~ 21	6.1
Pr-silicate	~ 10	6.5

Selection of rare earth silicate for interface layer

Find out the effect of SrO capping

SrO capping for achieving small EOT

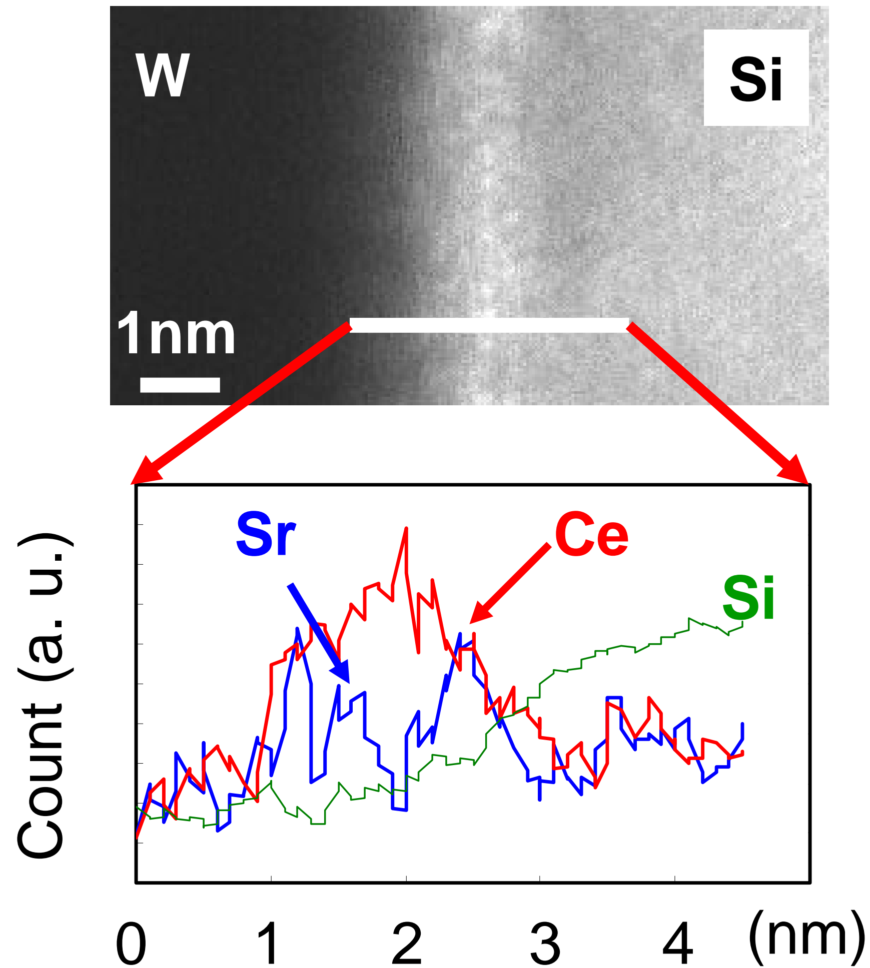




Diffusion of Sr to enhance the dielectric constant of RE-silicate

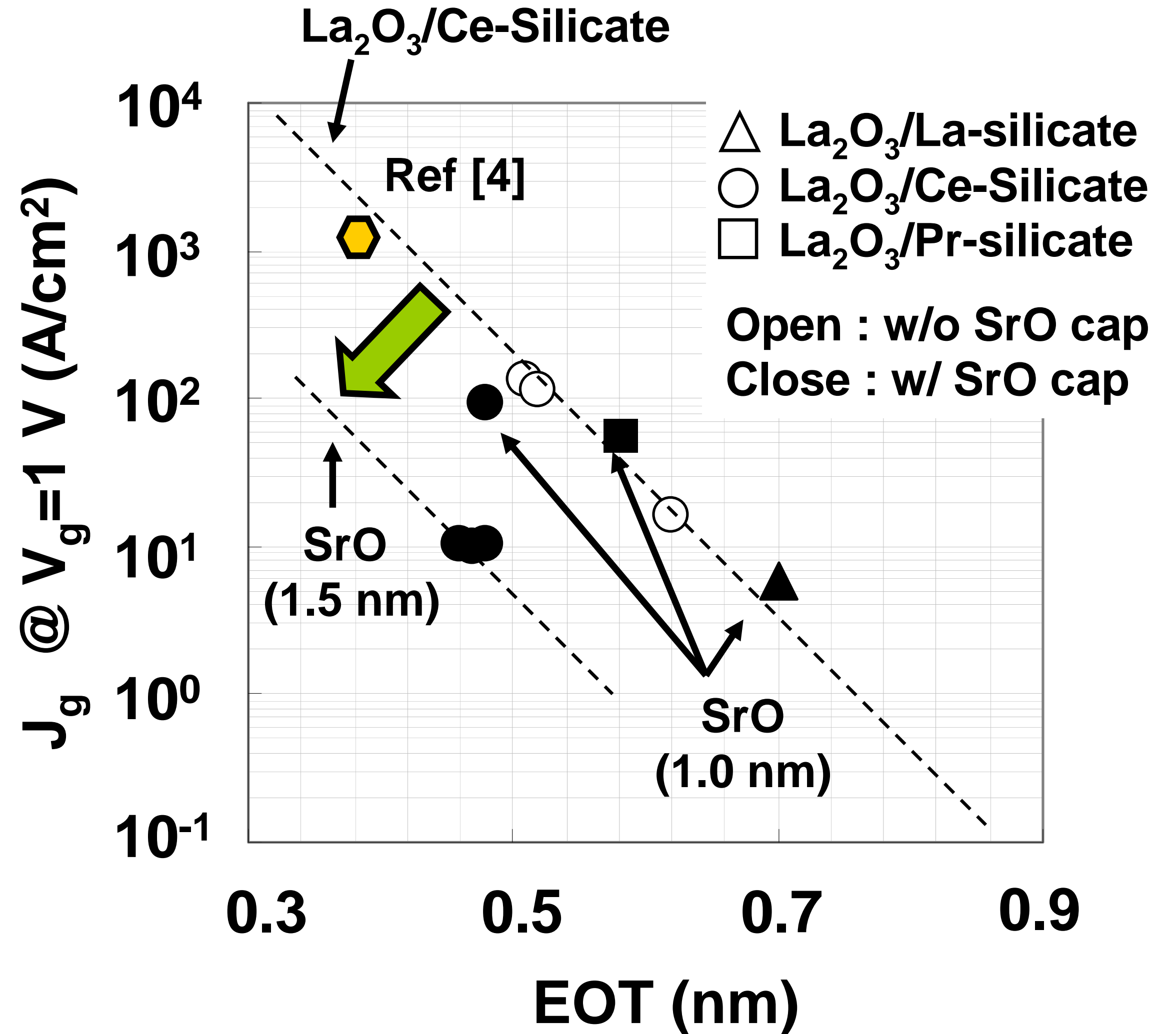
0.5nm EOT can be achieved with Ce-silicate capped with SrO which enhances the k-value

EDX Analysis of the Distribution of Sr



Sr is diffused into Ce-silicate and possibly down to Si interface

SrO effect on Current Density



Further EOT scaling is possible

A guideline for material selection: direct contact of high-k with Si structure