Future nanoelectronic device technologies - high-k, nanowire and alternative channel

@Xian Jiaotong University
December 24, 2009

東京工業大学
Tokyo Institute of Technology

先端研究中心
Frontier Research Center

岩井 洋 Hiroshi Iwai,
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
Institute Overview

Established in 1881 → 130th anniversary in 2011
3 undergraduate schools
   School of Science, School of Engineering, School of Bioscience and Biotechnology
7 graduate schools
   Science and Engineering Science, Science and Engineering Technology,
   Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
   Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

<table>
<thead>
<tr>
<th></th>
<th>Undergraduate</th>
<th>Graduate</th>
<th>Master's</th>
<th>Doctoral</th>
<th>Teaching Staff</th>
<th>Student/Instructor</th>
<th>Staff</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tokyo Inst.</td>
<td>5,000</td>
<td>5,000</td>
<td>3,500</td>
<td>1,500</td>
<td>1,200</td>
<td>8.3</td>
<td>550</td>
</tr>
<tr>
<td>Per Year</td>
<td>1,200</td>
<td></td>
<td>1,800</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Japan has successfully expanded its overseas operations across various regions. The distribution of overseas branches is as follows:

- **Asia**: 847 branches
- **Europe**: 78 branches
- **North America**: 12 branches
- **Africa**: 16 branches
- **South America**: 24 branches
- **Oceania**: 5 branches

**Total**: 982 branches

(As of May 1, 2005)
Tokyo Institute of Technology
東京工業大学

Interdisciplinary Graduate School of Science and Engineering

Dept. of Electronics and Physics
物理電子System創造専攻

Frontier Research Center 先端研究中心

G CEO (Global Center of Excellence) for Photonics Nanodevice Integration Engineering

Innovation Research Initiatives (革新的研究集団）

Consists of about 10 professor who have big projects

Consists of 5 EE Related departments

2 major campuses
Ookayama, Tokyo
Suzukakedai, Yokohama

5000 Under graduate students
5000 Graduate Students
Interdisciplinary Graduate School of Science and Engineering
大学院総合理工学研究科

J2 Building:
Frontier Collaborative Research Center (FCRC)
先端創造共同研究中心
MBE and Sputter Chamber

Sputter Chamber

MBE Chamber

1/f noise measurement system; 6 inch wafer

RTA Furnace No.1

RTA Furnace No.2

RF measurement system; 8 inch wafer, 40 GHz

Back Pressure: 10^-8 Pa
During Deposition: 10^-7 Pa
Deposition rate: 0.1 to 1 monolayer/minute

Iwai Lab. Equipment

MBE and Sputter Chamber

Sputter Chamber

MBE Chamber

1/f noise measurement system; 6 inch wafer

RTA Furnace No.1

RTA Furnace No.2

RF measurement system; 8 inch wafer, 40 GHz
岩井研究室 ~Iwai Lab.~

ご挨拶
Welcome to Iwai Lab.

次世代高性能半導体デバイスに向けた研究テーマ

Siデバイスの重要性

现代社会: 生産、金融、通信、交通等の社会機能
インターネット、WiMax, Bluetooth, 携帯電話, ナビゲーション, デジタルテレビ, CD, DVDなどの技術

Siモールドおよびアルミナ製のSiデバイスの製造

硅素化の重要性

分子の微細化 (100倍まで100倍の縮小に) 1000年

High-k/Metalゲートスタック

次世代ゲート絶縁膜材料として La2O3が注目

XPS measurement by Prof. T. Hattori, NITE 2003

高機能・低消費電力化には EOT=0.5nmが必要

La2O3は特性が良い直接結合が可能

High-kとSiの直接結合が必要

C_Dir = \frac{\varepsilon_{SiO2}}{t_{SiO2}} \Rightarrow t_{SiO2} = \frac{\varepsilon_{SiO2}}{EOT} EOT = SiO2等価換算厚

外部機関との連携研究

東京工業大学 ブロック研究センター 東京工業大学

ULVAC ULVAC PHI 水素化研究所

IR HOME (シーガル) Nanyang大学 (シーガル) LET(フランス)

産業大学 北九州工業大学 名古屋大学 産業技術大学
Three IEEE Fellows Win 2009 Nobel Prize in Physics

“. . .for breakthroughs involving the transmission of light in fiber optics and inventing an imaging semiconductor circuit, the three scientists created the technology behind digital photography and helped link the world through fiber optic networks.”

(l-r) Dr. Charles K. Kao
Dr. Willard S. Boyle
Dr. George E. Smith
Nobel Prizes in Electron Devices

- **1956** – The Transistor
  William Shockley, John Bardeen, and Walter Brattain

- **1973** – Tunneling Diode
  Leo Esaki, Ivar Giaever
  – Josephson Junction
  Brian David Josephson

- **2000** – Integrated Circuit
  Jack Kilby
  – Semiconductor Heterojunction Devices
  Zohres Alferov and Herbert Kroemer

- **2007** – Giant Magneto resistive Effect (GMR)
  Albert Fert and Peter Grunberg

- **2009** – Charge Coupled Devices
  George Smith and Willard Boyle
  – Fiber Optic Technology
  Charles Kao

By Dr. Lu Terman, at IEDM 2009
Sir Isaac Newton

“If I can see so far, it is because I stand on the shoulders of giants”

By Dr. Lu Terman, at IEDM 2009
1. Scaling
J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator.

Drain Current was several orders of magnitude smaller than expected

Even Shockley!
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

Al Gate

Si

Drain

Si/SiO₂ Interface is extraordinarily good

Al

SiO₂

Si
Downsizing of the components has been the driving force for circuit evolution.

<table>
<thead>
<tr>
<th>Year</th>
<th>Vacuum Tube</th>
<th>Transistor</th>
<th>IC</th>
<th>LSI</th>
<th>ULSI</th>
</tr>
</thead>
<tbody>
<tr>
<td>1900</td>
<td>10 cm</td>
<td>cm</td>
<td>mm</td>
<td>10 μm</td>
<td>100 nm</td>
</tr>
<tr>
<td>1950</td>
<td>10^{-1}m</td>
<td>10^{-2}m</td>
<td>10^{-3}m</td>
<td>10^{-5}m</td>
<td>10^{-7}m</td>
</tr>
<tr>
<td>1960</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1970</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. **We have never experienced such a tremendous reduction of devices in human history.**
Downsizing

1. **Reduce Capacitance**
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. **Increase number of Transistors**
   - Parallel processing
     - Increase circuit operation speed

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.
Scaling Method: by R. Dennard in 1974

W_{dep}: Space Charge Region (or Depletion Region) Width

W_{dep} has to be suppressed. Otherwise, large leakage between S and D.

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

By the scaling, W_{dep} is suppressed in proportion, and thus, leakage can be suppressed.

K = 0.7 for example

Good scaled I-V characteristics
## Downscaling merit: Beautiful!

<table>
<thead>
<tr>
<th>Geometry &amp; Supply voltage</th>
<th>$L_g$, $W_g$</th>
<th>$T_{ox}$, $V_{dd}$</th>
<th>K</th>
<th>Scaling $K : K=0.7$ for example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive current in saturation</td>
<td>$I_d$</td>
<td>K</td>
<td>(I_d = v_{sat}W_gC_o(V_g-V_{th}))</td>
<td>(C_o: ) gate C per unit area</td>
</tr>
<tr>
<td>(I_d) per unit $W_g$</td>
<td>$I_d/\mu m$</td>
<td>1</td>
<td>$I_d$ per unit $W_g = I_d/ W_g = 1$</td>
<td></td>
</tr>
<tr>
<td>Gate capacitance</td>
<td>$C_g$</td>
<td>K</td>
<td>(C_g = \varepsilon_o\varepsilon_{ox}L_g W_g/t_{ox})</td>
<td>(KK/K = K)</td>
</tr>
<tr>
<td>Switching speed</td>
<td>$\tau$</td>
<td>K</td>
<td>$\tau = C_gV_{dd}/I_d$</td>
<td>(KK/K = K)</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>$f$</td>
<td>$1/K$</td>
<td>$f = 1/\tau = 1/K$</td>
<td></td>
</tr>
<tr>
<td>Chip area</td>
<td>$A_{chip}$</td>
<td>$\alpha$</td>
<td>$\alpha$: Scaling factor</td>
<td>In the past, $\alpha&gt;1$ for most cases</td>
</tr>
<tr>
<td>Integration (# of Tr)</td>
<td>$N$</td>
<td>$\alpha/K^2$</td>
<td>$N \rightarrow \alpha/K^2 = 1/K^2$, when $\alpha=1$</td>
<td></td>
</tr>
<tr>
<td>Power per chip</td>
<td>$P$</td>
<td>$\alpha$</td>
<td>$fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha = 1$, when $\alpha=1$</td>
<td></td>
</tr>
</tbody>
</table>
Scaling down approach is very beautiful and important.

| 2 Generations scaling | k = 0.7^2 = 0.5  
|                       | if we keep the chip area the same for scaling |

**Single MOFET**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td>0.5</td>
</tr>
<tr>
<td>Lg</td>
<td>0.5</td>
</tr>
<tr>
<td>Id</td>
<td>0.5</td>
</tr>
<tr>
<td>Cg</td>
<td>0.5</td>
</tr>
</tbody>
</table>

**P (Power)/Clock**

\[ P \rightarrow 0.5^3 = 0.125 \]

\[ \tau (Switching\ time) \rightarrow 0.5 \]

**Chip**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>N (# of Tr)</td>
<td>(1/0.5^2 = 4)</td>
</tr>
<tr>
<td>f (Clock)</td>
<td>(1/0.5 = 2)</td>
</tr>
<tr>
<td>P (Power)</td>
<td>1</td>
</tr>
</tbody>
</table>
Actual past downscaling trend until year 2000

Change in 30 years

<table>
<thead>
<tr>
<th>Ideal scaling</th>
<th>Real Change</th>
<th>Ideal scaling</th>
<th>Real Change</th>
<th>Ideal scaling</th>
<th>Real Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$</td>
<td>$K$</td>
<td>$10^{-2}$</td>
<td>$10^{-2}$</td>
<td>$I_d$</td>
<td>$K(10^{-2})$</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-1}$</td>
<td>$I_d/\mu m$</td>
<td>$1$</td>
<td>$10^1$</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-1}$</td>
<td>$N$</td>
<td>$\alpha/K^2(10^5)$</td>
<td>$10^4$</td>
</tr>
<tr>
<td>$A_{chip}$</td>
<td>$\alpha$</td>
<td>$10^1$</td>
<td>$P$</td>
<td>$\alpha(10^1)$</td>
<td>$10^5$</td>
</tr>
</tbody>
</table>

Vd scaling insufficient, $\alpha$ increased \[ \rightarrow \] N, Id, f, P increased significantly

Past 30 years scaling
Merit: N, f increase
Demerit: P increase

$V_{dd}$ scaling insufficient

Additional significant increase in $I_d$, f, P

## Microprocessors Trend??

<table>
<thead>
<tr>
<th>Year</th>
<th>Lg</th>
<th>Tox</th>
<th>f</th>
<th>P</th>
<th>N</th>
</tr>
</thead>
<tbody>
<tr>
<td>Past: 1972 (Intel)</td>
<td>10,000 nm</td>
<td>1200 nm</td>
<td>0.00075 GHz</td>
<td>a few 100 mW</td>
<td>2.25k</td>
</tr>
<tr>
<td>Today: 2002 (Intel)</td>
<td>sub-70 nm</td>
<td>1.4 nm</td>
<td>2.53 GHz</td>
<td>several 10 W</td>
<td>50 M</td>
</tr>
<tr>
<td>2008 (Intel)</td>
<td>sub-25 nm</td>
<td>0.7 nm</td>
<td>30 GHz</td>
<td>10 kW</td>
<td>1.8B</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MIPS 1M MIPS (TIPS)</td>
</tr>
</tbody>
</table>

### Heat generation

- **2002**: 10W/cm² Hot plate
- **2006**: 100W/cm² Surface of nuclear reactor
- **2010**: 1000W/cm² rocket nozzle
- **2016**: 10000W/cm² Sun surface

Heat Sink Technology

- Fan-sinks
- Extrusion Heatsinks
- Skive
- Crimped Fin
- Spiral Fan-sink

Heat Sink Thermal Performance vs. Time
Tera-scale Research Prototype
Connecting 80 simple cores on a single test chip

Intel processors with two cores are here now and quad-core processors are right around the corner. In the coming years, the number of cores on a chip will continue to grow, launching an era of vastly more powerful computers. These are the machines that will deliver efficient teraflop performance with the capabilities needed to handle tomorrow’s emerging applications. They must also scale to an increasing number of cores – perhaps 10s or even 100s of them.

This test chip represents Intel’s first tera-scale research prototype silicon. The purpose of the prototype is to develop a design methodology appropriate for tera-scale computing by using a tiled approach. Each tile includes a small core, or compute element, with a few simple instructions that can generate data, and a router that connects each tile to adjacent tiles and to 3D stacked memory that will be added in the future. The prototype consists of 80 tiles in an 8x10 array with an on-chip interconnect fabric.

The key technologies of this first Tera-scale Research Prototype are a mesh interconnect (left) and support for 3D stacked memory (above).
- The concerns for limits of down-scaling have been announced for every generation.

- However, down-scaling of CMOS is still the ‘royal road’* for high performance and low power.

- Effort for the down-scaling has to be continued by all means.

* Euclid of Alexandria (325BC?-265BC?)
  ‘There is no royal road to Geometry’
Mencius (Meng-zi), China (372BC?-289BC?)
  孟子: 王道, 霸道 (Rule of right vs. Rule of military)
- There will be still 4~6 generations left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IJWJT2008).

- Even after reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

- Two candidates have emerged for R & D
  1. Nanowire/tube MOSFETs
  2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.
Before reaching the scaling limit, we need to pursue the down scaling limit, introducing new materials such as (1) high-k.

Then, (2) Si-nanowire and (3) Alternative channel (III-V and Ge).

That is why I am concentrating the research of the above 3 – (1), (2), (3).
Scaling Limit in MOSFET

SiO2 Scaling

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
High-k Thin Film for Gate Insulator

**MOSFET**

<table>
<thead>
<tr>
<th>Physical Gate Length (nm)</th>
<th>2005</th>
<th>2008</th>
<th>2010</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equivalent Oxide Thickness (nm)</td>
<td>1.1</td>
<td>0.8</td>
<td>0.7</td>
<td>0.6</td>
</tr>
</tbody>
</table>
Gate oxide scaling is very important also for suppressing the variation.

Random Variability Reduction Scenario
in ITRS 2007

Planar Bulk & Poly-Si/SiON
\( T_{\text{inv}}=2.5\text{nm} \)
\( N_A=3\times10^{18} \)

Planar Bulk & Metal/High-k
\( T_{\text{inv}}=1.8\text{nm} \)
\( N_A=1.5\times10^{18} \)

Assumption: Random dopant fluctuation is Main source of Random Variability: Line width roughness of \( L_g \) and \( W_g \) is not considered in this
## Historical trend of high-k R&D

<table>
<thead>
<tr>
<th>Year</th>
<th>MOSFET</th>
<th>Gate Stack in production</th>
</tr>
</thead>
<tbody>
<tr>
<td>1960</td>
<td>1st FET IC LSI</td>
<td>PMOS NMOS CMOS</td>
</tr>
<tr>
<td>1970</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1980</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1990</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2005</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### MOSFET Gate Stack in production
- **Gate insulator**: \( \text{SiO}_2 \), \( \text{SiO}_x\text{N}_y \)
- **Gate electrode**: \( \text{Al} \), \( \text{N}^+\text{Poly Si} \), \( \text{Double Poly Si} \)
- **Silicide above Poly Si electrode**: \( \text{MoSi}_2 \rightarrow \text{WSi}_2 \), \( \text{TiSi}_2 \), \( \text{CoSi}_2 \), \( \text{NiSi} \)

### R&D for high-k
- **MOSFET**: \( \text{Ni}_3\text{Si}_4 \), \( \text{Al}_2\text{O}_3 \), \( \text{ZrO}_2 \)
- **DRAM Capacitor**: \( \text{NO}, \text{AO (Al}_2\text{O}_3/\text{SiO}_2) \)
- **NV Memory**: \( \text{NO, AO (Al}_2\text{O}_3/\text{SiO}_2) \)
- **Analog/RF**: \( \text{Ta}_2\text{O}_5, \text{Al}_2\text{O}_3, \text{Ta}_2\text{O}_5 \)

### Pure Si Period
- \( \text{NO, Ni}_3\text{Si}_4 \) to \( \text{Ta}_2\text{O}_5, \text{Al}_2\text{O}_3, \text{Ni}_3\text{Si}_4 \)

### Recent new high-k
- \( \text{NO, AO (Al}_2\text{O}_3/\text{SiO}_2) \) to \( \text{Ta}_2\text{O}_5, \text{Ni}_3\text{Si}_4 \)
### Choice of High-k

<table>
<thead>
<tr>
<th>Candidates</th>
<th>□</th>
<th>Gas or liquid at 1000 K</th>
<th>□</th>
<th>Radio active</th>
<th>□</th>
<th>He</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Li Be</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Na Mg</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>K Ca Sc</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sr Y Zr</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cs Ba Hf</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fr Ra</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>La Ce Pr Nd</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sm Eu Gd Tb Dy Ho Er Tm Yb Lu</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Unstable at Si interface

- Si + MO\(_x\) M + SiO\(_2\)
- Si + MO\(_x\) MSi\(_x\) + SiO\(_2\)
- Si + MO\(_x\) M + MSi\(_x\)O\(_y\)

- □ HfO\(_2\) based dielectrics are selected as the first generation materials, because of their merit in
  1) band-offset, 2) dielectric constant 3) thermal stability

- □ La\(_2\)O\(_3\) based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

Choice of High-k are selected as the first generation materials, because of their merit in
1) band-offset, 2) dielectric constant 3) thermal stability
Dielectric constant:

- SiO$_2$: 4
- Si$_3$N$_4$: ~7
- Al$_2$O$_3$: ~9
- Y$_2$O$_3$: ~10
- Gd$_2$O$_3$: ~10
- HfO$_2$: ~23
- La$_2$O$_3$: ~27

HfO$_2$ was chosen for the 1st generation.
La$_2$O$_3$ is more difficult material to treat.
Dielectric constant value vs. Band offset (Measured)

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>3.9</td>
</tr>
<tr>
<td>AlₓSiᵧOz</td>
<td></td>
</tr>
<tr>
<td>(Ba,Sr)TiO₃</td>
<td>200-300</td>
</tr>
<tr>
<td>BeAl₂O₄</td>
<td>8.3-9.43</td>
</tr>
<tr>
<td>CeO₂</td>
<td>16.6-26</td>
</tr>
<tr>
<td>CeHfO₄</td>
<td>10-20</td>
</tr>
<tr>
<td>CoTiO₃/Si₃N₄</td>
<td></td>
</tr>
<tr>
<td>EuAlO₃</td>
<td>22.5</td>
</tr>
<tr>
<td>HfO₂</td>
<td>26-30</td>
</tr>
<tr>
<td>Hf silicate</td>
<td>11</td>
</tr>
<tr>
<td>La₂O₃</td>
<td>20.8</td>
</tr>
<tr>
<td>LaScO₃</td>
<td>30</td>
</tr>
<tr>
<td>La₂SiO₅</td>
<td></td>
</tr>
<tr>
<td>MgAl₂O₄</td>
<td></td>
</tr>
<tr>
<td>NdAlO₃</td>
<td>22.5</td>
</tr>
<tr>
<td>PrAlO₃</td>
<td>25</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td>7</td>
</tr>
<tr>
<td>SmAlO₃</td>
<td>19</td>
</tr>
<tr>
<td>SrTiO₃</td>
<td>150-250</td>
</tr>
<tr>
<td>Ta₂O₅</td>
<td>25-24</td>
</tr>
<tr>
<td>Ta₂O₅-TiO₂</td>
<td></td>
</tr>
<tr>
<td>TiO₂</td>
<td>86-95</td>
</tr>
<tr>
<td>TiO₂/Si₃N₄</td>
<td></td>
</tr>
<tr>
<td>Y₂O₃</td>
<td>8-11.6</td>
</tr>
<tr>
<td>YₓSiₙOₓ</td>
<td></td>
</tr>
<tr>
<td>ZrO₂</td>
<td>22.2-28</td>
</tr>
<tr>
<td>Zr-Al-O</td>
<td></td>
</tr>
<tr>
<td>Zr silicate</td>
<td></td>
</tr>
<tr>
<td>(Zr,Sn)TiO₄</td>
<td>40-60</td>
</tr>
</tbody>
</table>

\[\sqrt{\phi_B} \times k \] : Figure of Merit of High-k

C.A. Billmann et al., MRS Spring Symp., 1999
S. De Gebdt, IEDM Short Coyuse, 2004

T. Hattori, INFOS , 2003
Too large high-k cause significant short channel effect

- Too large high-k SiO₂

- Penetration of lateral field from Drain through high-k causes significant short channel effects
The oxides become hydroxide and carbonate in H₂O and CO₂ ambient.

\[
\text{Ln}_2\text{O}_3 + \text{H}_2\text{O} \xrightarrow{.} \text{Ln}_2(\text{OH})_3
\]

\[
\text{Ln}_2\text{O}_3 + \text{H}_2\text{O} \xrightarrow{.} 2(\text{LnOOH})
\]

\[
2\text{Ln(OH)} + \text{H}_2\text{O} \xrightarrow{.} 3\text{Ln}_2(\text{OH})_3
\]

\[
\text{Ln}_2\text{O}_3 + \text{CO}_2 \xrightarrow{.} \text{Ln}_2\text{O}_2(\text{CO}_3)
\]

\[
\text{Ln} : \text{Lanthanide}
\]

Absorption of moisture and CO₂
Hygroscopic Properties of $\text{La}_2\text{O}_3$

After 30 hours in clean room (temperature & humidity controlled)
Experimental apparatus

Temperature: ~20°C
Humidity: 80%
Humidification time: 0 ~ 120 hrs

acryl (PMMA) or glass (PYREX)

Samples
Ultra pure water

Thermometer
Hygrometer

glass (PYREX)  acryl (PMMA)

*PMMA : CH₂C(CH)₃COOCH₃
Change of CET for all studied
Absorption test in case of acryl apparatus after the Al electrode formation

Moisture absorption is protected

C-V

Capacitance (µF/cm²) vs Voltage (V)

- Fresh
- 24hrs (with electrode)

Pr₂O₃ / n-Si(100)
R.T.-depo
RTA : N₂ 600°C
### Choice of High-k

<table>
<thead>
<tr>
<th>Candidates</th>
<th>HfO₂ based dielectrics are selected as the first generation materials, because of their merit in 1) band-offset, 2) dielectric constant 3) thermal stability</th>
<th>La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unstable at Si interface</td>
<td>Si + MOₓ M + SiO₂</td>
<td>Si + MOₓ MSiₓ + SiO₂</td>
</tr>
<tr>
<td>Gas or liquid at 1000 K</td>
<td>He</td>
<td>B C N O F Ne</td>
</tr>
<tr>
<td>Radio active</td>
<td>Al Si P S Cl Ar</td>
<td></td>
</tr>
<tr>
<td>Li</td>
<td>Be</td>
<td></td>
</tr>
<tr>
<td>Na</td>
<td>Mg</td>
<td></td>
</tr>
<tr>
<td>K</td>
<td>Ca Sc</td>
<td></td>
</tr>
<tr>
<td>Sr Y Zr</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cs Ba</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fr Ra</td>
<td></td>
<td></td>
</tr>
<tr>
<td>La Ce Pr Nd Sm Eu Gd Tb Dy Ho Er Tm Yb Lu</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ac Th Pa U Np Pu Am Cm Bk Cf Es Fm Md No Lr</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

R. Hauser, IEDM Short Course, 1999
Mobility degradation causes for High-k MOSFETs (HfO$_2$, Al$_2$O$_3$ based oxide)

Remote scattering is dominant

S. Saito et al., IEDM 2003,
S. Saito et al., ECS Symp. on ULSI Process Integration
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness
Present Status of high-k Research

HfSiON:
- High effective mobility even at EOT=1nm
- Thermal stability
- IL of 0.5~0.7nm is essential for high \( \mu \)
- Difficult to achieve EOT<0.7nm?

**References**

[1] C. Choi, VLSI05
[2] R. Choi, IEDM02
[3] Y. Akasaka, VLSI05
[7] S. J. Rhee, VLSI05
For the past 45 years, SiO2 and SiON have been used for gate insulators. However, as we move towards the 45nm node ($L_g=22$nm), EOT can be reduced further beyond 0.5 nm by using direct contact to Si. By choosing appropriate materials and processes, EOT can be reduced to 0.7~0.8 nm.

One order of magnitude improvement in EOT is observed. Today, EOT is 1.0 nm, but with the introduction of High-k materials, EOT can be reduced to 0.5 nm. This reduction in EOT leads to a decrease in power per MOSFET ($P$).
High-k for Further Scaling

SiO$_x$ interfacial layer (typ. 0.5~0.7nm)

- Hf based oxide limit excess gate leakage

SiO$_2$ interfacial layer inserted or re-grown for
- recovery of degraded mobility
- interface state, reliability (TDDB, BTI), etc.

- SiO$_2$-IL free structure (direct contact of high-k/Si) is required for EOT=0.5nm
- EOT scaling is expected down to 0.5 nm in ITRS
SiO$_x$-IL growth at HfO$_2$/Si Interface

Phase separator

HfO$_2$ + Si + O$_2$ $\rightarrow$ HfO$_2$ + Si + 2O* $\rightarrow$ HfO$_2$ + SiO$_2$

Oxygen supplied from W gate electrode

SiO$_x$-IL is formed after annealing
Oxygen control is required for optimizing the reaction

D.J. Lichtenwalner, Trans. ECS 11, 319
H. Shimizu, JJAP, 44, pp. 6131
La-Silicate Reaction at La$_2$O$_3$/Si

Direct contact high-k/Si is possible

La$_2$O$_3$ + Si + nO$_2$

- La$_2$SiO$_5$, La$_2$Si$_2$O$_7$,
- La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
Gate Leakage vs EOT, ($V_g=|1|V$)}

![Graph showing gate leakage vs EOT with various materials represented by different markers.](image)

- **Materials**: Al$_2$O$_3$, HfAlO(N), HfO$_2$, HfSiO(N), HfTaO, La$_2$O$_3$, Nd$_2$O$_3$, Pr$_2$O$_3$, PrSiO, PrTiO, SiON/SiN, Sm$_2$O$_3$, SrTiO$_3$, Ta$_2$O$_5$, TiO$_2$, ZrO$_2$(N), ZrSiO, ZrAlO(N).
Quantum Effect in Gate Stack

- Poly-Si (10^20 cm^-3): 0.3 nm
- Metal: 0.1 nm
- K. Natori, SSDM (2005)

Thickness shown in EOT

- 0.5 ~ 0.6 nm
- depending on $E_{eff}$

Total parasitic capacitance ~ 0.6nm of EOT

- A question if the performance improvement can be obtained with EOT<0.5nm
- Is EOT<0.5nm achievable?
EOT = 0.48 nm

Transistor with La2O3 gate insulator

Our results
Electrical Characterization of thin \( \text{La}_2\text{O}_3 \) MOSFET EOT<0.5nm
EOT<0.5nm with Gain in Drive Current

14% of $I_d$ increase is observed even at saturation region

EOT below 0.4nm is still useful for scaling
Mobility concerns
Electrical characteristics of W/La$_2$O$_3$ nFET annealed at 500 °C

W/La$_2$O$_3$/nFET, 500°C anneal

Improvement in electrical characteristics
SS=66mV/dec, $\mu_{\text{eff}}=300\text{cm}^2/\text{Vs}$

EOT grows from 0.5 to 1.3nm
Schematic illustration of $\mu_{\text{eff}}$ reduction at small EOT

Spatial distribution of metal gate induced defects approaches to high-k/Si interface with small EOT

Some of the defects generates interfacial states
\( \mu_{\text{eff}} \) of W/La\(_2\)O\(_3\) and W/HfO\(_2\) nFET on EOT

- W/La\(_2\)O\(_3\) exhibits higher \( \mu_{\text{eff}} \) than W/HfO\(_2\)
- \( \mu_{\text{eff}} \) start degrades below EOT=1.4nm
FET characteristics of W/La$_2$O$_3$ on EOT

All characteristics start to degrade or shift below EOT=1.4nm

N$_{fix}$=7x10$^{12}$ cm$^{-2}$

Aggressive N$_{fix}$ generation at EOT<1.2nm

N$_{fix}$ and D$_{it}$

All characteristics start to degrade or shift below EOT=1.4nm
Gate Metal Induced Defects Compensation

Suppression of aggressive shift in $V_{fb}$

TEM

EDX
Mobility Improvement with Mg Incorporation

Recovery of $\mu_{\text{eff}}$ mainly at low $E_{\text{eff}}$
Material selection against EOT growth

1. metal selection
2. high-k selection
EOT growth of W/La$_2$O$_3$ on annealing temperature

30min in F.G.

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

Silicate reaction further proceeds with the annealing temperature
Suppression of Silicate Reaction

Oxygen block

Barrier for Ta diffusion

Limited silicate reaction

La$_2$O$_3$ + Si + nO$_2$ → La$_2$SiO$_5$, La$_2$Si$_2$O$_7$, La$_{9.33}$Si$_6$O$_{26}$, La$_{10}$(SiO$_4$)$_6$O$_3$, etc.

Oxygen control is the key technology in achieving small EOT with high temperature annealing
Cap effect of SrO

Selection of rare earth silicate for interface layer
Find out the effect of SrO capping
SrO capping for achieving small EOT

500 °C anneal (30min)

La₂O₃ (1nm) on RE-silicate

<table>
<thead>
<tr>
<th></th>
<th>w/o SrO capping</th>
<th>with SrO capping</th>
</tr>
</thead>
<tbody>
<tr>
<td>La-silicate</td>
<td>1.5</td>
<td>1.0</td>
</tr>
<tr>
<td>Ce-silicate</td>
<td>1.0</td>
<td>0.5</td>
</tr>
<tr>
<td>Pr-silicate</td>
<td>1.5</td>
<td>1.0</td>
</tr>
</tbody>
</table>

Diffusion of Sr to enhance the dielectric constant of RE-silicate

0.5nm EOT can be achieved with Ce-silicate capped with SrO which enhances the k-value
EDX Analysis of the Distribution of Sr

Sr is diffused into Ce-silicate and possibly down to Si interface.
SrO effect on Current Density

Further EOT scaling is possible
A guideline for material selection: direct contact of high-k with Si structure

- Suppression of fixed charge by diffuse into high-k
  - Careful thickness control not to diffuse down to Si surface

- High dielectric constant and wide bandgap for leakage suppression
  - Low fixed charge density by SrO incorporation

- High dielectric constant assisted by Sr incorporation
  - Diffusion barrier for Sr toward Si surface
Si Nanowire FET
FinFET to Nanowire

Channel conductance is well controlled by Gate even at L=5nm

Ion/Ioff=230000

 Ion/Ioff=52200

N-FET
(L_g=10 nm)
Swing =75 mV/ déc
DIBL =80 mV/V
I_{off}=10 nA/μm

N+ Poly Si Gate

Buried Oxide

10nm

F.-L.Yang, VLSI2004
Si nanowire FET as a strong candidate after CMOS limitation

1. Compatibility with current CMOS process
2. Good controllability of $I_{OFF}$
3. High drive current

1D ballistic conduction

Multi quantum Channel

High integration of wires

by the courtesy of Professor H. Iwai
1D conduction per one quantum channel:
\[ G = \frac{2e^2}{h} = 77.5 \, \mu\text{S/wire or tube} \]
regardless of gate length and channel material

That is 77.5 microA/wire at 1V supply

This an extremely high value

However, already 20 micro A/wire was obtained experimentally by Samsung
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Maximum number of wires per 1 µm

Front gate type MOS 165 wires /µm

Surrounded gate type MOS 33 wires/µm

6nm pitch
By nano-imprint method

- Metal gate electrode (10nm)
- High-k gate insulator (4nm)
- Si Nano wire (Diameter 2nm)

30nm pitch: EUV lithography

Surrounded gate MOS
Increase the number of wires towards vertical dimension
Theoretical model of SiNW FET
Landauer Formalism for Ballistic FET

Potential Energy

\[ \frac{dU_L(x)}{dx} \approx 0 \]

\[ I_D = \frac{q}{\pi \hbar} \sum_i \int [f(E, \mu_S) - f(E, \mu_D)] T_i(E) dE \]

From \( x_{\text{max}} \) to \( x_{\text{min}} \)

\[ T_i(E) \approx 1 \]

\[ I_D = G_0 \left( \frac{k_B T}{q} \right) \sum_i g_i \ln \left\{ \frac{1 + \exp\left[ (\mu_S - E_{i0}) / k_B T \right]}{1 + \exp\left[ (\mu_D - E_{i0}) / k_B T \right]} \right\} \]
Carrier Density obtained from E-k Band

\[ |Q| = |Q_f| + |Q_b| \]

\[
= \frac{q}{\pi} \sum_i g_i \left[ \int_{k_{i \text{min}}}^{\infty} dk \frac{dk}{1 + \exp \left( \frac{E_i(k) - \mu_S}{k_B T} \right)} + \int_{-\infty}^{k_{i \text{min}}} dk \frac{dk}{1 + \exp \left( \frac{E_i(k) - \mu_D}{k_B T} \right)} \right]
\]
Carrier Density obtained from Band Diagram

\[
\frac{|Q|}{C_G} = (V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q}
\]

\[
\alpha = 1 + \frac{C_P}{C_G}
\]
IV Characteristics of Ballistic SiNW FET

Small temperature dependency
35\(\mu\)A/wire for 4 quantum channels
Model of Carrier Scattering

Linear Potential Approx. : Electric Field $E$

Transmission Probability to Drain

$T(\varepsilon) = \frac{F(0) - G(0)}{F(0)}$  
Injection from Drain=0
Résumé of the Compact Model

\[ I = \frac{q}{\pi \hbar} \sum_i g_i \int [f(\varepsilon, \mu_s) - f(\varepsilon, \mu_D)] T_i d\varepsilon \]

\[ (V_G - V_i) - \alpha \frac{\mu_S - \mu_0}{q} = \frac{|Q_f + Q_b|}{C_G}. \]

\[ \mu_S - \mu_D = qV_D \]

\[ C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left( \frac{\sqrt{2r+t_{ox}} + \sqrt{t_{ox}}}{\sqrt{2r+t_{ox}} - \sqrt{t_{ox}}} \right)}. \]

(Planar Gate)

\[ C_G = \frac{2\pi \varepsilon_{ox}}{\ln \left( \frac{r+t_{ox}}{r} \right)}. \]

(GAA)

\[ |Q_f + Q_b| = \frac{q}{\pi} \sum_i g_i \left[ \int_{-\infty}^{\infty} \frac{dk}{1 + \exp \left\{ \frac{\varepsilon_i(k) - \mu_S}{k_BT} \right\}} - \int_{-\infty}^{0} \frac{1}{1 + \exp \left\{ \frac{\varepsilon_i(k) - \mu_S}{k_BT} \right\}} - \int_{0}^{\infty} \frac{1}{1 + \exp \left\{ \frac{\varepsilon_i(k) - \mu_D}{k_BT} \right\}} \right] T_i(\varepsilon_i(k))dk \]

(Planar Gate)

\[ T(\varepsilon) = \frac{\sqrt{2D_0 qE}}{\left( \sqrt{B_0 + D_0} + \sqrt{D_0} \right) qE + \sqrt{2mD_0B_0} \ln \left( \frac{qEx_0 + \varepsilon}{\varepsilon} \right)} \]

(Carrier distribution in Subbands)

Unknowns are \( I_D, (\mu_S - \mu_0), (\mu_D - \mu_0), \) および \((Q_f+Q_b)\)
I-$V_D$ Characteristics (RT)

- Electric current: $20 \sim 25 \mu A$
- No saturation at Large $V_D$
Cross section of Si NW

First principal calculation, TAPP

D=1.96nm [001]  D=1.94nm [011]  D=1.93nm [111]
Si nanowire FET with 1D Transport

Orientation | [001] | [011] | [111]
Diameter (nm) | 0.86 | 0.94 | 0.89

<table>
<thead>
<tr>
<th>Energy (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>G</td>
</tr>
</tbody>
</table>
Wave Number

Small mass with [011]
Large number of quantum channels with [001]
Effective mass

Electron

Hole

Lighter effective masses make conductance higher

Electron

Hole

[100] [111] > [110] lighter

[100] [110] [111]
Numbers of Quantum Channels

Quantum channels denote subband edges within 0.1 eV from CBM and VBM

Quantum channels increase in large wire

Quantum channel → Passage for transport

CB
[110] [111] < [100]

VB
[111] < [110] < [100]
SiNW FET Fabrication
Brief process flow of Si Nanowire FET

1. S/D&Fin Patterining (ArF Lithography and RIE Etching)
2. Sacrificial Oxidation & Oxide Removal (not completely released from BOX layer)
3. Nanowire Sidewall Formation (oxide support protector)
4. Gate Oxidation (5nm) & Poly-Si Deposition (75nm)
5. Gate Lithography & RIE Etching
6. Gate Sidewall Formation
7. Ni SALISIDE Process
(a) Fin structure formed on BOX layer. (b) XTEM image of fin shown in (a) (c) XTEM image after sacrificial oxidation (d) Cross sectional SEM image after partial removal of sacrificial oxide (e) XTEM after nanowire sidewall formation
SiNW FET Fabrication

S/D & Fin Patterning

Sacrificial Oxidation

Oxide etch back

SiN sidewall support formation

Gate Oxidation & Poly-Si Deposition

Gate Lithography & RIE Etching

Gate Sidewall Formation

Ni SALISIDE Process (Ni 9nm / TiN 10nm)

Backend

Standard recipe for gate stack formation
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.
Fabricated SiNW FET

SiNW

SiN support

Poly-Si

Nanowire

SiN

30nm

500nm
**IdVg and IdVd Characteristics**

- Ion/Ioff ratio of ~$10^7$, high Ion of 49.6 $\mu$A/wire

\[
\begin{align*}
V_G - V_{th} &= 1.0V \\
V_G - V_{th} &= 0.8V \\
V_G - V_{th} &= 0.6V \\
V_G - V_{th} &= 0.4V
\end{align*}
\]

- S.S. = 71mV/dec
- $V_{th} = -0.36V$
- $L_g = 200nm$
- $L_g = 35nm$
- $L_g = 25nm$
Effective mobility extraction

Effective electron mobility ($\text{cm}^2/\text{V}s$)

- $L_g=500\text{nm}$
- Number of NWs: 64
- Univ. curve Si (100)
- Measured at RT

Inversion Carrier Density ($\text{cm}^{-2}$)

- Source-Drain $5\mu\text{m}$
Comparison of Si NW FET being already reported with Si NW FETs in this work

\[ (V_g - V_{th} = 1.0\text{V}) \]

- nMOS
- pMOS

our result

\( L_g \) for small
(a) 
wire formation

(b) 
(A) 10nm 10nm 10nm 
(B) 10nm 18nm 10nm 
(C) 10nm 25nm
Output characteristics of 10x10cm$^2$ SiNW FET

- Gate voltage (V): -1.0, -0.5, 0, 0.5, 1.0
- Drain voltage (V): 0, 0.2, 0.4, 0.6, 0.8, 1.0
- Drain current (µA): 40, 35, 30, 25, 20, 15, 10, 5
- Drain voltage (V): 0, 0.2, 0.4, 0.6, 0.8, 1.0
- Drain current (µA): 40, 35, 30, 25, 20, 15, 10, 5

- $V_d=1.0V$
- $V_d=50mV$
- $L_g=160nm$
- $T_{ox}=3nm$
- $V_g-V_{th}=1.2V$ (step 0.2V)

(A) 10x10nm$^2$
Even with large $L_g$, fairly nice $I_{ON}$ have been achieved
Occupying area of Si bulk planar FET and Si NW FET. Drive current should be compared with the same width, $W$. 

Planer  

Si nanowire
On current evaluation base on gate width

Numbers of wires are determined by the lithographic technology

\[ \#N = \frac{1000 \text{(nm)}}{P} \quad \text{or} \quad \frac{1000 \text{(nm)}}{D+P/2} \]

(at D<P/2)  
(at D>P/2)

<table>
<thead>
<tr>
<th>Year</th>
<th>half-pitch (nm), P</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010</td>
<td>45</td>
</tr>
<tr>
<td>2014</td>
<td>28</td>
</tr>
<tr>
<td>2018</td>
<td>18</td>
</tr>
<tr>
<td>2022</td>
<td>11</td>
</tr>
</tbody>
</table>

(based on ITRS2008update)
Performance of SiNW FET in ITRS

With device scaling in $T_{ox}$ and $L_g$, SiNW FET can exceed the required performance in ITRS.
Our new roadmap

Extended CMOS: More Moore + CMOS logic

Beyond the horizon

Natural direction of downsizing

Si Fin, Tri-gate
Si Nano wire
Ill-V Ge Nano wire
Tube
CNT
Graphene

Diameter = 2nm
Diameter = 10nm

Si Channel
Nanowire

Selection

ITRS Beyond CMOS

High conduction
By 1D conduction

Extended CMOS
More Moore

More Moore

ITRS

Cloud
Examples of foundry facility: UMC

**Fab 12A (Tainan, Taiwan)**
- US$3 billion investment
- Production since 2001
- 38K wafers/month by E/06
- 90, 65nm in production

**Fab 12i (Singapore)**
- US$3.6 billion investment
- Production since 2004
- 25K wafers/month by E/06
- 130, 90nm in production
- Ready for 65nm pilot
Volume production with larger wafer is a solution.

<table>
<thead>
<tr>
<th></th>
<th>12”-Fab</th>
<th>8”-Fab</th>
<th>12”/8” Usage Ratio</th>
<th>12”/8” Wafer Size Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power</strong></td>
<td>1,100 KWH/Wafer</td>
<td>660 KWH/Wafer</td>
<td>1.7</td>
<td></td>
</tr>
<tr>
<td><strong>Water</strong></td>
<td>6.1 M3/Wafer</td>
<td>4.7 M3/Wafer</td>
<td>1.3</td>
<td>2.25</td>
</tr>
<tr>
<td><strong>Waste Water</strong></td>
<td>3.8 M3/Wafer</td>
<td>2.9 M3/Wafer</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td><strong>Waste Air</strong></td>
<td>20,000 CMH/Wafer</td>
<td>13,000 CMH/Wafer</td>
<td>1.5</td>
<td></td>
</tr>
</tbody>
</table>

**TSMC**
Dragonfly is further high performance.

Ultra small volume
Small number of neuron cells
Extremely low power
Real time image processing (Artificial) Intelligence
3D flight control
Mosquito
Infrared Sensor
Humidity CO₂

But do not know how?
Algorithm becomes more important!
System and and
High performance!
When do we start planning for next wafer size transition?

We are here

When does this happen?

200mm/1990

(125/150mm - 1981)

9 yrs + 2 yrs delay*

300mm/2001

9 yrs? + 2 yrs delay?

450mm/2012

9 yrs + ? yrs delay

675mm/2021

When do we start planning for next wafer size transition?
Crystal pulling furnace becomes too huge
Si crystal height cannot be very long because of its weigh

**Furnace**
- Height: 12 m
- Weight: 36 ton
- Hot zone: 40 inch
- Cusp-type super conductive magnet

**Crystal**
- Diameter: 400 mm
- Weight: over 400 kg
- Body length: over 1 m
Conclusions

1. High-k with EOT less than 0.5 nm is promising.

2. Si-Nanowire MOSFETs have very high possibility to take over after conventional planar CMOS reaches the scaling limit.

3. III-V MOSFETs:
   We have just started the joint-research with NCTU, through JST-NSC Japan-Taiwan program and wish to have successful results in 3 years.