High-k Gate Stack Technology Beyond 0.5 nm EOT

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Tokyo Institute of Technology

Hiroshi Iwai

Cool Earth by integrated circuits

1.By controlling the system by microprocessor (Integrated Circuits) more efficiently, energy consumption of the system will be significantly reduced.

Every human system：transportation system, manufacturing, Office

2.Power saving of Integrated Circuits in IT network （Server, Data Center, Router）

Power of Transistor $= CV^2/2$

C: Capacitance of Tr $\propto$ D   D : Size

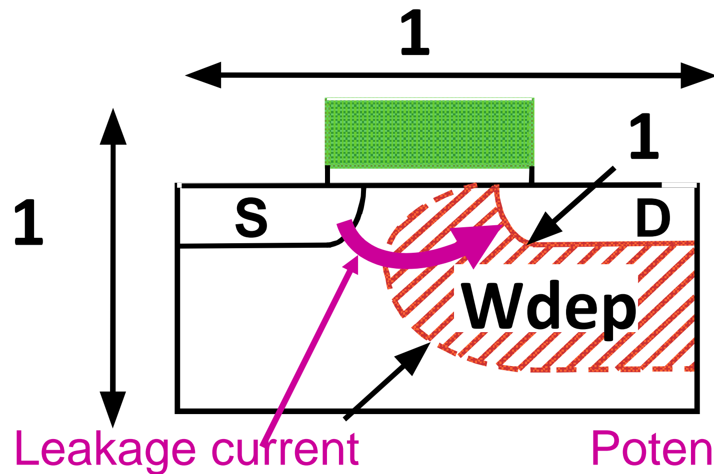
V: Supply Voltage

To reduce the power, D and V should be reduced!

Scaling: Every 3 years; D and V reduces with 0.7 times

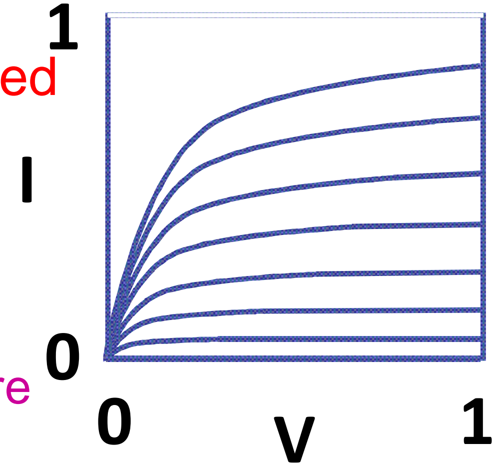
k= 0.7 in 3 years	k= 0.7^2 =0.5 in 6 years
MOFET	MOFET
Vdd → 0.7	Vdd → 0.5
Lg → 0.7	Lg → 0.5
Id → 0.7	Id → 0.5
Cg → 0.7	Cg → 0.5
P (Power)/Clock → $0.7^3 = 0.34$	P (Power)/Clock → $0.5^3 = 0.125$
τ (Switching time) → 0.7	τ (Switching time) → 0.5

Scaling Method: by R. Dennard in 1974

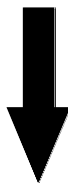


Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage between S and D



Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

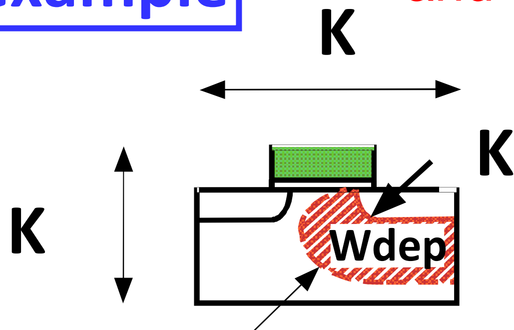


K=0.7 for example

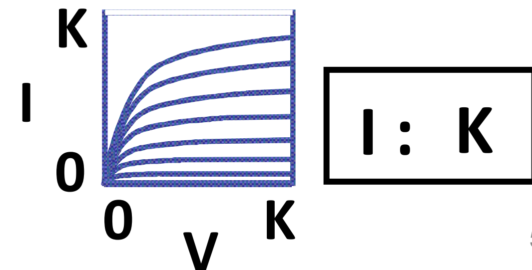
X , Y , Z : K, V : K, Na : 1/K

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$Wdep \propto \sqrt{V/Na}$$
: K

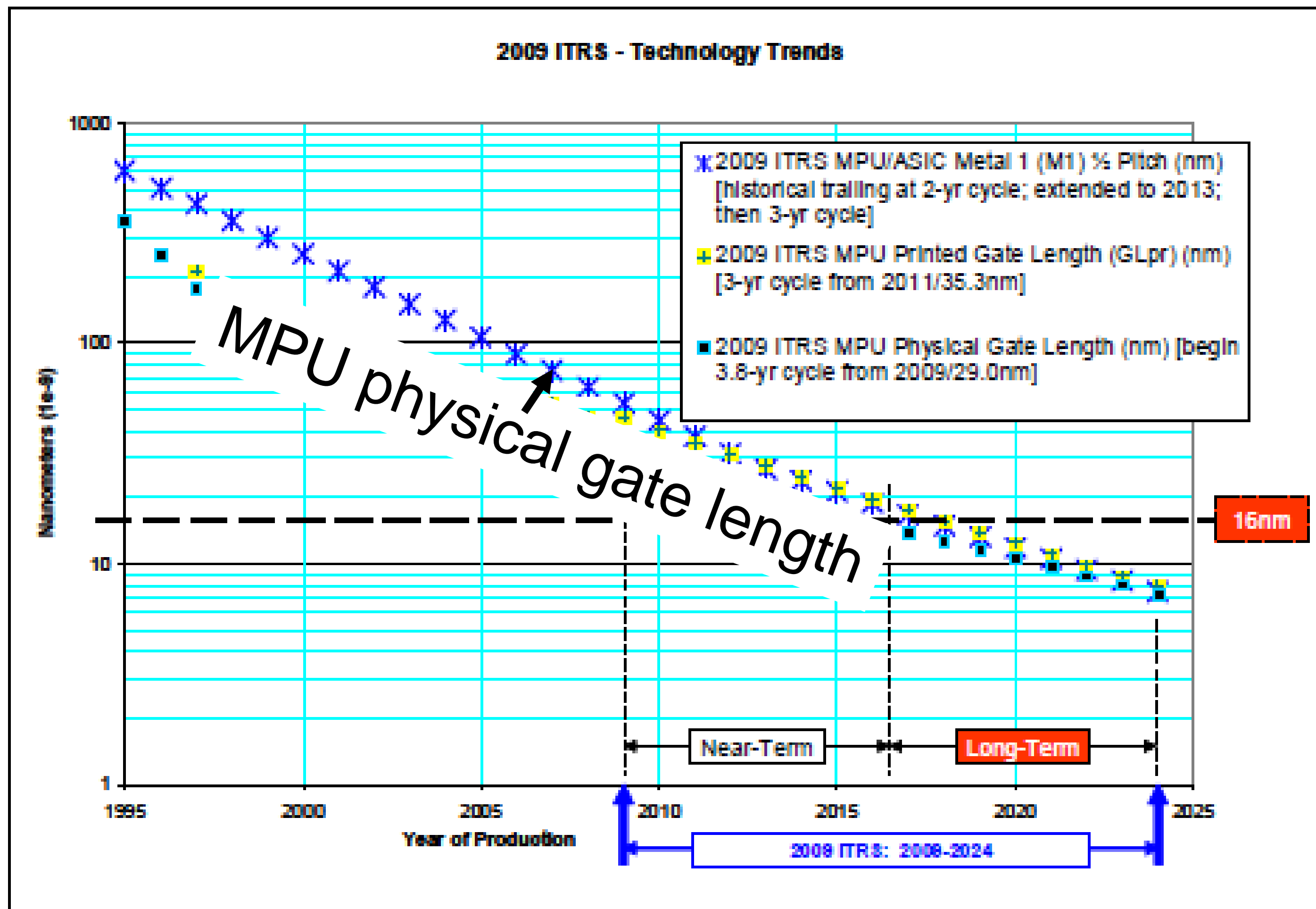


I : K

ITRS expect Lg less than 10nm

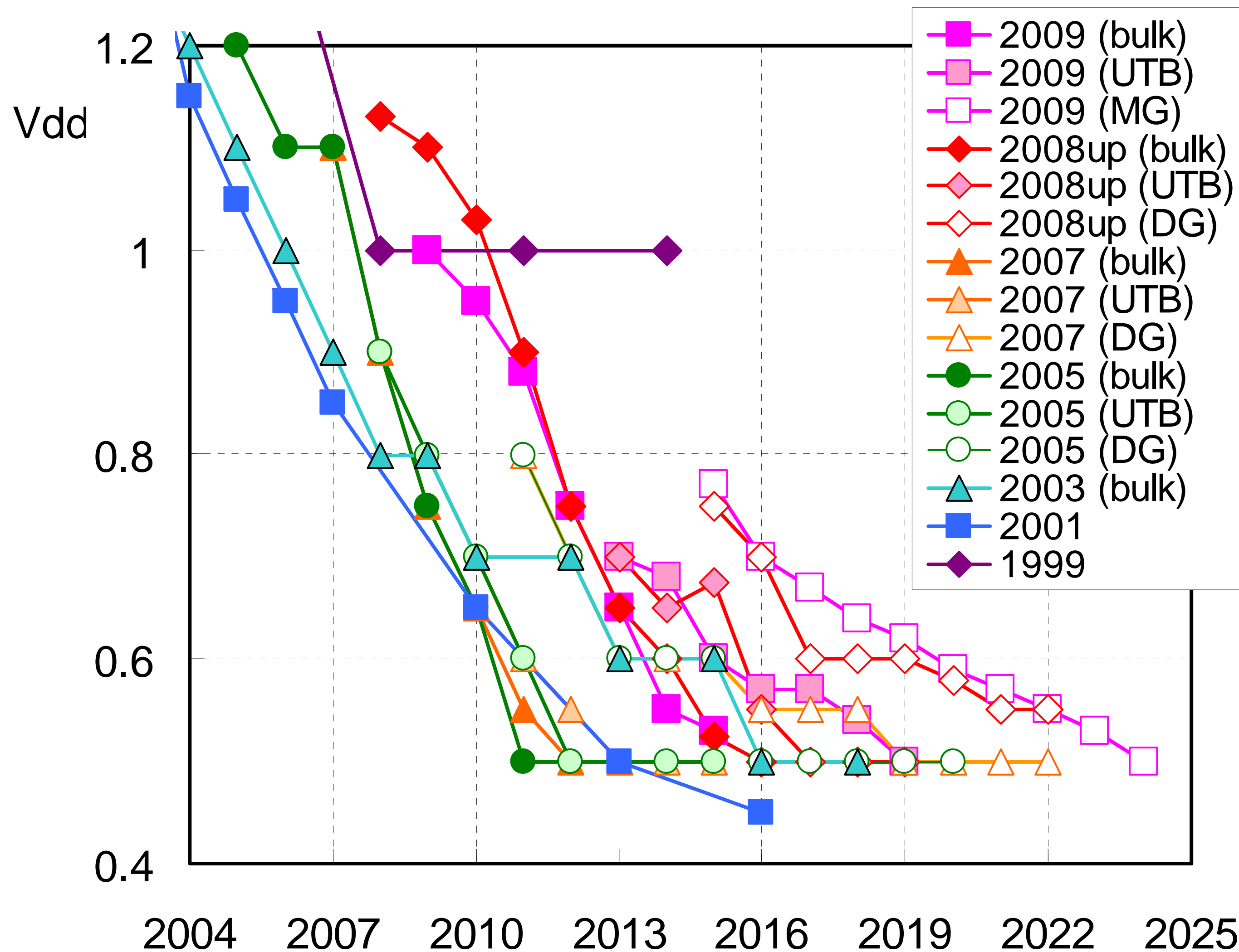
ITRS: International Technology Roadmap for Semiconductors

2009 ITRS Technology Trend: MPU gate length



However EOT stops at 0.5 nm in ITRS!

EOT (Equivalent oxide thickness of gate insulator)



How far can we go?

Past

0.7 times per 3 years

In 40 years: 15 generations,
Size 1/200, Area 1/40,000

1973年

Now

8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm

→ 0.35μm → 0.25μm → 180nm → 130nm → 90nm → 65nm → 45nm

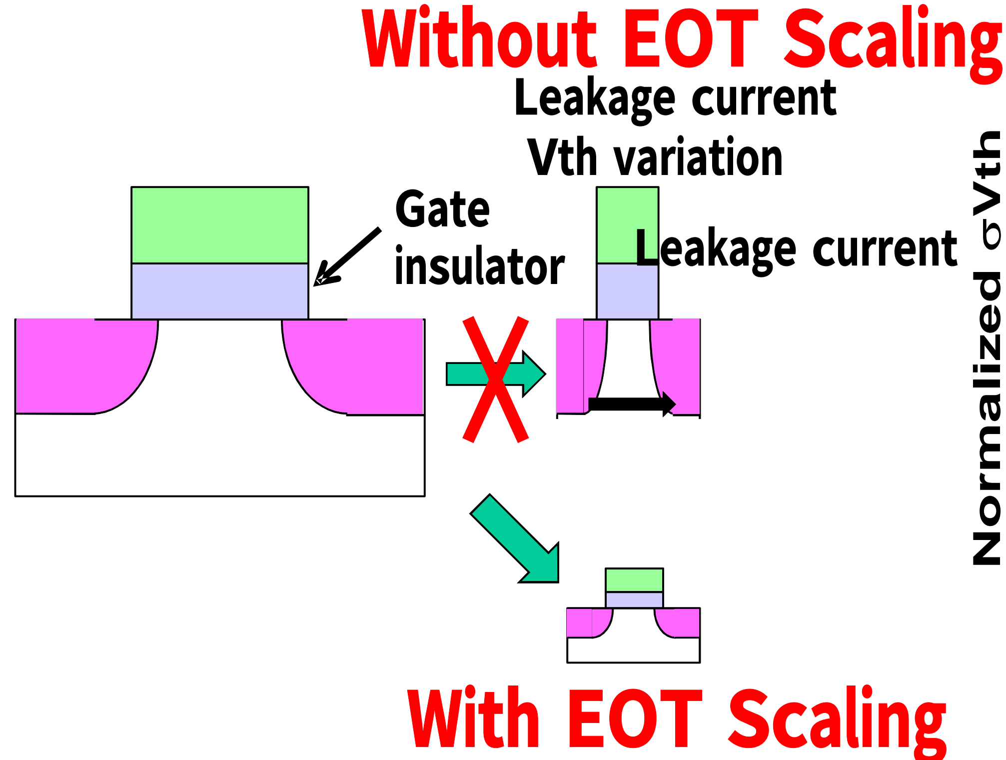
Future

→ 32nm → 22nm → 16nm → 11.5 nm → 8nm → 5.5nm? → 4nm? → 2.9 nm?

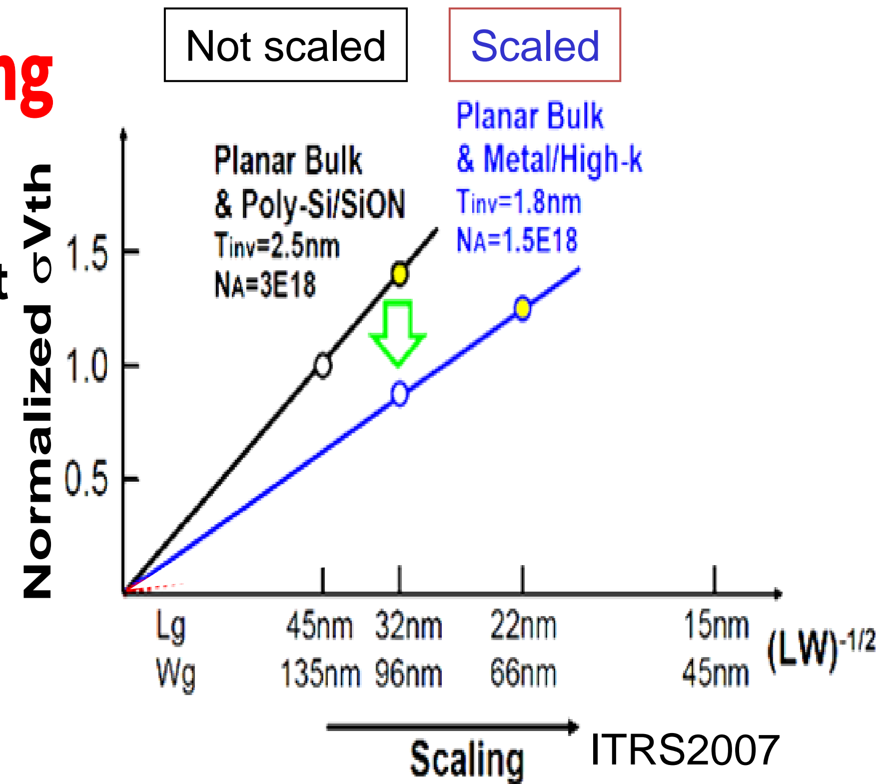
- **At least 5,6 generations, for 15 ~ 20 years**
- **Hopefully 8 generations, for 30 years**

$k = 0.7$ and $\alpha = 1$	$k = 0.7^2 = 0.5$ and $\alpha = 1$
Single MOFET	
Vdd → 0.7	Vdd → 0.5
Lg → 0.7	Lg → 0.5
Id → 0.7	Id → 0.5
Cg → 0.7	Cg → 0.5
P (Power)/Clock → $0.7^3 = 0.34$	P (Power)/Clock → $0.5^3 = 0.125$
τ (Switching time) → 0.7	τ (Switching time) → 0.5
Chip	
N (# of Tr) → $1/0.7^2 = 2$	N (# of Tr) → $1/0.5^2 = 4$
f (Clock) → $1/0.7 = 1.4$	f (Clock) → $1/0.5 = 2$
P (Power) → 1	P (Power) → 1

Without EOT scaling
→ Huge Off leakage and Vth variation



Vth variation



Thus, EOT scaling beyond 0.5 nm is very important!

Choice of High-k

Candidates

● Gas or liquid at 1000 K

○ Radio active

Unstable at Si interface

① $Si + MO_X \quad M + SiO_2$

② $Si + MO_X \quad MSi_X + SiO_2$

③ $Si + MO_X \quad M + MSi_XO_Y$

● H ● He

Li Be ● B ● C ● N ● O ● F ● Ne

① Na Mg Al Si ● P ● S ● Cl ● Ar

K Ca Sc ② Ti ① V ① Cr ① Mn ① Fc ① Co ① Ni ① Cu ① Zn ① Ga ① Ge ● As ● Se ● Br ● Kr

● Rh Sr Y Zr ① Nb ① Mo Tc ① Ru ① Rb ① Pd ● Ag ① Cd ① In ① Sn ① Sb ① Te ● I ● Xe

● Cs ③ Ba ★ Hf ① Ta ① W ① Re ① Os ① Ir ● Pt ● Au ● Hg ● Tl ① Pb ① Bi ○ Po ○ At ○ Rn

○ Fr ○ Ra ☆ ○ Rf ○ Ha ○ Sg ○ Ns ○ Hs ○ Mt

★ La Ce Pr Nd ○ Pm Sm Eu Gd Tb Dy Ho Er Tm Yb Lu

☆ ○ Ac ○ Th ○ Pa ○ U ○ Np ○ Pu ○ Am ○ Cm ○ Bk ○ Cf ○ Es ○ Fm ○ Md ○ No ○ Lr

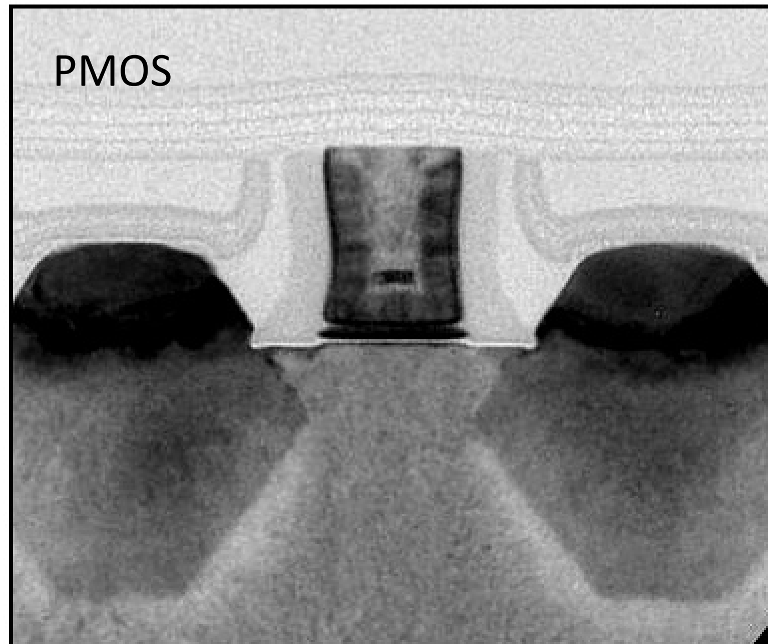
HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

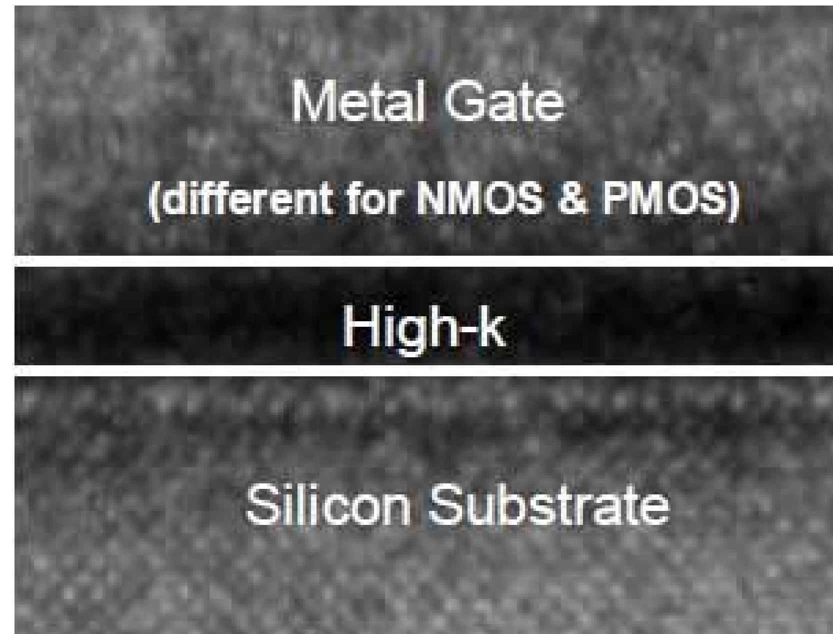
La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

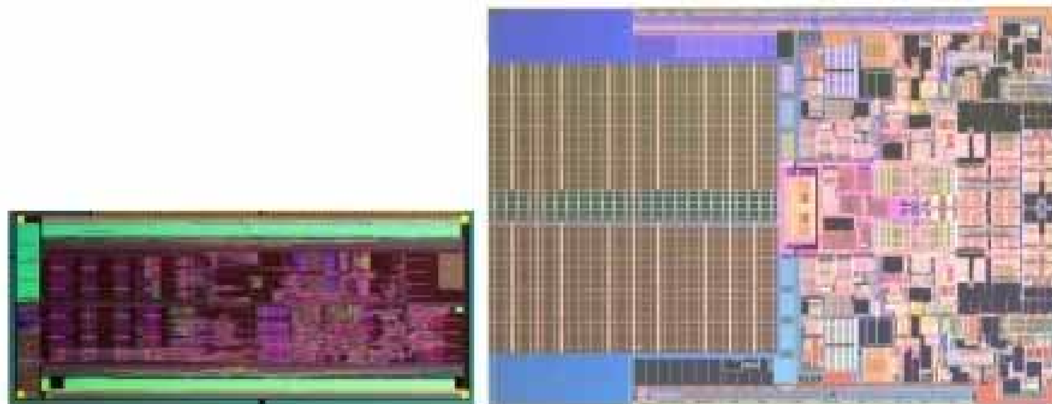
R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

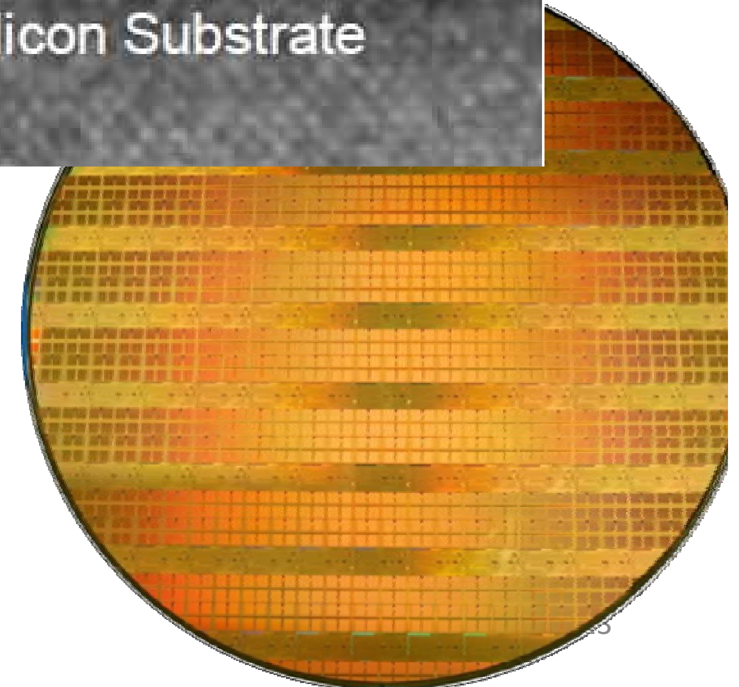
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness

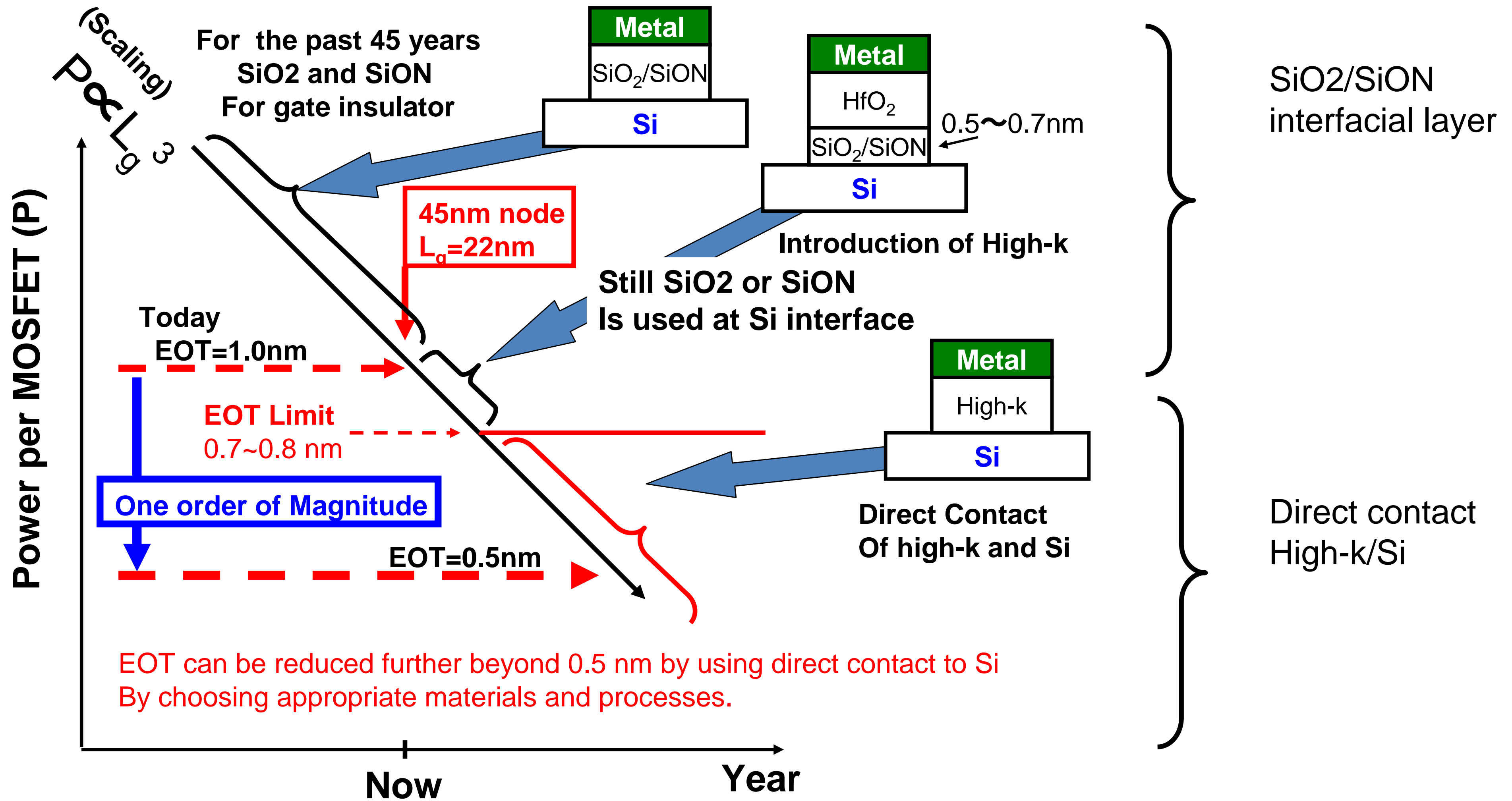




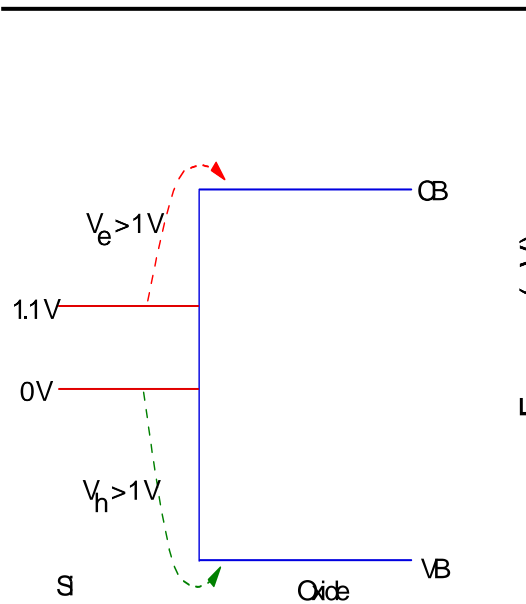


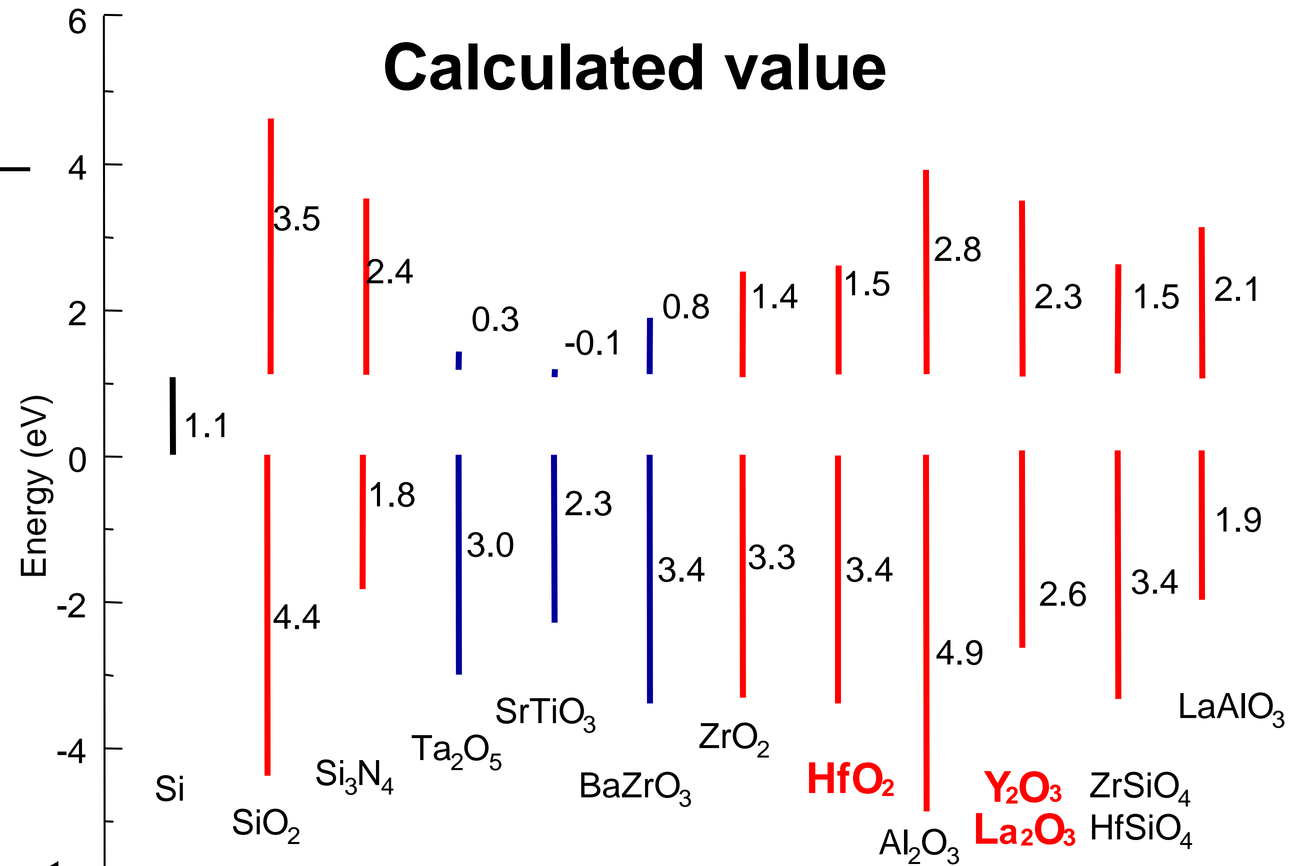


Direct contact technology of high-k to Si



Band Offsets





J Robertson, J Vac Sci Technol B **18** 1785 (2000)

Dielectric constant

SiO2; 4
Si3N4: ~ 7
Al2O3: ~ 9

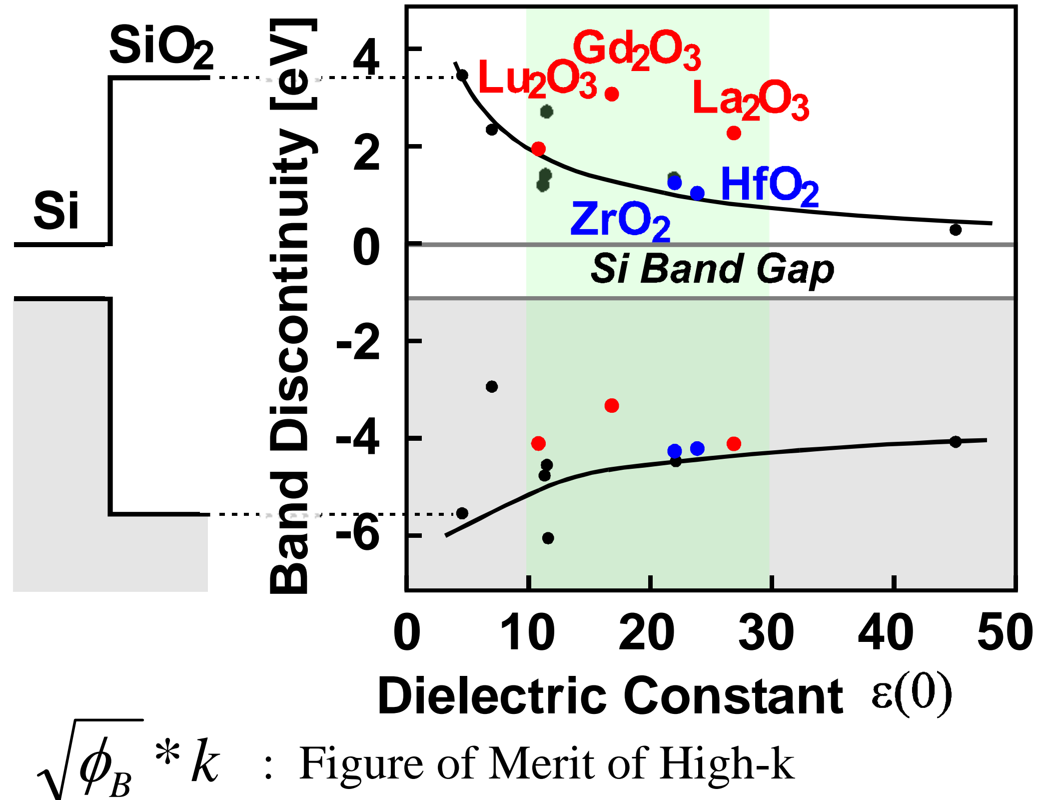
Y2O3; ~10
Gd2O3: ~10

HfO2; ~23
La2O3: ~27

HfO2 was chosen for the 1st generation
La2O3 is more difficult material to treat

Dielectric constant value vs. Band offset (Measured)

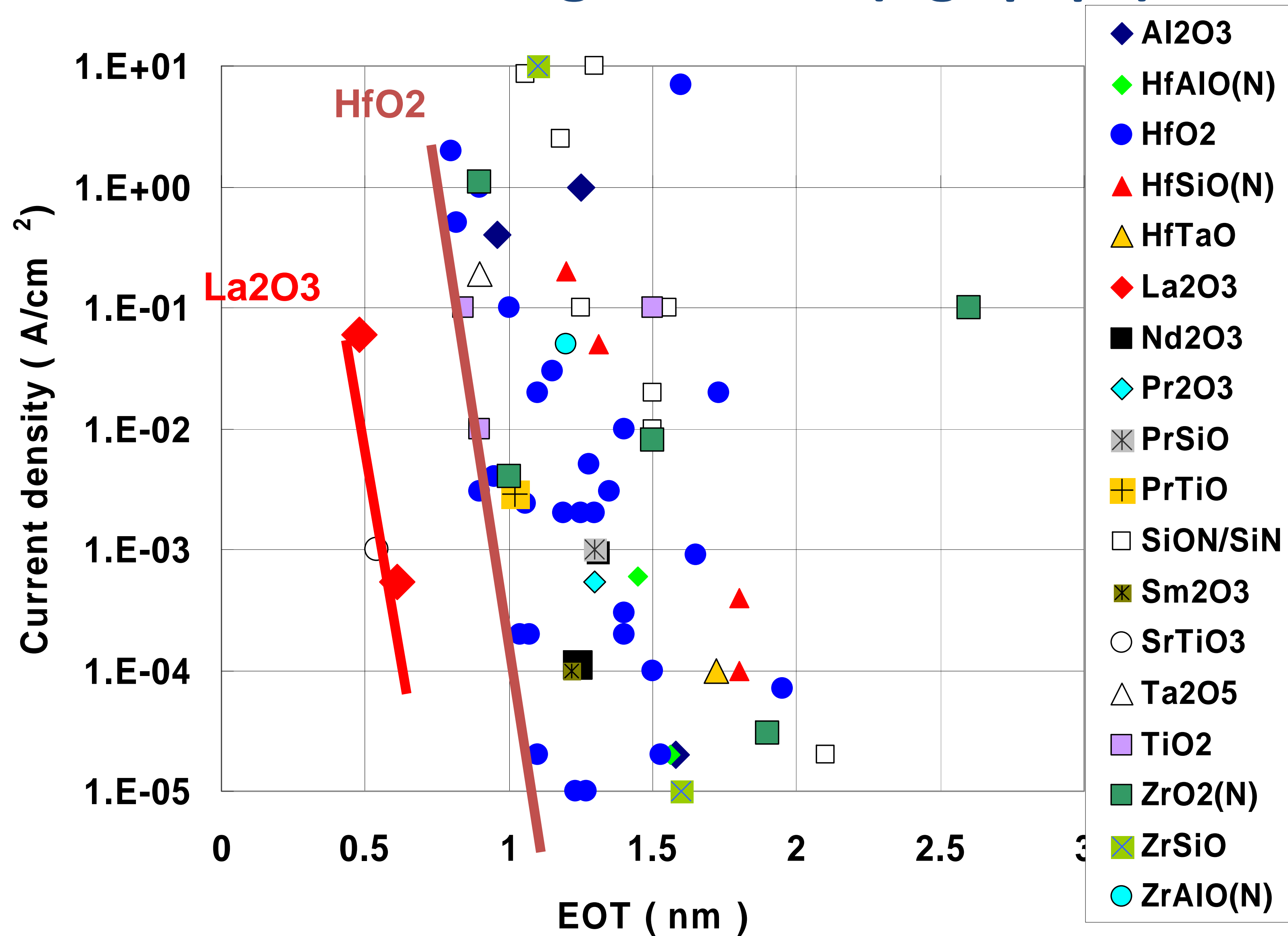
Material	Dielectric constant
SiO_2	3.9
Al_xSi_yOz	
$(Ba,Sr)TiO_3$	200-300
$BeAl_2O4$	8.3-9.43
CeO_2	16.6-26
$CeHfO_4$	10-20
$CoTiO_3/Si_3N_4$	
$EuAlO_3$	22.5
HfO_2	26-30
Hf silicate	11
La_2O_3	20.8
$LaScO_3$	30
La_2SiO_5	
$MgAl_2O_4$	
$NdAlO_3$	22.5
$PrAlO_3$	25
Si_3N_4	7
$SmAlO_3$	19
$SrTiO_3$	150-250
Ta_2O_5	25-24
$Ta_2O_5-TiO_2$	
TiO_2	86-95
TiO_2/Si_3N_4	
Y_2O_3	8-11.6
$Y_xSi_yO_z$	
ZrO_2	22.2-28
Zr-Al-O	
Zr silicate	
$(Zr,Sn)TiO_4$	40-60



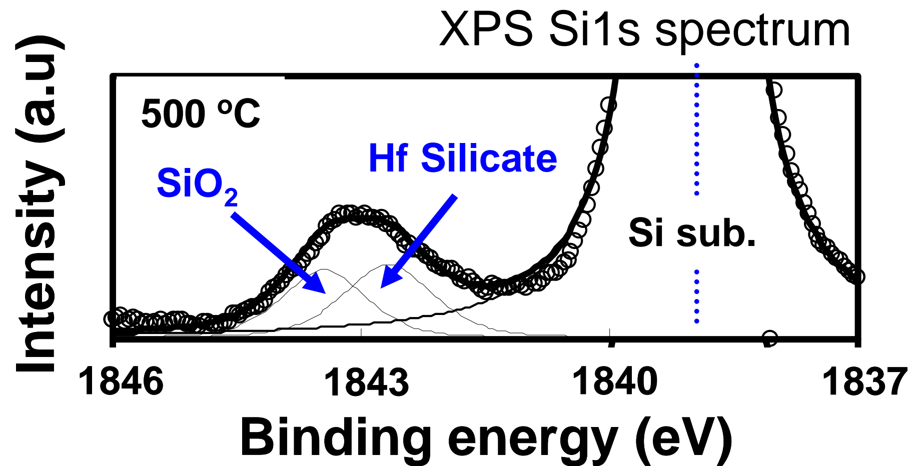
C.A. Billmann et al.,, MRS Spring Symp., 1999,
R.D.Shannon, J. Appl. Phys., 73, 348, 1993
S. De Gebdt, IEDM Short Coyuse, 2004

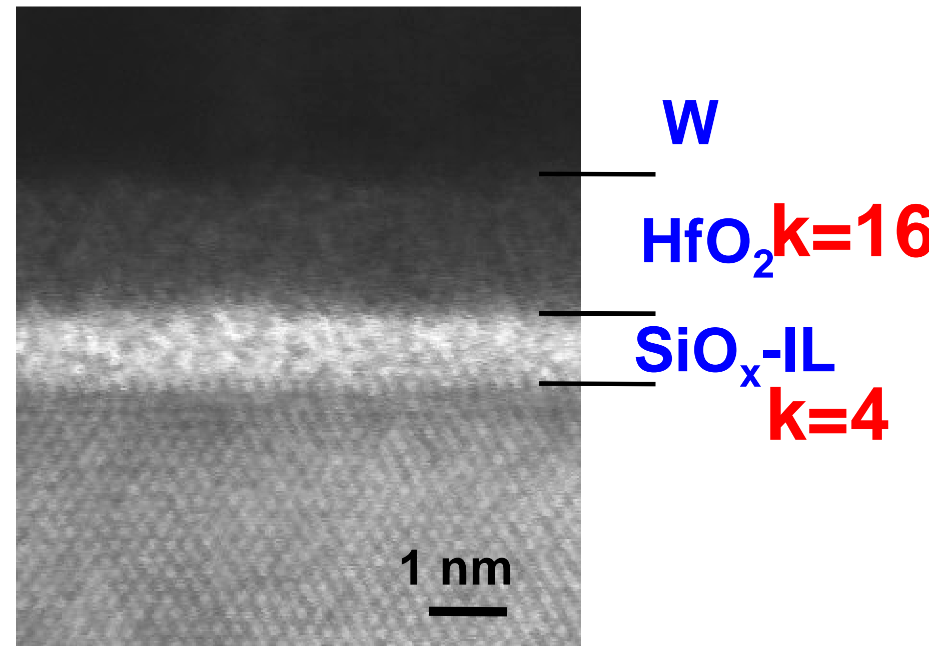
T. Hattori, INFOS , 2003

Gate Leakage vs EOT, (Vg=|1|V)

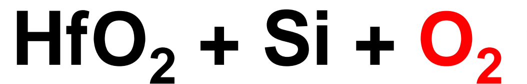
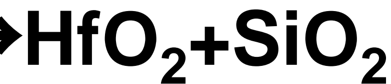


SiO_x-IL growth at HfO_2/Si Interface



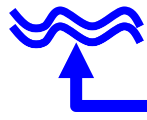


Phase separator

$$HfO_2 + Si + O_2 \rightarrow HfO_2 + Si + 2O^* \rightarrow HfO_2 + SiO_2$$

H. Shimizu, JJAP, 44, pp. 6131



Oxygen supplied from W gate electrode

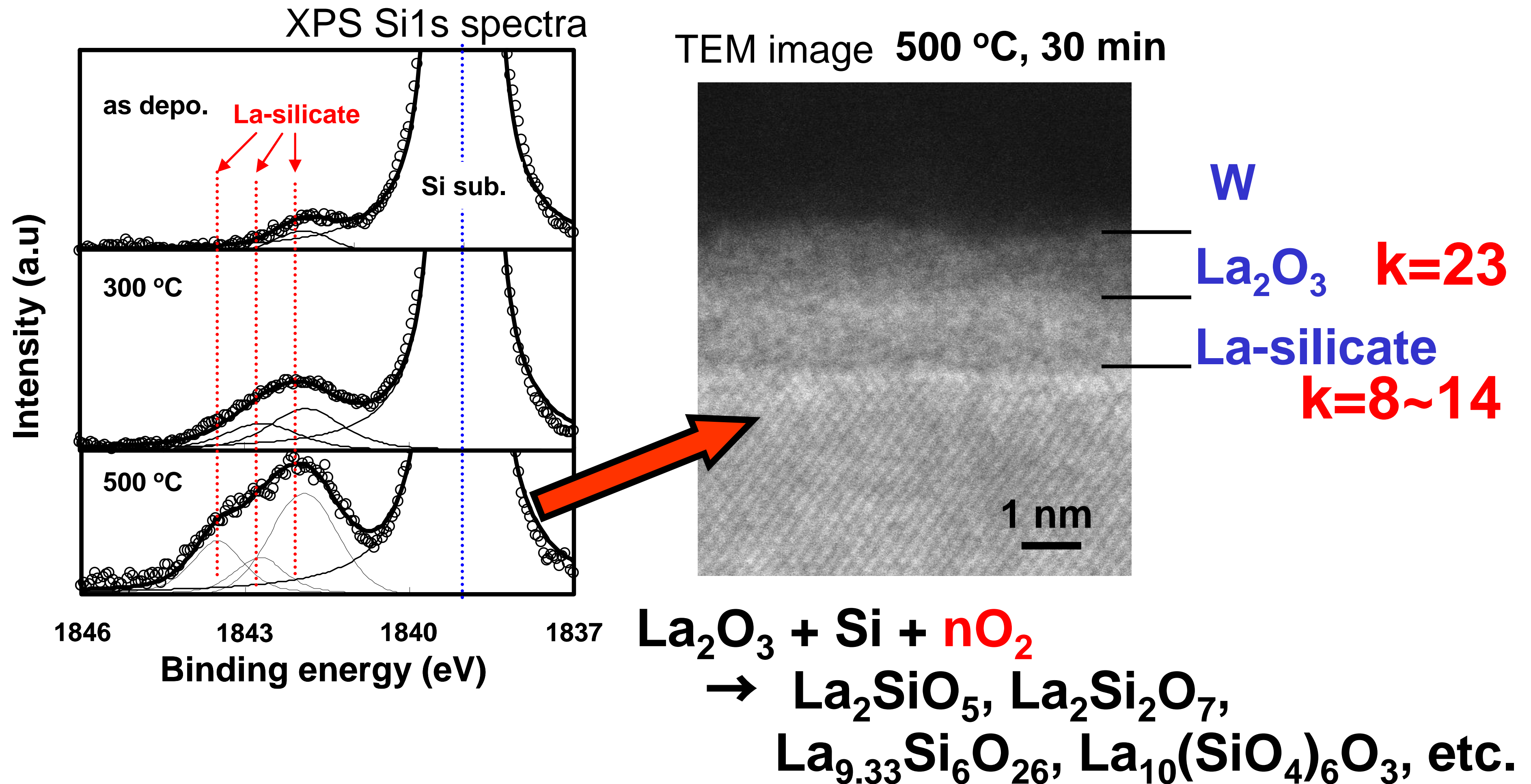
D.J.Lichtenwalner, Tans. ECS 11, 319

SiO_x-IL is formed after annealing

Oxygen control is required for optimizing the reaction

La-Silicate Reaction at La_2O_3/Si

Direct contact high-k/Si is possible



La_2O_3 + Si + nO_2

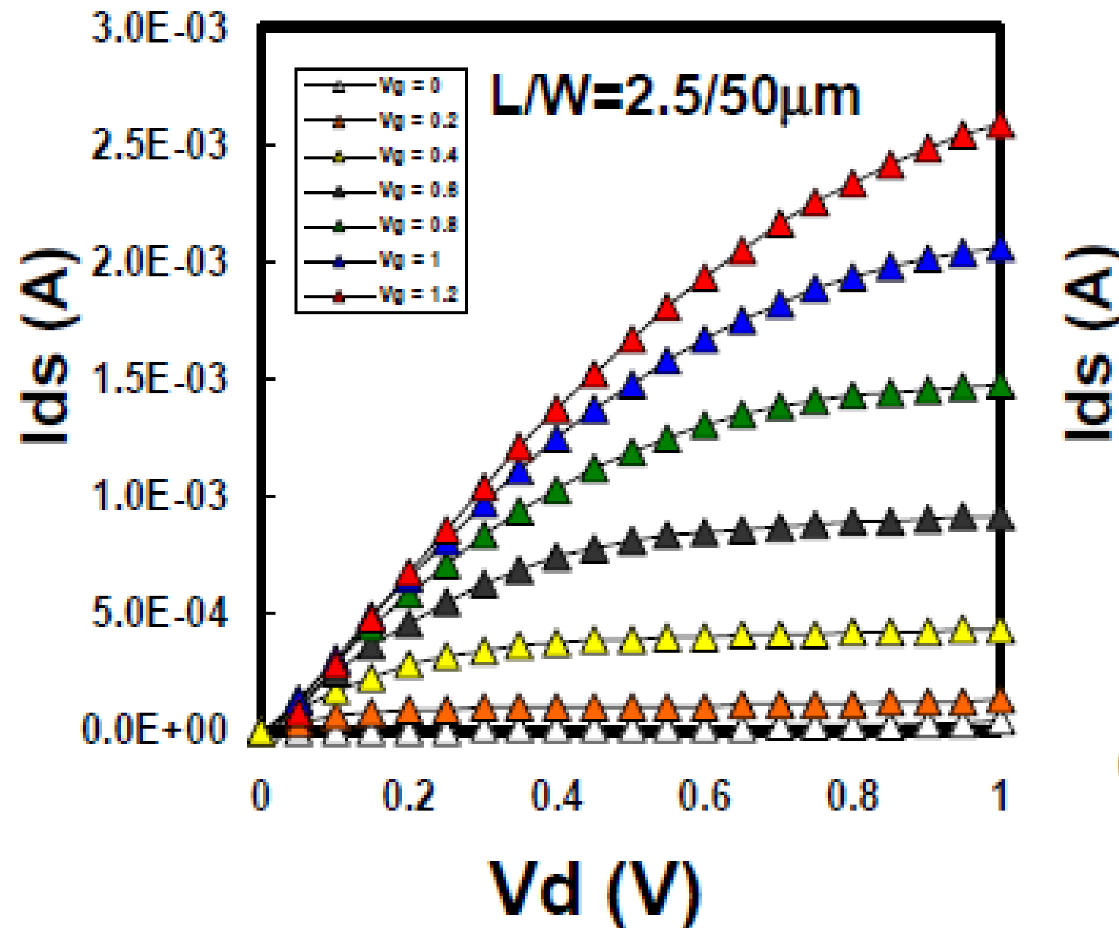
→ La_2SiO_5, $La_2Si_2O_7$, $La_{9.33}Si_6O_{26}$, $La_{10}(SiO_4)_6O_3$, etc.

La_2O_3 can achieve direct contact of high-k/Si

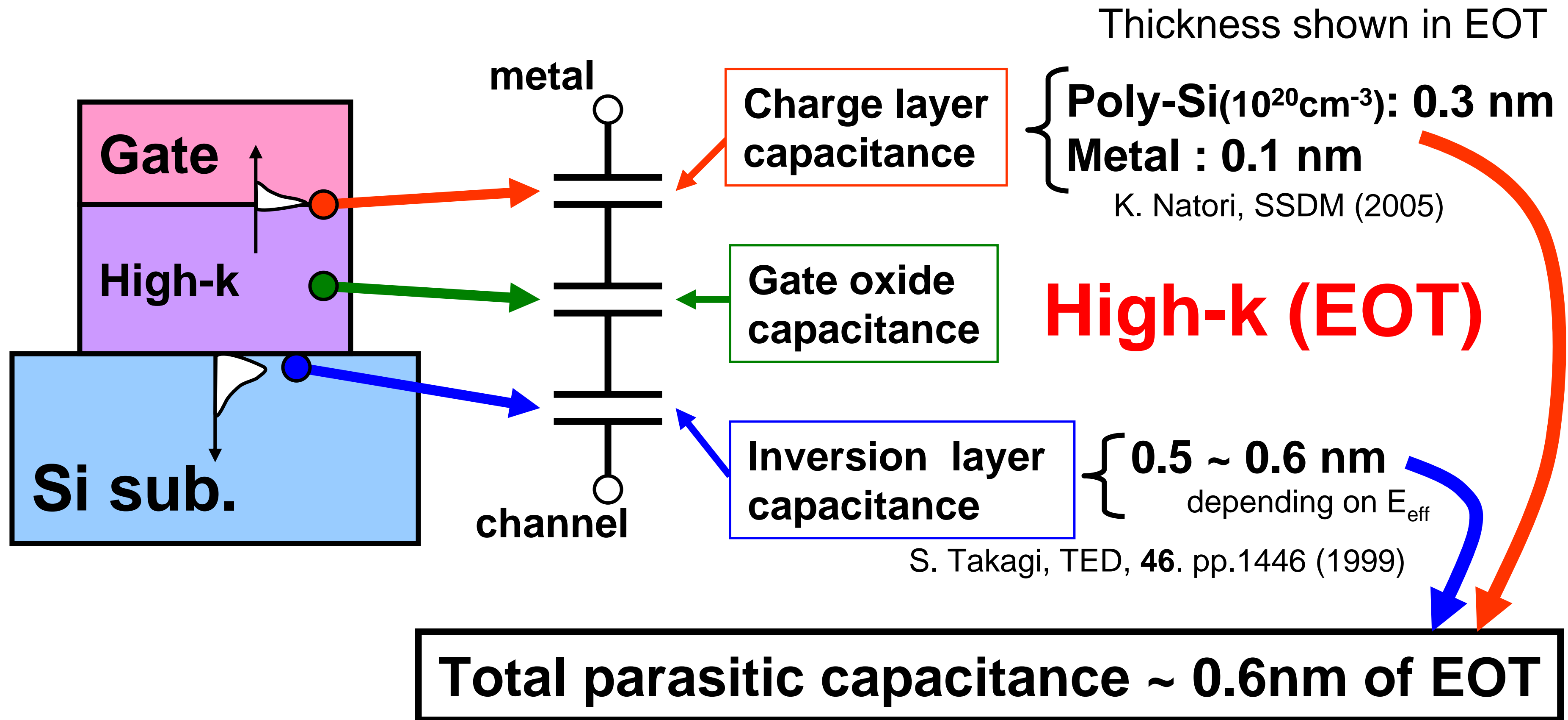
EOT = 0.48 nm

Our results

Transistor with La_2O_3 gate insulator

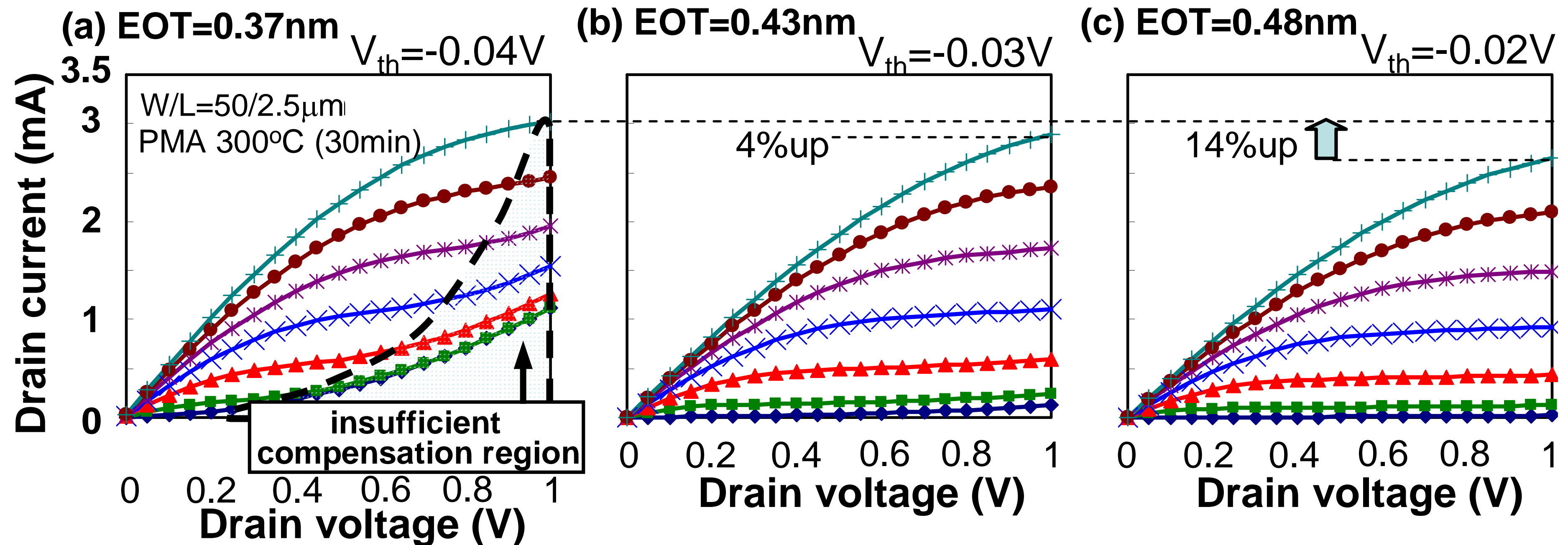


Quantum Effect in Gate Stack

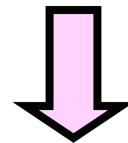


- A question if the performance improvement can be obtained with EOT<0.5nm
- Is EOT<0.5nm achievable?

EOT<0.5nm with Gain in Drive Current



14% of I_d increase is observed even at saturation region

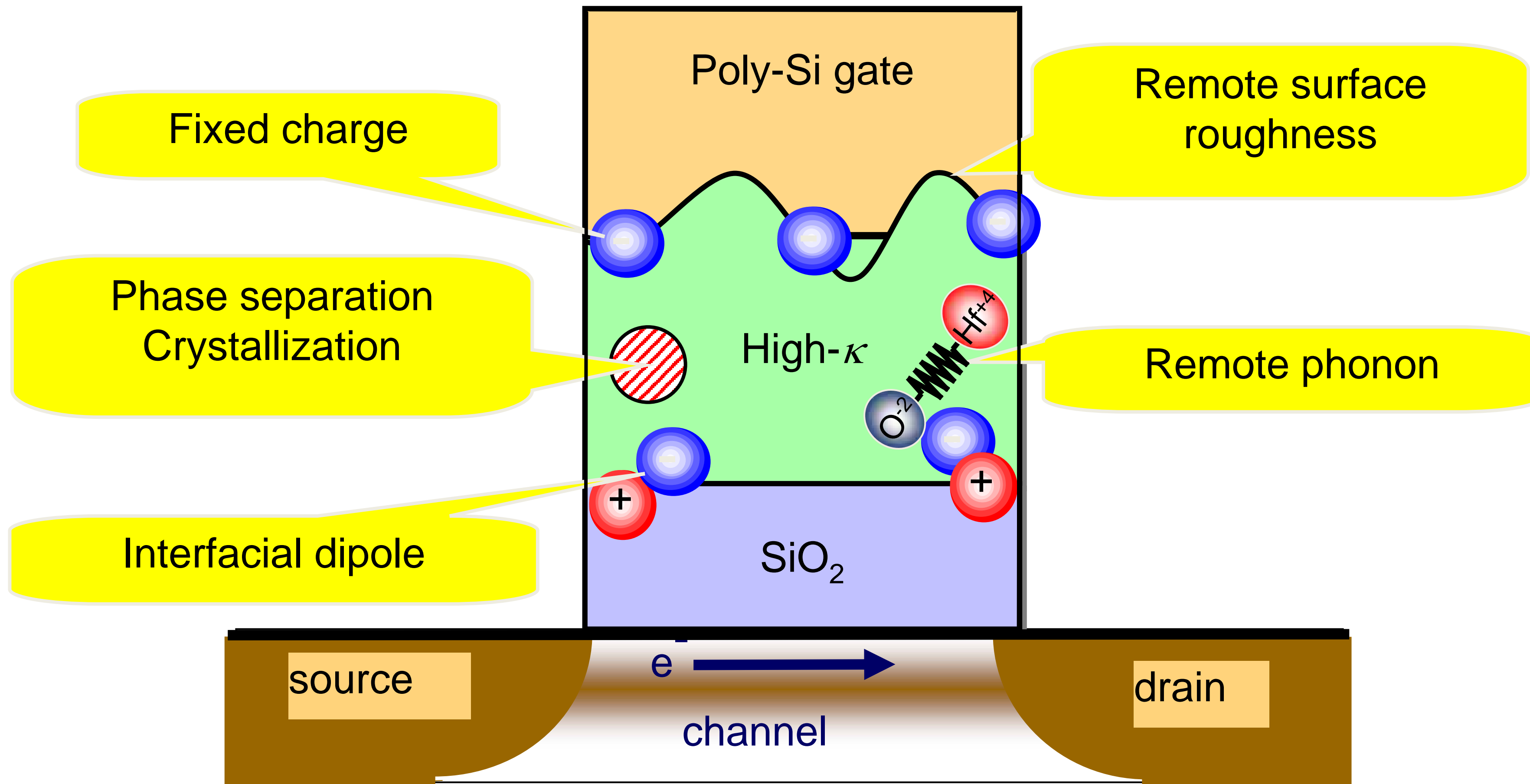


EOT below 0.4nm is still useful for scaling

Mobility concerns

Mobility degradation causes for High-k MOSFETs (HfO_2, Al_2O_3 based oxide)

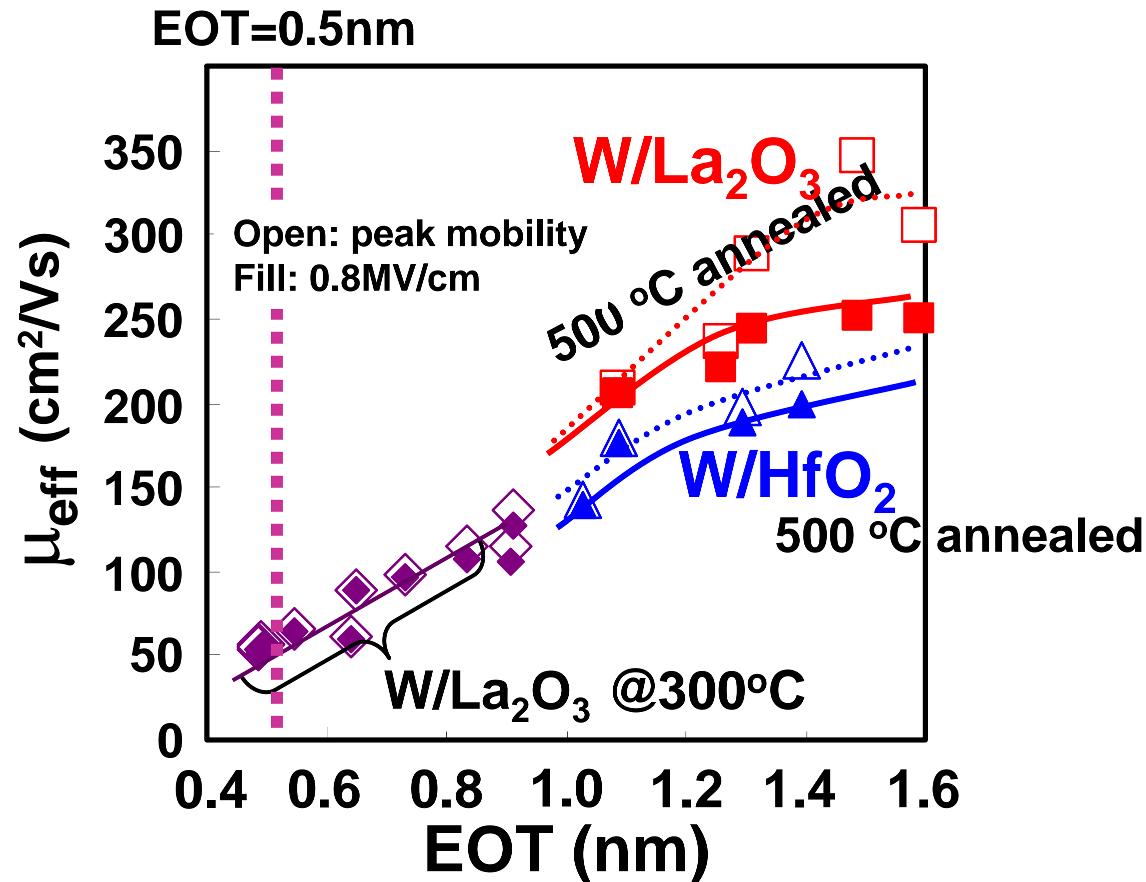
Remote scattering is dominant



S. Saito et al., IEDM 2003,

S. Saito et al., ECS Symp. on ULSI Process Integration

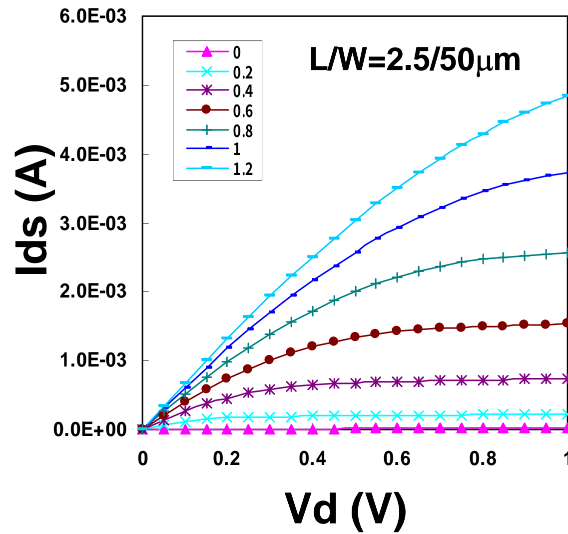
μ_{eff} of W/La_2O_3 and W/HfO_2 nFET on EOT

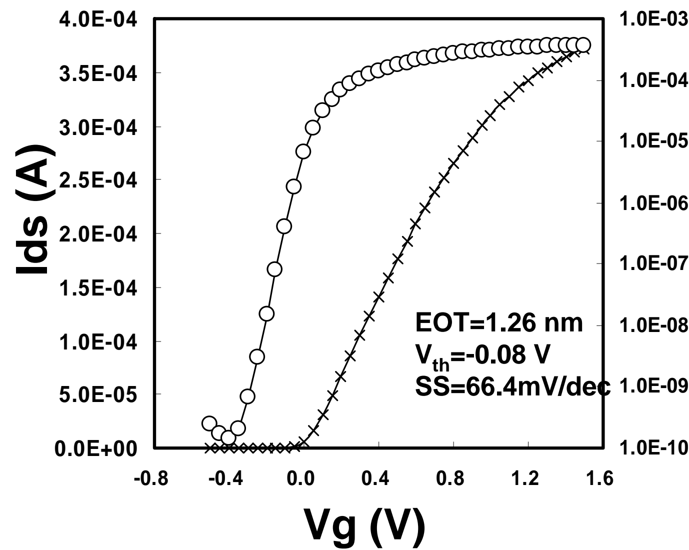


- W/La_2O_3 exhibits higher μ_{eff} than W/HfO_2
- μ_{eff} start degrades below EOT=1.4nm

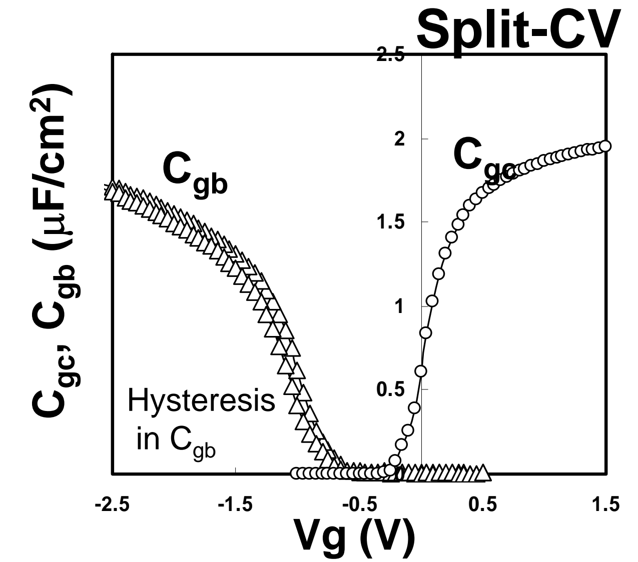
Electrical characteristics of W/La_2O_3 nFET annealed at 500 °C

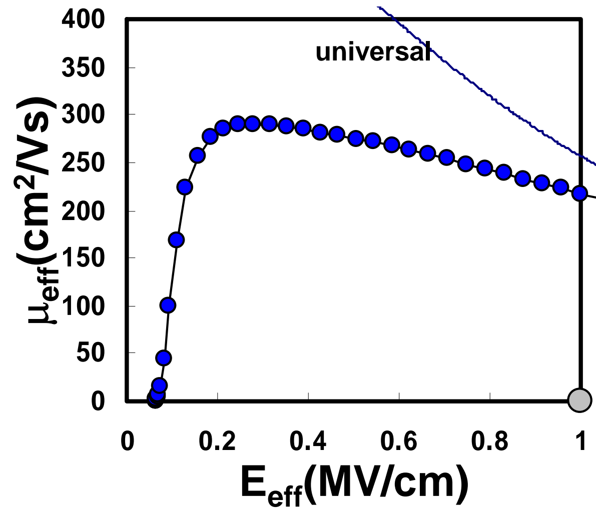
W/La_2O_3/nFET, 500°C anneal





Split-CV

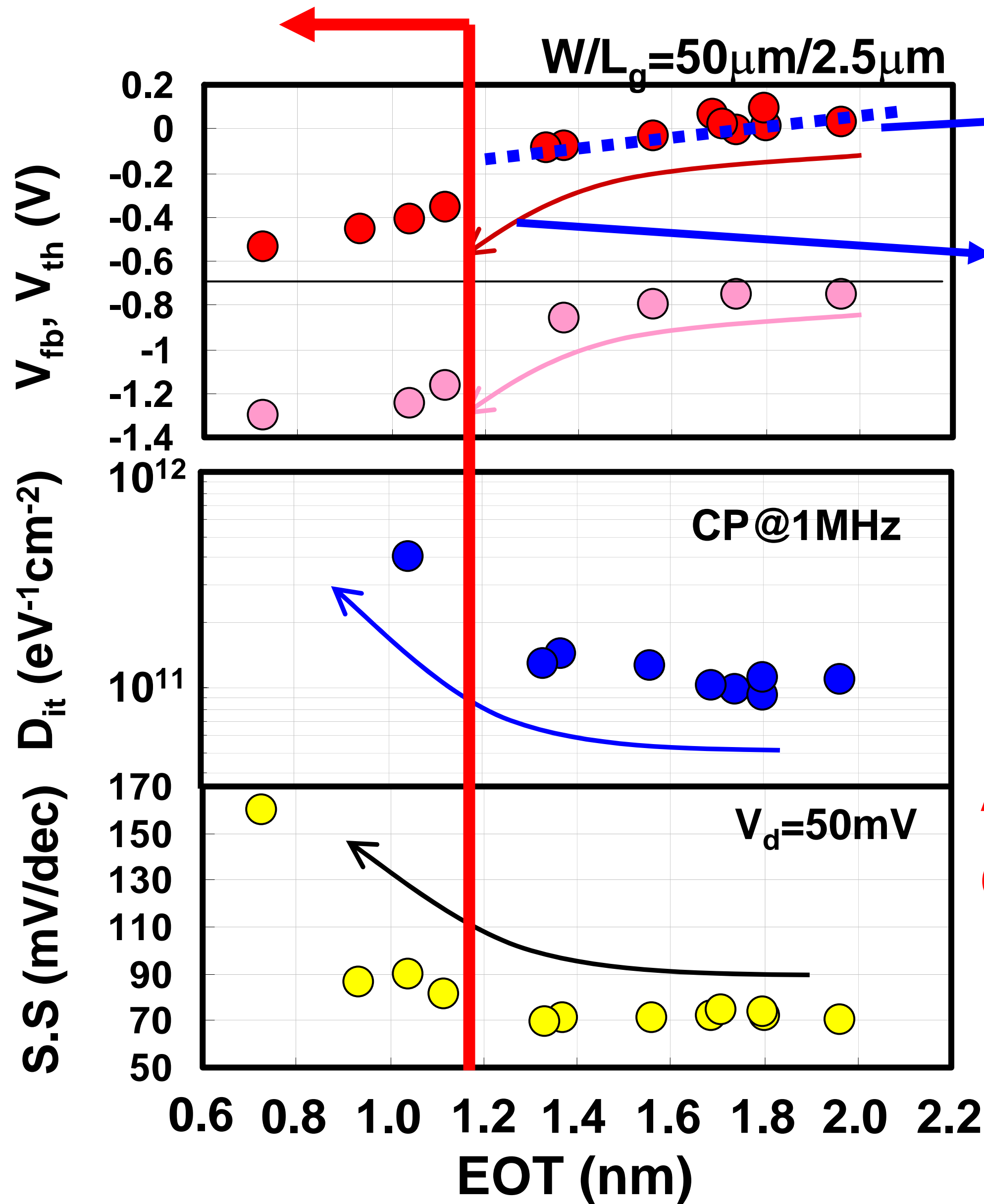




Improvement in electrical characteristics
SS=66mV/dec, μ_{eff}=300cm²/Vs

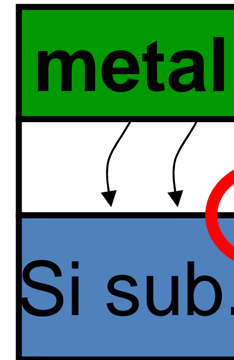
However, EOT grows from 0.5 to 1.3nm!

FET characteristics of W/La_2O_3 on EOT



$N_{fix}=7x10^{12}$ cm^{-2}

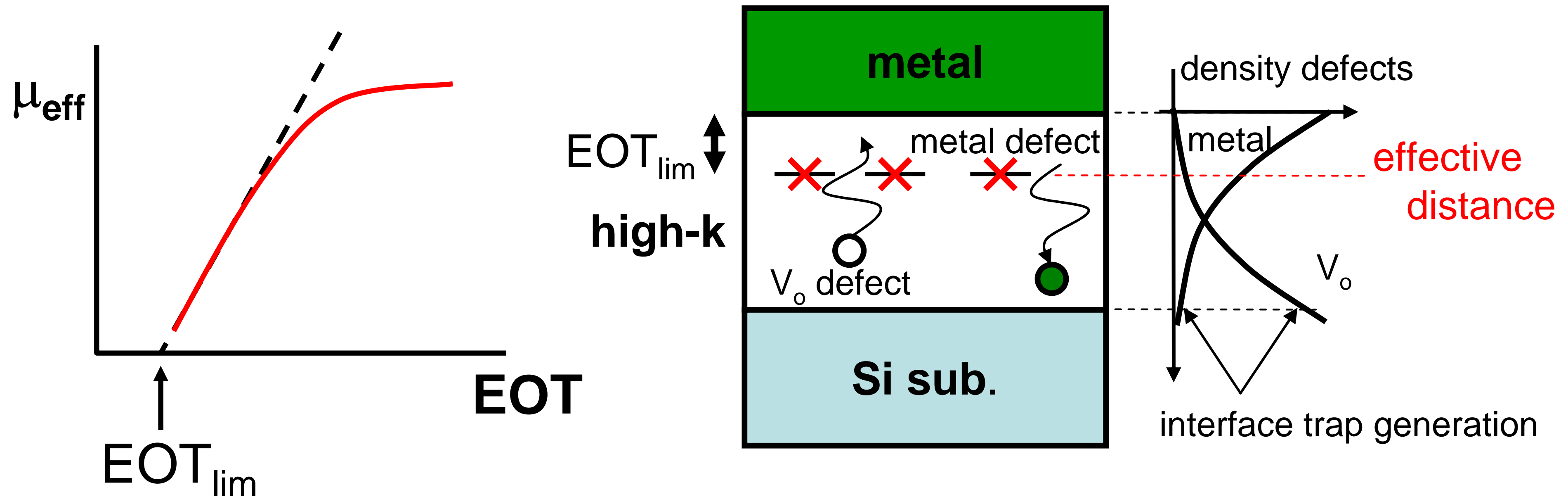
Aggressive N_{fix} generation at EOT<1.2nm



N_{fix} and D_{it}

All characteristics start to degrade or shift below EOT=1.4nm

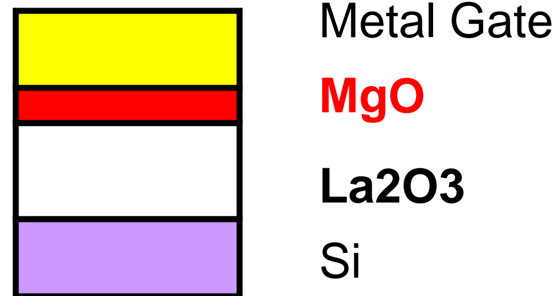
Schematic illustration of μ_{eff} reduction at small EOT

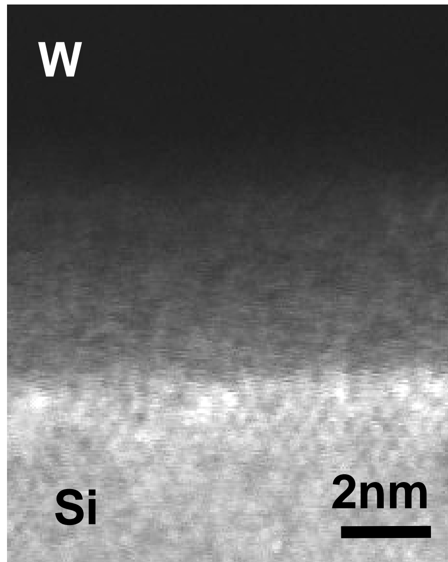


Spatial distribution of metal gate induced defects approaches to high-k/Si interface with small EOT

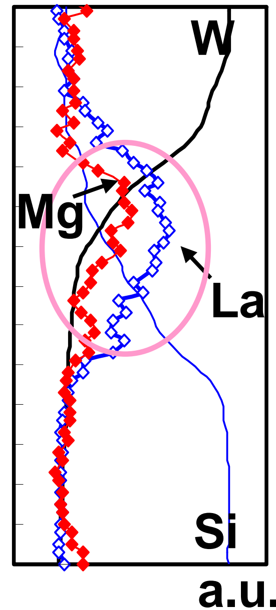
Some of the defects generates interfacial states

Gate Metal Induced Defects Compensation

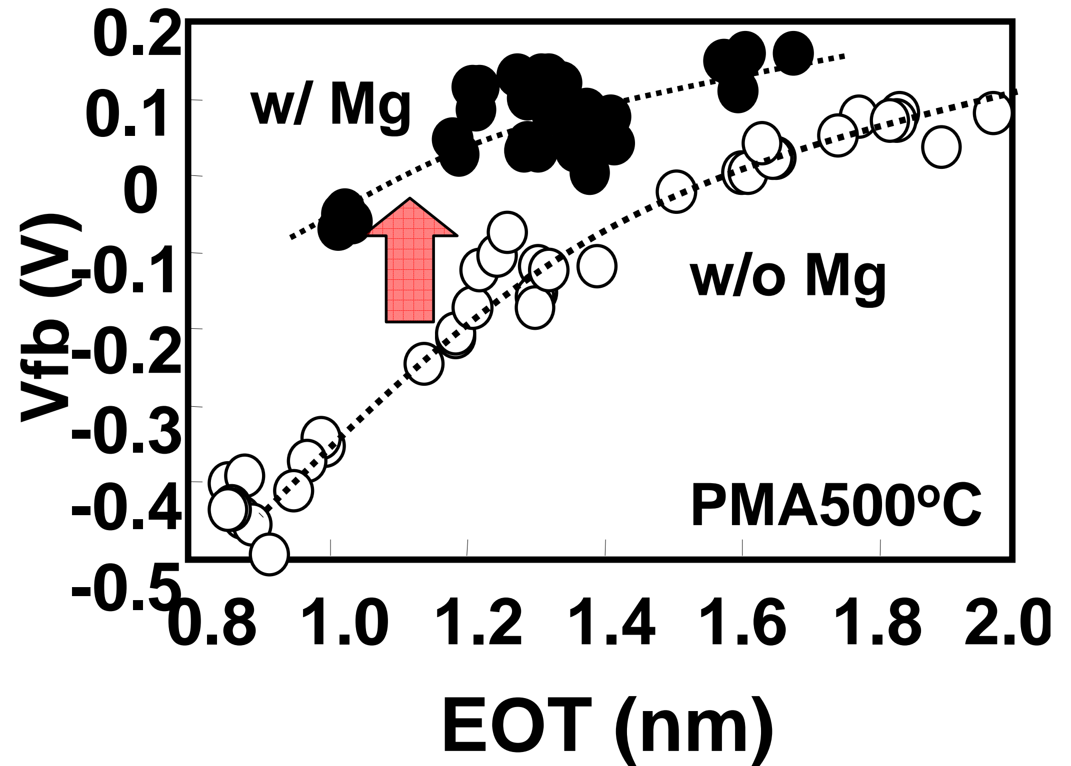




TEM

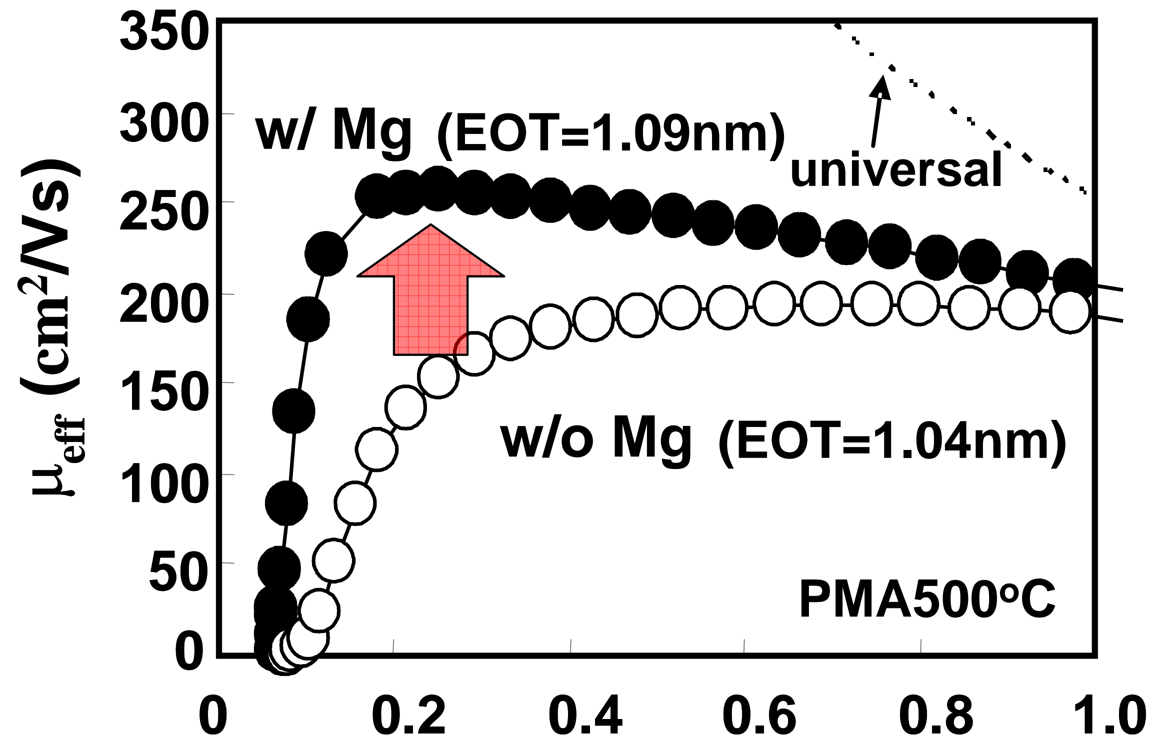


EDX



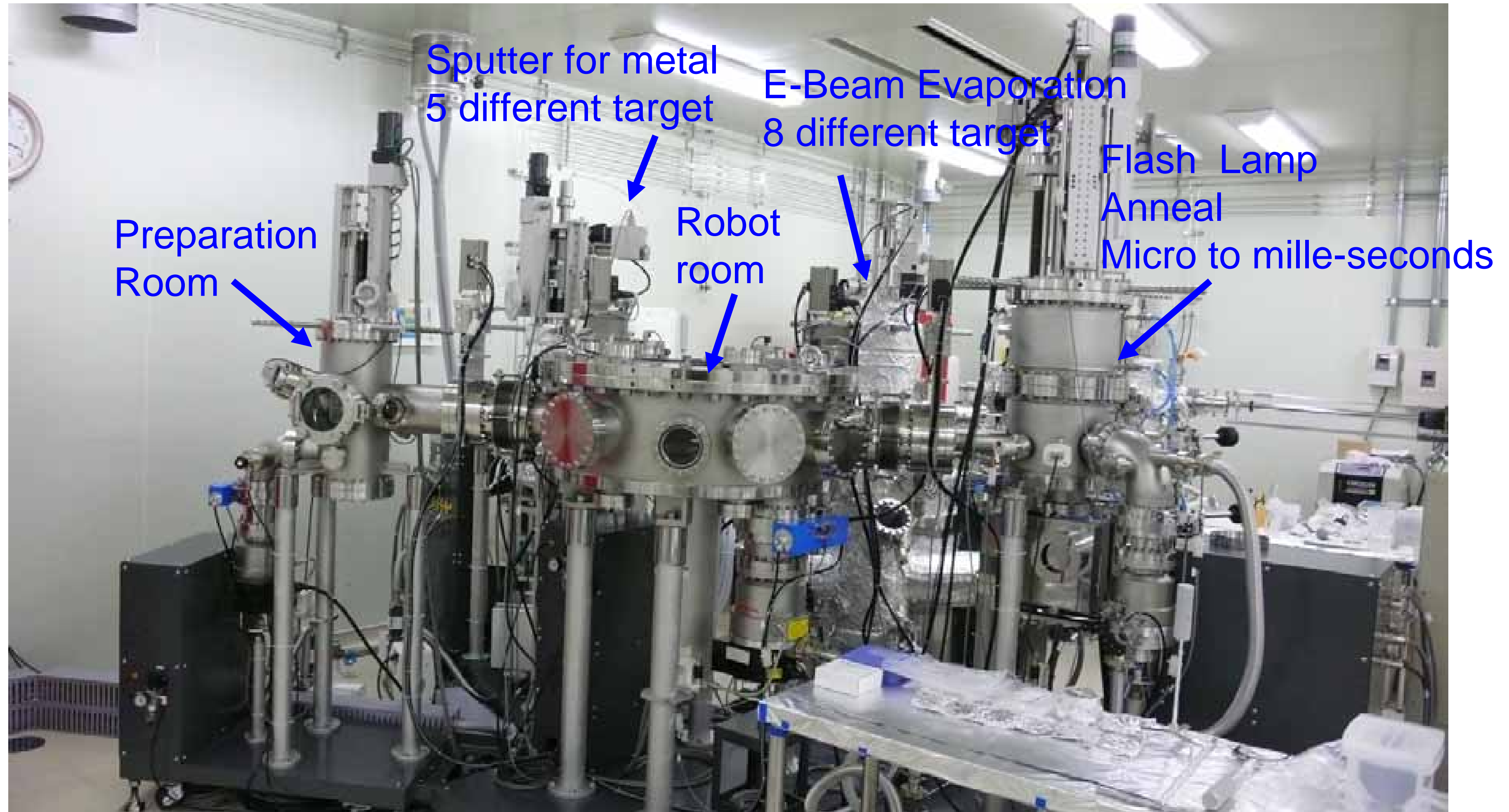
Suppression of aggressive shift in V_{fb}

Mobility Improvement with Mg Incorporation



Recovery of μ_{eff} mainly at low E_{eff}

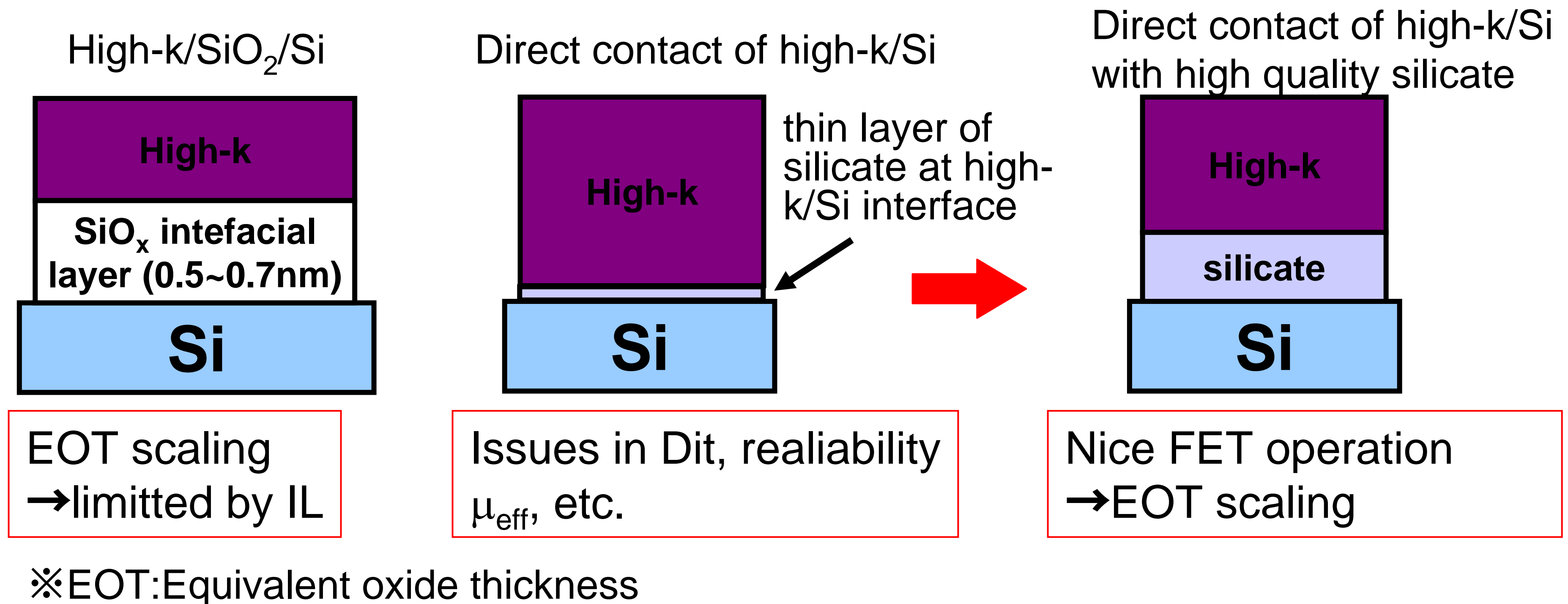
Cluster tool for high-k thin film deposition



Recent/Current Research Items in my group For High-k gate dielectrics

(1) FET operation with EOT<0.5mn
(2) High μ_{eff} with direct contact of La-silicate/Si
(3) Origin of degradations at EOT<1.3nm
(4) Modeling of defects in dielectrics
(5) μ_{eff} recovery with Mg incorporation
(6) Atomic structure of La-silicates
(7) Small EOT with low leakage current
(8) Interface dipole at high-k interface
(9) Defect compensation with Ce-oxide capping

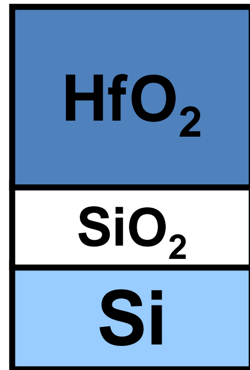
Direct contact of high-k/Si with La-silicate foramtion



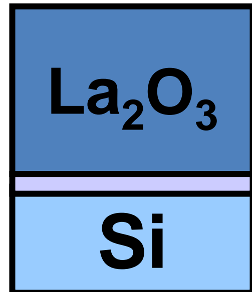
Originality

Foramtion of high-k quality La-silicate using the reaction of La_2O_3 and Si substrate

High quality La-silicate



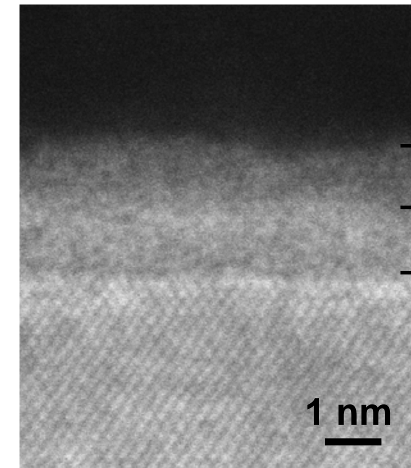
- HfO_2 formes SiO_2 at interface

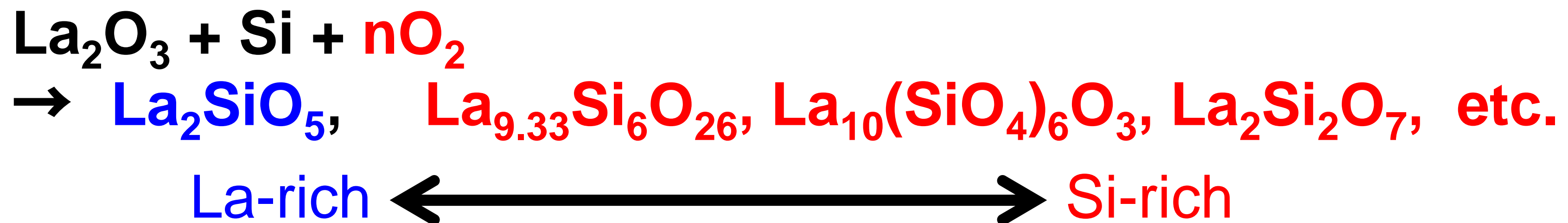


La-rich silicate La_2SiO_5

- μ_{eff} degradation
- defects in silicate (hysteresis)
- large D_{it} ($10^{13}cm^{-2}/eV$)

La_2O_3/Si after 500 °C 30min

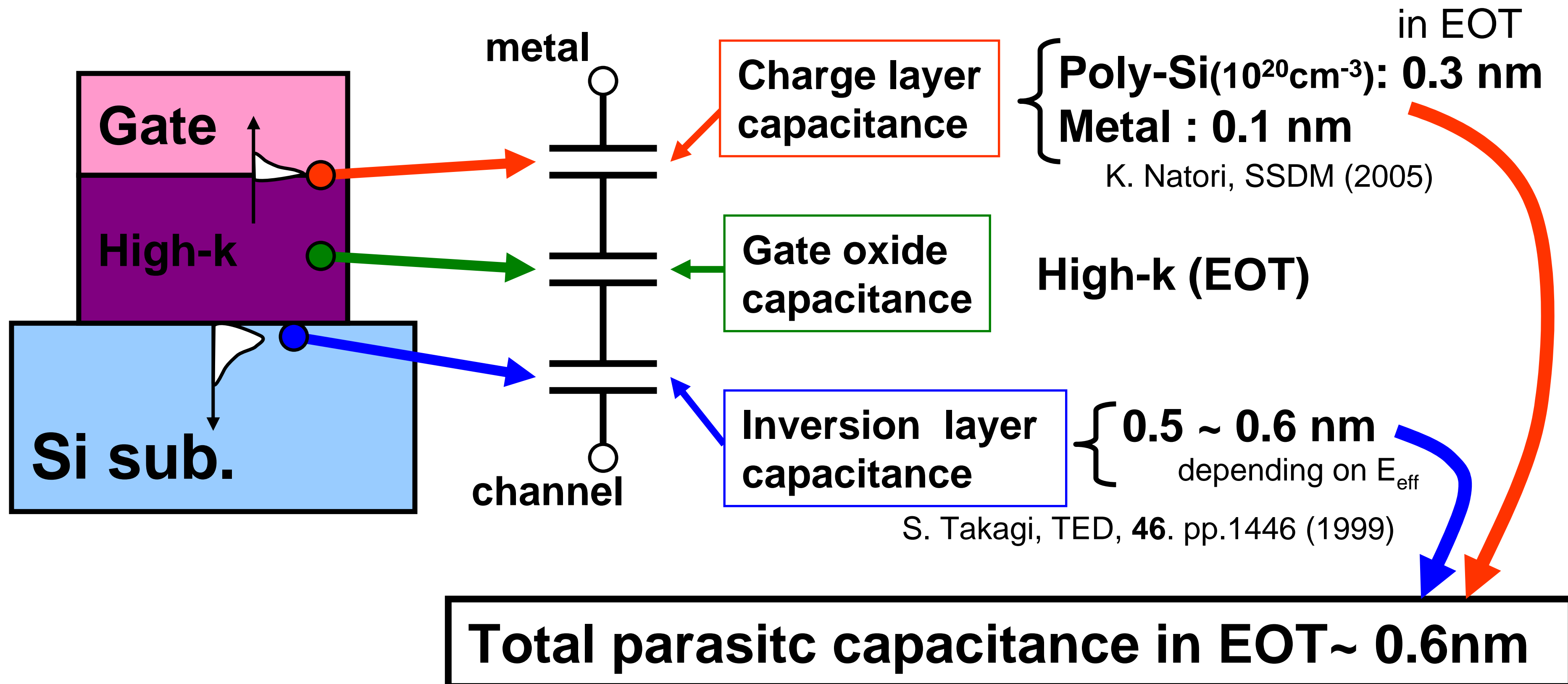




Proper oxygen atom supply to form high quality Si-rich La-silicate

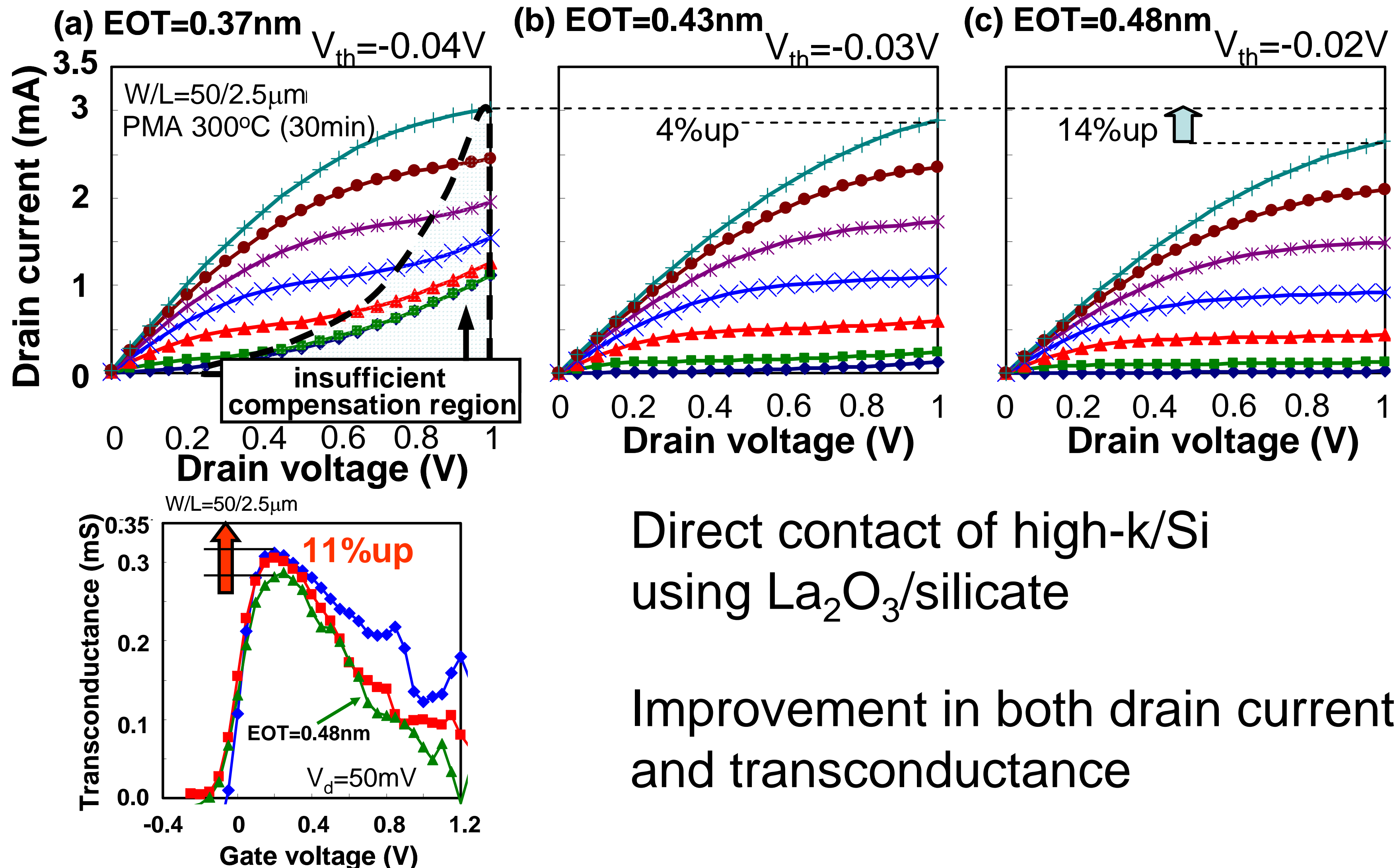
K. Kakushima, et al., ESSDERC '08, Edinburgh

(1) Overwhelming the EOT below 0.5 nm



- Question about device improvement below EOT=0.5nm (written in ITRS roadmap)
- Difficulty in fabrication process to achieve EOT<0.5nm

FET operation of EOT=0.37nm



Direct contact of high-k/Si using La_2O_3/silicate

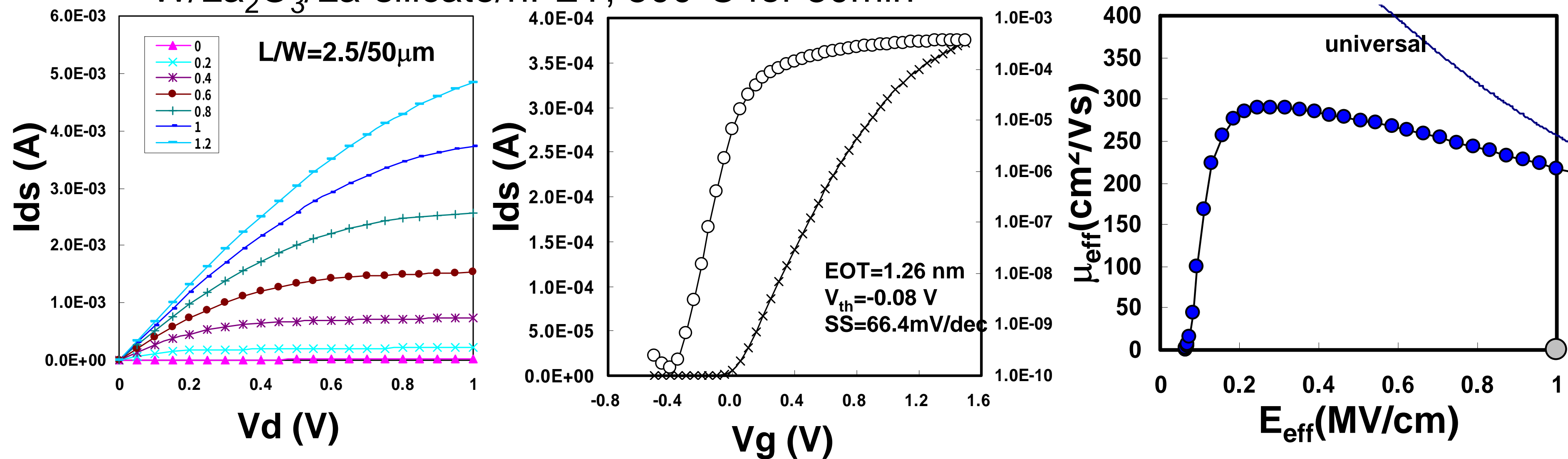
Improvement in both drain current and transconductance

EOT scaling below 0.5nm is still useful

K. Kakushima, et al., Microelectron. Reliab., **50**, 790 (2010)

(2) Direct high-k/Si using La-silicate/Si with high μ_{eff}

EOT=1.26nm



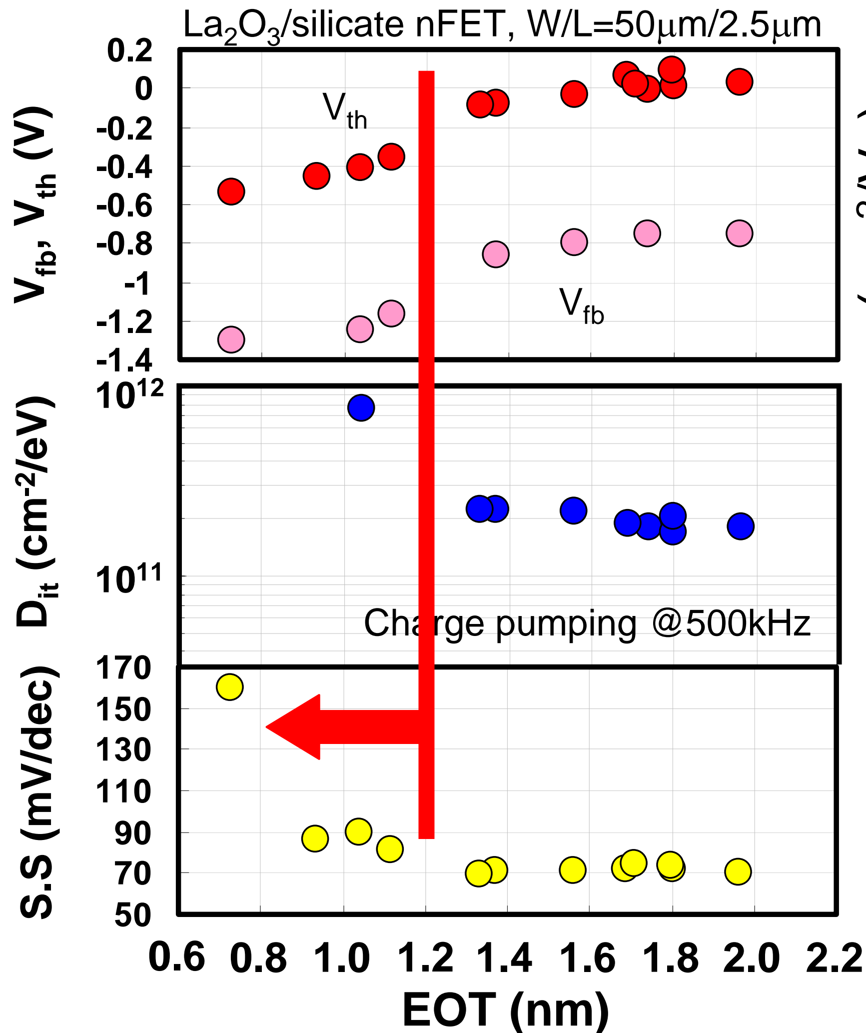
High peak μ_{eff} of 300cm^2/Vs with 500°C annealing

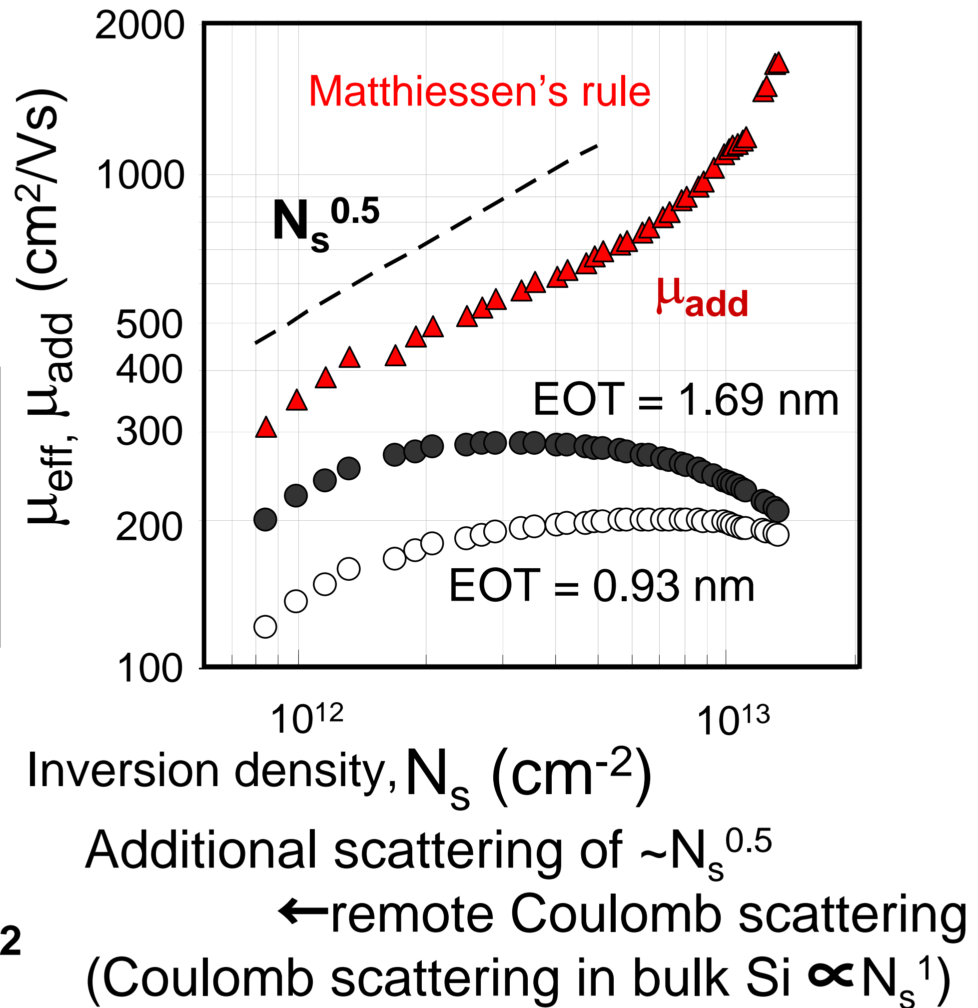
→ nice proerties of Si-rich La-silicate/Si interface

Fairly nice properties can be achieved even with direct high-k/Si interface (EOT~1.2)

K. Kakushima, et al., ESSDERC '08, Edinburgh

(3) Origin of degradations at EOT<1.3nm



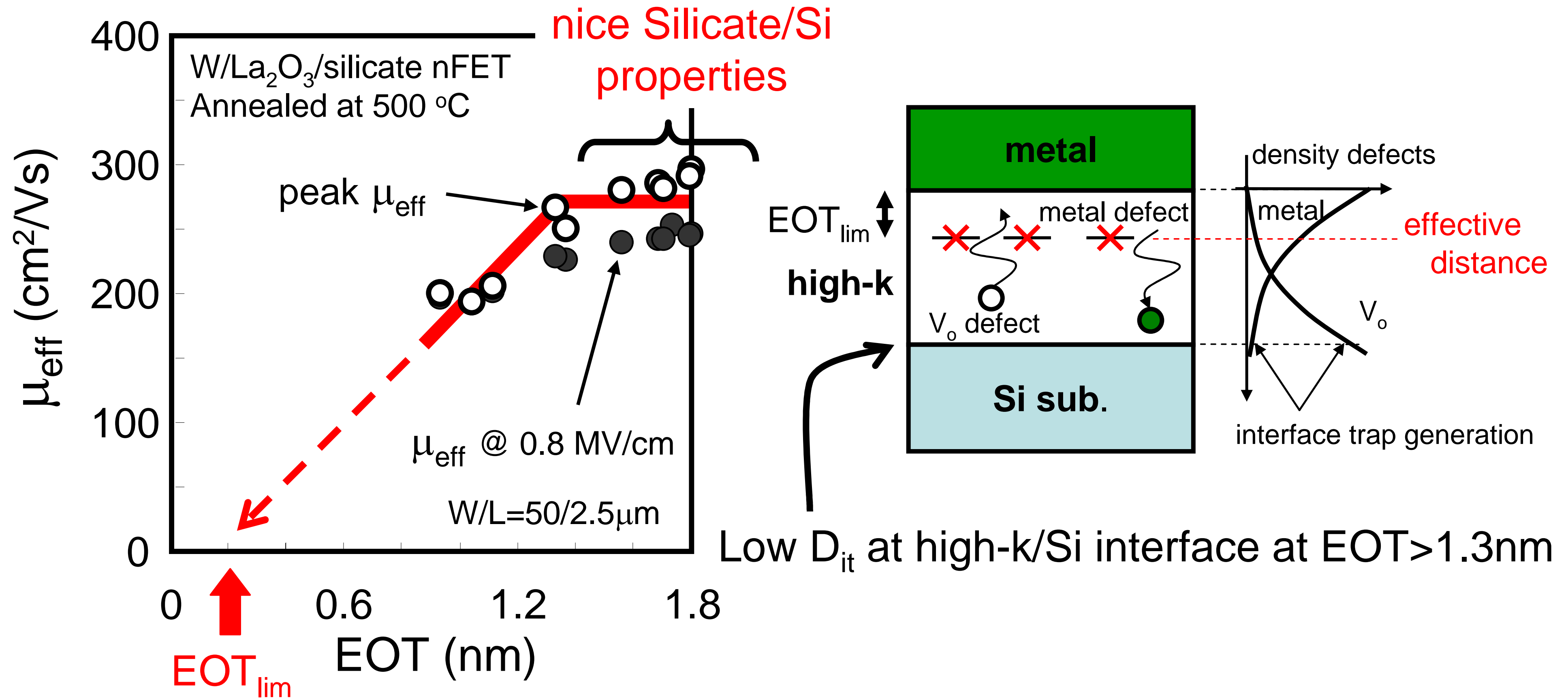


Additional scattering of ~$N_s^{0.5}$
←remote Coulomb scattering
(Coulomb scattering in bulk Si ∝N_s^1)

Coulomb scattering from high-k at EOT<1.3nm

K. Kakushima, et al., Solid-State Electron., **54**, 715 (2010)

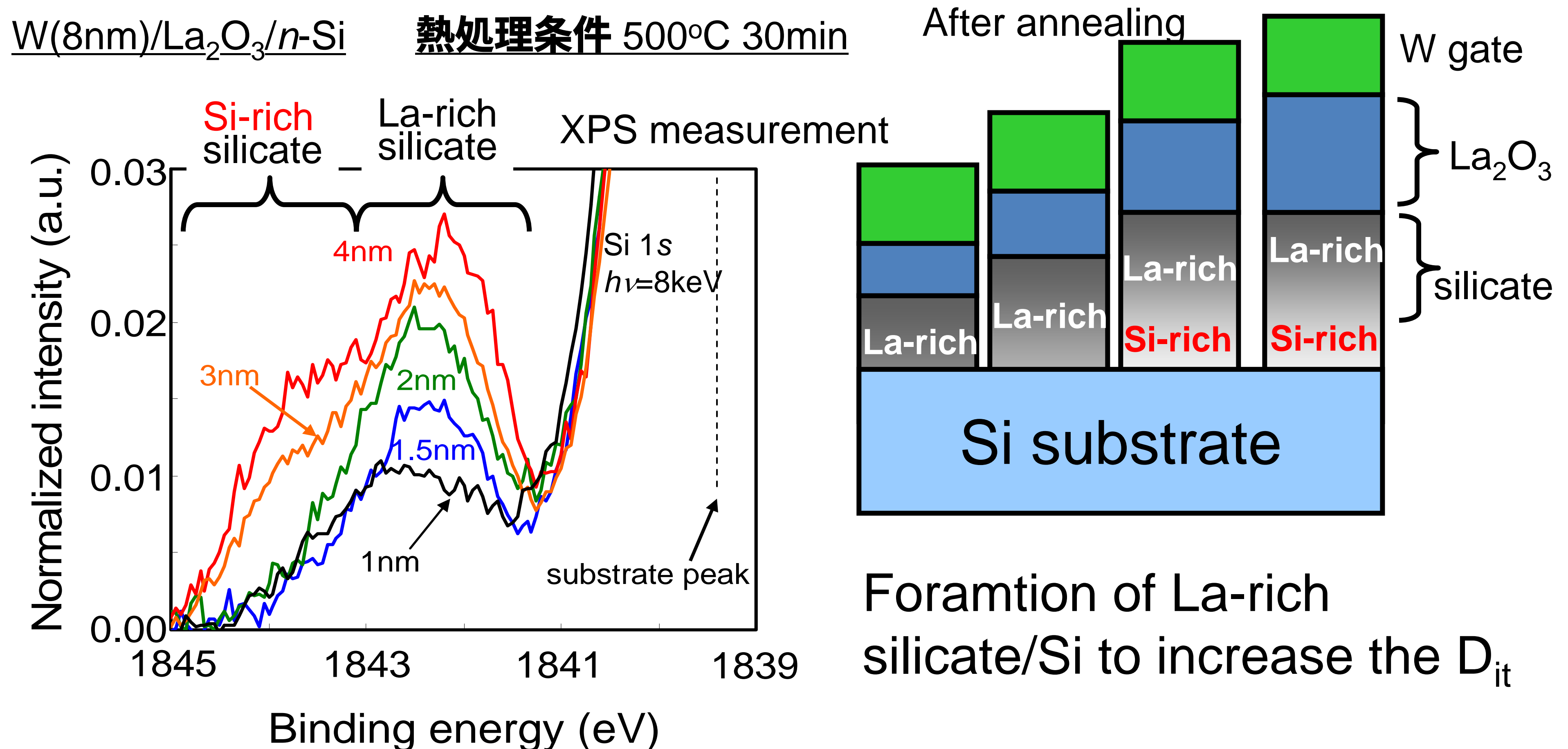
Defects from metal electrode



Metal atom diffusions to degrade the μ_{eff} in EOT<1.3nm

K. Kakushima, et al., Solid-State Electron., **54**, 715 (2010)

(4) Modeling of defects in dielectrics

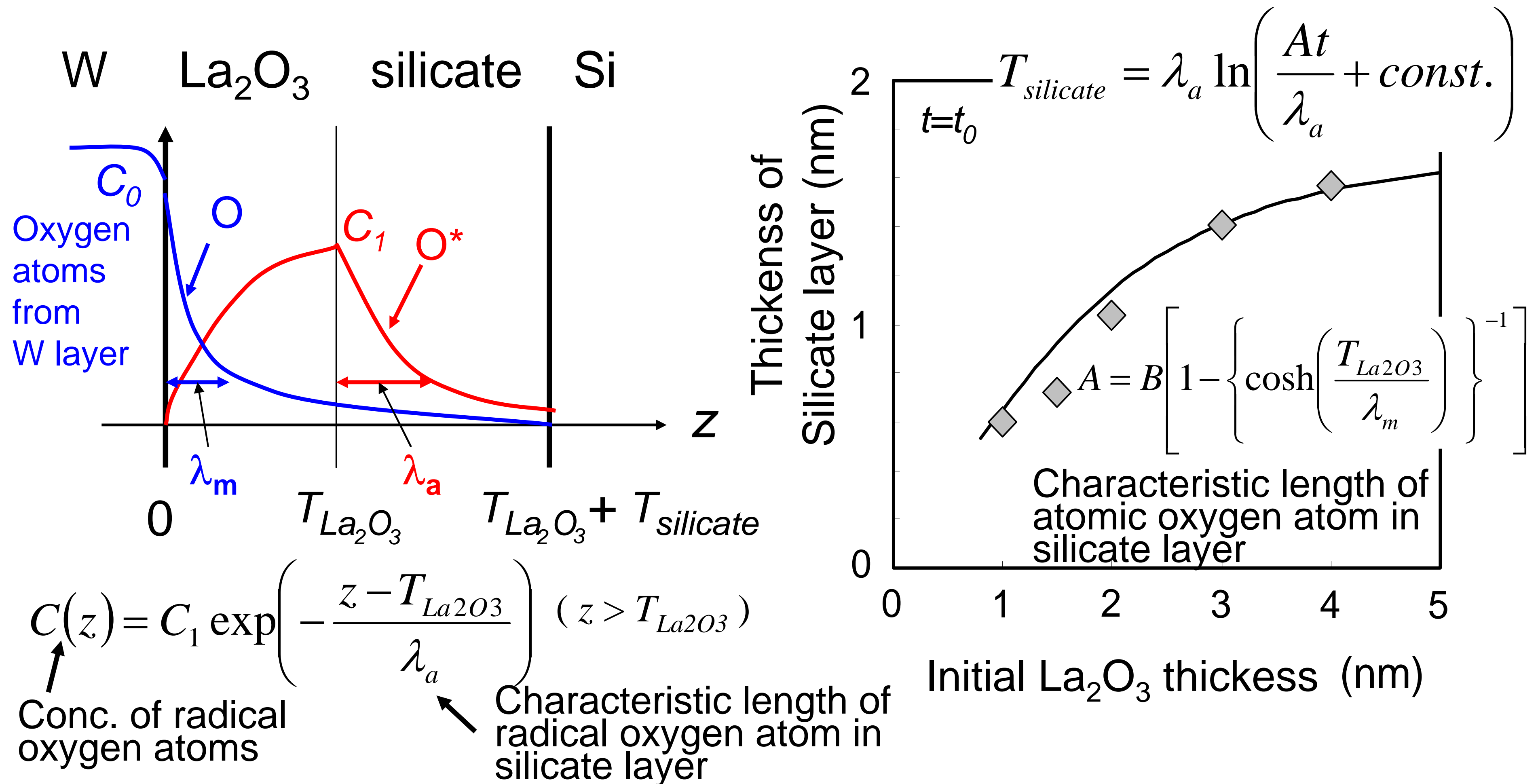


La-rich silicate formation with thin La_2O_3 layer

→one of the reasons for μ_{eff} degradation

K. Kakushima, et al., Solid-State Electron., **54**, 720 (2010)

Thickness dependent silicate formation

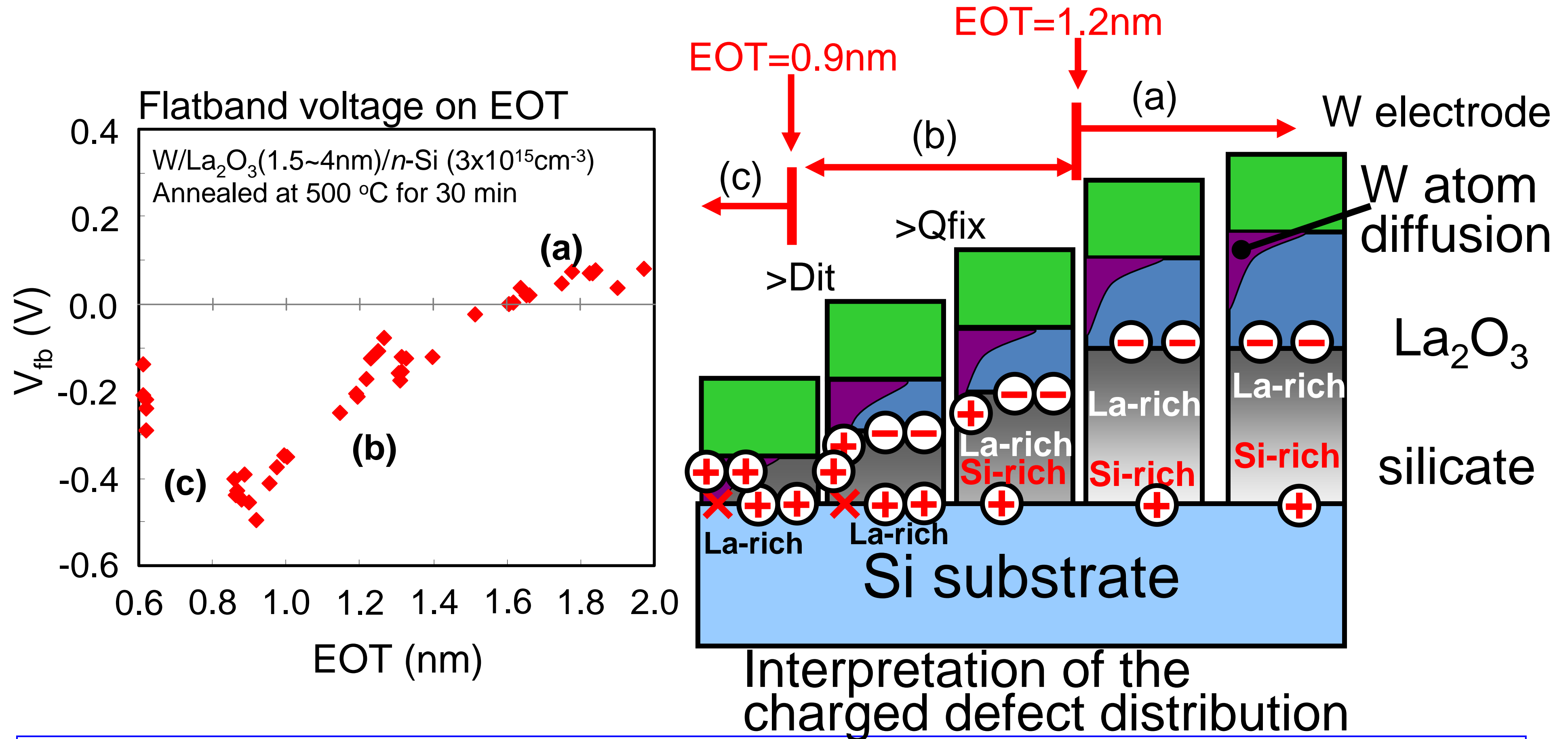


Radical oxygen atoms produced by La_2O_3 determins the thickness of silicate layer

→thin layer of La_2O_3 makes thin La-rich silicate

K. Kakushima, et al., Solid-State Electron., **54**, 720 (2010)

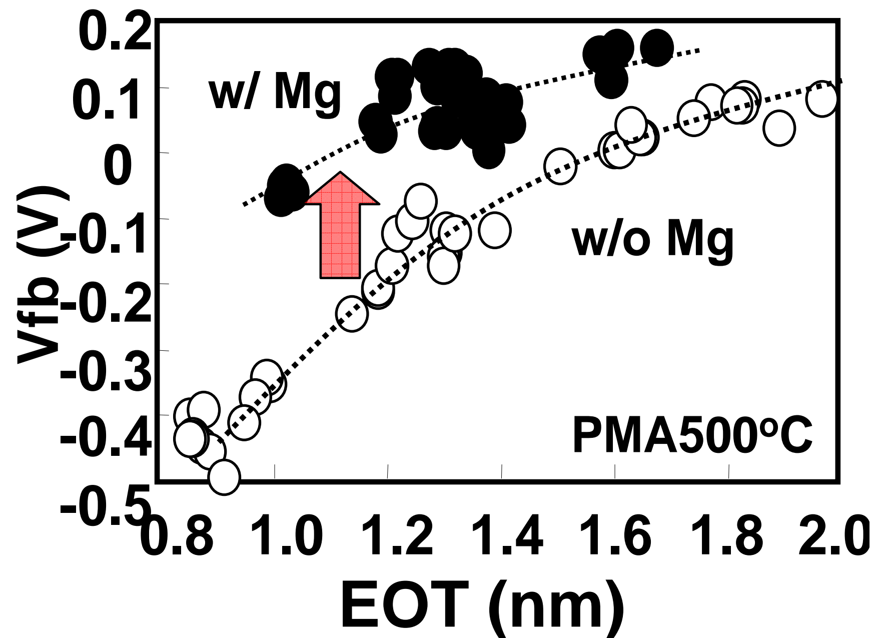
Modeling of the defect distribution in high-k



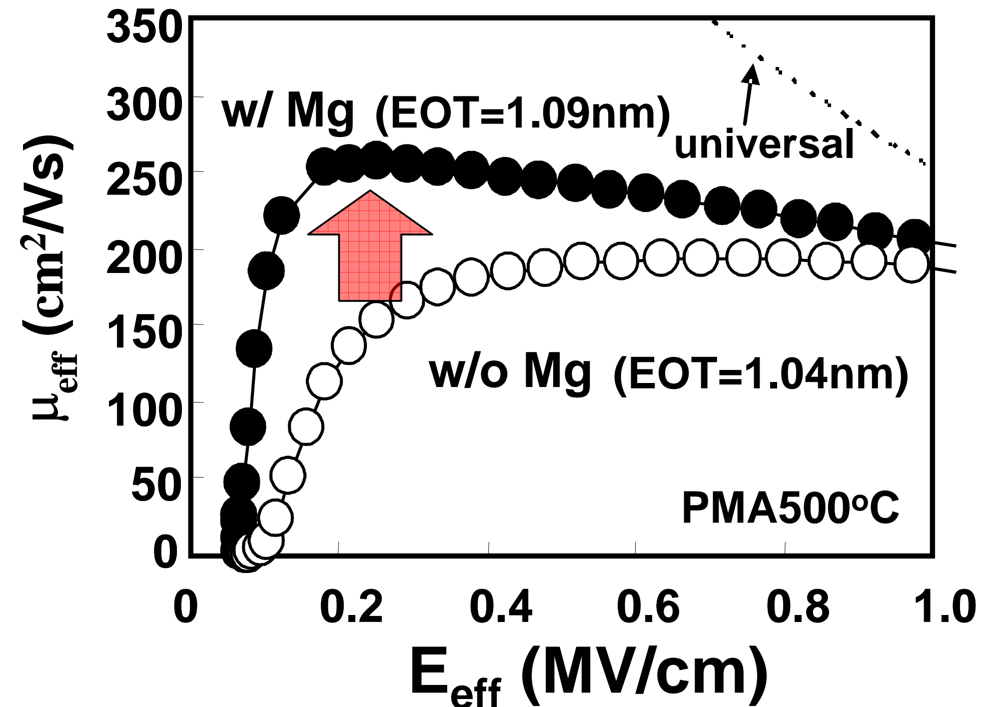
- W atom diffsuion from electrode shift the V_{fb}
- Increase of D_{it} might be due to the diffusion of W atoms reaching to the high-k/Si interface and/or La-rich silicate formation

(5) μ_{eff} recovery with Mg incorporation

Mg incorporation into La-silicate



Suppression of V_{fb} shift at small EOT



μ_{eff} recovery

Incorprotation of Mg into La-silicate can recover the μ_{eff}

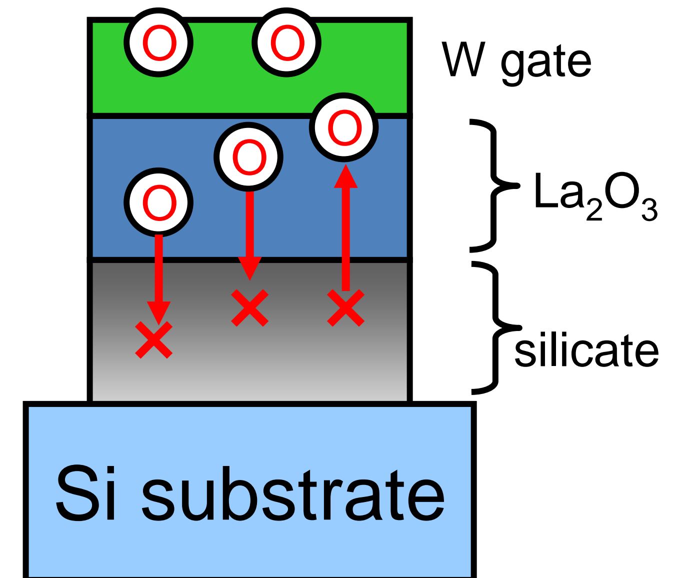
T. Koyanagi, K. Tachi, K. Okamoto, K. Kakushima, et al, Jpn. J. Appl. Phys., **48**, 05DC02 (2009)

Alkali earth incorporation into La-silicate中

Compound	Ionic conductivity (mS/cm) @500°C
$La_{9.33}Si_6O_{26}$	0.023
$La_{10}Si_6O_{27}$	4.3
$La_{10}Mg_{0.2}Si_{5.8}O_{26.8}$	14
$La_{9.8}Mg_{0.3}Si_{5.7}O_{26.4}$	12

⇩ High La conc.

ref: H. Yoshioka et al., SSI **179**, 2165 (2008)



Oxygen ion conductivity
high→ easy Vo formation, easy to recover
low→difficult to form Vo, difficult to recover

High ionic conductivity with Mg incorporation

→ Compensation of defects from W electrode

T. Koyanagi, K. Okamoto, K. Kakushima, et al., ECS Trans., **25**, 17 (2009)

(6) Atomic structure of La-silicates

Purpose

Investigation of the atomic structure of La-silicate

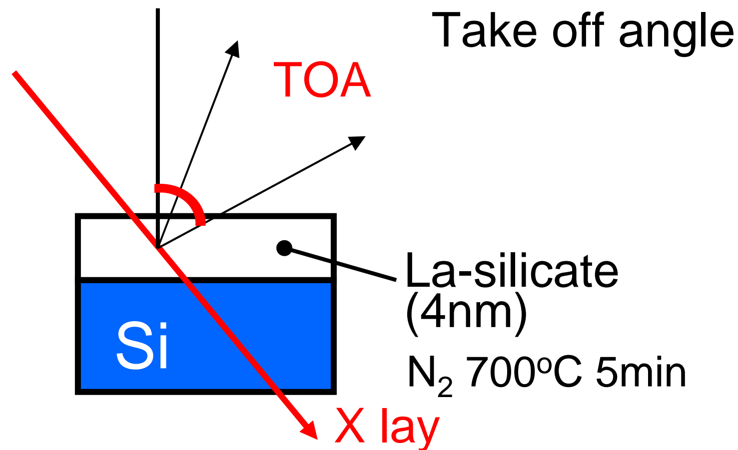
La-silicate for gate dielectric (<4nm)

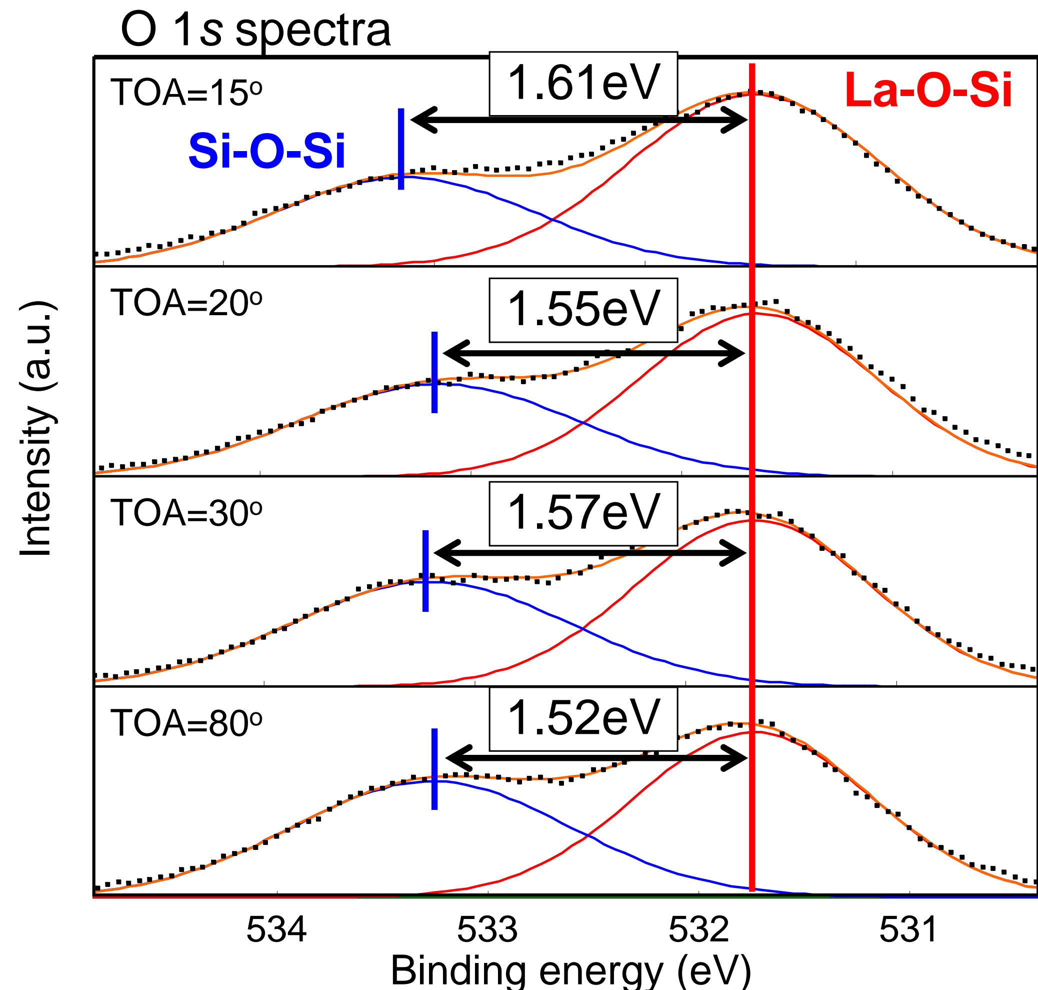
Compositional gradient normal to the surface

Method

Angle-resolved XPS measurment

O 1*s* spectra of La-silicate on different TOA





Binding energy of Si-O-Si and La-O-Si differes on the TOA

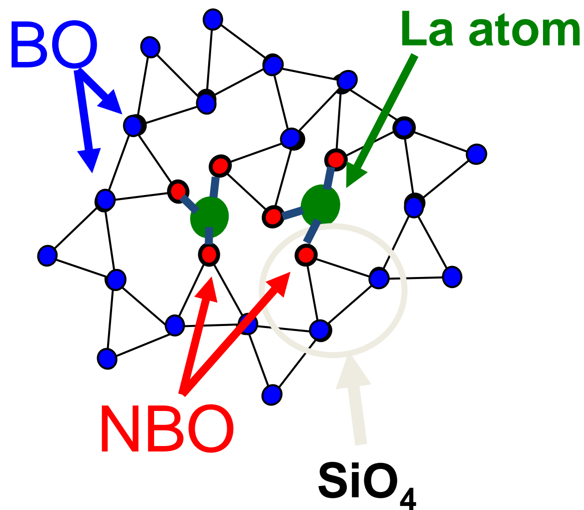
Difference in the binding energy of La-O-Si and Si-O-Si should be constant

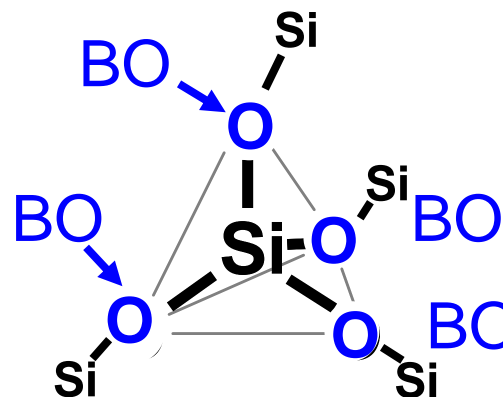
→ Lack of physics based interpretation

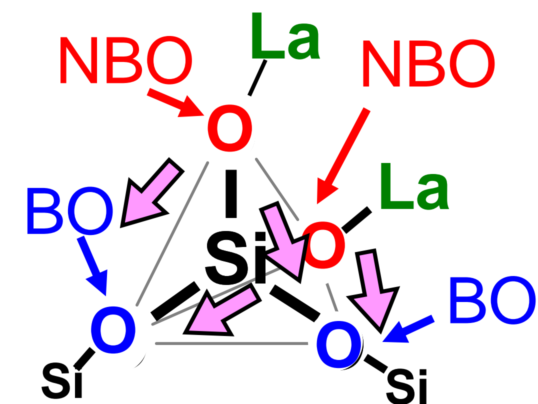
Atomic structure of La-silicate

Network of tetrahedrons (SiO_4)
amorphous

Si-O-Si bonding
BO: bridging oxygen atom
La-O-Si bonding
NBO:non-bridging oxygen atom







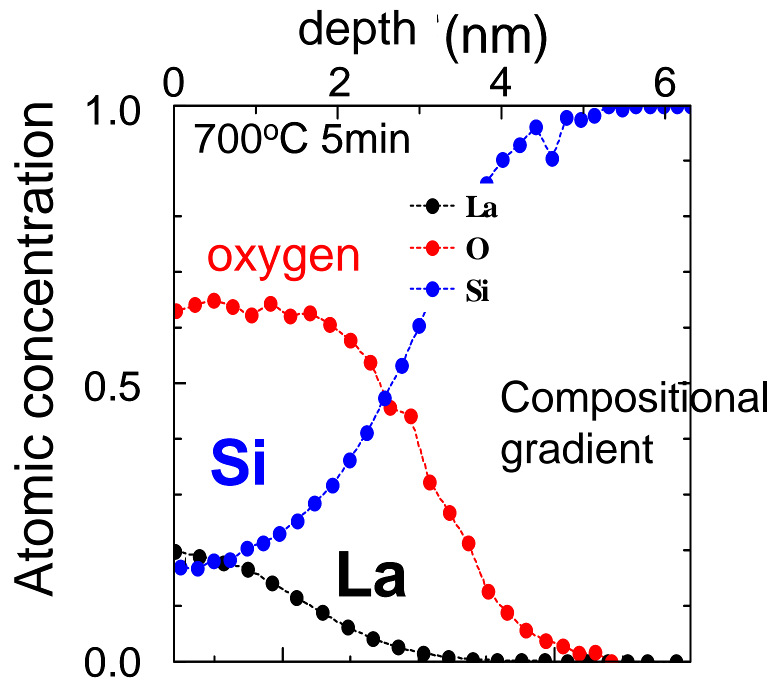
The influence of second neighbor atom should be accounted

La atom concentration dependent binding energy shift

※A common method for Na-dope glass

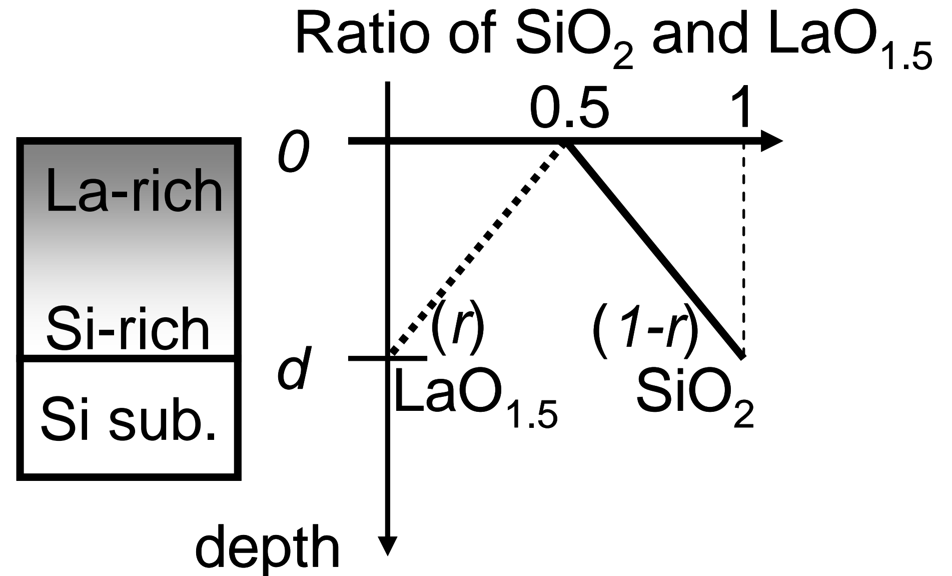
La atom distribution in La-silicate

Atomic distribution determined by RBS



Surface is $La_{0.2}Si_{0.16}O_{0.64}$

K. Kimura, et al, Proc. IWNC, pp. 89 (2005)

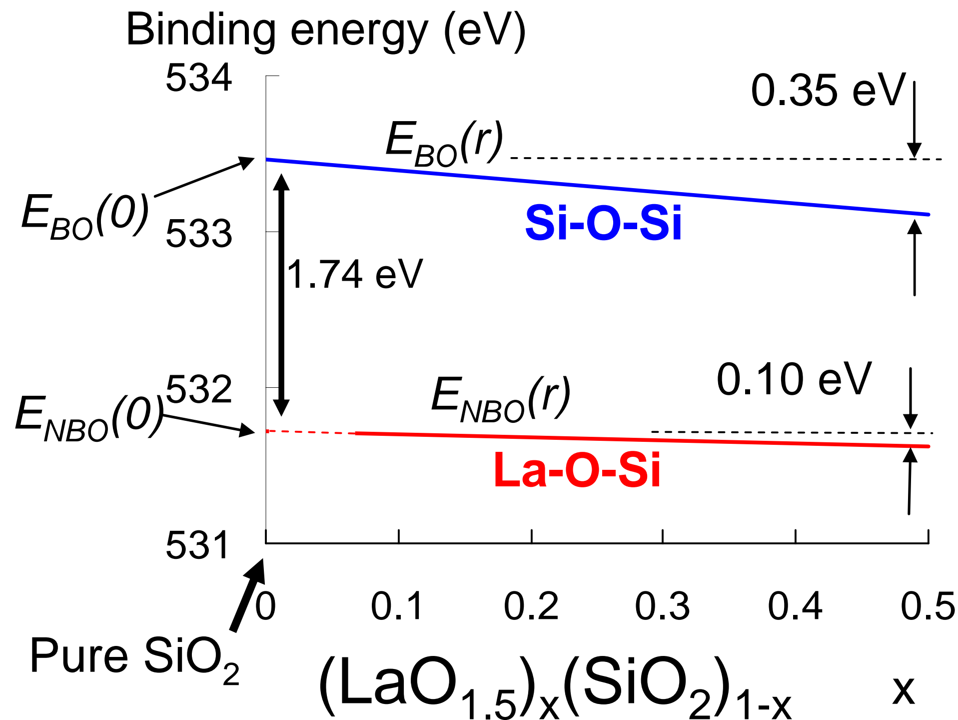


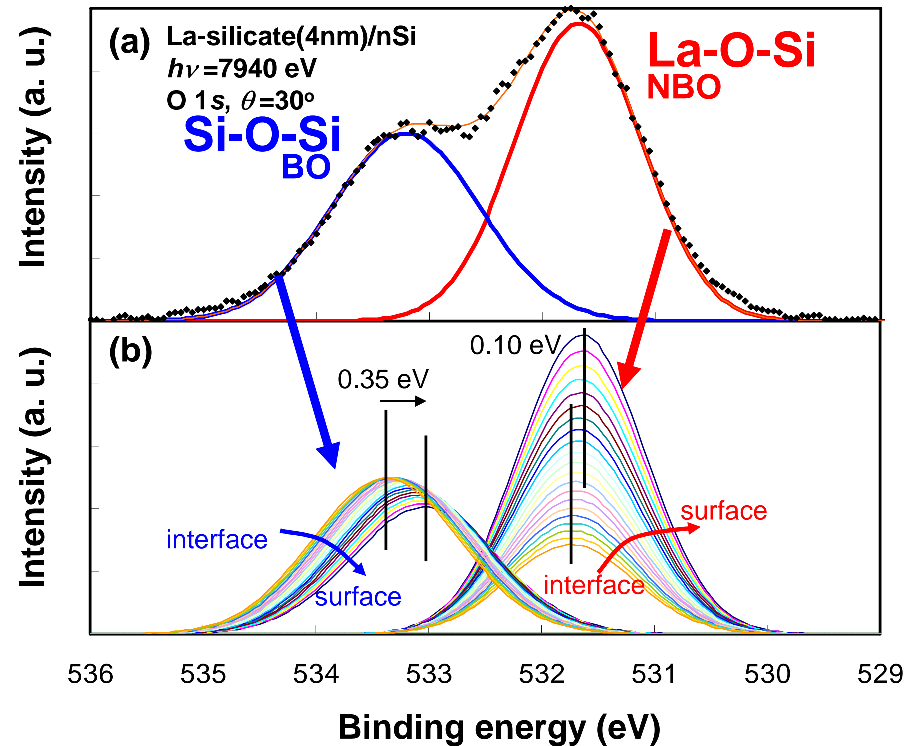
A simple model for the distribution used in this study

Extraction of concentration dependent binding energy shift

Concentration dependent binding energy shift

BO: bridging oxygen atom
NBO:non-bridging oxygen atom





Reconstruction of the obtained O 1*s* spectrum

K. Kakushima, et al., J. Appl. Phys., **104**, 104908 (2009)

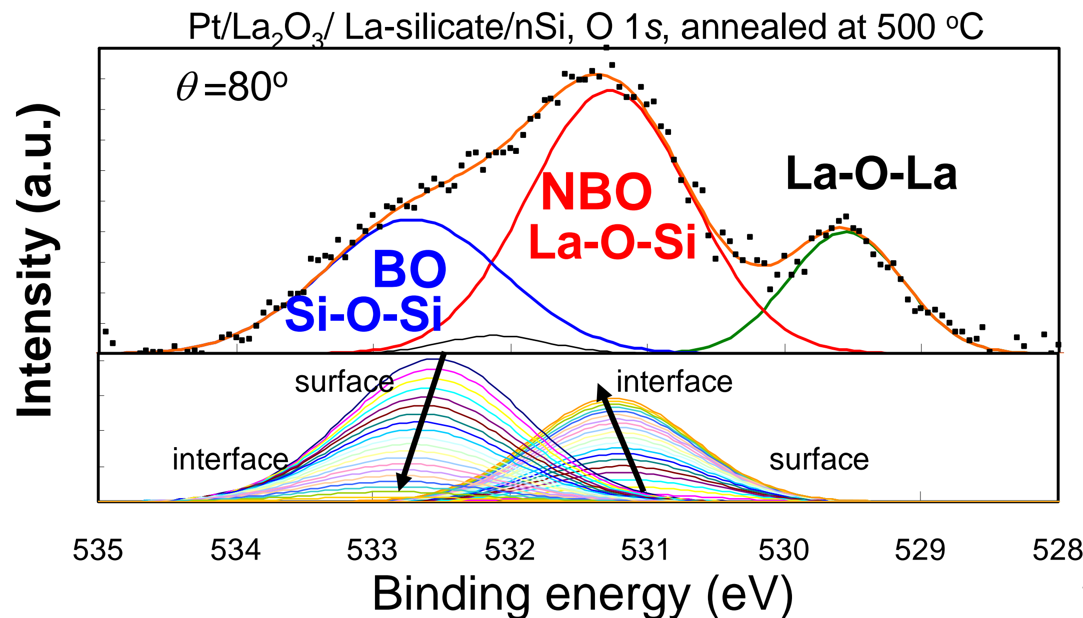
Summary of the deconvolution

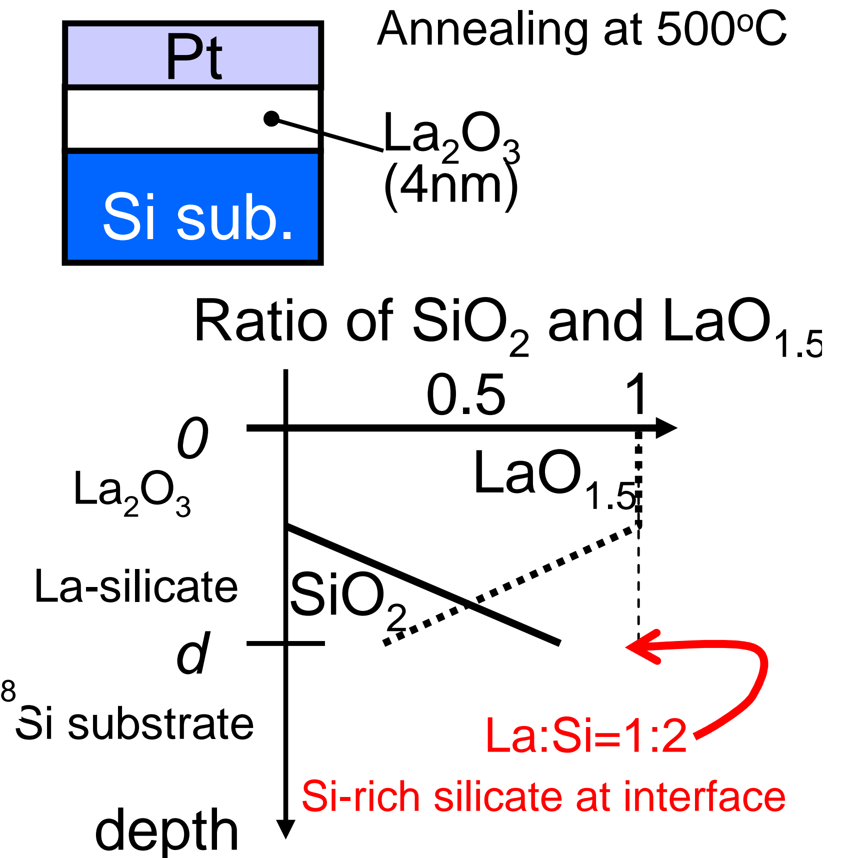
	Binding energy of O 1*s*, eV (FWHM, eV)	Take-off angle (degree)				
		15	20	30	52	80
Conventional fitting	NBO 1*s*	531.49 (1.57)	531.63 (1.57)	531.71 (1.48)	531.76 (1.57)	531.75 (1.53)
	BO 1*s*	533.10 (1.46)	533.18 (1.41)	533.28 (1.41)	533.26 (1.34)	533.27 (1.29)
	$\Delta E_{BO\text{-}NBO}$	**1.61**	**1.55**	**1.57**	**1.50**	**1.52**
This work	NBO 1*s* at $r=0$, $E_{NBO}(0)$	531.42 (1.32)	531.60 (1.32)	531.64 (1.32)	531.72 (1.32)	531.70 (1.32)
	BO 1*s* at $r=0$, $E_{BO}(0)$	533.17 (1.53)	533.33 (1.53)	533.38 (1.53)	533.46 (1.53)	533.45 (1.60)
	$\Delta[E_{BO}(0)-E_{NBO}(0)]$	**1.75**	**1.73**	**1.74**	**1.74**	**1.75**

A constant binding energy difference between BO and NBO

→Physical meaning

Extraction of La concentration from a spectrum

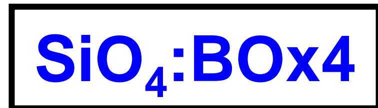


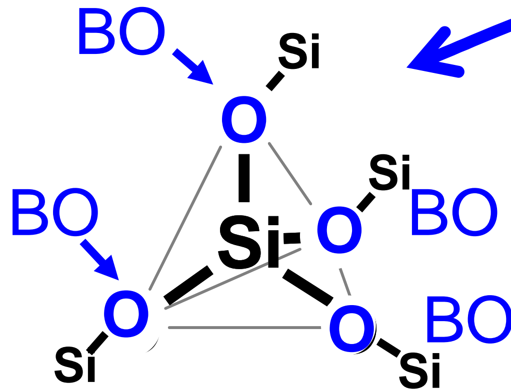


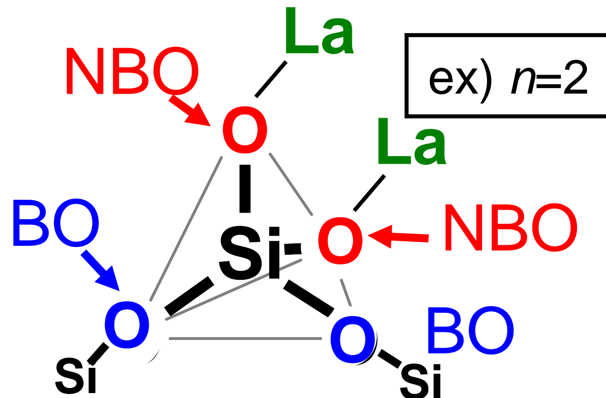
La atom distribution can be detected from one O 1*s* spectrum

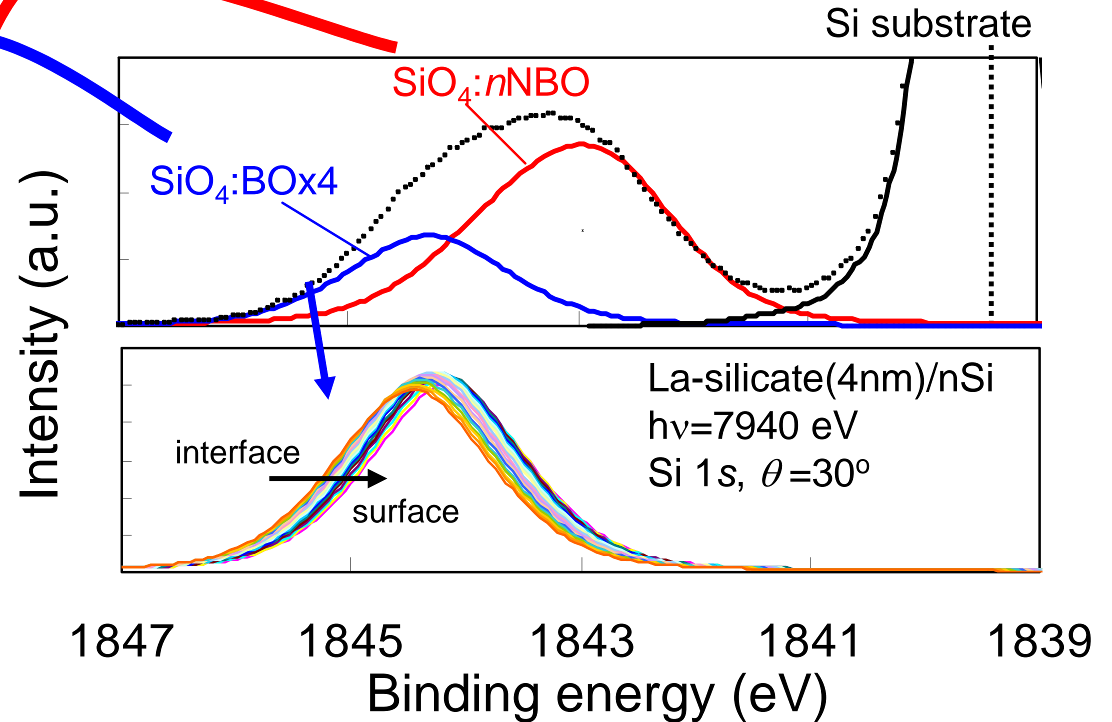
K. Kakushima, et al., J. Appl. Phys., **104**, 104908 (2009)

Analysis of Si 1*s* spectra









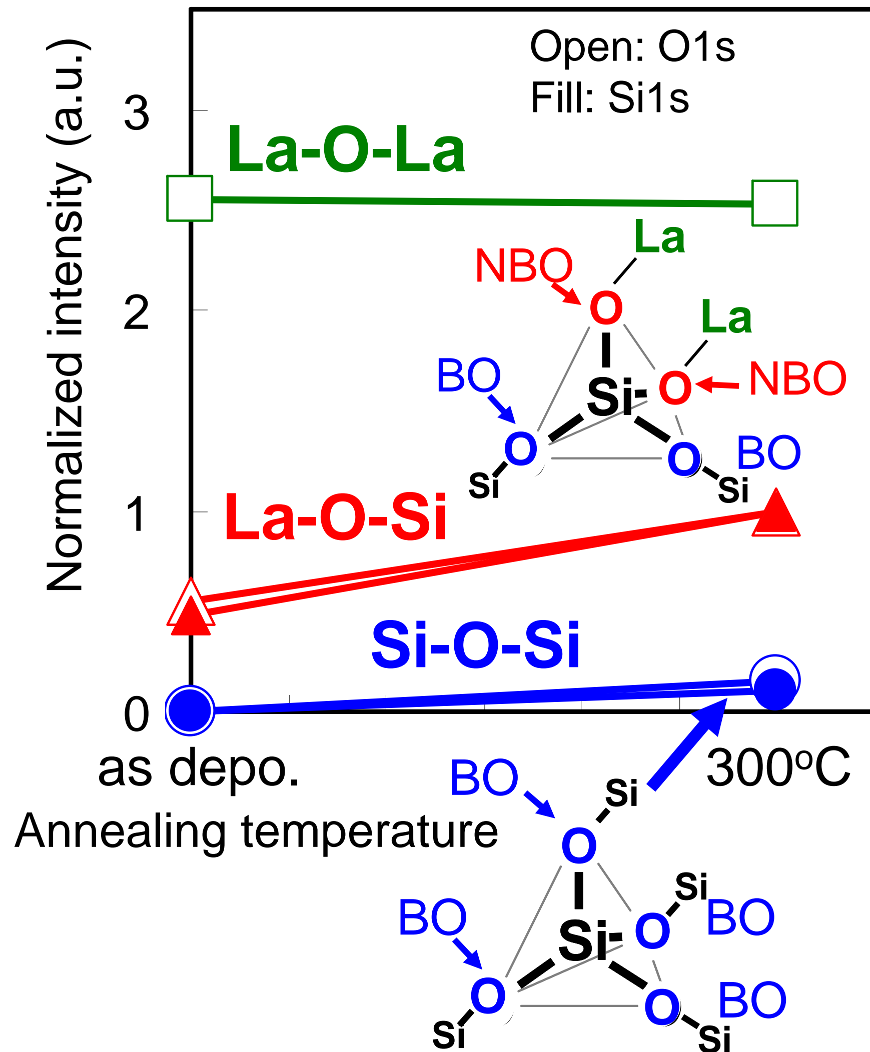
Distinguish
SiO_4:BOx4 and SiO_4:*n*NBO (*n*=1~3)

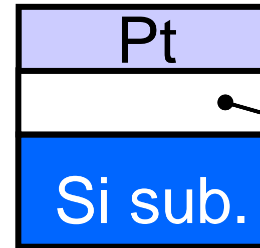
O 1*s* spectra：the amount of BOs and NBOs

Si 1*s* spectra: the amount of SiO_4 with four BOs

the amount of SiO_4 with NBO(s)

Determination of oxygen sites after annealing





samples
- as-depo.
- 300°C 5min

After annealing at 300°C

O1s

Increase in NBO(La-O-Si)

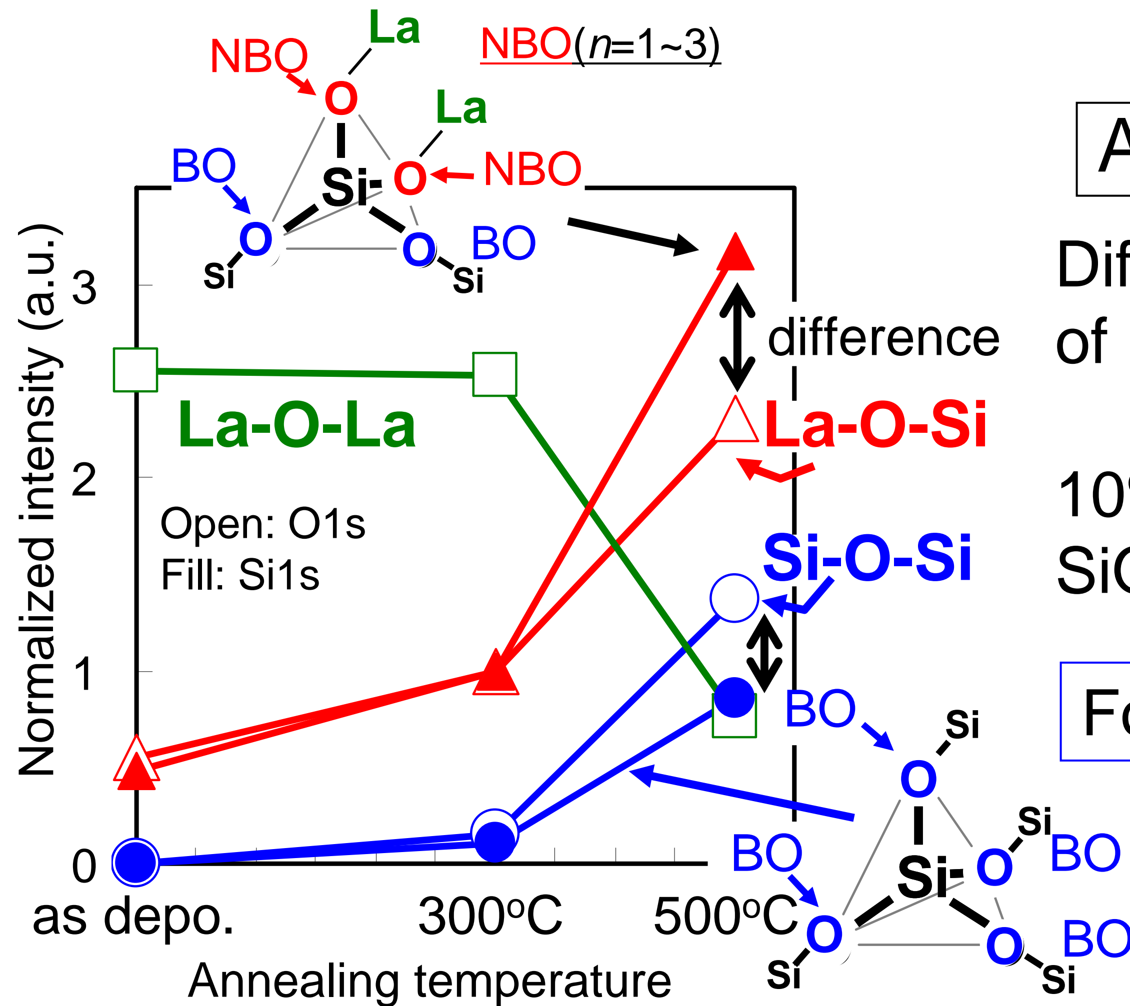
Si1s

Same increase amount of SiO_4:nNBO

→formation of La-rich silicate

K. Kakushima, et al., J. Appl. Phys., **104**, 104908 (2009)

Formation of Si-rich silicate



Annealing at 500°C

Difference in the increase of NBO and SiO_4:nNBO

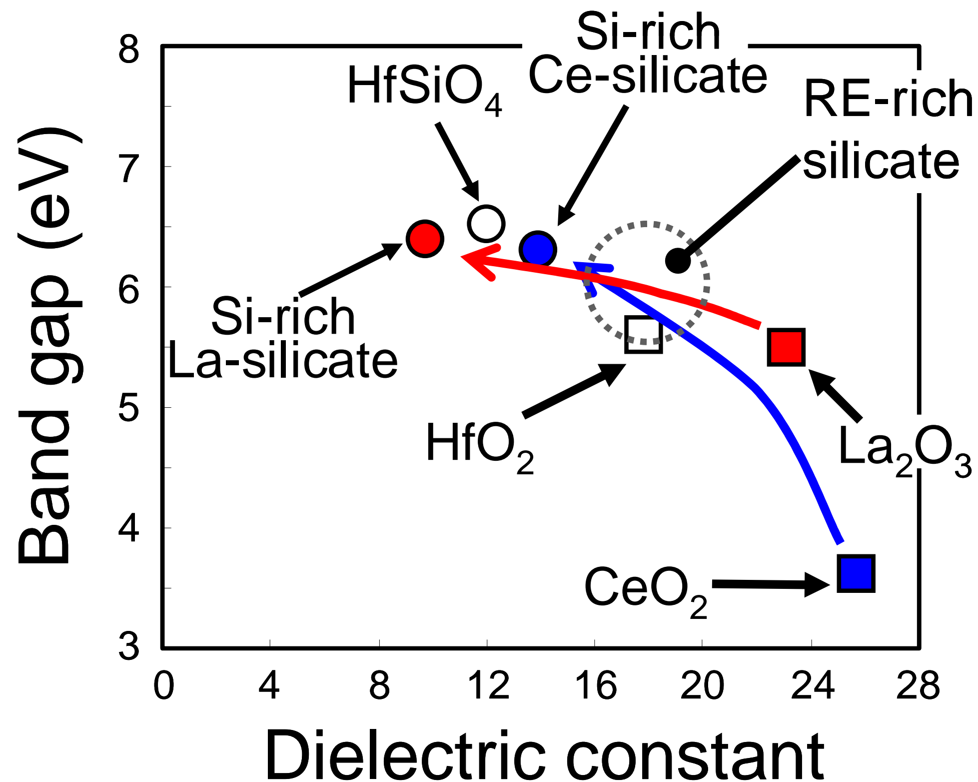
10% of the newly created SiO_4 is in SiO_4:BOx4 phase

Formation of Si-rich silicate

This method enables us to see the oxygen site in the newly created silicate

K. Kakushima, et al., J. Appl. Phys., **104**, 104908 (2009)

(7) Small-EOT with small-leakage current



- high *k*-value
- wide E_g

La_2O_3: k-value decreases with excess silicate reaction

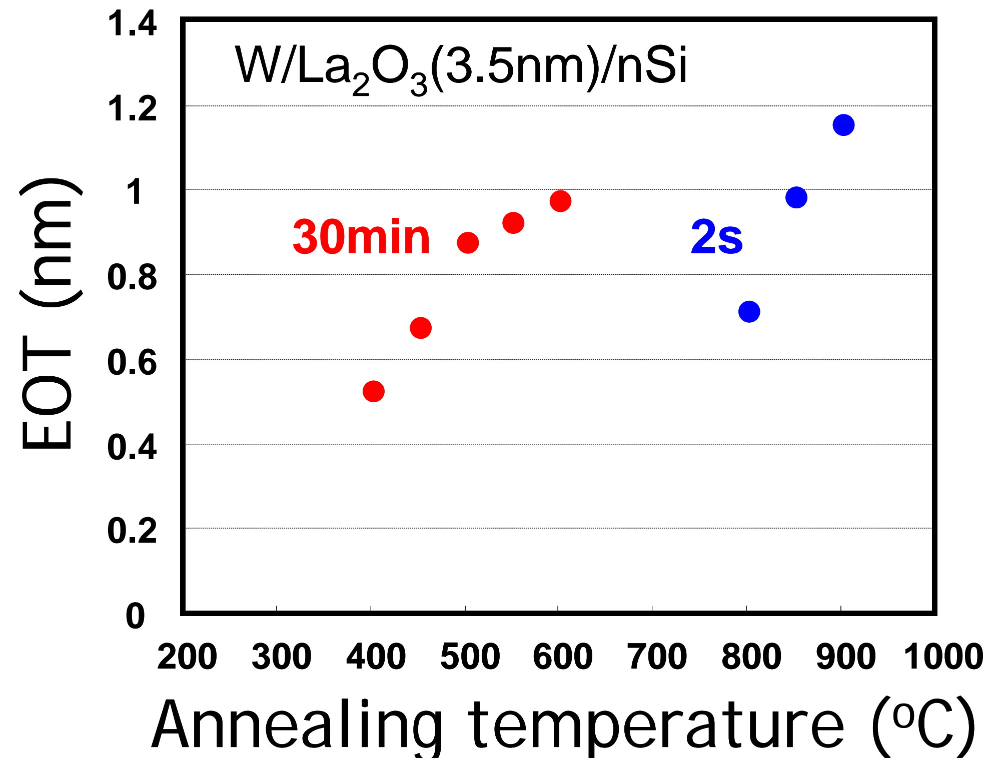
CeO_2: small E_g

→combination of La_2O_3 and CeO_2

Formation of rare earth-rich silicate with nice interface properties

Excess silicate formation with La_2O_3

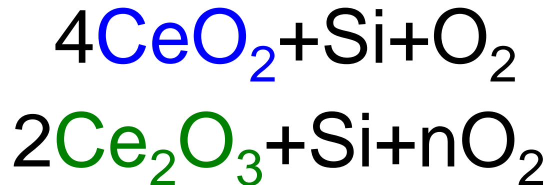
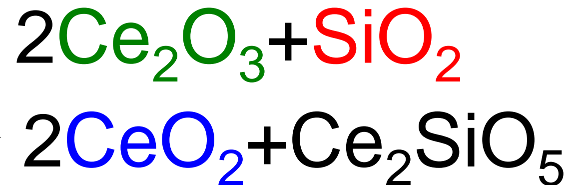
High temperature annealing promotes the reaction
→increase in the EOT



Annealing for short period before thermal equilibrium
→Suppression of the EOT increase

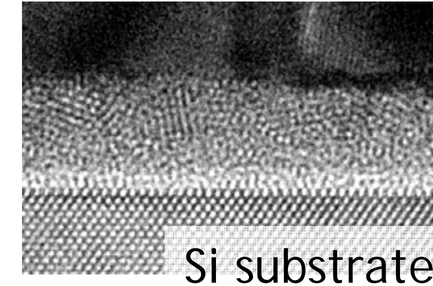
論文準備中

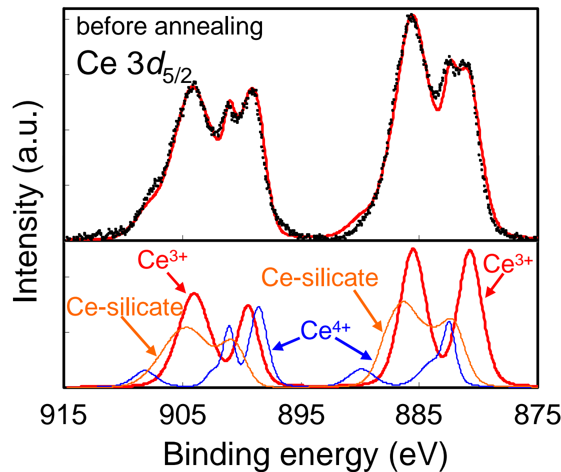
Issues in CeO_x

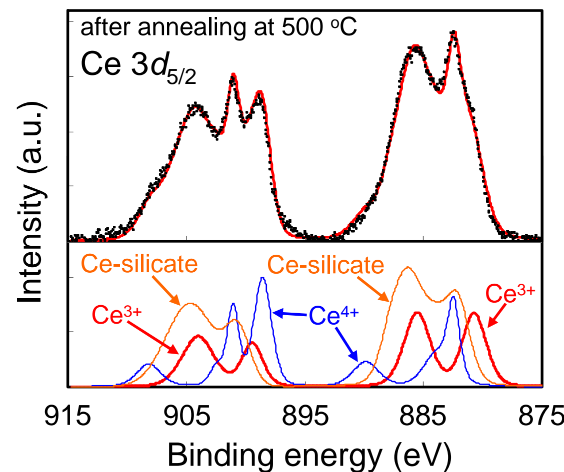
$$4CeO_2 + Si + O_2 \rightarrow 2Ce_2O_3 + SiO_2$$

$$2Ce_2O_3 + Si + nO_2 \rightarrow 2CeO_2 + Ce_2SiO_5$$





Ce_2O_3	CeO_2	silicate
47%	19%	34%



Ce_2O_3	CeO_2	silicate
26%	26%	48%

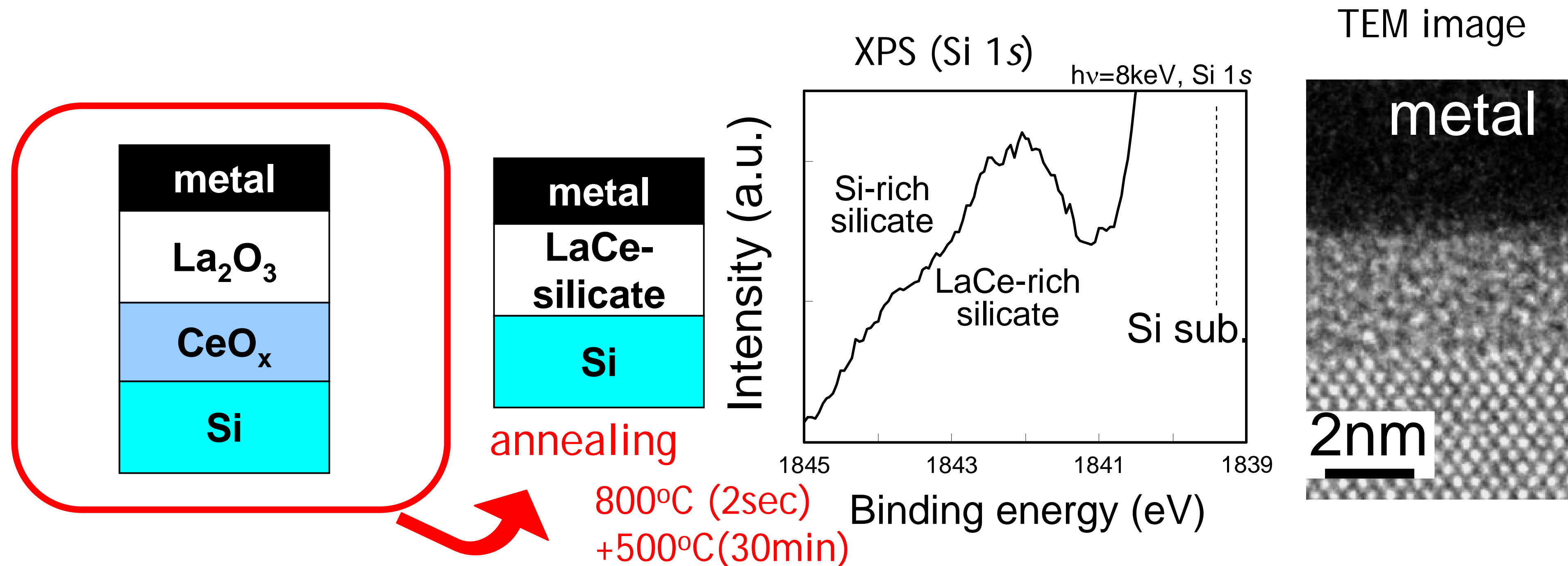
Valence number changes with annealing

Ce^{3+}, Ce^{4+} and silicate

CeO_2 within CeO_x forms SiO_2 as an interfacial layer

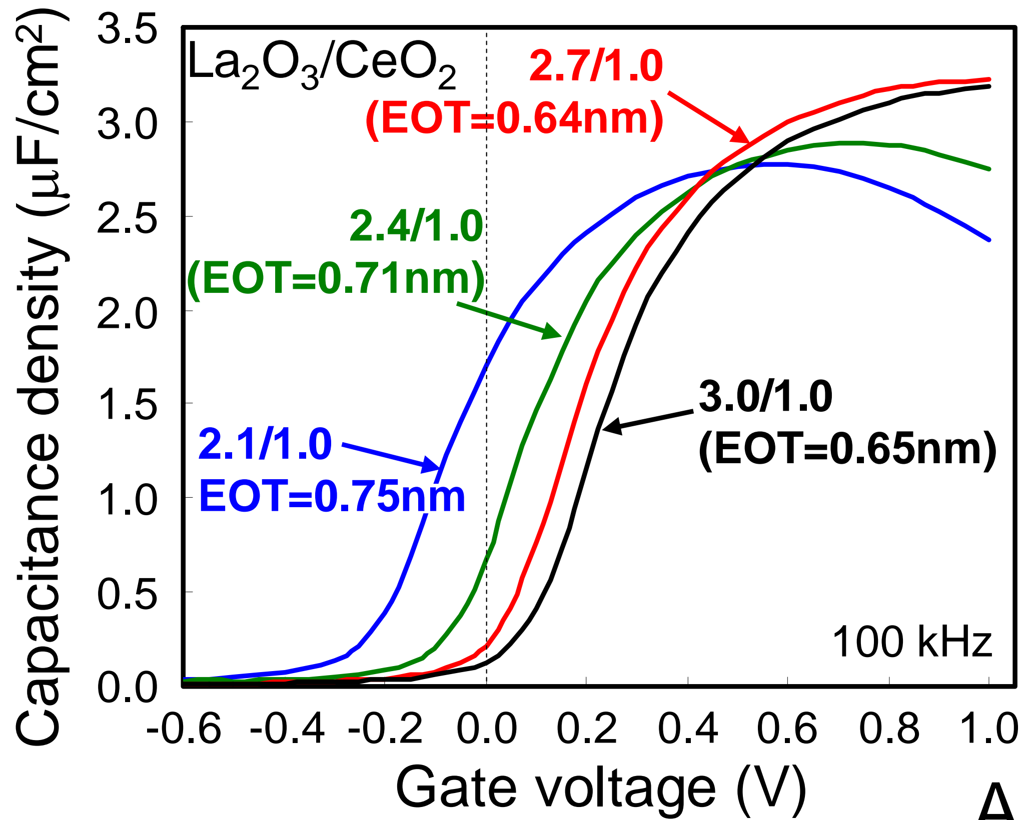
論文準備中

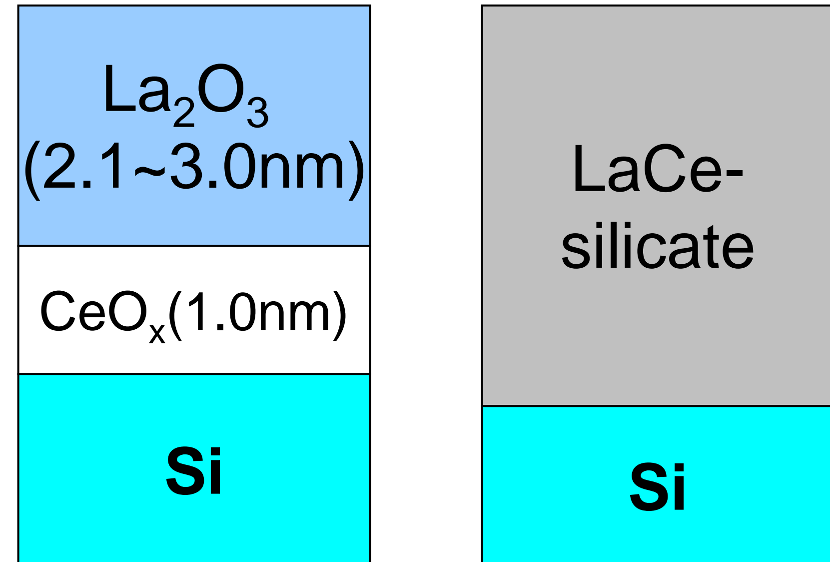
LaCe-silicate using La_2O_3 and CeO_x



- Intermixing of La, Ce and Si atoms with high temperature annealing
- Uniform LaCe-silicate with sharp interface

LaCe-silicate with different La concentration





Annealing condition

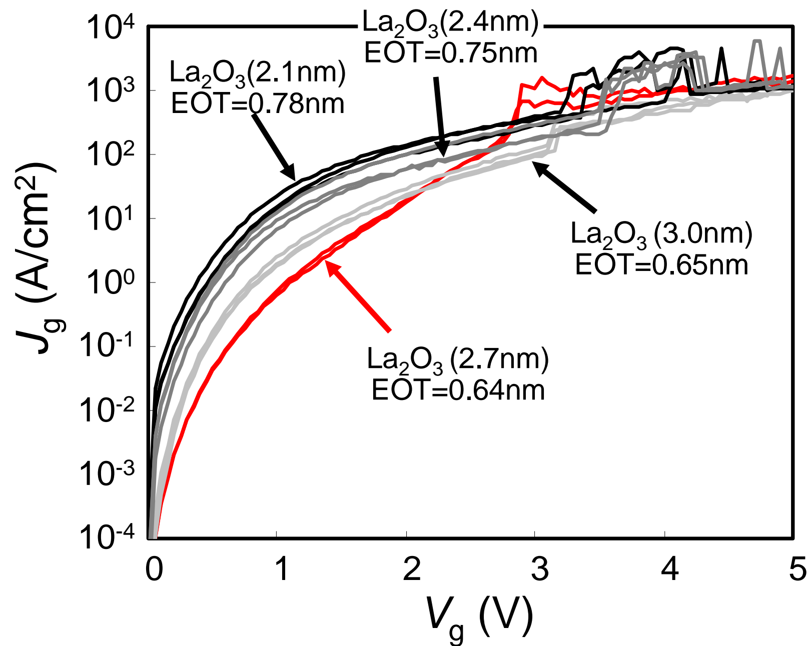
800°C(2sec)+500°C(30min)

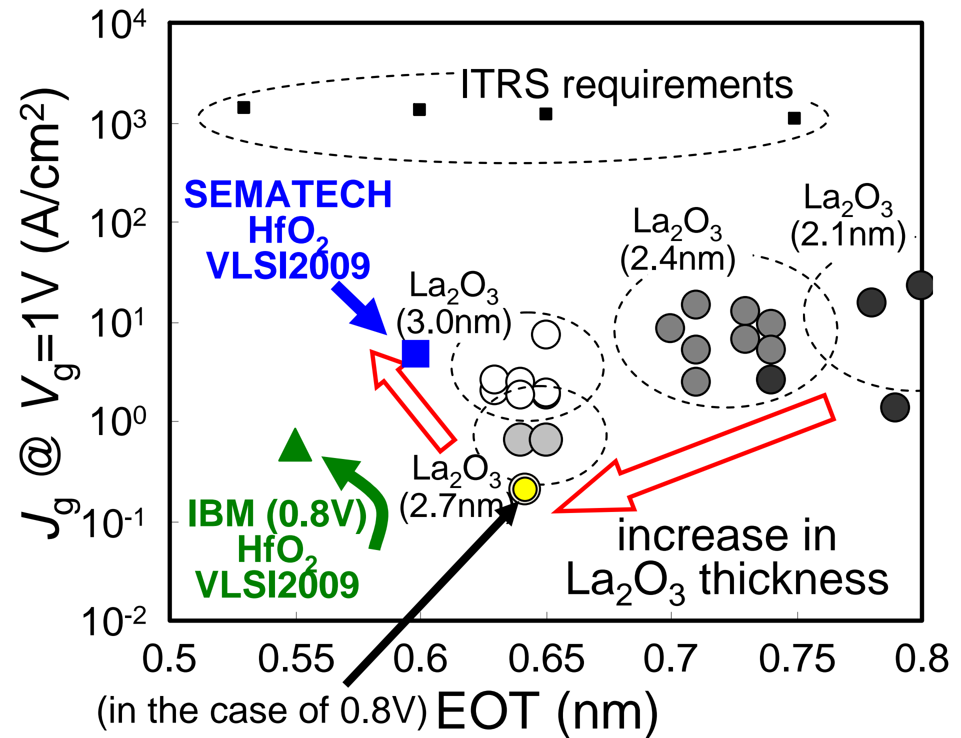
D_{it}~10^{11}cm^{-2}/eV

k-value of 17.4 with $La_{1.5}Ce_{0.5}SiO_5$

K. Kakushima.et al., VLSI symp. tech. 7.1 (2010)

Gate leakage current with LaCe-silicate



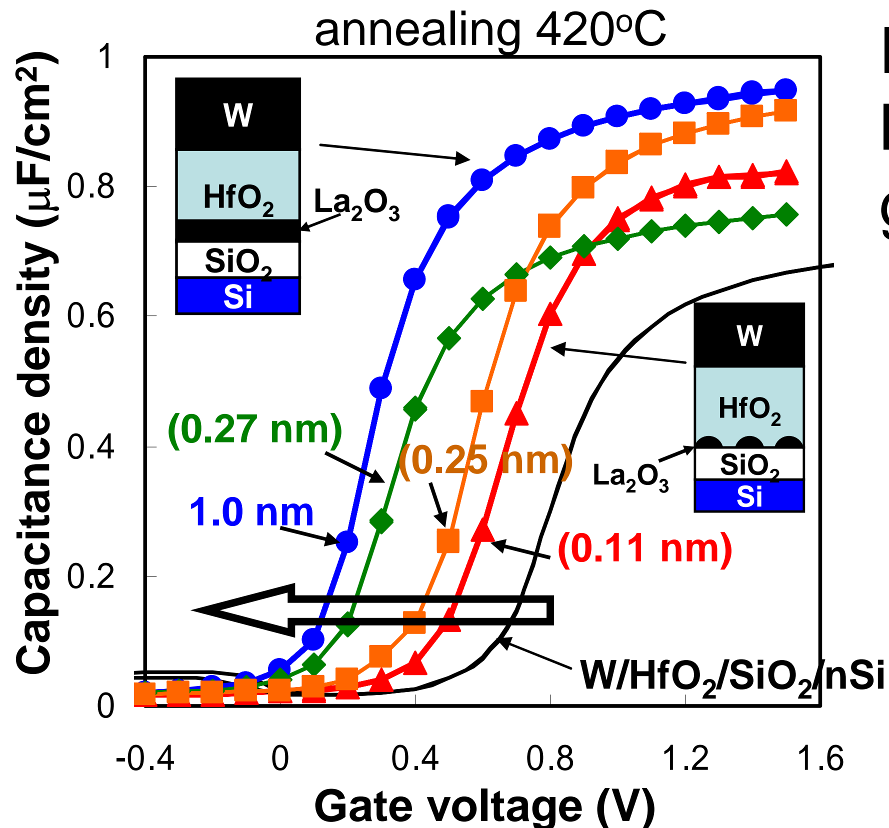


J_g=0.65A/cm^2 at EOT=0.64nm

(世界最小レベル)

K. Kakushima.et al., VLSI symp. tech. 7.1 (2010)

(8) Interface dipole at high-k interface



Incorporation of La atoms:
Negative flatband shift for HfO_2 gate dielectrics

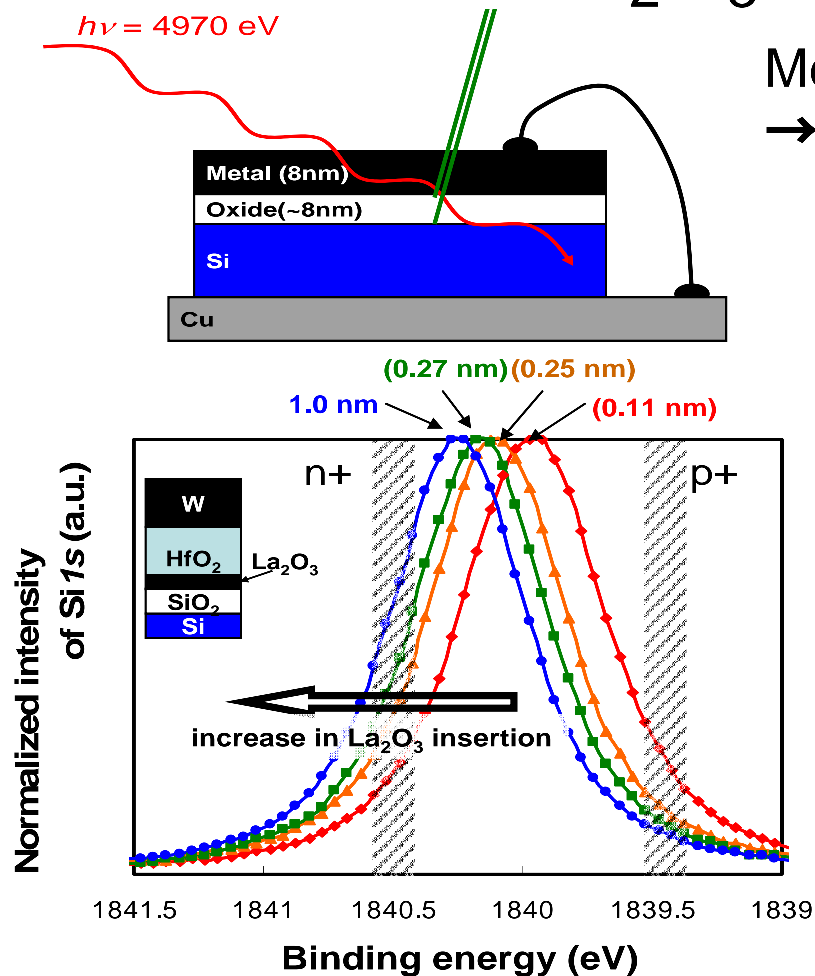
Reported mechanism

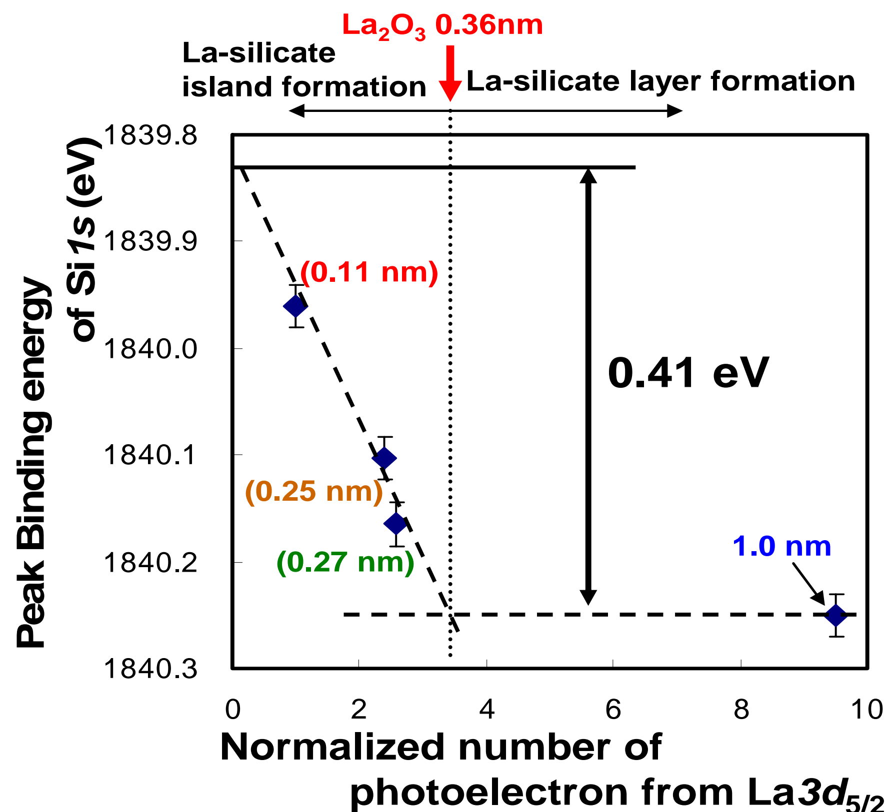
1. La capping on HfO_2
   X. Wang, VLSI symp. tech. 2006
2. La concentration in $HfLaO_x$
   Y. Yamamoto, SSDM 2006

The amount of La atoms at HfO_2/SiO_2 determines the Vfb
An interface dipole at high-k/SiO_2

Binding energy shift of the substrate with the amount of La_2O_3 insertion

Measurement with XPS
→No influence of Dit

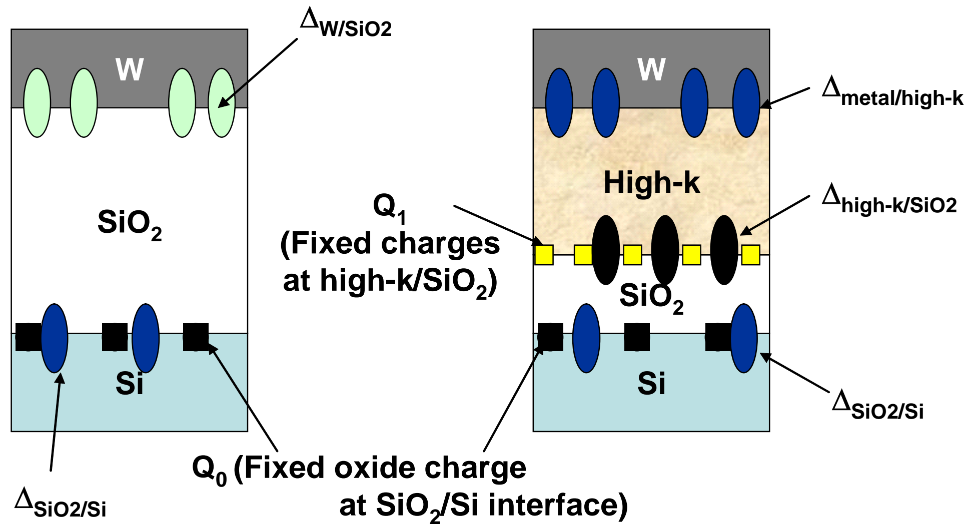


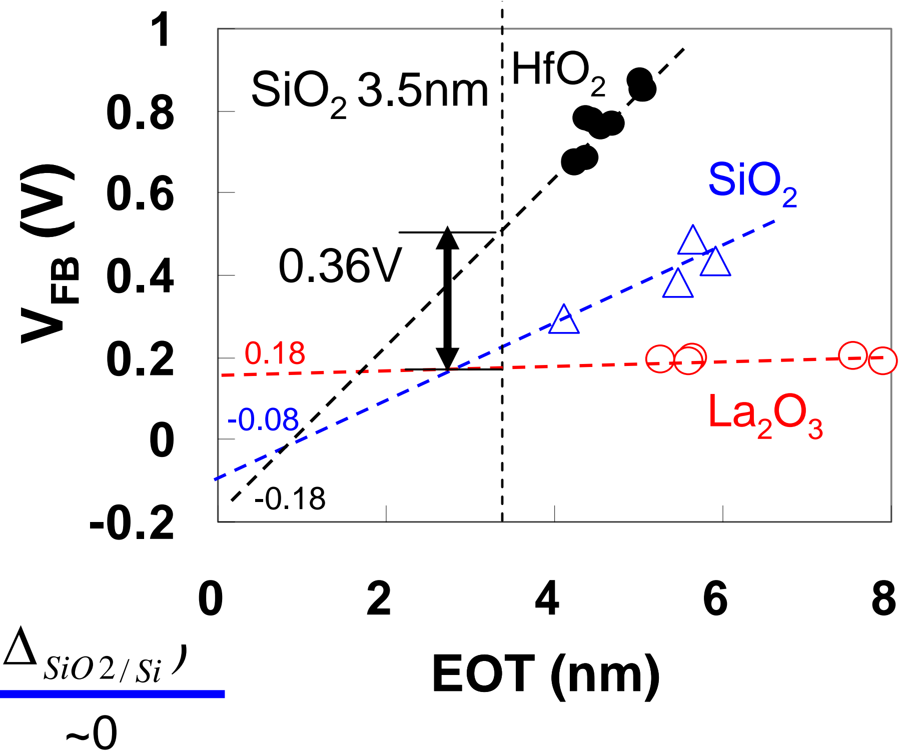


- Direct observation of the band bending of the substrate
- The amount of La atoms at High-k/SiO_2 determines the V_{FB}

K. Kakushima, et al., Appl. Surf. Sci., **254**, 6106 (2008)

Dipole extraction from $HfO_2/SiO_2/Si$ and $La_2O_3/SiO_2/Si$





Metal/SiO_2/Si

$$V_{FB} = -EOT\left(\frac{Q_0}{\varepsilon_0 \varepsilon_{ox}}\right) + \frac{\varphi_{ms}}{q} + (\Delta_{metal/SiO2} + \Delta_{SiO2/Si})$$

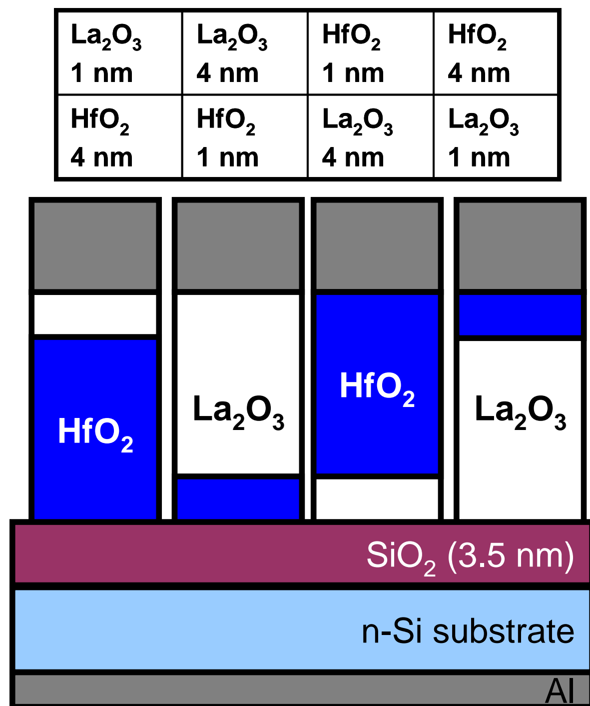
~0

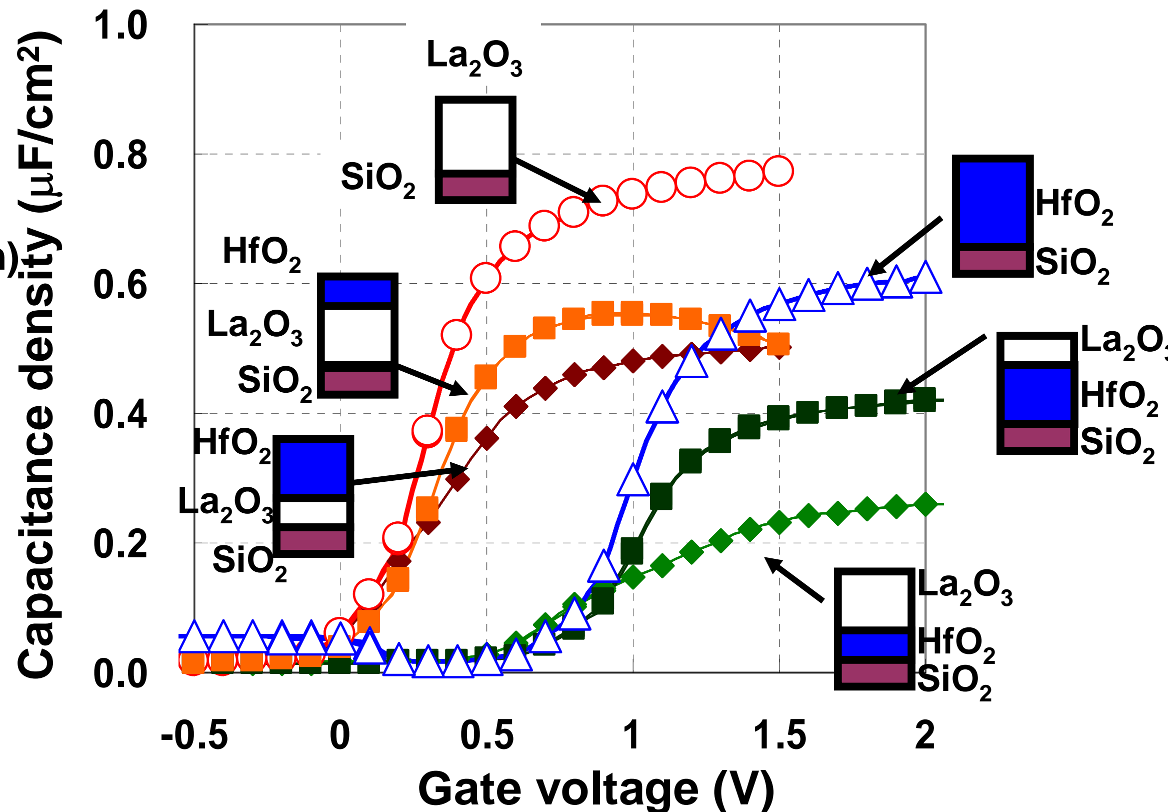
Metal/high-k/SiO_2/Si

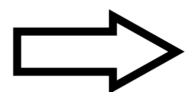
$$V_{FB} = -EOT\left(\frac{Q_0 + Q_1}{\varepsilon_0 \varepsilon_{ox}}\right) + \frac{Q_1 \cdot EOT_{IL}}{\varepsilon_0 \varepsilon_{ox}} + \frac{\varphi_{ms}}{q} + (\Delta_{metal/high-k} + \Delta_{high-k/IL} + \Delta_{IL/Si})$$

$(\Delta W/HfO_2 + \Delta HfO_2/SiO_2) - (\Delta W/La_2O_3 + \Delta La_2O_3/SiO_2) = 0.36$ V

Dipole at metal interface：W/HfO_2, W/La_2O_3







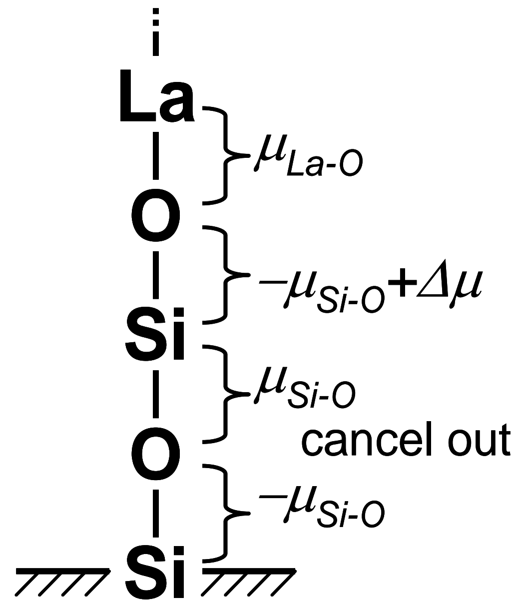
ΔW/HfO_2=ΔW/La_2O_3

⇨ $\Delta HfO_2/SiO_2$-$\Delta La_2O_3/SiO_2$=0.36 V

No difference at metal interface

→ High-k/SiO_2 is the reason for V_{FB} shift

Modeling of the interface dipole



μ: dipole moment

(electronegativity)×(bonding length)

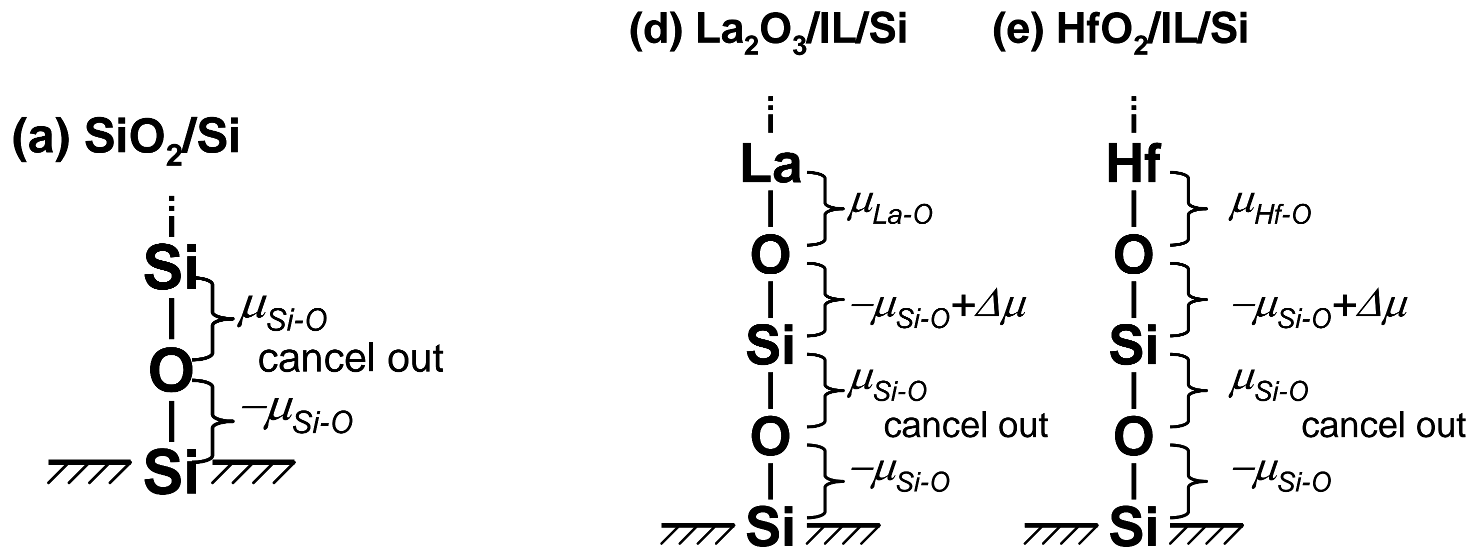
$$\mu_{all}=2/3\mu_{La\text{-}O}-2/4\mu_{Si\text{-}O}+\Delta\mu$$

Valence number of O and Si — O and Si — Second neighbor of O and SiO molecule

$$=2/3\times0.604-2/4\times0.246+0.141$$
$$=0.169\ (nm)$$

Definition of dipole moment for electron transfer

Estimation of V_{FB}



	calculation	μ_{all}	V_{FB} (V)
(a) SiO_2/Si	$1/2\mu_{Si\text{-}O}-1/2\mu_{Si\text{-}O}$	0	0.40
(d) La_2O_3/SiO_2	$2/3\mu_{La\text{-}O}-1/2\mu_{Si\text{-}O}+\Delta\mu$	0.169	0.08
(e) HfO_2/SiO_2	$1/2\mu_{Hf\text{-}O}-1/2\mu_{Si\text{-}O}+\Delta\mu$	-0.023	0.44

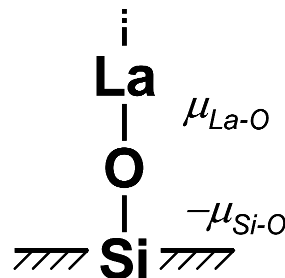
0.36V

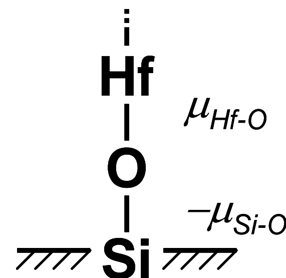
$$V_{FB}=\eta\mu_{all}+\phi_{ms} \qquad \phi_{ms}=0.4\ \text{eV}$$

$\eta=-1.87$ using experimentally deduced 0.36V

Estimation of V_{FB} for direct high-k/Si

(b) La_2O_3/Si **(c) HfO_2/Si**





$$V_{FB}=\eta\mu_{all}+\phi_{ms}$$

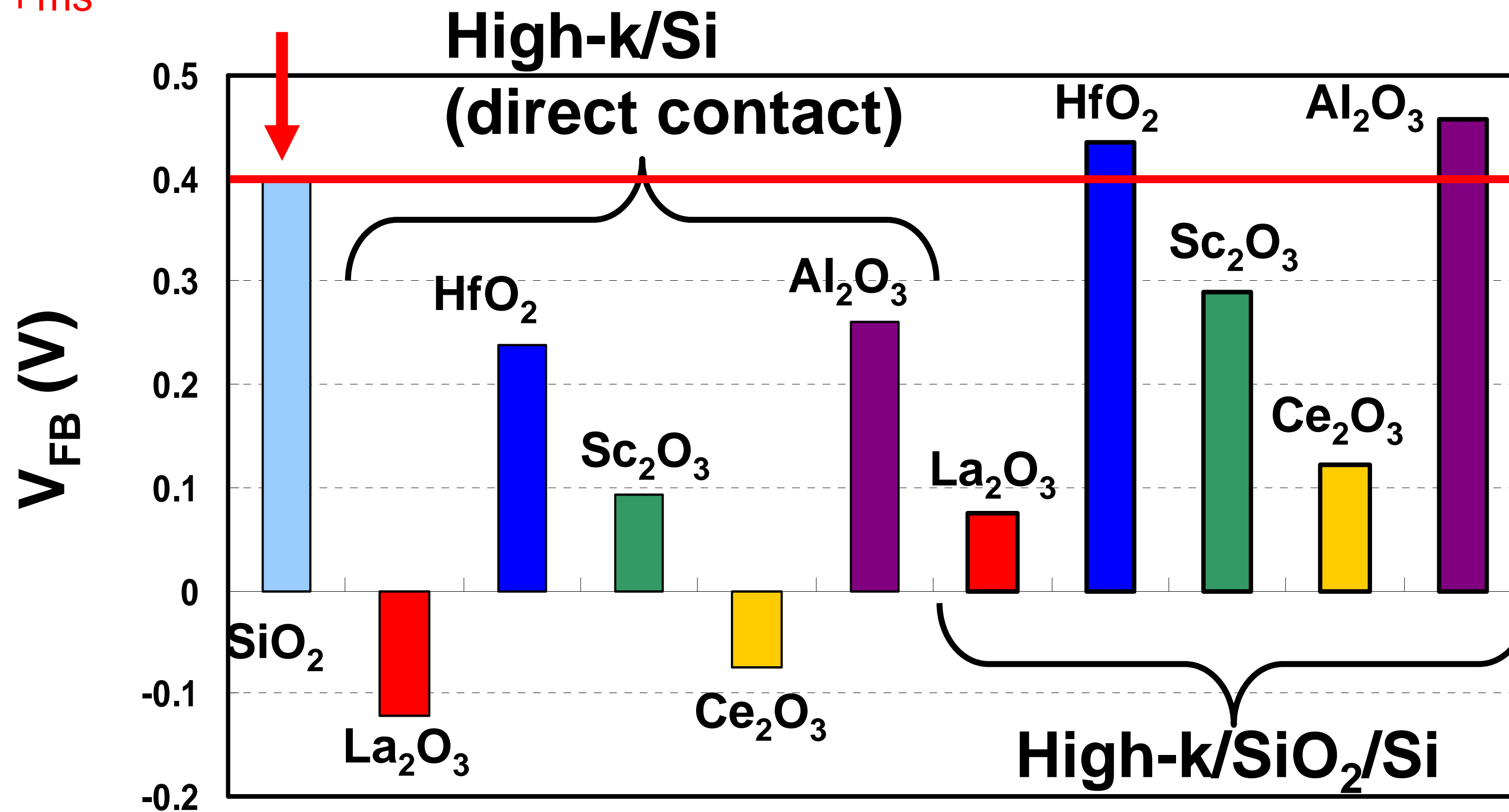
$\eta=-1.87$ $\phi_{ms}=0.4$ eV

	calculation	μ_{all}	estimation V_{FB} (V)
(b) La_2O_3/Si	$2/3\mu_{La\text{-}O}-1/2\mu_{Si\text{-}O}$	0.279	-0.12
(c) HfO_2/Si	$1/2\mu_{Hf\text{-}O}-1/2\mu_{Si\text{-}O}$	0.087	0.24

Proposed model can predicts the V_{FB} even with direct contact of high-k/Si

K. Kakushima, et al., Solid-State Electron., **52**, 1280 (2008)

V_{FB} estimation on wide materials

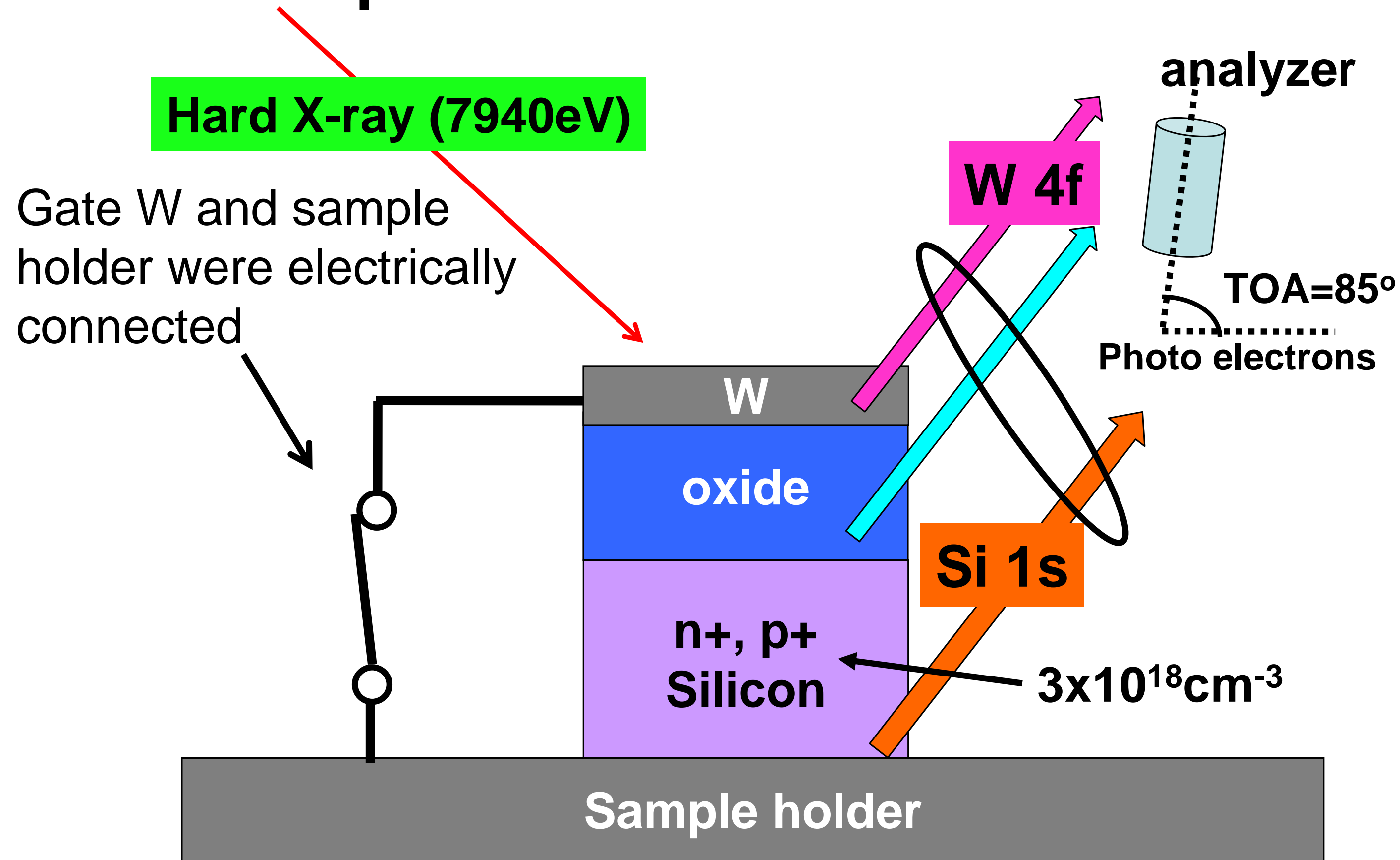


Measured and modeled V_{FB}

Oxide	Measured V_{fb}(V)	Modeled V_{fb} (V)	EOT (nm)
SiO_2	0.38	0.40	5.46
La_2O_3	-0.13	-0.12	1.15
HfO_2	0.34	0.24	0.90
Sc_2O_3	0.18	0.09	1.40
Ce_2O_3	-0.04	-0.07	1.11

A fairly nice mode to predict the V_{FB}

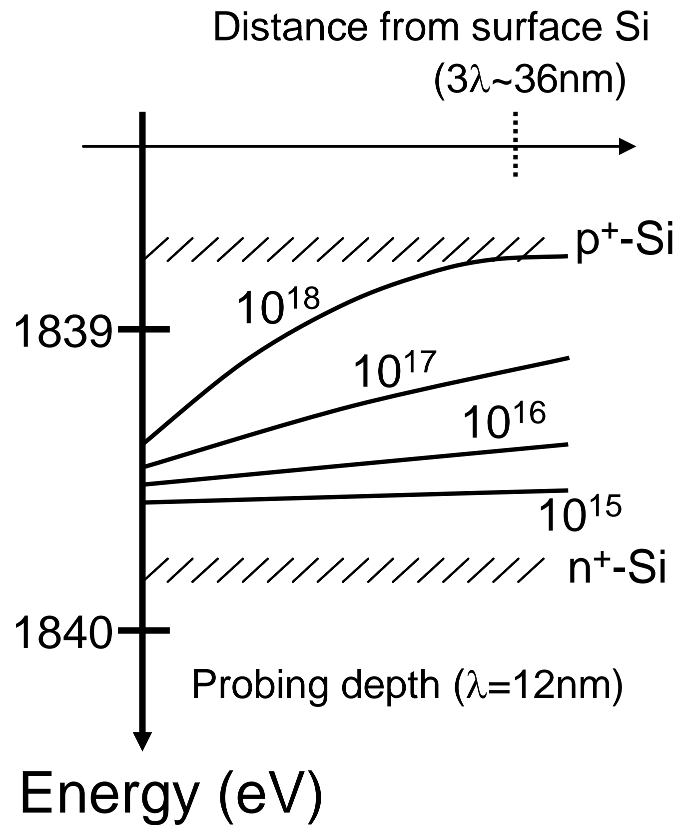
Interface dipole measurement with XPS

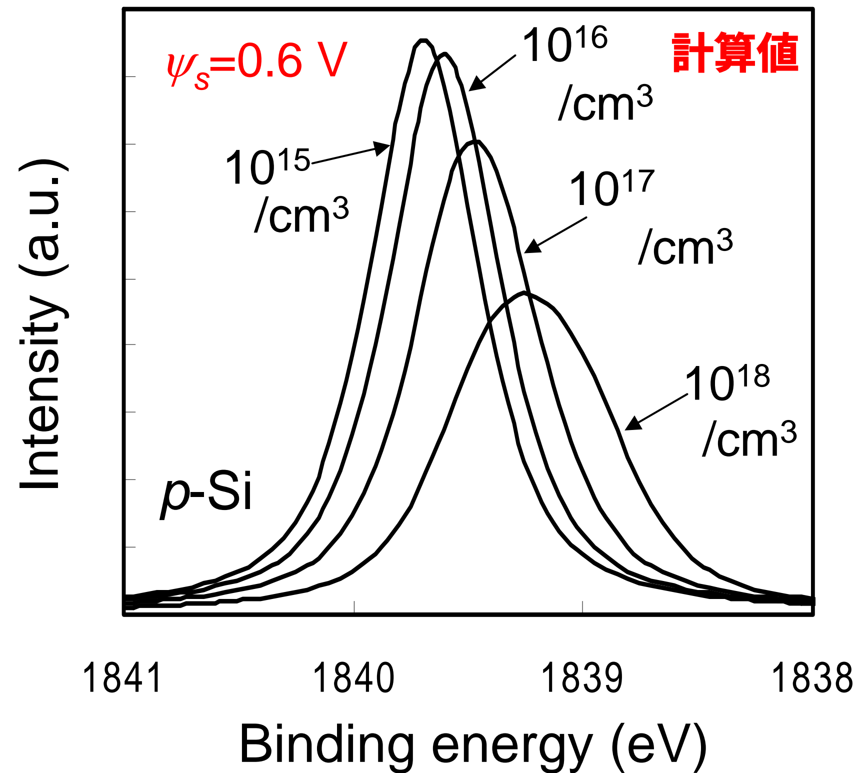


Fermi level of metal and Si are fixed to the ground potential

No influence of Dit

An example of Si 1s XPS spectra on different doping





$$\psi(z) \approx \psi_s \left(1 - \sqrt{\frac{qN_b}{2\varepsilon_{Si}\psi_s}} \cdot z \right)^2$$

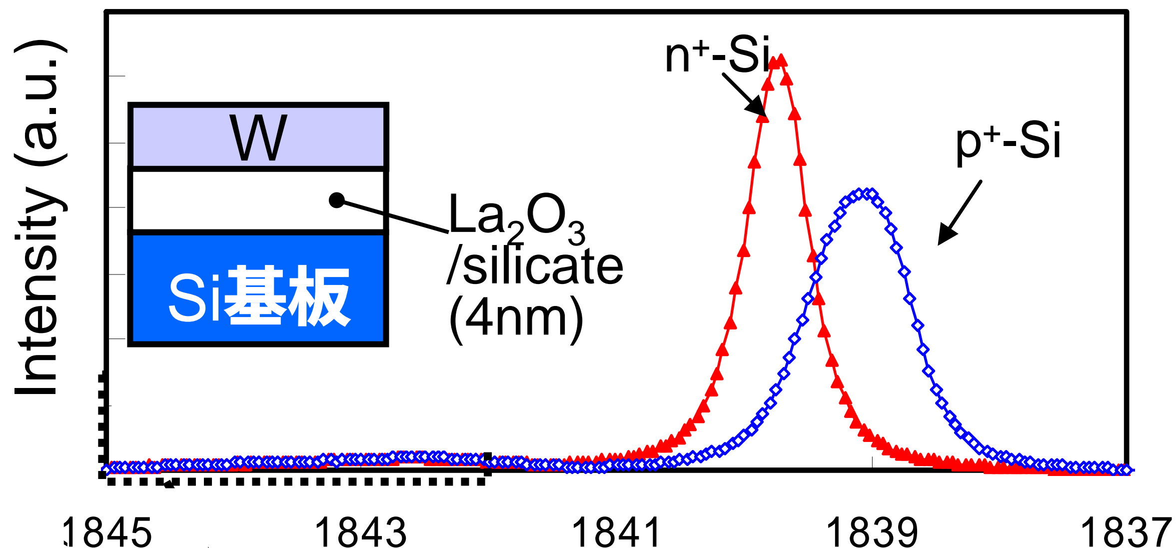
N_b: doping concentration
ψ_s: surface potential

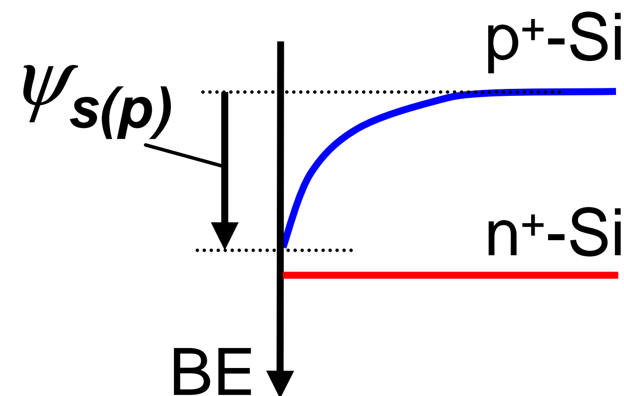
Spectra broadening due to band bending at surface

Extraction of surface potential

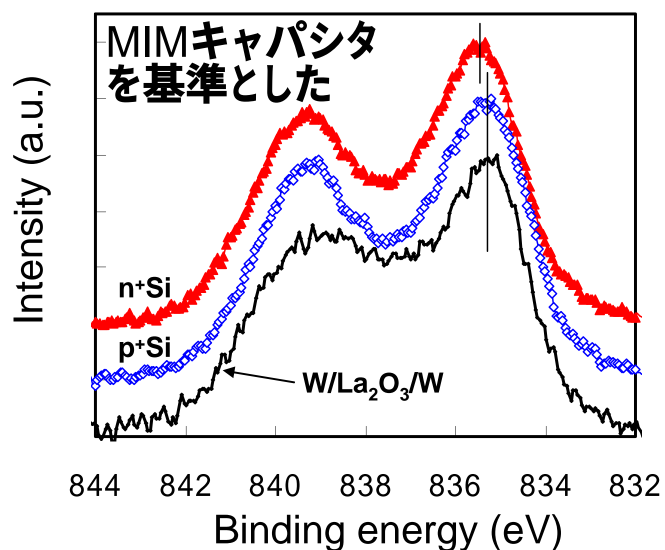
K. Kakushima, et al., J. Appl. Phys., **104**, 104908 (2008)

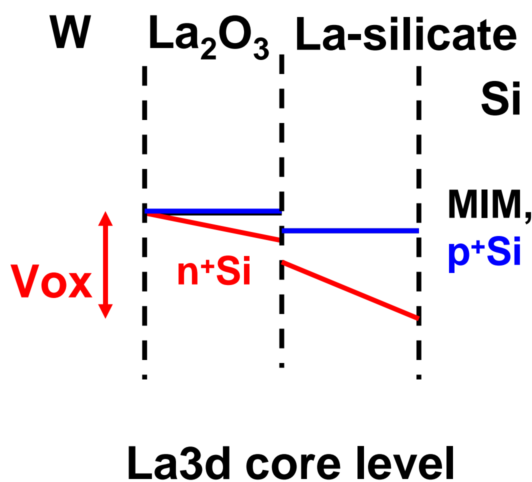
Quantitative estimation of interface dipole





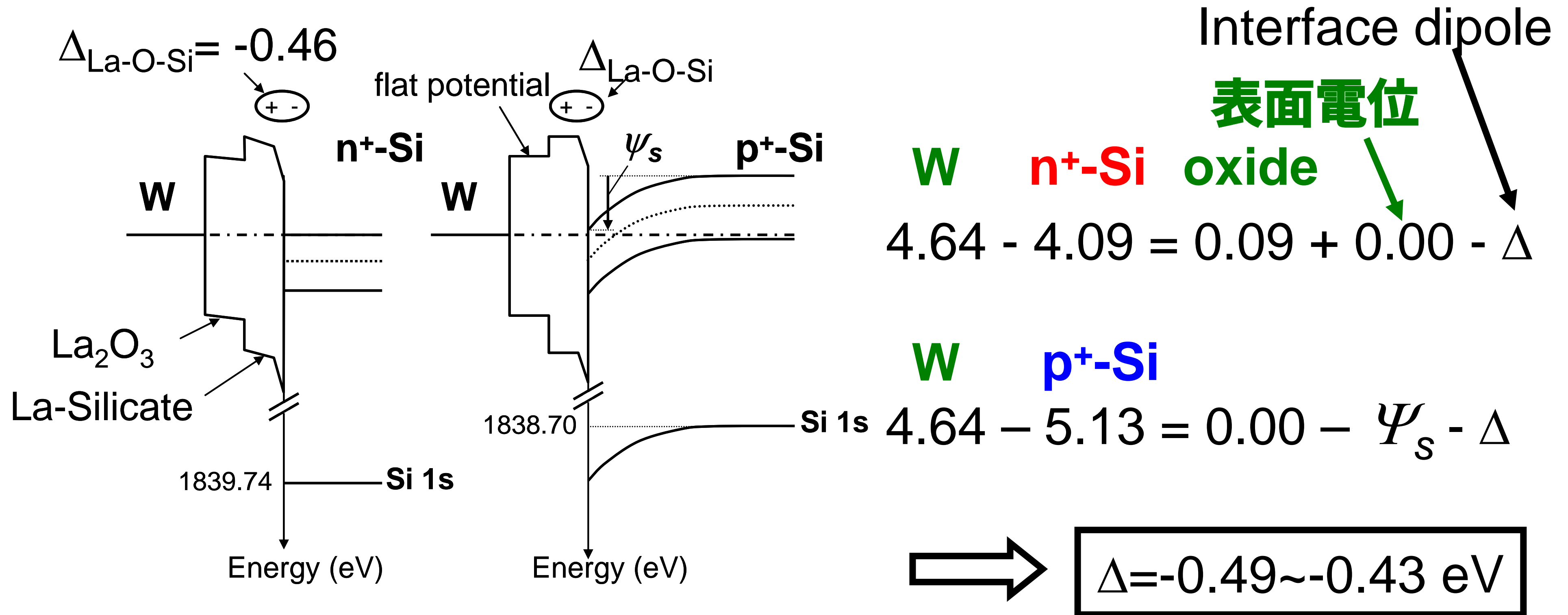
Surface potential extraction from Si 1*s*





Voltage in the oxide from La3$d_{5/2}$ spectra

Band diagram of La_2O_3/La-silicate/Si

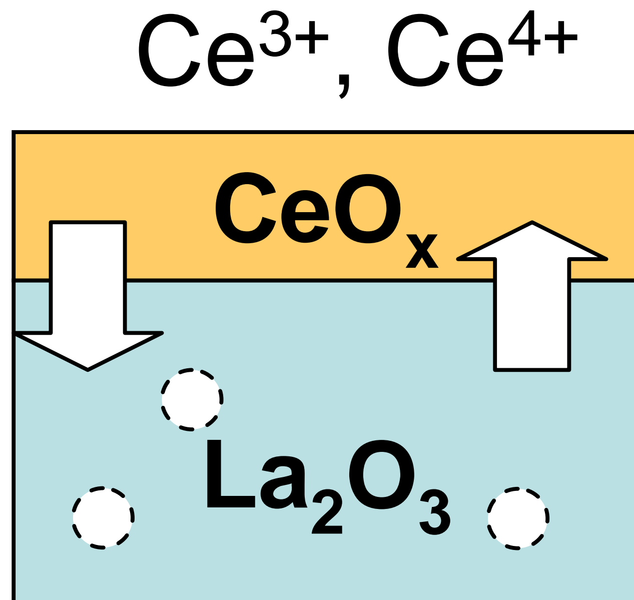


Dipole extracted from capacitors: -0.52 eV

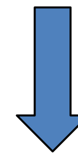
Good agreement with electrical measurements

(9) Defect compensation with CeO_x capping

Ce^{3+}, Ce^{4+}



Valence number changes to fix the oxygen partial pressure

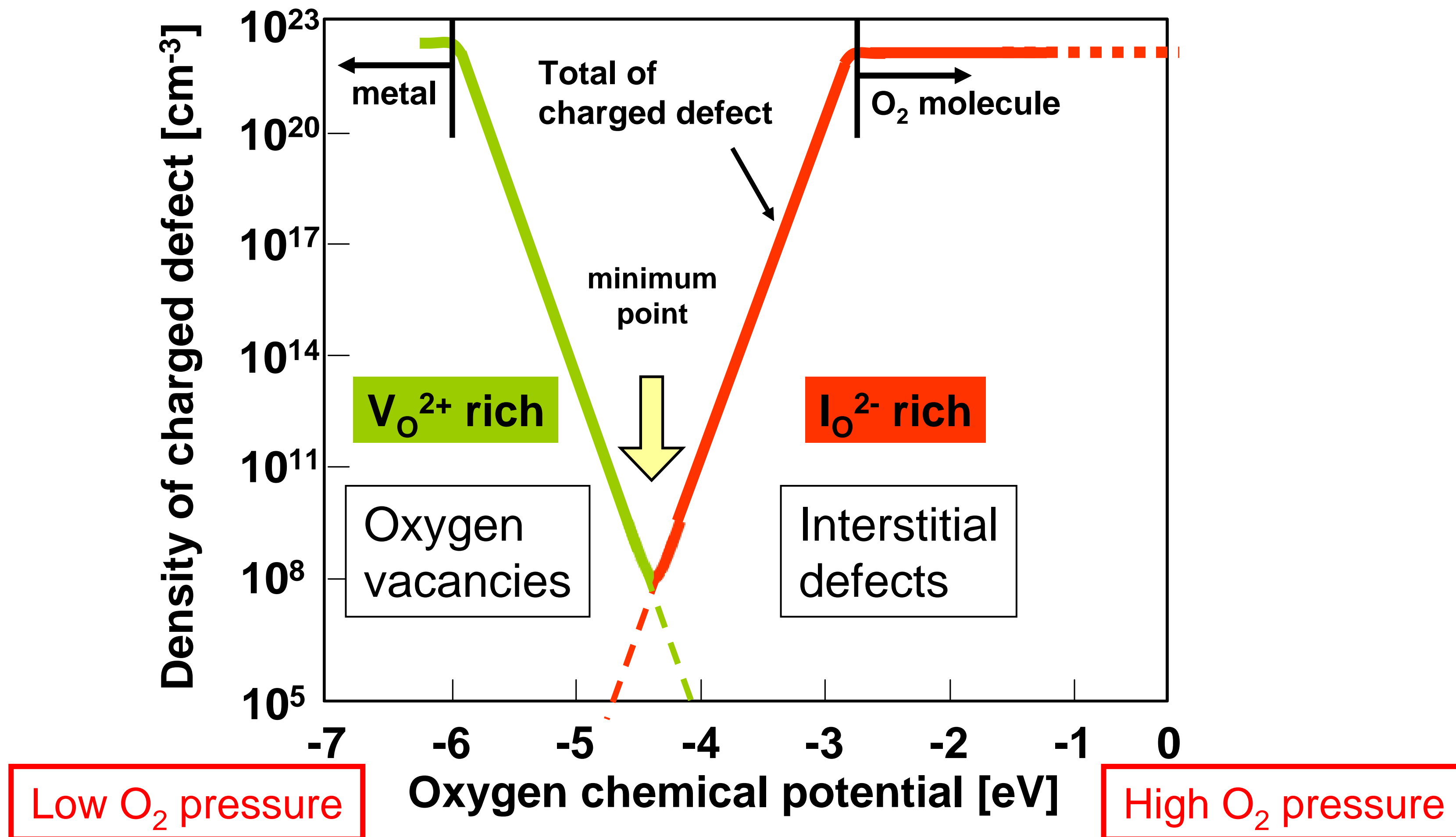


Keeps the defects in the La_2O_3 to a certain value

Control of the defect concentration with capping

→ recovery of μ_{eff} and V_{FB} shift

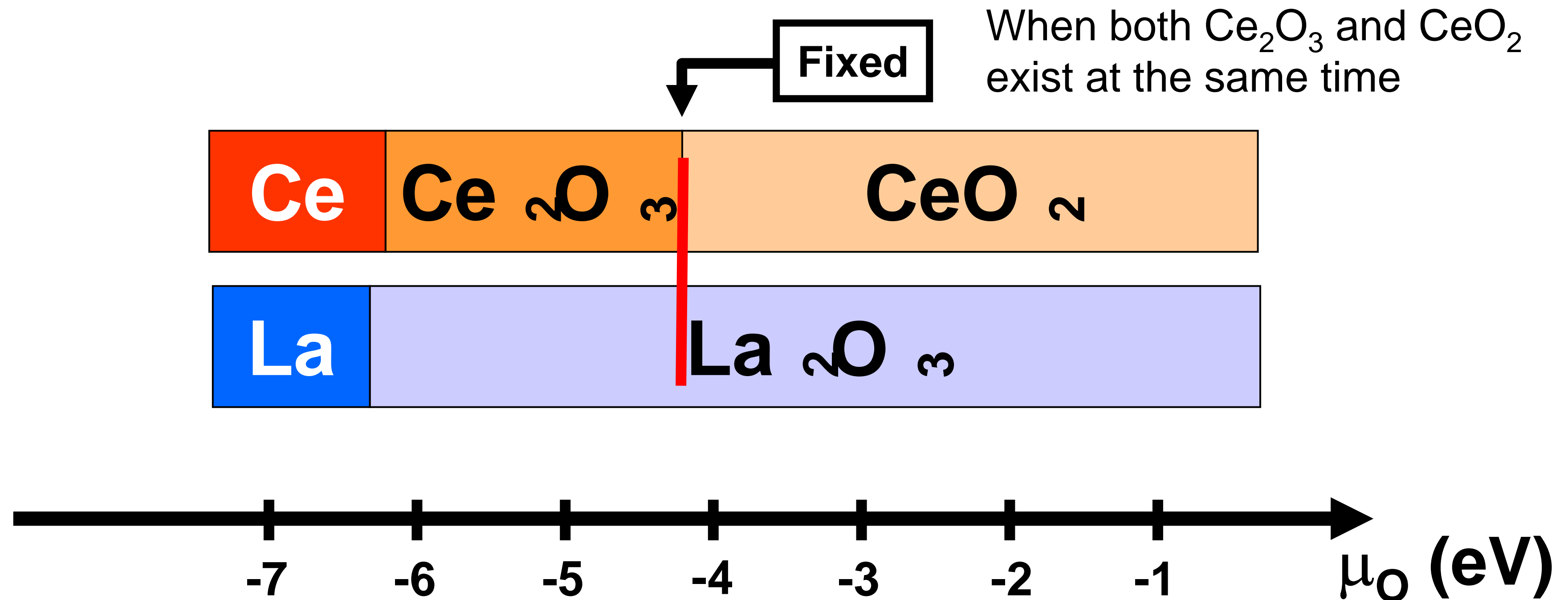
Theoretical study of the defects in La_2O_3



Smallest charged defect can be achievd atoxygen chemical potential of −4.2eV

M. Kouda, N. Umezawa, K. Kakushima, et al., VLSI symp. tech., 200 (2009)

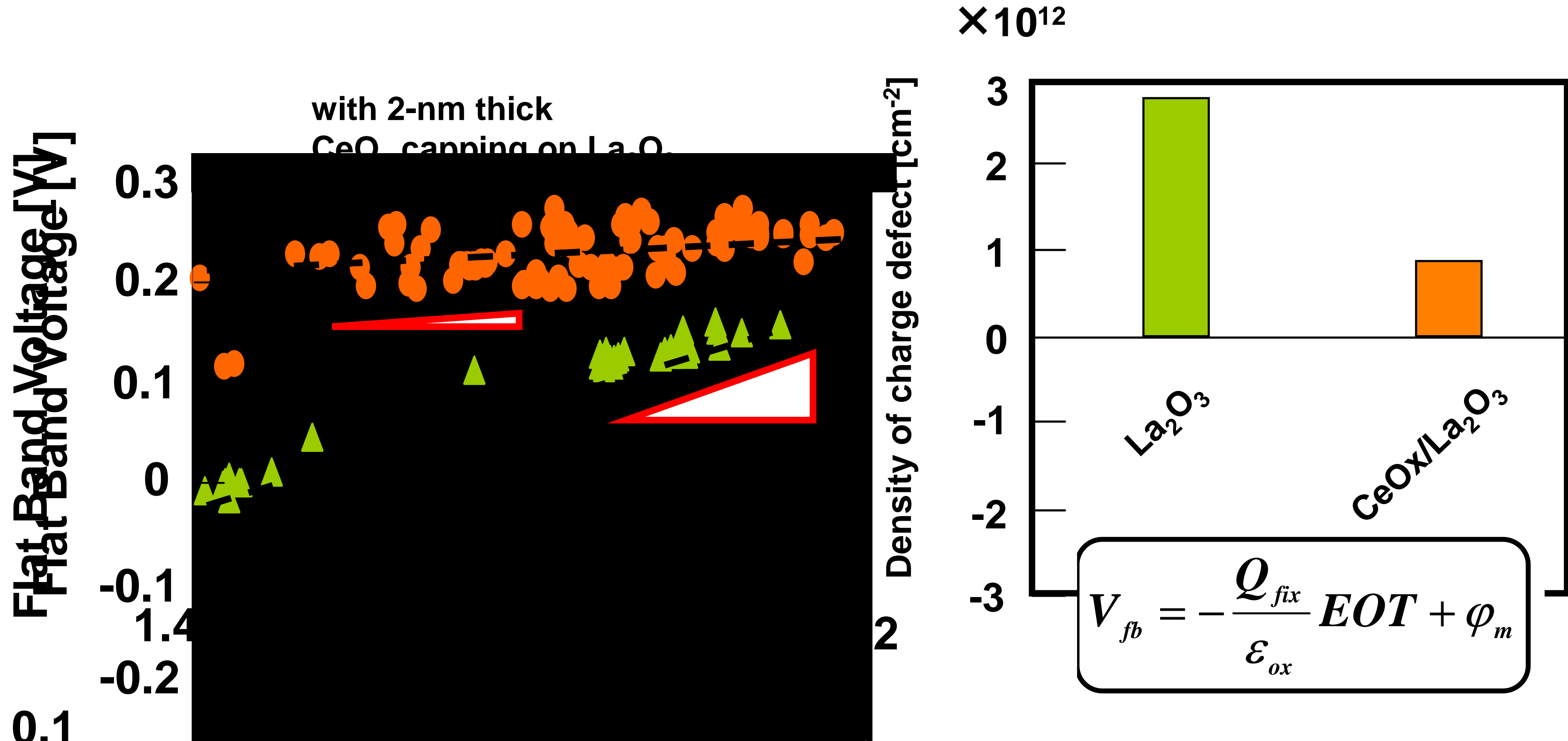
Fixation of the chemical potential with CeO_x



Adjacent high-k has the same chemical potential
CeO_x shows μ_O where smallest defects can be achieved with La_2O_3

M. Kouda, N. Umezawa, K. Kakushima, et al., VLSI symp. tech., 200 (2009)

Suppression of fixed charge with CeO_x capping

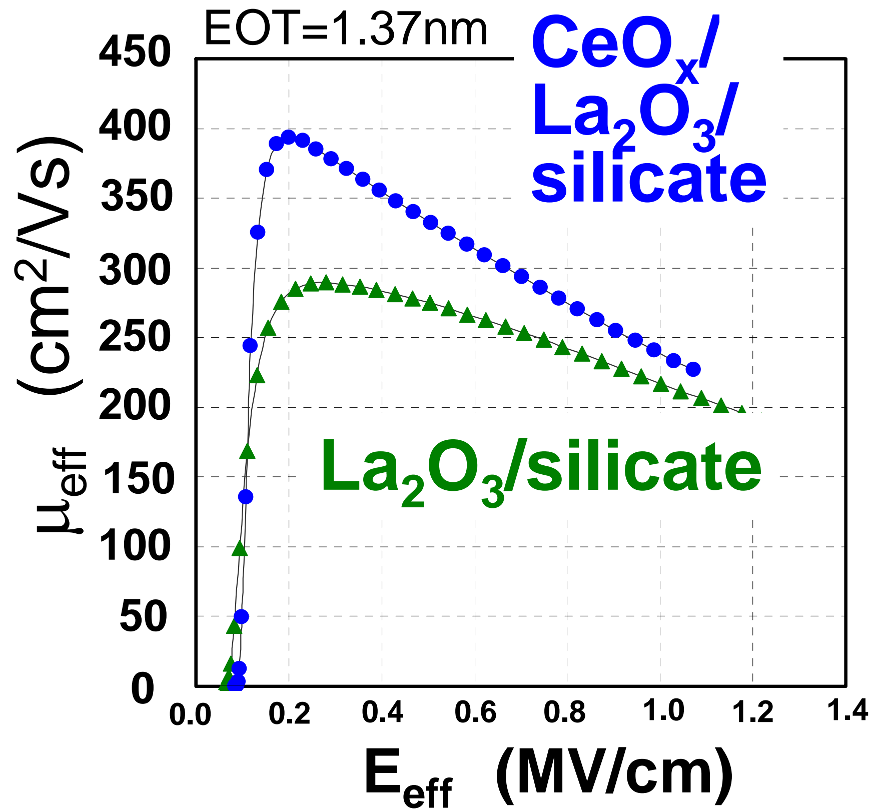


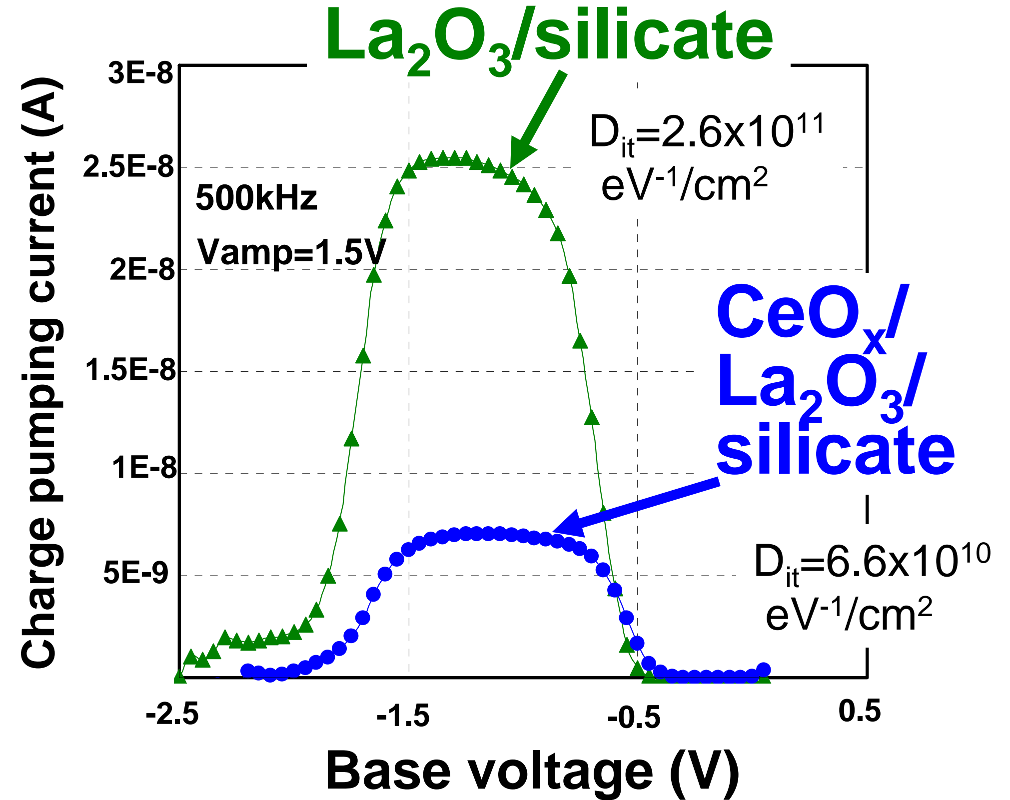
$$V_{fb} = -\frac{Q_{fix}}{\varepsilon_{ox}} EOT + \varphi_m$$

Fixed charge density reduction by 66%

M. Kouda, N. Umezawa, K. Kakushima, et al., VLSI symp. tech., 200 (2009)

μ_{eff} and D_{it} improvement with CeO_x capping





Improvement in the low field μ_{eff} and D_{it}

M. Kouda, K. Tachi, K. Kakushima, et al., ECS Trans., **16**, 153 (2008)