Si Nanoelectronic Device Technology

November 30, 2009

Hiroshi Iwai
Tokyo Institute of Technology
My research standing point and aim

Contribute to our human society through developing new electronic device technology.

Still our society does need the improvement of electronic device for power consumption and performance, as well as new function.
My research standing point and aim

Develop the technologies for which not many people are participating now, and which are very difficult and challenging, but which I believe to be the key and mainstream after 10 – 25 years.
For integrated circuit technology, there are still strong demands for decreasing power consumption, and increasing performance as you can see for center and also for your own PC.

What we can do from integrated circuit side?

Solution is not in so-called ‘beyond CMOS’ technology, but in the extension mainstream CMOS technology.

Extension of mainstream technology will take care the problems for another 20 years.
What I can contribute in the extension mainstream CMOS technology which will be realized in 25 years.

We selected challenging items.

1. High-k with EOT less than 0.5 nm
2. Si nanowire FET
3. Si nanowire FET
Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage between S and D

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

Good scaled I-V characteristics

Wdep $\propto \sqrt{V/Na}$

$K=0.7$ for example

$X, Y, Z: K, V: K, Na: 1/K$
Scaling down approach is very beautiful and important.

| 2 Generations scaling | k = 0.7² = 0.5 
if we keep the chip area the same for scaling |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Single MOFET</td>
<td>Vdd → 0.5</td>
</tr>
<tr>
<td></td>
<td>Lg → 0.5</td>
</tr>
<tr>
<td></td>
<td>Id → 0.5</td>
</tr>
<tr>
<td></td>
<td>Cg → 0.5</td>
</tr>
<tr>
<td></td>
<td>P (Power)/Clock</td>
</tr>
<tr>
<td></td>
<td>→ 0.5³ = 0.125</td>
</tr>
<tr>
<td></td>
<td>τ (Switching time) → 0.5</td>
</tr>
<tr>
<td>Chip</td>
<td>N (# of Tr) → 1/0.5² = 4</td>
</tr>
<tr>
<td></td>
<td>f (Clock) → 1/0.5 = 2</td>
</tr>
<tr>
<td></td>
<td>P (Power) → 1</td>
</tr>
</tbody>
</table>
- The concerns for limits of down-scaling have been announced for every generation.

- However, down-scaling of CMOS is still the ‘royal road’* for high performance and low power.

- Effort for the down-scaling has to be continued by all means.

---

* Euclid of Alexandria (325BC?-265BC?)
  ‘There is no royal road to Geometry’

Mencius (Meng-zi), China (372BC?-289BC?)
  孟子: 王道, 足道  (Rule of right vs. Rule of military)
- There will be still 4~6 generations left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

- Even after reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

- Two candidates have emerged for R & D
  1. Nanowire/tube MOSFETs
  2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.
Before reaching the scaling limit, we need to pursue the down scaling limit, introducing new materials such as (1) high-k.

Then, (2) Si-nanowire and (3) Alternative channel (III-V and Ge).

That is why I am concentrating the research of The above 3 – (1), (2), (3).
Random Variability Reduction Scenario in ITRS 2007

Planar Bulk & Poly-Si/SiON
$T_{inv}=2.5\,\text{nm}$
$N_A=3\times10^{18}$

Planar Bulk & Metal/High-k
$T_{inv}=1.8\,\text{nm}$
$N_A=1.5\times10^{18}$

Assumption: Random dopant fluctuation is the main source of Random Variability. Line width roughness of $L_g$ and $W_g$ is not considered in this study.

Source: 2007 ITRS Winter Public Conf.
EOT (Equivalent gate oxide thickness) is supposed to saturate at 0.5

Saturation of EOT thinning is a serious roadblock to proper down-scaling → short-channel effect & Vth variation

Is 0.5nm real limit?
High-k for Further Scaling

SiO\textsubscript{x} interfacial layer (typ.0.5~0.7nm)

SiO\textsubscript{2} interfacial layer inserted or re-grown for
- recovery of degraded mobility
- interface state, reliability (TDDB, BTI), etc.

- SiO\textsubscript{2}-IL free structure (direct contact of high-k/Si)
  is required for EOT=0.5nm

- EOT scaling is expected down to 0.5 nm in ITRS

ITRS2007

Bulk

DG

Year

2007 2012 2017 2022

EOT (nm)

2007 2012 2017 2022

Scaling in EOT

Hf based oxide

High-k

excess gate leakage

× limit

Si
**SiO\(_x\)-IL growth at HfO\(_2\)/Si Interface**

**Phase separator**

\[
\text{HfO}_2 + \text{Si} + \text{O}_2 \rightarrow \text{HfO}_2 + \text{Si} + 2\text{O}^* \rightarrow \text{HfO}_2 + \text{SiO}_2
\]

Oxygen supplied from W gate electrode

D.J. Lichtenwalner, Tans. ECS 11, 319

H. Shimizu, JJAP, 44, pp. 6131

**SiO\(_x\)-IL is formed after annealing**

Oxygen control is required for optimizing the reaction
La-Silicate Reaction at $\text{La}_2\text{O}_3$/Si

Direct contact high-k/Si is possible

$\text{La}_2\text{O}_3 + \text{Si} + n\text{O}_2 \rightarrow \text{La}_2\text{SiO}_5, \text{La}_2\text{Si}_2\text{O}_7, \text{La}_{9.33}\text{Si}_6\text{O}_{26}, \text{La}_{10}(\text{SiO}_4)_6\text{O}_3$, etc.

La$_2$O$_3$ can achieve direct contact of high-k/Si
EOT < 0.5nm with Gain in Drive Current

14% of $I_d$ increase is observed even at saturation region

EOT below 0.4nm is still useful for scaling
Si nanowire FET with Semi-1D Ballistic Transport

Merit of Si-nanowire


Trade off

Carrier scattering probability

Small Large

# of quantum channel

Small Large

High Conduction (1D)

Go=77.8µS/wire

Multiple quantum channel (QC) used for conduction


Reduction in Ioff (Ids-leak)

Good control ofIds-leak by surrounding gate

Increase in Ion (Ids-sat)

High-density lateral and vertical integration

Merit of Si-nanowire


High-density lateral and vertical integration

Carrier scattering probability

Small Large

# of quantum channel

Small Large

High Conduction (1D)

Go=77.8µS/wire

Multiple quantum channel (QC) used for conduction

(a) A cross sectional TEM image of Si NW FET in this work. Oxide support still remains thanks to nanowire sidewall (SiN). Semi-Around gate structure, nearby 300 degree of whose channel is surrounded by gate oxide and poly-Si electrode. Schematic illustration is shown in upper-right.
$D_W=25\text{nm}$ and $D_H=35\text{nm}$.
Fairly nice $I_{on}/I_{off}$ ratio of $10^7$ with a low subthreshold slope of $71\text{mV/dec}$. has been obtained.
Effective electron mobility of [110]-directed multi channel Si NW FET in this work. (D_W=25nm, D_H=35nm)